

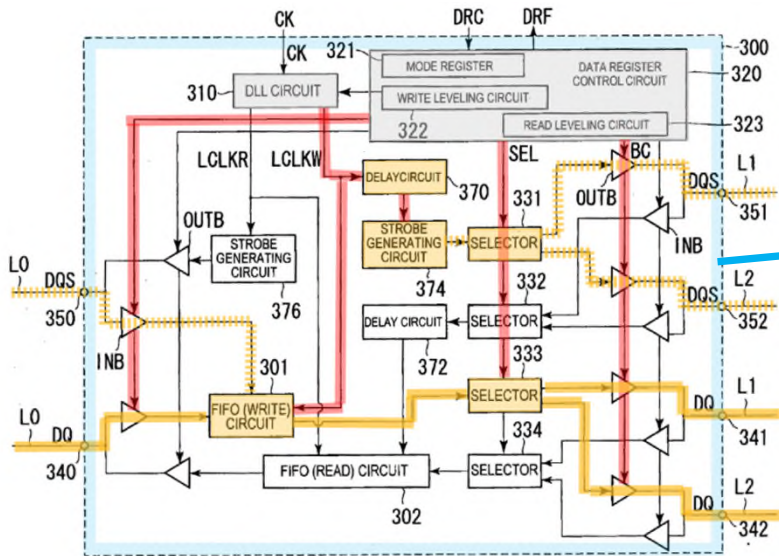
Hiraishi (EX1005)

FIG.5

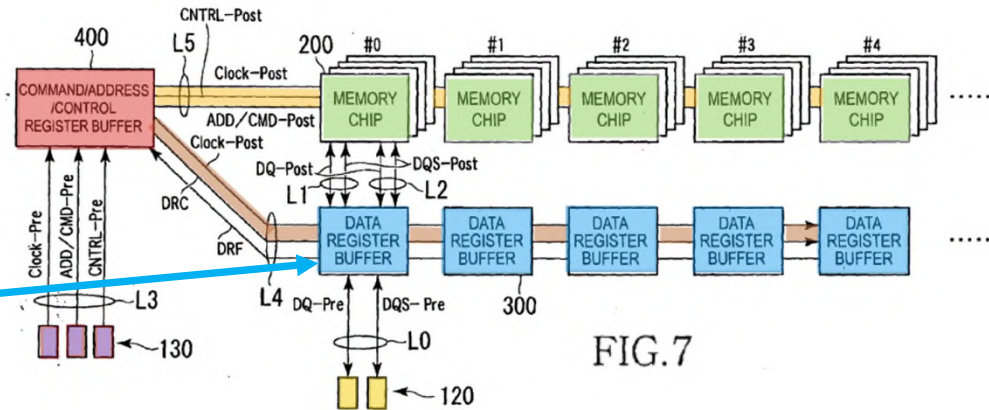


FIG.7

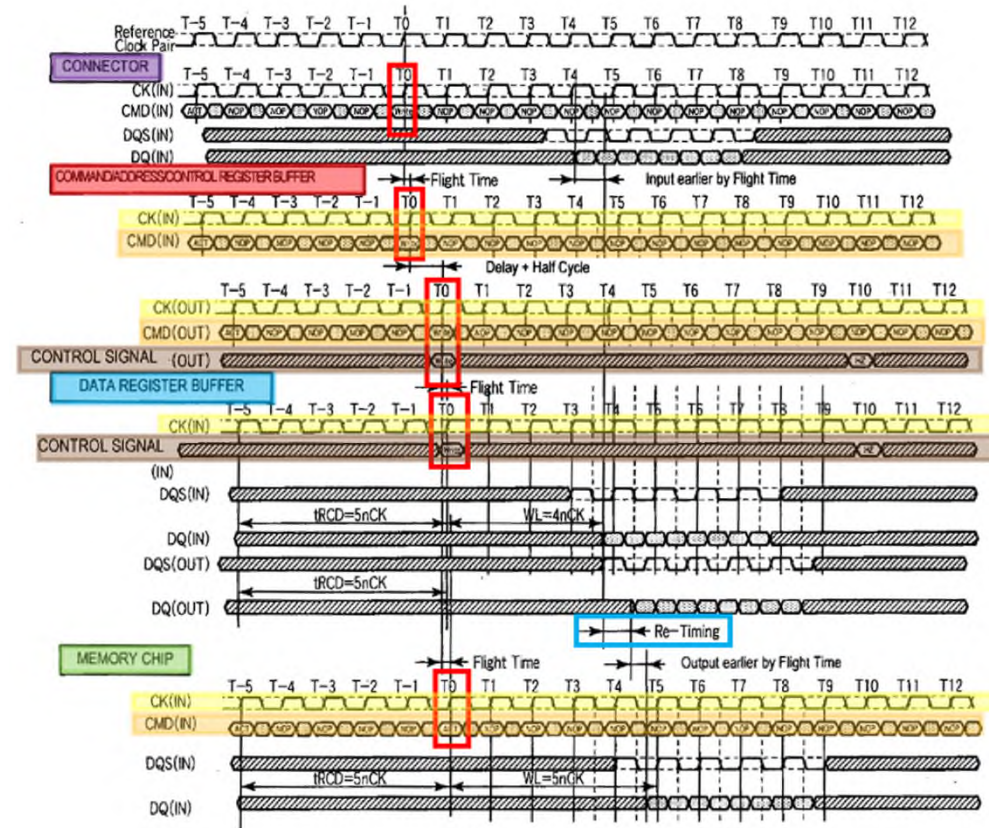


FIG.12

[0132] FIG. 12 is a timing chart for explaining the write operation of the memory module 100 according to the present embodiment.

[0133] In the write operation, the memory controller issues an active command ACT and a write command Write in order, and after a lapse of a write latency (WL) since the write command Write is issued, burst outputs write data. In the example shown in FIG. 12, the active command ACT reaches the command/address/control connectors 130 at the time T-5 that is synchronized with the clock signal CK, and the write command Write reaches the command/address/control connectors 130 at the time T0. In this example, WL=4, so that write data DQ is input to the data connectors 120 from a time T4.

[0134] Because a flow of the command is similar to that in the read operation shown in FIG. 11, redundant explanations will be omitted. The write data DQ reaching the data connectors 120 is input to the data register buffer 300. At this moment, there occurs a time difference (Flight Time) between a timing at which the write command reaches the command/address/control connectors 130 and a timing at which the write command (Direction Control) is input to the data register buffer 300. In consideration of this point, the memory controller outputs the write data DQ by delaying it by an amount equivalent to the Flight Time.

[0135] The data register buffer 300 loads the received write data DQ in the FIFO (Write) circuit 301 with a data strobe signal DQS that is delayed by a predetermined phase amount (for example, phase difference of about 90 degrees). The data register buffer 300 then performs a re-timing in synchronization with the internal clock LCLKW using the FIFO (Write) circuit 301 to convert WL into WL=5, and outputs the write data DQ and the data strobe signal DQS. As described above, the write data is transferred from the data register buffer 300 to the memory chip 200 using either one of the two data lines L1 and L2. The data line to be used is determined by a designated Rank.

[0136] The memory chip 200 receives the write data DQ that is burst output from the data register buffer 300, and writes it in the memory cell array. At this time, there occurs a predetermined time difference (Flight Time) between a timing at which the write data DQ and the data strobe signal DQS are output from the data register buffer 300 and a timing at which the write data DQ and the data strobe signal DQS are input to the memory chip 200. In consideration of this point, the data register buffer 300 outputs the write data DQ earlier by an amount equivalent to the Flight Time. With this configuration, it becomes possible for the memory chip 200 to receive the write data DQ in a correct manner.