

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD, MICRON TECHNOLOGY,
INC., MICRON SEMICONDUCTOR PRODUCTS, INC., and
MICRON TECHNOLOGY TEXAS LLC,¹
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

IPR2022-00711
Patent 10,860,506 B2



DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

[Ex. 2013, p. 1](#)

Samsung Ex. 1086, p. 1

Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2023-00847

Key Arguments

GROUND 1-3

- Hiraishi alone or with Butt is missing a limitation (the “strobe delay feature”).
- Hiraishi does not have DQ/DQS skew problems.

GROUND 4-5

- The Hiraishi-Tokuhiro combination is missing a limitation (the “sampling” limitation).
- Petitioner's new “sampling” theory is improper and fails.
- There is no motivation to modify Hiraishi, as proposed, and no reasonable chance of success.

TOPICS

GROUND 1-3

Brief Technical Background Of The “Strobe Delay Feature”

Hiraishi Does Not Meet The “Strobe Delay Feature”

Hiraishi-Butt Also Does Not Meet the Strobe Delay Feature

A POSA Would Not Modify Hiraishi With Butt’s Strobe Centering

GROUND 4-5

Hiraishi-Tokuhiro Does Not Meet the “Sampling” Limitation

A POSA Would Not Have Modified Hiraishi with Tokuhiro As Proposed

Hiraishi-Tokuhiro Is Inoperable – No Reasonable Chance of Success

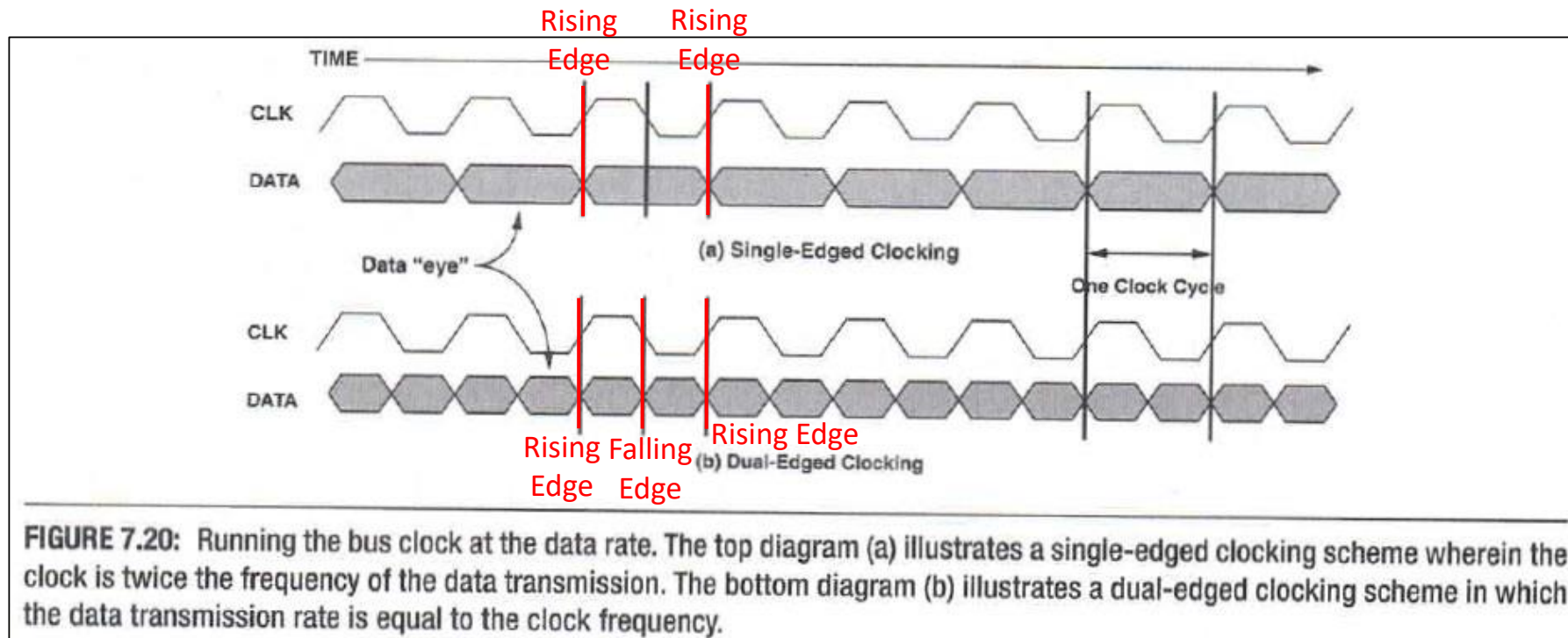
DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Ex. 2013, p. 3

Samsung Ex. 1086, p. 3

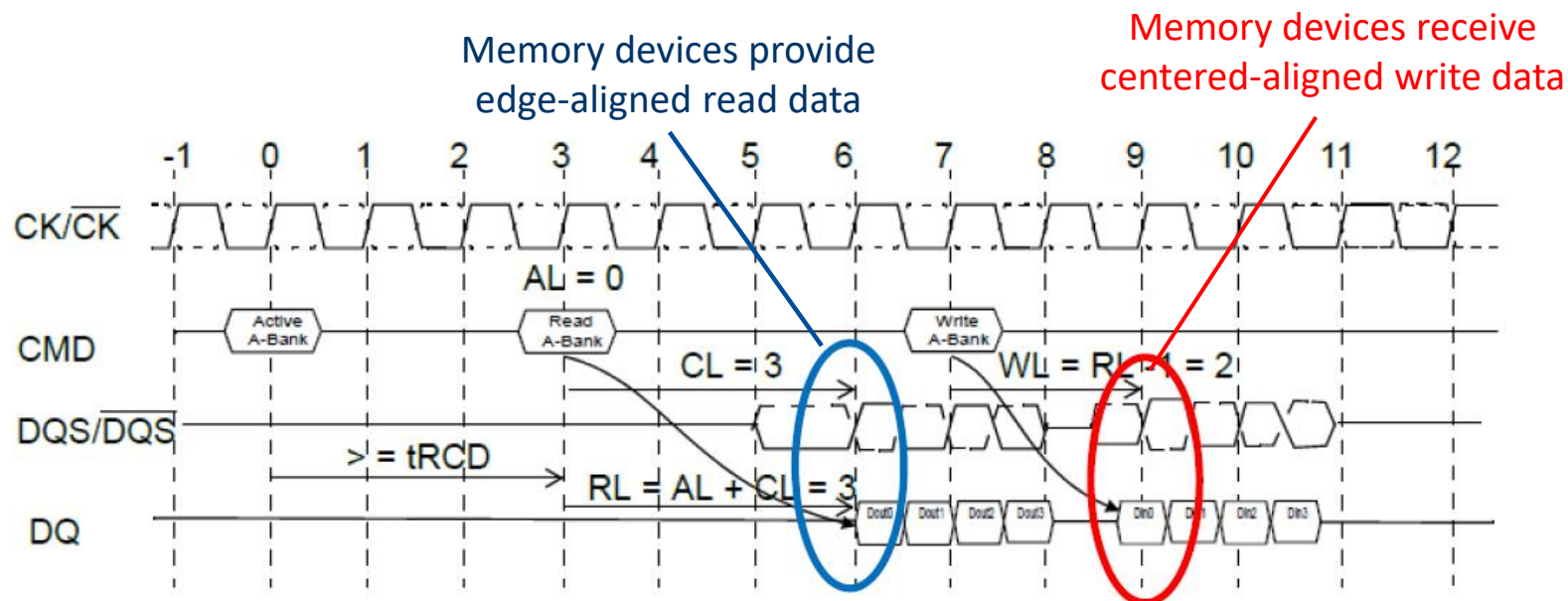
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Strobe Signals Are Used to Synchronize DDR Transmissions



EX2001, 334.

Data Strobe Centering for Read/Write Operations

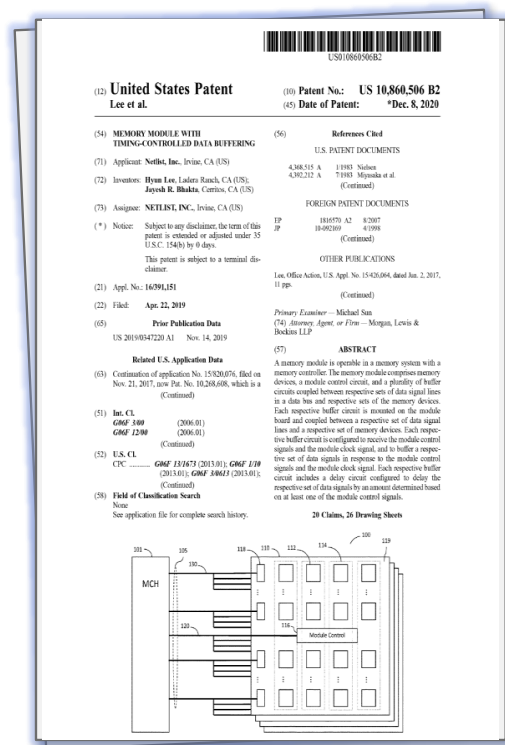


AL = 0 and CL = 3, RL = (AL + CL) = 3, WL = (RL - 1) = 2, BL = 4]

Figure 31 — Example 2: Read followed by a write to the same bank, where AL = 0 and CL = 3, RL = (AL + CL) = 3, WL = (RL - 1) = 2, BL = 4

EX2002 (JESD79-2F), 43

Conventional Leveling Techniques Are Insufficient

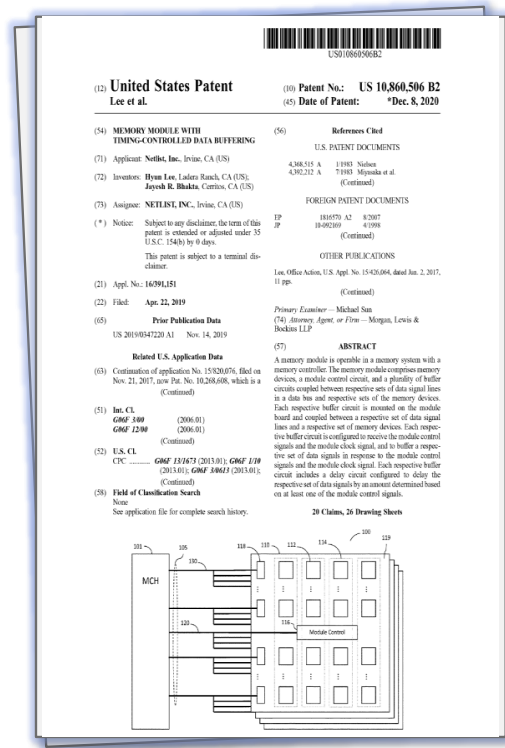


The '506 Patent

In some conventional memory systems, the memory controllers include leveling mechanisms for write and/or read operations to compensate for unbalanced wire lengths and memory device loading on the memory module. As memory operating speed and memory density continue to increase, however, such leveling mechanisms are also insufficient to insure proper timing of the control and/or data signals received and/or transmitted by the memory modules.

EX1001, 2:28-35.

One Embodiment of the '506 Patent's Novel Approach to Synchronizing Data and Data Strobe Signals



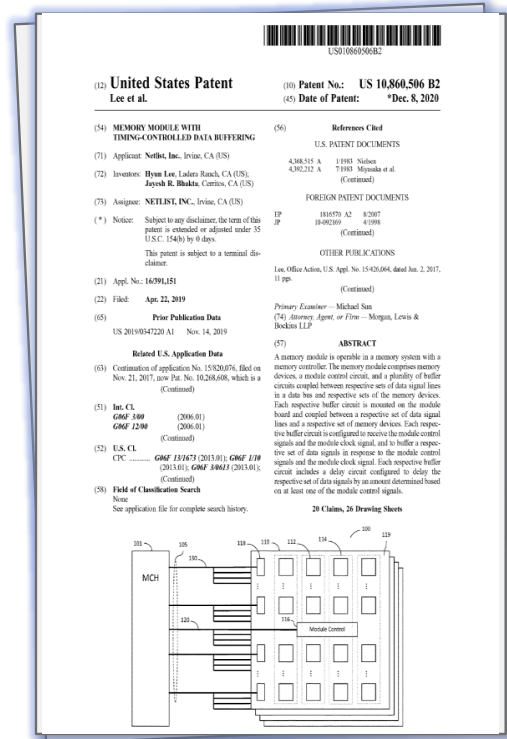
The “Strobe Delay Feature” of Claim 1

'506 Patent, Claim 1

wherein a first data buffer of the data buffers is coupled to the first memory device and is configurable to, in response to one or more of the module control signals: delay the first read strobe by a first predetermined amount to generate a first delayed read strobe; sample the first section of the read data using the first delayed read strobe; and

wherein the first predetermined amount is determined based at least on signals received by the first data buffer during one or more previous operations.

EX1001, Claim 1.



TOPICS

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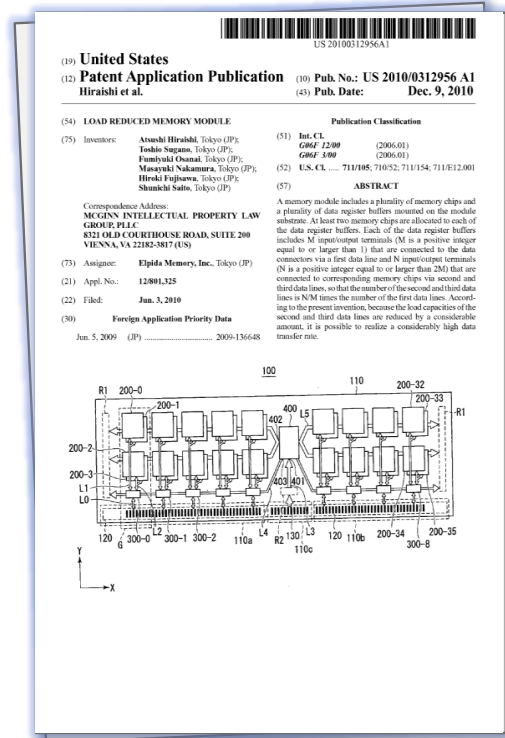
DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Ex. 2013, p. 9

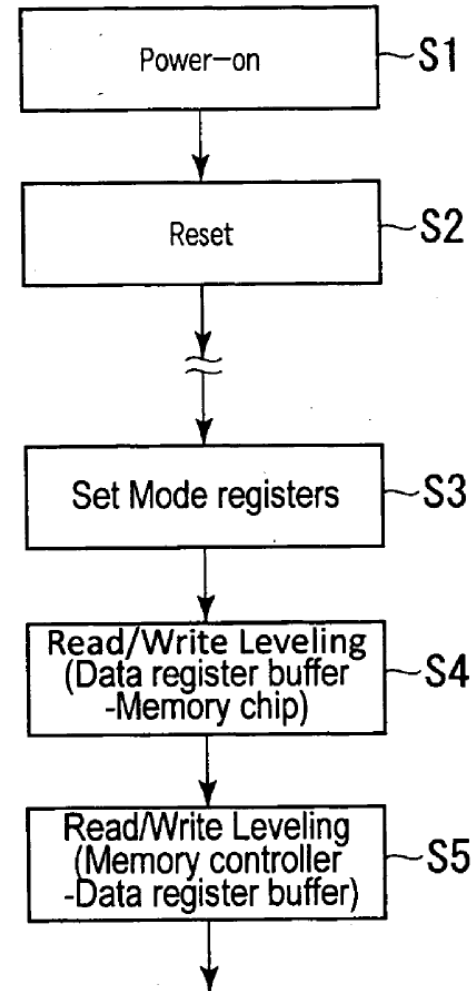
Samsung Ex. 1086, p. 9

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Hiraishi's Read/Write Leveling



EX1005, FIG. 13.
Patent Owner Response at 14.



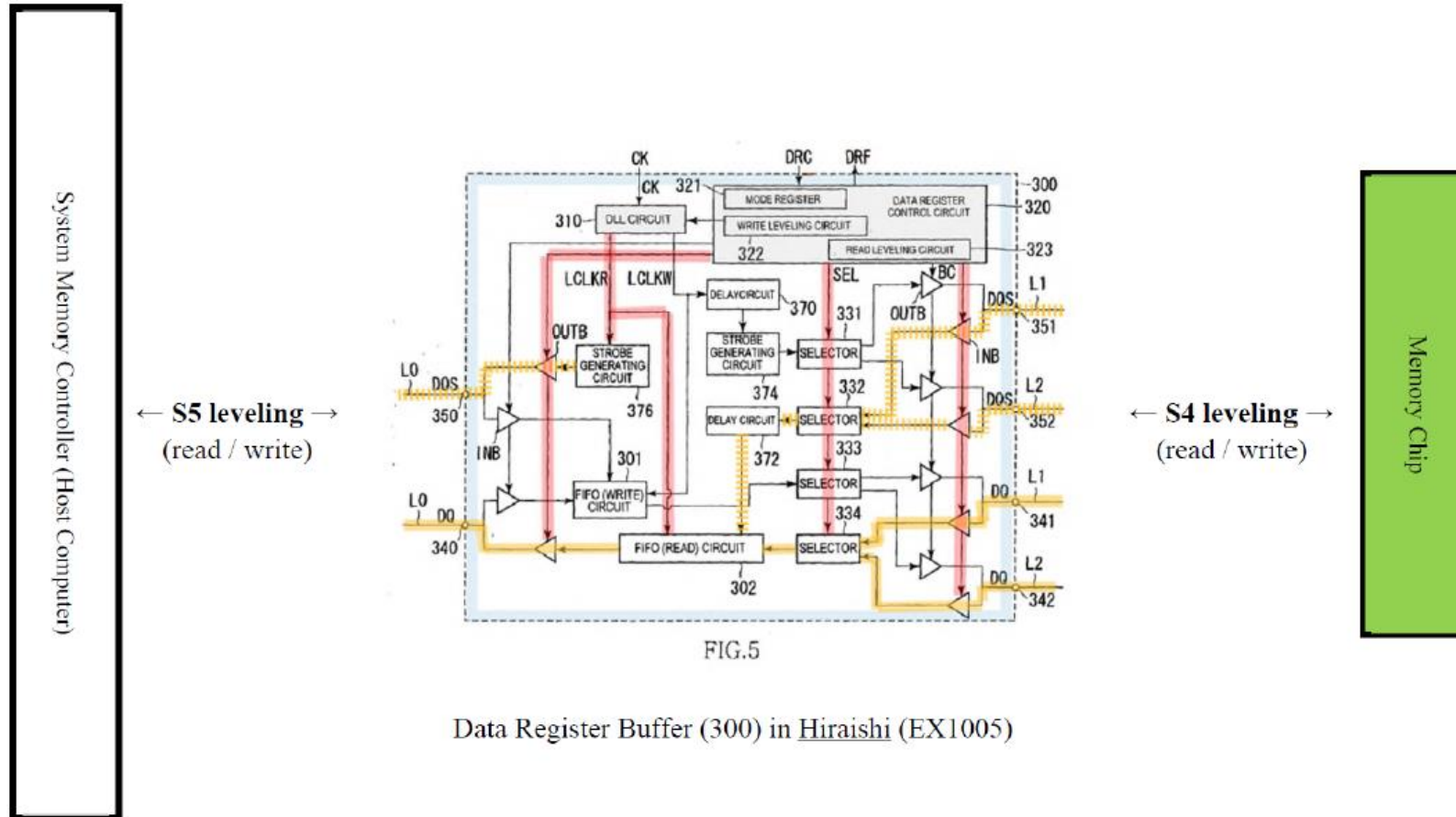
DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Ex. 2013, p. 10

Samsung Ex. 1086, p. 10

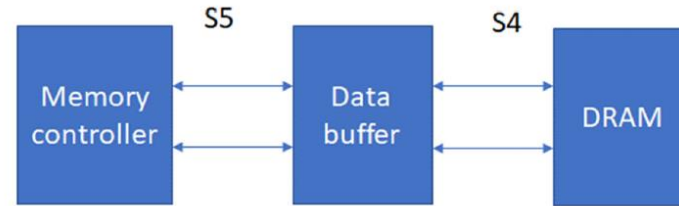
Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2023-00847

Hiraishi's Read/Write Leveling

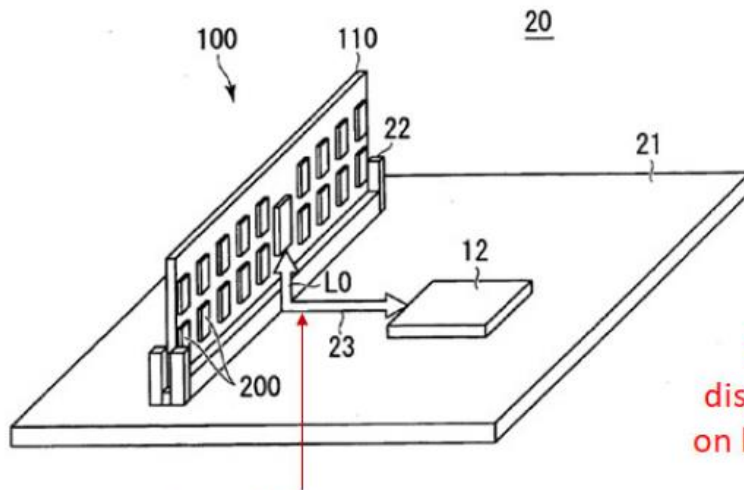


Data Register Buffer (300) in Hiraishi (EX1005)

Hiraishi's Read/Write Leveling

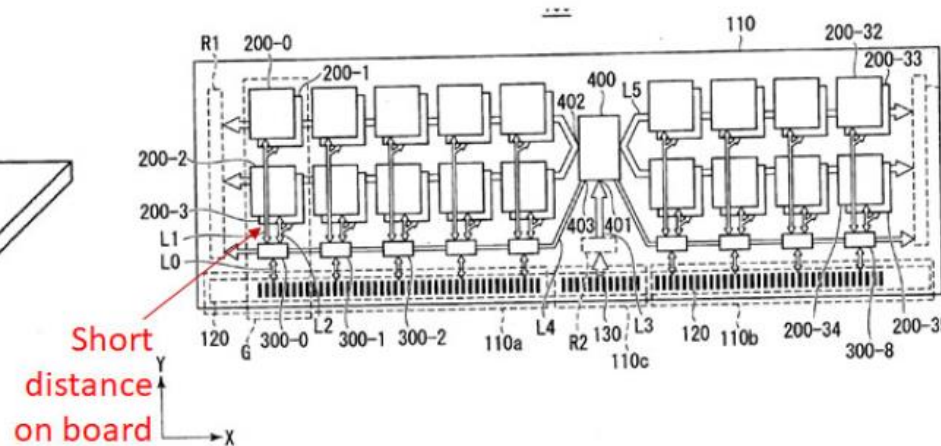


Patent Owner Response at 16.



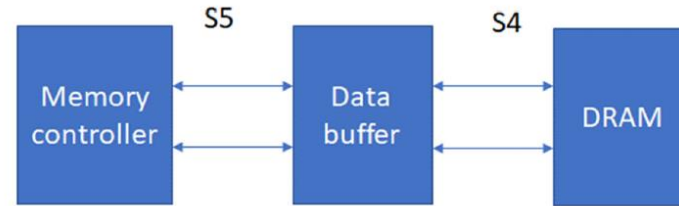
Hiraishi, FIG. 3

Long distance across
memory bus and off
board



Hiraishi, FIG. 1

Hiraishi's Read/Write Leveling



Patent Owner Response at 16.

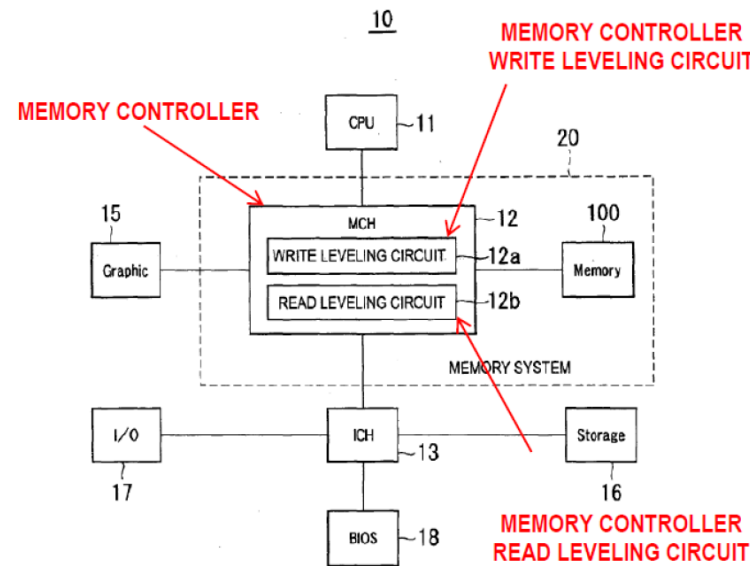
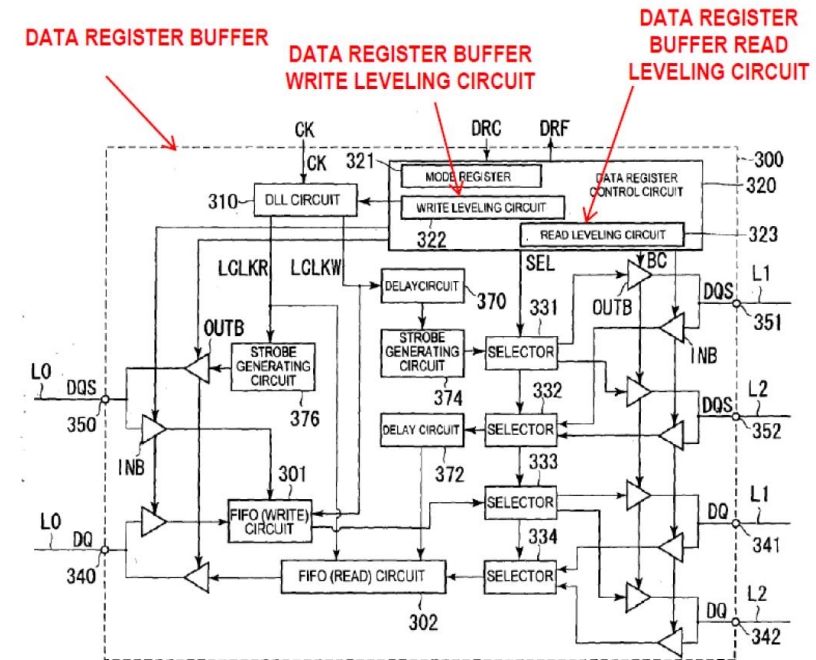


FIG. 2

Hiraishi, FIG. 2
Patent Owner Response at 18.



Hiraishi, FIG. 5
Patent Owner Response at 17.

FIG. 5

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Ex. 2013, p. 13

Samsung Ex. 1086, p. 13

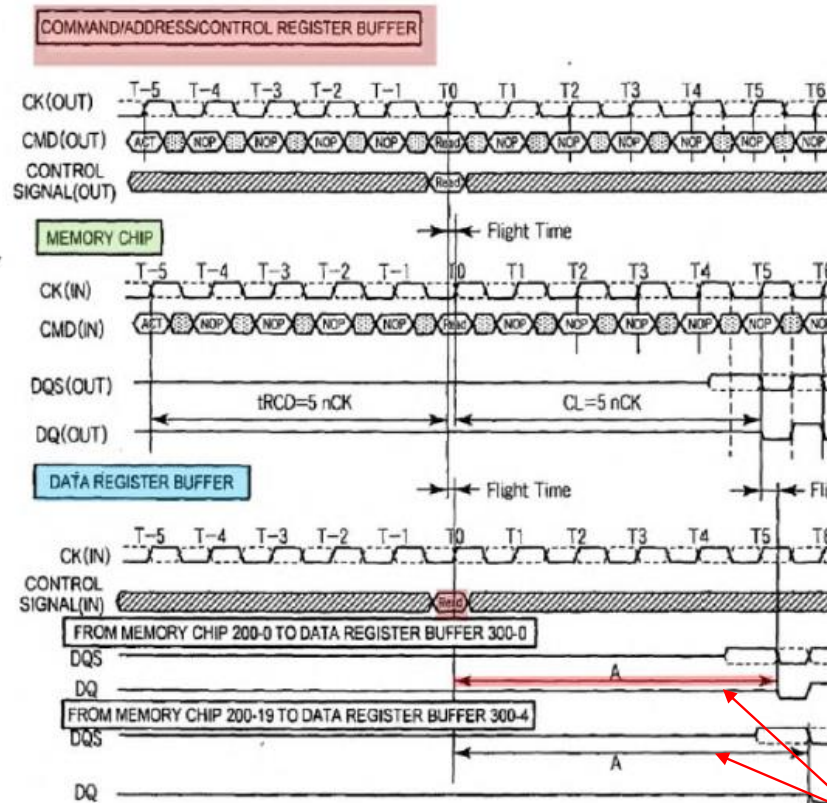
Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2023-00847

Hiraishi's S4 Read Leveling Does Not Delay Received DQS Signals Based On Previous Memory Operations ("Strobe Delay Feature")

[0147] FIG. 15 is a timing chart for explaining the read leveling operation between the data register buffer 300 and the memory chip 200. This operation is performed by the read leveling circuit 323 shown in FIG. 5.

[0151] The read data DQ output from the memory chip 200 reaches the data register buffer 300, by which the data register buffer 300 can find a time A from an input timing of the read command Read that is input as a part of the control signal DRC until the read data DQ is input. The time is measured for each of the memory chips 200, stored in the data register control circuit 320 in the data register buffer 300, and used in an adjustment of an activation timing of the input buffer circuit INB and the like. In FIG. 15, two cases are shown

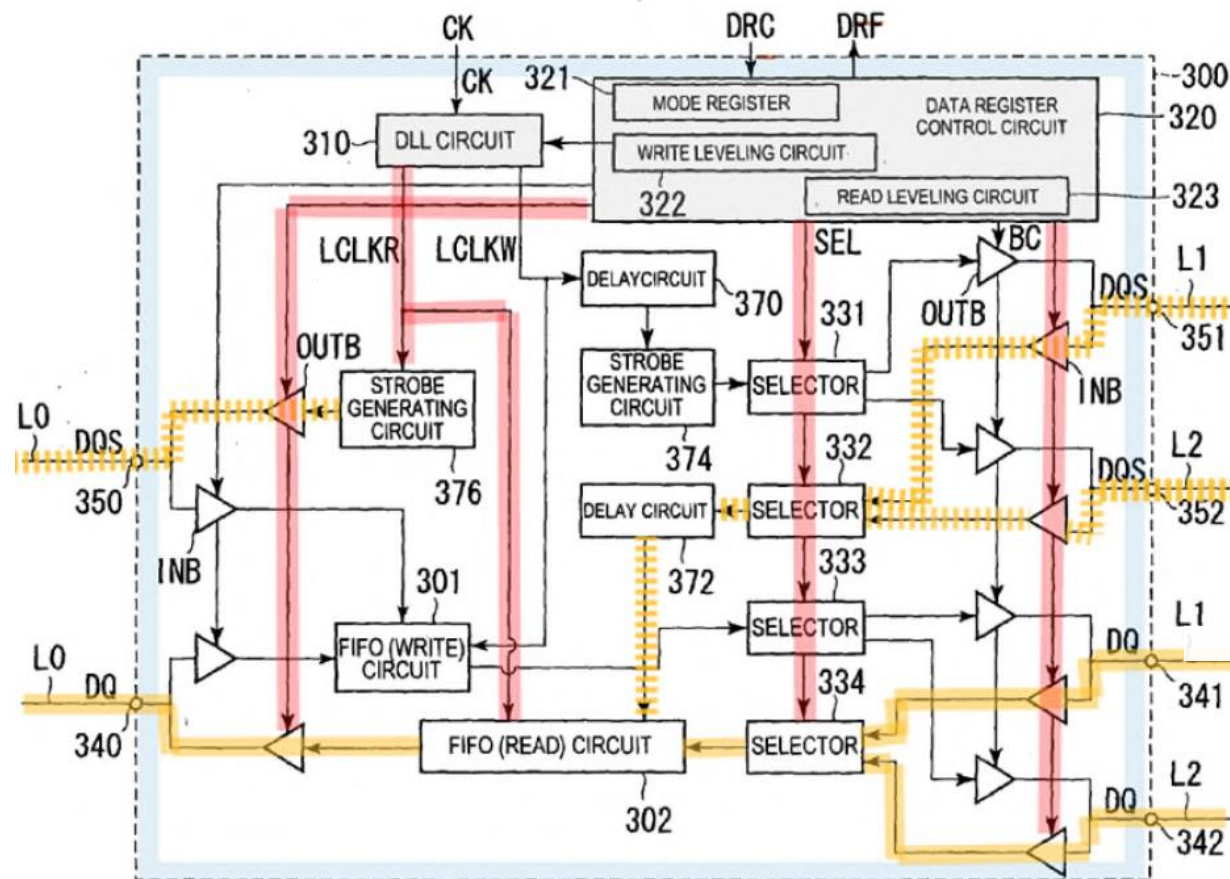
Hiraishi, [0147], [0151].



EX1005 (Hiraishi), FIG. 15 (reproduced from EX1003, ¶1281.

FIG. 15

Hiraishi's S4 Read Leveling Does Not Delay Received DQS Signals Based On Previous Memory Operations ("Strobe Delay Feature")



Hiraishi, FIG. 5

FIG.5

Petition at 36.

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Ex. 2013, p. 15

Samsung Ex. 1086, p. 15

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Dr. Wedig's Testimony about Hiraishi's Read Leveling

Robert Wedig
Samsung's Expert

SAMSUNG

4 A. Okay. So the read leveling, what it does, 10:49:35AM
5 it's used in an adjustment of the activation timing
6 from the input buffer circuit INB and the like.
7 That's the purpose of S4 leveling.

8 Q. I thought you were going to give me your 10:49:55AM
9 own instead of reading it.

10 A. Well, those are my words. My words come 10:49:59AM
11 from reading the specification. I think the
12 specification is clear.

13 Q. What does it mean to adjust an activation 10:50:09AM
14 timing of an input buffer?

15 A. It means to determine when to activate it, 10:50:15AM
16 when to enable it, when to turn it on, is basically
17 what it means. So it allows the data to pass when
18 it's activated.

EX2008, 59:4-18.

Patent Owner Response at 23.

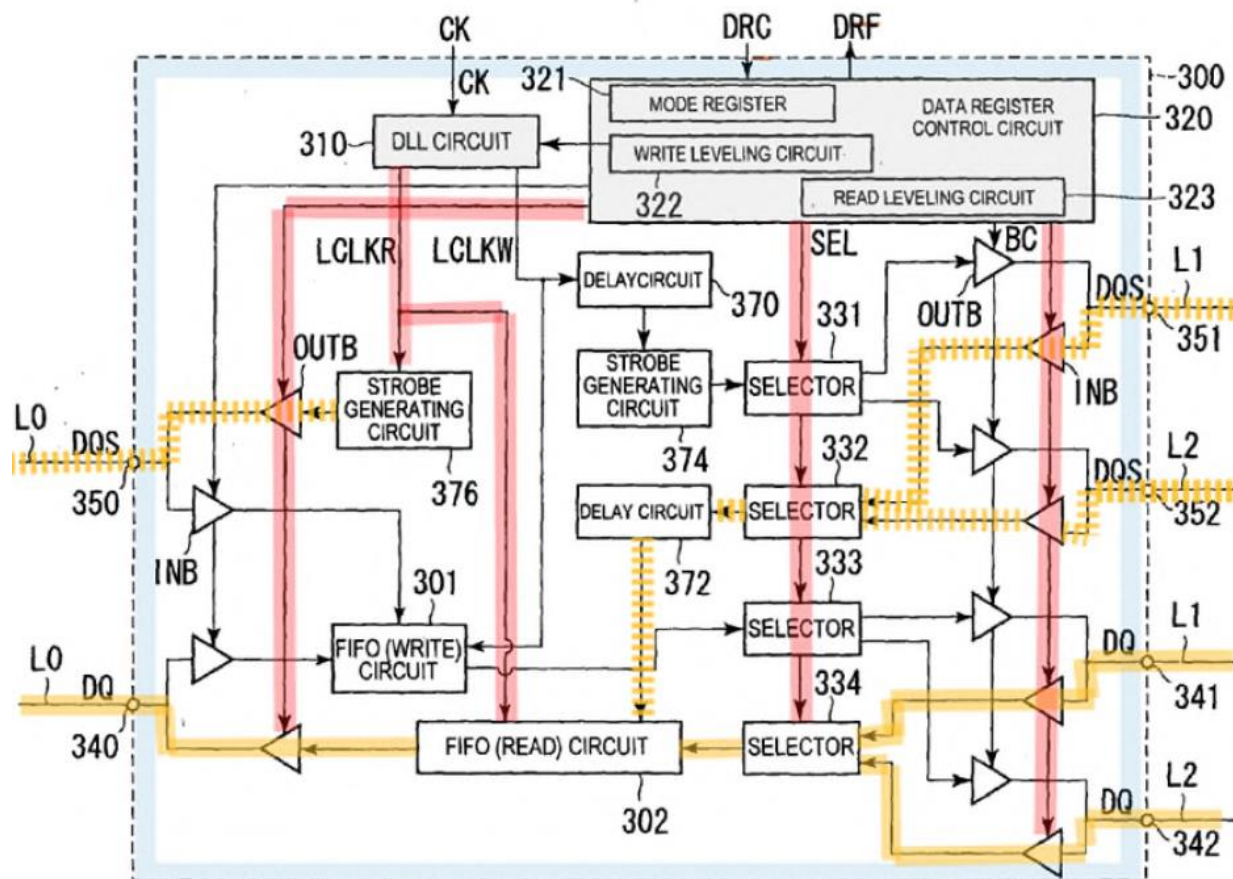
DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Ex. 2013, p. 16

Samsung Ex. 1086, p. 16

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Hiraishi's Data Buffer Does Not Delay Received DQS Signals Based On Previous Memory Operations ("Strobe Delay Feature")



Hiraishi, FIG. 5

FIG. 5

output terminals 351 and 352. A phase of the selected data strobe signal DQS is delayed by about 90 degrees by a delay circuit 372, and then the data strobe signal DQS is supplied to the FIFO (Read) circuit 302 as an input trigger signal. The

Hiraishi, [0091]

[0129] The data register buffer 300 loads the read data DQ that is output from the memory chip 200 in the FIFO (Read) circuit 302 with a data strobe signal DQS that is delayed by a predetermined phase amount (for example, phase difference of about 90 degrees). At this moment, there occurs a prede-

Hiraishi, [0129]

Hiraishi's Read Leveling Is Not Related to Strobe Centering

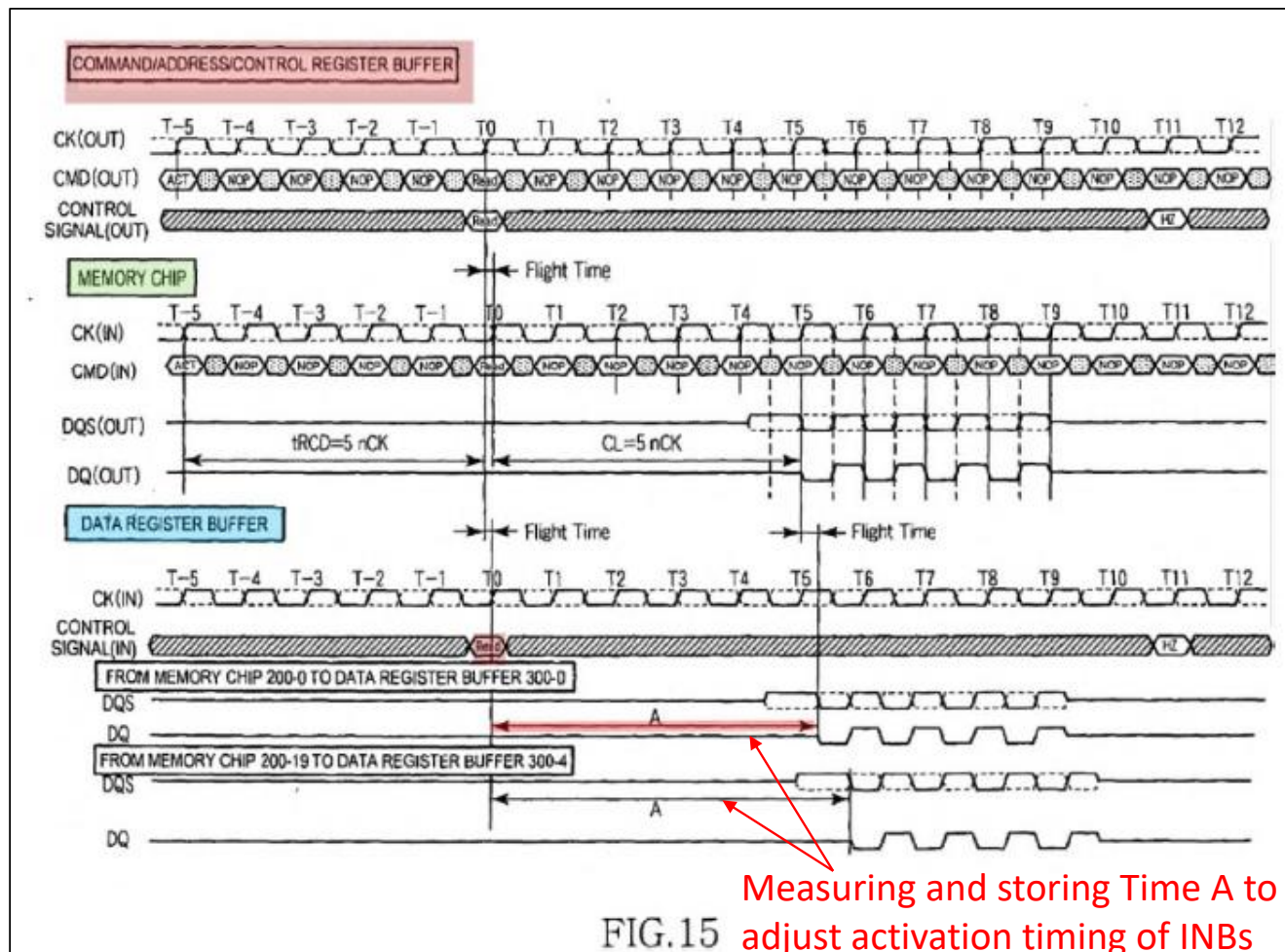


FIG. 15

Measuring and storing Time A to adjust activation timing of INBs

[0147] FIG. 15 is a timing chart for explaining the read leveling operation between the data register buffer 300 and the memory chip 200. This operation is performed by the read leveling circuit 323 shown in FIG. 5.

EX1005 (Hiraishi), [0147].

[0151] The read data DQ output from the memory chip 200 reaches the data register buffer 300, by which the data register buffer 300 can find a time A from an input timing of the read command Read that is input as a part of the control signal DRC until the read data DQ is input. The time is measured for each of the memory chips 200, stored in the data register control circuit 320 in the data register buffer 300, and used in an adjustment of an activation timing of the input buffer circuit INB and the like. In FIG. 15, two cases are shown

EX1005 (Hiraishi), [0151].

EX1005 (Hiraishi), FIG. 15 (reproduced from EX1003, ¶1281).

Patent Owner Sur-Reply at 1.

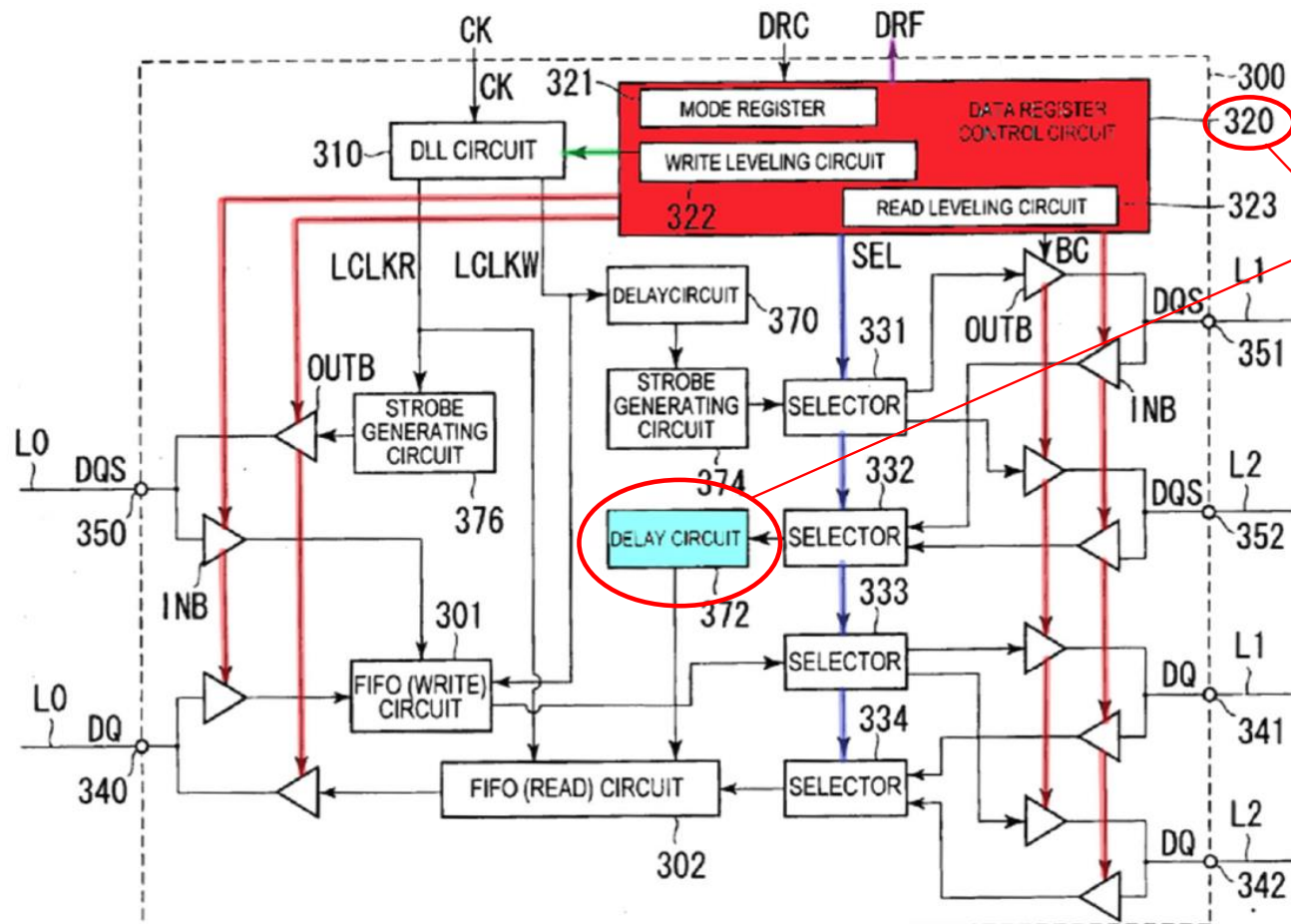
DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Ex. 2013, p. 18

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Hiraishi's Data Buffer Cannot Delay Received DQS Signals Based On Previous Memory Operations ("Strobe Delay Feature")



Hiraishi, FIG. 5

FIG. 5

Data register control circuit 320 is not connected to Delay Circuit 372

Hiraishi's “adjust[ment] of read timing”

The Samsung logo, consisting of the word "SAMSUNG" in white capital letters inside a blue oval.

[0140] Upon completing the mode register setting operation, a leveling operation between the data register buffer 300 and the memory chip 200 is performed (Step S4). The leveling operation is to adjust a write timing or a read timing in consideration of a propagation time of a signal. The adjustment of the write timing is performed by a write leveling operation, and the adjustment of the read timing is performed by a read leveling operation.

Petitioner Reply at 3-4.

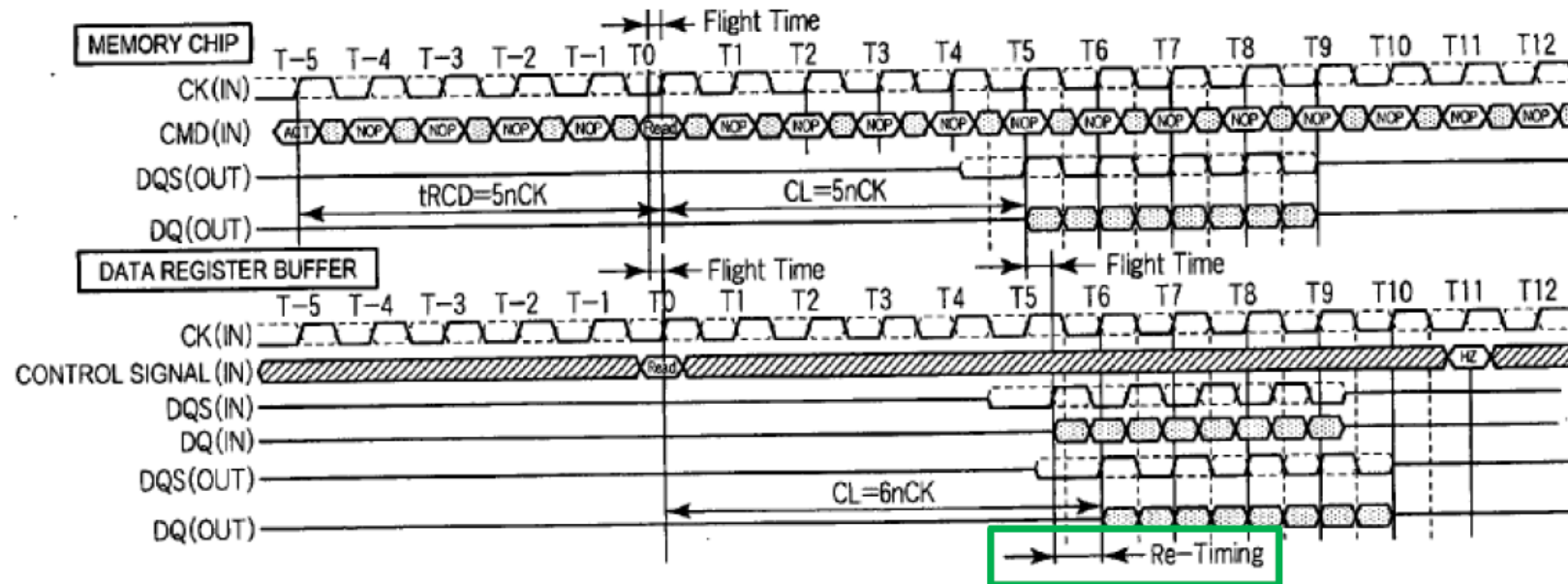
DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Ex. 2013, p. 20

Samsung Ex. 1086, p. 20

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Hiraishi's DQS Re-timing



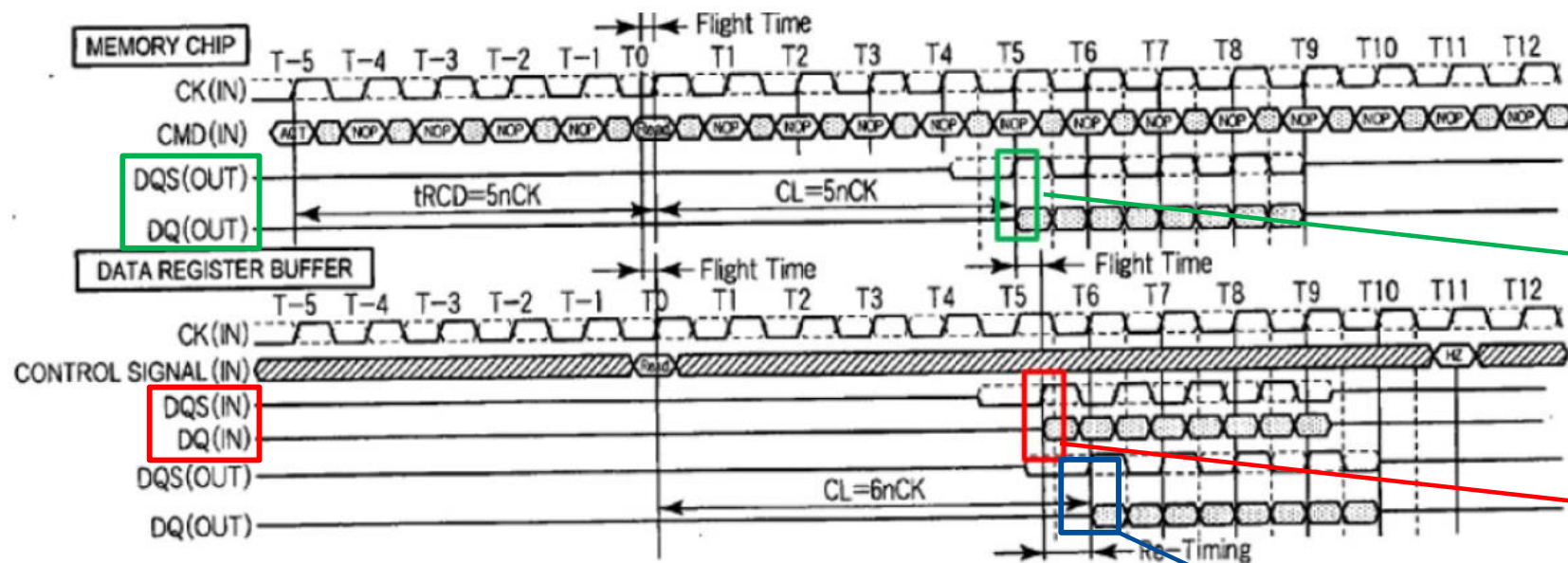
Hiraishi, FIG. 11

FIG. 11

[0130] Thereafter, the data register buffer 300 performs a re-timing in synchronization with the internal clock LCLKR using the FIFO (Read) circuit 302 to convert CL into CL=6, and outputs the read data DQ and the data strobe signal DQS.

EX1005 (Hiraishi), [0130]

Hiraishi's Re-Timing Does Not Adjust DQ/DQS Alignment



Hiraishi, FIG. 11

FIG.11

DQS/DQ signals are edge-aligned when they leave the memory chip

DQS/DQ signals remain edge-aligned when they arrive at the data buffer

DQS/DQ signals continue to be edge-aligned after re-timing

Hiraishi's Re-Timing Does Not Adjust DQ/DQS Alignment

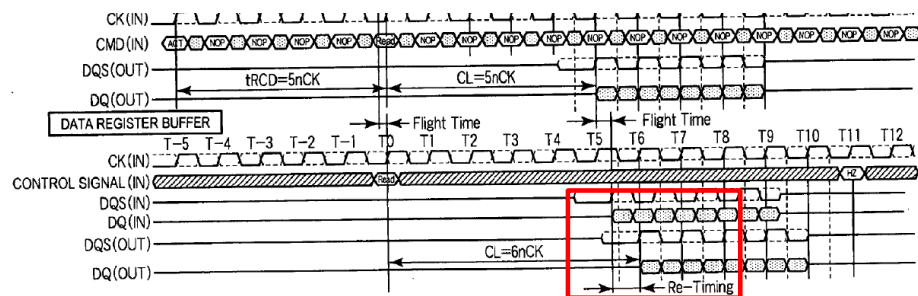
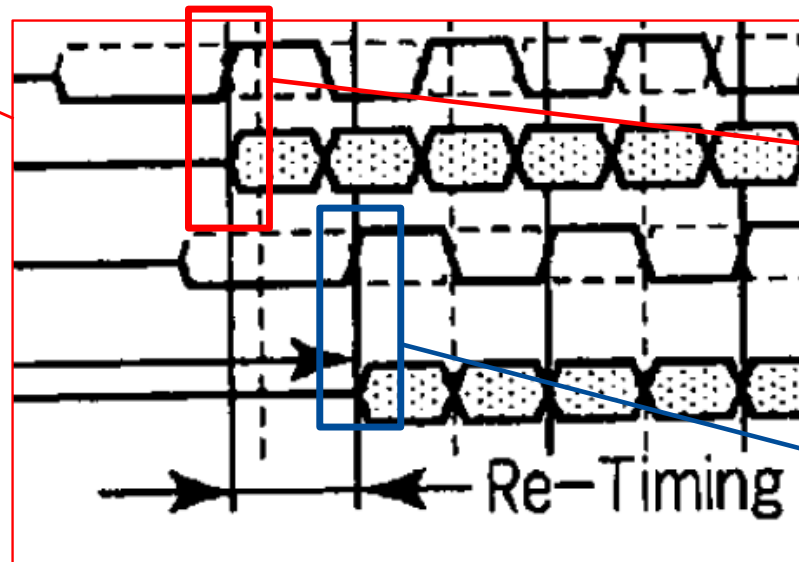


FIG. 11



DQS/DQ signals remain edge-aligned when they arrive at the data buffer (before re-timing)

DQS/DQ signals continue to be edge-aligned after re-timing

Hiraishi, FIG. 11

TOPICS

GROUND 1-3

Brief Technical Background Of The “Strobe Delay Feature”

Hiraishi Does Not Meet The “Strobe Delay Feature”

Hiraishi-Butt Also Does Not Meet the Strobe Delay Feature

A POSA Would Not Modify Hiraishi With Butt’s Strobe Centering

GROUND 4-5

Hiraishi-Tokuhiro Does Not Meet the “Sampling” Limitation

A POSA Would Not Have Modified Hiraishi with Tokuhiro As Proposed

Hiraishi-Tokuhiro Is Inoperable – No Reasonable Chance of Success

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Ex. 2013, p. 24

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The Proposed Modification of Hiraishi With Butt

Robert Wedig
Samsung's Expert

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“Like the datapaths 114 in Butt, the read leveling circuit 323 and delay circuit 372 would iteratively test memory access using different offsets to a received data strobe signal DQS, in order to find the maximum, minimum, and optimum offsets. The optimum offset would then be used in later memory read operations; the read leveling circuit 323 would adjust the base delay of the delay circuit 372 in the amount of the optimum offset (e.g., “about 90 degrees”).”

EX1003 (Wedig Declaration), ¶150.

The Hiraishi-Butt Combination Does Not Change Hiraishi's Circuitry

Robert Wedig
Samsung's Expert

The Samsung logo, consisting of the word "SAMSUNG" in white capital letters inside a blue oval.

Q. In a situation where Hiraishi is not determined to contain all of the circuitry necessary to perform the read leveling operation that you claim it does, what circuitry from Butt would you specifically add to Hiraishi then?

A. Well, this is not in my report, so I would have to -- I would be generating new information, I would be generating new opinions. Because like I said, I felt it's already there.

EX2008 (Wedig Deposition), 139:9-17.

Petitioner's Reply: The Proposed Modification of Hiraishi With Butt

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Thus, even though Figure 5 of Hiraishi does not expressly show a wire between read leveling circuit 323 and delay circuit 372, a POSITA would understand that such a connection exists — especially in the combination with Butt

Petitioner Reply at 9.

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Ex. 2013, p. 27

Samsung Ex. 1086, p. 27

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The Proposed Modification Requires Much More Than a “Wire”



20 And so, again, this is only in the 2:15:22PM
21 assumption that -- only in the assumption that you
22 feel that Hiraishi doesn't already do it. And so
23 you would need a mechanism for -- you would need a
24 mechanism for doing a programmable delay. You would
25 need a mechanism for generating the various offsets.
1 You would need a mechanism for feeding back the
2 value. You would need all the different aspects
3 that cause Butt to operate.

EX2008 (Wedig Deposition), 139:20-140:3.

Missing “Aspects That Cause Butt To Operate”

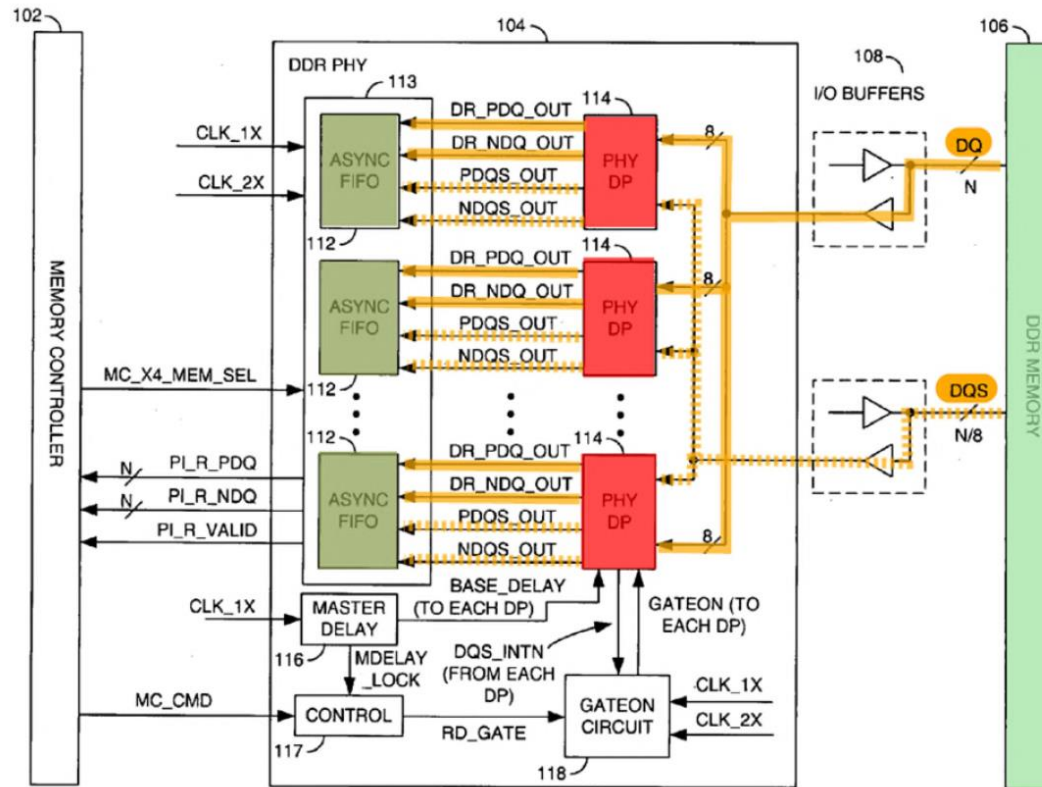


FIG. 2

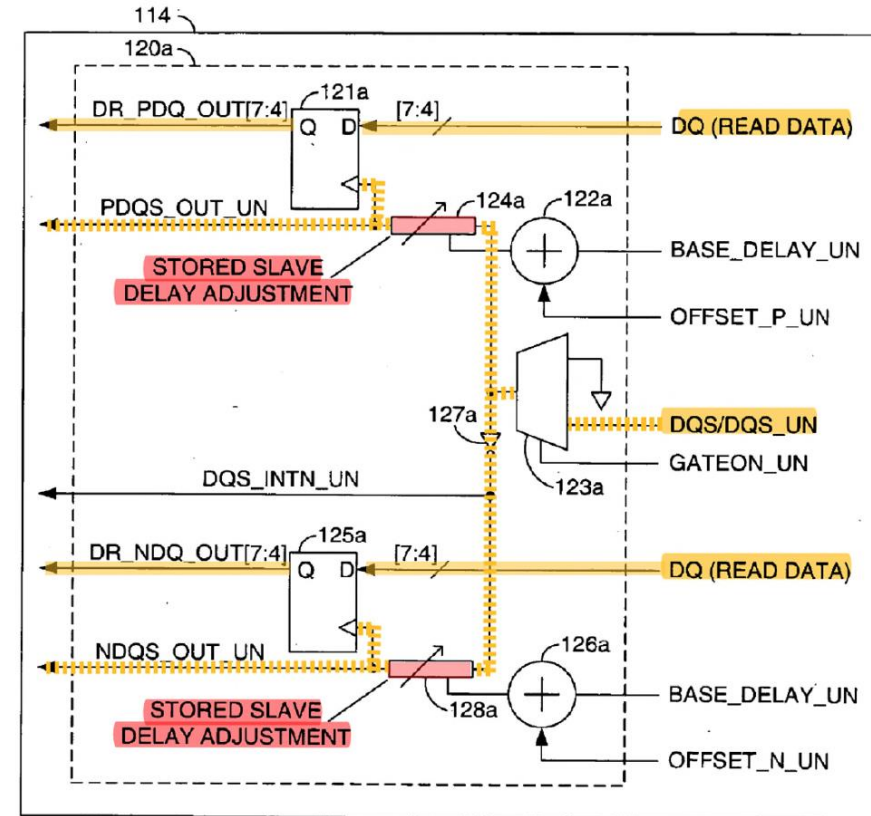


FIG. 3A

Petition at 44-45.

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Ex. 2013, p. 29

Samsung Ex. 1086, p. 29

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DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Ex. 2013, p. 30

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No Motivation To Combine – Hiraishi's DQ and DQS are Edge-Aligned

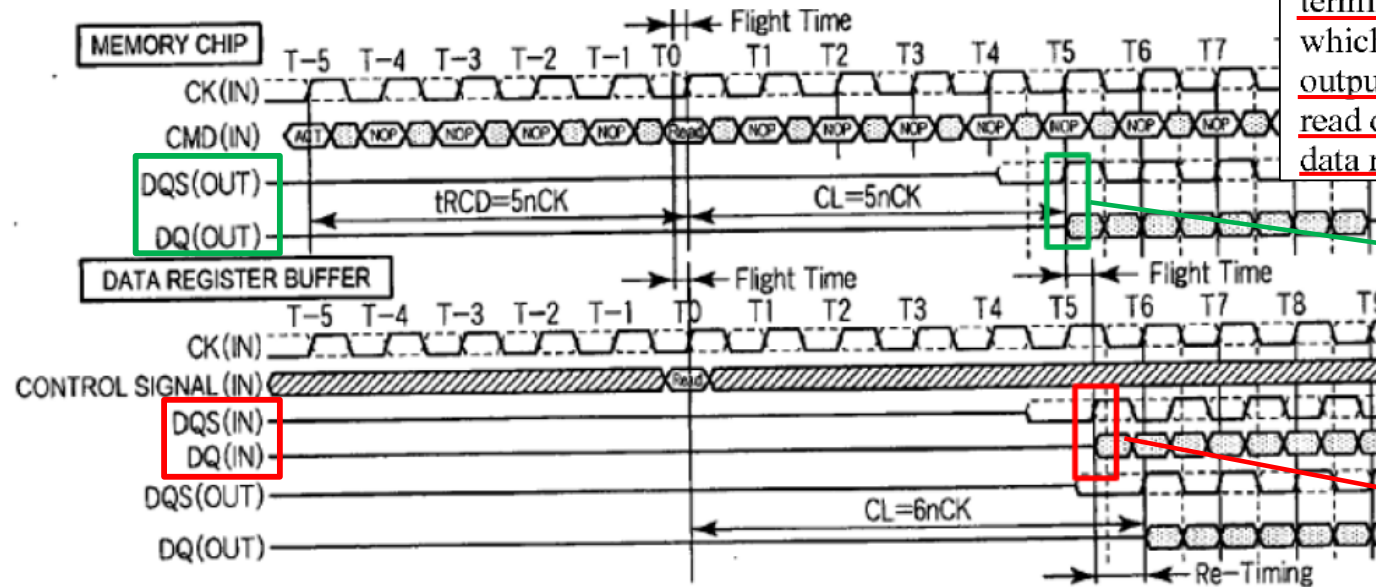


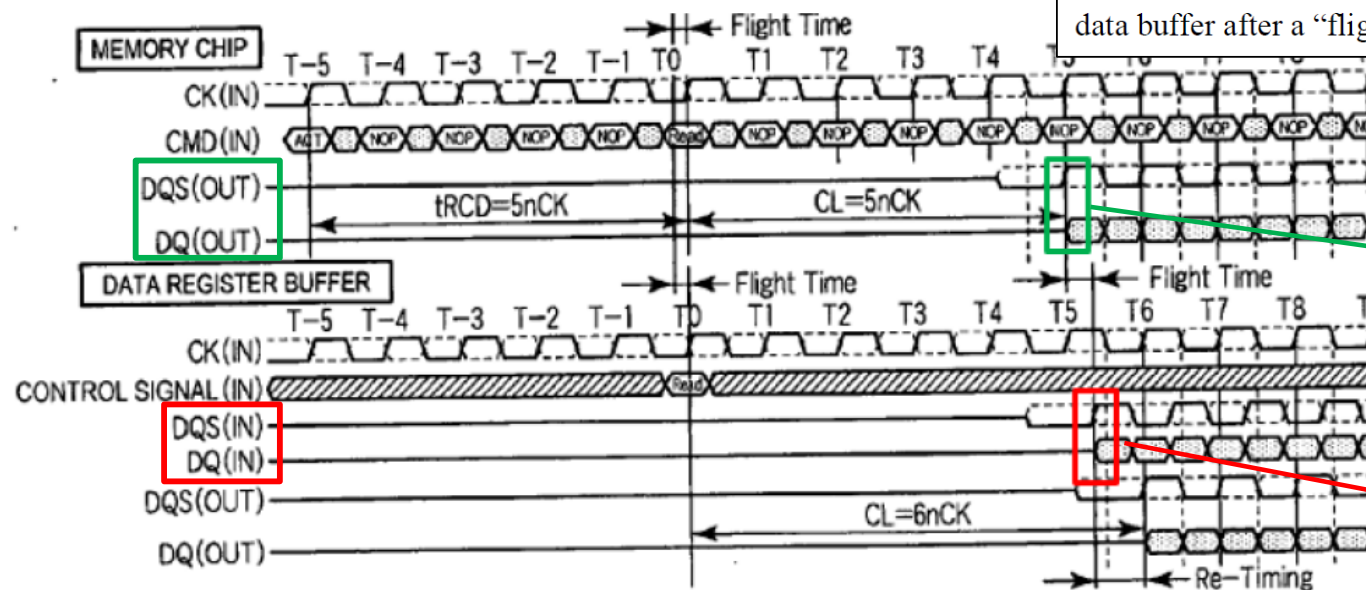
FIG. 11

[0129] The data register buffer 300 loads the read data DQ that is output from the memory chip 200 in the FIFO (Read) circuit 302 with a data strobe signal DQS that is delayed by a predetermined phase amount (for example, phase difference of about 90 degrees). At this moment, there occurs a predetermined time difference (Flight Time) between a timing at which the read data DQ and the data strobe signal DQS are output from the memory chip 200 and a timing at which the read data DQ and the data strobe signal DQS are input to the data register buffer 300.

DQS/DQ signals are edge-aligned when they leave the memory chip

DQS/DQ signals remain edge-aligned when they arrive at the data buffer

No Motivation To Combine – Hiraishi's DQ and DQS are Edge-Aligned



300.” EX1005, [0129]. This “flight time” is shown in FIG. 11 (see below), and DQS(IN) and DQ(IN) have the same “flight time,” i.e., are edge-aligned. Specifically, the DQS(OUT) and DQ(OUT) leave the memory chip edge-aligned, as shown in the green annotation below, and the DQS(IN) and DQ(IN) arrive at the data buffer after a “flight time,” but nonetheless still edge-aligned.

EX2006 (Mangione-Smith Decl.), ¶180

DQS/DQ signals are edge-aligned when they leave the memory chip

DQS/DQ signals remain edge-aligned when they arrive at the data buffer

FIG. 11

Hiraishi, FIG. 11

Patent Owner Response at 26-27
Patent Owner Sur-reply at 2-3.

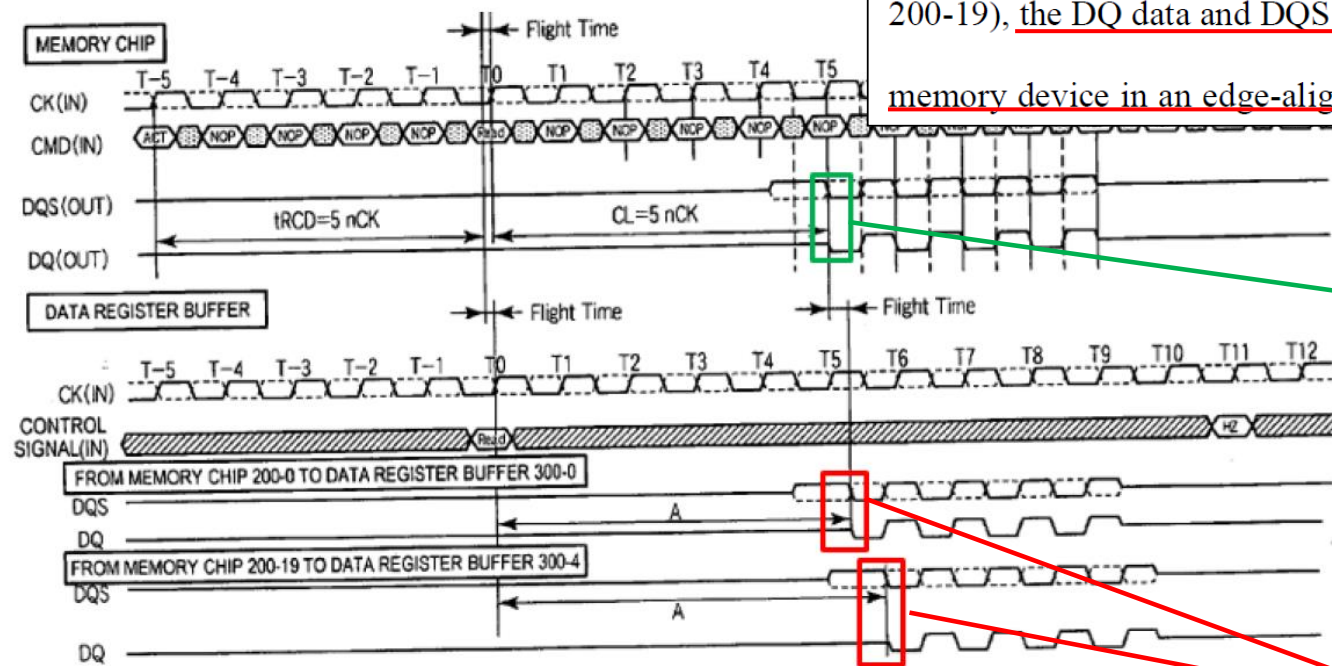
DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Ex. 2013, p. 32

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No Motivation To Combine – Hiraishi's DQ and DQS are Edge-Aligned



81. Moreover, Hiraishi shows in FIG. 15 that, while the flight time varies as between different memory devices (*e.g.*, memory chip 200-0 and memory chip 200-19), the DQ data and DQS strobe is again received by the data buffer from any memory device in an edge-aligned state. Here, the memory chip begins outputting

EX2006 (Mangione-Smith Decl.), ¶181

DQS/DQ signals are edge-aligned when they leave the memory chip

DQS/DQ signals remain edge-aligned when they arrive at the data buffer

FIG. 15

Hiraishi, FIG. 15

Patent Owner Response at 27

Patent Owner Sur-reply at 9.

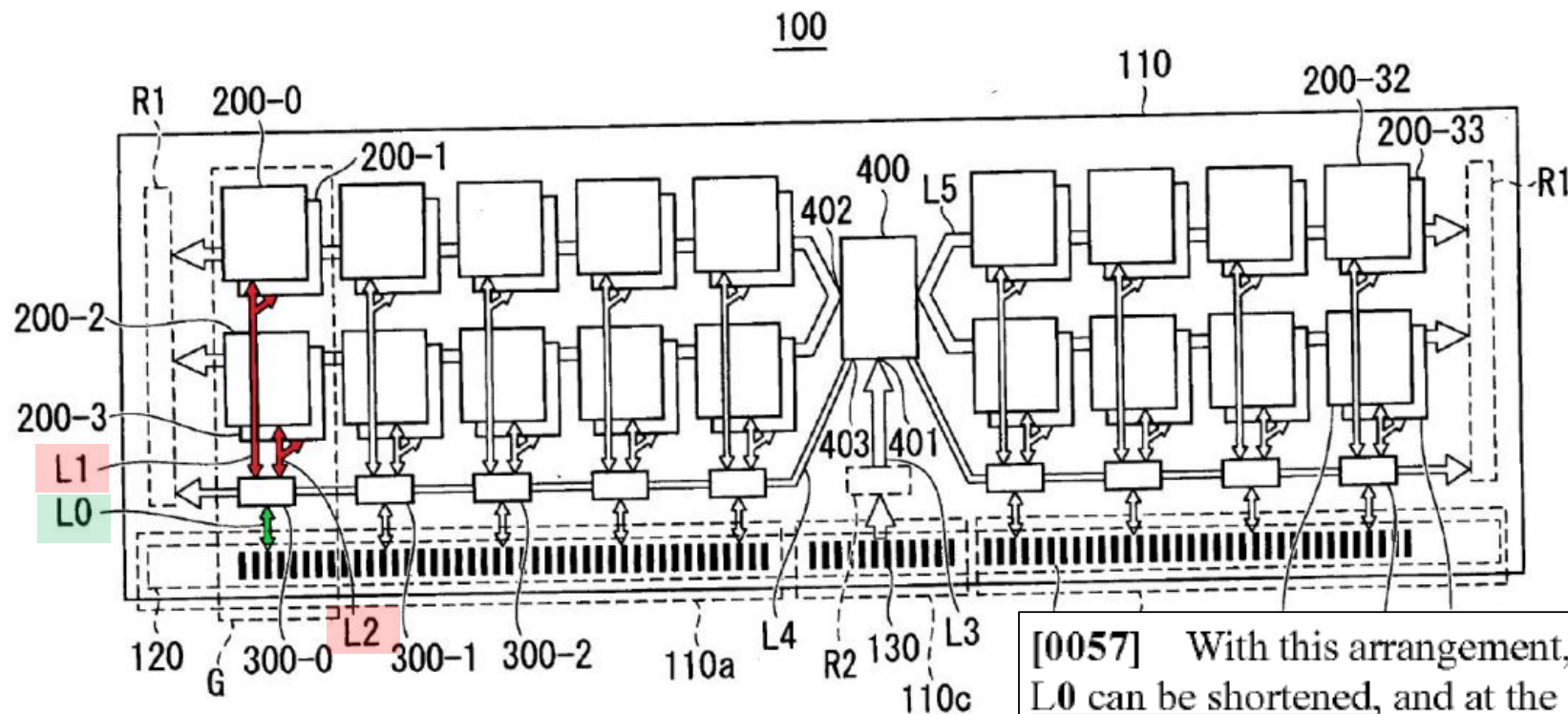
DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Ex. 2013, p. 33

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No Motivation To Combine – Hiraishi's DQ/DQS are Edge-Aligned



Hiraishi, FIG. 1,

[0057] With this arrangement, a line length of the data line L0 can be shortened, and at the same time, the line length of the data line L0 can be made substantially equal among the groups. Similarly, line lengths of the data lines L1 and L2 can be shortened, and at the same time, the line lengths of the data lines L1 and L2 can be made substantially equal among the groups.

Petition at 25, 32.

Patent Owner Sur-reply at 3, 9-10.

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Hiraishi, [0057]

Ex. 2013, p. 34

Samsung Ex. 1086, p. 34

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Hiraishi Does Not Suffer From DQ/DQS Skew Problems

Table 65 — Timing Parameters by Speed Bin (Cont'd)

NOTE: The following general notes from page 170 apply to Table 65: Note a. VDD =VDDQ = 1.5V +/- 0.075V

		DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Units
Cumulative error across 8 cycles	tERR(8per)	- 241	241	- 217	217	- 193	193	- 169	169	ps
Cumulative error across 9 cycles	tERR(9per)	- 249	249	- 224	224	- 200	200	- 175	175	ps
Cumulative error across 10 cycles	tERR(10per)	- 257	257	- 231	231	- 205	205	- 180	180	ps
Cumulative error across 11 cycles	tERR(11per)	- 263	263	- 237	237	- 210	210	- 184	184	ps
Cumulative error across 12 cycles	tERR(12per)	- 269	269	- 242	242	- 215	215	- 188	188	ps
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR(nper)	$tERR(nper)_{min} = (1 + 0.68\ln(n)) * tJIT(per)_{min}$ $tERR(nper)_{max} = (1 + 0.68\ln(n)) * tJIT(per)_{max}$								ps
Data Timing										
DQS, DQS# to DQ skew, per group, per access	tDQSQ	-	200	-	150	-	125	-	100	ps

EX2006, ¶123 (citing EX1020, p. 164)

125. Thus, under the DDR3 standard Hiraishi's data buffer (and Tokuhiro's memory controller) can be assured of receiving edge-aligned DQ data and DQS strobes from the memory devices within a very tight tolerance, and therefore they have no need to perform any additional strobe-centering operation.

EX2006 (Mangione-Smith Decl.), ¶125

Hiraishi Does Not Suffer From DQ/DQS Skew Problems

Butt Proposes an Alternative Approach

ship. A conventional approach performs system-level timing analysis using a simulation program for integrated circuit emphasis (SPICE) to determine a timing that yields adequate setup and hold time margin within a data valid window. The conventional approach is not programmable and can vary for different hardware implementations. The conventional approach does not calibrate the actual data valid window in silicon. The conventional approach relies heavily on the pre-silicon, system-level, SPICE timing analysis.

EX1029 (Butt) at [0003].

“The objects, features and advantages of the present invention include providing a method for read data strobe centering (data eye training) that may ... eliminate reliance on a system level, pre-silicon, SPICE timing analysis on the data valid window.”

EX1029 (Butt) at [0006].

Patent Owner Sur-Reply at 4.

No Flaw Identified in Hiraishi's Approach

5	THE DEPONENT: I don't believe so. I
6	think reading Hiraishi, a person would understand
7	how the -- the delay centers the strobe in the eye
8	and wouldn't -- <u>wouldn't identify any particular</u>
9	<u>flaw in that approach.</u> I don't recall Dr. Wedig
10	identifying any particular flaw in that approach.

EX1046 (Mangione-Smith Deposition), 266:5-10

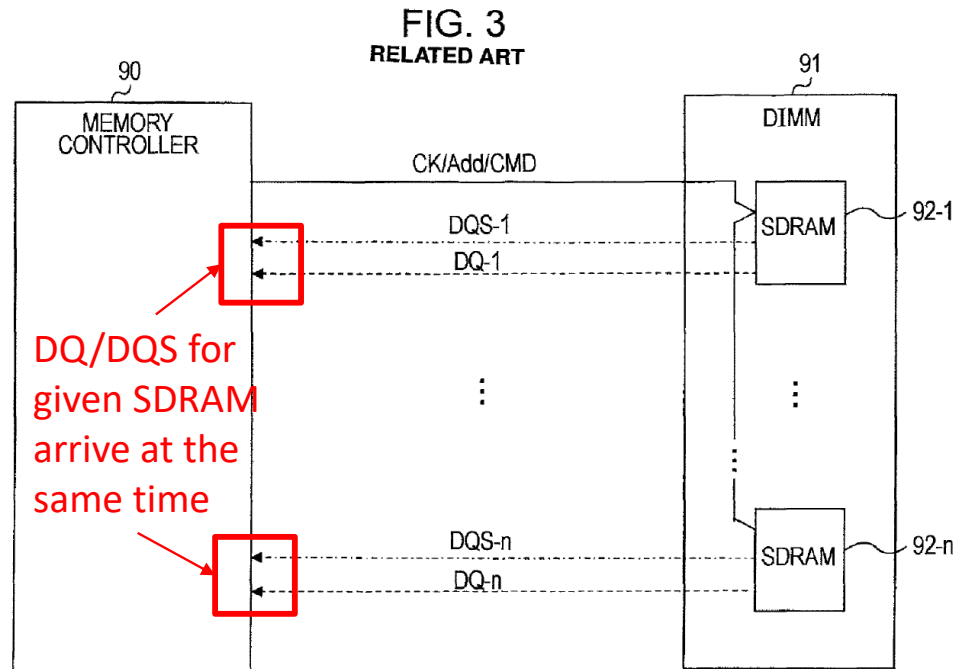
DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Ex. 2013, p. 36

Samsung Ex. 1086, p. 36

Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2023-00847

DQ/DQS Also Arrive Edge-Aligned In Tokuhiro



EX1006 (Tokuhiro), FIG. 3, cited at EX2006, ¶120
EX2006, ¶120 cited at Patent Owner Response at 48.

Therefore, the data signal DQ-n and the data strobe signal DQS-n output from the SDRAM 92-n to which the clock signal CK is input lastly arrives at the memory controller 90 approximately 1 ns after the data signal DQ-1 and the data strobe signal DQS-1 output from the SDRAM 92-1 to which the clock signal CK is input firstly where the data transmission speed is 7 ps/mm as the case described above. $7 \text{ ps/mm} \times 133 \text{ mm} = 931 \text{ ps}$.

EX1006 (Tokuhiro), 3:1-8, cited at EX2006, ¶120
EX2006, ¶120 cited at Patent Owner Response at 48.

Patent Owner Response at 47-48.

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Ex. 2013, p. 37

Samsung Ex. 1086, p. 37

Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2023-00847

There Universal Meaning of Read Leveling

[0147] FIG. 15 is a timing chart for explaining the read leveling operation between the data register buffer 300 and the memory chip 200. This operation is performed by the read leveling circuit 323 shown in FIG. 5.

Hiraishi

EX1006 (Hiraishi), [0147]
Patent Owner Response at 15, 23.

window (i.e., DQS is center-aligned with DQ). Read leveling is the process of 'training' the DQS/DQS# to be positioned in the middle of the DQ bit window. Conventional read level

Bhakta

EX1054 (Bhakta), 7:13-15
Patent Owner Sur-reply at 12.

The DDR3 Standard Does Not Provide for Read Leveling

Although, the DDR3 memory interface compensates the arrival time when the data strobe signals DQS-1 to DQS-n arrive at the SDRAMs 92-1 to 92-n in the write operations according to the JEDEC standards as described above, compensations of the signal arrival time in read operations are not provided with the JEDEC standards.

EX1006 (Tokuhiro), 2:54-59

JEDEC Standard No. 79-3C

Page 42

4 DDR3 SDRAM Command Description and Operation (Cont'd)

4.8 Write Leveling

For better signal integrity, the DDR3 memory module adopted fly-by topology for the commands, addresses, control signals, and clocks. The fly-by topology has benefits from reducing number of stubs and their length, but it also causes flight time skew between clock and strobe at every DRAM on the DIMM.

EX1020 (JEDEC), p. 42.

Patent Owner Response at 20.

Patent Owner Sur-Reply at 11.

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

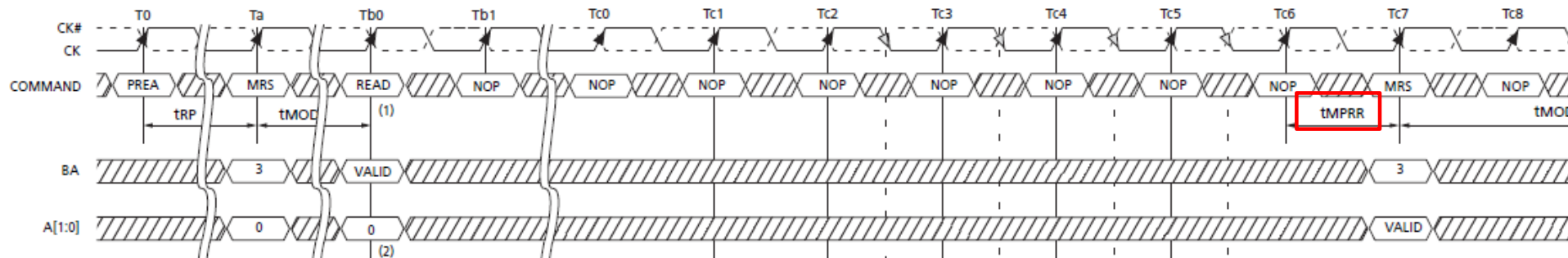
Ex. 2013, p. 39

Samsung Ex. 1086, p. 39

Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2023-00847

DDR3 Describes Only Write leveling Not Read Leveling

- After $RL = AL + CL$, DRAM bursts out the predefined Read Calibration Pattern.
- Memory controller repeats these calibration reads until read data capture at memory controller is optimized.
- After end of last MPR read burst, wait until tMPRR is satisfied.
- MRS MR3, Opcode “A2 = 0b” and “A[1:0] = valid data but value are don’t care”
 - All subsequent read and write accesses will be regular reads and writes from/to the DRAM array.
- Wait until tMRD and tMOD are satisfied.
- Continue with “regular” DRAM commands, like activate a memory bank for regular read or write access,...



EX1020 (JEDEC), p. 51.

4.10.3 Relevant Timing Parameters

The following AC timing parameters are important for operating the Multi Purpose Register: tRP, tMRD, tMOD, and tMPRR. For more details refer to “Electrical Characteristics & AC Timing for DDR3-800 to DDR3-1600” on page 155.

EX1020 (JEDEC), p. 50.

Petitioner’s Reply at 16.

Patent Owner Sur-Reply at 11.

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Ex. 2013, p. 40

Samsung Ex. 1086, p. 40

Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2023-00847

Petitioner's Alleged Motivation To Combine Fails

Petition

It would have been obvious to apply the teachings of Butt to Hiraishi to set the delay for delay circuit 372 in Hiraishi's Figure 5, e.g., by read leveling circuit 323, based on signals received during a prior read leveling process.

EX1003, ¶¶149-150. Hiraishi explicitly calls for “read leveling,” e.g., EX1005, ¶¶[0090],[0140],[0147], Fig.5(323), Fig.13(step S4), Fig.15, and as explained above Butt teaches the details for performing read leveling. Butt

provides the motivation: to “enable[] a reliable data read operation for high speed applications.” EX1029, ¶[0036]. A POSITA would have had a reasonable

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Petition at 47.

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Ex. 2013, p. 41

Samsung Ex. 1086, p. 41

Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2023-00847

Butt's Strobe Centering Was For DDR Memory

physical layer (PHY) core. The circuit 106 may be implemented as one or more double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices. The

EX1029 (Butt), [0015]

[0011] FIG. 4 is a timing diagram illustrating various data and strobe signals of a DDR SDRAM interface;

EX1029 (Butt), [0011]

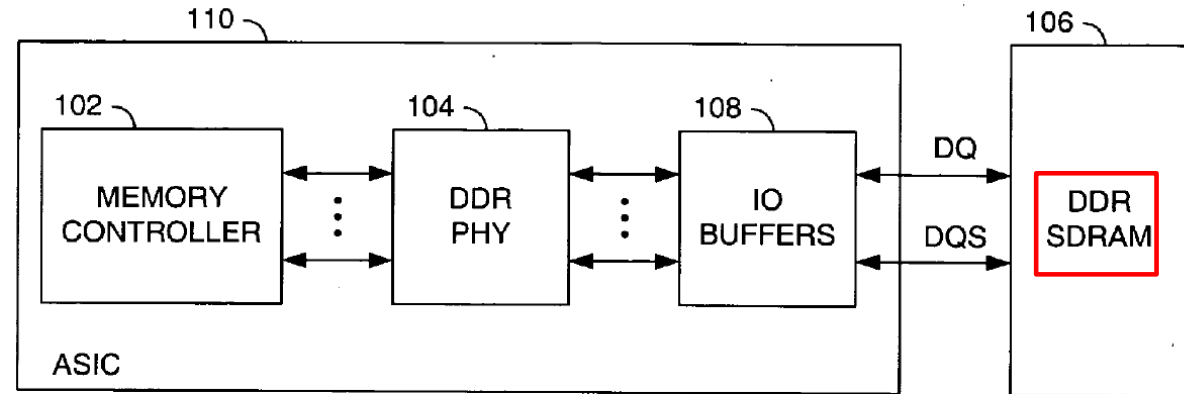
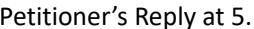


FIG. 1

The Samsung logo, consisting of the word "SAMSUNG" in white, bold, sans-serif capital letters, centered within a blue oval.

Ex. 2013, p. 43

Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2023-00847

TOPICS

GROUND 1-3

Brief Technical Background Of The “Strobe Delay Feature”

Hiraishi Does Not Meet The “Strobe Delay Feature”

Hiraishi-Butt Also Does Not Meet the Strobe Delay Feature

A POSA Would Not Modify Hiraishi With Butt’s Strobe Centering

GROUND 4-5

Hiraishi-Tokuhiro Does Not Meet the “Sampling” Limitation

A POSA Would Not Have Modified Hiraishi with Tokuhiro As Proposed

Hiraishi-Tokuhiro Is Inoperable – No Reasonable Chance of Success

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Ex. 2013, p. 44

Samsung Ex. 1086, p. 44

Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2023-00847

Hiraishi-Tokuhiro (Ground 4) Does Not Satisfy the “Sampling” Limitation

1[g] | sample the first section of the read data using the first delayed read strobe; and

14[k] | sampling the first section of the read data using the first delayed read strobe; and

Petition

4. Claim 1

Claim limitations 1[pre] through 1[e], **1[g]**, and 1[h] are disclosed by Hiraishi alone or with Butt as explained in Ground 1. *Supra*, §§VI.A.1.a)-g),i)-

11. Claim 14

Claim limitations 14[pre] through 14[i], **14[k]**, and 14[l] are disclosed by Hiraishi and Butt with Tokuhiro for the same reasons described in Ground 1.

How The “Sampling” Limitation Is Alleged To be Satisfied In Ground 1

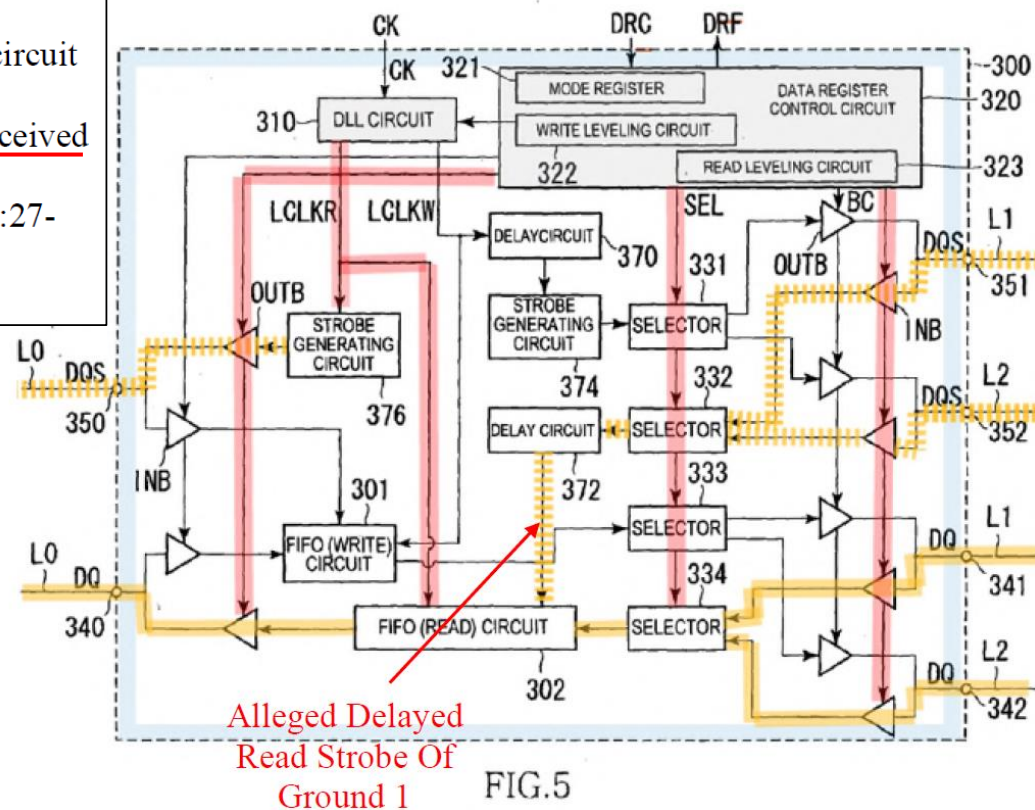
A POSITA would have understood that, when the data signal is latched in the FIFO, it necessarily is sampled (registered) and, because the delayed DQS signal acts “as an input trigger signal” to latch the data in the FIFO (Read) circuit 302, this is necessarily done in accordance with the delayed strobe signal received from delay circuit 372. EX1003, ¶132; EX1005, [0091]; see also EX1001, 13:27-29, 17:15-18 (discussing sampling).

Petition, 37

Q. And in your opinion, that delayed read strobe from 372 is sampling the read data in the FIFO 302?

A. Yes. It would have to. If it doesn't sample it, how is it going to capture it?

EX2008 (Wedig Deposition), 102:4-7



Patent Owner Response at 51.

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Ex. 2013, p. 46

Samsung Ex. 1086, p. 46

Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2023-00847

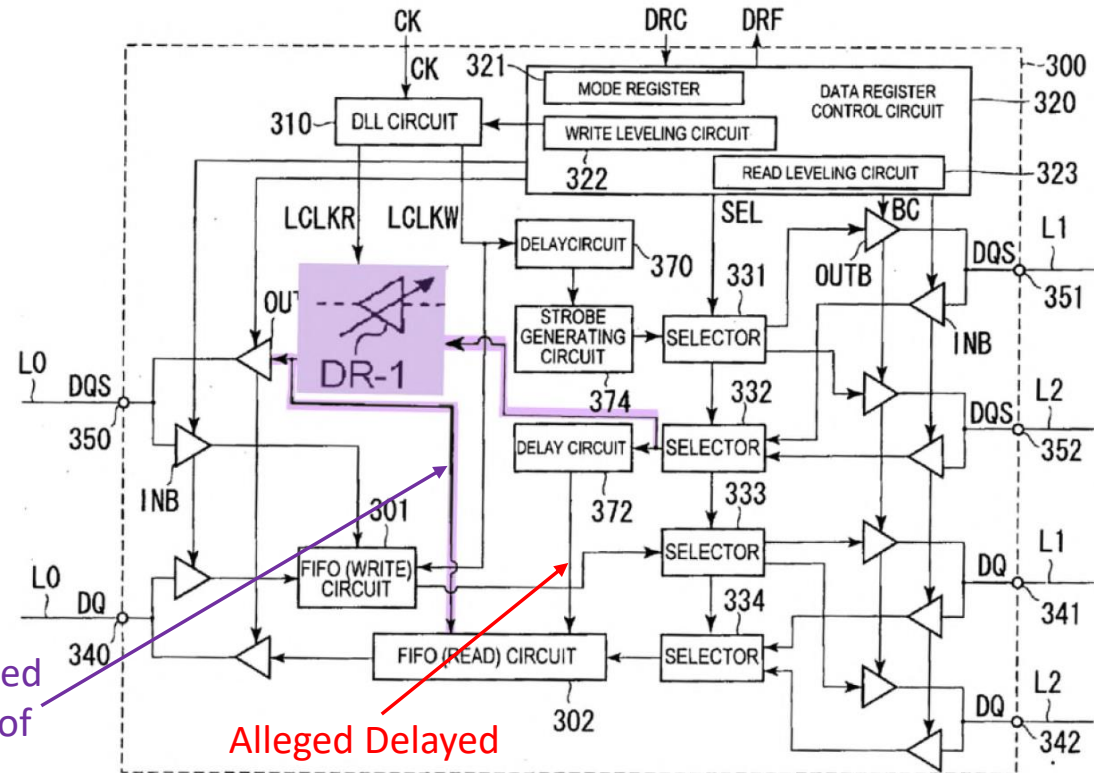
Hiraishi-Tokuhiro (Ground 4) Does Not Satisfy the “Sampling” Limitation

Therefore, the modified data buffer 300-0 would be configured to “*delay the first read strobe* [e.g., DQS from selector 332 to purple delay element DR-1, as taught by Tokuhiro] *a first predetermined amount* [e.g., the amount calculated as taught by Tokuhiro to remove fly-by delays] to generate a first delayed read strobe [e.g., sent to FIFO (Read) Circuit 302].” EX1003, ¶323.

Petition at 121

Alleged Delayed
Read Strobe of
Ground 4

Alleged Delayed
Read Strobe of
Ground 4



Petition at 109.

Patent Owner Response at 55.

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Ex. 2013, p. 47

Samsung Ex. 1086, p. 47

Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2023-00847

Ground 4's Alleged Delayed Read Strobe Does Not Sample Read Data



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strobe DQS as before to properly latch the incoming data DQ. Based on Tokuhiro's teachings, the added read delay circuit DR-1 is configured to delay the read data strobe signal DQS (purple, received from selector 332, purple) and to use the delayed strobe to clock out data from FIFO (Read) Circuit 302 so that the delayed data DQ from the Read FIFO is in sync with the delayed strobe. EX1003, ¶304; EX1020, p.56; EX1006, 18:53-64. Alternatively, delay elements

Petition at 110

Ground 4's Alleged Delayed Read Strobe Does Not Sample Read Data

Robert Wedig
Samsung's Expert

SAMSUNG

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304. In this exemplary implementation, Tokuhiko's read delay circuit (DR- 216 1, purple) is added to Hiraishi's data buffer to remove the large fly-by delays, while the existing delay circuit 372 continues to make fine timing adjustments to the phase of the incoming strobe DQS as before to properly latch the incoming data DQ. Based on the principles in Tokuhiko, including setting the read delays based on delays in a write operation, the added read delay circuit DR-1 is configured to delay the read data strobe signal DQS (purple, received from selector 332, purple) and to use the delayed strobe to clock out data from FIFO (Read) Circuit 302 so that the delayed data DQ from the Read FIFO is in sync with the delayed strobe....

EX1003 (Wedig Declaration) at ¶304

Ground 4's Alleged Delayed Read Strobe Does Not Sample Read Data

Robert Wedig
Samsung's Expert

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304. In this exemplary implementation, Tokuhiko's read delay circuit (DR- 216 1, purple) is added to Hiraishi's data buffer to remove the large fly-by delays, while the existing delay circuit 372 continues to make fine timing adjustments to the phase of the incoming strobe DQS as before to properly latch the incoming data DQ. Based on the principles in Tokuhiko, including setting the read delays based on delays in a write operation, the added read delay circuit DR-1 is configured to delay the read data strobe signal DQS (purple, received from selector 332, purple) and to use the delayed strobe to clock out data from FIFO (Read) Circuit 302 so that the delayed data DQ from the Read FIFO is in sync with the delayed strobe....

EX1003 (Wedig Declaration) at ¶304

Petitioner's New Theory: Clocking Out Data at the FIFO Output Is the Same as Sampling the Read Data Per the Claims



requirement “utmost importance”). The Board’s regulations authorize the Board to “exclude or give no weight to” arguments not fully described in the petition. 37 C.F.R. § 42.104(b)(5); 37 C.F.R. § 42.23(b). Petitioner’s new theory is not mere elaboration of its previous arguments. Petitioner’s new theory changes how the combination purportedly works by now relying on a signal used to clock out data from the read FIFO, instead of one that latches data into the FIFO, for allegedly satisfying the “sampling” limitation. That is impermissible. *Henny Penny Corp. v. Frymaster LLC*, 938 F.3d 1324, 1330-31 (Fed. Cir. 2019) (“[A]n IPR petitioner may not raise in reply ‘an entirely new rationale’ for why a claim would have been obvious.”).

Patent Owner Sur-Reply at 16.

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Ex. 2013, p. 51

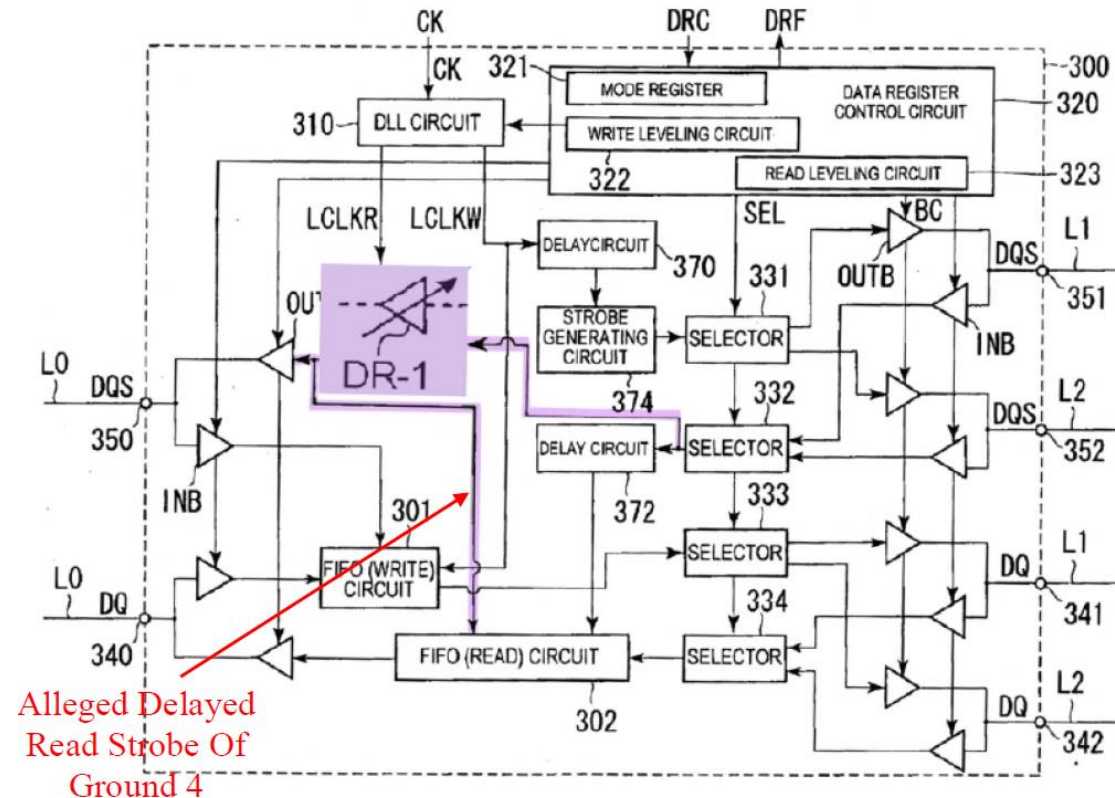
Samsung Ex. 1086, p. 51

Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2023-00847

Petitioner's New "Sampling" Theory

Petitioner's needs to establish that:

- (i) the proposed DQS signal from the DR-1 element is capable of clocking out data from the FIFO's output, and
- (ii) clocking out data from a FIFO's output is sampling within the meaning of the 506 patent.



Dr. Wedig Does Not Suggest That Strobe Signals Can Clock Out Data

Requirement (i): the proposed DQS signal from the DR-1 element is capable of clocking out data from the FIFO's output.

- **Petitioner's Reply:** “Dr. Wedig went on to explain that LCLKR could be used to sample the outgoing DQ (data) signal in the FIFO 302” Reply, 23.

Dr. Wedig Does Not Suggest That Strobe Signals Can Clock Out Data

Requirement (i): the proposed DQS signal from the DR-1 element is capable of clocking out data from the FIFO's output

22 Q. And a clock signal is not a strobe signal,
23 right?
24 MR. CHANDLER: Objection, form.
25 A. No. That's correct. I mean they each
1 have their purpose. But they're not identical, no,
2 that's correct.

EX2008 (Wedig Deposition), 223:22-224:2.

Patent Owner Response at 52.
Patent Owner Sur-Reply at 19.

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Ex. 2013, p. 54

Samsung Ex. 1086, p. 54

Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2023-00847

Dr. Wedig Does Not Suggest That Strobe Signals Can Clock Out Data

Requirement (i): the proposed DQS signal from the DR-1 element is capable of clocking out data from the FIFO's output.

23 So, I may have spoken a little too
24 quickly. Because the LCLKR is a clock, and it does
25 clock the FIFO. So it does, you know, capture state
1 in a FIFO. It captures whatever is at the end, you
2 know, as it's shown in the diagram, and as shown in
3 Figure 5, it captures data at some point near the
4 end of the FIFO.

EX2008 (Wedig Deposition), 219:23-220:3

18 So it does a type of sampling. It does a
19 type of sampling in that this samples the data
20 that's already in the FIFO, but it doesn't -- it
21 does not sample the initial data coming into the
22 FIFO. Only the DQS can do that.
23 That's what I meant to say.

EX2008 (Wedig Deposition), 220:18-23

- **Petitioner's Reply:** "Dr. Wedig went on to explain that LCLKR could be used to sample the outgoing DQ (data) signal in the FIFO 302" Reply, 23.

Patent Owner Response at 52.
Patent Owner Sur-Reply at 19.

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Ex. 2013, p. 55

Samsung Ex. 1086, p. 55

Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2023-00847

Hiraishi Does Not Suggest That Strobe Signals Can Clock Out Data

Requirement (i): the proposed DQS signal from the DR-1 element is capable of clocking out data from the FIFO's output.

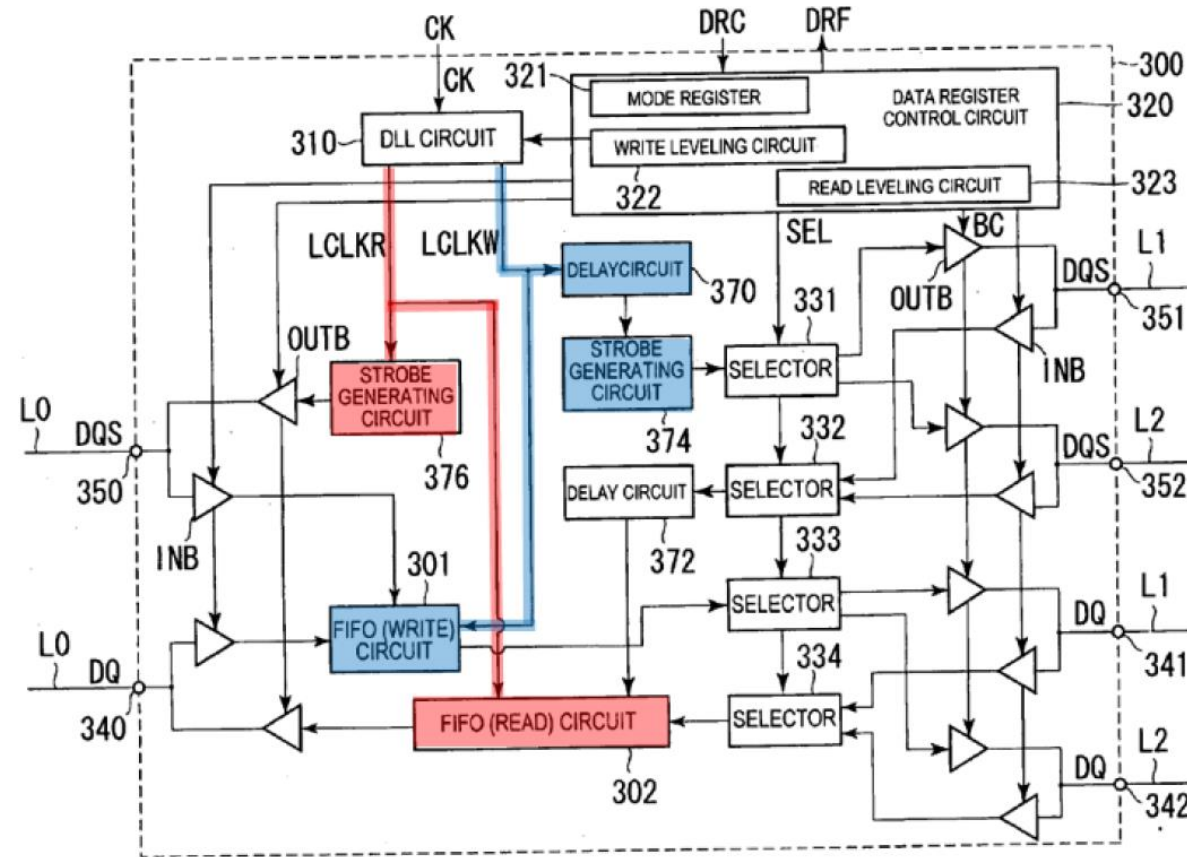


FIG. 5

Patent Owner Response at 61.

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Ex. 2013, p. 56

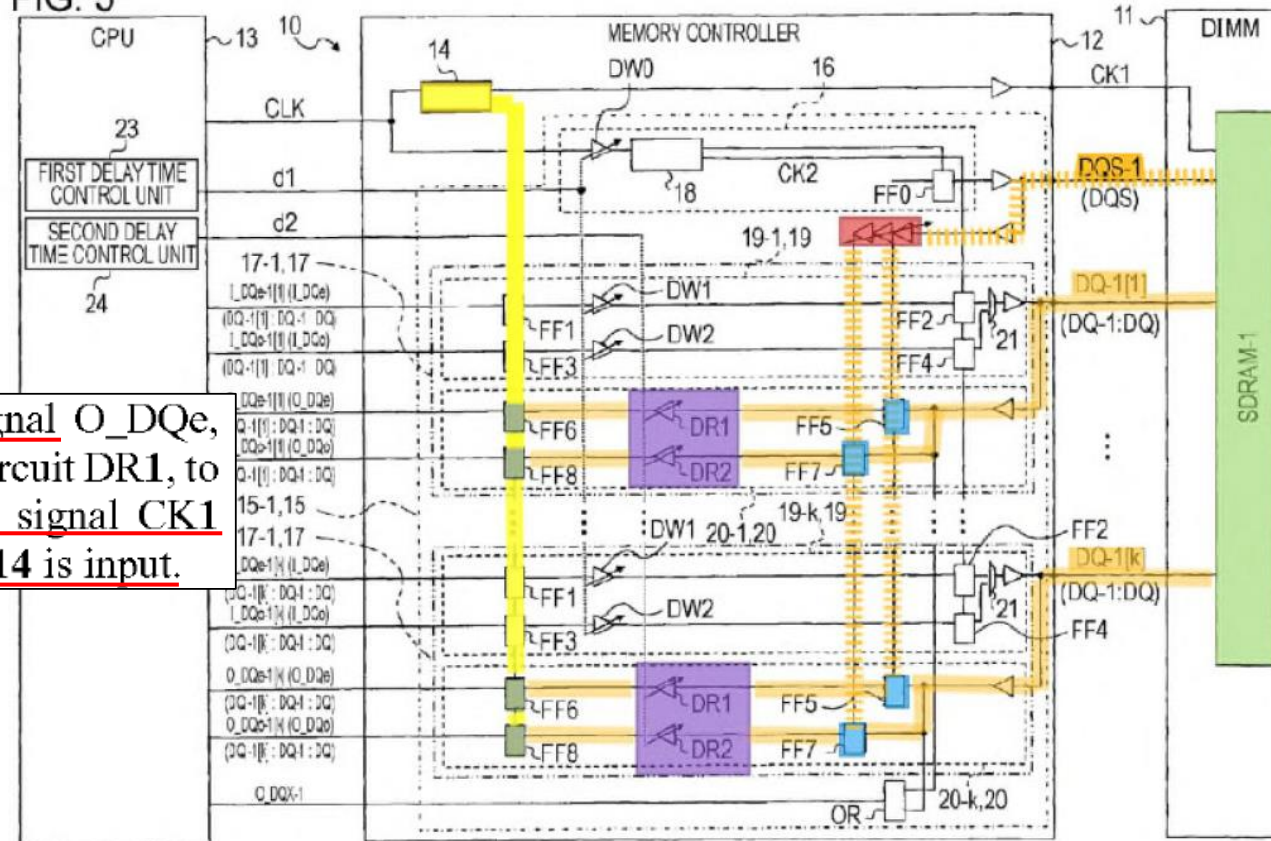
Samsung Ex. 1086, p. 56

Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2023-00847

Tokuhiro Does Not Suggest That Strobe Signals Can Clock Out Data

Requirement (i): the proposed DQS signal from the DR-1 element is capable of clocking out data from the FIFO's output.

FIG. 5



The flip-flop FF6 outputs the third data signal O_DQe, which is input from the second variable delay circuit DR1, to the CPU 13 (described later) when the clock signal CK1 generated from the first clock signal generator 14 is input.

The Claims Sample a First Section of Read Data Using Delayed Strobe

Requirement (i): the proposed DQS signal from the DR-1 element is capable of clocking out data from the FIFO's output.

delay the first read strobe by a first predetermined amount to generate a first delayed read strobe;
sample the first section of the read data using the first delayed read strobe; and
transmit the first section of the read data to a first section of the data bus;

The '506 Does Not Suggest That Strobe Signals Can Clock Out Data

Requirement (i): the proposed DQS signal from the DR-1 element is capable of clocking out data from the FIFO's output.

of the enable signals ENA or ENB. The selected read data signal is delayed in a delay circuit 1660 by an amount controlled by the delay signal DS. The delayed read data signal is then sampled by a receiver circuit 1670 according to the read strobe RDQS from the DQS routing circuit 620, and transmitted by transmitter 1680 onto the corresponding data signal line 130 via the first DQ pin 1601.

506 Patent, 17:54-58

17 Q. And what does the CK0 clock signal and DS
18 delay signal going into 1660 do?
19 A. Well, as best I recall, the DS, the delay
20 signal, delays the input, the YB values. And then
21 once they pass through that delay, they are clocked
22 when CK0 is asserted.

EX1046 (Mangione-Smith), 112:17-22

Patent Owner Sur-Reply at 19-20.

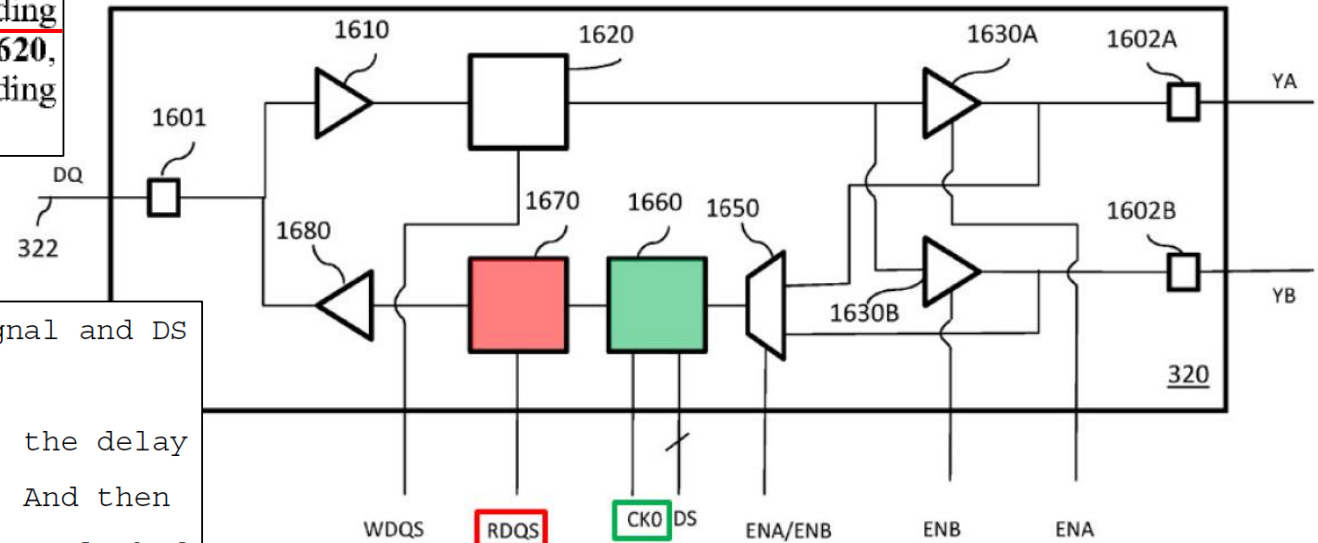


FIG. 16

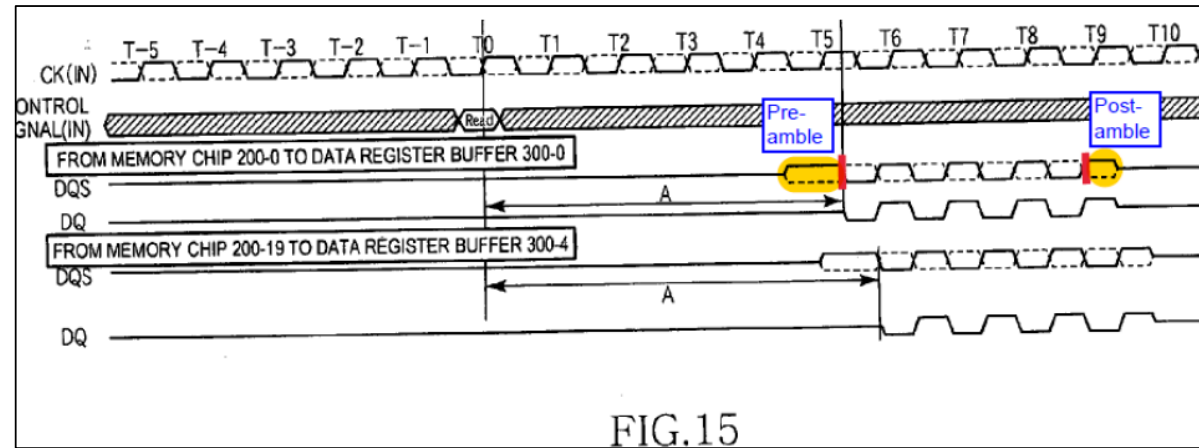
DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Ex. 2013, p. 59

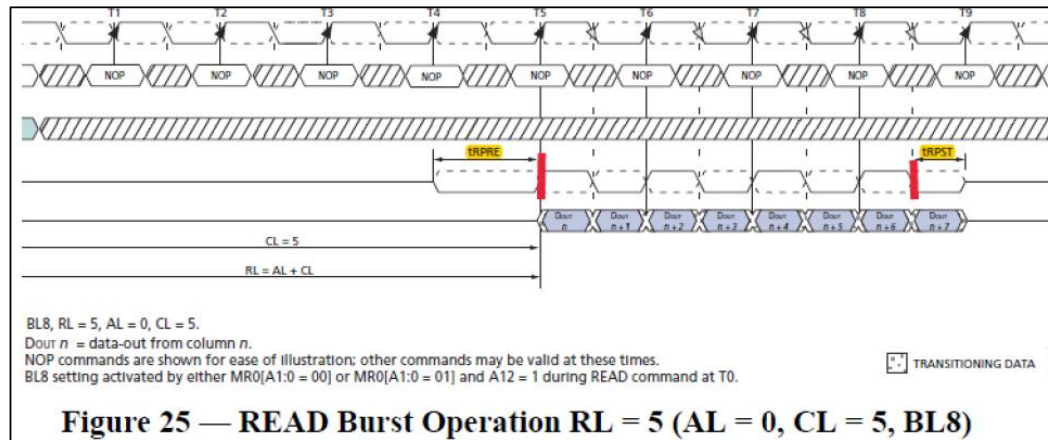
Samsung Ex. 1086, p. 59

Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2023-00847

Using DQS Signals To Clock Out Data Would Lead To Failures



Hiraishi, FIG. 15



EX1020 at 56.

Patent Owner Sur-Reply at 23.

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Ex. 2013, p. 60

Samsung Ex. 1086, p. 60

Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2023-00847

A POSA Would Not Use A Strobe Signal To Clock Out Data

Requirement (i): the proposed DQS signal from the DR-1 element is capable of clocking out data from the FIFO's output.

William Mangione-Smith
Netlist's Expert



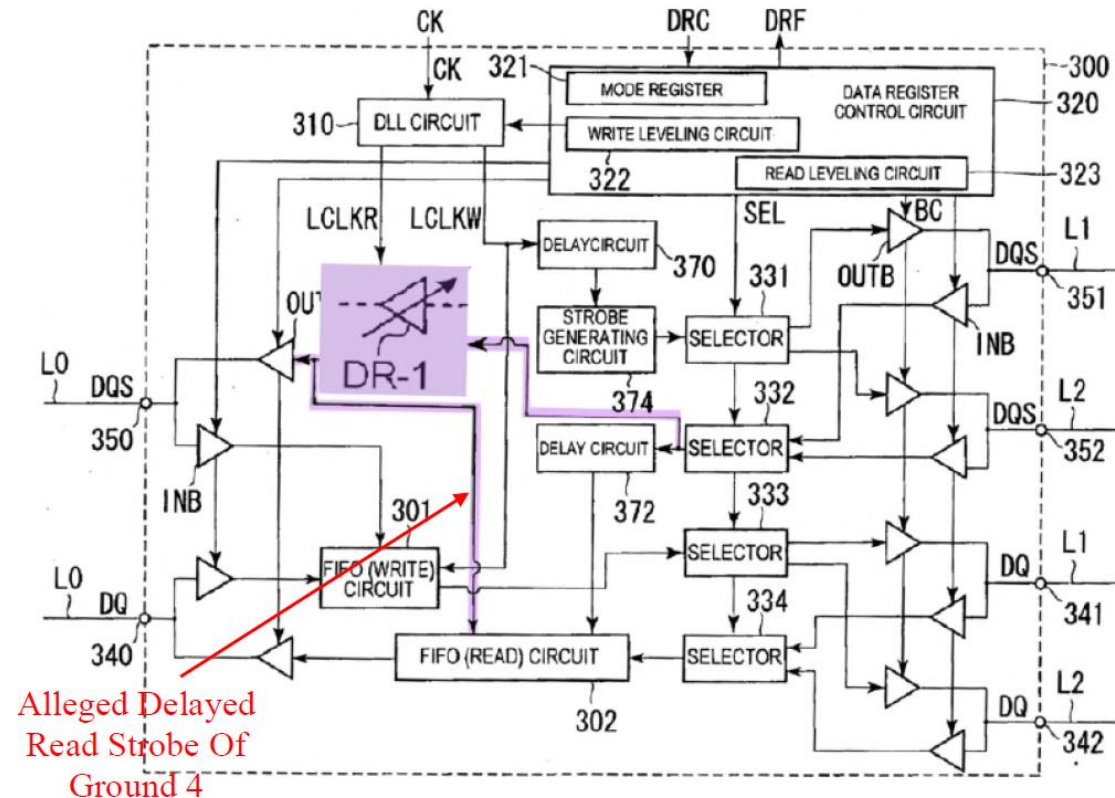
made, the DQS will still be ahead of the DQ data. Moreover, clocking out data with a DQS signal would mean the data is only being clocked out at an edge of the DQS signal, which in all likelihood will not be the correct timing. This is why Hiraishi uses a clock signal to clock out data from the FIFO.

EX2006 (Mangione-Smith Declaration), ¶156

Petitioner's New "Sampling" Theory

Petitioner's needs to establish that:

- (i) the proposed DQS signal from the DR-1 element is capable of clocking out data from the FIFO's output, and
- (ii) clocking out data from a FIFO's output is sampling within the meaning of the 506 patent.**



Petitioner's New "Sampling" Theory

Robert Wedig
Samsung's Expert

SAMSUNG

Requirement (ii): clocking out data from a FIFO's output is the claimed "sampling"

24 First of all, it would be impossible to
25 sample the data with the LCLKR, because the LCLKR
1 doesn't know whether the data is valid. It's only
2 the DQS signal that tells you when the value on the
3 DQ signal is valid. So it's got to be the DQS
4 signal. LQR would not know when the data is valid.
5 Until it gets into the FIFO and now it's
6 being passed down the line, and it takes that value
7 after it's been captured already, then LQR passes it
8 out to the memory controller.

Patent Owner Sur-Reply at 17.
Patent Owner Response at 53.

EX2008 (Wedig Deposition), 104:24-105:5

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Ex. 2013, p. 63

Samsung Ex. 1086, p. 63

Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2023-00847

Petitioner's New "Sampling" Theory

Robert Wedig
Samsung's Expert

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8 And so by my understanding of the word
9 sample, sample meaning the normal English word of
10 sample; that is, to take a sample of or to get a
11 copy of, it does do a type of sampling.

EX2008 (Wedig Deposition), 220: 8-11

Petitioner's New "Sampling" Theory

Requirement (ii): clocking out data from a FIFO's output is the claimed "sampling"

of the enable signals ENA or ENB. The selected read data signal is delayed in a delay circuit 1660 by an amount controlled by the delay signal DS. The delayed read data signal is then sampled by a receiver circuit 1670 according to the read strobe RDQS from the DQS routing circuit 620, and transmitted by transmitter 1680 onto the corresponding data signal line 130 via the first DQ pin 1601.

506 Patent, 17:54-58

delay the first read strobe by a first predetermined amount to generate a first delayed read strobe;
sample the first section of the read data using the first delayed read strobe; and
transmit the first section of the read data to a first section of the data bus;

506 Patent, Claim 1

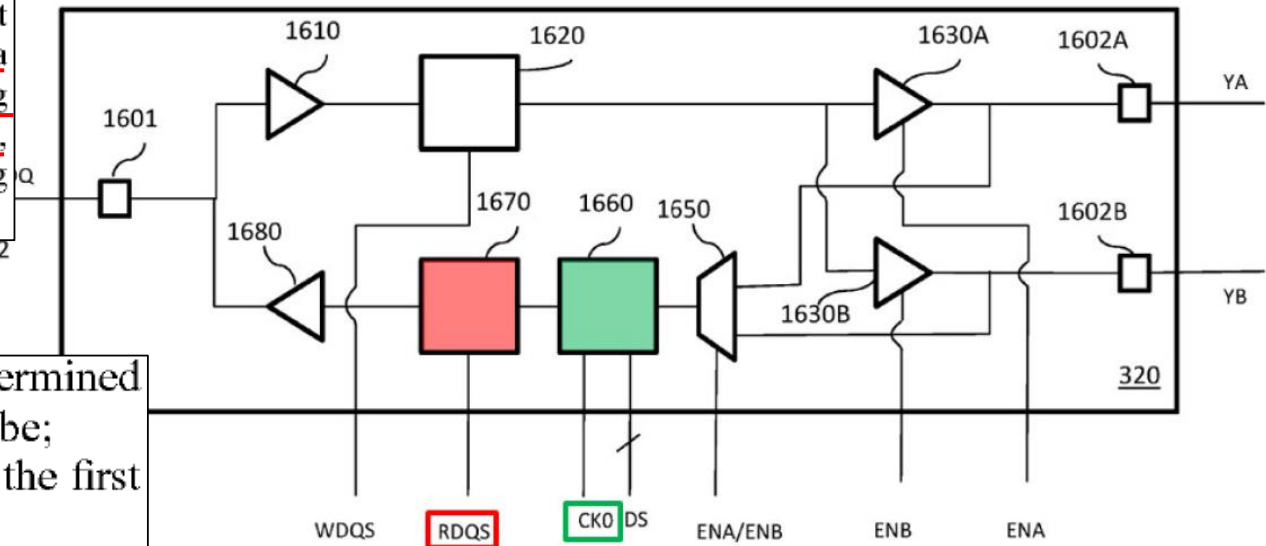


FIG. 16

TOPICS

GROUND 1-3

Brief Technical Background Of The “Strobe Delay Feature”

Hiraishi Does Not Meet The “Strobe Delay Feature”

Hiraishi-Butt Also Does Not Meet the Strobe Delay Feature

A POSA Would Not Modify Hiraishi With Butt’s Strobe Centering

GROUND 4-5

Hiraishi-Tokuhiro Does Not Meet the “Sampling” Limitation

A POSA Would Not Have Modified Hiraishi with Tokuhiro As Proposed

Hiraishi-Tokuhiro Is Inoperable – No Reasonable Chance of Success

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Ex. 2013, p. 66

Samsung Ex. 1086, p. 66

Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2023-00847

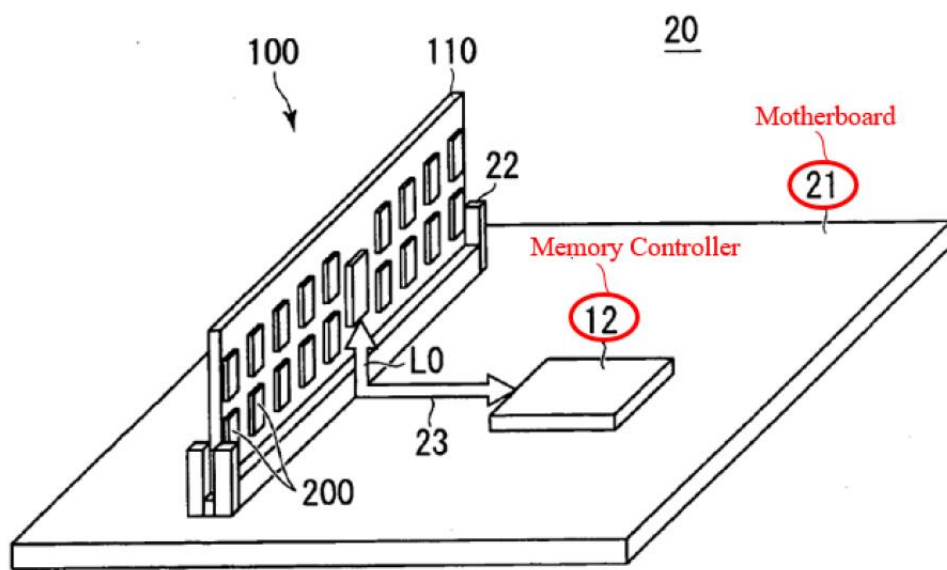
No Motivation to Combine Hiraishi And Tokuhiro As Proposed

Petitioner's alleged motivation to combine:

- (1) To use “Tokuhiro’s technique of setting the read delays based on the write delays” to simplify Hiraishi’s independent write and read leveling operations. Pet. 98.**
- (2) To remove fly-by delays, “making the read data arrive at the memory controller from the different data buffers at substantially the same time.” Pet., 100.**
- (3) To remove “fly-by delays that are greater than one clock cycle.” Pet., 101.**

The Samsung logo, consisting of the word "SAMSUNG" in white capital letters inside a blue oval.

No Motivation to Combine Hiraishi And Tokuhiro As Proposed



Hiraishi, FIG. 3

14 So as between the memory controller and
15 the data buffer, is the purpose of Hiraishi's S5
16 leveling to account for fly-by delays?
17 A. Yeah, that's my understanding. I mean, it
18 helps to even out the fly-by delays into the
19 memory -- into the memory controller.

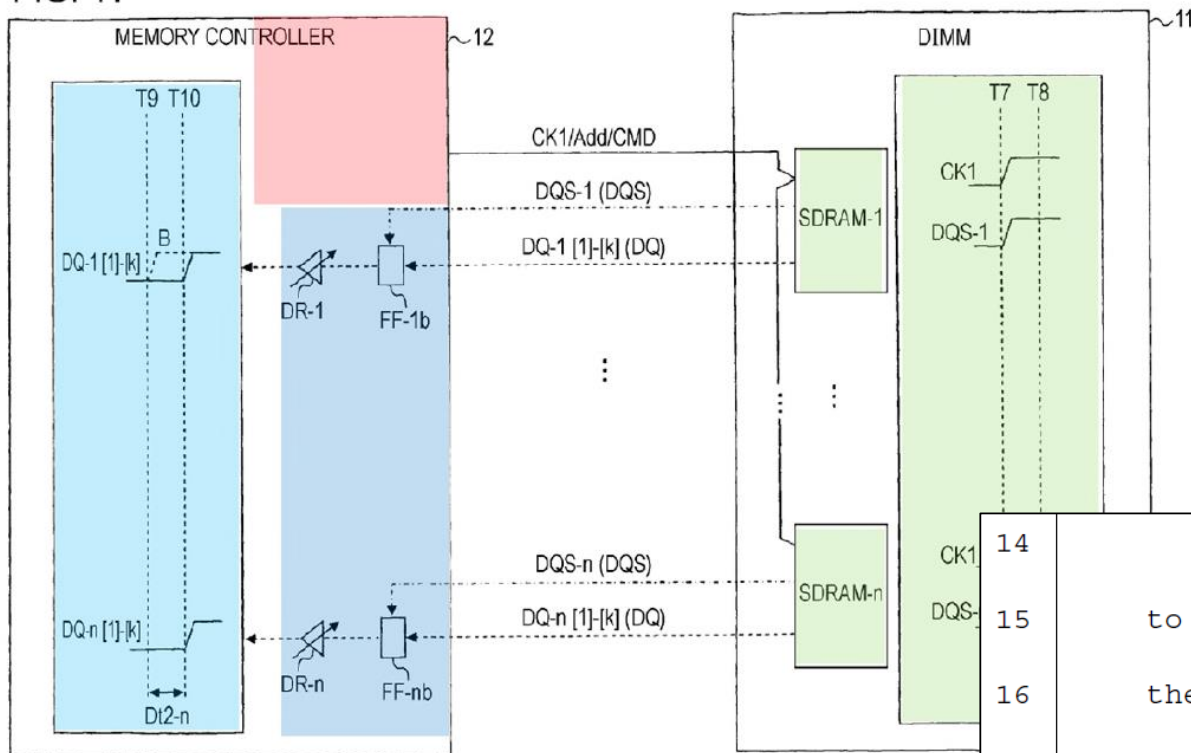
EX2008 (Wedig Deposition), 79:14-19.

9 Q. So at that point, Hiraishi has removed
10 fly-by delays between the memory controller and the
11 data buffer?
12 MR. CHANDLER: Objection, form.
13 A. Effectively, yes.

EX2008 (Wedig Deposition), 170:9-13.

No Motivation to Combine Hiraishi And Tokuhiro As Proposed

FIG. 11



Tokuhiro, FIG. 11

14 A. Because the whole purpose of Tokuhiro is
 15 to -- the whole purpose of Tokuhiro is it will solve
 16 the problem of fly-by delays, and that is to make it
 17 so that the data arrives to the memory controller at
 18 the same time.

EX2008 (Wedig Deposition), 161:14-18.

No Motivation to Combine Hiraishi And Tokuhiro As Proposed

Robert Wedig
Samsung's Expert

The Samsung logo, consisting of the word "SAMSUNG" in white capital letters inside a blue oval.

307. A Skilled Artisan would have understood that an important advantage of this combination is that the memory controller (MCH) receives all read data at substantially the same time, so it does not need to manage large fly-by delays of read data either during the training or during normal operation as it tries to capture the correct value of the read data. Accordingly, the memory controller can be implemented with less circuitry and functionality. For example, the memory controller does not need extra logic and circuitry (e.g., FIFOs) to re-order read data that has been captured in different clock cycles due to the larger than clock cycle fly-by delays on the module.

EX1003 (Wedig Declaration), ¶1307.

Petition at 103.

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Ex. 2013, p. 70

Samsung Ex. 1086, p. 70

Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2023-00847

No Motivation to Combine Hiraishi And Tokuhiro As Proposed

Robert Wedig
Samsung's Expert

SAMSUNG

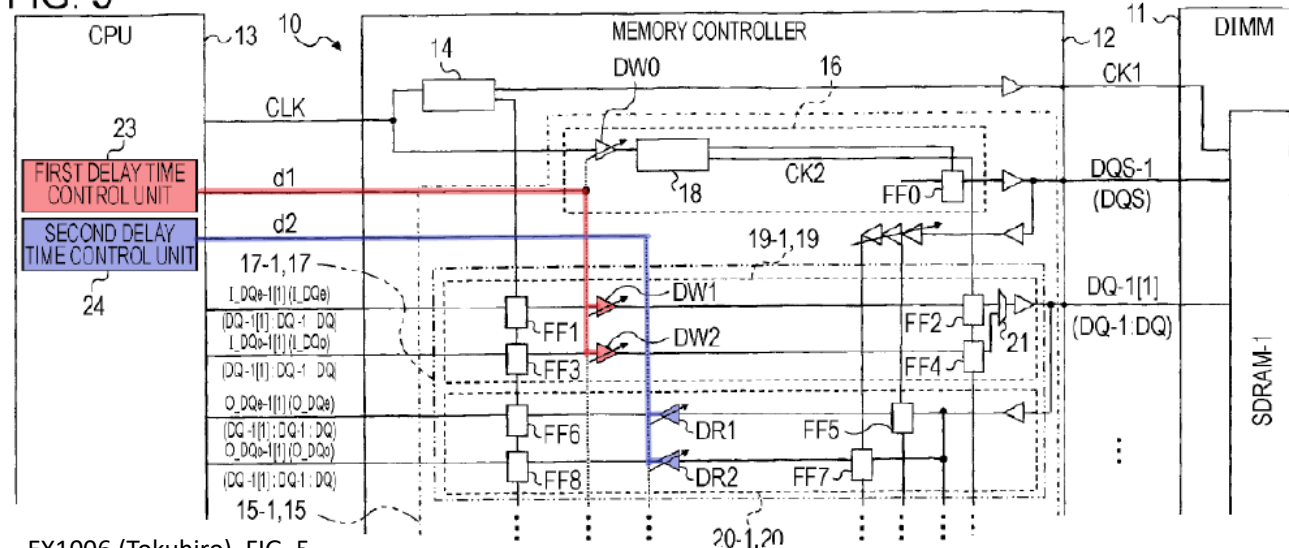
Q. In the combination of Hiraishi and Tokuhiro, Hiraishi's memory controller is still adjusting the incoming data so that it is being captured in the valid data eye?

A. Yeah, just like it was before. I mean, there's no -- you had to do that when you did before you ever added Tokuhiro.

EX2008, 181:9-15.

No Motivation to Combine Hiraishi And Tokuhiro As Proposed

FIG. 5



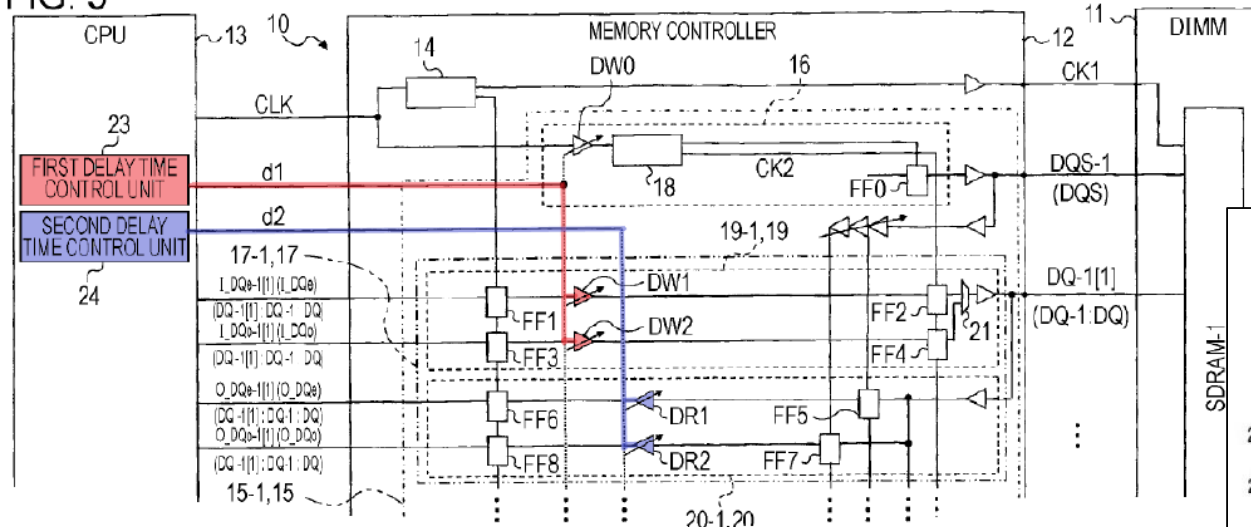
EX1006 (Tokuhiro), FIG. 5

More specifically, for the n-channel SDRAM-n, the first delay time control unit 23 (not shown in FIG. 7) gradually prolongs the delay time for the first variable delay circuit DW-n until the clock signal CK1 and the data strobe signal DQS-n are input to the n-channel SDRAM-n substantially at the same time. Then, the first delay time control unit 23

EX1006 (Tokuhiro), 13:55-60

No Motivation to Combine Hiraishi And Tokuhiro As Proposed

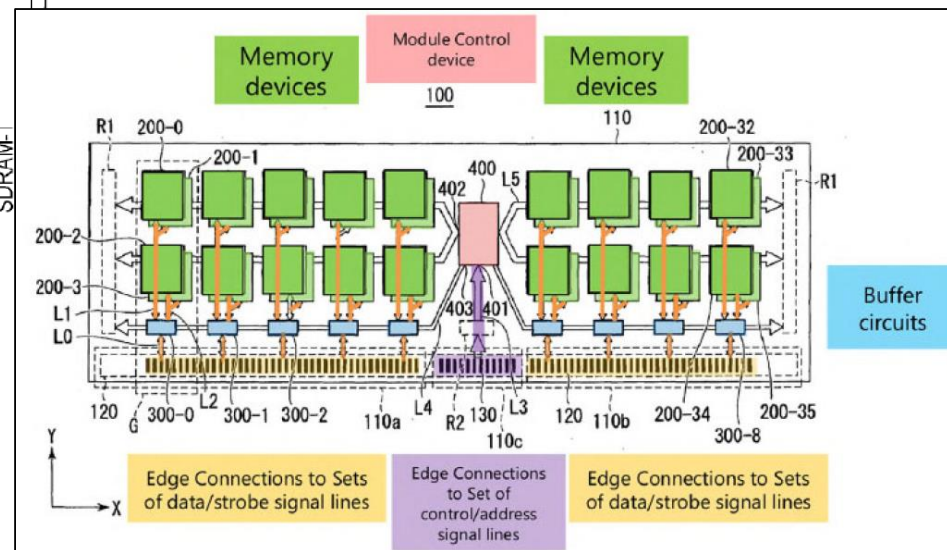
FIG. 5



EX1006 (Tokuhiro), FIG. 5

19 Q. Now, in Tokuhiro d1 and d2, those are
 20 dedicated control signal lines coming out of the CPU
 21 into the memory controller; is that right?
 22 A. That's the way Tokuhiro shows it. That's
 23 the way he chose to implement it. That's correct.

EX2008 (Wedig Deposition), 155:19-23



EX1005 (Hiraishi), FIG. 5 (annotated by Petition at 14).

No Motivation to Combine Hiraishi And Tokuhiko As Proposed

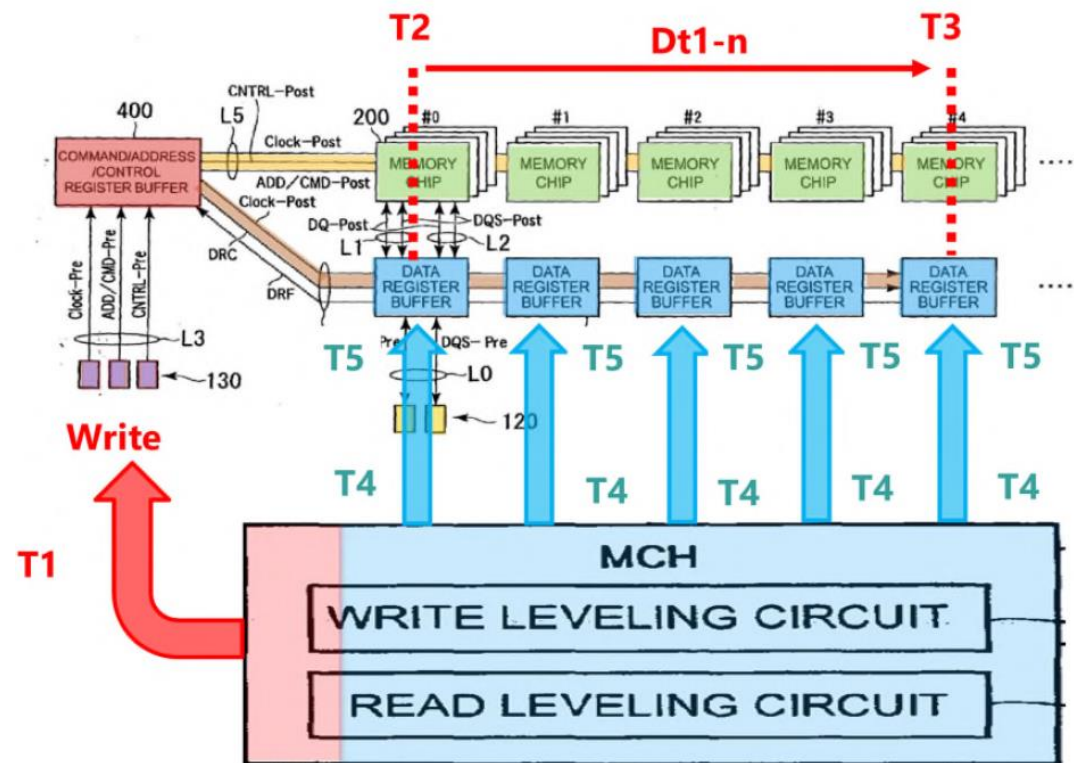
4	But just at a very high level, you need to
5	be able to have circuitry -- you need to be able to
6	have logic, which is already basically there, a lot
7	of it is already there, but you might need to modify
8	some of it to be able to detect the delay, to be
9	able to measure the delay, and then you need to be
10	able to rewrite the -- you need to be able to write
11	the delay for the read path into DR1.
12	And so the basic control logic is there.
13	So you would need to make some changes to that.

EX2008 (Wedig Deposition), 152:4-13.

11	So you would need to make some changes to
12	that, and then you would need to be able to provide
13	some feedback to the module controller.

EX2008 (Wedig Deposition), 151:11-13.

No Motivation to Combine Hiraishi And Tokuhiro As Proposed



Second Implementation

Petition at 117.

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Ex. 2013, p. 75

Samsung Ex. 1086, p. 75

Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2023-00847

Samsung's Motivation Arguments Fail

Petitioner's alleged motivation to combine:

- (1) To use “Tokuhiko’s technique of setting the read delays based on the write delays” to simplify Hiraishi’s independent write and read leveling operations. Pet. 98.**
- (2) To remove fly-by delays, “making the read data arrive at the memory controller from the different data buffers at substantially the same time.” Pet., 100.**
- (3) To remove “fly-by delays that are greater than one clock cycle.” Pet., 101.**

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Samsung's Motivation Arguments Fail

Petitioner's alleged motivation to combine:

- (1) To use “Tokuhiro’s technique of setting the read delays based on the write delays” to simplify Hiraishi’s independent write and read leveling operations. Pet. 98.**
- (2) To remove fly-by delays, “making the read data arrive at the memory controller from the different data buffers at substantially the same time.” Pet., 100.
- (3) To remove “fly-by delays that are greater than one clock cycle.” Pet., 101.

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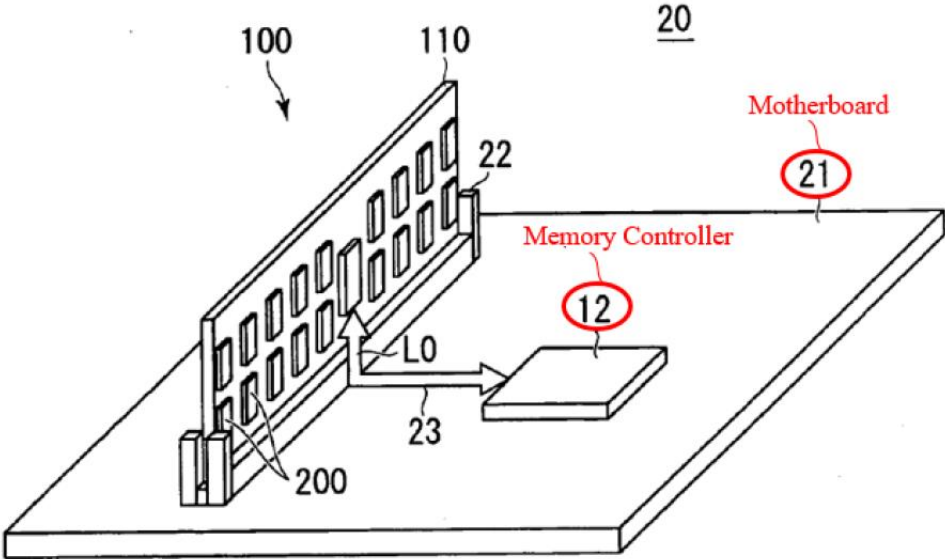
Samsung's Motivation Arguments Fail

Petitioner's alleged motivation to combine:

- (1) To use “Tokuhiko’s technique of setting the read delays based on the write delays” to simplify Hiraishi’s independent write and read leveling operations. Pet. 98.
- (2) To remove fly-by delays, “making the read data arrive at the memory controller from the different data buffers at substantially the same time.” Pet., 100.**
- (3) To remove “fly-by delays that are greater than one clock cycle.” Pet., 101.

The Samsung logo, consisting of the word "SAMSUNG" in white capital letters inside a blue oval.

Samsung's Motivation Arguments Fail



Hiraishi, FIG. 3

14 So as between the memory controller and
15 the data buffer, is the purpose of Hiraishi's S5
16 leveling to account for fly-by delays?

17 A. Yeah, that's my understanding. I mean, it
18 helps to even out the fly-by delays into the
19 memory -- into the memory controller.

EX2008, 79:14-19

9 Q. So at that point, Hiraishi has removed
10 fly-by delays between the memory controller and the
11 data buffer?

12 MR. CHANDLER: Objection, form.

13	A. Effectively, yes.
----	----------------------

EX2008, 170:9-13.

Samsung's Motivation Arguments Fail

Petitioner's alleged motivation to combine:

- (1) To use “Tokuhiro’s technique of setting the read delays based on the write delays” to simplify Hiraishi’s independent write and read leveling operations. Pet. 98.
- (2) To remove fly-by delays, “making the read data arrive at the memory controller from the different data buffers at substantially the same time.” Pet., 100.
- (3) To remove “fly-by delays that are greater than one clock cycle.” Pet., 101.**

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Samsung's Motivation Arguments Fail

The delay on the order of 1 ns will become greater than a typical data period of the DDR3 memory interface, at minimum 0.625 ns, so that the delay may affect in reading data from the SDRAM 92.

EX1006, 3:9-12

Table 50 — For IDD testing the following parameters are utilized.

Parameter Bin	DDR3-800		DDR3-1066			DDR3-1333			DDR3-1600			Unit
	5-5-5	6-6-6	6-6-6	7-7-7	8-8-8	7-7-7	8-8-8	9-9-9	8-8-8	9-9-9	10-10-10	
$t_{CKmin}(IDD)$	2.5		1.875			1.5			1.25			ns
CL(IDD)	5	6	6	7	8	7	8	9	8	9	10	
$t_{RCDmin}(IDD)$	12.5	15	11.25	13.13	15	10.5	12	13.5	10	11.25	12.5	ns
$t_{RCmin}(IDD)$	50	52.5	48.75	50.63	52.50	46.5	48	49.5	45	46.25	47.5	ns
$t_{RASmin}(IDD)$	37.5	37.5	37.5	37.5	37.5	36	36	36	35	35	35	ns
$t_{RPmin}(IDD)$	12.5	15	11.25	13.13	15	10.5	12	13.5	10	11.25	12.5	ns

EX2006, ¶176

Petition at 94.

Patent Owner Response at 83-84.

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Ex. 2013, p. 81

Samsung Ex. 1086, p. 81

Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2023-00847

Samsung's Motivation Arguments Fail

177. As shown in the table above, for the fastest DDR3-1600 (i.e. data rate is 1600 million transfer per second 1600MTs) the clock period is exactly 1.25 ns. Tokuhiro expressly states that 1 ns is “greater than a typical data period of the DDR3 memory interface,” which at minimum is 0.625 ns (meaning exactly half the 1.25ns = 0.625ns), *see* tCKmin in Table 50 above. Thus, the data period in Tokuhiro is referenced to half a clock cycle where one data bit/word is outputted/transmitted.

EX2006, ¶177

Samsung's Motivation Arguments Fail

William Mangione-Smith

Netlist's Expert



178. I also note that Tokuhiro cannot deal with delays greater than one clock cycle because Tokuhiro determines delays by “gradually prolong[ing] the delay time for the first variable delay circuit DW-n until the clock signal CK1 and the data strobe signal DQS-n are input to the n-channel SDRAM-n substantially at the same time” EX1006, 13:55-60. This process can only align the DQS-n with the next up or down clock edge, as shown in Tokuhiro’s FIG. 7. It would not know to align the DQS to the next up or down clock edge to get to a greater than one clock cycle delay because all clock rising edges look the same and all clock falling edges look the same. Therefore, Tokuhiro can only align the DQS with the next up or down clock edge, which would necessarily occur in less than one clock cycle.

EX2006 (Mangione-Smith Declaration), ¶178

More specifically, for the n-channel SDRAM-n, the first delay time control unit 23 (not shown in FIG. 7) gradually prolongs the delay time for the first variable delay circuit DW-n until the clock signal CK1 and the data strobe signal DQS-n are input to the n-channel SDRAM-n substantially at the same time. Then, the first delay time control unit 23

EX1006 (Tokuhiro), 13:55-60

Patent Owner Response at 84.

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Ex. 2013, p. 83

Samsung Ex. 1086, p. 83

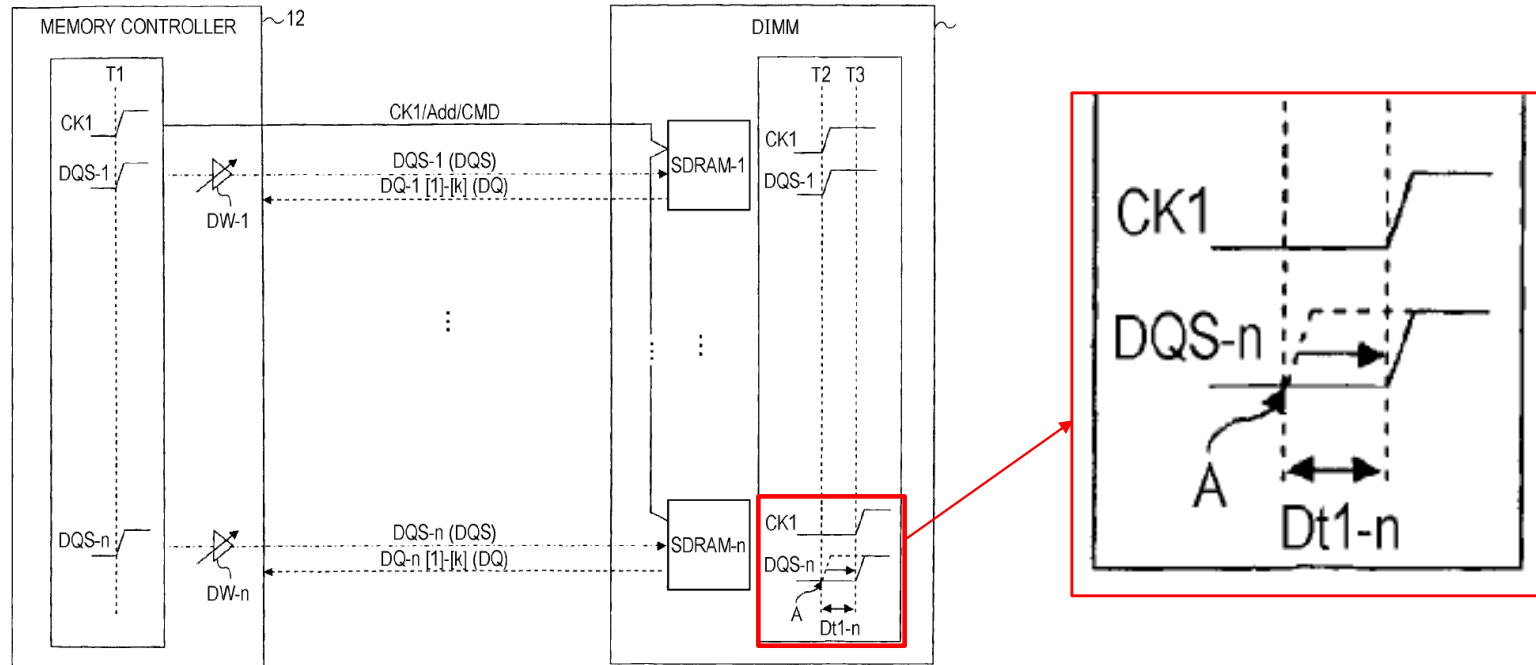
Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2023-00847

Samsung's Motivation Arguments Fail

178. ... This process can only align the DQS-n with the next up or down clock edge, as shown in Tokuhiro's FIG. 7.... Therefore, Tokuhiro can only align the DQS with the next up or down clock edge, which would necessarily occur in less than one clock cycle.

EX2006 (Mangione-Smith Declaration), ¶178

FIG. 7



EX1006, FIG. 7 (cited at EX2006, ¶178)

Patent Owner Response at 84.

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Ex. 2013, p. 84

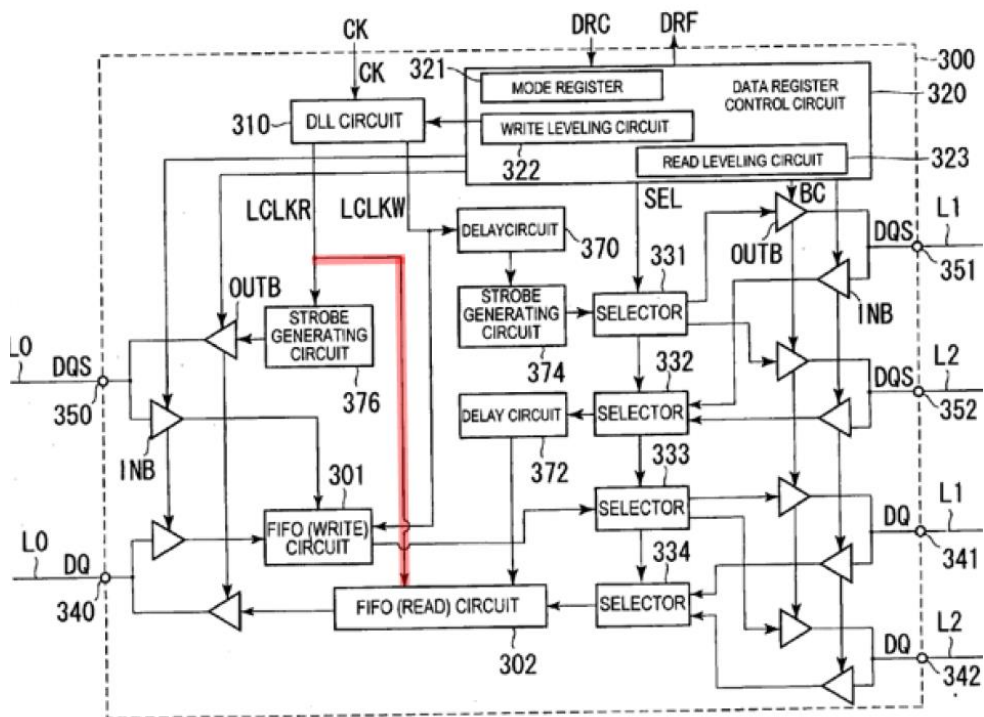
Samsung Ex. 1086, p. 84

Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2023-00847

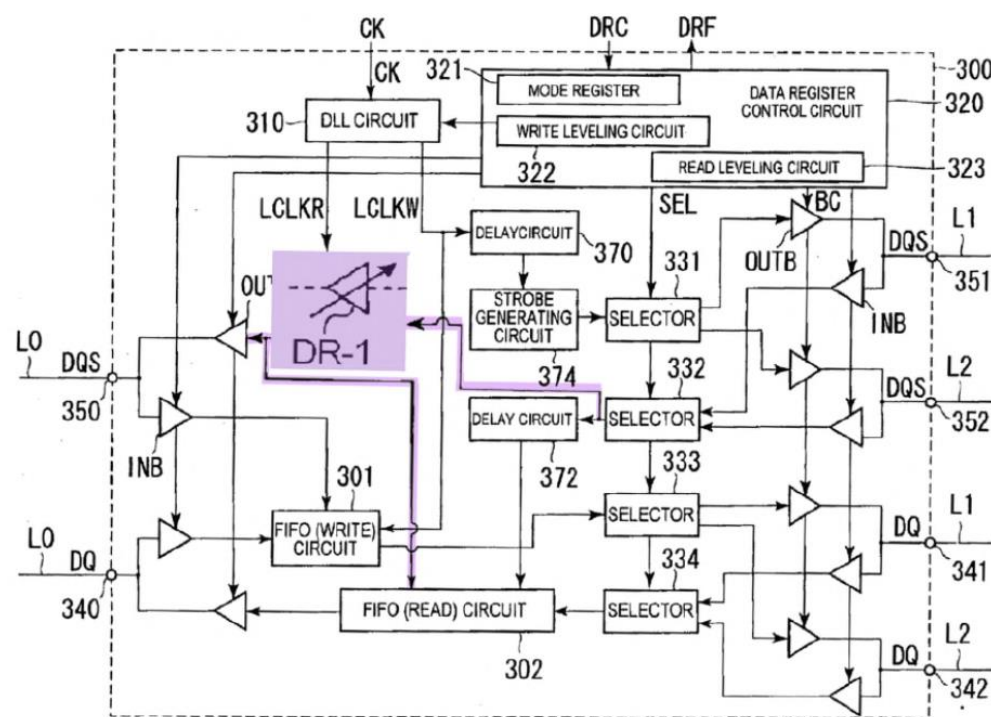
William Mangione-Smith
Netlist's Expert



No Motivation to Remove Hiraishi LCLKR Signal From the FIFO



Hiraishi, FIG. 5



Proposed Combination

TOPICS

GROUND 1-3

Brief Technical Background Of The “Strobe Delay Feature”

Hiraishi Does Not Meet The “Strobe Delay Feature”

Hiraishi-Butt Also Does Not Meet the Strobe Delay Feature

A POSA Would Not Modify Hiraishi With Butt’s Strobe Centering

GROUND 4-5

Hiraishi-Tokuhiro Does Not Meet the “Sampling” Limitation

A POSA Would Not Have Modified Hiraishi with Tokuhiro As Proposed

Hiraishi-Tokuhiro Is Inoperable – No Reasonable Chance of Success

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Ex. 2013, p. 86

Samsung Ex. 1086, p. 86

Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2023-00847

Hiraishi-Tokuhiro Is Inoperable – No Reasonable Chance of Success

15	Have you ever seen a reference that
16	doesn't use the memory controller to adjust for
17	fly-by delays that are going to the memory
18	controller?
19	A. I haven't looked for that. I'm not
20	familiar with it. I haven't searched. It may be
21	there, I just haven't looked.

EX2008 (Wedig Deposition), 171:15-21

First and Second Implementation

18	Q. Have you seen a reference that describes a
19	module controller programming a delay element for
20	read leveling?
21	A. No, not a single reference.

EX2008 (Wedig Deposition), 194:18-21

Second Implementation

Hiraishi-Tokuhiro Is Inoperable – No Reasonable Chance of Success

(1) “first delayed read strobe” cannot be used to clock out the data from the FIFO.

EX2006 (Mangione-Smith Decl.), ¶156

(2) Tokuhiro’s variable delay circuit DR-1 cannot delay the read strobe DQS to convert the read latency to CL=6, as required by Hiraishi.

EX2006 (Mangione-Smith Decl.), ¶157

(3) Tokuhiro’s read and write leveling are controlled, not by its memory controller or any on-module controller, but by the computer’s main CPU.

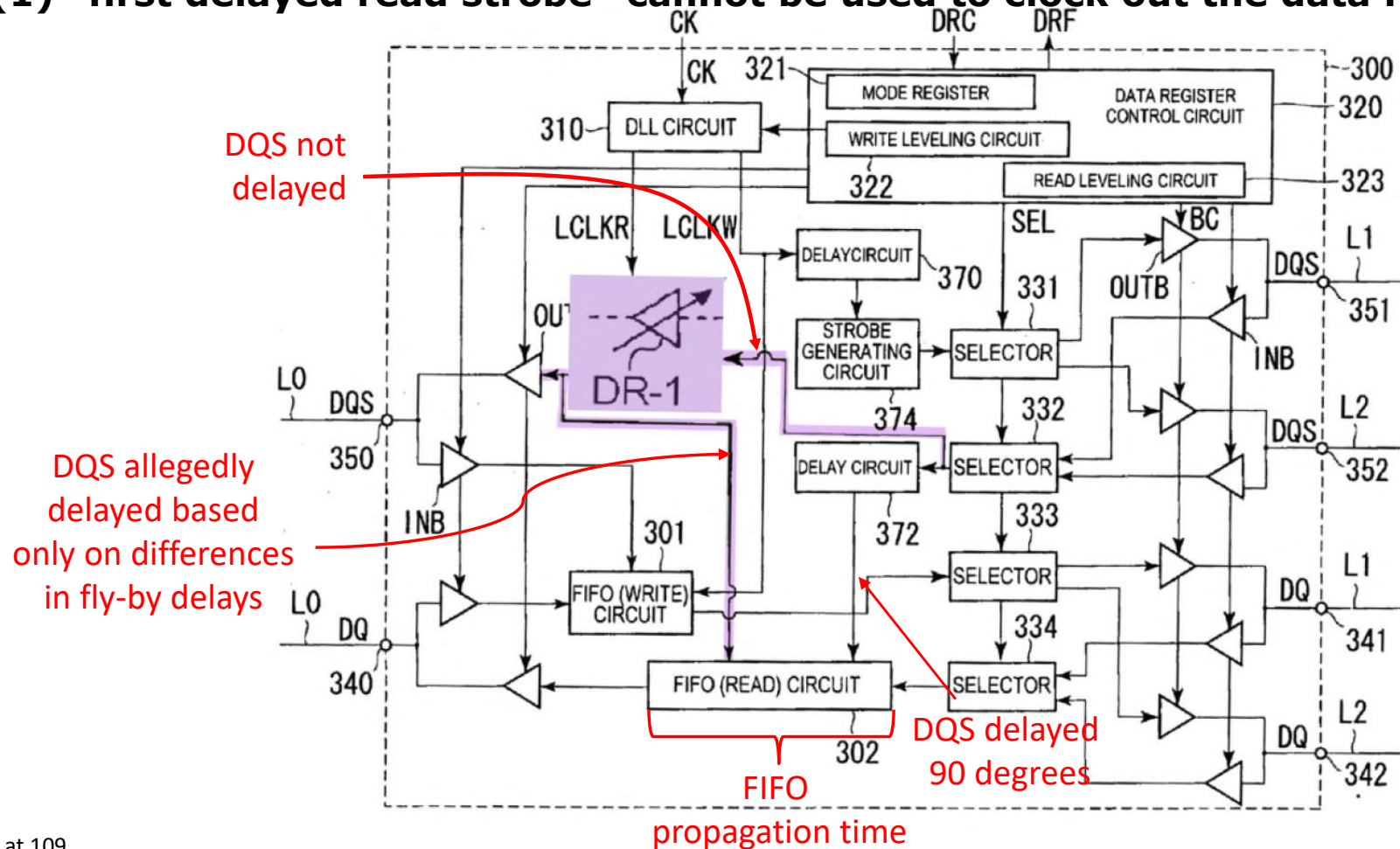
EX2006 (Mangione-Smith Decl.), ¶¶147-151

(4) Tokuhiro’s incorporated delay element DR-1 cannot operate without a control signal comparable to that used by Tokuhiro.

EX2006 (Mangione-Smith Decl.), ¶¶152-155

Hiraishi-Tokuhiro Is Inoperable – No Reasonable Chance of Success

(1) “first delayed read strobe” cannot be used to clock out the data from the FIFO.



Petition at 109.
Patent Owner Response at 66-67.

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

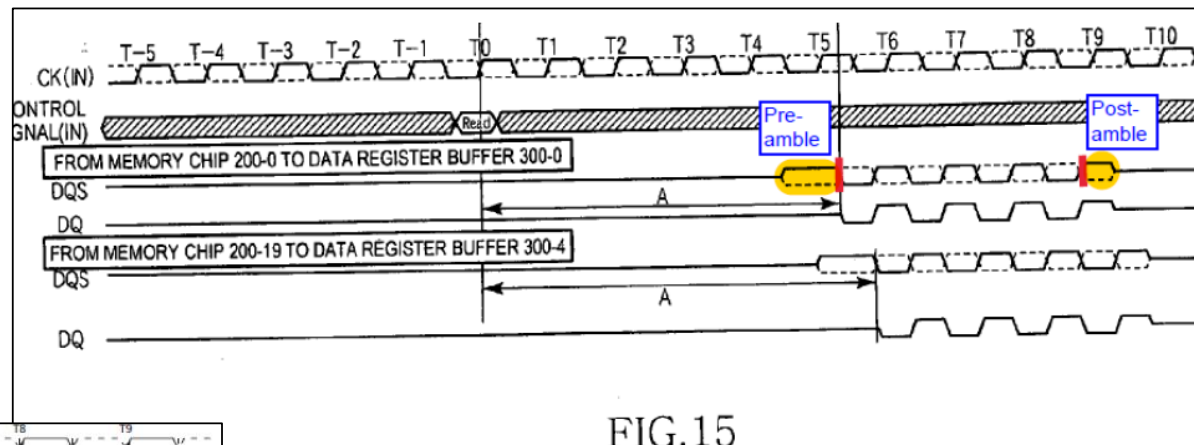
Ex. 2013, p. 89

Samsung Ex. 1086, p. 89

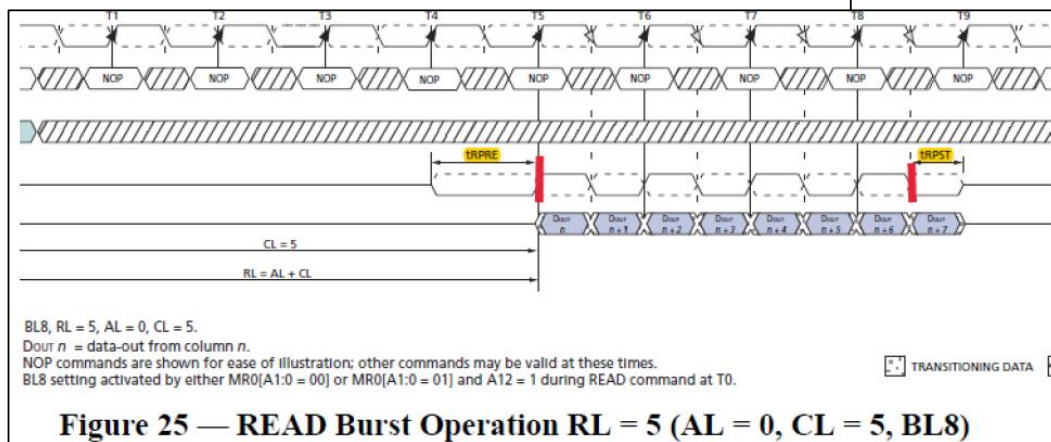
Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2023-00847

Hiraishi-Tokuhiro Is Inoperable – No Reasonable Chance of Success

(1) “first delayed read strobe” cannot be used to clock out the data from the FIFO.



Hiraishi, FIG. 15



EX1020 at 56.

Patent Owner Sur-Reply at 23.

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Ex. 2013, p. 90

Samsung Ex. 1086, p. 90

Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2023-00847

Hiraishi-Tokuhiro Is Inoperable – No Reasonable Chance of Success

(1) “first delayed read strobe” cannot be used to clock out the data from the FIFO.

EX2006 (Mangione-Smith Decl.), ¶156

(2) Tokuhiro’s variable delay circuit DR-1 cannot delay the read strobe DQS to convert the read latency to CL=6, as required by Hiraishi.

EX2006 (Mangione-Smith Decl.), ¶157

(3) Tokuhiro’s read and write leveling are controlled, not by its memory controller or any on-module controller, but by the computer’s main CPU.

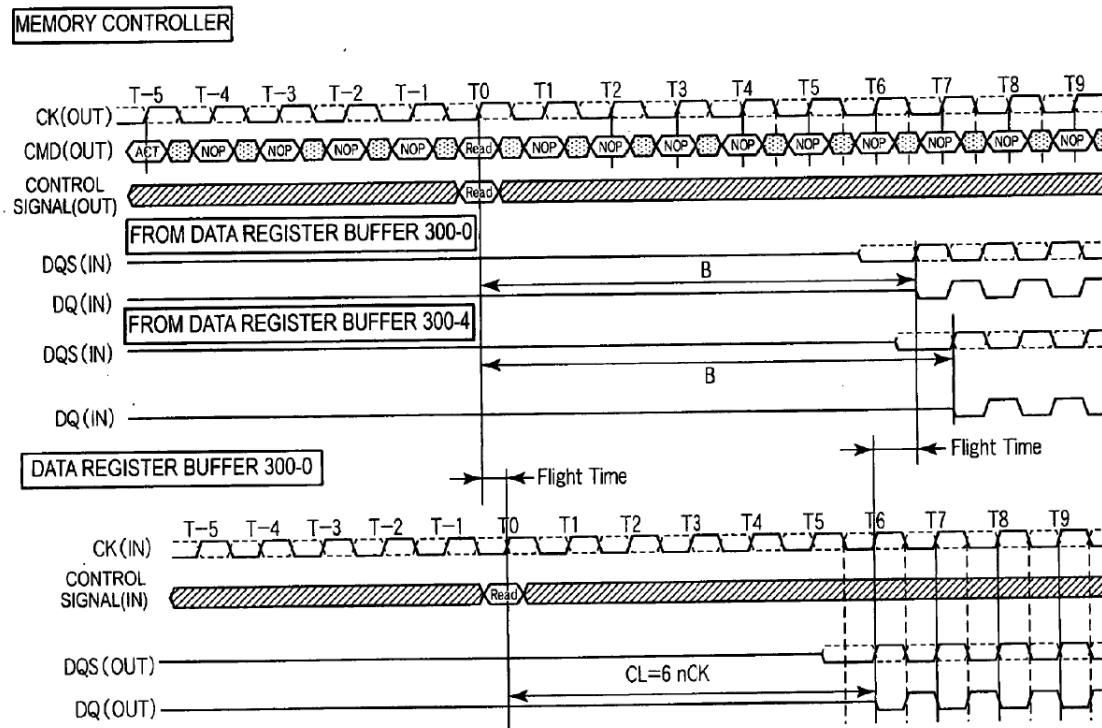
EX2006 (Mangione-Smith Decl.), ¶¶147-151

(4) Tokuhiro’s incorporated delay element DR-1 cannot operate without a control signal comparable to that used by Tokuhiro.

EX2006 (Mangione-Smith Decl.), ¶¶152-155

Hiraishi-Tokuhiro Is Inoperable – No Reasonable Chance of Success

(2) Tokuhiro's variable delay circuit DR-1 cannot delay the read strobe DQS to convert the read latency to CL=6, as required by Hiraishi.



EX1005 (Hiraishi) at FIG. 17.

FIG.17

[0160] The data register buffer 300 receives the read command Read, and after a lapse of a predetermined CAS latency, outputs dummy data DQ. The dummy data DQ is not the read data read out from the memory chip 200 but data that is automatically generated by the data register control circuit 320 in the data register buffer 300. In the example shown in FIG. 17, the CAS latency is set to six clock cycles (CL=6), so that an output of the dummy data DQ begins at a time T6. The dummy data DQ is, for example, a signal in which a High level and a Low level are repeated in an alternate manner.

EX1005 (Hiraishi) at [0160].

Hiraishi-Tokuhiro Is Inoperable – No Reasonable Chance of Success

(1) “first delayed read strobe” cannot be used to clock out the data from the FIFO.

EX2006 (Mangione-Smith Decl.), ¶156

(2) Tokuhiro’s variable delay circuit DR-1 cannot delay the read strobe DQS to convert the read latency to CL=6, as required by Hiraishi.

EX2006 (Mangione-Smith Decl.), ¶157

(3) Tokuhiro’s read and write leveling are controlled, not by its memory controller or any on-module controller, but by the computer’s main CPU.

EX2006 (Mangione-Smith Decl.), ¶¶147-151

(4) Tokuhiro’s incorporated delay element DR-1 cannot operate without a control signal comparable to that used by Tokuhiro.

EX2006 (Mangione-Smith Decl.), ¶¶152-155

Hiraishi-Tokuhiro Is Inoperable – No Reasonable Chance of Success

EX2008 (Wedig Deposition) at 155:19-233.

EX2008 (Wedig Deposition) at 204:6-10.

Patent Owner Response at 69.

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

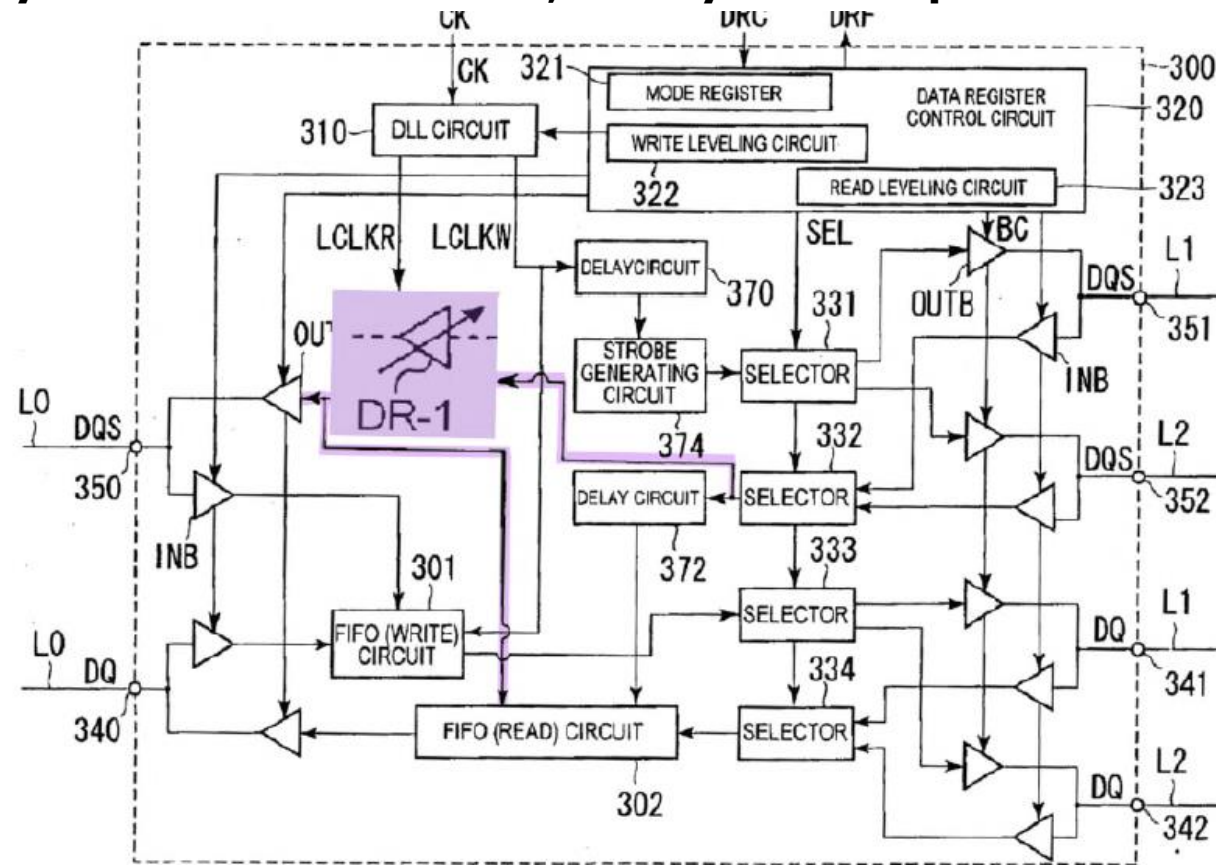
Ex. 2013, p. 94

Samsung Ex. 1086, p. 94

Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2023-00847

Hiraishi-Tokuhiro Is Inoperable – No Reasonable Chance of Success

(3) Tokuhiro's read and write leveling are controlled, not by its memory controller or any on-module controller, but by the computer's main CPU.



Petition at 109 (annotating Hiraishi's FIG. 5)

Patent Owner Response at 70.

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Ex. 2013, p. 95

Samsung Ex. 1086, p. 95

Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2023-00847

Hiraishi-Tokuhiro Is Inoperable – No Reasonable Chance of Success

(1) “first delayed read strobe” cannot be used to clock out the data from the FIFO.

EX2006 (Mangione-Smith Decl.), ¶156

(2) Tokuhiro’s variable delay circuit DR-1 cannot delay the read strobe DQS to convert the read latency to CL=6, as required by Hiraishi.

EX2006 (Mangione-Smith Decl.), ¶157

(3) Tokuhiro’s read and write leveling are controlled, not by its memory controller or any on-module controller, but by the computer’s main CPU.

EX2006 (Mangione-Smith Decl.), ¶¶147-151

(4) Tokuhiro’s incorporated delay element DR-1 cannot operate without a control signal comparable to that used by Tokuhiro.

EX2006 (Mangione-Smith Decl.), ¶¶152-155

Hiraishi-Tokuhiro Is Inoperable – No Reasonable Chance of Success

(4) Tokuhiro’s incorporated delay element DR-1 cannot operate without a control signal comparable to that used by Tokuhiro.

¶¶316-19. Furthermore, like the original *block* diagram of Hiraishi, the modified *block* diagram for the combination was not meant to show all connections, see *supra* pp.6-10, which is why it does not show *all* “inputs to the delay element DR-1,” POR 70, such as those from control circuit 320.

Petitioner’s Reply at 31.

Hiraishi-Tokuhiro Is Inoperable – No Reasonable Chance of Success

(4) Tokuhiro's incorporated delay element DR-1 cannot operate without a control signal comparable to that used by Tokuhiro.

While Hiraishi's strobe generating circuit 376 requires only a local clock signal to operate, the incorporated variable delay element (DR-1) requires a separate control signal (d2 for DR1), per Tokuhiro's express disclosure, which is unaccounted for in the proposed combination. As such, a POSA would recognize that incorporating Tokuhiro's variable delay element (DR-1) in place of Hiraishi's strobe generating circuit 376, as proposed, would render Hiraishi's data buffer incapable of performing read leveling.

EX2006 (Mangione-Smith Decl.), ¶155