

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

Case No. IPR2023-00847
Patent No. 10,268,608

PATENT OWNER'S SUR-REPLY

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<i>Wasica Fin. GmbH v. Cont'l Auto. Sys., Inc.</i> , 853 F.3d 1272 (Fed. Cir. 2017)	8

EXHIBIT LIST

Exhibit No.	Document
EX2001	Statutory Disclaimer for 15/820,076
EX2002	Power of Attorney and Filing Receipt for 15/820,076
EX2003	IPR2022-00237 IPR Petition
EX2004	U.S. Publication No. 2010/0312925 (Osanai)
EX2005	IPR2022-00711 Record of Oral Hearing
EX2006	IPR2022-00237 DECISION Denying Institution of IPR
EX2007	IPR2022-0711 IPR Petition
EX2008	U.S. Patent No. 8,713,379 (Takeman)
EX2009	IPR2022-00237 Petitioner's Request for Rehearing
EX2010	IPR2022-00237 DECISION Denying Petitioner's Request for Rehearing
EX2011	IPR2022-00237 Declaration of Donald Alpert, Ph.D.
EX2012	Deposition Transcript of Robert Wedig
EX2013	Declaration of Dr. William Mangione-Smith
EX2014	JEDEC STANDARD, DDR2 SDRAM SPECIFICATION (JESD79-2F) (November 2009)
EX2015	JEDEC STANDARD, DDR3 SDRAM Standard (JESD79-3F) (Revision of JESD79-3E, July 2010) (July 2012)
EX2016	Deposition of Robert Wedig in IPR2022-00711 (506 IPR)
EX2017	Electronics Cooling, Challenges In Thermal Management Of Memory Modules
EX2018	JEDEC STANDARD, Double Data Rate (DDR) SDRAM Specification (JES79) (June 2000)
EX2019	JEDEC STANDARD, DDR3 SDRAM Specification (JESD79-3A) (Revision of JESD79-3) (September 2007)
EX2020	Petition for Inter Partes Review of U.S. Patent No. 10,860,506 (IPR2022-00711)
EX2021	Final Written Decision (IPR2022-00711)

EX2022	DECISION Denying Patent Owner's Request on Rehearing of Final Written Decision (IPR2022-00711)
EX2023	Final Written Decision (IPR2022-00236)

I. The Claimed Data Path Does Not Include Strobe Signal Lines (Both Grounds)

The '035 patent confirms that the '608 patent's claimed "data path" excludes strobe signal lines. Claim 1 of the '035 patent recites "data paths for transmitting *respective* data and strobe signals." The term "respective" demonstrates that there can be data paths for strobe signals and *separate* data paths for data signals. EX1031, 19:35-37.¹ Claims 15-16 provide further support, reciting separate "first" and "second" "data path[s]" for strobe signals and data signals, respectively. EX1031, 20:60-21:2.

In contrast, the claims of the '608 patent recite "a data path *corresponding to each data signal line*," but not the strobe signal line, in the "respective set[s] of data/strobe signal lines." EX1001, 19:29-45; *see also id.*, Fig. 3, 4:20-32, 6:11, 6:19-20, 8:2-3, 10:31-35 (DQ0 to DQn-1 data signal lines 322 are grouped with a *single* DQS signal line 324 to form a set of "signal lines 130"):

¹ Emphasis added throughout unless otherwise indicated.

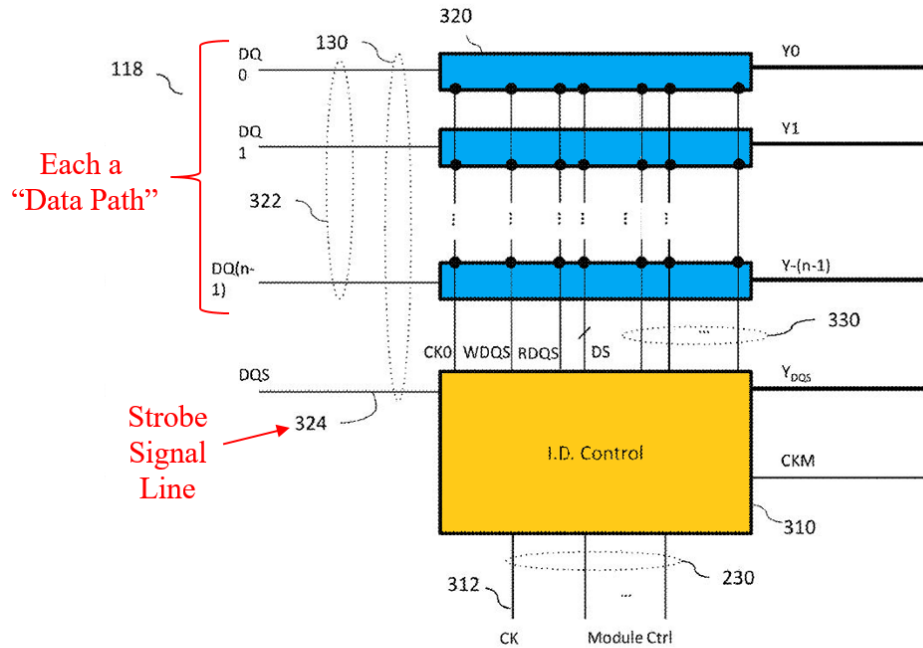


FIG. 3

The DQS line is therefore not part of a “data path” that corresponds to *each* “data signal line” because there is only a single DQS line for each n-bit group of data signal lines. EX1001, FIGs. 3, 4A-4B, 11:20-45.

Extrinsic evidence like Butt and dictionary (Reply 5, 10-12) cannot alter the plain claim language, which plainly restricted the claimed “data paths” to those corresponding to data signal lines. *E.g.*, EX1001, 19:43-45, 19:49-50. That there may be unclaimed data paths corresponding to strobe signal lines in other context are of no moment to patentability. POR, 21-23.

Petitioner also asserts that “the *entire* buffer circuit [is] in the ‘data path’.” Reply, 5-6 (original emphasis included). That is incorrect because the claims require “each respective buffer circuit *include*[s] a data path.” EX1001, 19:43-44. The

buffer circuit is thus more than the data path. EX1001, Fig. 3 (clock signals 312 and module control signals 230 are not on DQ or DQS lines, and not on any data path even under Petitioner's broad definition); EX1003, ¶142 (not all parts of the Hiraishi's buffer are on the (orange) data paths Dr. Wedig identified); EX2012, 40:11-16, 86:19-87:3; EX2013, ¶¶96-99.

Claim 10, which has been disclaimed and is deemed to not have existed, does not suggest otherwise. First, claim 10 introduces new elements—"first data path" and "second data path"—and does *not* refer back to or mention the "data path" of claim 1. Second, claim 10 is consistent with the '035 patent's claims in that there are (first) data paths for data signals and separate (second) data paths for strobe signals. But the "data path[s]" here correspond specifically to data signal lines.

Indeed, the description for Figure 16—that Petitioner argues is similar to Hiraishi—only uses the term "data path" in connection with DQ signal lines, while describing the path carrying strobe signals as a "strobe path." EX1001, 16:47-17:60; *see also* EX1001, 10:31-35. In that context, Figures 15-16 of the '608 patent are not just subparts of some broader "data path," as Petitioner argues, but rather intrinsic evidence that expressly differentiates between "data path" and "strobe path" and between "data signal lines" and "strobe signal lines." *Contra* Reply, 8-9; *see also* POR, 21-23; EX2013, ¶¶70-78. Petitioner's construction is contrary to Figures 15-16 which distinguish "data paths" from "strobe paths."

Petitioner nevertheless argues that because the claims do not recite that a “data path” *is* a “data signal line,” the recited “data path” can also correspond to strobe signal lines. Reply, 5, 8-9. Were that the case, the inventors could have just recited “a data path corresponding to *each* data/strobe signal line.”

Petitioner suggests that, because DQ and DQS signals need to be aligned, they are both transmitted on the data path. Reply, 9-10. Alignment ensures reliable sampling, but does not suggest, let alone require, the two signals be both transmitted on “data path.” POR, 6-7. Indeed, before DDR, data signals were aligned with clock signals, (EX2012, 55:2-16), but not even Petitioner suggests clock signals are on a data path. POR, 5-6.

Dr. Mangione-Smith’s testimony on the ’506 patent is no help to Petitioner since the claims of the ’506 patent do not even recite a “data path” and the patentability didn’t turn on the meaning of “data path.” *Contra* Reply 6.

Finally, Netlist consistently interpreted the term “data path” in this proceeding and the parallel district court; and Petitioner does not contend otherwise.

II. No Collateral Estoppel Applies (Grounds 1 & 2)

Even though IPR2022-00236 and this proceeding involve different issues of patentability which were not essential to the IPR2022-00236 FWD, (*see Google LLC v. Hammond Development International, Inc.*, 54 F.4th 1377, 1381 (Fed. Cir. 2022)), Petitioner repeatedly argues for preclusion. That is incorrect.

First, as explained in Section I, the '608 patent and the IPR2022-00236's '035 patent recite different "data paths."

Second, as Dr. Mangione-Smith testified without rebuttal, there are other "important differences in the claims" of the '608 patent and the '035 patent at issue in IPR2022-00236. EX2013, ¶197. For example, "[t]he '035 patent uses the [recited] 'timing information' to 'control timing of respective data and strobe signals,' while the '608 patent delays a signal through a data path corresponding to a data signal line with a delay circuit that is included in the data path." *Id.* And unlike the '035 patent, the '608 patent recites both a tristate buffer and delay circuit in the data path. *See id.*

Third, the '608 patent requires the "delay circuit [on the data path] [be] configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals," with the "module control signals" being "in response to [] system command signals" received from the control/address signal lines in the memory bus. EX1001, 19:52-55, 19:21-26, 19:15-18. The recited "system command signals" also result in "module command signals" used by memory devices for performing memory operations. *Id.*, 19:24-26, 19:29-32. The '035 patent does not have comparable language. This difference is significant because, with these requirements, not all signals sent by Hiraishi's command/address/control register buffer 400 (alleged

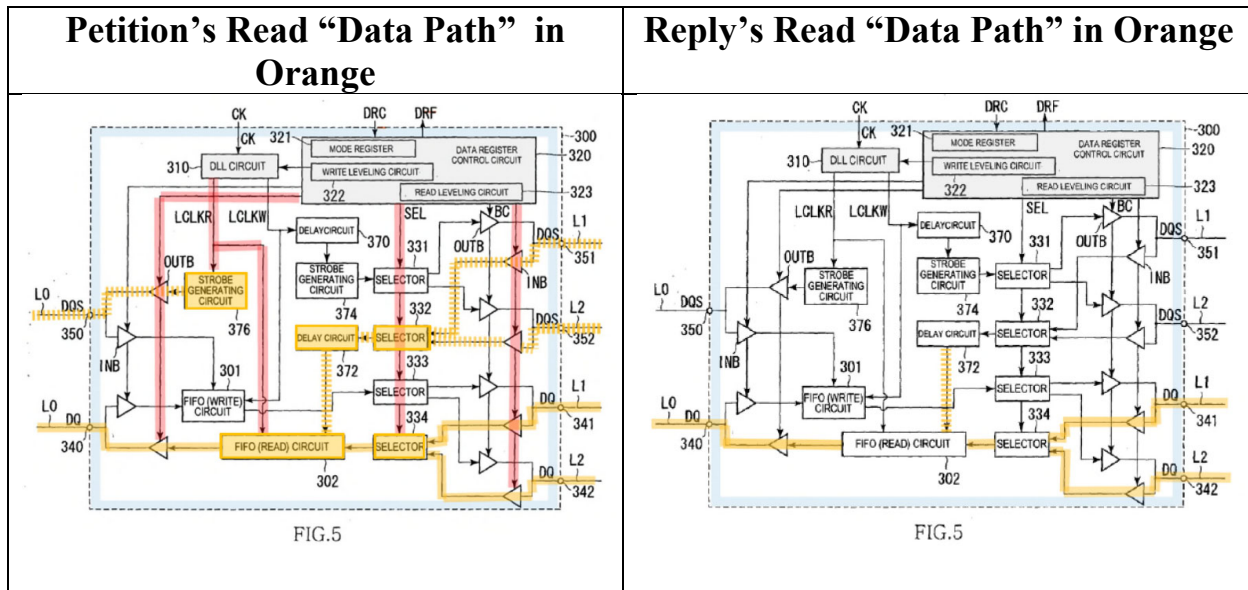
“module control device”) to the data register buffer 300 (alleged “buffer circuits”) qualifies as a claimed “module control signal.” Specifically, Hiraishi’s S4 does not involve a memory controller and therefore has no module control signal that is outputted by the command/address/control register buffer 400 “in response to [] system command signals” received “via the set of control/address signal lines” of the memory bus, per the claims. EX1001, 19:21-26, 19:15-18. Instead, in S4, “the command/address/control register buffer 400 ... issues the active command ACT and the read command Read” on its own. EX1005, [0147]-[0148]; *compare* EX1005, Fig. 15 (no signals received at module edge connectors for leveling operation) *with* Figs. 11-12 (system control information at connectors for read/write).

The two proceedings also involve different unpatentability theories. EX2013, ¶198. For example, IPR2022-00236 did not involve moving Tokuhiko’s delay element out of the memory controller and into the data buffer, while this is a necessary part of Ground 2 here. Pet., 87-91; EX2013, ¶199. Also, in IPR2022-00236 the Board relied on Hiraishi’s input (“INB”) buffers to find that there was sufficient teaching for “controlling the timing of the data and strobe signals on the data paths on which those signals travel.” EX2023, 36; EX2013, ¶199. Here, Dr. Wedig testified under oath that INB is not part of the “delay circuit.” EX2012, 31:23-25.

III. Ground 1 Does Not Render Challenged Claims Unpatentable

A. The Reply Substantially Revised Petitioner's Unpatentability Theory

As the Board recognized, Petitioner maps the “data path” to both the data lines and the strobe lines. Pet., 34; Paper 13, 30-31. The Reply, however, relies for the first time on a mapping that identifies only Hiraishi's FIFOs as the “delay circuit.” See comparison below.



Pet., 34; Reply, 14.

This is a stark departure from the Petition and Dr. Wedig's declaration, which did not argue that Hiraishi's FIFO alone was the “delay circuit.” Pet. 39, 47, 51; EX1003, ¶¶152, 166. In fact, Dr. Wedig testified unequivocally that his opinions are based on Hiraishi disclosing the claimed “delay circuit” as a *combination* of components identified in paragraphs 152 and 166 of his declaration because “they

all work together to implement the delay circuit.” EX2012, 16:21-20:16; EX1003, ¶¶152, 166; POR, 28-29; *see also* EX2012, 137:13-22, 140:13-16. The Reply also argues for the first time that Butt’s FIFOs 112 are a “delay circuit.” Reply, 16. This is patently improper, particularly when the Board here found at institution that Petitioner only cited Butt for the alleged understanding of “data path.” Paper 13, 11-12; *Henny Penny Corp. v. Frymaster LLC*, 938 F.3d 1324, 1329–31 (Fed. Cir. 2019); *Wasica Fin. GmbH v. Cont’l Auto. Sys., Inc.*, 853 F.3d 1272, 1286 (Fed. Cir. 2017).

Petitioner and Dr. Wedig unambiguously and repeatedly relied on the **combination** of Hiraishi’s DLL 310, FIFOs 301/302, delay circuits 370/372, and strobe generating circuits 374/376 to satisfy the “delay circuit” and its functionality, and it cannot switch to a different set of components mid-trial.²

The new theory also fails as a matter of law because there is no record evidence supporting the attorney argument that Hiraishi’s FIFOs **alone** satisfy the claimed “delay circuit” and its functionality, including for reasons discussed in Sections B-C below. There is also no evidence that Butt discloses the claimed

² Petitioner also argues that “the term ‘data path’ is broad enough to include the ‘delay circuit’ ***no matter where it is physically located within the buffer circuit.***” Reply, 16. The argument is incorrect for the same reason why the entire buffer circuit of the ’608 is not on the data path. *See supra*, 2-3.

“delay circuit.”

B. Petitioner Has Not Established That Hiraishi’s FIFOs Delay A Signal on the Data Path “In Response To” Module Control Signals

Petitioner argues alleged generic similarities between Hiraishi’s Figure 5 and the ‘608 patent’s Figure 16 suggests obviousness. Reply 13-15. But there are significant differences, including that the ‘608 patent’s buffer circuit includes a DQ routing circuit 320 per data signal line, each of which includes a delay circuit 1660 that receives a “delay signal DS,” which has no corollary in Hiraishi. EX1001, 10:31-35, 17:48-56, FIG. 3. Moreover, the ‘608 patent’s buffer circuit includes a circuit 1670 that samples the delayed read signal. *Id.*, 17:56-60. This directly contrasts with *Hiraishi* which *uses a delayed strobe signal* from delay circuit 372 to sample *non-delayed data in FIFO 302*. EX1005, FIG. 5, [0084], [0092].

The alleged superficial similarities of a subset of buffer components also do not suggest similarity in functionality, and Petitioner ignores the fact that Hiraishi has no delay circuit delaying a data signal “in response to at least one of the module control signals,” per Element 1[f]. EX1001, 10:61-11:2, 12:30-37, 16:10-24, 17:48-60.

Contrary to Petitioner’s insinuation (Reply 12-13), the Board never found that Osanai discloses this limitation, concluding only that Osanai’s data register control circuit 320 selects certain paths using SEL, INB, and OUTB signals, which are sent to selectors 331–334 and INB/OUTB buffers. EX1066, 19, 24, 26. Here, Petitioner

relies on INB/OUTB buffers and the signals sent thereto to satisfy a different limitation (“tristate buffer”) (Pet., 39), and it does not argue that selectors 331–334 or INB/OUTB delay a signal at all. Thus, if anything, IPR2022-00236 supports Netlist’s position that Hiraishi’s DRC signals are used for purposes other than for its FIFOs to delay a signal through a data path.

Netlist never argued that “in response to” means “directly in response to,” but Dr. Wedig did *not* opine that Hiraishi’s FIFOs operate directly or indirectly in response to any module control signal to delay a signal in the data path corresponding to a data signal line. Instead, he opined only that Hiraishi’s FIFOs operate in response to the “module *clock* signal,” a separate claim element. *Id.* (citing Hiraishi, [0087]); *see also id.*, ¶161 (Hiraishi’s retiming also allegedly involved the FIFOs responding to CK in the form of LCLKW/LCLKR); EX1001, 19:24-28. This is a clear failure of proof.

Petitioner’s re-written theory fails for two additional reasons. **First**, Hiraishi does not perform S4 in response to any signal that is based on a “system command signal” received by the memory module, as required by the claimed “module control signal.” EX1001, 19:21-26, 19:15-18; *Contra* Reply, 18. As noted above, Hiraishi performs S4 without participation by the memory controller. As shown below, Figure 15 for S4 read leveling shows no command input via “CONNECTOR” to the memory module, in contrast to FIG. 11 for a read operation which shows CMD(IN)

to the memory module via “CONNECTOR.” That is, any “module control signal” generated in S4 is not “in response to [] system command signals” and not a claimed module control signal. EX1005, [0148], Fig. 15; *see also* [0142]-[0146], Figs. 14A-14B (compare Fig. 12) (S4 write-leveling also does not involve “system command signals”). Hence, Hiraishi’s S4 operations do not determine a delay “in response to” a claimed module control signal; and as explained below, their output—when applied to LCLKR/LCLKW—does not result in a delay “in response to” a claimed module control signal.

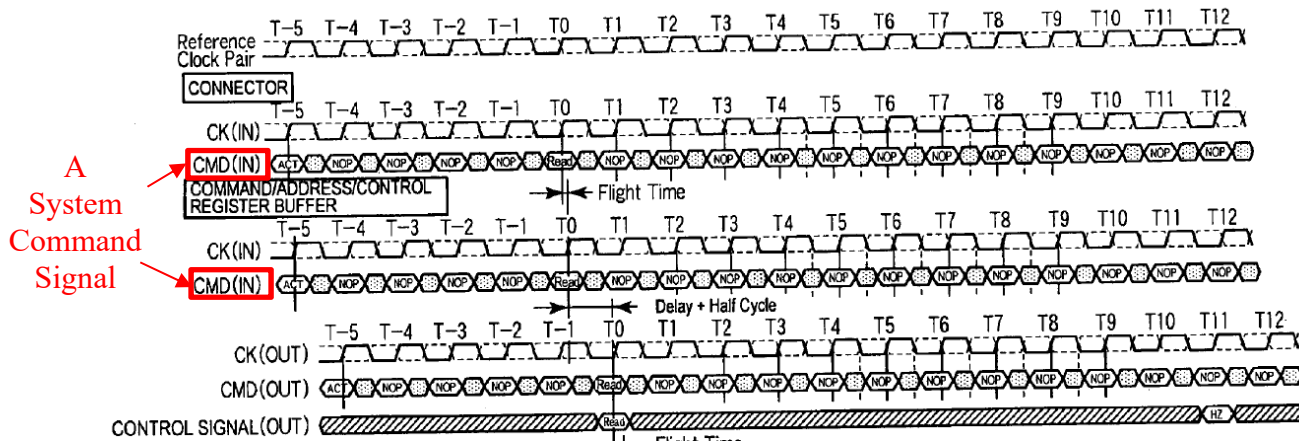


FIG. 11 (Partial) – Read Operation

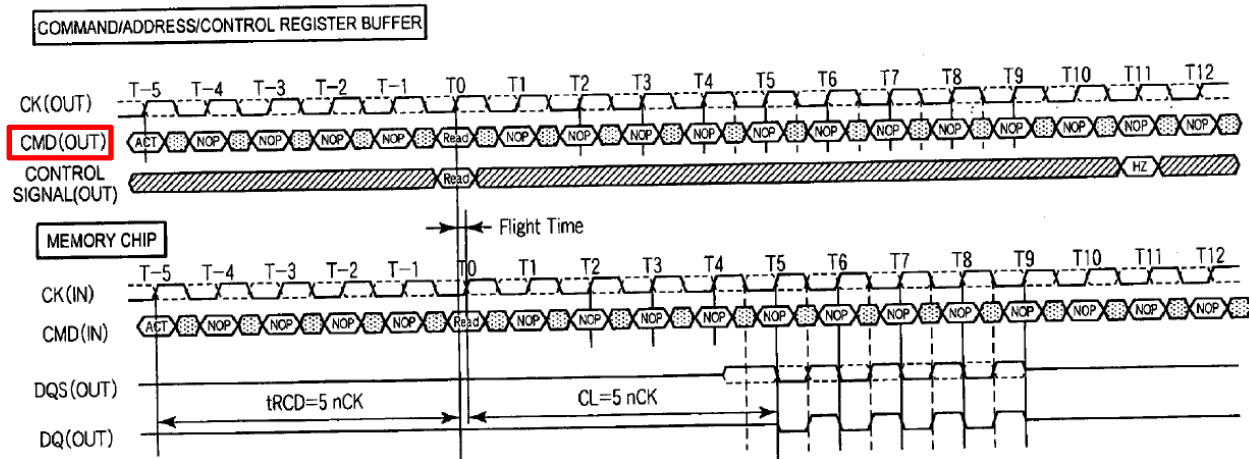


FIG. 15 (Partial) – Read Leveling

Second, even if the Board allows Petitioner to now characterize Hiraishi's LCLKR/LCLKW as module control signals, these are free running *clock* signals under Petitioner's theory. Specifically, Petitioner argues that Butt explains how Hiraishi operates (Pet. 36) and Dr. Wedig testified that Butt's master delay circuit 116 provides a free running clock even though it applies a delay. EX2016, 123:14-18, 124:6-13; EX1029, FIG. 2, [0021]. Like Hiraishi's DLL 310, Butt's circuit 116 is a DLL that provides a shifted clock signal based on a reference CLK. EX1029, [0021]. Thus, under Petitioner's own theory, Hiraishi's LCLKR/LCLKW signals are also free running, continuous clocks that include the adjustment even when there is no DRC in response to system command signals for memory operations involving a memory device. EX1001, 19:21-32. As such, they are *not* "in response to" any claimed module control signal.

C. Hiraishi Does Not Determine an Amount Of Delay To Apply To A Signal On The Data Path

The combination fails to teach a delay “amount determined by the command processing circuit ...,” not because Hiraishi adds a fixed amount of delay, but because “[b]y resetting internal latency to the next clock cycle, Hiraishi’s buffer circuit need not compute individual delays” POR, 48-49; 49 (“... Hiraishi can account for all delays by simply resetting latency to the next clock cycle for all buffer circuits.”); 55 (“Hiraishi has a simple solution ...—setting buffer latency to the next clock cycle, for all memory devices, which effectively eliminates the need to determine any individual delay amounts.”).

As Dr. Wedig testified, Hiraishi’s re-timing relies on Hiraishi’s FIFOs operating in response to module *clock* signals (CK) regenerated as LCLKW/LCLKR.³ EX1003, ¶161. Hiraishi thus has no need to determine an amount of delay to apply. This is possible because, as Dr. Wedig confirmed, the memory chips, the data buffer and the data register buffer all receive the same “system-level CLK” and have a common understanding of timing. EX2012, 74:9-24; EX2013, ¶126. As an analogy, if a committee were to announce at 5 pm the

³ As explained, any alleged delay embodied by LCLKW/LCLKR is not “in response to” a claimed “module control signal,” whether “in response to” modifies “determine” or “delay.”

results of several awards given out during the day, the committee simply makes the announcement at 5 pm without determining how long it has to wait after each award. Dr. Wedig confirmed this is how Hiraishi times the output of data at time T6. EX2012, 76:13-77:7, 78:10-79:8 (“[T]he DLL circuit gives you the timing for the chip. So yeah, so it’s going to generate the CLK.... [I]t will CLK it out at T6. And yeah, the DLL circuit is in charge of making that CLK.”); POR, 50. Thus, the issue is not whether the DQ/DQS is delayed during Hiraishi’s re-timing process, but whether Hiraishi *determines the amount of the delay*, per Element 1[i]. On that issue, Hiraishi only discloses re-timing latency parameter (CL/WL) to the next higher clock cycle, as Hiraishi shows in FIGs. 11-12 for example, thereby avoiding determining individual delays. POR, 46-52, 55-57.

Petitioner continues to conflate Hiraishi’s re-timing and leveling operations, but fails to identify any disclosure in Hiraishi that supports its argument that Hiraishi uses the previously-stored leveling values to re-time DQ/DQS signals. Reply, 23. Instead, FIGs. 11-12 show that CL and WL are each increased by one, with no reference to using leveling results:

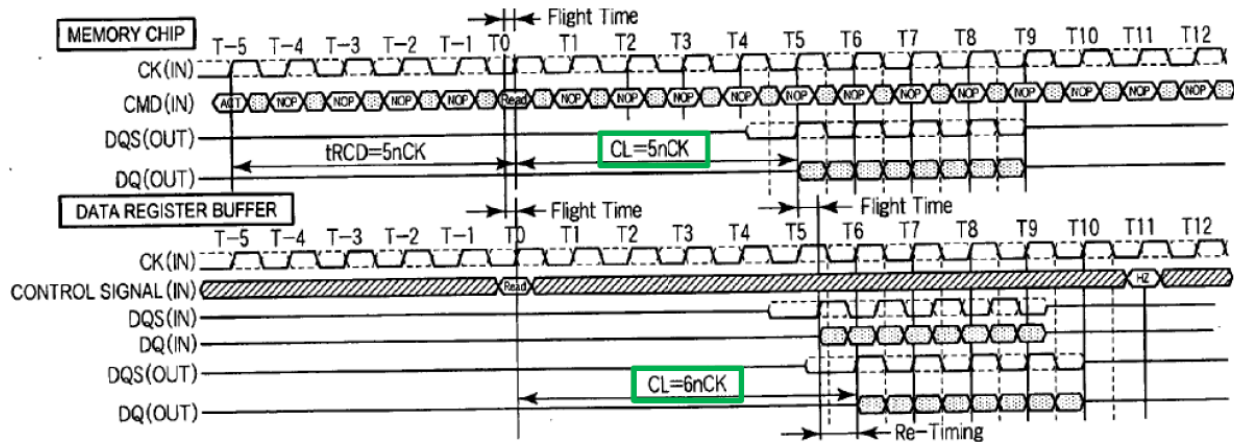


FIG.11

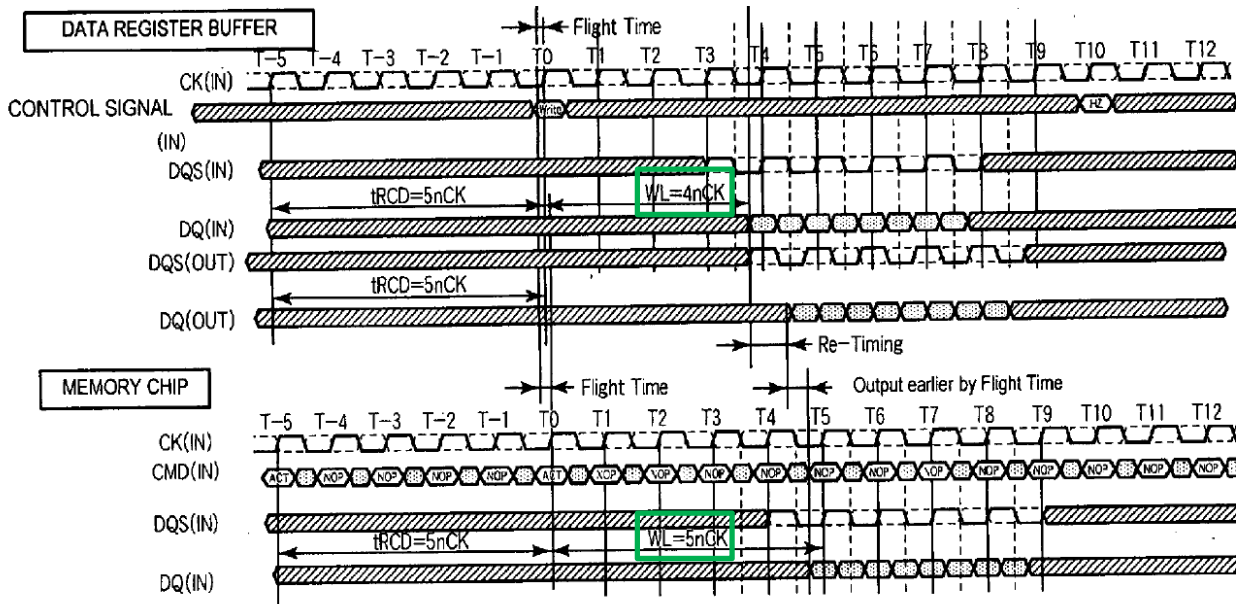


FIG.12

EX1005, FIGs. 11-12.

Petitioner makes a strawman argument that there are different flight times between the data buffers and memory chips in Hiraishi. Reply, 20-21. But the salient question is *how* Hiraishi accounts for those differences. Petitioner argues that Hiraishi determines an amount of delay based on whether data is being sent/received on the longer data line L1 or the shorter data line L2. Reply, 20-30.

Petitioner acknowledges that this requires measuring the amount of flight time delay for each memory chip. Reply, 21-25 (repeatedly referring to measuring flight time delays). But in the only two instances where Hiraishi actually mentions measuring flight times, the measured time is “used in an adjustment of an activation timing of the input buffer circuit INB and the like.” EX1005, [0151], [0161] (Hiraishi’s INB’s are relied on to satisfy the separately-recited “tristate buffer”).

Significantly, Hiraishi measures flight time delays to control the activation of INB buffers, but never mentions using that measurement for its re-timing operations. Other parts of Hiraishi’s disclosure further confirm that Hiraishi does not determine individual delays for L1 versus L2 for re-timing. EX1005, [0024]-[0025]; EX1003, ¶129. For instance, the timing diagrams for read and write operations illustrated in Figures 11-12 and their respective textual descriptions do *not* describe separate re-timing procedures for L1 versus L2 or suggest that the depicted conversion of CL/WL to the next higher clock cycle applies to only L1 (or L2). *Id.* If Hiraishi was in fact determining different amounts of delay for L1 and L2, the timing diagrams for the two would necessarily look different under Petitioner’s theory. But they do not. *Id.*

That the JEDEC standard requires *integer* latency values further support Netlist’s argument. Reply, 24-25, fn. 7-8. This is because Hiraishi discloses that all flight time delays are less than one clock cycle, as both experts testified. EX2012

(Wedig), 70:23-71:7; 79:15-80:16; EX2013, ¶256, ¶120. Thus, with data exchanged with integer latency values, Hiraishi's solution is to simply increase read/write latency to the next clock cycle to account for the differences in flight time.

Concerning the argument that clock speeds were getting to the point where two signals could be on the same line at the same time (aka "wire pipelining"), Dr. Mangione-Smith disputed that this was an anticipated problem before the priority date. EX1074, 246:2-247:5, 232:19-22. As for Petitioner's reply examples on pages 25-30, at best they show that it is possible to **back out** an amount of delay as the difference between the total latency increase (one clock cycle) and the individual flight time delays (allegedly 0.3 or 0.7 clock cycle). But being able to reverse engineer a value does not mean that the alleged "command processing circuit" of Hiraishi ever determines that value, as required by the claims.⁴ Hiraishi doesn't because it doesn't need to.

Finally, the Board's denial of institution in IPR2017-00730 confirms Netlist's points. First, Petitioner acknowledges that "the Board concluded that read data was output at a given time (e.g., T6 corresponding to 're-timing to CL=6') **which does**

⁴ Even if leveling result is used to alter LCLKR/LCLKW, those are free running clocks neither determined in response to nor delaying a data signal "in response to" a claimed module control signal. See *supra* 12.

not change as a result of read or write leveling.” Reply, 31. That is, the Board concluded that read/write leveling does not change Hiraishi’s re-timing operation.

Second, the chop-quoted conclusion by the Board (Reply, 31) concerns DQS, not DQ: Hiraishi’s write leveling “determines an amount of time by which to shift the output **of DQS** from data register buffer 300 so that it arrives at memory chip 200 **substantially matched with clock signal CK.**” EX1014, 10. This is wholly consistent with Netlist’s description of Hiraishi’s write leveling (POR, 41-46), which has nothing to do with delaying DQ data, as required by the ’608 patent.

IV. Ground 2 Does Not Render Challenged Claims Unpatentable

A. Ground 2 Also Fails All- Elements Rule

For the same reasons as stated for Ground 1, Petitioner has not shown that the “data path” limitation and “delay circuit” limitation can be met by DQS and FIFOs only respectively.

Petitioner’s citation to the alleged alternative combination for Ground 2 changes nothing. First, with respect to using Tokuhiro’s leveling operation in Hiraishi, neither option would meet elements 1[c] and 1[f] simultaneously. As a preliminary matter, the DRC signals in S5 training would not qualify as the claimed “module control signals” because although they may be in response to system command signal(s), those system command signals do not also result in “module command signal(s)” that memory devices use to “perform the memory operations,”

as required by the claims. *See* EX1001, 19:21-26, 19:29-32; EX1005, [0152]-[0161], Figs. 16A, 16B, 17 (no memory device participation in S5 write or read leveling). Adding Tokuhiko does not change that. In Tokuhiko, the memory controller sends only clock and DQS signal to the memory module to perform write leveling (from which read timing is adjusted also). When combined with Hiraishi, instead of the memory device, it would be Hiraishi's data buffer that returns a value via the DQ line in response to the memory controller's leveling request because the memory controller has no knowledge of the memory devices on the other side of the data buffer. Hence, there are still not any system command signals from which a claimed module control signal can be generated. Using module controller to compute the delay would also not cure the deficiency because in that case, the read/write commands are provided by the on-module register buffer 400 9 (as in S4), not by the memory controller. EX1005, FIG. 15, [0147]-[0151]. Thus, Ground 2 does not disclose any delay or determination of delay in response to a "module control signal" that is in turn "in response to [] system command signals," per claim 1 and as in Ground 1.

Second, Dr. Wedig testified that "Hiraishi's existing read FIFO circuit is adapted to delay the read data," but that "in alternative implementations, delay elements similar to Tokuhiko's DR elements can be used *instead of or in addition to Hiraishi's FIFO circuit* for delaying the read data." EX1003, ¶262. But, even in the

alternative implementation, Tokuhiro's "read delay circuit DR-1 (purple) is added to the Strobe Generating Circuit 376 to *delay* both *the strobe signal DQS* 350 and *the signal clocking out* data," except that the components from which data is being clocked out are DR elements instead of FIFO circuits. Pet., 89. But neither DQS nor the signal clocking out data are "a signal through [a] data path," per the claims. POR, 59-60; EX1001, 19:49-55. The signal clocking out data is a free running one that does not respond to a module control signal as explained in Ground 1. Furthermore, delaying DQS to have it aligned with read data from FIFO does not delay the read data itself (*e.g.*, EX2012, 84:13-85:10, EX2029, [0020]); and a DQS signal cannot clock out data from FIFO as explained below. Moreover, Petitioner does not explain how the delay caused by the FIFO as a result of serially receiving the alleged DQS can be accounted for.

B. Petitioner Has Failed To Establish That The Proposed Hiraishi-Tokuhiro Combination Is Operable

The Board has not previously considered the Hiraishi-Tokuhiro Combination presented here which adds one of Tokuhiro's delay DR-1 elements to Hiraishi's Strobe Generating Circuit 376. *Supra*, Section II.

First, the Reply's citation to Hiraishi's S4 read/write leveling (Reply, 33) is irrelevant because Ground 2 is not based on S4 leveling between the memory chip and the data buffer. Instead, Ground 2 is based on adjusting for fly-by delays as seen by the memory controller, which is ubiquitously addressed by the memory controller

in Hiraishi, Tokuhito, and every memory system seen by either expert. EX2013, ¶¶58, 64-65, 147, 180, 186; EX2016, 171:15-21, 177:14-19. Moreover, the issue is not whether Hiraishi's Figure 5 shows all signals, but whether DR1 from Tokuhito's memory controller can be operable in the very different environment of Hiraishi's buffer circuit when Hiraishi clearly does not have control signal lines or communication with a CPU. This is a failure of proof because Petitioner has not provided a reasoned explanation as to how the combination, as *Petitioner* proposed it, can be made operable. Finally, Netlist's figures are not missing similar signals. EX1001, FIGs. 15-16 (showing delay signal DS), 11:8-12, 17:15-18, 17:54-56.

Second, the combination is also inoperable because Petitioner has not established that a DQS signal can be used to *clock out* data. Petitioner misleadingly conflates the use of DQS and clock signals for purposes of *sampling* data, as disclosed by the '608 patent, with the distinct operation of *clocking out* data. Dr. Mangione-Smith testified that either type of signal can be used to *sample* data, but was unequivocal that DQS signals cannot be used to reliably clock out data. EX2013, ¶165. Sampling and clocking out data are two different operations, as Hiraishi expressly discloses (EX1005, [0087], [0091]) and as Dr. Wedig confirmed. EX2016, 104:24-106:4.

The Butt reference is no different. As Dr. Mangione-Smith explained, Butt *samples* a group of read data signals in the FIFO using a delayed DQS signal and

clocks out data from the FIFO “in response to clock signal CLK_1X.” EX1074, 240:14-242:3; EX1029, [0019]-[0020] (“to sampling the read data with the read data strobe signal DQS”). Dr. Wedig also confirmed that Butt is not delaying data at all (EX2012, 84:13-85:10), while the claims require “delay[ing] a signal through the data path” corresponding to a data signal line, *i.e.*, a delay of a data signal.

The new and improper ***attorney argument*** that Butt uses a GATEON signal to “gate” or “block” the DQS preamble/postamble does not change the fact that Butt does not delay DQ, only DQS. E.g., EX1029, FIG. 4, [0005]. Nonetheless, Butt says nothing about gating/blocking DQS preamble/postamble and Dr. Mangione-Smith disputed the characterization during a lengthy deposition exchange. EX1074, 189:19-202:20; *Elbit Systems of Am., LLC v. Thales Visionix, Inc.*, 881 F.3d 1354, 1359 (Fed. Cir. 2018) (“‘attorney argument is not evidence’ and cannot rebut other admitted evidence”). GATEON cannot have the purported function because it is used to gate read DQS when DQS is in “**OFF**” mode. EX1029, [0023]-[0024]. But attorney argument does not explain how GATEON can be used (1) to block only a portion of a signal (*i.e.*, preamble/postamble), or (2) in read mode (per the combination) where the DQS signal CANNOT be in an OFF mode.⁵

⁵ A preamble/postamble-less DQS would still not be in the data path. *Supra*, Section I.

Thus, Petitioner has failed to present any evidence that describes or suggests anything other than a clock signal being used to *clock out* data, as the name implies.

Finally, Netlist is not distinguishing the prior art based on unclaimed technical details. Reply, 36. But it is holding Petitioner to the required explanation of specific evidence that supports its arguments, which it has failed to do so. *See In re Vaidyanathan*, 381 F. App'x 985, 993 (Fed. Cir. 2010) (holding that a Petitioner must identify ‘how’ particular references would be combined to invalidate the patented invention.”); *Trivascular, Inc. v. Samuels*, 812 F.3d 1056, 1066 (Fed. Cir. 2016); *Samsung Elecs. Co. v. Elm 3DS Innovations, LLC*, 925 F.3d 1373, 1381-82 (Fed. Cir. 2019); *ActiveVideo Networks, Inc. v. Verizon Commc'ns, Inc.*, 694 F.3d 1312, 1327 (Fed. Cir. 2012) (“The expert failed to explain how specific references could be combined, which combination(s) of elements in specific references would yield a predictable result, or how any specific combination would operate or read on the asserted claims.”).

C. Petitioner Has Failed To Establish a Motivation To Combine

As noted above, the Board has not considered the Hiraishi-Tokuhiro Combination as presented here. *Supra*, Sections II, IV.B.

1. Petitioner’s Fly-By Delay Arguments

Petitioner’s discussion of fly-by delays in the Reply is not grounded in evidence. The discussion does not cite even once to Dr. Wedig’s declaration, and

instead relies on mischaracterizations of Dr. Mangione-Smith's deposition testimony about attorney-created figures which he saw for the first time during his deposition. Dr. Mangione-Smith testified, with respect to the attorney-created EX1079, that he "didn't find flight time delays greater than one clock cycle considered in Hiraishi *at all*." EX1074, 231:21-232:4. Dr. Mangione-Smith further confirmed there is no disclosure in Hiraishi which "would suggest he envisioned the possibility of there being two commands on a line at the same time" and that "engineers try to avoid it as much as possible." EX1074, 232:19-233:11; 246:2-247:12. As for whether horizontal delays greater than one clock cycle would also be a problem for Hiraishi, Dr. Mangione-Smith testified that Hiraishi does not "talk[] about operating at high enough speeds where wire pipelining would occur on the fly-by lines," and that "they were focused on DDR3 where a lot of these issues were not fundamentally present as a problem" EX1074, 69:17-70:14.⁶ Hiraishi's disclosures corroborate Dr. Mangione-Smith's testimony: Hiraishi contains a dozen signal timing diagrams, and not a single one shows delays greater than one clock cycle such that there would be more than one signal on a line at a time. Dr.

⁶ Wire pipelining means two commands on a line at the same time, which can occur when horizontal delays are greater than 1 CK. EX1074, 69:17-70:6, 232:19-22.

Mangione-Smith also testified that he did not believe wire pipelining was a known problem at the time of the invention. EX1074, 246:2-247:5. Moreover, even at DDR3's maximum operating frequency of 1066MHz (EX2015, Table 67), at the assumed 70 ps/cm rate (EX1001, 9:52-10:6), a signal would have to travel further ($1/(1066\text{MHz} \times 70\text{ps/cm})$) than the 13.3-cm maximum width of the module to encounter wire-pipelining. EX1018, p. 4.20.4-29. Thus, there is no reason to believe Hiraishi (i) would need to account for delays greater than 1 CK, or (ii) could accommodate wire pipelining without substantial additional modification given the undisputed record evidence that "[i]t's difficult to get working right. It takes very good engineers." EX1074, 247:6-12.

2. Petitioner Has Failed To Rebut Netlist's Arguments on Motivation to Combine (Reply, 43-46)

First, Tokuhiko does not address delays greater than one clock cycle. POR, 73-74, 82-83. Petitioner has no answer for Dr. Mangione-Smith's analysis of Tokuhiko that its "process can only *align the DQS* with the next up or down clock edge, which would necessarily occur in less than one clock cycle." EX2013, ¶175.⁷

⁷ Butt, Hiraishi and Tokuhiko all disclose delaying DQS by moving DQS to align it with the set of data signals as a group. EX1005, [0053], [0085], [0128]; EX1029, FIG. 3A-3B, [0025]-[0032], EX1006, Fig. 4. Because the '608 patent recites "a data

Dr. Wedig is silent on the issue.

Second, Netlist's argument that a data buffer is "space-constrained" is based on *Petitioner's own proposal* to add delay elements to each of Hiraishi's nine data buffers (and presumably the required control circuitry (e.g., CPU 13)), which Petitioner has not addressed. POR, 76-78, Reply 45.

Third, Hiraishi's alleged control lines DRC/DRF are *to* the module, not *on* the module, and in any event terminate at the control circuit 320.⁸

Moreover, as noted above, Hiraishi does not have all the circuitry and control signals it needs because it doesn't have delay elements in its strobe generating circuit 376 to begin with, and instead provides only a clock signal thereto.

Netlist never argued that "Hiraishi does not need read leveling" Reply, 46. Instead, as Dr. Wedig confirmed, Hiraishi already discloses S5 leveling performed by the memory controller; and therefore doesn't need a new circuit to perform the redundant function. POR, 14-16; EX2012, 57:15-17, 58:6-59:18 ("... it's the memory controller that needs to do that delay.").

path corresponding to the *each* data signal line," it requires the capability of adjusting DQ lines individually, which DQS adjustment alone cannot accomplish.

⁸ Petitioner's "fourth" point on page 46 is addressed below in Section IV.C.3.

3. Petitioner Has Not Addressed the Motivations for the Specific Modifications to Hiraishi

First, the Reply fails to address *why* a POSA would have undertaken the specific modifications of replacing Hiraishi's local clock LCLKR signal with a DQS signal that cannot clock out FIFO data. POR, 65-70; *supra*, §IV.B; POR, Section VII.B.2; EX2013, ¶166. An explanation is particularly needed here because none of the cited prior art or background references use DQS to clock out data. The bare assertion is clear hindsight.

Second, the Reply fails to address *why* a POSA would have moved Tokuhiko's delay elements out of the memory controller and into Hiraishi's data buffer, instead of implementing them as Tokuhiko does, *i.e.*, in the memory controller. POR, 78-80. Petitioner's arguments about the benefits of the combination are unavailing since those benefits are untethered to the proposed modification. While Petitioner argues that using Hiraishi's data buffer instead of the memory controller to adjust for delays into the memory controller is a "suitable option," the state of the art indicates the opposite: none of the cited prior art (Hiraishi, Tokuhiko, and Giovannini) does it, and Dr. Wedig has never seen it done. POR, 78-80. This too is clear hindsight.

Dated: July 26, 2024

Respectfully submitted,

By: /Jonathan Lindsay/

Case No. IPR2023-00847

Patent No. 10,268,608

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CERTIFICATE OF WORD COUNT

I hereby certify, pursuant to 37 C.F.R. section 42.24, that the foregoing Patent Owner Sur-Reply contains 5,595 words, excluding the words in the table of contents, table of authorities, exhibit list, this certificate of word count, and certificate of service. The word count is based on the word count of the Microsoft Word program used to prepare the Patent Owner Sur-Reply.

/s/Jonathan M. Lindsay
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CERTIFICATE OF SERVICE

I hereby certify, pursuant to 37 C.F.R. sections 42.6, that on July 26, 2024, a complete copy of **PATENT OWNER'S SUR-REPLY** was served upon the following, by ELECTRONIC MAIL:

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