

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,

Petitioner,

v.

NETLIST, INC.,

Patent Owner

IPR2023-00847

Patent 10,268,608 B2

**PETITIONER'S OPPOSITION TO NETLIST'S MOTION TO SUBMIT
LATE SUPPLEMENTAL INFORMATION UNDER 37 C.F.R. § 42.123(b)**

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I. INTRODUCTION

The Board has repeatedly rejected similar motions by Netlist under 37 C.F.R. § 42.123(b) and should do so again here.

II. ARGUMENT

A. Netlist failed to show that McAlexander’s testimony “reasonably could not have been obtained earlier”

Netlist received McAlexander’s expert report in November 2023 and then turned down *six* opportunities to depose McAlexander — on February 26, March 8, March 14, April 3, April 9, and July 10, 2024, *see* Tishman Decl. ¶¶ 4–13 & Exs. C–I — including *three* opportunities *before* Netlist’s Patent Owner Response was due here on March 29, *see* Paper 20, so Netlist cannot possibly show that McAlexander’s testimony on July 19, 2024 “reasonably could not have been obtained earlier,” 37 C.F.R. § 42.123(b). The legal test is *not* whether Netlist “could have known [before the deposition on July 19, 2024] that Mr. McAlexander would give [allegedly] inconsistent testimony,” Mot. 5, but rather whether Netlist reasonably could have *obtained* the testimony earlier, as the Board has repeatedly held when rejecting similar motions (including by Netlist). *See, e.g., Samsung Elecs. Co. v. Netlist, Inc.*, IPR2022-00996, Paper 48, at 4 (PTAB Dec. 6, 2023) (“[Netlist] does not satisfactorily explain why it did not seek to depose Mr. Holbrook in this proceeding or why it did not depose Mr. Holbrook earlier.”); *ExtractionTek Sales LLC v. Gene Pool Techs., Inc.*, IPR2022-00625, Paper 33, at

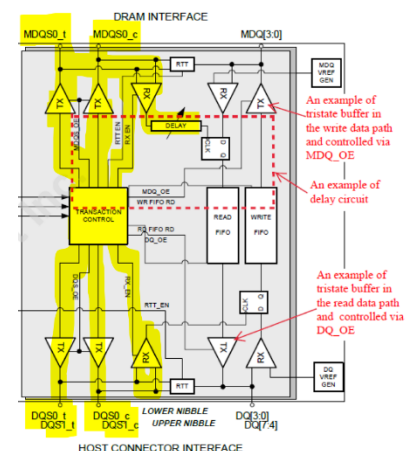
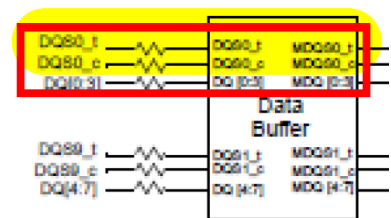
2–5 (PTAB Mar. 30, 2023) (denying motion where movant “cancelled [the] scheduled deposition in this case” causing the delay); *PEAG LLC v. VARTA Microbattery GmbH*, IPR2020-01212, Paper 46, at 4 (PTAB Dec. 30, 2021) (denying motion where movant “had not requested additional discovery on these issues earlier during the *inter partes* review”).

B. McAlexander’s testimony is not “relevant” here because he was assuming Netlist’s interpretation of the ’608 patent

Netlist has also failed to show that McAlexander’s testimony is “relevant,” 37 C.F.R. § 42.123(a)(2), because there is “no inconsistency” with any position taken by Samsung. *PNC Bank N.A. v. USAA*, IPR2021-01077, Paper 73, at 82–83 (PTAB Jan. 20, 2023) (denying motion to supplement).

McAlexander’s testimony and opinions were expressly “[b]ased on *Netlist’s* apparent view of the scope of the ’608 patent claims,” Tishman Decl. Ex. C at 36 (emphasis added), **not** Samsung’s view, so Samsung is not taking inconsistent positions in the two proceedings. The only party being inconsistent is Netlist, as shown by

Netlist’s complaint against Samsung on the right. When Netlist sued Samsung, Netlist expressly identified the **strobe signal** (DQS) highlighted in yellow — not just the DQ data signal — as part of the “data path,” as shown by the solid red box



above, and expressly pointed to a “delay circuit” on the data path that ***included the strobe signal***, as shown by the dashed red box above. EX1057, 58–59 (yellow highlighting added above); *see also* Tishman Decl. ¶ 15. But after Samsung filed this IPR, Netlist suddenly changed its tune and took the position that the “data path” ***excludes*** the DQS strobe signal, contrary to its complaint above.

C. Netlist failed to show that consideration of McAlexander’s testimony “would be in the interests-of-justice” especially given that it is inadmissible hearsay

Netlist has also failed to show why “consideration of [McAlexander’s deposition] would be in the interests-of-justice,” 37 C.F.R. § 42.123(b), especially “at the eleventh-hour of this [IPR]” when Samsung has no opportunity to respond, *PNC Bank*, IPR2021-01077, Paper 73, at 83–84 (denying motion to supplement).

First, McAlexander’s testimony is inadmissible hearsay: he is not an expert in this IPR and he was not deposed in this IPR. No exceptions apply:

Netlist cannot show McAlexander is “unavailable” under FRE 804 given that Netlist made “no attempt to bring [him] forward as a witness in this [IPR].” *CaptionCall, L.L.C. v. Ultratec, Inc.*, IPR2015-00637, Paper 98, at 15–16 (PTAB Sept. 7, 2016), *appeal dismissed*, No. 2017-1210 (Fed. Cir. Jan. 19, 2022).

Nor can Netlist show that McAlexander’s testimony is “not hearsay under Rule 801(d)(2)(B)–(D).” Mot. 1. “Since an expert witness is not subject to the control of the party opponent [i.e., Samsung] with respect to consultation and

testimony he or she is hired to give, the expert witness cannot be deemed an agent [i.e., of Samsung].” *HTC Corp. v. Telefonaktiebolaget LM Ericsson*, 12 F.4th 476, 489–90 (5th Cir. 2021) (affirming exclusion of expert testimony from another case). Furthermore, construction of the term “data path” is not an issue in McAlexander’s case, *see* Tishman Decl. ¶ 3 & Ex. B at 6, so Netlist cannot show that Samsung “authorized [McAlexander] to make a statement on the subject” of claim construction, or that such testimony was “a matter within the scope” of McAlexander’s engagement, or that Samsung “adopted or believed it to be true.” Fed. R. Evid 801(d)(2)(B)–(D). Indeed, McAlexander’s testimony and opinions were expressly “[b]ased on *Netlist’s* apparent view of the scope of the ’608 patent claims,” Tishman Decl. Ex. C at 36 (emphasis added), *not* Samsung’s view.

Second, no authority supports Netlist’s absurd theory that because “the testimony was given without objections by Samsung” in the *other* proceeding, it “became binding on Samsung” in *this* IPR. Mot. 2. Samsung had no reason to object *during* McAlexander’s deposition because “[Netlist] did not give [Samsung] notice that it was taking [McAlexander’s] deposition for purposes of this [IPR],” which also deprived Samsung of any reason to ask McAlexander questions during his deposition that would be relevant to the construction of “data path” in this IPR. *ExtractionTek Sales*, IPR2022-00625, Paper 33, at 3 (denying motion to supplement); *cf. Berroteran v. Superior Court*, 12 Cal.5th 867, 890–93 (2022)

(holding that discovery deposition from one case normally cannot be introduced in another case given lack of “motive” to ask many questions of your own witness).

Third, McAlexander’s testimony is also inadmissible under FRE 403 given that the testimony has little “probative value” and is “substantially outweighed” by “unfair prejudice,” “unfair delay,” and “wasting time.” The cited testimony is at best *extrinsic* evidence, and the Federal Circuit has expressly cautioned that “there is a virtually unbounded universe of potential extrinsic evidence of some marginal relevance that could be brought to bear on any claim construction question” and “undue reliance on extrinsic evidence poses the risk that it will be used to change the meaning of claims in derogation of the ‘indisputable [intrinsic] records’” *Phillips v. AWH Corp*, 415 F.3d 1303, 1318–19 (Fed. Cir. 2005) (en banc). Thus, the Board “need not resort to extrinsic evidence” to determine the construction of “data path.” *Samsung Elecs. Co. v. Netlist, Inc.*, IPR2022-00615, Paper 96, at 52–53 (PTAB Apr. 17, 2024) (dismissing motion to supplement).

Granting Netlist’s motion at this late date would just invite every party to bombard the Board with endless motions to submit random evidence from outside the IPR, contrary to the interests of justice.

III. CONCLUSION

Netlist’s motion should be denied, as the Board has repeatedly done before.

Dated: Aug. 28, 2024

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CERTIFICATE OF COMPLIANCE

I hereby certify that this **Petitioner’s Opposition to Netlist’s Motion to Submit Late Supplemental Information Under 37 C.F.R. § 42.123(b)** complies with the Order on August 19, 2024 [Paper 34] stating that “Petitioner may file, no later than August 28, 2024, an opposition to Patent Owner’s motion of no more than 5 pages.”

Dated: Aug. 28, 2024

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), I certify that on this 28th day of August, 2024, **Petitioner's Opposition to Netlist's Motion to Submit Late Supplemental Information Under 37 C.F.R. § 42.123(b)** was served by email on the following counsel for Patent Owner:

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Dated: Aug. 28, 2024

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,

Petitioner,

v.

NETLIST, INC.,

Patent Owner

IPR2023-00847

Patent 10,268,608 B2

**DECLARATION OF DANIEL TISHMAN IN OPPOSITION TO NETLIST'S
MOTION TO SUBMIT LATE SUPPLEMENTAL INFORMATION UNDER
37 C.F.R. § 42.123(b)**

DECLARATION

I, Daniel A. Tishman, declare as follows:

1. I am an attorney at the firm of Fish & Richardson P.C., counsel of record for Samsung in *Netlist Inc. v. Samsung Elecs. Co.*, No. 2:22-cv-00293-JRG (E.D. Tex. filed Aug. 1, 2022) (the “EDTX Case”). In that case, Netlist amended the complaint on July 20, 2023 — almost one year after the case was originally filed — to assert U.S. Patent No. 10,268,608. I have personal knowledge of the facts set forth herein, and if called to testify, I could and would competently testify to the same.

2. Pursuant to the scheduling order then in effect, fact discovery in the EDTX Case closed on November 20, 2023. A true and correct copy of that scheduling order is attached as Exhibit A.

3. A true and correct copy of the Claim Construction Memorandum Opinion and Order (Dkt. 228) in the EDTX Case is attached as Exhibit B. Regarding claim construction of the ’608 patent, “the parties[’] only dispute [was] whether the preamble of Claim 1 of the ’608 Patent is limiting.” Ex. B, at 6.

4. Mr. Joseph C. McAlexander III, Samsung’s technical expert, served his Initial Expert Report on November 20, 2023, in accordance with the scheduling order. A true and correct copy of an excerpt of Mr. McAlexander’s Initial Expert Report is attached as Exhibit C.

5. At Netlist's request, Samsung agreed to extend the expert discovery cutoff in the EDTX Case from January 9, 2024, to February 16, 2024. A true and correct copy of the court's amended scheduling order showing that change is attached as Exhibit D.

6. Mr. McAlexander was scheduled to be deposed on February 16, 2024, the last day of expert discovery. However, he was ultimately unavailable for deposition that day due to illness. True and correct copies of email correspondence between myself and Netlist's counsel concerning rescheduling Mr. McAlexander's deposition are attached as Exhibits E through I.

7. On February 14, 2024, Samsung therefore offered to look into alternative dates for Mr. McAlexander's deposition. Exhibit E, at 3 (Feb. 14, 2024, email).

8. On February 19, 2024, Samsung offered Mr. McAlexander for a rescheduled deposition on February 26, 2024. Exhibit E, at 2 (Feb. 19, 2024, email).

9. On February 22, 2024, Netlist's counsel responded that "February 26th does not work for Netlist" and requested an alternative date. Exhibit E, at 1 (Feb. 22, 2024, email). The same day, Samsung offered March 8, 2024, as an alternative date for Mr. McAlexander's deposition. Exhibit E, at 1 (Feb. 22, 2024, email).

10. On February 25, 2024, Netlist’s counsel informed me that Netlist was not available for the McAlexander deposition offered on March 8 and specifically requested a date the week of March 11. Ex. F, at 2 (Feb. 25, 2024, email). Two days later, I responded offering Mr. McAlexander on March 14, 2024, during the week requested by Netlist. Ex. F at 1 (Feb. 27, 2024, email).

11. Despite confirming that Netlist was available on March 14, Netlist declined to take Mr. McAlexander’s deposition on that date, stating “it does not make sense to proceed with Mr. McAlexander’s expert deposition.” Ex. G, at 1 (Mar. 11, 2024, email). Netlist instead requested Mr. McAlexander’s “availability for early April.” *Id.*

12. On March 19, Samsung offered Mr. McAlexander for deposition on April 3, 2024, as Netlist requested. Ex. H, at 3 (Mar. 19, 2024, email). On March 29, Netlist declined to take Mr. McAlexander’s deposition on April 3 and requested a date the second week of April instead. Ex. H, at 2 (Mar. 29, 2024, email). On April 4, Samsung offered Mr. McAlexander for deposition on April 9, noting that Mr. McAlexander would have very little availability after that date. Ex. H, at 2 (Apr. 4, 2024, email). On April 5, Netlist turned down the April 9 date. Ex. H, at 1 (Apr. 5, 2024, email).

13. On June 18, 2024, Samsung offered Mr. McAlexander for a rescheduled deposition on July 10, 2024. Ex. I, at 2 (June 18, 2024, email). Netlist

responded that it was unavailable on July 10 and requested July 19 instead. Ex. I, at 2 (June 19, 2024, email). On July 8, 2024, Samsung confirmed that July 19 worked for Mr. McAlexander. Ex. I, at 1 (July 8, 2024, email). Mr. McAlexander's deposition proceeded on that date.

14. Netlist's counsel deposed Mr. McAlexander on July 19, 2024. A true and correct copy of an excerpt from this deposition is attached as Exhibit J. A true and correct copy of Exhibit 101, which was marked during this excerpt of Mr. McAlexander's deposition, is attached as Exhibit K.

15. On August 1, 2024, Netlist's counsel advised Samsung's counsel that Netlist planned to seek production in this IPR of an excerpt of Mr. McAlexander's testimony (attached as Exhibit J) relating to the meaning of "data path." In response, I informed Netlist's counsel that Samsung agreed to remove any confidentiality restrictions under the EDTX Protective Order with respect to the excerpt of Mr. McAlexander's testimony identified by Netlist, and I repeatedly requested that Netlist similarly remove any confidentiality restrictions under the EDTX Protective Order with respect to Netlist's infringement contentions for the claim limitation "data path." Despite my numerous requests, Netlist's counsel never removed the confidentiality restrictions under the EDTX Protective Order with respect to Netlist's infringement contentions for the claim limitation "data path," thus precluding the Board in this IPR from seeing Netlist's interpretation of

“data path” in its infringement contentions in the EDTX Case. A true and correct copy of the e-mail correspondence between counsel for Samsung and Netlist relating to Mr. McAlexander’s testimony and Netlist’s infringement contentions in the EDTX Case is attached as Exhibit L.

I, Daniel A. Tishman, do hereby declare and state, that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, under Section 1001 of Title 18 of the United States Code.

Executed on: August 23, 2024



Daniel A. Tishman

Exhibit A

**UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION**

NETLIST, INC.,	)	
	)	
Plaintiff,	)	
	)	Case No. 2:22-cv-293-JRG
vs.	)	
	)	JURY TRIAL DEMANDED
SAMSUNG ELECTRONICS CO, LTD;	)	(Lead Case)
SAMSUNG ELECTRONICS AMERICA,	)	
INC.; SAMSUNG SEMICONDUCTOR	)	
INC.,	)	
	)	
Defendants.	)	

NETLIST, INC.,	)	
	)	
Plaintiff,	)	
	)	Case No. 2:22-cv-294-JRG
vs.	)	
	)	JURY TRIAL DEMANDED
MICRON TECHNOLOGY, INC.; MICRON	)	
SEMICONDUCTOR PRODUCTS, INC.;	)	
MICRON TECHNOLOGY TEXAS LLC,	)	
	)	
Defendants.	)	

**THIRD AMENDED
DOCKET CONTROL ORDER**

Before this Court is the parties' Joint Motion to Amend Docket Control Order. Having considered the same, the Court is of the opinion the motion should be **GRANTED**. Accordingly, the deadlines in the above-captioned cases are amended as follows:

Current Deadline	Amended Deadline	Event
April 15, 2024	No change	*Jury Selection – 9:00 a.m. in Marshall, Texas
7 days before Jury Selection	No change	*Defendant to disclose final invalidity theories, final prior art references/combinations, and final equitable defenses

10 days before Jury Selection	No change	*Plaintiff to disclose final election of asserted claims
March 18, 2024	No change	* If a juror questionnaire is to be used, an editable (in Microsoft Word format) questionnaire shall be jointly submitted to the Deputy Clerk in Charge by this date.
March 11, 2024	No change	* Pretrial Conference – 9:00 am in Marshall, Texas before Judge Roy Payne
March 4, 2024	No change	*Notify Court of Agreements Reached During Meet and Confer The parties are ordered to meet and confer on any outstanding objections or motions <i>in limine</i> . The parties shall advise the Court of any agreements reached no later than 1:00 p.m. three (3) business days before the pretrial conference.
March 4, 2024	No change	*File Joint Pretrial Order, Joint Proposed Jury Instructions, Joint Proposed Verdict Form, Responses to Motions <i>in Limine</i> , Updated Exhibit Lists, Updated Witness Lists, and Updated Deposition Designations
February 26, 2024	No change	*File Notice of Request for Daily Transcript or Real Time Reporting. If a daily transcript or real time reporting of court proceedings is requested for trial, the party or parties making said request shall file a notice with the Court and e-mail the Court Reporter, Shelly Holmes, at shelly_holmes@txed.uscourts.gov .
February 20, 2024	No change	File Motions <i>in Limine</i> The parties shall limit their motions <i>in limine</i> to issues that if improperly introduced at trial would be so prejudicial that the Court could not alleviate the prejudice by giving appropriate instructions to the jury.
February 20, 2024	No change	Serve Objections to Rebuttal Pretrial Disclosures
February 12, 2024	No change	Serve Objections to Pretrial Disclosures; and Serve Rebuttal Pretrial Disclosures
January 29, 2024	No change	Serve Pretrial Disclosures (Witness List, Deposition Designations, and Exhibit List) by the Party with the Burden of Proof
January 22, 2024	January 30, 2024	*Response to Dispositive Motions (including <i>Daubert</i> Motions). Responses to dispositive motions that were filed <u>prior</u> to the dispositive

		motion deadline, including <i>Daubert</i> Motions, shall be due in accordance with Local Rule CV-7(e), not to exceed the deadline as set forth in this Docket Control Order. Motions for Summary Judgment shall comply with Local Rule CV-56.
January 8, 2024	January 16, 2024	*File Motions to Strike Expert Testimony (including <i>Daubert</i> Motions) No motion to strike expert testimony (including a <i>Daubert</i> motion) may be filed after this date without leave of the Court.
January 8, 2024	January 16, 2024	*File Dispositive Motions No dispositive motion may be filed after this date without leave of the Court. Motions shall comply with Local Rule CV-56 and Local Rule CV-7. <u>Motions to extend page limits will only be granted in exceptional circumstances. Exceptional circumstances require more than agreement among the parties.</u>
December 23, 2023	January 9, 2024	Deadline to Complete Expert Discovery
December 11, 2023	December 18, 2023	Serve Disclosures for Rebuttal Expert Witnesses
November 13, 2023	November 20, 2023	Deadline to Complete Fact Discovery and File Motions to Compel Discovery
November 13, 2023	November 20, 2023	Serve Disclosures for Expert Witnesses by the Party with the Burden of Proof

(*) indicates a deadline that cannot be changed without an acceptable showing of good cause. Good cause is not shown merely by indicating that the parties agree that the deadline should be changed.

I. ADDITIONAL REQUIREMENTS

Mediation: While certain cases may benefit from mediation, such may not be appropriate for every case. The Court finds that the Parties are best suited to evaluate whether mediation will benefit the case after the issuance of the Court's claim construction order. Accordingly, the Court **ORDERS** the Parties to file a Joint Notice indicating whether the case should be referred for mediation **within fourteen days of the issuance of the Court's claim construction order**. As a part of such Joint Notice, the Parties should indicate whether they have a mutually agreeable mediator for the Court to consider. If the Parties disagree about

whether mediation is appropriate, the Parties should set forth a brief statement of their competing positions in the Joint Notice.

Summary Judgment Motions, Motions to Strike Expert Testimony, and Daubert Motions: For each motion, the moving party shall provide the Court with two (2) hard copies of the completed briefing (opening motion, response, reply, and if applicable, sur-reply), excluding exhibits, in D-three-ring binders, appropriately tabbed. All documents shall be single-sided and must include the CM/ECF header. These copies shall be delivered to the Court within three (3) business days after briefing has completed. For expert-related motions, complete digital copies of the relevant expert report(s) and accompanying exhibits shall be submitted on a single flash drive to the Court. Complete digital copies of the expert report(s) shall be delivered to the Court no later than the dispositive motion deadline.

Indefiniteness: In lieu of early motions for summary judgment, the parties are directed to include any arguments related to the issue of indefiniteness in their *Markman* briefing, subject to the local rules' normal page limits.

Lead Counsel: The Parties are directed to Local Rule CV-11(a)(1), which provides that “[o]n the first appearance through counsel, each party shall designate a lead attorney on the pleadings or otherwise.” Additionally, once designated, a party’s lead attorney may only be changed by the filing of a Motion to Change Lead Counsel and thereafter obtaining from the Court an Order granting leave to designate different lead counsel. The true lead counsel should be designated early and should not expect to parachute in as lead once the case has been largely developed.

Motions for Continuance: The following will not warrant a continuance nor justify a failure to comply with the discovery deadline:

- (a) The fact that there are motions for summary judgment or motions to dismiss pending;
- (b) The fact that one or more of the attorneys is set for trial in another court on the same day, unless the other setting was made prior to the date of this order or was made as a special provision for the parties in the other case;
- (c) The failure to complete discovery prior to trial, unless the parties can demonstrate that it was impossible to complete discovery despite their good faith effort to do so.

Amendments to the Docket Control Order (“DCO”): Any motion to alter any date on the DCO shall take the form of a motion to amend the DCO. The motion to amend the DCO shall include a proposed order that lists all of the remaining dates in one column (as above) and the proposed changes to each date in an additional adjacent column (if there is no change for a date the proposed date column should remain blank or indicate that it is unchanged). In other words, the DCO in the proposed order should be complete such that one can clearly see all the remaining deadlines and the changes, if any, to those deadlines, rather than needing to also refer to an earlier version of the DCO.

Proposed DCO: The Parties’ Proposed DCO should also follow the format described above under “Amendments to the Docket Control Order (‘DCO’).”

Joint Pretrial Order: In the contentions of the Parties included in the Joint Pretrial Order, the Plaintiff shall specify all allegedly infringed claims that will be asserted at trial. The Plaintiff shall also specify the nature of each theory of infringement, including under which subsections of 35 U.S.C. § 271 it alleges infringement, and whether the Plaintiff alleges divided infringement or infringement under the doctrine of equivalents. Each Defendant shall indicate the nature of each theory of invalidity, including invalidity for anticipation, obviousness, subject-matter eligibility, written description, enablement, or any other basis for invalidity. The Defendant shall also specify each prior art reference or combination of references upon which the Defendant shall rely at trial, with respect to each theory of invalidity. The contentions of the Parties may not be amended, supplemented, or dropped without leave of the Court based upon a showing of good cause.

Trial: All parties must appear in person at trial. All non-individual (including but not limited to corporate) parties must appear at trial through the presence in person of a designated representative. Once they have appeared, any representative of a non-individual party shall not be replaced or substituted without express leave of Court.

So ORDERED and SIGNED this 9th day of November, 2023.



RODNEY GILSTRAP
UNITED STATES DISTRICT JUDGE

Exhibit B

**IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION**

NETLIST, INC.,	§	
	§	
<i>Plaintiff,</i>	§	
	§	
v.	§	CIVIL ACTION NO. 2:22-CV-00293-JRG
	§	(Lead Case)
SAMSUNG ELECTRONICS CO, LTD, <i>et</i>	§	
<i>al.</i>	§	
	§	
<i>Defendants.</i>	§	

NETLIST, INC.,	§	
	§	
<i>Plaintiff,</i>	§	
	§	
v.	§	CIVIL ACTION NO. 2:22-CV-00294-JRG
	§	
MICRON TECHNOLOGY, INC., <i>et al.</i>	§	
	§	
<i>Defendants.</i>	§	

CLAIM CONSTRUCTION MEMORANDUM OPINION AND ORDER

In these consolidated patent cases, Netlist alleges infringement by Samsung and Micron (and their affiliates) (together, “Defendants”) of claims from four patents related to computer memory—U.S. Patent Nos. 7,619,912 (the “’912 Patent”); 9,858,215 (the “’215 Patent”); 10,268,608 (the “’608 Patent”); and 11,093,417 (the “’417 Patent”). The parties present ten disputes¹ about the proper construction of claim terms from the patents. Having considered the

¹ The parties briefed disputes for eleven claim terms, but Netlist has since withdrawn its assertion of a number of claims from the ’912 Patent. *See* Joint Notice of Mootness Regarding Construction of Claims No Longer Asserted, Dkt. No. 201. As result, there is no longer a live dispute concerning one of the terms. *See id.* at 2–3.

parties' briefing and arguments of counsel during a September 26, 2023 hearing, the Court resolves the disputes as follows.

I. BACKGROUND

A. U.S. Patent 7,619,912

The '912 Patent relates "specifically to devices and methods for improving the performance, the memory capacity, or both, of memory modules." '912 Patent at 1:22–24. Generally, doubling the memory size of a DRAM² device more than doubles the associated cost. For example,

by fabricating a 1-GB memory module using thirty-six 256-Mb memory devices [instead of 18 512-Mb devices], the cost of the resulting 1-GB memory module can be reduced since the unit cost of each 256-Mb memory device is typically lower than one-half the unit cost of each 512-Mb memory device. The cost savings can be significant, even though twice as many 256-Mb memory devices are used in place of the 512-Mb memory devices.

Id. at 4:51–58. "In other words, the price per bit ratio of the higher-density DRAM devices is greater than that of the lower-density DRAM devices." *Id.* at 4:62–64. Thus, under certain market conditions, there is an economic incentive for using pairs of lower-density DRAM devices instead of individual higher-density devices. *Id.* at 4:64–5:5.

The problem, however, is that a computer system may not be configured to provide the required control signals, like chip-select signals, for the lower-density chips. For example, a system expecting four ranks of memory might only provide two chip-select signals, but more are needed if replacing higher-density devices with lower-density devices. *See id.* at 7:20–35.

To address the problem, the patent teaches using a logic element, such as a programmable

² DRAM stands for "dynamic random-access memory." Stone Decl., Dkt. No. 129-6 ¶ 23. That the memory is "dynamic" means "the memory only remembers its information while power is maintained; if power is turned off, the contents of the DRAMs are lost." *Id.*

logic device (PLD), to “translate” the computer system’s signals to signals appropriate for the lower-density memory devices. As an example, Table 1 shows a logic table for translating two chip-select signals and a row/column address signal from the computer (CS_0 , CS_1 , A_{n+1}) to four chip-select signals connected to the memory devices (CA_{0A} , CA_{0B} , CA_{1A} , CA_{1B}). *Id.* at 7:60–67.

The claims recite this “translation” functionality as responding to command and input signals from the computer by generating command and output signals to the memory devices. For example, Claim 1 recites:

a circuit mounted to the printed circuit board, the circuit comprising
a logic element and a register, **the logic element** receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input control signals corresponding to **a second number of DDR memory devices** arranged in a second number of ranks, the second number of DDR memory devices smaller than **the first number of DDR memory devices** and the second number of ranks less than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of DDR memory devices arranged in the first number of ranks, wherein *the circuit further responds to a first command signal and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices*, the first command signal and the set of input control signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks;

Id. at 32:66–33:23 (all emphasis added). The “second number of DDR memory devices” are the higher-density devices replaced by the lower-density “first number of DDR memory devices.”

B. U.S. Patents 9,858,215 and 11,093,417

The '215 and '417 Patents have a common disclosure. Like the '912 Patent, these patents relate “specifically to devices and methods for improving the performance, the memory capacity, or both, of memory modules.” '215 Patent at 1:43–45; *see also* '417 Patent at 1:48–50. Typically, DRAM is arranged in “ranks.” '215 Patent at 2:41–47. During operation, those ranks are selected by address and command signals received from the processor, such as chip-select signals. *Id.* at 2:61–65.

As shown in FIG. 2 (below), in a conventional memory module, each memory device (30a, 30b) has data lines (DQa, DQb) and a strobe line (DQSa, DQ Sb). The data lines (102a, 102b) are connected to a common data line (112) and the strobe lines (104a, 104b) are connected to a common strobe line (114). This means the computer system is exposed to the loads of both memory devices at the same time, which can negatively affect performance. '215 Patent at 6:60–7:13; *see also id.* at 9:43–45 (“increased load on the memory bus can degrade speed performance”).

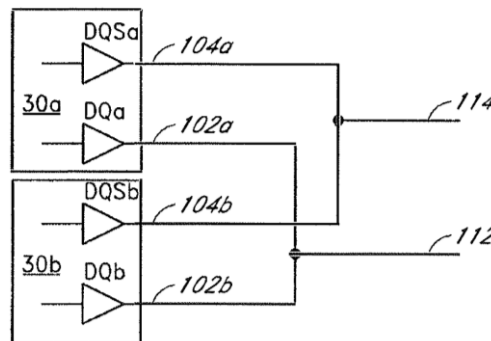


FIG. 2 of the '215 and '417 Patents

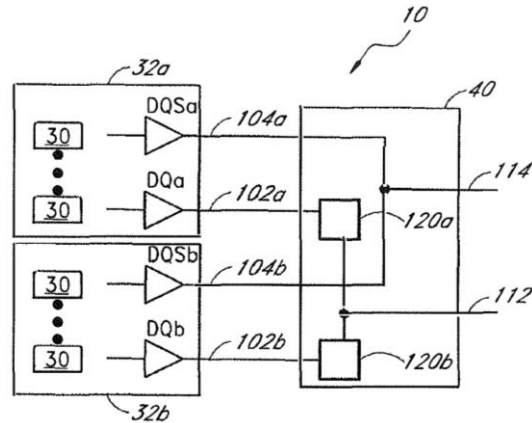


FIG. 4A of the '215 and '417 Patents

In contrast, FIG. 4A (above) shows a circuit (40) that “selectively isolates” the loads of the memory devices from the computer system. The circuit has a pair of switches (120a, 120b) on data lines (102a, 102b). Each switch can be actuated to selectively connect one or both data lines to a common data line (112). This allows a data signal to be transmitted from the memory controller to the memory devices of one or both ranks (32a, 32b) via the data lines (102a, 102b) and thereby isolate the memory devices when advantageous to do so. *See generally* '215 Patent at 8:27–56.

Notably, these patents also include the subject matter of the '912 Patent. Specifically, the description relating to FIGS. 9A–19 of the '215 Patent and '417 Patent is generally the same as the description of FIGS. 1A–14 of the '912 Patent. The '215 Patent and '417 Patent add sections on “Load Isolation,” “Back-to-Back Adjacent Read Commands,” “Serial-Presence-Detect Device,” “Tied Data Strobe Signal Pins,” and “Memory Density Multiplication,” in addition to the '912 Patent’s subject matter on “Command Signal Translation.” *See generally* '215 Patent at 5:18–13:49, 17:41–37:9.

C. U.S. Patents 10,268,608

The '608 Patent relates specifically to “multi-rank memory modules and methods of

operation.” ’608 Patent at 1:37–38. The patent teaches a memory module having memory devices, a module control circuit, and buffer circuits between respective sets of data signal lines in a data bus and respective sets of the memory devices. Each buffer circuit is positioned between a set of data lines and a set of memory devices. The buffer circuit buffers data signals in response to module control and clock signals. Each respective buffer circuit includes a delay circuit configured to delay the respective set of data signals by an amount determined based on at least one of the module control signals. ’608 Patent at [57].

As far as claim construction is concerned, the parties only dispute whether the preamble of Claim 1 of the ’608 Patent is limiting.

II. LEGAL STANDARDS

A. Claim Construction Generally

“[T]he claims of a patent define the invention to which the patentee is entitled the right to exclude.” *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc). As such, if the parties dispute the scope of the claims, the court must determine their meaning. *See, e.g., Verizon Servs. Corp. v. Vonage Holdings Corp.*, 503 F.3d 1295, 1317 (Fed. Cir. 2007) (Gajarsa, J., concurring in part); *see also Markman v. Westview Instruments, Inc.*, 517 U.S. 370, 390 (1996), *aff’g*, 52 F.3d 967, 976 (Fed. Cir. 1995) (en banc).

Claim construction, however, “is not an obligatory exercise in redundancy.” *U.S. Surgical Corp. v. Ethicon, Inc.*, 103 F.3d 1554, 1568 (Fed. Cir. 1997). Rather, “[c]laim construction is a matter of [resolving] disputed meanings and technical scope, to clarify and when necessary to explain what the patentee covered by the claims” *Id.* A court need not “repeat or restate every claim term in order to comply with the ruling that claim construction is for the court.” *Id.*

When construing claims, “[t]here is a heavy presumption that claim terms are to be given

their ordinary and customary meaning.” *Aventis Pharm. Inc. v. Amino Chems. Ltd.*, 715 F.3d 1363, 1373 (Fed. Cir. 2013) (citing *Phillips*, 415 F.3d at 1312–13). Courts must therefore “look to the words of the claims themselves . . . to define the scope of the patented invention.” *Id.* (citations omitted). The “ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application.” *Phillips*, 415 F.3d at 1313. This “person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification.” *Id.*

Intrinsic evidence is the primary resource for claim construction. *See Power-One, Inc. v. Artesyn Techs., Inc.*, 599 F.3d 1343, 1348 (Fed. Cir. 2010) (citing *Phillips*, 415 F.3d at 1312). For certain claim terms, “the ordinary meaning of claim language as understood by a person of skill in the art may be readily apparent even to lay judges, and claim construction in such cases involves little more than the application of the widely accepted meaning of commonly understood words.” *Phillips*, 415 F.3d at 1314; *see also Medrad, Inc. v. MRI Devices Corp.*, 401 F.3d 1313, 1319 (Fed. Cir. 2005) (“We cannot look at the ordinary meaning of the term . . . in a vacuum. Rather, we must look at the ordinary meaning in the context of the written description and the prosecution history.”). But for claim terms with less-apparent meanings, courts consider “those sources available to the public that show what a person of skill in the art would have understood disputed claim language to mean . . . [including] the words of the claims themselves, the remainder of the specification, the prosecution history, and extrinsic evidence concerning relevant scientific principles, the meaning of technical terms, and the state of the art.” *Phillips*, 415 F.3d at 1314.

B. Means-Plus-Function Claiming³

A patent claim may be expressed using functional language. *See* 35 U.S.C. § 112 ¶ 6 (pre-AIA); *Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1347–49 & n.3 (Fed. Cir. 2015) (en banc in relevant portion). Under 35 U.S.C. § 112 ¶ 6, a structure may be claimed as a “means . . . for performing a specified function,” and an act may be claimed as a “step for performing a specified function.” *Masco Corp. v. United States*, 303 F.3d 1316, 1326 (Fed. Cir. 2002). When it applies, § 112 ¶ 6 limits the scope of the functional term “to only the structure, materials, or acts described in the specification as corresponding to the claimed function and equivalents thereof.” *Williamson*, 792 F.3d at 1347.

However, § 112 ¶ 6 does not apply to all functional claim language. There is a rebuttable presumption that § 112 ¶ 6 applies when the claim language includes “means” or “step for” terms, and a rebuttable presumption it does *not* apply in the absence of those terms. *Masco Corp.*, 303 F.3d at 1326; *Williamson*, 792 F.3d at 1348. These presumptions stand or fall according to whether one of ordinary skill in the art would understand the claim with the functional language to denote sufficiently definite structure or acts for performing the function in the context of the entire specification. *See Media Rights Techs., Inc. v. Capital One Fin. Corp.*, 800 F.3d 1366, 1372 (Fed. Cir. 2015) (noting § 112 ¶ 6 does not apply when “the claim language, read in light of the specification, recites sufficiently definite structure” (quotation marks omitted) (citing *Williamson*, 792 F.3d at 1349; *Robert Bosch, LLC v. Snap-On Inc.*, 769 F.3d 1094, 1099 (Fed. Cir. 2014))); *Masco Corp.*, 303 F.3d at 1326 (noting § 112 ¶ 6 does not apply when the claim includes an “act” corresponding

³ Each of the patents has an effective filing date before the effective date of the Leahy-Smith America Invents Act, Pub. L. No. 112-29, § 3, 125 Stat. 284, 285-93 (2011). The Court therefore refers to the pre-AIA version of the statute.

to “how the function is performed”); *Personalized Media Commc’ns, LLC v. I.T.C.*, 161 F.3d 696, 704 (Fed. Cir. 1998) (noting § 112 ¶ 6 does not apply when the claim includes “sufficient structure, material, or acts within the claim itself to perform entirely the recited function . . . even if the claim uses the term ‘means.’” (quotation marks and citation omitted)).

Construing a means-plus-function limitation involves multiple steps. “The first step . . . is a determination of the function of the means-plus-function limitation.” *Medtronic, Inc. v. Advanced Cardiovascular Sys., Inc.*, 248 F.3d 1303, 1311 (Fed. Cir. 2001). “The next step is to determine the corresponding structure described in the specification and equivalents thereof. Structure disclosed in the specification is corresponding structure only if the specification or prosecution history clearly links or associates that structure to the function recited in the claim.” *Id.* (citations and quotations omitted). The corresponding structure “must include all structure that actually performs the recited function.” *Default Proof Credit Card Sys. v. Home Depot U.S.A., Inc.*, 412 F.3d 1291, 1298 (Fed. Cir. 2005). But § 112 does not permit “incorporation of structure from the written description beyond that necessary to perform the claimed function.” *Micro Chem., Inc. v. Great Plains Chem. Co.*, 194 F.3d 1250, 1258 (Fed. Cir. 1999).

“[S]tructure can be recited in various ways, including [by using] ‘a claim term with a structural definition that is either provided in the specification or generally known in the art,’ or a description of the claim limitation’s operation and ‘how the function is achieved in the context of the invention.’” *Dyfan, LLC v. Target Corp.*, 28 F.4th 1360, 1366 (Fed. Cir. 2022) (quoting *Apple, Inc. v. Motorola, Inc.*, 757 F.3d 1286, 1299 (Fed. Cir. 2005)). For § 112 ¶ 6 limitations implemented by a programmed general-purpose computer or microprocessor, the corresponding structure described in the patent specification must usually include an algorithm for performing the function. *WMS Gaming Inc. v. Int’l Game Tech.*, 184 F.3d 1339, 1349 (Fed. Cir. 1999). In that case, the

corresponding structure is not a general-purpose computer but rather the special-purpose computer programmed to perform the disclosed algorithm. *Aristocrat Techs. Austl. Pty Ltd. v. Int'l Game Tech.*, 521 F.3d 1328, 1333 (Fed. Cir. 2008).

C. Indefiniteness

“[A] patent is invalid for indefiniteness if its claims, read in light of the specification delineating the patent, and the prosecution history, fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention.” *Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 901 (2014). The claims “must be precise enough to afford clear notice of what is claimed” while recognizing that “some modicum of uncertainty” is inherent due to the limitations of language. *Id.* at 908.

“Indefiniteness must be proven by clear and convincing evidence.” *Sonix Tech. Co. v. Publ'ns Int'l, Ltd.*, 844 F.3d 1370, 1377 (Fed. Cir. 2017). And in the context of § 112 ¶ 6, “[t]he party alleging that the specification fails to disclose sufficient corresponding structure must make that showing by clear and convincing evidence.” *TecSec, Inc. v. IBM*, 731 F.3d 1336, 1349 (Fed. Cir. 2013) (quoting *Budde v. Harley-Davidson, Inc.*, 250 F.3d 1369, 1380–81 (Fed. Cir. 2001)).

III. THE LEVEL OF ORDINARY SKILL IN THE ART

The level of ordinary skill in the art is the skill level of a hypothetical person who is presumed to have known the relevant art at the time of the invention. *In re GPAC*, 57 F.3d 1573, 1579 (Fed. Cir. 1995). In resolving the appropriate level of ordinary skill, courts consider the types of and solutions to problems encountered in the art, the speed of innovation, the sophistication of the technology, and the education of workers active in the field. *Id.* Importantly, “[a] person of ordinary skill in the art is also a person of ordinary creativity, not an automaton.” *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 421 (2007).

Only Micron offers, through its expert's declaration, a level of ordinary skill in the art for consideration. According to Micron's expert, a skilled artisan at the time of invention for the '215 and '417 Patents

would have been someone with an advanced degree in electrical or computer engineering and at least two years working in the field, or a bachelor's degree in such engineering disciplines and at least three years working in the field. Such a person would have been knowledgeable about the design and operation of computer memories, most particularly DRAM and SDRAM devices that were compliant with various standards of the day, and how they interact with other components of a computer system, such as memory controllers. He or she would also have been familiar with the structure and operation of circuitry used to access and control computer memories, including sophisticated circuits such as ASICs and CPLDs and less sophisticated circuits such as tri-state buffers, flip flops, and registers.

Stone Decl., Dkt. No. 144-3 ¶ 21. Since no other party challenges that proposed level of skill, the Court adopts it for analysis of the disputed terms.

IV. THE DISPUTED TERMS

- A. “first number of DDR memory devices arranged in a first number of ranks” and “second number of DDR memory devices in a second number of ranks” ('912 Patent);**
- “memory devices mounted on the printed circuit board and arranged in a plurality of N-bit wide ranks” ('417 Patent);**
- “plurality of memory integrated circuits mounted on the printed circuit board and arranged in a plurality of ranks including a first rank and a second rank” ('215 Patent)**

Netlist's Construction	Defs.' Construction
“a predetermined group of [DDR] memory devices on a memory module that can send or receive a fixed number of data bits via a fixed width data bus, in response to a read or write command and independently from other [DDR] memory devices on the memory module” ⁴	“Rank” means “an independent set of one or more memory devices on a memory module that act together in response to command signals, including chip-select signals, to read or write the full bit-width of the memory module.”

The parties present two disputes, each centered on the meaning of “rank.” First, they dispute whether a “rank” of memory can have a single memory device. Second, they dispute whether a “rank” of memory must be capable of sending or receiving a fixed number of data bits via a fixed width data bus. *See* Dkt. No. 129 at 1.

1. *Whether a rank of memory can be a single memory device*

According to Netlist, a “rank” must include more than one memory device. Netlist first relies on JEDEC⁵ standards at the time of the effective filing dates of the underlying applications, which require a rank of either 64 or 72 bits, but does not define devices wider than 16 bits. Dkt. No. 129 at 2–4. Netlist also relies on Micron’s expert’s testimony that “[i]n the past for this definition of a rank . . . it has been more than one chip.” *Id.* at 2–3 (quoting Strone Depo. Tr., Dkt. No. 129-5 at 44:15–20). Netlist says the specification supports this conclusion by consistently referring to “ranks” as multiple memory devices (plural). *Id.* at 4.

Defendants counter with four reasons why the intrinsic evidence shows a “rank” can be a single memory device. First, the ’215 Patent describes and claims “*at least one* first memory

⁴ Netlist’s proposed construction for the ’912 Patent includes the reference to “DDR.” *See* Joint Cl. Constr. Chart, Dkt. No. 160-1 at 1 (Term 1). Also, Netlist’s proposed construction for the ’215 Patent uses “memory integrated circuits” rather than “memory devices.” *Id.* at 8 (Term 14).

⁵ JEDEC, or the Joint Electron Device Engineering Council, sets specifications for semiconductor memory circuits.

integrated circuit in [a] first rank and *at least one* second memory integrated circuit in [a] second rank,” suggesting the possibility of a one-device rank. Dkt. No. 143 at 2 (citing ’215 Patent at 3:31–35, 37:34–38; emphasis added). Second, Claim 55 of the ’912 Patent recites “each rank . . . comprises a plurality of DDR DRAM chip packages,” so if “rank” requires more than one memory device this phrase is superfluous. *Id.* Third, the specification repeatedly contemplates memory modules with two memory devices arranged in two ranks, one device in each rank. *Id.* at 2–3 (citing, *inter alia*, Figure 6A of the ’912 Patent). Finally, cited prior art defines a “rank” as having *one or more* memory devices. *Id.* at 3 (quoting U.S. Patent 6,982,892 at 2:60–61 (emphasis added)).

Regarding Netlist’s *extrinsic* evidence, Defendants call it unnecessary in light of the *intrinsic* evidence and “untethered to the asserted patents or their priority dates.” *Id.* at 4–5. Regardless, it notes one treatise from around the time of the invention states “a rank of memory is a ‘bank’ of *one or more* DRAM devices that operate in lockstep in response to a given command.” *Id.* at 5 (citing Bruce Jacob et al., *Memory Systems: Cache, DRAM, Disk* (2007), Dkt. No. 129-19 at 413 (emphasis added)).

The Court agrees with Defendants. As Jacob explains:

In modern memory systems, multiple DRAM devices are commonly grouped together to provide the data bus width and capacity required by a given memory system. For example, 18 DRAM devices, each with a 4-bit-wide data bus, are needed in a given rank of memory to form a 72-bit-wide data bus. In contrast, embedded systems that do not require as much capacity or data bus width typically use fewer devices in each rank of memory—*sometimes as few as one device per rank*.

Bruce Jacob et al., *Memory Systems: Cache, DRAM, Disk* (2007), Dkt. No. 129-19 at 414 (emphasis added). Although Netlist stresses the last sentence of this excerpt applies only to embedded systems, Dkt. No. 150 at 4, nothing to which Netlist refers suggests the ordinary meaning of “rank”

differs depending on the system's complexity. To the contrary, while a one-device rank may be more likely found in an embedded system rather than a personal computer or server, Jacob shows the ordinary meaning of "rank" applies to both types of systems.

Other evidence supports this conclusion. For one, Jacob's definition is consistent with the PTAB's preliminary construction in a decision granting *inter partes* review of the '215 Patent. *See* Dkt. No. 143-3 at 12 ("On this preliminary record, we determine that the intrinsic evidence supports Petitioner's position that a rank may have only one memory device."). Perhaps most persuasively, Netlist itself previously stated a "rank" can be a single device. *See* App. Br., Dkt. No. 143-23 at 7 (noting that, in FIG. 2 of U.S. Patent 7,881,150, "each 'rank' includes only a single memory device"⁶).

Netlist's best argument relates to the JEDEC standards at the time, but it is still not persuasive. Those standards require a rank of 64 or 72 bits, but do not define DDR memory greater than 16 bits. *See* Dkt. No. 129 at 2. Thus, simple math suggests there will never be a rank consisting of only one memory device in an embodiment using that standard. That, however, does not alter the ordinary meaning of "rank" as used in the claims. Accordingly, the Court concludes a "rank" can include a single memory device.

2. Netlist's "fixed width data bus" requirement and "partial read" capability

Netlist claims the parties disagree about how a skilled artisan would determine which memory devices on a memory module belong to a particular rank. Dkt. No. 129 at 7. To help in that regard, Netlist asserts each "rank" is associated with its own chip-select signal and outputs or receives data via a "fixed width" bus, and "[n]othing in the '912 patent suggests . . . a rank of memory

⁶ FIG. 2 of the '150 Patent is identical to FIG. 2 of the '215 and '417 Patents).

devices refers to a group of memory devices that is dynamically reconstituted to account for the changing memory bit width.” *Id.* at 7–8. According to Netlist, “a POSITA would understand that a ‘rank’ must have the capability to send or receive the full bit-width of the memory module, but need not always do so.” *Id.* at 9. Defendants question why this dispute matters, but nonetheless note the “patents contemplate ‘increasing the number of memory devices per rank.’” Dkt. No. 143 at 6 (citing ’912 Patent at 2:24–27).

To start, the Court agrees with Netlist that nothing in the patent suggests a changing memory bit width for a particular embodiment. The language to which Defendants point simply compares different memory modules to one another. *See* ’912 Patent at 2:27–30 (“For example, a memory module with four ranks has double the memory capacity of a memory module with two ranks and four times the memory capacity of a memory module with one rank.”).

That said, Netlist’s proposed construction on this issue is too light on structure and too heavy on “capabilities.” “Rank” has a clear structural definition, and the Court need not resolve the various capabilities the embodiments may or may not have because of that structure. As such, the Court declines to adopt Netlist’s “fixed width data bus” language and “partial read” capability as not sufficiently tied to structure. *See Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1468 (Fed. Cir. 1990) (“Apparatus claims cover what a device *is*, not what a device *does*.”).

Finally, the Court rejects Defendants’ proposed language of “in lockstep” as potentially confusing to a jury for those cases in which a “rank” comprises only one device. The Court, however, agrees that, in embodiments with ranks having more than one memory device, those devices operate together. With that in mind, the Court construes “rank” in these terms as “a ‘bank’ of one or more devices on a memory module that operate in response to a given signal.”

B. “[row/column] address signal” (’912 Patent, all claims)

Netlist’s Construction	Defs.’ Construction
Plain and ordinary meaning.	“a varying electrical impulse that conveys an address of either a row or a column of memory locations from one point to another”

Each claim requires “a logic element . . . receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal” ’912 C1 Patent at 1:33–36 (Claim 1)⁷; *see also id.* at 2:27–30 (Claim 15), 3:53–56 (Claim 28), 4:47–52 (Claim 39). The parties dispute whether the address signals can include “packetized control and address information” that is decoded by logic into output signals.

Defendants take a two-step approach to reach their construction. First, they point to a previously agreed-to construction for “signal” from earlier litigation. *See* Dkt. No. 143 at 9. Then they *assume* the agreed-to construction includes “packetized” signals and claim “Netlist offers no construction that would exclude ‘packetized’ signals and identifies no disclaimer or lexicography that would justify such a construction.” *See id.* at 10.

Defendants’ argument concerns Netlist’s assertion, in 2009, of the ’912 Patent against Google in the United States District Court for the Northern District of California. *See* Joint Cl. Const. & Prehr’g Statement, Dkt. No. 143-8. During that litigation, the parties informed the court they agreed on the construction of “signal” as “a varying electrical impulse that conveys information from one point to another.” *See id.*, Ex. A. Netlist then filed an IDS with the Patent Office citing that Joint Statement. Information Disclosure Statement (June 8, 2010), Dkt. No. 143-9 at 5 (Cite No. 92). Defendants argue filing the IDS with the Office constitutes disclaimer. Dkt. No. 143

⁷ Referring to the *Inter Partes* Reexamination Certificate, Dkt. No. 129-1 at 43–50.

at 8 (citing *Golden Bridge Tech. Inc. v. Apple Inc.*, 758 F.3d 1362 (Fed. Cir. 2014)).

Netlist does not contest the IDS might be binding in certain circumstances, but argues no construction is necessary for the jury to understand the scope of “signal.” Dkt. No. 129 at 13. Regardless, says Netlist, “[p]acketized information transfer is not an electrical impulse, i.e., a high or a low which translates into a 1 or 0,” and “[t]he intrinsic record makes no reference to packetized transfer of information as being the same as signals.” Dkt. No. 150 at 5–6.

The Court agrees with Netlist. Rather than presenting the underlying dispute to the Court—here, whether “[row/column] address signal” includes “packetized” signals—Defendants point to a 2010 agreed construction that resolved a *different* dispute—“whether types of signals (e.g., command and control signals) needed to have ‘pins of a device dedicated for that specific information.’” Dkt. No. 143 at 9 (citing Netlist’s Open’g Cl. Constr. Br. (N.D. Cal.), Dkt. No. 143-12 at 9–13). Given the different disputes, that prior construction has no effect here.

If anything, based on the intrinsic record, Defendants must show why the ordinary meaning of “[row/column] address signal” *includes* packetized information. After all, the ’912 Patent does *not* refer to packetized information for addressing. Nor do traditional DIMMS include “multiplex control and address information demuxed from the data.” *See Wolfe Depo. Tr.*, Dkt. No. 129-23 at 28:8–16. Because Defendants fail to present any evidence to the contrary, the Court rejects that the scope of the disputed term includes “packetized” signals. Otherwise, the Court will give this term a “plain and ordinary meaning” construction.

- C. **“A memory module connectable to a computer system, the memory module comprising” (’912 Patent, preamble of all asserted claims);**
“A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including

a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising:” (’608 Patent, Claim 1)

Netlist’s Construction	Defs.’ Construction
Limiting preamble	Preamble not limiting

“In general, a preamble limits the invention if it recites essential structure or steps, or if it is ‘necessary to give life, meaning, and vitality’ to the claim. Conversely, a preamble is not limiting ‘where a patentee defines a structurally complete invention in the claim body and uses the preamble only to state a purpose or intended use for the invention.’” *Catalina Mktg, Inc. v. Coolsavings.com, Inc.*, 289 F.3d 801, 808 (Fed. Cir. 2002).

Here, the preambles do not “only state a purpose or intended use for the invention.” In fact, they state no purpose or intended use at all, instead requiring the memory module to be connectable to a computer system or operable to communication with a controller via a memory bus. As Micron’s expert explains, “DRAM chips are mounted on small printed-circuit boards . . . typically referred to as memory modules.” Stone Decl., Dkt. No. 129-6 ¶ 26. And “DRAM chips and the interfaces to the boards that include the DRAM chips, e.g., memory modules, are standardized so that memories from different vendors can be used in a variety of computers from different manufacturers.” *Id.* ¶ 27.

Based in part on this explanation from Dr. Stone, the Court agrees with Netlist. The important concepts of a “small printed-circuit board” and “standardized interfaces” to computers are absent from the body of the claims. Thus, not only do the claims fail to recite a structurally complete invention, “[a] skilled artisan would understand a ‘memory module’ is distinct from, and has essential structural requirements not necessarily found in, other modular computer accessories[, including] the structure necessary to connect to a memory controller.” Cl. Constr. Order (*Samsung*

l), Dkt. No. 129-7 at 28. Accordingly, the Court holds these are limiting preambles.

D. The Buffer Control Terms ('215 Patent, Claims 1, 21; '417 Patent, Claim 1)

Netlist's Construction	Def.' Constructions
These limitations do not require the first rank and second rank of memory integrated circuits to be on different forks.	“logic coupled to the buffer and configured to respond to the first memory command by providing first control signals to selectively electrically couple the input of the buffer to a first data signal line at the output of the data buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer, and disabling a second data signal line at the output of the buffer connected to the second memory integrated circuit” ('215 Patent, Claim 1)
	“wherein logic is further configured to respond to the second memory command by providing second control signals to selectively electrically couple the input of the buffer to a second data signal line at the output of the data buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer, and disabling a first data signal line at the output of the buffer connected to the first memory integrated circuit” ('215 Patent, Claim 1)
	“a data buffer coupled between the data signal lines in the N-bit wide memory bus and corresponding data pins of memory devices in each of the plurality of N-bit wide ranks, the buffer configurable to selectively electrically couple a single data signal line at the input of the buffer to a first signal line and second signal line at the output of the buffer to transfer N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide rank, wherein each signal line at the output of the buffer is connected to a different N-bit wide rank” ('417 Patent, Claims 1, 6, 11)

Despite that the claims do not facially require enabling one data buffer while disabling other data buffers, Defendants argue the claims should be so limited based on the specification and

the prosecution history. Regarding the specification, Defendants point to the differences between FIG. 2 and FIG. 4A and characterize the invention as using a “fork-in-the-road” architecture for enabling load isolation. Dkt. No. 143 at 14. Defendants then stress allegedly disavowing statements made by Netlist in IPR proceedings for related patents in which Netlist characterized the ability to “selectively electrically couple” the memory controller to the data buffer as a key contribution of the inventions. *Id.* at 15–17.

According to Netlist, however, there is no such fork-in-the-road requirement. For one, says Netlist, FIGS. 8A and 8B show an embodiment without such an arrangement, suggesting a “fork in the road” is not essential to the invention. Dkt. No. 129 at 18–21, 23–24; Dkt. No. 150 at 8–9.

The Court agrees with Netlist. Regarding the specification, the Court rejects Defendants’ assertion that “the only relevant disclosure . . . is directed to using a buffer to disable a data path for isolation.” Dkt. No. 143 at 14. The “Load Isolation” section composes only part of the disclosures. *See* ’215 Patent at 5:17–11:37. In fact, much of the disclosures repeat the subject matter of the ’912 Patent—the translation of address and control signals from the computer system to memory modules using a logic element. *See id.* at 13:50–17:40. The disclosures also include sections on “Back-to-Back Adjacent Read Commands,” *id.* at 12:37–13:49, “Serial-Presence-Detect Device[s],” *id.* at 17:41–30:3, and “Tied Data Strobe Signal Pins,” *id.* at 30:5–37:9. The claims at issue include some subject matter from these other sections.⁸ Thus, the Court is not convinced the

⁸ For example, Claims 1 and 21 of the ’215 Patent relate to memory commands that cause the memory module to receive or output data bursts, ’215 Patent at 37:51–62, which the patent discusses under the “Back-to-Back Adjacent Read Commands” section, *see generally id.* at 11:39–13:50. Similarly, the last two limitations of Claim 1 of the ’417 Patent concern CAS latency, ’417 Patent at 42:54–67, which the patent discloses under the “Serial-Presence-Detect Device” section, *id.* at 22:36–62.

claims are directed only to the “load isolation” disclosure as opposed to other aspects of the patents.

Regarding Netlist’s IPR statements, they specifically concerned the phrase “selectively electrically coupled” in the claims at issue, which Netlist clearly tied to the “Load Isolation” part of the disclosure. For example, Netlist had an entire section of its brief dedicated to explaining the importance of “load isolation.” *See* App.’s Br., Dkt. No. 143-23 at 10–14. It explained:

Adding the configurability to **selectively electrically couple** a device data line to a common data line was a key contribution of the inventions. When a memory device’s data line is permanently electrically connected to the common data line, as is the case for both memory devices in the conventional memory module of FIG. 2, the computer system is always exposed to the electrical load of each such memory device on a module. But when a switch or other mechanism is used to **selectively electrically couple** the data lines, such as shown in FIG. 3A, the electrical load of the memory devices can be disconnected from the computer system by the switch. When the switch is not actuated, there is no electrical connection between the device data line and common data line, which means there is no electrical connection between the computer system (connected to the common data line) and the memory device (connected to the device data line). When that happens, the electrical load of the memory module is reduced to the load of the circuit 40 (*i.e.*, the switches and other components of the circuit, but not the memory devices).

Solving the problem of increased loading due to additional memory devices was essential to overcoming the shortcomings of prior art memory modules.

Id. at 41–42 (emphasis added).

Here, however, the claims at issue use different language than “selectively electrically coupled” and, as discussed *supra*, are not so clearly tied to this “load isolation” concept to justify finding clear and unmistakable disclaimer. Accordingly, the Court rejects any fork-in-the-road requirement for these claims.

E. “logic” (’215 Patent, Claim 1; ’417 Patent, Claim 1)

Netlist’s Construction	Micron’s Construction
Plain and ordinary meaning, not subject to § 112 ¶ 6.	Subject to § 112 ¶ 6, but there is no disclosure of adequate structure or algorithm for the functions of: <u>For Claim 1 of the ’417 Patent</u> “output[ing] data buffer control signals in response to the read or write memory command” <u>For Claim 1 of the ’215 Patent:</u> “(i) respond[ing] to the first memory command by providing first control signals to the buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer; and (ii) further respond[ing] to the second memory command by providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer”

Claim 1 of the ’417 Patent recites “[a] memory module operable in a computer system” comprising:

- a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system; [and]
- logic coupled to the printed circuit board and configurable to receive a set of input address and control signals associated with a read or write memory command via the address and control signal lines and to output a set of registered address and control signals in response to the set of input address and control signal

’417 Patent at 42:7–22. The claims further require the input address and control signals to include registered chip-select signals that are either “active” or “non-active.” *Id.* at 42:22–40. Claim 1 of the ’215 Patent includes a similar “logic” limitation, but requires the “logic” to be connected to a buffer that itself is coupled between a memory integrated circuit and a memory bus. *See* ’215

Patent at 37:47–62.

Pointing to *Williamson and Egenera, Inc. v. Cisco Sys.*, 972 F.3d 1367 (Fed. Cir. 2020), Micron argues “the ‘logic’ limitations are claimed in a purely functional manner and fail to recite sufficient structure for performing the claimed functionality.” Dkt. No. 143 at 24–26. In *Egenera*, the court considered whether the phrase “logic to modify said received messages to transmit said modified messages to the external communication network and to the external storage network” was subject to § 112 ¶ 6. *Egenera* argued the recited “logic to modify” was structural because it was part of a “control node,” but the court rejected that argument. *See Egenera*, 972 F.3d at 1374 (“Mere inclusion of a limitation within a structure does not automatically render the limitation itself sufficiently structural. . . . [T]he question is not whether ‘logic’ is utterly devoid of structure but whether the claim term recites sufficient structure to perform the claimed functions.”). *Egenera* also argued the claim language defined the “inputs, outputs, connections, and operation” of the logic component, thus providing sufficiently definite structure, but the court also rejected that argument. *Id.* (“[T]he claims and specification provide no structural limitation to the ‘inputs, outputs, connections, and operation’ of the claimed ‘logic to modify.’”).

Here, the “logic” is distinguishable from *Egenera*’s “logic to modify.” In *Egenera*, the appellant argued that “logic” denoted “software, firmware, circuitry, or some combination thereof.” The district court called that definition “so broad and formless as to be a generic black box for performing the recited computer-implemented functions.” *Egenera*, 972 F.3d at 1374 (quoting the district court). As used in these claims, however, “logic” clearly connotes *physical* structure rather than software, as the claims require the “logic” to be coupled to either a printed circuit board (in the ’417 Patent) or a buffer (in the ’215 Patent). Thus, “logic” here is not so “broad and formless” as the “logic to modify” of *Egenera*.

Moreover, the limitation requires connection of address and control signal lines, the receipt of address and control signals over those lines, and the output of chip-select signals based on the input signals. This is consistent with the specifications' disclosure of PLDs, ASICs, FPGAs, and CPLDs as "logic elements." *See, e.g.*, '417 Patent at 7:17–31 (noting that, "[i]n certain embodiments, the circuit [40] comprises a logic element selected from a group consisting of: a programmable-logic device (PLD), an application-specific integrated circuit (ASIC), a field-programmable gate array (FPGA), a custom-designed semiconductor device, and a complex programmable-logic device (CPLD)"). In light of that disclosure, and because a skilled artisan would have "been familiar with the structure and operation of circuitry used to access and control computer memories," Stone Decl., Dkt. No. 144-3 ¶ 21, the Court finds this limitation recites sufficiently definite structure to avoid invoking § 112 ¶ 6. Accordingly, this term will be given a "plain and ordinary meaning" construction.

F. “circuitry” (’417 Patent, Claims 1, 6, 11)

Netlist’s Construction	Micron’s Construction
Plain and ordinary meaning, not subject to § 112 ¶ 6	Subject to §112, ¶ 6, but there is no disclosure of adequate structure or algorithm for the function of “transfer[ring] the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signal”

Claim 1 recites:

circuitry coupled between the data signal lines in the N-bit wide memory bus and corresponding data pins of memory devices in each of the plurality of N-bit wide ranks, the circuitry being configurable to transfer the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signals and in accordance with an overall CAS latency of the memory module[.]

’417 Patent at 42:54–62. Claims 6 and 11 further limit the “circuitry” to include “logic pipelines” and “data paths,” respectively. *See id.* at 43:19–22 (Claim 6), 44:10–14 (Claim 11). Micron contends “circuitry” is governed by 35 U.S.C. § 112 ¶ 6 but is indefinite for lack of corresponding structure. Dkt. No. 143 at 28–30.

“[W]hen the structure-connoting term ‘circuit’ is coupled with a description of the circuit’s operation, sufficient structural meaning generally will be conveyed to persons of ordinary skill in the art, and § 112 ¶ 6 presumptively will not apply.” *Linear Tech. Corp. v. Impala Linear Corp.*, 379 F.3d 1311, 1320 (Fed. Cir. 2004). In *Linear Tech*, the court held the claims’ recitation of the circuit’s objective was sufficient to avoid invoking § 112 ¶ 6. *Id.* (noting “[t]he contextual language describes the objective of the ‘circuit,’ [which is] ‘monitoring a signal from the output terminal,’ and the desired output of the ‘circuit,’ [which is] ‘generating a first feedback signal’”).

Here, too, the claims at issue provide the objective and desired output of the circuit.

Specifically, Claim 1 recites “transfer[ring] the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signals and in accordance with an overall CAS latency of the memory module.” ’417 Patent at 42:57–62. Moreover, the claims recite registering data transfers through the circuitry “for an amount of time delay *such that* the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices.” *Id.* at 42:64–67 (emphasis added). Given Micron’s characterization of a skilled artisan as one “knowledgeable about the design and operation of computer memories, most particularly DRAM and SDRAM devices that were compliant with various standards of the day, and how they interact with other components of a computer system, such as memory controllers,” Stone Decl., Dkt. No. 144-3 ¶ 21, the Court holds § 112 ¶ 6 does not apply and will give this term a “plain and ordinary meaning” construction.

G. “the at least one of the circuit components” (’215 Patent, Claim 15)

Netlist’s Construction	Micron’s Construction
Plain and ordinary meaning	Indefinite

This dispute relates to both Claim 14 and Claim 15 of the ’215 Patent. The former requires the buffer of Claim 1 to include “circuit components configurable to provide a first data path or a second data path depending on whether the first rank or the second rank is selected to communicate data with the memory controller.” ’215 Patent at 39:24–28. Claim 15, which depends from Claim 14, then recites “the at least one of the circuit components is configured to provide the first data path in response to the first control signals, and is configured to provide the second data path in response to the second control signals.” *Id.* at 39:29–33. Micron argues this phrase from Claim 15 has at least two possible and equally plausible meanings: (1) “wherein [[the]] at least

one of the circuit components is configured to provide . . .”; or (2) “~~the at least one of the circuit components are configured to provide . . .~~” Dkt. No. 143 at 24. As such, Micron says, this phrase is indefinite. *Id.*

The Court disagrees. For one, there is no material difference in scope between Micron’s two proffered meanings. In other words, regardless of whether (1) “at least one of the circuit components” or (2) “the circuit components” are configured as required by the claims, those two phrases effectively mean the same thing. In addition, the only substantive limitation added by Claim 15 is the requirement that the provision of the data paths be “in response” to control signals. Thus, construing the phrase as “the circuit components” reflects how a skilled artisan would understand the term because it best aligns the language of Claim 15 with that of Claim 14. The Court therefore adopts that construction.

H. “burst of data strobe signals” (’215 Patent, Claims 12, 13, 28, 29)

Netlist’s Construction	Micron’s Construction
Plain and ordinary meaning.	Indefinite.

Claim 1 of the ’215 Patent is directed to

[a] memory module operable in a computer system to communicate data with a memory controller of the computer system via a memory bus in response to memory commands received from the memory controller, the memory commands including a first memory command and a subsequent second memory command, the first memory command to cause the memory module to receive or output a first data burst and the second memory command to cause the memory module to receive or output a second data burst . . .

’215 Patent at 37:12–21. Claim 12, which depends from Claim 1, specifies:

the first memory command is a first read command and the second memory command is a second read command, wherein the first read command and the second read command are back to back adjacent

read commands, and wherein the memory module outputs the first data burst together with **a first burst of data strobe signals** in response to the first read command, wherein [the] memory module outputs the second data burst together with **a second burst of data strobe signals** in response to the second read command, wherein the second data burst follows the first data burst on the memory bus, and wherein the buffer is configured to prevent the **first burst of data strobe signals** and the **second burst of data strobe signals** from colliding with each other.

Id. at 39:1–14 (emphasis added).

Micron challenges this term as indefinite because the bursts could come from either “combined” or “non-combined” strobes. Dkt. No. 143 at 23. With “combined” strobes, two different memory devices have their strobe pins tied together. Stone Decl., Dkt. No. 144-3 ¶ 47. “Non-combined” strobes come from a single memory device. *Id.* ¶ 48. Netlist argues the term is broad enough to include both sources. Dkt. No. 129 at 26.

Micron focuses on the wrong question. Specifically, Micron looks to what *originates* the required “burst of data strobe signals,” rather than the “bursts” themselves. The claims only require “the memory module [to] output[] the first data burst together with a first burst of data strobe signals.” They say nothing about the underlying structural configuration that creates the “bursts.” Thus, Micron at most shows the claims are indifferent as to the configuration of the *source* of the “bursts,” and not what a “burst” is or is not. As such, it has not carried its burden on indefiniteness, and the Court will give this term a “plain and ordinary meaning” construction.

I. “operable in a computer system to communicate data” (’215 Patent, Claim 1; ’417 Patent, Claim 1)

Netlist’s Construction	Defs.’ Construction
Plain and ordinary meaning	“configured in a computer system to communicate data”

Defendants question whether this term “requires mere capability (including after modification) or whether it requires structure that presently is configured to perform the recited function.” Dkt. No. 143 at 20. They point to *TQ Delta, LLC v. CommScope Holding Co.*, No. 2:21-CV-309-JRG, 2022 WL 2071073 (E.D. Tex. June 8, 2022), in which the Court explained “‘operable to’ should be construed to refer to being configured to operate in the recited manner.” *Id.* Netlist, however, asserts “[t]hat concern is not present here” because a skilled artisan “would understand that memory modules are designed to communicate data with a memory controller . . . without modification.” Dkt. No. 129 at 27–28.

Based on the briefing, the parties apparently agree with the well-established principle “that a device capable of being modified to operate in an infringing manner is not sufficient, by itself, to support a finding of infringement.” *See Telemac Cellular Corp. v. Topp Telecom, Inc.*, 247 F.3d 1316, 1330 (Fed. Cir. 2001). In other words, if the claims recite some structure “operable” to perform a task, an accused device must be *presently* “operable” to perform that task to infringe. Given the parties’ apparent agreement on that point, the Court will give this term a “plain and ordinary meaning” construction.

J. “data buffer control signals” (’417 Patent, Claims 1, 3, 11)

Netlist’s Construction	Defs.’ Construction
Plain and ordinary meaning	“a signal sent to a buffer to selectively electrically couple the data signal line at the input of the buffer to a first signal line and a second signal line at the output of the buffer wherein each of the first signal line and the second signal line is connected to a different rank”

This term first appears near the end of the “logic” limitation of Claim 1. Specifically, the claim requires logic “configurable to output data buffer control signals in response to the read or write memory command.” ’417 Patent at 42:38–49.

Defendants base their construction on the limited disclosure of “control signals” in the specification. Dkt. No. 143 at 19 (noting the disputed term does not appear in the original specification). They suggest “[a]ny other construction ‘would likely render the claims invalid for lack of written description.’” *Id.* (quoting *Ruckus Wireless, Inc. v. Innovative Wireless Sols., LLC*, 824 F.3d 999, 1004 (Fed. Cir. 2016)).

The Court disagrees for two reasons. First, Defendants’ construction, which uses the phrase “selectively electrically couple,” introduces the “fork-in-the-road” approach into the claims. *See* Dkt. No. 143 at 19 (arguing “Netlist cannot escape its prosecution statements that describe the invention as requiring a fork-in-the-road implementation”). The Court has already rejected that position. *See* Part IV.D. *supra*. Second, the Court is not persuaded mixing the claim-construction and written-description inquiries is proper on this record. In *Ruckus Wireless*, the Federal Circuit’s decision hinged on first applying all the other rules of claim construction and still finding the term “ambiguous.” *See Ruckus Wireless, Inc.*, 824 F.3d at 1004 (“If, after applying all other available tools of claim construction, a claim is ambiguous, it should be construed to preserve its validity.”). Here, however, Defendants make no attempt to show “data buffer control signals” is ambiguous. *See* Dkt. No. 143 at 19. The Court will therefore give this term a “plain and ordinary meaning” construction.

K. **“overall CAS latency [of the memory module]”** (’417 Patent, Claim 1; ’215 Patent, Claims 3, 4, 24, 25)

“actual operational CAS latency of each of the memory devices” (’417 Patent, Claim 1)

“actual operational CAS latency of each of the plurality the memory integrated circuits” (’215 Patent, Claims 3, 4)

“actual operational CAS latency of the memory integrated circuits” (’215 Patent, Claims 24, 25)

Netlist’s Construction	Micron’s Construction
Plain and ordinary meaning	“overall CAS latency”: “The delay between: (1) the time when a read command is executed by the memory module, and (2) the time when the first piece of data is made available at an output of the memory module.” “actual operational CAS latency of each of the memory devices”: “the delay between: (1) the time when a read command is executed by each of the plurality of memory integrated circuits, and (2) the time when the first piece of data is made available at an output of each of the plurality of memory integrated circuits” “actual operational CAS latency of each of the [plurality of] memory devices”: “the delay between: (1) the time when a read command is executed by the memory integrated circuits, and (2) the time when the first piece of data is made available at an output of the memory integrated circuits”

“CAS latency” means “column address strobe latency.” As used in the claims, “overall CAS latency” refers to the “CAS latency” of a memory module, and “actual operational CAS latency” refers to the “CAS latency” of a memory device on the module. For example, Claim 1 of the ’417 Patent requires:

circuitry . . . configurable to transfer the burst of N-bit wide data signals between the N-bit wide memory bus and the memory

devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signals and in accordance with an **overall CAS latency** of the memory module;

wherein data transfers through the circuitry are registered for an amount of time delay such that the **overall CAS latency** of the memory module is greater than an **actual operational CAS latency** of each of the memory devices.

'417 Patent at 42:54–67 (emphasis added). *See also* '215 Patent at 38:1–10 (reciting, in Claims 3 and 4, “overall CAS latency” and “actual operational CAS latency of each of [a] plurality of memory devices”); *id.* at 40:47–55 (reciting, in Claims 24 and 25, “overall CAS latency” and “actual operational CAS latency of . . . memory integrated circuits”).

The parties generally agree “CAS latency” is a time between a command being executed and the presentation of data somewhere within the system, depending on the context of the surrounding language. For example, the parties agree the “overall CAS latency” of a memory module for a read command is the delay between (1) the time when the read command is executed by the memory module, and (2) the time when data is made available.⁹

The dispute concerns whether “CAS latency” refers *only* to “read” commands (Micron’s position), or also to “write” commands (Netlist’s position). According to Micron, the industry understood “CAS latency” at the relevant time as synonymous with “read latency.” Dkt. No. 143 at 22. It accuses Netlist of trying to improperly broaden the meaning of “CAS latency.” *Id.* at 23.

Netlist disagrees for three reasons. First, Netlist points to the claims, which it says support a construction that includes both “read” and “write” commands. Dkt. No. 129 at 29 (noting Claim 1 of the '417 Patent is expressly directed to both read and write commands and concerns “data

⁹ Netlist’s agreement is not explicit, but it does not challenge the structure of Micron’s proposed construction—only that it is limited to “read” commands. *See* Dkt. No. 129 at 28–29.

transfers through the circuitry”). *Id.* Second, Netlist alleges Micron’s construction would improperly exclude disclosed embodiments. *Id.* (citing ’215 Patent at 20:22–47). Last, Micron’s construction narrows the scope of the term’s ordinary meaning without showing clear disavowal. *Id.* at 30.

The disclosure addresses “CAS latency” in only one paragraph:

The circuit 40 comprises the SPD device 240 which reports the CAS latency (CL) to the memory controller of the computer system. The SPD device 240 reports a CL which has one more cycle than does the actual operational CL of the memory array. Data transfers between the memory controller and the memory module are registered for one additional clock cycle by the circuit 40. The additional clock cycle is added to the transfer time budget with an incremental overall CAS latency. This extra cycle of time advantageously provides sufficient time budget to add a buffer which electrically isolates the ranks of memory devices 30 from the memory controller 20. The buffer comprises combinatorial logic, registers, and logic pipelines. The buffer adds a one-clock cycle time delay, which is equivalent to a registered DIMM, to accomplish the address decoding. The one-cycle time delay provides sufficient time for read and write data transfers to provide the functions of the data path multiplexer/demultiplexer. Thus, for example, a DDR2 400-MHz memory system as described herein has an overall CAS latency of four, and uses memory devices with a CAS latency of three.

’215 Patent at 20:22–47 (cleaned up for easier reading).

Based on this paragraph, the Court agrees with Netlist. The disclosure explains the one-cycle time delay “provides sufficient time for *read and write data transfers* to provide the functions of the data path multiplexer/demultiplexer.” ’215 Patent at 20:39–42. Moreover, the disclosure refers to data transfers *between* the memory controller and the memory module” rather than in only one direction or the other. *Id.* at 20:27–29. Similarly, the claim limitations in which these terms appear refer to “caus[ing] the memory module to *receive or output*” a data burst, *id.* at 37:16–22 (emphasis added), and “data transfers *through* the circuitry,” ’417 Patent at 42:63 (emphasis added).

Regarding the extrinsic evidence, Micron’s expert agrees “CAS latency can relate to both read and write data transfers.” Stone Depo. Tr., Dkt. No. 129-5 at 76:16–18. And while Micron suggests “CAS latency” *usually* refers to “read latency,” it also recognizes these “are not well-known terms of art.” *See* Dkt. No. 143 at 22. Moreover, the parties agree “write latency” is closely related to “read latency.” Dkt. No. 129 at 30 (citing JESD79-2, Dkt. No. 129-2 at 24); Dkt. No. 143 at 23 (“While CAS latency was only associated with Read Latency (RL) at the relevant time, Write Latency (WL) was a concept that was defined *in terms of* Read Latency.”).

Based on the totality of the evidence, a skilled artisan would understand “CAS latency” includes both “read latency” and “write latency,” depending on the context. The Court therefore rejects Micron’s position and construes:

- **“overall CAS latency”** of a memory module as “the delay between: (1) the time when a command is executed by the memory module, and (2) the time when data is made available to or from the memory module”;
 - **“actual operational CAS latency”** of a memory device as “the delay between: (1) the time when a command is executed by the memory device, and (2) the time when data is made available to or from the memory device”; and
 - **“actual operational CAS latency”** of a memory integrated circuit as “the delay between: (1) the time when a command is executed by the memory integrated circuit, and (2) the time when data is made available to or from the memory integrated circuit.”
- L. “wherein data transfers through the circuitry are registered for an amount of time delay such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices” (’417 Patent, Claim 1)**

Netlist’s Construction	Micron’s Construction
Plain and ordinary meaning.	Indefinite

Micron contends this phrase is indefinite under either Netlist’s or Micron’s proposed

construction for “CAS latency.” Dkt. No. 143 at 21. Under Micron’s construction, which limits a “CAS latency” to a “read latency,” “[i]t is nonsensical to ‘register’ data *to be written* ‘for an amount of time delay’” that relates to a read latency. *Id.* And under Netlist’s “apparent” construction, there would be no time delay for “overall CAS latency,” which could then never be greater than the “actual operation CAS latency of the memory device.” *Id.*

According to Netlist, the “conflict” Micron identifies with respect to its construction for “CAS latency” further supports the notion that term is not limited to a “read” latency. Dkt. No. 150 at 10. Netlist also notes Micron’s reliance on Netlist’s “proposed construction” is from another proceeding rather than the “plain and ordinary meaning” construction it asserts now. *Id.*

The Court agrees with Netlist. As noted *supra*, “CAS latency” is not limited to only a “read latency,” see Part IV.K., which negates Micron’s first argument. Micron’s second argument—that registering data being transferred through the circuitry could never make a zero delay greater than anything—relates to infringement rather than indefiniteness. While it may be true that, under Netlist’s interpretation of “CAS latency,” the recited limitation can never be met by an accused device, that does not mean the term is indefinite—only that infringement is impossible. The Court therefore holds Micron has not carried its burden of showing this term is indefinite.

V. CONCLUSION

The Disputed Terms	The Court’s Construction
The “Rank” Terms (’912 Patent, ’417 Patent, ’215 Patent)	A “rank” of memory is “a ‘bank’ of one or more devices on a memory module that operate in response to a given signal”
“signal” / “row [/column] address signal” (’912 Patent, all claims)	Plain and ordinary meaning

“A memory module connectable to a computer system, the memory module comprising” (’912, preamble to all asserted claims) “A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising: (’608 Patent, Claim 1)	The preambles are limiting.
The Data Buffer Control Terms (’215 Patent, Claims 1, 21; ’417 Patent, Claim 1)	The claims do not require a “fork-in-the-road” approach.
“logic” (’417 Patent, Claim 1; ’215 Patent, Claim 1)	Plain and ordinary meaning
“circuitry” (’417 Patent, Claims 1, 6, 11)	Plain and ordinary meaning
“the at least one of the circuit components” (’215 Patent, Claim 15)	“the circuit components”
“burst of data strobe signals” (’215 Patent, Claims 12, 13, 28, 29)	Plain and ordinary meaning
“operable in a computer system to communicate data” (’215 Patent, Claim 1; ’417 Patent, Claim 1)	Plain and ordinary meaning
“data buffer control signals” (’417 Patent, Claims 1, 3, 11)	Plain and ordinary meaning
“overall CAS latency” of a memory module (’417 Patent, Claim 1; ’215 Patent, Claims 3, 4, 24, 25)	“the delay between (1) the time when a command is executed by the memory module, and (2) the time when data is made available to or from the memory module”
“actual operational CAS latency” of a memory device (’417 Patent, Claim 1)	“the delay between: (1) the time when a command is executed by the memory device, and (2) the time when data is made available to or from the memory device”

“actual operational CAS latency” of a memory integrated circuit (’215 Patent, Claims 3, 4, 24, 25)	“the delay between: (1) the time when a command is executed by the memory integrated circuit, and (2) the time when data is made available to or from the memory integrated circuit”
“wherein data transfers through the circuitry are registered for an amount of time delay such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices” (’417 Patent, Claim 1)	Plain and ordinary meaning

The Court **ORDERS** each party not to refer, directly or indirectly, to its own or any other party’s claim-construction positions in the presence of the jury. Likewise, the Court **ORDERS** the parties to refrain from mentioning any part of this opinion, other than the actual positions adopted by the Court, in the presence of the jury. No party may take a position before the jury that contradicts the Court’s reasoning in this opinion. Any reference to claim construction proceedings is limited to informing the jury of the positions adopted by the Court.

So ORDERED and SIGNED this 21st day of November, 2023.



RODNEY GILSTRAP
UNITED STATES DISTRICT JUDGE

Exhibit C

UNITED STATES DISTRICT COURT
EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

NETLIST, INC.

Plaintiff,

v.

SAMSUNG ELECTRONICS CO., LTD, et al.

Defendants.

Civil Case No. 2:22cv-00293-JRG
(Lead Case)

JURY TRIAL DEMANDED

NETLIST, INC.

Plaintiff,

v.

MICRON TECHNOLOGY TEXAS, LLC, et al.

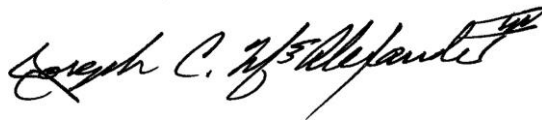
Defendants.

Civil Case No. 2:22cv-00294-JRG
(Member Case)

JURY TRIAL DEMANDED

INITIAL EXPERT REPORT OF JOSEPH C. McALEXANDER III

Dated: November 20, 2023



Joseph C. McAlexander III

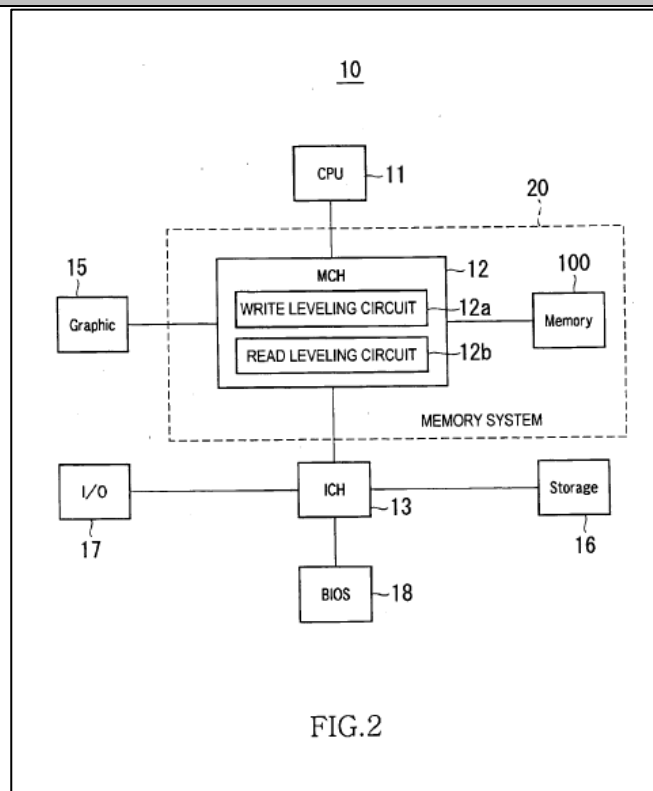
EXHIBIT C-3
INITIAL EXPERT REPORT OF JOSEPH C. M^CALEXANDER III
(U.S. PATENT NO. 10,268,608)

It is my opinion that U.S. Patent App. Pub. No. 2010/0312956 to Hiraishi (“Hiraishi”), published on December 9, 2010, alone and/or in view of the knowledge of a POSITA and/or in combination with U.S. Patent App. Pub. No. 2007/0008791 to Butt (“Butt”), published on January 11, 2007, and/or in combination with U.S. Patent Publication No. 8,020,022 (“Tokuhiro”), published on September 13, 2011, and/or in combination with U.S. Patent App. Pub. No. 2006/0277355 to Ellsberry (“Ellsberry”), published on December 7, 2006, anticipates and/or renders obvious all features of the asserted claims of the ’608 patent.

Specifically:

- Hiraishi anticipates at least claims 1-4 of the ’608 patent
- Hiraishi in view of the knowledge of a POSITA renders obvious at least claims 1-5 of the ’608 patent.
- Hiraishi in view of Butt and/or Tokuhiro and/or Ellsberry renders obvious at least claims 1-5 of the ’608 patent.

'608 patent	35 U.S.C. §§ 102, 103 Analysis
1[pre] A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising:	Based on Netlist's apparent view of the scope of the '608 patent claims, as articulated in its Infringement Contentions and which I disagree with, and to the extent the preamble of claim 1 is found to be limiting, it is my opinion that Hiraishi alone or in view of the knowledge of a person of ordinary skill in the art ("POSITA") discloses element 1[pre]. For example, Hiraishi discloses a memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines. The memory module 100 of Fig. 1 is operable to communicate with a memory controller MCH 12 in Figures 2-3 via a memory bus (e.g., line 23 in Figure 3). The memory bus includes control/address signal lines (e.g., command/address/control line L3) and a plurality of sets of data/strobe signal lines (e.g., data line L0). "FIG. 1 is a schematic diagram of a configuration of a memory module 100 according to an embodiment of the present invention; FIG. 2 is a block diagram of a configuration of an information processing system 10 including the memory module 100 according to the present embodiment;" Hiraishi at [0013-0014]. FIG. 1 Hiraishi at Fig. 1.



Hiraishi at Fig. 2.

“The memory module 100 shown in FIG. 1 and a graphic controller 15 are connected to the MCH 12. As shown in FIG. 2, the memory module 100 and the MCH 12 constitute a memory system 20, where the MCH 12 has a controller function for the memory module 100. That is, the MCH 12 functions as a memory controller for the memory module 100.” Hiraishi at [0065].

“As shown in FIG. 1, the memory module 100 according to the present embodiment includes a module substrate 110, a plurality of memory chips 200 mounted on the module substrate 110, a plurality of data register buffers 300, and a command/address/control register buffer 400. In the present embodiment, the memory module 100 includes thirty-six memory chips 200. When it is necessary to specify each of the memory chips, the memory chips are respectively represented by memory chips 200-0 to 200-35. Furthermore, in the present embodiment, the memory module 100 includes nine data register buffers 300. When it is necessary to specify each of the data register buffers, the data register buffers are respectively represented by data register buffers 300-0 to 300-8. On the other hand, the command/address/control register buffer 400 is provided as a single unit. However, it is not essential to

'608 patent	35 U.S.C. §§ 102, 103 Analysis
	set the number of units of the command/address/control register buffer 400 to one, but two or more units of the command/address/control register buffer 400 can be mounted without any limitation.” Hiraishi at [0045-0046]. “The module substrate 110 is a printed circuit board that includes a multilayer wiring. The planar shape of the module substrate 110 is substantially rectangle, as shown in FIG. 1, with a long side in the X direction and a short side in the Y direction. On one side of the module substrate 110 along the X direction, which is the long side, a plurality of data connectors 120 and a plurality of command/address/control connectors 130 are provided. The data connectors 120 and the command/address/control connectors 130 are terminals for making an electrical connection with a memory controller via a memory slot, which will be described later.” Hiraishi at [0047]. “The command/address/control connectors 130 are connectors for supplying a command signal, an address signal, a control signal, and a clock signal to be supplied to the command/address/control register buffer 400. As shown in FIG. 1, the command/address/control connectors 130 are arranged in an area 110 c that is located between the area 110 a and the area 110 b.” Hiraishi at [0049]. “An operation of the memory chip 200 is controlled based on the command signal, the address signal, the control signal, and the clock signal supplied from the command/address/control register buffer 400. Details on the memory chip 200 will be described later. A single data register buffer 300 is allocated for every four memory chips 200, as described above, so that nine data register buffers 300 are arranged along the X direction, which is the long side. The data register buffer 300 is a chip for buffering write data that is transferred via a data line L0 and outputting the write data to either one of the data lines L1 and L2, and at the same time, buffering read data that is transferred via either one of the data lines L1 and L2 and outputting the read data to the data line L0. The data line L0 is also formed inside the module substrate 110.” Hiraishi at [0054-0055] “The command/address/control register buffer 400 receives the command signal, the address signal, the control signal, and the clock signal (in some cases, collectively referred to as a command/address/control signal and the like) that are supplied from the command/address/control connectors 130 through an input terminal 401, buffers the signals, and supplies the signals to the memory chips 200. At the same time, the command/address/control register buffer 400 generates a control signal. The

command/address/control signal to be supplied to the memory chips 200 are output through an output terminal 402, and the control signal to be supplied to the data register buffers 300 are output through an output terminal 403.” Hiraishi at [0060].

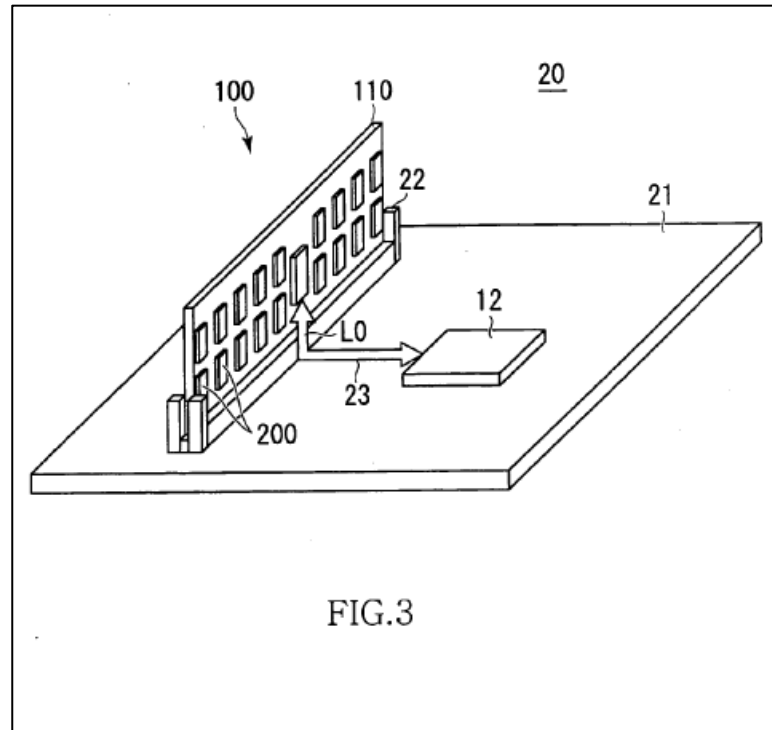
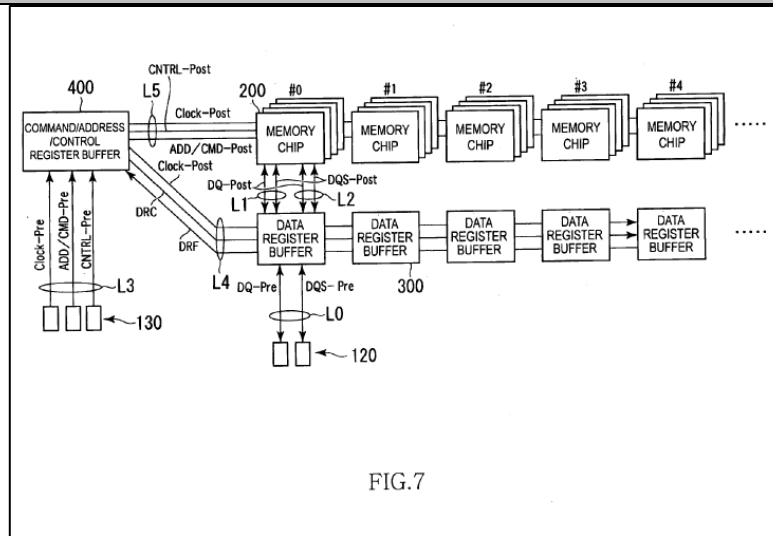


FIG.3

Hiraishi at Fig. 3.

“On a signal path between the memory controller 12 and the memory chips 200, there exist a line 23 formed on the motherboard 21 and the data line L0 and the command/address/control line L3 formed on the module substrate 110. However, as described above referring to FIG. 1, in the memory module 100 according to the present embodiment, because the data register buffer 300 is connected to the data line L0, the memory controller 12 cannot experience the load capacity of the memory chips 200 that exist on the signal path beyond the data register buffer 300. Similarly, because the command/address/control register buffer 400 is connected to the command/address/control line L3, the memory controller 12 cannot experience the load capacity of the memory chips 200 that exist on the signal path beyond the command/address/control register buffer 400. Therefore, the load capacity of the signal path that connects the memory controller 12 and the memory module 100 is reduced, making it possible to ensure an excellent signal quality even with a high data transfer rate.” Hiraishi at [0069].



Hiraishi at Fig. 7.

“FIG. 7 is a connection diagram of the memory module 100 according to the present embodiment. As shown in FIG. 7, in the present embodiment, the data register buffer 300 intervenes between the data connectors. 120 and the memory chips 200. The data connectors 120 and the data register buffer 300 are connected to each other with the data line L0, and the data register buffer 300 and the memory chips 200 are connected to each other with the data line L1 or L2. In FIG. 7, a plurality of data transferred through the data line L0 is represented by data DQ-Pre, and a plurality of data transferred through the data lines L1 and L2 is represented by data DQ-Post. Similarly, a data strobe signal transferred through the data line L0 is represented by a data strobe signal DQS-Pre, and a data strobe signal transferred through the data line L1 or L2 is represented by a data strobe signal DQS-Post.” Hiraishi at [0102-0103].

“As shown in FIG. 7, the command/address/control connectors 130 and the command/address/control register buffer 400 are connected to each other with the command/address/control line L3, the command/address/control register buffer 400 and the data register buffer 300 are connected to each other with a control line L4, and the command/address/control register buffer 400 and the memory chips 200 are connected to each other with a command/address/control line L5. In FIG. 7, a command/address/control signal transferred through the command/address/control line L3 is represented by a command/address signal ADD/CMD-Pre, and a command/address signal transferred through the command/address/control line L5 is represented by a command/address signal ADD/CMD-Post. Similarly,

'608 patent	35 U.S.C. §§ 102, 103 Analysis
	a control signal transferred through the command/address/control line L3 is represented by a control signal CNTRL-Pre, and a control signal transferred through the command/address/control line L5 is represented by a control signal CNTRL-Post.” Hiraishi at [0107].
1[a] a module board having edge connections for coupling to respective signal lines in the memory bus;	Based on Netlist’s apparent view of the scope of the ’608 patent claims, as articulated in its Infringement Contentions and which I disagree with, it is my opinion that Hiraishi alone or in view of the knowledge of a POSITA discloses element 1[a]. For example, Hiraishi discloses a module board (e.g., module substrate 110) having edge connections (e.g., command/address/control connectors 130 and data connectors 120) for coupling to respective signal lines (e.g., line 23) in the memory bus. “In one embodiment, there is provided a memory module comprising: a module substrate including a plurality of data connectors; a plurality of memory chips mounted on the module substrate, each of the memory chips including at least one data terminal; and a plurality of data register buffers mounted on the module substrate, each of the data register buffers being assigned to at least two memory chips, wherein each of the data register buffers includes M first input/output terminals each being connected to an associated one of the data connectors via a first data line formed on the module substrate, where M is a positive integer equal to or larger than 1, and N second input/output terminals each being connected to the data terminal of corresponding memory chips via a second data line formed on the module substrate, where N is a positive integer equal to or larger than 2M, so that number of the second data lines is N/M times number of the first data lines.” Hiraishi at [0010]. “FIG. 3 is a perspective view of a part of a configuration of a motherboard 21 on which the memory system 20 is mounted;

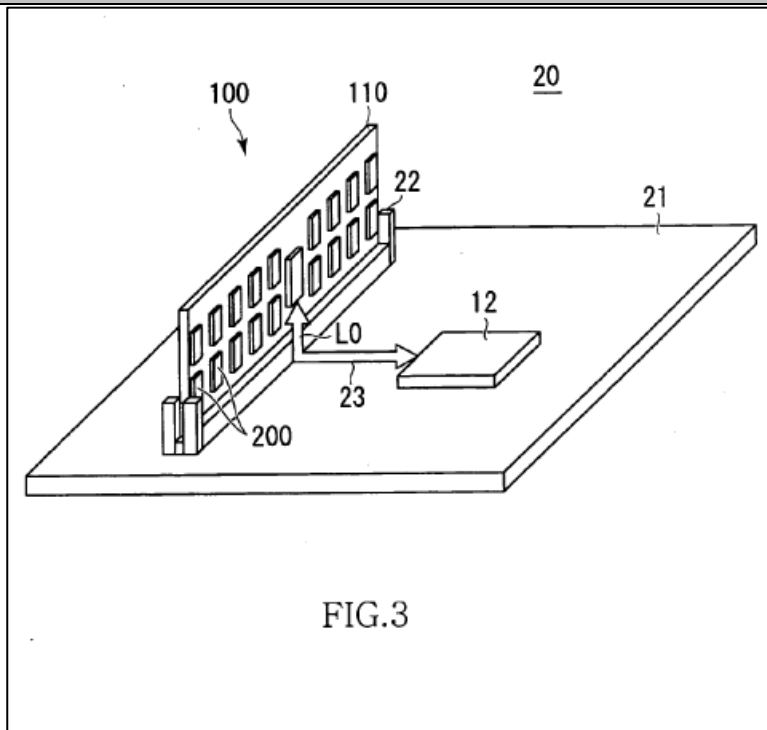


FIG. 3

Hiraishi at Fig. 3.

“As shown in FIG. 1, the memory module **100** according to the present embodiment includes a module substrate **110**, a plurality of memory chips **200** mounted on the module substrate **110**, a plurality of data register buffers **300**, and a command/address/control register buffer **400**.” Hiraishi at [0045].

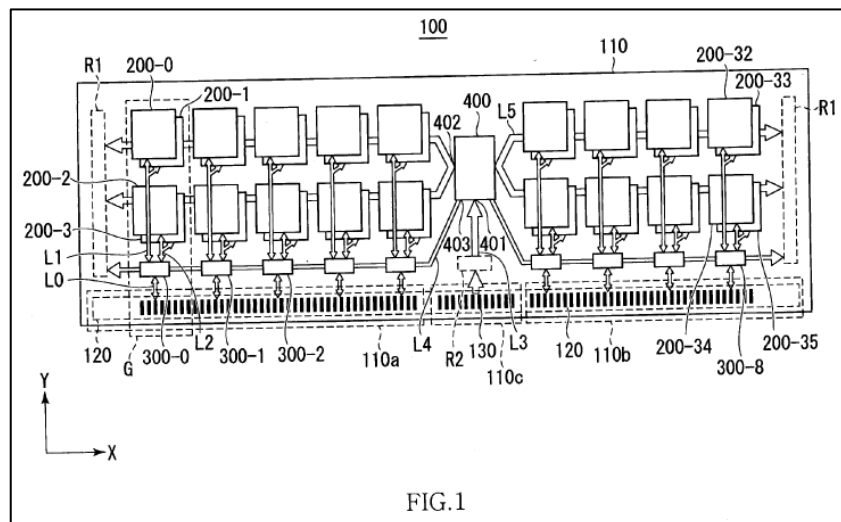


FIG. 1

Hiraishi at Fig. 1.

'608 patent	35 U.S.C. §§ 102, 103 Analysis
	“The module substrate 110 is a printed circuit board that includes a multilayer wiring. The planar shape of the module substrate 110 is substantially rectangle, as shown in FIG. 1, with a long side in the X direction and a short side in the Y direction. On one side of the module substrate 110 along the X direction, which is the long side, a plurality of data connectors 120 and a plurality of command/address/control connectors 130 are provided. The data connectors 120 and the command/address/control connectors 130 are terminals for making an electrical connection with a memory controller via a memory slot, which will be described later.” Hiraishi at [0047]. “The data connectors 120 are connectors for exchanging write data to be written in the memory chip 200 and read data read from the memory chip 200 between the memory module 100 and the memory controller. Although it is not particularly limited, the number of pins of the data connectors 120 is seventy two in the present embodiment. As shown in FIG. 1, among the seventy-two data connectors 120, data connectors corresponding to the memory chips 200-0 to 200-19 are arranged in an area 110a that is located substantially right below the memory chips 200-0 to 200-19, and data connectors corresponding to the memory chips 200-20 to 200-35 are arranged in an area 110 b that is located substantially right below the memory chips 200-20 to 200-35.” Hiraishi at [0048]. “The command/address/control connectors 130 are connectors for supplying a command signal, an address signal, a control signal, and a clock signal to be supplied to the command/address/control register buffer 400. As shown in FIG. 1, the command/address/control connectors 130 are arranged in an area 110 c that is located between the area 110 a and the area 110 b.” Hiraishi at [0049]. “As shown in FIG. 3, a memory slot 22 is provided on the motherboard 21, so that the memory module 100 is inserted in the memory slot 22. On the other hand, a memory controller 12 is directly mounted on the motherboard 21. As described above, a plurality of memory chips 200 are mounted on the memory module 100. On a signal path between the memory controller 12 and the memory chips 200, there exist a line 23 formed on the motherboard 21 and the data line L0 and the command/address/control line L3 formed on the module substrate 110. However, as described above referring to FIG. 1, in the memory module 100 according to the present embodiment, because the data register buffer 300 is connected to the data line L0, the memory controller 12 cannot experience the load capacity of the memory chips 200 that exist on the signal path beyond the data register buffer 300. Similarly, because the command/address/control register buffer 400 is connected to the command/address/control line L3, the memory controller 12 cannot experience

'608 patent	35 U.S.C. §§ 102, 103 Analysis
	the load capacity of the memory chips 200 that exist on the signal path beyond the command/address/control register buffer 400. Therefore, the load capacity of the signal path that connects the memory controller 12 and the memory module 100 is reduced, making it possible to ensure an excellent signal quality even with a high data transfer rate. Although only a single memory slot 22 is provided on the motherboard 21 in the memory system 20 shown in FIG. 3, in actual cases, a plurality of memory slots (for example, four) are provided on the memory system, so that the memory module 100 is mounted on each of the memory slots. As the number of units of the memory module 100 increases, the load capacity of the signal path increases by the number of memory modules. However, according to the present embodiment, because the load capacity per memory module is considerably smaller than that of a conventional memory module, it is possible to perform a high speed data transfer even when a plurality of memory modules are mounted.” Hiraishi at [0068-0070].
1[b] a module control device mounted on the module board and configured to receive system command signals for memory operations via the set of control/address signal lines and to output module command signals and module control signals in response to the system command signals, the module control device being further configured to receive a system clock signal and output a module clock signal; and	Based on Netlist’s apparent view of the scope of the ’608 patent claims, as articulated in its Infringement Contentions and which I disagree with, it is my opinion that Hiraishi alone or in view of the knowledge of a POSITA discloses element 1[b]. For example, Hiraishi discloses a module control device (e.g., command/address/control register buffer 400) mounted on the module board (e.g., module substrate 110) and configured to receive system command signals for memory operations via the set of control/address signal lines (e.g., command/address/control connectors 130 and command/address/control line L3). The module control device is also configured to output module command signals (e.g., ADD/CMD-Post) and module control signals (e.g., DRC) in response to the system command signals, and to receive a system clock signal (e.g., Clock-Pre) and output a module clock signal (e.g., Clock-Post). “FIG. 6 is a block diagram of the configuration of the command/address/control register buffer 400; FIG. 7 is a connection diagram of the memory module 100,” Hiraishi at [0018-0019]. “FIG. 6 is a block diagram of the configuration of the command/address/control register buffer 400. As shown in FIG. 6, the command/address/control register buffer 400 includes the input terminal 401 for connecting to the command/address/control connectors 130, the output terminal 402 for connecting to the memory chip 200, and the output terminal 403 and an input terminal 404 for connecting to the data register buffer 300.” Hiraishi at [0095-0096].

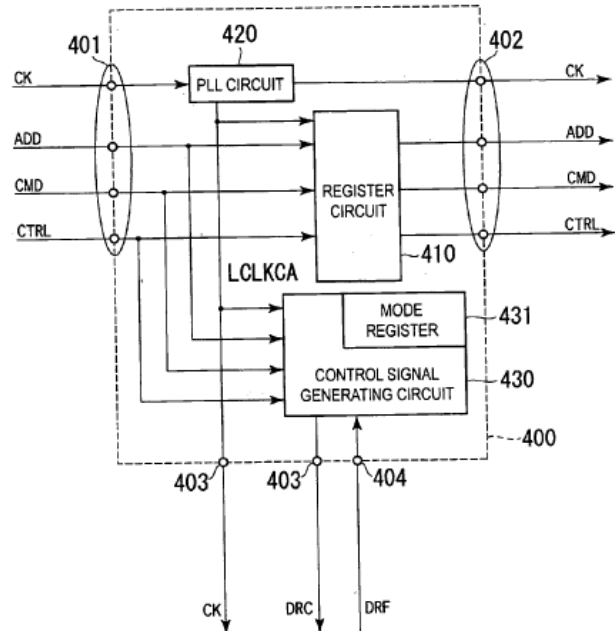


FIG. 6

Hiraishi at Fig. 6.

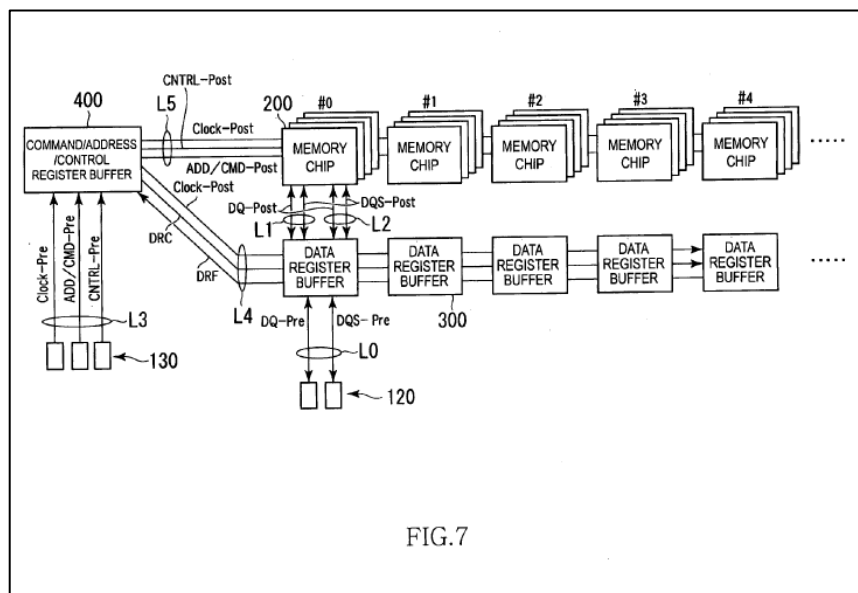
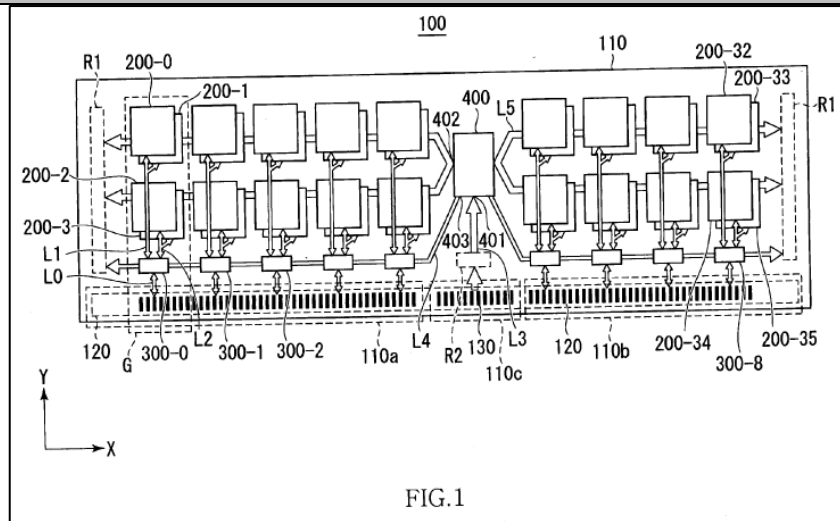


FIG. 7

Hiraishi at Fig. 7.

'608 patent	35 U.S.C. §§ 102, 103 Analysis
	“As shown in FIG. 1, the memory module 100 according to the present embodiment includes a module substrate 110, a plurality of memory chips 200 mounted on the module substrate 110, a plurality of data register buffers 300, and a command/address/control register buffer 400. In the present embodiment, the memory module 100 includes thirty-six memory chips 200. When it is necessary to specify each of the memory chips, the memory chips are respectively represented by memory chips 200-0 to 200-35. Furthermore, in the present embodiment, the memory module 100 includes nine data register buffers 300. When it is necessary to specify each of the data register buffers, the data register buffers are respectively represented by data register buffers 300-0 to 300-8. On the other hand, the command/address/control register buffer 400 is provided as a single unit. However, it is not essential to set the number of units of the command/address/control register buffer 400 to one, but two or more units of the command/address/control register buffer 400 can be mounted without any limitation.” Hiraishi at [0045-0046]. “The module substrate 110 is a printed circuit board that includes a multilayer wiring. The planar shape of the module substrate 110 is substantially rectangle, as shown in FIG. 1, with a long side in the X direction and a short side in the Y direction. On one side of the module substrate 110 along the X direction, which is the long side, a plurality of data connectors 120 and a plurality of command/address/control connectors 130 are provided. The data connectors 120 and the command/address/control connectors 130 are terminals for making an electrical connection with a memory controller via a memory slot, which will be described later.” Hiraishi at [0047]. “The command/address/control connectors 130 are connectors for supplying a command signal, an address signal, a control signal, and a clock signal to be supplied to the command/address/control register buffer 400. As shown in FIG. 1, the command/address/control connectors 130 are arranged in an area 110 c that is located between the area 110 a and the area 110 b.” Hiraishi at [0049]. “An operation of the memory chip 200 is controlled based on the command signal, the address signal, the control signal, and the clock signal supplied from the command/address/control register buffer 400. Details on the memory chip 200 will be described later.” Hiraishi at [0054]. “An operation of the data register buffer 300 is controlled based on the control signal supplied from the command/address/control register buffer 400. Details on the data register buffer 300 will be described later. Only a single command/address/control register buffer 400 is mounted on the module substrate 110. As shown in FIG. 1, the command/address/control register buffer 400 is arranged at an approximate center portion of the module substrate 110 in the X direction, which is the long side. The

'608 patent	35 U.S.C. §§ 102, 103 Analysis
	command/address/control register buffer 400 receives the command signal, the address signal, the control signal, and the clock signal (in some cases, collectively referred to as a command/address/control signal and the like) that are supplied from the command/address/control connectors 130 through an input terminal 401, buffers the signals, and supplies the signals to the memory chips 200. At the same time, the command/address/control register buffer 400 generates a control signal. The command/address/control signal to be supplied to the memory chips 200 are output through an output terminal 402, and the control signal to be supplied to the data register buffers 300 are output through an output terminal 403. The output terminal 402 is provided at each of the left side and the right side of the command/address/control register buffer 400. For example, the output terminal 402 at the left side is commonly connected to the memory chips 200-0 to 200-19 except for a control signal that is used to select the Rank. That is, the command signal, the address signal, and the clock signal are commonly supplied to the memory chips 200-0 to 200-19. Similarly, the output terminal 403 is provided at each of the left side and the right side of the command/address/control register buffer 400. For example, the output terminal 403 at the left side is commonly connected to the data register buffers 300-0 to 300-4, so that the generated control signal is commonly supplied to the data register buffers 300-0 to 300-4. In addition, on the module substrate 110, a terminating resistor R1 is provided at both edges in the X direction to prevent a reflection of the command/address signal and the control signal output from the command/address/control register buffer 400. Furthermore, in order to prevent a reflection wave of the command/address/control signal that is input to the command/address/control register buffer 400, a stub resistor R2 is inserted on a command/address/control line L3 that connects the command/address/control connectors 130 and the command/address/control register buffer 400. Details on the command/address/control register buffer 400 will be described later.” Hiraishi at [0058-0062].



Hiraishi at Fig. 1.

“On a signal path between the memory controller **12** and the memory chips **200**, there exist a line **23** formed on the motherboard **21** and the data line **L0** and the command/address/control line **L3** formed on the module substrate **110**. However, as described above referring to FIG. 1, in the memory module **100** according to the present embodiment, because the data register buffer **300** is connected to the data line **L0**, the memory controller **12** cannot experience the load capacity of the memory chips **200** that exist on the signal path beyond the data register buffer **300**. Similarly, because the command/address/control register buffer **400** is connected to the command/address/control line **L3**, the memory controller **12** cannot experience the load capacity of the memory chips **200** that exist on the signal path beyond the command/address/control register buffer **400**. Therefore, the load capacity of the signal path that connects the memory controller **12** and the memory module **100** is reduced, making it possible to ensure an excellent signal quality even with a high data transfer rate.” Hiraishi at [0069].

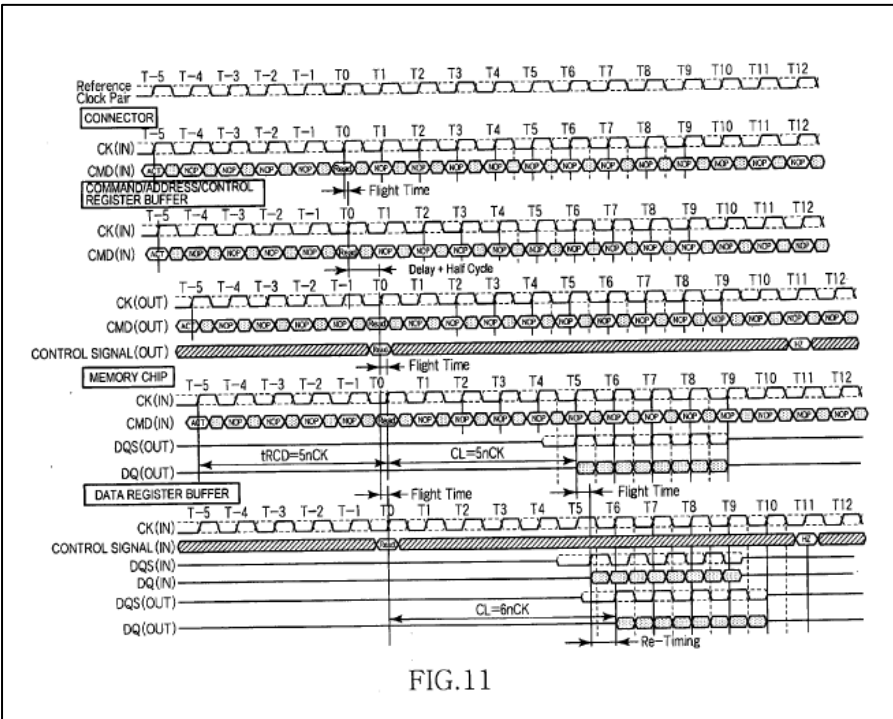
“The memory chip **200** is a DRAM, which includes, as shown in FIG. 4, a clock terminal **201**, a command terminal **202**, a control terminal **206**, an address terminal **203**, a data input/output terminal **204**, and a data strobe terminal **205** as external terminals. Among these terminals, the clock terminal **201**, the command terminal **202**, the control terminal **206**, and the address terminal **203** are connected to the command/address/control register buffer **400** via a command/address/control line **L5** shown in FIG. 1. The data input/output terminal **204** and the data strobe terminal **205** are connected to the data register buffer **300** via the data line **L1** or the data line **L2** shown in FIG. 1. Although not shown in FIG. 1, the memory chip **200** further includes other terminals such as a power supply terminal.” Hiraishi at [0073].

'608 patent	35 U.S.C. §§ 102, 103 Analysis
	“The clock terminal 201 is a terminal to which a clock signal CK is supplied. The clock signal CK is then supplied to an internal clock generating circuit 211. An internal clock ICLK, which is an output of the internal clock generating circuit 211, is supplied to various internal circuits. The clock signal CK is also supplied to a DLL circuit 212. The DLL circuit 212 takes a role of generating an internal clock LCLK and supplying the internal clock LCLK to a data input/output circuit 213 and a data strobe signal input/output circuit 214. The internal clock LCLK is a signal that is phase-controlled with respect to the clock signal CK, of which a phase is slightly advanced with respect to the clock signal CK such that phases of read data DQ and a data strobe signal DQS match with a phase of the clock signal CK. It is selected based on a set content in a mode register whether to use the DLL circuit 212. That is, when “DLL on mode” is set in a mode register 215, the DLL circuit 212 is enabled, so that the internal clock LCLK is phase-controlled with respect to the clock signal CK. On the other hand, when “DLL off mode” is set in the mode register 215, the DLL circuit 212 is disabled (the clock signal CK is shortcut), so that the internal clock LCLK is not phase-controlled with respect to the clock signal CK.” Hiraishi at [0074-0075]. “The command terminal 202 is a terminal to which a command signal CMD that includes a row address strobe (RAS) signal, a column address strobe (CAS) signal, a write enable (WE) signal, and the like is supplied. The control terminal 206 is a terminal to which a control signal CTRL for each Rank, such as a chip select (CS) signal, a clock enable (CKE) signal, and an on die termination (ODT) signal, is supplied. By the chip select (CS) signal, a DRAM for which a command is to be issued is switched, and an activation of a clock system and a control of an on die termination in the DRAM are performed. The command signal CMD is supplied to a command decoder 216. The command decoder 216 is a circuit that generates various internal commands ICMD by storing, decoding, and counting the command signal in synchronization with the internal clock ICLK. The generated internal commands are supplied to various control circuits (not shown) including the mode register 215. The control signal CTRL is supplied to a control circuit 218. The control circuit 218 is a circuit that generates an internal control signal such as the ODT signal based on the control signal CTRL.” Hiraishi at [0076]. “The address terminal 203 is a terminal to which an address signal ADD is supplied. The address signal is then supplied to an address latch circuit 217. The address latch circuit 217 is a circuit that latches the address signal ADD in synchronization with the internal clock ICLK. Among the address signals ADD that are latched in the address latch circuit 217, a row address is supplied to a row decoder 221 and a column address is supplied to a column decoder 222. In addition, upon entering a mode register set, the address signal ADD is supplied

'608 patent	35 U.S.C. §§ 102, 103 Analysis
	to the mode register 215, by which a content of the mode register 215 is updated.” Hiraishi at [0077]. “The FIFO circuits 301 and 302 shown in FIG. 5 are circuits that perform input and output of 1-bit data, so that in an actual case, the number of sets of the FIFO circuits 301 and 302 as many as a width of input/output data are provided. In the present embodiment, because a single data register buffer 300 inputs and outputs 1-byte data, 8 sets of the FIFO circuits 301 and 302 are required.” Hiraishi at [0085]. “The command/address/control signal that is supplied from the memory controller 12 is input from the input terminal 401. Among input command/address/control signals, the command signal CMD, the address signal ADD, and the control signal CTRL are supplied to a register circuit 410, and the clock signal CK is supplied to a PLL circuit 420. The register circuit 410 is a circuit that buffers the command signal CMD, the address signal ADD, and the control signal CTRL, and the buffered command signal CMD, address signal ADD, and control signal CTRL are supplied to the memory chip 200 via the output terminal 402. An operation timing of the register circuit 410 is defined by an internal clock LCLKCA that is generated by the PLL circuit 420. The PLL circuit 420 is a circuit that generates the internal clock LCLKCA based on the clock signal CK supplied from the memory controller 12 having the same circuit configuration and function as that of the DLL circuit 212 provided in the memory chip 200. It is selected based on a set content in a mode register 431 that is included in a control signal generating circuit 430 whether to use the PLL circuit 420. The PLL circuit 420 can be replaced with a DLL circuit. The control signal generating circuit 430 is a circuit that generates the control signal DRC to be supplied to the data register buffer 300 based on the command/address/control signal supplied via the input terminal 401, of which an operation is performed in synchronization with the internal clock LCLKCA. The control signal DRC for the data register buffer 300 is supplied to the data register buffer 300 via the output terminal 403. The feedback signal DRF is supplied to the control signal generating circuit 430 from the data register buffer 300 via the input terminal 404. The control signal DRC includes signals such as a signal indicating a direction of transmitting and receiving data, a signal for controlling an ODT timing at the data line L0 side of the data register buffer 300, a signal for controlling an ODT timing at the data lines L1 and L2 side, a signal for controlling on and off of the DLL circuit, a signal for controlling enable and disable of the data register buffer 300, and a signal for performing a mode switching of the data register buffer 300 and a mode register set and the like. A separate line can be allocated

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	to each of these signals, or a single common line can be allocated to a plurality of these signals. Alternatively, these signals can be transmitted to the data register buffer 300 as commands.” Hiraishi at [0097-0100]. “The address signal ADD, the command signal CMD, the control signal CTRL, and the clock signal CK supplied to the memory chips 200 are supplied from the command/address/control register buffer 400. The control signal DRC supplied to the data register buffer 300 is also supplied from the command/address/control register buffer 400. As shown in FIG. 7, the command/address/control connectors 130 and the command/address/control register buffer 400 are connected to each other with the command/address/control line L3, the command/address/control register buffer 400 and the data register buffer 300 are connected to each other with a control line L4, and the command/address/control register buffer 400 and the memory chips 200 are connected to each other with a command/address/control line L5. In FIG. 7, a command/address/control signal transferred through the command/address/control line L3 is represented by a command/address signal ADD/CMD-Pre, and a command/address signal transferred through the command/address/control line L5 is represented by a command/address signal ADD/CMD-Post. Similarly, a control signal transferred through the command/address/control line L3 is represented by a control signal CNTRL-Pre, and a control signal transferred through the command/address/control line L5 is represented by a control signal CNTRL-Post. The clock signal CK to be supplied to the memory chip 200 and the data register buffer 300 is supplied from the command/address/control register buffer 400. In FIG. 7, a clock signal transferred through the command/address/control line L3 is represented by a clock signal Clock-Pre, and a clock signal transferred through the command/address/control line L5 is represented by a clock signal Clock-Post.” Hiraishi at [0106-0108]. “The operation of the memory module 100 according to the present embodiment is explained below in more detail. FIG. 11 is a timing chart for explaining a read operation of the memory module 100 according to the present embodiment. In the read operation, an active command ACT and a read command Read are issued in order from the memory controller 12. In the example shown in FIG. 11, the active command ACT reaches the command/address/control connectors 130 at a time T-5 that is synchronized with the clock signal CK, and the read command Read reaches the command/address/control connectors 130 at a time T0.

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	The commands ACT and Read reaching the command/address/control connectors 130 are input to the command/address/control register buffer 400. At this moment, there occurs a predetermined time difference (Flight Time) between a timing at which the commands ACT and Read reaches the command/address/control connectors 130 and a timing at which the commands ACT and Read are input to the command/address/control register buffer 400. The command/address/control register buffer 400 registers the received commands ACT and Read with an input clock signal in the register circuit 410 shown in FIG. 6, and then outputs them to the memory chip 200. At this time, a synchronization with the output of the commands ACT and Read is taken by delaying the output of the clock signal CK by an amount equivalent to an additional $\frac{1}{2}$ clock cycle. In addition, the command/address/control register buffer 400 supplies a read command Read to the data register buffer 300 as a part of the control signal DRC. The memory chip 200 receives the commands ACT and Read, and starts an actual read operation. At this moment, there occurs a predetermined time difference (Flight Time) between a timing at which the commands ACT and Read are output from the command/address/control register buffer 400 and a timing at which the commands ACT and Read are input to the memory chip 200. Because CL=5 in the example shown in FIG. 11, the memory chip 200 starts a burst output of read data DQ at a time T5 in five clock cycles after receiving the read command Read. In the example shown in FIG. 11, the burst length is 8 bits (BL=8). The read data DQ and a data strobe signal DQS burst output from the memory chip 200 are supplied to the data register buffer 300. The data register buffer 300 loads the read data DQ that is output from the memory chip 200 in the FIFO (Read) circuit 302 with a data strobe signal DQS that is delayed by a predetermined phase amount (for example, phase difference of about 90 degrees). At this moment, there occurs a predetermined time difference (Flight Time) between a timing at which the read data DQ and the data strobe signal DQS are output from the memory chip 200 and a timing at which the read data DQ and the data strobe signal DQS are input to the data register buffer 300. Thereafter, the data register buffer 300 performs a re-timing in synchronization with the internal clock LCLKR using the FIFO (Read) circuit 302 to convert CL into CL=6, and outputs the read data DQ and the data strobe signal DQS. With this configuration, it becomes possible for the memory controller to receive the read data DQ in a correct manner.

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	The read operation of the memory module 100 according to the present embodiment is as described above. A write operation of the memory module 100 is explained next.” Hiraishi at [0122-0131].  FIG. 11 Hiraishi at Fig. 11.
1[c] memory devices mounted on the module board and configured to receive the module command signals and the module clock signal, and to perform the memory operations in response to the module command signals, the memory devices including a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of	Based on Netlist’s apparent view of the scope of the ’608 patent claims, as articulated in its Infringement Contentions and which I disagree with, it is my opinion that Hiraishi alone or in view of the knowledge of a POSITA discloses element 1[c]. For example, Hiraishi discloses memory devices (e.g., memory chips 200-0 to 200-35) mounted on the module board and configured to receive the module command signals (e.g., L5) and the module clock signal (e.g., Clock-Post) and to perform the memory operations in response to the module command signals. The memory devices include a plurality of sets of memory devices (e.g., 200-0 through 200-3) corresponding to respective sets of the plurality of sets of data/strobe signal lines (e.g., L0). “A memory module such as a DIMM (Dual Inline Memory Module) has a configuration in which a large number of memory chips such as DRAMs (Dynamic Random Access Memories) are mounted on a module substrate. Such a memory module is inserted in a memory slot provided on a motherboard, thereby a data transfer is performed between a memory controller and the memory module. In recent years, because a system requires a considerable

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data/strobe signal lines; and	amount of memory capacity, it is hard to provide the required memory capacity with a single memory module. Therefore, in most cases, the motherboard includes a plurality of memory slots, so that a plurality of memory modules can be mounted on the motherboard.” Hiraishi at [0004]. “As shown in FIG. 1, the memory module 100 according to the present embodiment includes a module substrate 110, a plurality of memory chips 200 mounted on the module substrate 110, a plurality of data register buffers 300, and a command/address/control register buffer 400. In the present embodiment, the memory module 100 includes thirty-six memory chips 200. When it is necessary to specify each of the memory chips, the memory chips are respectively represented by memory chips 200-0 to 200-35. Furthermore, in the present embodiment, the memory module 100 includes nine data register buffers 300. When it is necessary to specify each of the data register buffers, the data register buffers are respectively represented by data register buffers 300-0 to 300-8. On the other hand, the command/address/control register buffer 400 is provided as a single unit. However, it is not essential to set the number of units of the command/address/control register buffer 400 to one, but two or more units of the command/address/control register buffer 400 can be mounted without any limitation.” Hiraishi at [0045-0046]. FIG. 1 Hiraishi at Fig. 1. “The data connectors 120 are connectors for exchanging write data to be written in the memory chip 200 and read data read from the memory chip 200 between the memory module 100 and the memory controller. Although it is not particularly limited, the number of pins of the data connectors 120 is seventy two in the present embodiment. As shown in FIG. 1, among the seventy-two data connectors 120, data connectors corresponding to

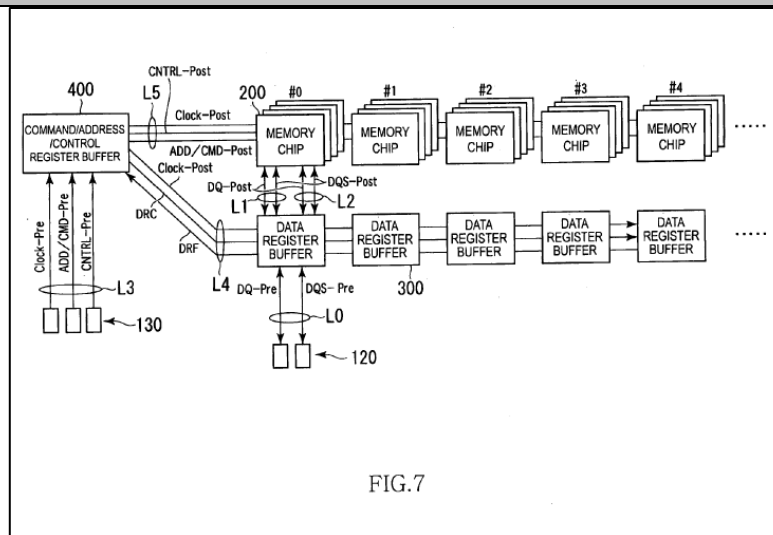
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	the memory chips 200-0 to 200-19 are arranged in an area 110a that is located substantially right below the memory chips 200-0 to 200-19, and data connectors corresponding to the memory chips 200-20 to 200-35 are arranged in an area 110 b that is located substantially right below the memory chips 200-20 to 200-35. The command/address/control connectors 130 are connectors for supplying a command signal, an address signal, a control signal, and a clock signal to be supplied to the command/address/control register buffer 400. As shown in FIG. 1, the command/address/control connectors 130 are arranged in an area 110 c that is located between the area 110 a and the area 110 b.” Hiraishi at [0048-0049]. “The memory chips 200 are, for example, DRAMs. The memory chips 200-0, 200-2, . . . with even branch numbers are mounted on one surface of the module substrate 110 (a first surface), and the memory chips 200-1, 200-3, . . . with odd branch numbers are mounted on the other surface of the module substrate 110 (a second surface). Two corresponding memory chips, for example, the memory chips 200-0 and 200-1 are mounted at positions facing each other across the module substrate 110, respectively.” Hiraishi at [0050]. “In the present embodiment, four memory chips 200 constitute a single group (a single set), and the four memory chips 200 constituting the single group belong to different Ranks from each other. For example, the memory chips 200-0 to 200-3 constitute a single group, and the memory chips 200-0 to 200-3 belong to different Ranks from each other. As shown in FIG. 1, the four memory chips 200 constituting a single group are connected to one of the data register buffers 300. For example, the group of the memory chips 200-0 to 200-3 is connected to the data register buffer 300-0. Among the memory chips 200-0 to 200-3, the memory chips 200-0 and 200-1 that are mounted on the upper side of the module substrate 110 are connected to the data register buffer 300-0 via a data line L1, and the memory chips 200-2 and 200-3 that are mounted on the lower side of the module substrate 110 are connected to the data register buffer 300-0 via a data line L2. An arrow of each of the data lines L1 and L2 shown in FIG. 1 indicates a line of 1 byte (8 bits). Both the data lines L1 and L2 are formed inside the module substrate 110.” Hiraishi at [0052-0053]. “An operation of the memory chip 200 is controlled based on the command signal, the address signal, the control signal, and the clock signal supplied from the command/address/control register buffer 400. Details on the memory chip 200 will be described later.” Hiraishi at [0054].

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	“With the above configuration, the single data register buffer 300, the data connectors 120 and the four memory chips 200 corresponding to the data register buffer 300 constitute a group G. The memory chips 200, the data register buffer 300, and the data connectors 120 included in the same group are arranged along the Y direction, which is the short side, and a plurality of groups G formed in the above manner are arranged along the X direction, which is the long side. Therefore, a relative positional relationship between each of the data register buffers 300 and corresponding four memory chips 200 becomes constant in all the groups G.” Hiraishi at [0056]. “The command/address/control register buffer 400 receives the command signal, the address signal, the control signal, and the clock signal (in some cases, collectively referred to as a command/address/control signal and the like) that are supplied from the command/address/control connectors 130 through an input terminal 401, buffers the signals, and supplies the signals to the memory chips 200. At the same time, the command/address/control register buffer 400 generates a control signal. The command/address/control signal to be supplied to the memory chips 200 are output through an output terminal 402, and the control signal to be supplied to the data register buffers 300 are output through an output terminal 403. The output terminal 402 is provided at each of the left side and the right side of the command/address/control register buffer 400. For example, the output terminal 402 at the left side is commonly connected to the memory chips 200-0 to 200-19 except for a control signal that is used to select the Rank. That is, the command signal, the address signal, and the clock signal are commonly supplied to the memory chips 200-0 to 200-19. Similarly, the output terminal 403 is provided at each of the left side and the right side of the command/address/control register buffer 400. For example, the output terminal 403 at the left side is commonly connected to the data register buffers 300-0 to 300-4, so that the generated control signal is commonly supplied to the data register buffers 300-0 to 300-4.” Hiraishi at [0060-0061]. “As shown in FIG. 3, a memory slot 22 is provided on the motherboard 21, so that the memory module 100 is inserted in the memory slot 22. On the other hand, a memory controller 12 is directly mounted on the motherboard 21. As described above, a plurality of memory chips 200 are mounted on the memory module 100. On a signal path between the memory controller 12 and the memory chips 200, there exist a line 23 formed on the motherboard 21 and the data line L0 and the command/address/control line L3 formed on the module substrate 110. However, as described above referring to FIG. 1, in the memory module 100 according to the present embodiment, because the data register buffer 300 is connected to the data line L0, the memory controller 12 cannot

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	experience the load capacity of the memory chips 200 that exist on the signal path beyond the data register buffer 300. Similarly, because the command/address/control register buffer 400 is connected to the command/address/control line L3, the memory controller 12 cannot experience the load capacity of the memory chips 200 that exist on the signal path beyond the command/address/control register buffer 400. Therefore, the load capacity of the signal path that connects the memory controller 12 and the memory module 100 is reduced, making it possible to ensure an excellent signal quality even with a high data transfer rate.” Hiraishi at [0068-0069]. “It is selected based on a set content in a mode register whether to use the DLL circuit 212. That is, when “DLL on mode” is set in a mode register 215, the DLL circuit 212 is enabled, so that the internal clock LCLK is phase-controlled with respect to the clock signal CK. On the other hand, when “DLL off mode” is set in the mode register 215, the DLL circuit 212 is disabled (the clock signal CK is shortcut), so that the internal clock LCLK is not phase-controlled with respect to the clock signal CK. The command terminal 202 is a terminal to which a command signal CMD that includes a row address strobe (RAS) signal, a column address strobe (CAS) signal, a write enable (WE) signal, and the like is supplied. The control terminal 206 is a terminal to which a control signal CTRL for each Rank, such as a chip select (CS) signal, a clock enable (CKE) signal, and an on die termination (ODT) signal, is supplied. By the chip select (CS) signal, a DRAM for which a command is to be issued is switched, and an activation of a clock system and a control of an on die termination in the DRAM are performed. The command signal CMD is supplied to a command decoder 216. The command decoder 216 is a circuit that generates various internal commands ICMD by storing, decoding, and counting the command signal in synchronization with the internal clock ICLK. The generated internal commands are supplied to various control circuits (not shown) including the mode register 215. The control signal CTRL is supplied to a control circuit 218. The control circuit 218 is a circuit that generates an internal control signal such as the ODT signal based on the control signal CTRL.” Hiraishi at [0075-0076]. “The row decoder 221 is a circuit that selects one of word lines WL included in a memory cell array 230. In the memory cell array 230, a plurality of word lines WL and a plurality of bit lines BL intersect with each other, and a memory cell MC is arranged at each intersection point (only a single word line WL, a single bit line BL, and a single memory cell MC are shown in FIG. 4). The bit line BL is connected to one of sense amplifiers SA that are included in a sense amplifier array 231. The column decoder 222 performs a selection of the sense amplifier SA.

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	The selected sense amplifier SA is connected to the data input/output circuit 213. The internal clock LCLK and an internal data strobe signal PDQS are supplied to the data input/output circuit 213. In a read operation, the data input/output circuit 213 outputs read data in synchronization with the internal clock LCLK, and in a write operation, the data input/output circuit 213 loads write data in synchronization with the internal data strobe signal PDQS. With this arrangement, in the read operation, the read data read out from the memory cell array 230 is output from the data input/output terminal 204, and in the write operation, the write data received from the data input/output terminal 204 is supplied to the memory cell array 230. The data strobe terminal 205 is a terminal for performing input and output of the data strobe signal DQS, which is connected to the data strobe signal input/output circuit 214. The data strobe signal input/output circuit 214 generates the internal data strobe signal PDQS described above, and supplies it to the data input/output circuit 213.” Hiraishi at [0078-0080]. “The input/output terminals 340 and 350 are connected to the data connectors 120 via the data line L0. On the other hand, the input/output terminals 341 and 351 are connected to the memory chip 200 via the data line L1, and the input/output terminals 342 and 352 are connected to the memory chip 200 via the data line L2. In this manner, for the data register buffer 300, the number of the input/output terminals (M) to be connected to the memory controller 12 and the number of the input/output terminals (N) to be connected to the memory chip 200 are different from each other, which is, in the present embodiment, N=2M. In other words, the number of the data lines L1 and L2 is N/M times the number of the data line L0 (two times in the present embodiment).” Hiraishi at [0086]. “An output operation timing of the FIFO (Write) circuit 301 is defined by the internal clock LCLKW that is generated by the DLL circuit 310. An output operation timing of the FIFO (Read) circuit 302 is defined by the internal clock LCLKR that is generated by the DLL circuit 310. The DLL circuit 310 is a circuit that generates the internal clocks LCLKW and LCLKR based on the clock signal CK that is supplied from the command/address/control register buffer 400, having the same circuit configuration and function as that of the DLL circuit 212 provided in the memory chip 200. It is selected based on a set content in a data register control circuit 320 whether to use the DLL circuit 310. The DLL circuit 310 can be replaced with a PLL circuit. The data register control circuit 320 is a circuit that controls the operation of the data register buffer 300 based on a control signal DRC that is supplied from the command/address/control register buffer 400. Specifically, the data register control circuit 320 controls operations of an input buffer INB and an output buffer OUTB by generating a buffer control signal BC, and at the same time,

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	controls operations of selectors 331 to 334 by generating a select signal SEL. Contents of controlling the output buffer OUTB include, for example, an adjustment of output impedance and an on/off control of an ODT operation. It is selected based on a set content in a mode register 321 that is included in the data register control circuit 320 whether to use the ODT function.” Hiraishi at [0087-0088]. “The selector 333 is a circuit that supplies data DQ that is an output of the FIFO (Write) circuit 301 to either one of the input/output terminals 341 and 342. The selector 334 is a circuit that selects data DQ input from either one of the input/output terminals 341 and 342 and supplies the selected data DQ to the FIFO (Read) circuit 302. The selectors 331 and 332 perform the similar functions as those of the selectors 333 and 334, respectively. Specifically, the selector 332 selects a data strobe signal DQS input from either one of the input/output terminals 351 and 352. A phase of the selected data strobe signal DQS is delayed by about 90 degrees by a delay circuit 372, and then the data strobe signal DQS is supplied to the FIFO (Read) circuit 302 as an input trigger signal. The selector 331 supplies the data strobe signal DQS that is supplied from the strobe generating circuit 374 to either one of the input/output terminals 351 and 352. A phase of the data strobe signal DQS generated by the strobe generating circuit 374 is delayed by about 90 degrees with respect to the internal clock LCLKW by a delay circuit 370. Each of the selections by the selectors 331 to 334 is specified by the select signal SEL that is an output of the data register control circuit 320.” Hiraishi at [0091]. “FIG. 7 is a connection diagram of the memory module 100 according to the present embodiment. As shown in FIG. 7, in the present embodiment, the data register buffer 300 intervenes between the data connectors. 120 and the memory chips 200. The data connectors 120 and the data register buffer 300 are connected to each other with the data line L0, and the data register buffer 300 and the memory chips 200 are connected to each other with the data line L1 or L2. In FIG. 7, a plurality of data transferred through the data line L0 is represented by data DQ-Pre, and a plurality of data transferred through the data lines L1 and L2 is represented by data DQ-Post. Similarly, a data strobe signal transferred through the data line L0 is represented by a data strobe signal DQS-Pre, and a data strobe signal transferred through the data line L1 or L2 is represented by a data strobe signal DQS-Post.” Hiraishi at [0102-0103].



Hiraishi at Fig. 7.

“As described above, in the present embodiment, the four memory chips **200** are allocated to a single data register buffer **300**. The four memory chips **200** are memory chips that constitute different Ranks from each other, which are exclusively activated by the chip select (CS) signal or the clock enable (CKE) signal included in the control signal CTRL. The address signal ADD and the command signal CMD are commonly supplied to the four memory chips **200**.

The address signal ADD, the command signal CMD, the control signal CTRL, and the clock signal CK supplied to the memory chips **200** are supplied from the command/address/control register buffer **400**. The control signal DRC supplied to the data register buffer **300** is also supplied from the command/address/control register buffer **400**.” Hiraishi at [0105-0106].

“As shown in FIG. 7, the command/address/control connectors **130** and the command/address/control register buffer **400** are connected to each other with the command/address/control line L3, the command/address/control register buffer **400** and the data register buffer **300** are connected to each other with a control line L4, and the command/address/control register buffer **400** and the memory chips **200** are connected to each other with a command/address/control line L5. In FIG. 7, a command/address/control signal transferred through the command/address/control line L3 is represented by a command/address signal ADD/CMD-Pre, and a command/address signal transferred through the command/address/control line L5 is represented by a command/address signal ADD/CMD-Post. Similarly, a control signal transferred through the command/address/control line L3 is represented by a control signal CNTRL-Pre, and a control signal transferred through the command/address/control line L5 is represented by a control signal CNTRL-Post.” Hiraishi at [0107].

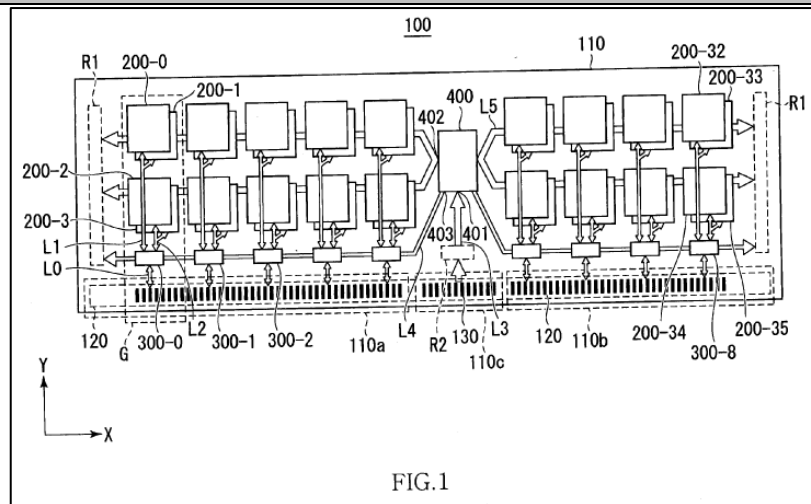
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	“FIG. 10 shows a consecutive read operation from a Rank0 to a Rank3 with a case that a burst length is 4 bits (BL=4) (or a case that a burst operation is stopped at 4 bits by a burst chop). In the example shown in FIG. 10, a read command is issued at times T0, T2, T4, and T6 that are synchronized with the clock signal CK in the order of the Rank0, the Rank2, the Rank1, and the Rank3. In response to these read commands, after a lapse of a predetermined CAS latency (in this example, CL=12), 4-bit read data DQ is burst output. As a result, in a period from a time T12 to a time T14, a data transfer is performed from the memory chip 200 of the Rank0 using the data line L1, in a period from the time T14 to a time T16, a data transfer is performed from the memory chip 200 of the Rank2 using the data line L2, in a period from the time T16 to a time T18, a data transfer is performed from the memory chip 200 of the Rank1 using the data line L1, and in a period from the time T18 to a time T20, a data transfer is performed from the memory chip 200 of the Rank3 using the data line L2. That is, the data lines L1 and L2 are used in an alternate manner. The read data sequentially transferred in the above manner are supplied to the data register buffer 300, and after being buffered in a FIFO circuit included in the data register buffer 300, output to the data line L0. In the example, shown in FIG. 10, since the read data is input to the data register buffer 300, the read data is output with one cycle delay.” Hiraishi at [0117-0119]. “In this manner, in the present embodiment, because the interleaving operation can be performed using the two data lines L1 and L2, it is possible to perform a read operation for a plurality of memory chips without interruption. As a result, the read data output from the data register buffer 300 can also be supplied to the memory controller without interruption, so that the usage efficiency of a bus can be enhanced. Although the data lines L1 and L2 are not simultaneously used in the present embodiment, if the data lines L1 and L2 are put together in a single data line, it is required to spare a time equal to or longer than one cycle between read data output from different memory chips. On the other hand, in the present embodiment, because the two data lines L1 and L2 are alternately used, it is not necessary to put a time between read data output from different memory chips. Although the read operation is explained as an example in FIG. 10, a similar interleaving operation can be applied for a write operation. The operation of the memory module 100 according to the present embodiment is explained below in more detail. FIG. 11 is a timing chart for explaining a read operation of the memory module 100 according to the present embodiment.

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	In the read operation, an active command ACT and a read command Read are issued in order from the memory controller 12. In the example shown in FIG. 11, the active command ACT reaches the command/address/control connectors 130 at a time T-5 that is synchronized with the clock signal CK, and the read command Read reaches the command/address/control connectors 130 at a time T0. The commands ACT and Read reaching the command/address/control connectors 130 are input to the command/address/control register buffer 400. At this moment, there occurs a predetermined time difference (Flight Time) between a timing at which the commands ACT and Read reaches the command/address/control connectors 130 and a timing at which the commands ACT and Read are input to the command/address/control register buffer 400. The command/address/control register buffer 400 registers the received commands ACT and Read with an input clock signal in the register circuit 410 shown in FIG. 6, and then outputs them to the memory chip 200. At this time, a synchronization with the output of the commands ACT and Read is taken by delaying the output of the clock signal CK by an amount equivalent to an additional ½ clock cycle. In addition, the command/address/control register buffer 400 supplies a read command Read to the data register buffer 300 as a part of the control signal DRC. The memory chip 200 receives the commands ACT and Read, and starts an actual read operation. At this moment, there occurs a predetermined time difference (Flight Time) between a timing at which the commands ACT and Read are output from the command/address/control register buffer 400 and a timing at which the commands ACT and Read are input to the memory chip 200. Because CL=5 in the example shown in FIG. 11, the memory chip 200 starts a burst output of read data DQ at a time T5 in five clock cycles after receiving the read command Read. In the example shown in FIG. 11, the burst length is 8 bits (BL=8). The read data DQ and a data strobe signal DQS burst output from the memory chip 200 are supplied to the data register buffer 300. The data register buffer 300 loads the read data DQ that is output from the memory chip 200 in the FIFO (Read) circuit 302 with a data strobe signal DQS that is delayed by a predetermined phase amount (for example, phase difference of about 90 degrees). At this moment, there occurs a predetermined time difference (Flight Time) between a timing at which the read data DQ and the data strobe signal DQS are output from the memory chip 200 and a timing at which the read data DQ and the data strobe signal DQS are input to the data register buffer 300." Hiraishi at [0120-0129].

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	“The memory chip 200 receives the read command Read and performs an actual read operation. In the example shown in FIG. 15, the CAS latency is set to five clock cycles (CL=5), so that an output of read data DQ begins at the time T5. The read data DQ at the time of the read leveling is, for example, a signal in which a High level and a Low level are repeated in an alternate manner.” Hiraishi at [0150]. “As described above, the DLL circuit is a circuit that generates an internal clock signal of which a phase is controlled with respect to an external clock signal, which is used for matching the phases of the read data DQ and the data strobe signal DQS with the phase of the clock signal CK. In a recent high speed memory such as a DDR3 DRAM, a use of the DLL circuit is substantially essential. If the DLL circuit is not used, it is difficult to perform a data transfer in a proper manner. On the other hand, the DLL circuit has a problem of relatively large power consumption.” Hiraishi at [0163]. “However, in the memory module 100 according to the present embodiment, because the load capacities of the data lines L1 and L2 connected to the memory chip 200 are considerably small, even when a high speed memory such as a DDR3 DRAM is used, the ODT operation can be set off in an actual operation. Besides, because a distance between the memory chip 200 and the data register buffer 300 is considerably short, even if a synchronization control is not performed using a DLL circuit, it is possible to perform a data transfer in a correct manner. That is, because both the ODT function and the DLL circuit can be set to off, it is possible to reduce the power consumption by a considerable amount. In addition, because the ODT function and the DLL circuit can be eliminated from the memory chip 200, it is also possible to reduce the chip dimension.” Hiraishi at [0170].
1[d1] a plurality of buffer circuits corresponding to respective sets of the plurality of sets of data/strobe signal lines, wherein each respective buffer circuit of the plurality of buffer circuits is mounted on the module board, coupled between a respective set of data/strobe signal lines and a	Based on Netlist’s apparent view of the scope of the ’608 patent claims, as articulated in its Infringement Contentions and which I disagree with, it is my opinion that Hiraishi alone or in view of the knowledge of a POSITA discloses element 1[d1]. For example, Hiraishi discloses a plurality of buffer circuits (e.g., data register buffer circuits 300) corresponding to respective sets of the plurality of sets of data/strobe signal lines (e.g., DQ-Pre, DQS-Pre). Each buffer circuit is mounted on the module board (e.g., module substrate 110), coupled between a respective data/strobe signal lines (e.g., L0 with DQ-Pre, DQS-Pre and L1/L2 with DQ-Post, DQS-Post) and a respective set of memory devices (e.g., memory chips 200-0 through 200-3). Each buffer circuit is configured to receive the module control signals (e.g., DRC) and the module clock signal (e.g., CK, Clock-Post).

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respective set of memory devices, and configured to receive the module control signals and the module clock signal,

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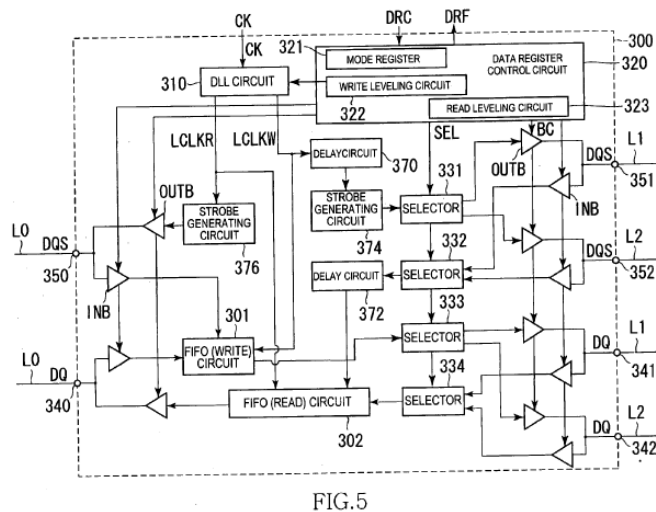
Hiraishi at Fig. 1.

“As shown in FIG. 1, the memory module **100** according to the present embodiment includes a module substrate **110**, a plurality of memory chips **200** mounted on the module substrate **110**, a plurality of data register buffers **300**, and a command/address/control register buffer **400**. In the present embodiment, the memory module **100** includes thirty-six memory chips **200**. When it is necessary to specify each of the memory chips, the memory chips are respectively represented by memory chips **200-0** to **200-35**. Furthermore, in the present embodiment, the memory module **100** includes nine data register buffers **300**. When it is necessary to specify each of the data register buffers, the data register buffers are respectively represented by data register buffers **300-0** to **300-8**. On the other hand, the command/address/control register buffer **400** is provided as a single unit. However, it is not essential to set the number of units of the command/address/control register buffer **400** to one, but two or more units of the command/address/control register buffer **400** can be mounted without any limitation.” Hiraishi at [0045-0046].

“The memory chips **200** are, for example, DRAMs. The memory chips **200-0**, **200-2**, . . . with even branch numbers are mounted on one surface of the module substrate **110** (a first surface), and the memory chips **200-1**, **200-3**, . . . with odd branch numbers are mounted on the other surface of the module substrate **110** (a second surface). Two corresponding memory chips, for example, the memory chips **200-0** and **200-1** are mounted at positions facing each other across the module substrate **110**, respectively.

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	The memory module 100 according to the present embodiment has a so-called 4-Rank configuration. The number of Ranks indicates the number of memory spaces that can be selected in an exclusive manner. Although the same address is assigned to each of the Ranks, one of the Ranks is selected by exclusively activating a chip select (CS) signal or a clock enable (CKE) signal. In the present embodiment, four memory chips 200 constitute a single group (a single set), and the four memory chips 200 constituting the single group belong to different Ranks from each other. For example, the memory chips 200-0 to 200-3 constitute a single group, and the memory chips 200-0 to 200-3 belong to different Ranks from each other. As shown in FIG. 1, the four memory chips 200 constituting a single group are connected to one of the data register buffers 300. For example, the group of the memory chips 200-0 to 200-3 is connected to the data register buffer 300-0. Among the memory chips 200-0 to 200-3, the memory chips 200-0 and 200-1 that are mounted on the upper side of the module substrate 110 are connected to the data register buffer 300-0 via a data line L1, and the memory chips 200-2 and 200-3 that are mounted on the lower side of the module substrate 110 are connected to the data register buffer 300-0 via a data line L2. An arrow of each of the data lines L1 and L2 shown in FIG. 1 indicates a line of 1 byte (8 bits). Both the data lines L1 and L2 are formed inside the module substrate 110.” Hiraishi at [0050-0053]. “A single data register buffer 300 is allocated for every four memory chips 200, as described above, so that nine data register buffers 300 are arranged along the X direction, which is the long side. The data register buffer 300 is a chip for buffering write data that is transferred via a data line L0 and outputting the write data to either one of the data lines L1 and L2, and at the same time, buffering read data that is transferred via either one of the data lines L1 and L2 and outputting the read data to the data line L0. The data line L0 is also formed inside the module substrate 110. With the above configuration, the single data register buffer 300, the data connectors 120 and the four memory chips 200 corresponding to the data register buffer 300 constitute a group G. The memory chips 200, the data register buffer 300, and the data connectors 120 included in the same group are arranged along the Y direction, which is the short side, and a plurality of groups G formed in the above manner are arranged along the X direction, which is the long side. Therefore, a relative positional relationship between each of the data register buffers 300 and corresponding four memory chips 200 becomes constant in all the groups G.” Hiraishi at [0055-0056].

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	“An operation of the data register buffer 300 is controlled based on the control signal supplied from the command/address/control register buffer 400. Details on the data register buffer 300 will be described later.” Hiraishi at [0058]. “The command/address/control register buffer 400 receives the command signal, the address signal, the control signal, and the clock signal (in some cases, collectively referred to as a command/address/control signal and the like) that are supplied from the command/address/control connectors 130 through an input terminal 401, buffers the signals, and supplies the signals to the memory chips 200. At the same time, the command/address/control register buffer 400 generates a control signal. The command/address/control signal to be supplied to the memory chips 200 are output through an output terminal 402, and the control signal to be supplied to the data register buffers 300 are output through an output terminal 403.” Hiraishi at [0060]. “The memory chip 200 is a DRAM, which includes, as shown in FIG. 4, a clock terminal 201, a command terminal 202, a control terminal 206, an address terminal 203, a data input/output terminal 204, and a data strobe terminal 205 as external terminals. Among these terminals, the clock terminal 201, the command terminal 202, the control terminal 206, and the address terminal 203 are connected to the command/address/control register buffer 400 via a command/address/control line L5 shown in FIG. 1. The data input/output terminal 204 and the data strobe terminal 205 are connected to the data register buffer 300 via the data line L1 or the data line L2 shown in FIG. 1. Although not shown in FIG. 1, the memory chip 200 further includes other terminals such as a power supply terminal.” Hiraishi at [0073]. “FIG. 5 is a block diagram of the configuration of the data register buffer 300,” Hiraishi at [0017].



Hiraishi at Fig. 5.

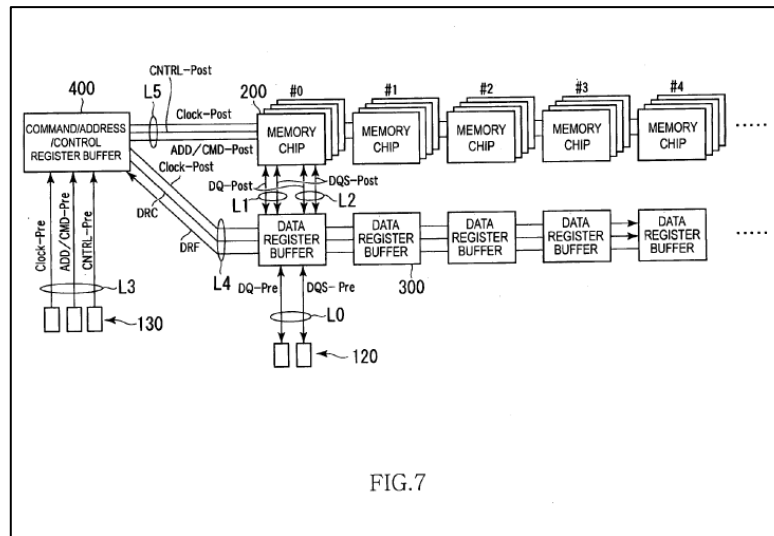
“FIG. 5 is a block diagram of the configuration of the data register buffer **300**.

As shown in FIG. 5, the data register buffer **300** includes a FIFO (Write) circuit **301** and a FIFO (Read) circuit **302**. The FIFO (Write) circuit **301** buffers data DQ that is supplied via an input/output terminal **340** with a data strobe signal DQS that is supplied via an input/output terminal **350**. The FIFO (Read) circuit **302** buffers data DQ that is supplied via an input/output terminal **341** or **342** with a data strobe signal DQS that is supplied via an input/output terminal **351** or **352**. A strobe generating circuit **376** generates a data strobe signal DQS to be supplied to the data connectors **120**, in synchronization with an internal clock LCLKR that is generated by a DLL circuit **310**. A strobe generating circuit **374** generates a data strobe signal DQS to be supplied to the memory chip **200**, in synchronization with an internal clock LCLKW that is generated by the DLL circuit **310**.

The FIFO circuits **301** and **302** shown in FIG. 5 are circuits that perform input and output of 1-bit data, so that in an actual case, the number of sets of the FIFO circuits **301** and **302** as many as a width of input/output data are provided. In the present embodiment, because a single data register buffer **300** inputs and outputs 1-byte data, 8 sets of the FIFO circuits **301** and **302** are required.” Hiraishi at [0083-0085].

“In this manner, the data register buffer **300** buffers the write data that is transferred via the data line L0 and outputs the write data to either one of the data lines L1 and L2, and buffers the read data that is transferred via either one of the data lines L1 and L2 and outputs the read data to the data line L0. Because the data register buffer **300** only performs the buffering of the data,

transfer rates of the write data and the read data that are transferred via the data line L0 and transfer rates of the write data and the read data that are transferred via the data lines L1 and L2 are equal to each other. Therefore, the data register buffer 300 can be implemented with a chip that is provided at relatively low cost instead of an expensive chip such as an AMB used in a Fully Buffered memory module.” Hiraishi at [0092-0093].



Hiraishi at Fig. 7.

“As shown in FIG. 7, in the present embodiment, the data register buffer 300 intervenes between the data connectors. 120 and the memory chips 200. The data connectors 120 and the data register buffer 300 are connected to each other with the data line L0, and the data register buffer 300 and the memory chips 200 are connected to each other with the data line L1 or L2. In FIG. 7, a plurality of data transferred through the data line L0 is represented by data DQ-Pre, and a plurality of data transferred through the data lines L1 and L2 is represented by data DQ-Post. Similarly, a data strobe signal transferred through the data line L0 is represented by a data strobe signal DQS-Pre, and a data strobe signal transferred through the data line L1 or L2 is represented by a data strobe signal DQS-Post.

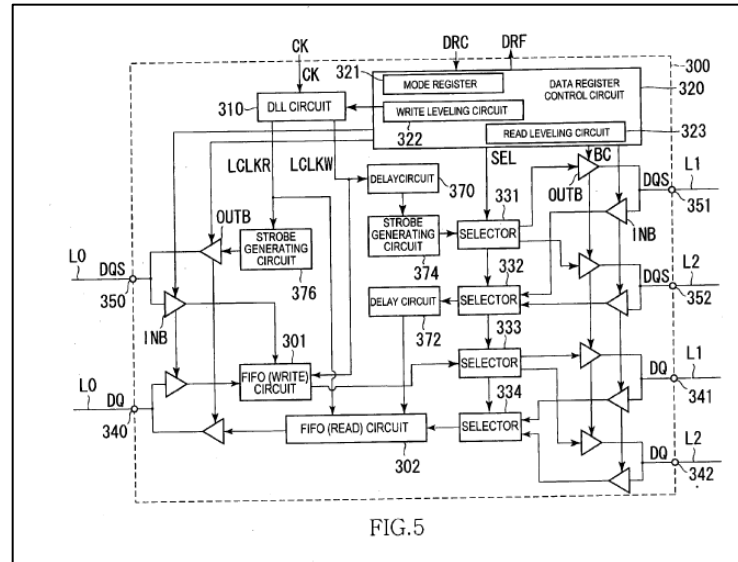
Although the data DQ-Pre and the data DQ-Post have the same content, because the data DQ is buffered by the data register buffer 300, the timing is off between the data DQ-Pre and the data DQ-Post. The same is true for a relationship between the data strobe signal DQS-Pre and the data strobe signal DQS-Post. Therefore, in the present embodiment, it is required to perform a timing adjustment between the memory chips 200 and the data register buffer 300 and a timing adjustment between the data register buffer 300 and the

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	memory controller in a separate manner. Details on the timing adjustments will be described later. As described above, in the present embodiment, the four memory chips 200 are allocated to a single data register buffer 300. The four memory chips 200 are memory chips that constitute different Ranks from each other, which are exclusively activated by the chip select (CS) signal or the clock enable (CKE) signal included in the control signal CTRL. The address signal ADD and the command signal CMD are commonly supplied to the four memory chips 200. The address signal ADD, the command signal CMD, the control signal CTRL, and the clock signal CK supplied to the memory chips 200 are supplied from the command/address/control register buffer 400. The control signal DRC supplied to the data register buffer 300 is also supplied from the command/address/control register buffer 400. As shown in FIG. 7, the command/address/control connectors 130 and the command/address/control register buffer 400 are connected to each other with the command/address/control line L3, the command/address/control register buffer 400 and the data register buffer 300 are connected to each other with a control line L4, and the command/address/control register buffer 400 and the memory chips 200 are connected to each other with a command/address/control line L5. In FIG. 7, a command/address/control signal transferred through the command/address/control line L3 is represented by a command/address signal ADD/CMD-Pre, and a command/address signal transferred through the command/address/control line L5 is represented by a command/address signal ADD/CMD-Post. Similarly, a control signal transferred through the command/address/control line L3 is represented by a control signal CNTRL-Pre, and a control signal transferred through the command/address/control line L5 is represented by a control signal CNTRL-Post. The clock signal CK to be supplied to the memory chip 200 and the data register buffer 300 is supplied from the command/address/control register buffer 400. In FIG. 7, a clock signal transferred through the command/address/control line L3 is represented by a clock signal Clock-Pre, and a clock signal transferred through the command/address/control line L5 is represented by a clock signal Clock-Post.” Hiraishi at [0103-0108].
1[d2] the each respective buffer circuit including a data path corresponding to each data signal line in the respective set	Based on Netlist’s apparent view of the scope of the ’608 patent claims, as articulated in its Infringement Contentions and which I disagree with, it is my opinion that Hiraishi alone or in view of the knowledge of a POSITA or in combination with the referenced prior art discloses element 1[d2]. See claim limitation 1[d1] analysis above.

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of data/strobe signal lines, and a command processing circuit configured to decode the module control signals and to control the data path in accordance with the module control signals and the module clock signal,	For example, Hiraishi discloses each buffer circuit including a data path corresponding to each data signal line in the respective set of data/strobe signal lines (e.g., between DQS on L0 and DQS on L1/L2, and between DQ on L0 and DQ on L1/L2 in Fig. 5). Hiraishi discloses each buffer circuit further including a command processing circuit (e.g., Data Register Control Circuit 320 and logic in DLL Circuit 310) configured to decode the module control signals (e.g., DRC) and to control the data path in accordance with the module control signals (e.g., DRC) and the module clock signal (e.g., CK). “A single data register buffer 300 is allocated for every four memory chips 200, as described above, so that nine data register buffers 300 are arranged along the X direction, which is the long side. The data register buffer 300 is a chip for buffering write data that is transferred via a data line L0 and outputting the write data to either one of the data lines L1 and L2, and at the same time, buffering read data that is transferred via either one of the data lines L1 and L2 and outputting the read data to the data line L0. The data line L0 is also formed inside the module substrate 110. With the above configuration, the single data register buffer 300, the data connectors 120 and the four memory chips 200 corresponding to the data register buffer 300 constitute a group G. The memory chips 200, the data register buffer 300, and the data connectors 120 included in the same group are arranged along the Y direction, which is the short side, and a plurality of groups G formed in the above manner are arranged along the X direction, which is the long side. Therefore, a relative positional relationship between each of the data register buffers 300 and corresponding four memory chips 200 becomes constant in all the groups G.” Hiraishi at [0055-0056]. “An operation of the data register buffer 300 is controlled based on the control signal supplied from the command/address/control register buffer 400. Details on the data register buffer 300 will be described later.” Hiraishi at [0058]. “The command/address/control register buffer 400 receives the command signal, the address signal, the control signal, and the clock signal (in some cases, collectively referred to as a command/address/control signal and the like) that are supplied from the command/address/control connectors 130 through an input terminal 401, buffers the signals, and supplies the signals to the memory chips 200. At the same time, the command/address/control register buffer 400 generates a control signal. The command/address/control signal to be supplied to the memory chips 200 are output through an output terminal 402, and the control signal to be supplied to the data register buffers 300 are output through an output terminal 403.” Hiraishi at [0060].

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	“The output terminal 402 is provided at each of the left side and the right side of the command/address/control register buffer 400. For example, the output terminal 402 at the left side is commonly connected to the memory chips 200-0 to 200-19 except for a control signal that is used to select the Rank. That is, the command signal, the address signal, and the clock signal are commonly supplied to the memory chips 200-0 to 200-19. Similarly, the output terminal 403 is provided at each of the left side and the right side of the command/address/control register buffer 400. For example, the output terminal 403 at the left side is commonly connected to the data register buffers 300-0 to 300-4, so that the generated control signal is commonly supplied to the data register buffers 300-0 to 300-4.” Hiraishi at [0061]. “On a signal path between the memory controller 12 and the memory chips 200, there exist a line 23 formed on the motherboard 21 and the data line L0 and the command/address/control line L3 formed on the module substrate 110. However, as described above referring to FIG. 1, in the memory module 100 according to the present embodiment, because the data register buffer 300 is connected to the data line L0, the memory controller 12 cannot experience the load capacity of the memory chips 200 that exist on the signal path beyond the data register buffer 300. Similarly, because the command/address/control register buffer 400 is connected to the command/address/control line L3, the memory controller 12 cannot experience the load capacity of the memory chips 200 that exist on the signal path beyond the command/address/control register buffer 400. Therefore, the load capacity of the signal path that connects the memory controller 12 and the memory module 100 is reduced, making it possible to ensure an excellent signal quality even with a high data transfer rate.” Hiraishi at [0069]. “The memory chip 200 is a DRAM, which includes, as shown in FIG. 4, a clock terminal 201, a command terminal 202, a control terminal 206, an address terminal 203, a data input/output terminal 204, and a data strobe terminal 205 as external terminals. Among these terminals, the clock terminal 201, the command terminal 202, the control terminal 206, and the address terminal 203 are connected to the command/address/control register buffer 400 via a command/address/control line L5 shown in FIG. 1. The data input/output terminal 204 and the data strobe terminal 205 are connected to the data register buffer 300 via the data line L1 or the data line L2 shown in FIG. 1. Although not shown

in FIG. 1, the memory chip **200** further includes other terminals such as a power supply terminal.” Hiraishi at [0073].



Hiraishi at Fig. 5.

“FIG. 5 is a block diagram of the configuration of the data register buffer **300**. As shown in FIG. 5, the data register buffer **300** includes a FIFO (Write) circuit **301** and a FIFO (Read) circuit **302**. The FIFO (Write) circuit **301** buffers data DQ that is supplied via an input/output terminal **340** with a data strobe signal DQS that is supplied via an input/output terminal **350**. The FIFO (Read) circuit **302** buffers data DQ that is supplied via an input/output terminal **341** or **342** with a data strobe signal DQS that is supplied via an input/output terminal **351** or **352**. A strobe generating circuit **376** generates a data strobe signal DQS to be supplied to the data connectors **120**, in synchronization with an internal clock LCLKR that is generated by a DLL circuit **310**. A strobe generating circuit **374** generates a data strobe signal DQS to be supplied to the memory chip **200**, in synchronization with an internal clock LCLKW that is generated by the DLL circuit **310**.

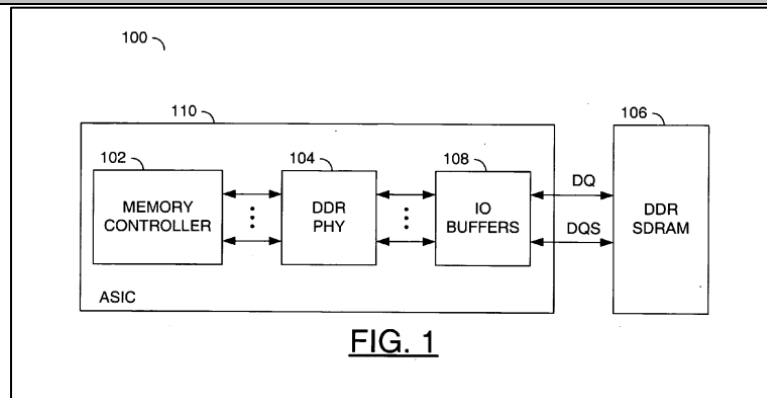
The FIFO circuits **301** and **302** shown in FIG. 5 are circuits that perform input and output of 1-bit data, so that in an actual case, the number of sets of the FIFO circuits **301** and **302** as many as a width of input/output data are provided. In the present embodiment, because a single data register buffer **300** inputs and outputs 1-byte data, 8 sets of the FIFO circuits **301** and **302** are required.” Hiraishi at [0083-0085].

“In this manner, the data register buffer **300** buffers the write data that is transferred via the data line L0 and outputs the write data to either one of the data lines L1 and L2, and buffers the read data that is transferred via either one

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	of the data lines L1 and L2 and outputs the read data to the data line L0. Because the data register buffer 300 only performs the buffering of the data, transfer rates of the write data and the read data that are transferred via the data line L0 and transfer rates of the write data and the read data that are transferred via the data lines L1 and L2 are equal to each other. Therefore, the data register buffer 300 can be implemented with a chip that is provided at relatively low cost instead of an expensive chip such as an AMB used in a Fully Buffered memory module.” Hiraishi at [0092-0093]. “The control signal generating circuit 430 is a circuit that generates the control signal DRC to be supplied to the data register buffer 300 based on the command/address/control signal supplied via the input terminal 401, of which an operation is performed in synchronization with the internal clock LCLKCA. The control signal DRC for the data register buffer 300 is supplied to the data register buffer 300 via the output terminal 403. The feedback signal DRF is supplied to the control signal generating circuit 430 from the data register buffer 300 via the input terminal 404. The control signal DRC includes signals such as a signal indicating a direction of transmitting and receiving data, a signal for controlling an ODT timing at the data line L0 side of the data register buffer 300, a signal for controlling an ODT timing at the data lines L1 and L2 side, a signal for controlling on and off of the DLL circuit, a signal for controlling enable and disable of the data register buffer 300, and a signal for performing a mode switching of the data register buffer 300 and a mode register set and the like. A separate line can be allocated to each of these signals, or a single common line can be allocated to a plurality of these signals. Alternatively, these signals can be transmitted to the data register buffer 300 as commands.” Hiraishi at [0099-0100]. FIG. 7 Hiraishi at Fig. 7.

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	“As shown in FIG. 7, in the present embodiment, the data register buffer 300 intervenes between the data connectors. 120 and the memory chips 200. The data connectors 120 and the data register buffer 300 are connected to each other with the data line L0, and the data register buffer 300 and the memory chips 200 are connected to each other with the data line L1 or L2. In FIG. 7, a plurality of data transferred through the data line L0 is represented by data DQ-Pre, and a plurality of data transferred through the data lines L1 and L2 is represented by data DQ-Post. Similarly, a data strobe signal transferred through the data line L0 is represented by a data strobe signal DQS-Pre, and a data strobe signal transferred through the data line L1 or L2 is represented by a data strobe signal DQS-Post. Although the data DQ-Pre and the data DQ-Post have the same content, because the data DQ is buffered by the data register buffer 300, the timing is off between the data DQ-Pre and the data DQ-Post. The same is true for a relationship between the data strobe signal DQS-Pre and the data strobe signal DQS-Post. Therefore, in the present embodiment, it is required to perform a timing adjustment between the memory chips 200 and the data register buffer 300 and a timing adjustment between the data register buffer 300 and the memory controller in a separate manner. Details on the timing adjustments will be described later. As described above, in the present embodiment, the four memory chips 200 are allocated to a single data register buffer 300. The four memory chips 200 are memory chips that constitute different Ranks from each other, which are exclusively activated by the chip select (CS) signal or the clock enable (CKE) signal included in the control signal CTRL. The address signal ADD and the command signal CMD are commonly supplied to the four memory chips 200. The address signal ADD, the command signal CMD, the control signal CTRL, and the clock signal CK supplied to the memory chips 200 are supplied from the command/address/control register buffer 400. The control signal DRC supplied to the data register buffer 300 is also supplied from the command/address/control register buffer 400. As shown in FIG. 7, the command/address/control connectors 130 and the command/address/control register buffer 400 are connected to each other with the command/address/control line L3, the command/address/control register buffer 400 and the data register buffer 300 are connected to each other with a control line L4, and the command/address/control register buffer 400 and the memory chips 200 are connected to each other with a command/address/control line L5. In FIG. 7, a command/address/control signal transferred through the command/address/control line L3 is represented by a command/address signal ADD/CMD-Pre, and a command/address signal transferred through the

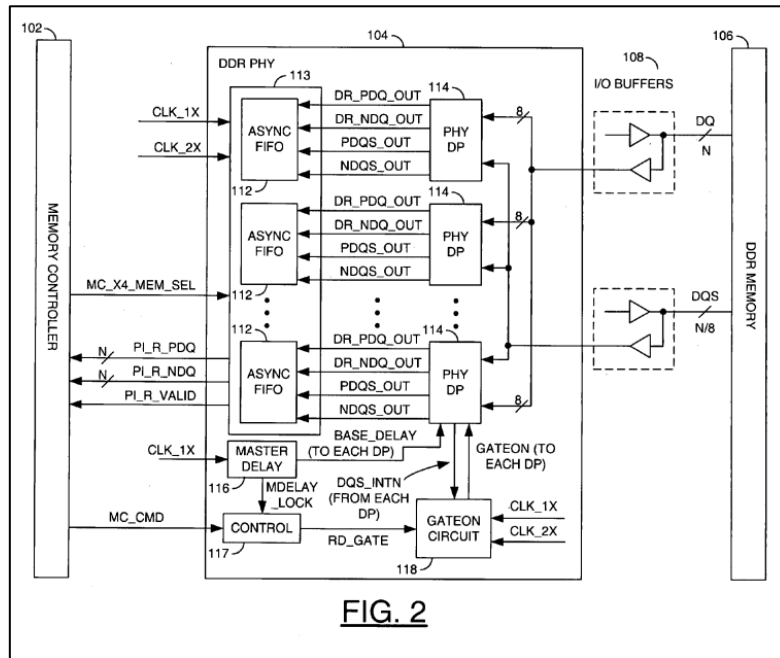
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	command/address/control line L5 is represented by a command/address signal ADD/CMD-Post. Similarly, a control signal transferred through the command/address/control line L3 is represented by a control signal CNTRL-Pre, and a control signal transferred through the command/address/control line L5 is represented by a control signal CNTRL-Post. The clock signal CK to be supplied to the memory chip 200 and the data register buffer 300 is supplied from the command/address/control register buffer 400. In FIG. 7, a clock signal transferred through the command/address/control line L3 is represented by a clock signal Clock-Pre, and a clock signal transferred through the command/address/control line L5 is represented by a clock signal Clock-Post.” Hiraishi at [0103-0108]. “As shown in FIGS. 8A and 8B, the 1-bit data is transferred via a predetermined connector 121 of the data connectors 120. The connector 121 is connected to the data register buffer 300 via a single data line L0. As explained above referring to FIG. 5, in the present embodiment, two data lines L1 and L2 are allocated to a single data line Lo. Specifically, the data line L1 is commonly connected to the memory chips 200-0 and 200-1, and the data line L2 is commonly connected to the memory chips 200-2 and 200-3. With the above configuration, the load capacity of a single data line L1 or L2 is reduced, the number of branch points decreases, and a line length from a branch point is shortened. As a result, the signal quality of data transferred on the data lines L1 and L2 is enhanced. Specifically, terminals connected to the single data line L1 are only three terminals total including data input/output terminals of the memory chips 200-0 and 200-1 and a data output terminal of the data register buffer 300. Furthermore, because the memory chips 200-0 and 200-1 are arranged facing each other across the module substrate 110, as shown in FIG. 8A, if a branch point P is arranged in an area sandwiched by the memory chips 200-0 and 200-1, the line length from the branch point to each of the memory chips 200-0 and 200-1 is considerably shortened. In addition, because the memory chips 200-0 to 200-3 are mounted at positions close to each other, a perspective difference in edges of the memory chips 200-0 to 200-3 is also suppressed to the minimum.” Hiraishi at [0110-0111]. To the extent that this limitation is not present in Hiraishi, which I believe it is, it would have been obvious in view of Butt. Butt discloses circuit 104 between memory controller 102 and DDR memory 106 that buffers data and includes a data path (e.g., signal path). Circuit 104 includes a command processing circuit configured to decode control signals and control the data path in accordance with the control signals and the clock signal.



Butt at Fig. 1.

“Referring to FIG. 1, a block diagram is shown illustrating a system 100 in which one or more preferred embodiments of the present invention may be implemented. In one example, the system 100 may comprise a circuit (or block) 102, a circuit (or block) 104, a circuit (or block) 106 and a circuit (or block) 108. The circuit 102 may be implemented as a memory controller. The circuit 104 may be implemented as a memory interface. In one example, the circuit 104 may be implemented as a double data rate (DDR) physical layer (PHY) core. The circuit 106 may be implemented as one or more double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices. The circuit 108 may be implemented, in one example, as stub series terminated logic (SSTL) IO buffers. The circuit 104 may be coupled between the circuit 102 and the circuit 106. In one example, the circuit 104 may be coupled to the circuit 106 by the circuit 108. The circuit 104 may be configured to receive a plurality of data signals (e.g., DQ) and a plurality of read data strobe signals (e.g., DQS). In one example, the plurality of read data strobe signals may comprise a single read data strobe for each byte of the signals DQ. In another example (e.g., an x4 mode), the plurality of data strobe signals DQS may comprise a separate strobe signal (e.g., DQS_UN and DQS_LN, respectively) for each nibble (e.g., upper and lower) of the signal DQ. In one example, the circuits 102, 104 and 108 may be implemented (or instantiated) on an application specific integrated circuit (ASIC) 110. However, the circuit 102 may be implemented separately and mounted on a common printed circuit board (PCB) along with the circuits 104, 106 and 108. The ASIC 110 may be implemented, in one example, as a platform (or structured) ASIC. In one example, the circuit 104 may be implemented based on diffused datapath (DP) and master delay modules. In another example, the circuit 104 may be implemented based on R-cell datapath and master delay modules. In one example, the circuit 104 may be implemented in an R-cell transistor fabric of the ASIC 110. As used herein, R-cell generally refer to an area of silicon containing one or more diffusions for forming the parts of N and/or P type transistors and the contact points where wires may be attached in subsequent manufacturing steps (e.g., to power, ground, inputs and outputs). Wire layers may be added to the R-cell transistor fabric to make

particular transistors, logic gates, soft and firm IP blocks and/or storage elements.” Butt at [0015-0016].



Butt at Fig. 2.

“Referring to FIG. 2, a more detailed block diagram of the circuit 104 is shown illustrating example read data logic and signal paths in which a preferred embodiment of the present invention may be implemented. In one example, the circuit 104 may comprise a number of asynchronous (ASYNC) first-in first-out (FIFO) buffers 112, FIFO synchronization logic 113, a number of physical read datapaths (DPs) 114, a master delay (MDELAY) logic 116, a control logic 117 and a programmable gating signal generator 118. Each of the physical read datapaths 114 may be configured to receive (i) a respective portion of the read data signals DQ from the DDR memory 106, (ii) a respective read data strobe signal or signals DQS associated with the respective portion of the received read data signals and (iii) a gating signal (e.g., GATEON) from the programmable gating signal generator 118. Each of the physical read datapaths 114 may communicate with a corresponding one of the asynchronous FIFOs 112 via a number of signals (e.g., DR_PDQ_OUT, DR_NDQ_OUT, PDQS_OUT, and NDQS_OUT). In one example, separate signals (e.g., PDQS_OUT_UN, NDQS_OUT_UN, PDQS_OUT_LN, and NDQS_OUT_LN) may be generated for each nibble of the DPs 114. In one example, the asynchronous FIFOs 112 may be configured to interface the physical read datapaths 114 with the memory controller 102. In general, the signals DQ and DQS may be presented to the DDR PHY 104 on a number of buses. The signals DQ and DQS may be broken out to multiple instantiations of DP hardmacros. The DPs may be configured via internal settings to delay the read data strobe

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	signals DQS based on one or more control signals (or values) from the MDELAY circuit 116. Each of the DPs 114 may be configured to present the DQ data to a respective asynchronous FIFO 112 via the signals DR_PDQ_OUT and DR_NDQ_OUT, after the data is sampled using the delayed read data strobe signals DQS. The FIFOs 112 are generally configured to transfer the read data DQ from the read data strobe (or DQS) domain to the CLK_1X domain for presentation to the memory controller 102. The read data DR_PDQ_OUT and DR_NDQ_OUT are generally written to the FIFOs 112 in response to (e.g., clocked by) the signals PDQS_OUT and NDQS_OUT, respectively). The memory controller 102 may be configured to read the data DQ (e.g., via signals PI_R_PDQ and PI_R_NDQ) from the FIFOs 112 in response to the clock signal CLK_1X. In one example, the FIFOs 112 may be implemented as eight words deep. As briefly described above, the read datapaths 114 are generally programmable from when the data/strobe pairs DQ/DQS are received at the input to the circuit 104, to sampling the read data with the read data strobe signal DQS, and passing the data to the memory controller 102. The programmability of the read datapaths 114 generally provides flexibility for handling different column address strobe (CAS) latencies, burst lengths, device process variation, and/or propagation delays.” Butt at [0017-0020]. “The master delay (MDELAY) logic 116 is generally configured to calculate a delay value for generating a one-quarter cycle or one-fifth cycle delay with respect to the device reference clock (e.g., the signal CLK_1X). The calculated delay is generally used by the datapaths 114 to center a read data capture clock (e.g., the signal DQS) in a valid DDR device read data window. The calculated delay generally tracks process, voltage and temperature (PVT) corners for reliable read data latching. The MDELAY logic 116 may be configured to generate the one-quarter cycle or one-fifth cycle delay using a delay lock loop (DLL). Once the DLL is locked to the clock signal CLK_1X, a signal (e.g., MDELAY_LOCK) may be generated indicating the locked state. The signal MDELAY_LOCK may be presented to an input of the control logic 117 and/or the memory controller 102. The MDELAY logic 116 may be configured to generate one or more control signals (or values) for transferring the delay settings (or values) to one or more slave delay cells (describe in more detail in connection with FIGS. 3A and 3B) in each of the DPs 114. The delay values, when transferred to each of the DPs 114, are generally referred to as base delays. In one example, a base delay may be implemented for each nibble of each DP byte. For example, a first base delay value (e.g., BASE_DELAY_UN) may be implemented for each upper nibble and a second base delay value (e.g., BASE_DELAY_LN) may be implemented for each lower nibble. The DPs 114 may also be programmed with offset delay values corresponding to each nibble (e.g., OFFSET_P_UN, OFFSET_N_UN, OFFSET_P_LN and OFFSET_N_LN). In one example, each of the DPs 114 may have a set of base delays that are independent of the other DPs 114. The offset delay values may

be added to or subtracted from the respective base delay values. The control circuit 117 may be configured to generate one or more control signals for controlling and/or configuring the FIFOs 112 and datapaths 114. In one example, the control circuit 117 may be configured to generate a gating signal (e.g., RD_GATE) in response to a signal (e.g., MC_CMD) received from the controller 102. In one example, the circuit 117 may be configured to generate the signal RD_GATE in response to decoding a READ command in the signal MC_CMD. The signal RD_GATE is generally configured to prevent invalid states (e.g., when DQS is in a 3-state, or OFF, mode) from entering the circuit 113. The signal RD_GATE may be used to generate one or more gating signals. The programmable gateon generating circuit 118 may be configured to generate the signal GATEON in response to the signal RD_GATE, a first clock signal (e.g., CLK_1X), a second clock signal (e.g., CLK_13_2X) and a data strobe signal (e.g., DQS_INTN) received from the DPs 114. The signal GATEON may be used to gate the read data strobe signal DQS received from the memory device 106. In one example, separate gating signals (e.g., GATEON_UN, GATEON_LN, etc.) may be generated for each nibble of the DPs 114. The signal DQS_INTN may be used to de-assert the signal GATEON. In one example, separate signals (e.g., DQS_INTN_UN and DQS_INTN_LN) may be generated for each nibble of the DPs 114. Although the circuit 118 is shown implemented separately from the DPs 114, it will be understood by those skilled in the art that the circuit 118 may be implemented as part of the DPs 114 (e.g., the signal GATEON may be generated within the DPs 114 or external to the DPs 114).” Butt at [0021-0024].

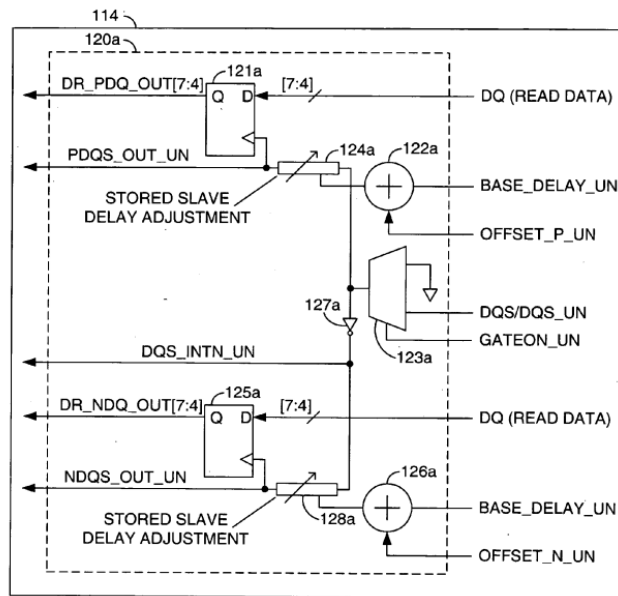


FIG. 3A

Butt at Fig. 3A.

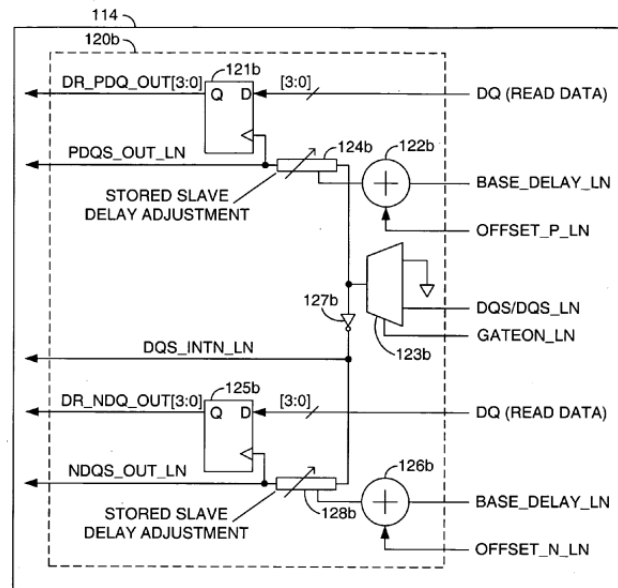


FIG. 3B

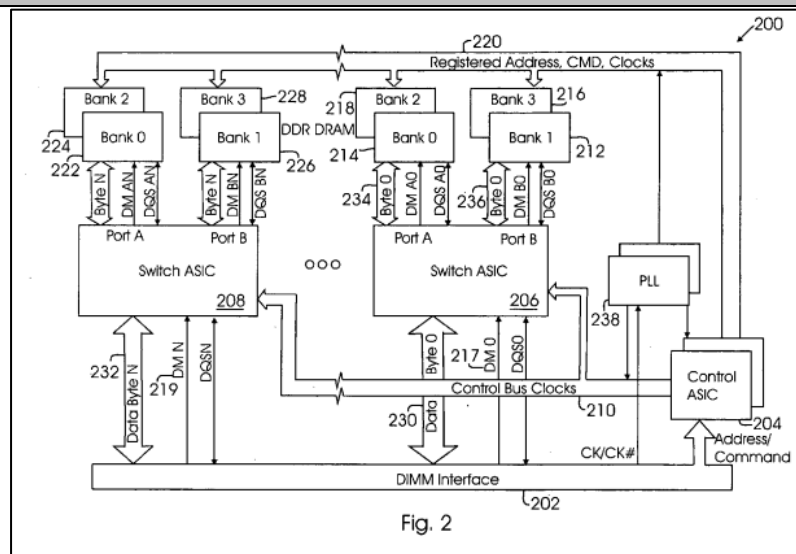
Butt at Fig. 3B.

“Referring to FIGS. 3(A-B), more detailed block diagrams of a datapath 114 of FIG. 2 are shown illustrating an example read data latching and gating circuit in accordance with a preferred embodiment of the present invention. In one example, each datapath 114 may comprise an upper nibble pathway 120 a (FIG. 3A) and a lower nibble pathway 120 b (FIG. 3B). The upper nibble pathway 120 a may have a first input that may receive a number of bits of the signal DQ (e.g., bits 7:4), a second input that may receive the signal BASE_DELAY_UN, a third input that may receive the signal OFFSET_P_UN, a fourth input that may receive the signal OFFSET_N_UN, a fifth input that may receive the signal DQS (or the signal DQS_UN in the x4 mode), a sixth input that may receive a signal (e.g., GATEON_UN). The upper nibble pathway 120 a may also have a first output that may present a number of bits (e.g., the signal DR_PDQ_OUT[7:4]), a second output that may present a number of bits (e.g., the signal DR_NDQ_OUT[7:4]), a third output that may present a signal (e.g., PDQS_OUT_UN), a fourth output that may present a signal (e.g., NDQS_OUT_UN) and a fifth output that may present a signal (e.g., DQS_INTN_UN).” Butt at [0025].

“The upper nibble pathway 120 a may comprise a circuit (or block) 121 a, a circuit (or block) 122 a, a circuit (or block) 123 a, a circuit (or block) 124 a, a circuit (or block) 125 a, a circuit (or block) 126 a, a circuit (or block) 127 a and a circuit (or block) 128 a. The circuit 121 a may be implemented as one or more registers. The circuit 122 a may be implemented as an adder block. The circuit

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	123 a may be implemented as a multiplexer circuit. The circuit 124 a may be implemented as a slave delay adjustment block. The circuit 125 a may be implemented as one or more registers. The circuit 126 a may be implemented as an adder block. The circuit 127 a may be implemented as an inverter circuit. The circuit 128 a may be implemented as a slave delay adjustment block. The circuit 121 a may be configured to latch an upper nibble (e.g., bits 7:4) of the read data signal DQ in response to a clock input. The circuit 121 a may be further configured to present the latched read data as the signal DR_PDQ_OUT[7:4]. The circuit 122 a may be configured to generate a sum (or difference) of the signals BASE_DELAY_UN and OFFSET_P_UN. The circuit 123 a may be configured to select either the signal DQS (or the signal DQS_UN in the x4 mode) or a predetermined logic level (e.g., a LOW or logic 0) in response to the signal GATEON_UN. The circuit 124 a may be configured to delay the signal presented by the circuit 123 a based on the sum (or difference) generated by the circuit 122 a. An output of the circuit 124 a may present the signal PDQS_OUT_UN to the clock input of the circuit 121 a and the third output of the upper nibble pathway 120 a. The circuit 125 a may be configured to latch an upper nibble (e.g., bits 7:4) of the read data signal DQ in response to a clock input. The circuit 125 a may be further configured to present the latched read data as the signal DR_NDQ_OUT[7:4]. The circuit 126 a may be configured to generate a sum (or difference) of the signals BASE_DELAY_UN and OFFSETN_UN. The circuit 127 a may be configured to generate the signal DQS_INTN_UN as a digital complement of the signal presented by the circuit 123 a. The signal DQS_INTN_UN may be presented to an input of the circuit 128 a and the fifth output of the upper nibble pathway 120 a. The circuit 128 a may be configured to generate the signal NDQS_OUT_UN by delaying the signal DQS_INTN_UN based on the sum (or difference) generated by the circuit 126 a. An output of the circuit 128 a may present the signal NDQS_OUT_UN to the clock input of the circuit 125 a and the fourth output of the upper nibble pathway 120 a.” Butt at [0026-0028]. “The lower nibble pathway 120 b may have a first input that may receive a number of bits (e.g., bits 3:0) of the signal DQ, a second input that may receive the signal BASE_DELAY_LN, a third input that may receive the signal OFFSET_P_LN, a fourth input that may receive the signal OFFSET_N_LN, a fifth input that may receive the signal DQS (or the signal DQS_LN in the x4 mode), a sixth input that may receive a signal (e.g., GATEON_LN). The lower nibble pathway 120 b may also have a first output that may present a number of bits (e.g., the signal DR_PDQ_OUT[3:0]), a second output that may present a number of bits (e.g., the signal DR_NDQ_OUT[3:0]), a third output that may present the signal PDQS_OUT_LN, a fourth output that may present the signal NDQS_OUT_LN and a fifth output that may present the signal DQS_INTN_LN. The lower nibble pathway 120 b may comprise a circuit (or block) 121 b, a circuit (or block) 122 b, a circuit (or block) 123 b, a circuit (or block) 124 b, a circuit (or block) 125 b, a circuit (or block) 126 b, a circuit (or

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	block) 127 b and a circuit (or block) 128 b. The circuit 121 b may be implemented as one or more registers. The circuit 122 b may be implemented as an adder block. The circuit 123 b may be implemented as a multiplexer circuit. The circuit 124 b may be implemented as a slave delay adjustment block. The circuit 125 b may be implemented as one or more registers. The circuit 126 b may be implemented as an adder block. The circuit 127 b may be implemented as an inverter circuit. The circuit 128 b may be implemented as a slave delay adjustment block. The circuit 121 b may be configured to latch a lower nibble (e.g., bits 3:0) of the read data signal DQ in response to a clock input. The circuit 121 b may be further configured to present the latched read data as the signal DR_PDQ_OUT[3:0]. The circuit 122 b may be configured to generate a sum (or difference) of the signals BASE_DELAY_LN and OFFSET_P_LN. The circuit 123 b may be configured to select either the signal DQS (or the signal DQS_LN in the x4 mode) or a predetermined logic level (e.g., a LOW or logic 0) in response to the signal GATEON_LN. The circuit 124 b may be configured to delay the signal presented by the circuit 123 b based on the sum (or difference) generated by the circuit 122 b. An output of the circuit 124 b may present the signal PDQS_OUT_LN to the clock input of the circuit 121 b and the third output of the lower nibble pathway 120 b. The circuit 125 b may be configured to latch a lower nibble (e.g., bits 3:0) of the read data signal DQ in response to a clock input. The circuit 125 b may be further configured to present the latched read data as the signal DR_NDQ_OUT[3:0]. The circuit 126 b may be configured to generate a sum (or difference) of the signals BASE_DELAY_LN and OFFSET_N_LN. The circuit 127 b may be configured to generate the signal DQS_INTN_LN as a digital complement of the signal presented by the circuit 123 b. The signal DQS_INTN_LN may be presented to an input of the circuit 128 b and the fifth output of the lower nibble pathway 120 b. The circuit 128 b may be configured to generate the signal NDQS_OUT_LN by delaying the signal DQS_INTN_LN based on the sum (or difference) generated by the circuit 126 b. An output of the circuit 128 b may present the signal NDQS_OUT_LN to the clock input of the circuit 125 b and the fourth output of the lower nibble pathway 120 b.” Butt at [0029-0032]. To the extent that this limitation is not present in Hiraishi and/or Butt, which I believe it is, it would have been obvious in view of Ellsberry.



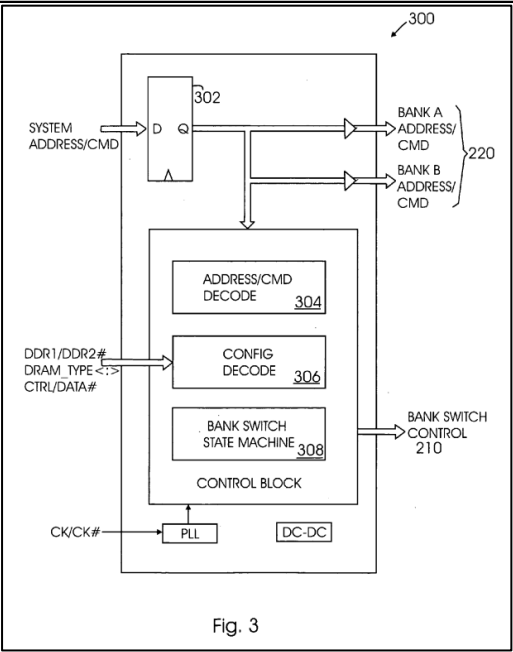
Ellsberry at Fig. 2.

“The invention relates to a device, system, and method for expanding the memory capacity of a memory module. A control unit and memory bank switch are mounted on a memory module or, alternately, on a system motherboard to selectively control write and read operations to/from memory devices communicatively coupled to the memory bank switch. By selectively activating or deactivating the memory devices in real-time, separate smaller-capacity memory devices may emulate a single larger-capacity memory device. That is, the invention expands the addressable memory capacity on a module by making two smaller-capacity memory devices emulate a single higher-capacity memory device. A state machine is used to send Read/Write commands to the intended memory bank while sending no-operation commands to the other memory bank. This permits maintaining multiple memory banks communicatively coupled to the data bus without device activation and termination cycle delays. One embodiment of the invention provides a system having a processor, a bus communicatively coupled to the processor to carry data to and from the processor, and memory sockets coupled to the bus. A memory module is coupled to a memory socket, the memory module including a control unit to receive memory address information from the bus, and a memory bank switch communicatively coupled to the control unit and the bus. The control unit maps a received logical address to a physical address corresponding to the particular memory bank configuration employed. It also directs commands to the memory banks to indicate which memory bank should be operational and which one should be passive (do nothing). The memory bank switch is designed to receive data information from the bus and direct the data information to a plurality of physical memory banks according to control signals from the control unit that maps one logical memory bank to a plurality of physical memory banks. The memory module further includes a plurality of memory devices coupled to the plurality of physical memory banks, the plurality of memory devices appearing

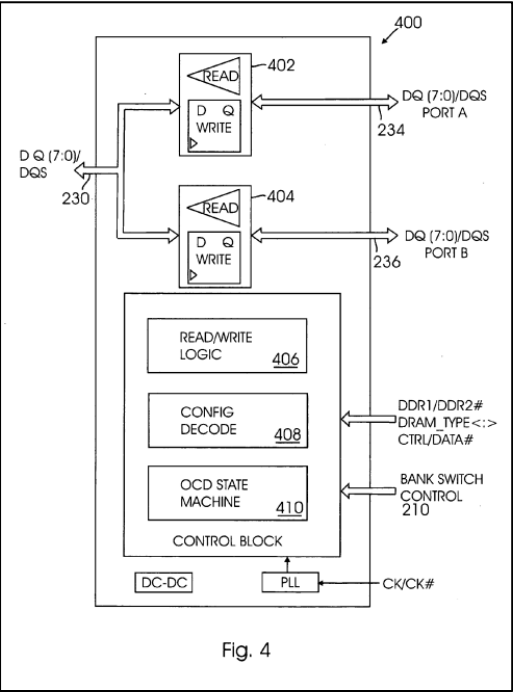
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	as a single memory device to the system processor. That is, the emulated single memory device has the capacity of the combined plurality of memory devices. The invention expands the memory capacity of a memory module by using a plurality of smaller-capacity memory devices that function as a single higher-capacity memory device. This is accomplished without the need to add more lines to the bus or any additional external signal. Moreover, the load on the bus is not increased because the memory bank switches present a single load to the bus, not the load of the individual memory devices coupled thereto. A control unit provides a state machine that controls the commands to a plurality of memory devices in multiple banks so as to read/write a single memory bank without the need to disconnect the other memory banks from the data bus.” Ellsberry at [0010-0012]. “FIGS. 7A-F illustrate an address mapping table, or bank switch state machine, that may be used by the control unit to map a received address (primary address space) to one of the memory banks (secondary address space) according to one embodiment of the invention. FIGS. 8A-B illustrate a command scheme for a control unit to operate multiple banks concurrently according to one embodiment of the invention.” Ellsberry at [0018-0019]. “One embodiment of the invention relates to a system that expands the memory capacity of a memory module without increasing the bus size. A controller and memory bank switch allow the use of separate smaller-capacity memory devices to emulate a single higher-capacity memory device to a host system. This effectively expands the number of addressable banks per memory module without the need for additional chip select lines on the main memory bus. For example, the invention expands the addressable memory banks on a module by making two smaller-capacity memory devices emulate a single higher-capacity memory device. In one implementation, the invention permits two separate SDRAM DDR devices to appear as a single higher-capacity SDRAM DDR device to a source device (e.g., microprocessor, memory controller, etc.).” Ellsberry at [0026]. “FIG. 2 illustrates a block diagram of a capacity-expanding memory system 200 according to one embodiment of the invention. In this embodiment of the invention, the capacity-expanding memory system 200 is communicatively coupled to a DIMM interface 202. The DIMM interface 202 may be coupled to a memory socket and communication bus over which data, memory addresses, commands, and control information are transmitted. The capacity-expanding feature of the invention is accomplished by a combination of a control unit 204 and one or more memory bank switches 206 & 208. The control unit 204 receives memory addresses and commands over the DIMM interface 202. In one embodiment of the invention, memory bank switches 206 & 208 receive data information from the DIMM interface 202 via data buses 230 & 232, respectively. The control unit 204 is communicatively coupled to the dual

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	memory bank switches 206 & 208 via a control bus 210 and indicates to the memory bank switches 206 & 208 how data from the DIMM interface 202 should be received and/or stored. According to one embodiment of the invention, the DIMM interface 202 provides a range of data bits simultaneously (e.g., Data Group 0 through Data Group N). A first data group (i.e., Data Group 0) is received by a first memory bank switch 206 while a second data group (i.e., Data Group N) is received by a second memory bank switch 208. Each memory bank switch 206 & 208 is communicatively coupled to a plurality of memory banks that may have one or more memory devices (e.g., dynamic random access memory (DRAM)). Data may be read from or written to these memory devices using any known addressing scheme (e.g., mapping memory addresses into a column and row). For example, memory bank switch 206 includes Port A and Port B, coupled to data busses 234 & 236 respectively, through which it sends and receives data information to and/or from four memory banks (i.e., Bank 0, Bank 1, Bank 2, and Bank 3). The four memory banks (i.e., Bank 0, Bank 1, Bank 2, and Bank 3) 212, 214, 216, and 218 are also communicatively coupled to an address bus 220 through which they receive address and command information from the control unit 204. Clocking information (Ck/Ck#) is received from the DIMM interface 202. An external phase lock loop (PLL) 238 regenerates a clock signal that can be used by the components on the memory system 200. The switch 208 may contain an internal PLL which derives the clock provided to the memory devices from the output of the external PLL 238. In one embodiment of the invention, the control unit 204 decodes a memory address received over the DIMM interface 202, determines to which memory bank the received address corresponds, and causes the memory bank switch 206 and 208 to activate the correct memory bank. For example, if the control unit 204 determines that a particular address is associated with, or mapped to, Bank 1 212 coupled to memory bank switch 206, then it causes Port B to be activated and Port A to be disabled so that the data is written to the correct memory bank 212. Additionally, each memory bank switch 206 and 208 includes signal drivers to drive data signals to and from the memory banks and to and from the DIMM interface 202. This reduces resistive and/or capacitive loading of the data bus coupled to the DIMM interface and the bus 110 while emulating a standard memory device interface. The control unit 204 may map a received address in a number of ways without departing from the invention. For instance, the control unit 204 may simply associate the lower memory addresses with Port A and higher memory addresses with Port B. Although address information may be sent to all memory banks over address bus 220, the memory bank switch 206 and/or control unit 204 determine which memory devices or banks are accessed (for either Read and/or Write operations, or other operations). The control unit 204 may implement a state machine that controls memory bank switches 206 and 208 thereby controlling which memory banks/devices coupled to Ports A and B are accessed. According to one embodiment of the invention, the operation of the switch 206/208 and control unit 204 will vary depending on the memory

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	addressing scheme (e.g., column or row addressing) implemented. In column mode operation, to meet system timing requirements, write-data is sent to both ports A and B of the switch 206/208 and control unit 204 uses the data mask (DM) signal to select the target memory device. That is, the DM signal indicates to which target memory device (e.g., Bank 0 214, Bank 1 212, Bank 2 218, or Bank 3 216) the data is written. Note that the DM signal 217/219 at the switch 206/208 is controlled by the control unit 204. Memory read operations, in column mode, work in a similar way as memory write operations. Both memory devices (e.g., Bank 0 214 and Bank 1 212), coupled to ports A and B, are read and the data from the selected target memory device is multiplexed onto the DIMM interface 202. That is, only the data read from the selected target memory device is sent to the DIMM interface 202. Alternatively, when row/bank mode addressing is used, read and write commands are sent only to the targeted memory device. A NOP (no-operation) command is sent to the non-targeted memory device. In one embodiment of the invention, a Serial Presence Detect (SPD) feature is implemented to collect and store the memory module configuration. The memory control configuration is communicated to the host system and stored. The memory module reports the total module memory capacity and data width along with the individual emulated memory device capacity that is formed by two or more small-capacity memory devices. The Serial Presence Detect operation is a standard feature of many DIMM modules.” Ellsberry at [0028-0034]. “In one embodiment of the invention, the control unit 204 is configurable via programmable pins (e.g., through logical pull-up or pull-down voltages, etc.) to have information about the type and size of memory devices coupled to the memory banks (e.g., Bank 0, Bank 1, Bank 2 and Bank 3). The control unit 204 is configured to recognize that a plurality of smaller-capacity memory devices is coupled to a particular memory bank switch. The control unit 204 then handles mapping the logical memory addresses it receives via the DIMM interface 202 to a corresponding bank for a particular memory bank coupled to the switches 206 and 208. This same principal is expanded when implementing a wider memory bus formed by several data groups composed of a plurality of memory bank switches and the associated memories.” Ellsberry at [0035].



Ellsberry at Fig. 3.



Ellsberry at Fig. 4.

Configuration	Primary Address Space	RC Mode INVERT	Mode	PHY Bank Select	Secondary Address Space
DDR I, 2 X 256M (x4)	BA 0h - 3h Row 0000h - 1FFFh Column 000h - FFFh	X	COLUMN	COL A(12)	BA 0h - 3h Row 0000h-1FFFh Column 000h-7FFh BA 0h - 3h Row 0000h-1FFFh Column 800h-FFFh
DDR I, 2 X 256M (x8)	BA 0h - 3h Row 0000h - 1FFFh Column 000h - 7FFh	X	COLUMN	COL A(11)	BA 0h - 3h Row 0000h-1FFFh Column 000h-3FFh BA 0h - 3h Row 0000h-1FFFh Column 400h-7FFh
DDR I, 2 X 512M (x4)	BA 0h - 3h Row 0000h - 3FFFh Column 000h - FFFh	X	ROW	ROW A(13)	BA 0h - 3h Row 0000h-1FFFh Column 000h-FFFh BA 0h - 3h Row 2000h-3FFFh Column 000h-FFFh

Fig. 7A

Ellsberry at Fig. 7A.

“FIGS. 7A-F illustrate an address mapping table, or bank switch state machine, that may be used by the control unit to map a received address (primary address space) to one of the memory banks (secondary address space) according to one embodiment of the invention. In this particular example, addresses are represented as memory rows and columns. Depending on the physical memory configuration detected, the control unit 204 selects a particular address bit (e.g., the most significant address column or row bit) from the received address to map to the memory banks. For example, where a DDR 1, 2×256 Megabyte (×4) configuration is used in the memory banks, the address bit corresponding to Column 12 is used to select a memory bank (banks on Port A or Port B). Also, where a DDR II, 2×1 Gigabyte (×8) configuration is used in the memory banks, the address bit corresponding to Row 14 is used to select a memory bank (banks on Port A or Port B). Thus, a primary space address received by the control unit 204 is mapped to a secondary space address corresponding to the memory banks.” Ellsberry at [0037].

“According to one embodiment of the invention, an application specific integrated circuit (ASIC) contains both the memory bank switch 206 and control unit 204 functions on a single die. This die is configurable to operate as either the memory bank switch 206 or the control unit 204 through a selection pin or pad. FIG. 3 illustrates a block diagram of an address and command processing system 300 for a capacity-expanding memory device according to one embodiment of the invention. This address and command processing system 300 may be implemented as part of the control unit 204. The command processing system 300 controls physical bank selection and bank switching direction. Memory addresses and command information are received from the DIMM interface 202, buffered in a register 302 and sent to all memory banks (e.g., Bank 0, Bank 1, Bank 2 and Bank 3) over address bus 220. The memory

'608 patent	35 U.S.C. §§ 102, 103 Analysis
	address and command information is also decoded 304 and memory configuration information 306 (e.g., DRAM type, etc.) is determined. The memory configuration information may be determined from preset information. A bank switch state machine 308 then determines which memory bank should be activated or accessed. In one embodiment of the invention, this state machine 308 is a logical translation table that maps a primary space address to a secondary space address based on the memory configuration present. For example, the state machine 308 may be the address mapping table illustrated in FIGS. 7A-F, which was previously described. The state machine 308 sends control information to the memory bank switches 206 & 208 via the control bus 210 to indicate which memory banks should be activated/deactivated or accessed.” Ellsberry at [0038-0039]. “In one embodiment of the invention, the control unit 204 maps one logical memory bank to two physical memory banks. This is accomplished by selectively enabling or activating one of the two physical memory banks (e.g., either Port A or Port B) while disabling or deactivating the other. In this manner, only one of the two physical memory banks is written to or read from. This scheme permits the operating system to generate memory addresses for a single, larger-capacity memory device while the control unit 200 maps that memory address to a plurality of smaller-capacity memory devices. Thus, the control unit 204 is able to map one logical memory bank to a plurality of physical memory banks. One embodiment of the invention provides a novel scheme for performing operations in a first memory bank (i.e., Port A in FIG. 2) without disabling or deactivating a second memory bank (i.e., Port B in FIG. 2). This scheme permits the memory bank switch 206 to operate in real-time and without noticeable delays. For example, in one implementation of the invention, the control unit 204 (FIG. 2) operates to send commands or instructions to two or more memory banks (e.g., Ports A & B) concurrently. That is, the control unit 204 sends the intended instruction to the selected memory bank and sends a no-op (no operation) instruction to the other memory bank(s).” Ellsberry at [0040-0041].

Command	Mode	Addr	P Bank	DDR A		DDR B	
				Command	Addr	Command	Addr
MRS	X	X	X	MRS	1	MRS	1
EMRS	X	X	X	EMRS	2	EMRS	2
REFRESH	X	X	X	REFRESH	X	REFRESH	X
SELF REFRESH ENTRY	X	X	X	SLF REFRESH ENTRY	X	SLF REFRESH ENTRY	X
SELF REFRESH EXIT	X	X	X	SLF REFRESH EXIT	X	SLF REFRESH EXIT	X
SINGLE BANK PRECHARGE	Col	X	X	SB PRECHG	X	SB PRECHG	X
	Row/ Bank	X	A	SB PRECHG	X	NOP	X
			B	NOP	X	SB PRECHG	X
ALL BANK PRECHARGE	X	X	X	AB PRECHG	X	AB PRECHG	X
ACTIVATE	Col	X	X	ACTIVATE	X	ACTIVATE	X
	Row/ Bank	X	A	ACTIVATE	X	NOP	X
			B	NOP	X	ACTIVATE	X
WRITE	X	X	A	WRITE	X	NOP	X
			B	NOP	X	WRITE	X
WRITE WITH AUTO PRECHARGE	Row/ Bank	X	A	WRITEAP	X	NOP	X
			B	NOP	X	WRITEAP	X
	Col	X	X	WRITEAP	X	WRITEAP	X
READ	X	X	A	READ	X	NOP	X
			B	NOP	X	READ	X
READ WITH AUTO PRECHARGE	Row/ Bank	X	A	READAP	X	NOP	X
			B	NOP	X	READAP	X
	Col	X	X	READAP	X	READAP	X

(a) (b) (c) (d) (e) (f) (g) (h) (i)

Fig. 8A

Ellsberry at Fig. 8A.

(a)	(b)	(c)	(d)	(e)	(f)	(g)	(h)	(i)
BURST TERM	Row/ Bank	X	A	BURST_TERM	X	NOP	X	
			B	NOP	X	BURST_TERM	X	
	Col	X	X	BURST_TERM or NOP based upon last write bank	X	BURST_TERM or NOP based upon last write bank	X	
NOP	X	X	X	NOP	X	NOP	X	
DEVICE DESELECT	X	X	X	DEVICE DESELECT	X	DEVICE DESELECT	X	
POWER DOWN ENTRY	X	X	X	PWR DOWN ENTRY	X	PWR DOWN ENTRY	X	
POWER DOWN EXIT	X	X	X	PWR DOWN EXIT	X	PWR DOWN EXIT	X	

NOTES: 1. if cl_mode = subtract; cl = cl - 1 to DDRs

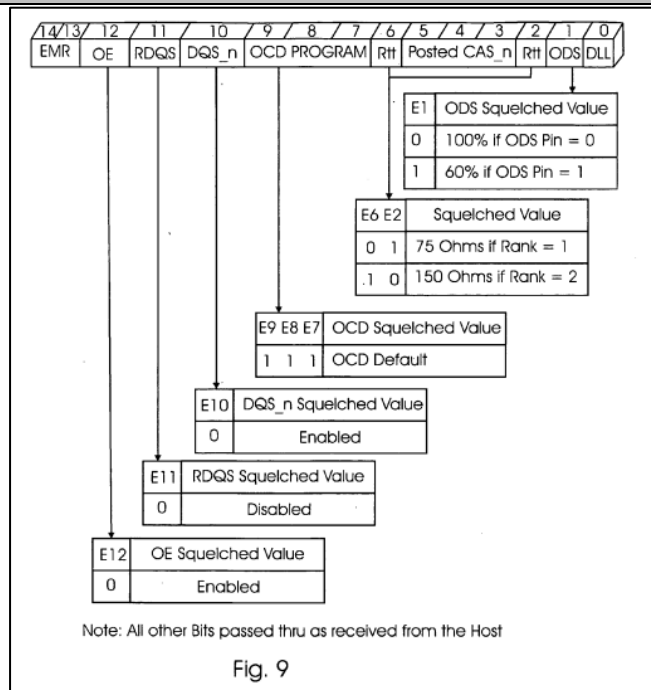
2. ods squelch-based on ODS setting, rtt squelch-based on REFF setting, ocd squelch-default, dqs_n enable, rdqs disable, out squelch - enable

3. A command consists of RAS_n, CAS_n, CS, WE_n, and A(10).

Fig. 8B

Ellsberry at Fig. 8B.

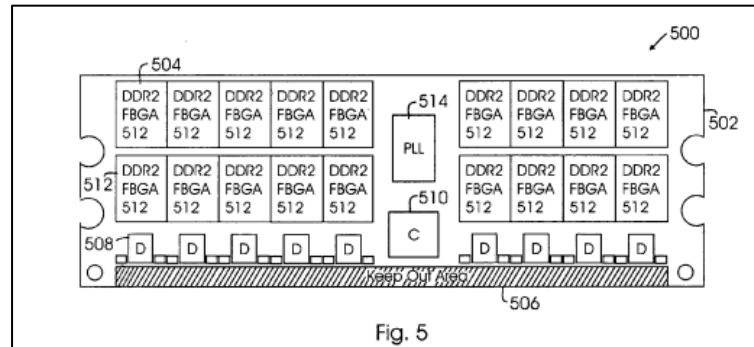
'608 patent	35 U.S.C. §§ 102, 103 Analysis
	“FIGS. 8A-B illustrate a command scheme for the switch/control unit combination to operate multiple banks concurrently according to one embodiment of the invention. In this implementation, two memory banks (i.e., DDR A and DDR B) are controlled by a control unit 204. An exemplary set of memory commands and/or operations are illustrated. Depending on which command is invoked and the memory addressing scheme used (e.g., column or row addressing), the control unit 204 operates to send either the same command to both memory banks (DDR A and DDR B) or different commands to each memory bank. For example, a “WRITE” command from the control unit 204 causes a “WRITE” operation to be sent to the intended memory bank (as determined by the address mapping) and a NOP command (no operation) to be sent to the other memory bank. Thus, data is written to a memory bank (e.g., banks on DDR A) while the other memory bank (banks on DDR B) receive a NOP. A “READ WITH AUTO PRECHARGE” (READAP) command would cause different actions depending on the addressing mode or memory configuration. If Row/Bank addressing is used, then a READAP command is sent to the intended bank while a NOP command is sent to the other bank. If Column addressing is employed, then the same READAP command is sent to both DDR A and DDR B. In Column addressing, the data mask (DM) signal (FIG. 2) may be used to select the target memory device (i.e., banks on DDR A or DDR B) to which data is written. Similarly, other instructions are implemented where either (1) the commands are sent to both memory banks/devices and a DM signal is used to select the targeted memory device or (2) the command is sent to the targeted device while a NOP command is sent to the non-targeted memory device. Thus, the control unit and switch architecture can control data to and from the memory banks without the delays caused by otherwise disabling the banks.” Ellsberry at [0042]. “Another feature of the invention squelches or suppresses extended mode register set (EMRS) commands from being passed to the SDRAMs. Instead of passing these commands directly to the memory devices, the control unit passes the command to the memory bank switch where the values are stored and one or more of the EMRS commands are squelched, modified, or suppressed. FIG. 9 illustrates a plurality of bits that are squelched from the original EMRS command according to one embodiment of the invention. The squelch function allows the memory devices to be configured to operate in conjunction with the controller/switch devices and host system, rather than be directly programmed by the host system.” Ellsberry at [0044].



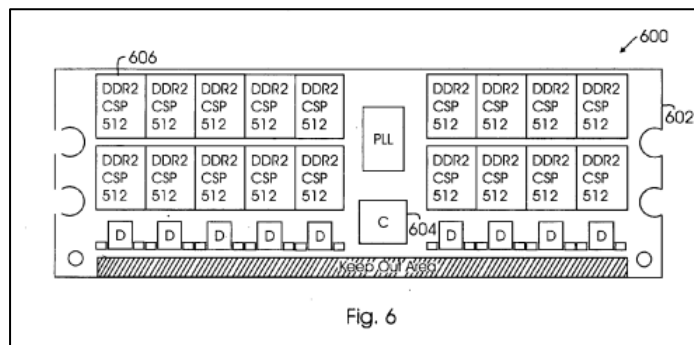
Ellsberry at Fig. 9.

“FIG. 4 illustrates a block diagram of a data processing system 400 for a capacity-expanding memory device according to one embodiment of the invention. This data processing system 400 may be implemented as part of the memory bank switch 206. Data is transmitted from the DIMM interface 202 via the data bus 230 to bidirectional signal drivers 402 & 404 that transmit and receive data over separate data busses 234 and 236 to the different sets of memory banks. A read/write logic unit 406 determines whether data is being read from or written to the memory devices (e.g., 212). Memory configuration information 408 is obtained from the control unit. An off-chip driver (OCD) state machine 410 is used by the system for impedance calibration using this tuning mechanism to adjust buffer drive strength to the DIMM interface 202. Typically, this impedance calibration takes place in the memory devices themselves, but in the present invention the OCD function is shifted to the switch device that sits between the memory devices and the DIMM interface. According to one embodiment of the invention, the control system 300 and memory bank switch system 400 may be implemented on the same semiconductor die. The semiconductor die may be configurable (via a selectable line/pin, for example) to operate as either a control unit 204 or a memory bank switch 206. The control unit 204 and/or memory bank switch 206 may be implemented as an application specific integrated circuit (ASIC). In one embodiment of the invention, the control unit and bank switch combination allows the use of a system with two separate SDRAM DDR devices to emulate a single, two-times capacity, SDRAM DDR device. In various embodiments of the invention, the control unit and bank switch combination may support

SDRAM DDR1 and DDR2 specifications (incorporated herein by reference) with memory capacities of 256 Mb, 512 Mb, and 1 Gb in speed grades of 200/266/333/400 Mbps in DDR1 and capacities of 256 Mb, 512 Mb, 1 Gb, and 2 Gb in speed grades of 400/533 Mbps in DDR2.” Ellsberry at [0045-0046].



Ellsberry at Fig. 5.



Ellsberry at Fig. 6.

“FIGS. 5 and 6 illustrate memory modules according to two different embodiments of the invention. In FIG. 5, the memory module 500 includes a substrate 502 on which a plurality of memory devices 504 are mounted. The memory module 500 also includes an edge interface 506 that serves to communicatively couple the memory module 500 to a memory slot or to a communication bus (e.g., memory bus, etc.). A memory controller 510 is mounted on the substrate 502 and configured to control write and read operations to/from the memory devices 506. The memory controller 510 is communicatively coupled to the edge interface 506 and receives address, command, and control signals from the edge interface 506. The memory controller 510 is also communicatively coupled to one or more memory bank switch 508 to control data Read and/or Write operations to/from the one or more memory devices 504 & 512. Memory bank switch 508 is communicatively coupled to memory devices 504 & 512 to route data to and from one or more of the memory devices 504 & 512. The memory bank switch 508 is also communicatively coupled to the edge interface 506 to pass signals between the edge interface 506 and the memory devices 504 & 512. The

'608 patent	35 U.S.C. §§ 102, 103 Analysis
	operation of the memory controller 510 and memory bank switch 508, as previously described, causes the memory devices 504 & 512 to emulate a single memory device having the total capacity of the combined memory devices 504 & 512. That is, the operating system addresses a single logical memory bank which is mapped by the controller 510 to the physical banks of memory devices 504 & 512. An external phase lock loop (PLL) 514 receives a clock signal from the edge interface 506 and provides a clock signal to the memory module components.” Ellsberry at [0047-0048]. “According to one embodiment of the invention, a memory controller 510 is a control unit 204 and the memory bank switches 508 are memory bank switches 206 as described above. In various embodiments of the invention, the memory bank switches 508 may be electrically coupled to two or more memory devices 504 & 512, thereby expanding the capacity of a memory module 500.” Ellsberry at [0049]. “In one implementation of the invention, illustrated in FIG. 5, the memory devices 504 & 512 on the memory module 500 may be arranged as nine memory bank switches or sets 508 having two memory banks 504 & 512 each. Each memory device has five hundred and twelve (512) megabits (MBit) of DRAM. As a result of this arrangement, the memory module 500 uses 512 MBit DRAM devices but appears, to the system processor, as a 1 GBit DRAM device. As a result of this architecture, the memory module presents a single electrical load to the system and is compatible with existing standards (e.g., JEDEC compatible, etc.). The Joint Electron Device Engineering Council (JEDEC) standards, used in many memory applications, are incorporated herein by reference.” Ellsberry at [0050].

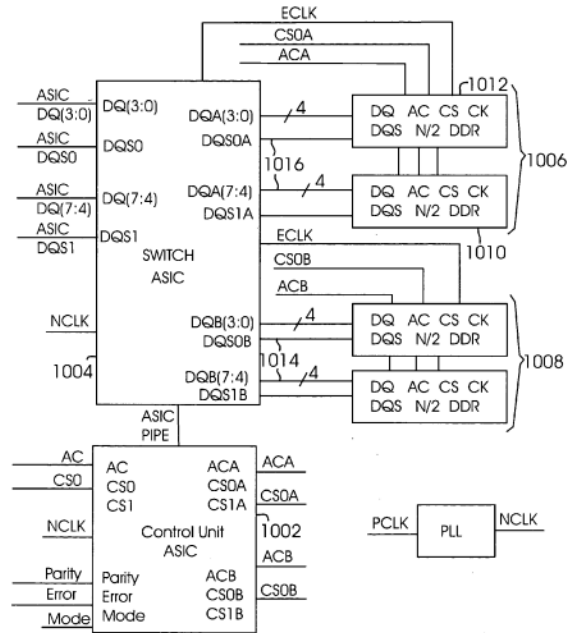


Fig. 10

Ellsberry at Fig. 10.

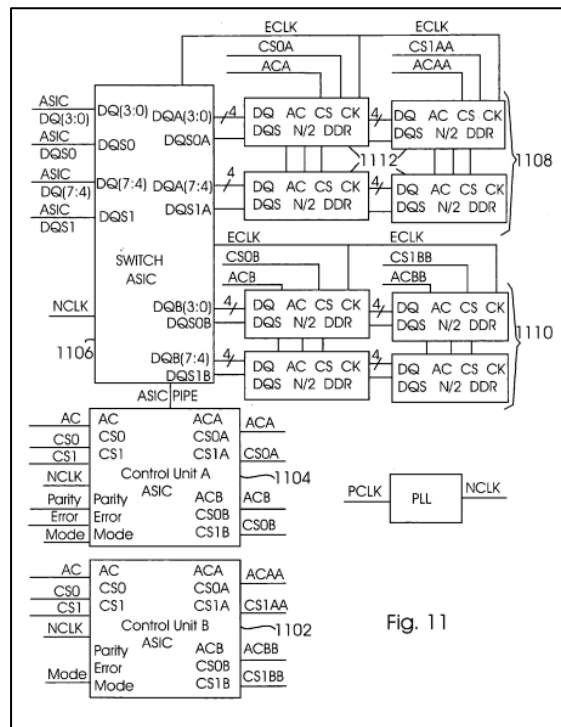


Fig. 11

Ellsberry at Fig. 11.

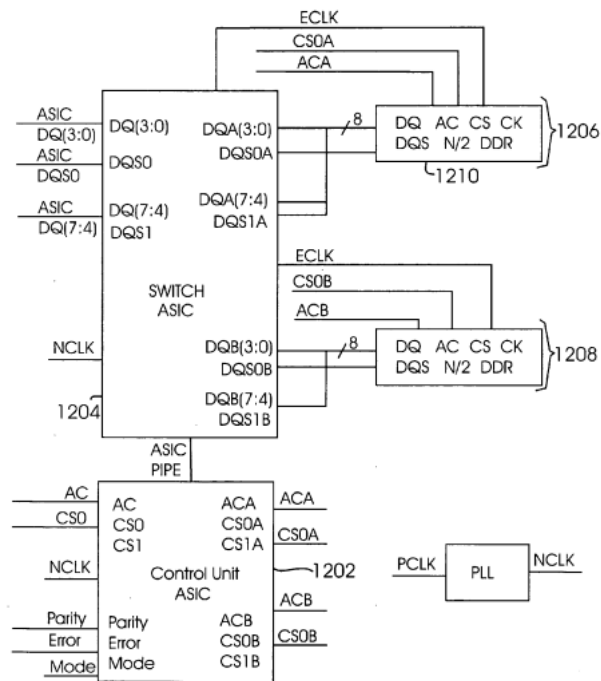


Fig. 12

Ellsberry at Fig. 12.

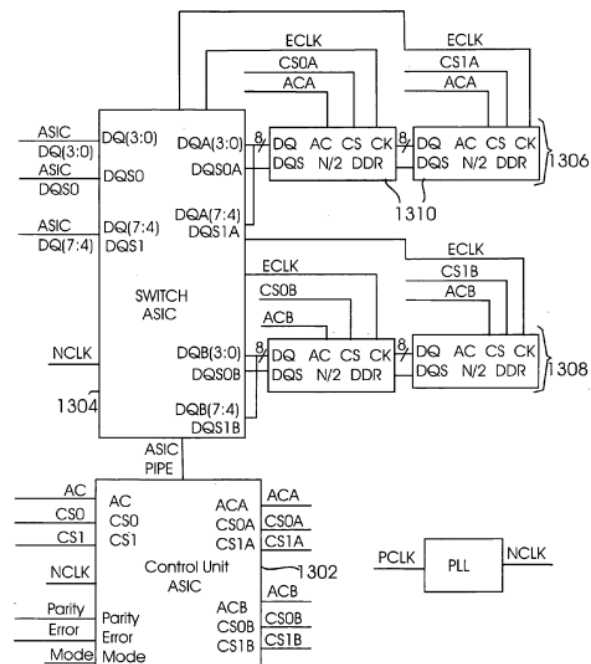
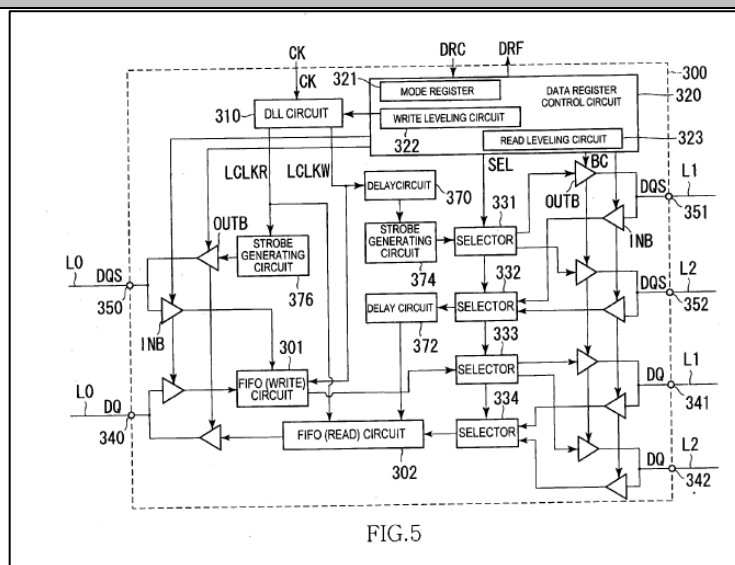


Fig. 13

'608 patent	35 U.S.C. §§ 102, 103 Analysis
	Ellsberry at Fig. 13. “FIGS. 10, 11, 12 and 13 illustrate different configurations of memory modules (e.g., DIMMs) that can be built using combinations of the control unit and bank switch according to various embodiments of the invention. These configurations employ the control unit and bank switch previously described. FIG. 10 illustrates a single chip-select memory configuration in which one control unit 1002 and one bank switch 1004 are used to control two memory banks 1006 & 1008, each memory bank having two memory devices 1010 & 1012 in separate data buses 1014 & 1016. FIG. 11 illustrates a dual chip-select memory configuration in which two control units 1102 & 1104 and one bank switch 1106 are used to control two memory banks 1108 & 1110, each memory bank having four memory devices 1112. FIG. 12 illustrates a single chip-select memory configuration in which one control unit 1202 and one bank switch 1204 are used to control two memory banks 1206 & 1208, each memory bank having one memory device 1210. FIG. 13 illustrates a dual chip-select memory configuration in which one control unit 1302 and one bank switch 1304 are used to control two memory banks 1306 & 1308, each memory bank having two memory devices 1310 in one common bus.” Ellsberry at [0052-0056].
1[d3] wherein the data path corresponding to the each data signal line includes at least one tristate buffer controlled by the command processing circuit and a delay circuit configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals.	Based on Netlist’s apparent view of the scope of the ’608 patent claims, as articulated in its Infringement Contentions and which I disagree with, it is my opinion that Hiraishi alone or in view of the knowledge of a POSITA or in combination with the referenced prior art discloses element 1[d3]. See claim limitations 1[d1] and 1[d2] analysis above. For example, Hiraishi discloses the data path corresponding to each data line including at least one tristate buffer (e.g., output buffers OUTB and input buffers INB) controlled by the command processing circuit (e.g., Data Register Control Circuit 320 and logic in DLL Circuit 310). A POSITA would also understand that driving bidirectional data/strobe lines using tristate buffers was common at the time. Hiraishi also discloses a delay circuit (logic in DLL Circuit 310, FIFO (Write) Circuit 301, FIFO (Read) Circuit 302, Delay Circuits 370, 372, and/or Strobe Generating Circuits 374, 376) configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals (e.g., DRC).



Hiraishi at Fig. 5.

“FIG. 5 is a block diagram of the configuration of the data register buffer **300**. As shown in FIG. 5, the data register buffer **300** includes a FIFO (Write) circuit **301** and a FIFO (Read) circuit **302**. The FIFO (Write) circuit **301** buffers data DQ that is supplied via an input/output terminal **340** with a data strobe signal DQS that is supplied via an input/output terminal **350**. The FIFO (Read) circuit **302** buffers data DQ that is supplied via an input/output terminal **341** or **342** with a data strobe signal DQS that is supplied via an input/output terminal **351** or **352**. A strobe generating circuit **376** generates a data strobe signal DQS to be supplied to the data connectors **120**, in synchronization with an internal clock LCLKR that is generated by a DLL circuit **310**. A strobe generating circuit **374** generates a data strobe signal DQS to be supplied to the memory chip **200**, in synchronization with an internal clock LCLKW that is generated by the DLL circuit **310**.

The FIFO circuits **301** and **302** shown in FIG. 5 are circuits that perform input and output of 1-bit data, so that in an actual case, the number of sets of the FIFO circuits **301** and **302** as many as a width of input/output data are provided. In the present embodiment, because a single data register buffer **300** inputs and outputs 1-byte data, 8 sets of the FIFO circuits **301** and **302** are required.” Hiraishi at [0083-0085].

“Furthermore, the data register control circuit **320** includes a write leveling circuit **322** and a read leveling circuit **323**. The write leveling circuit **322** is a circuit for performing a write leveling operation, and the read leveling circuit **323** is a circuit for performing a read leveling operation. Details on the write leveling operation and the read leveling operation will be described later.

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	The selector 333 is a circuit that supplies data DQ that is an output of the FIFO (Write) circuit 301 to either one of the input/output terminals 341 and 342. The selector 334 is a circuit that selects data DQ input from either one of the input/output terminals 341 and 342 and supplies the selected data DQ to the FIFO (Read) circuit 302. The selectors 331 and 332 perform the similar functions as those of the selectors 333 and 334, respectively. Specifically, the selector 332 selects a data strobe signal DQS input from either one of the input/output terminals 351 and 352. A phase of the selected data strobe signal DQS is delayed by about 90 degrees by a delay circuit 372, and then the data strobe signal DQS is supplied to the FIFO (Read) circuit 302 as an input trigger signal. The selector 331 supplies the data strobe signal DQS that is supplied from the strobe generating circuit 374 to either one of the input/output terminals 351 and 352. A phase of the data strobe signal DQS generated by the strobe generating circuit 374 is delayed by about 90 degrees with respect to the internal clock LCLKW by a delay circuit 370. Each of the selections by the selectors 331 to 334 is specified by the select signal SEL that is an output of the data register control circuit 320.” Hiraishi at [0090-0091]. “In this manner, the data register buffer 300 buffers the write data that is transferred via the data line L0 and outputs the write data to either one of the data lines L1 and L2, and buffers the read data that is transferred via either one of the data lines L1 and L2 and outputs the read data to the data line L0. Because the data register buffer 300 only performs the buffering of the data, transfer rates of the write data and the read data that are transferred via the data line L0 and transfer rates of the write data and the read data that are transferred via the data lines L1 and L2 are equal to each other. Therefore, the data register buffer 300 can be implemented with a chip that is provided at relatively low cost instead of an expensive chip such as an AMB used in a Fully Buffered memory module.” Hiraishi at [0092-0093]. “FIG. 6 is a block diagram of the configuration of the command/address/control register buffer 400. As shown in FIG. 6, the command/address/control register buffer 400 includes the input terminal 401 for connecting to the command/address/control connectors 130, the output terminal 402 for connecting to the memory chip 200, and the output terminal 403 and an input terminal 404 for connecting to the data register buffer 300.” The command/address/control signal that is supplied from the memory controller 12 is input from the input terminal 401. Among input command/address/control signals, the command signal CMD, the address signal ADD, and the control signal CTRL are supplied to a register circuit 410, and the clock signal CK is supplied to a PLL circuit 420. The register circuit 410 is a circuit that buffers the

command signal CMD, the address signal ADD, and the control signal CTRL, and the buffered command signal CMD, address signal ADD, and control signal CTRL are supplied to the memory chip **200** via the output terminal **402**.

An operation timing of the register circuit **410** is defined by an internal clock LCLKCA that is generated by the PLL circuit **420**. The PLL circuit **420** is a circuit that generates the internal clock LCLKCA based on the clock signal CK supplied from the memory controller **12** having the same circuit configuration and function as that of the DLL circuit **212** provided in the memory chip **200**. It is selected based on a set content in a mode register **431** that is included in a control signal generating circuit **430** whether to use the PLL circuit **420**. The PLL circuit **420** can be replaced with a DLL circuit.” Hiraishi at [0095-0098].

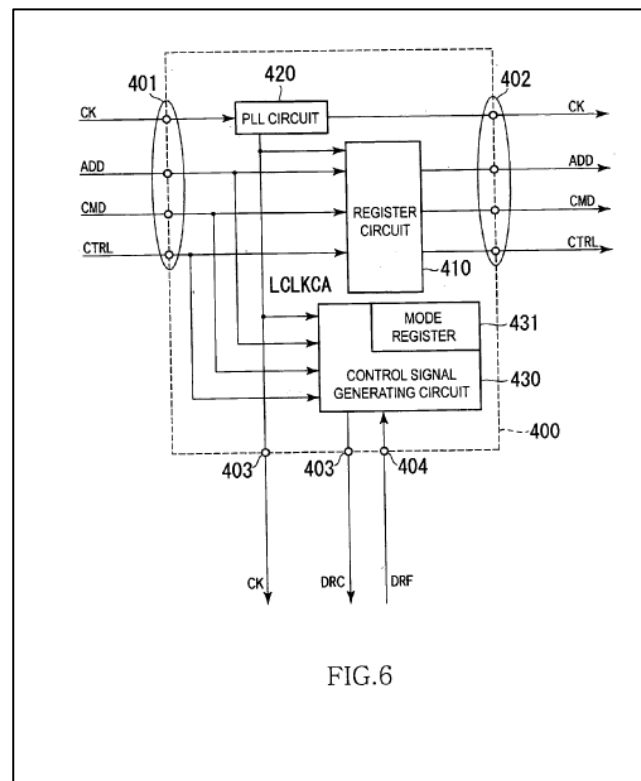


FIG.6

Hiraishi at Fig. 6.

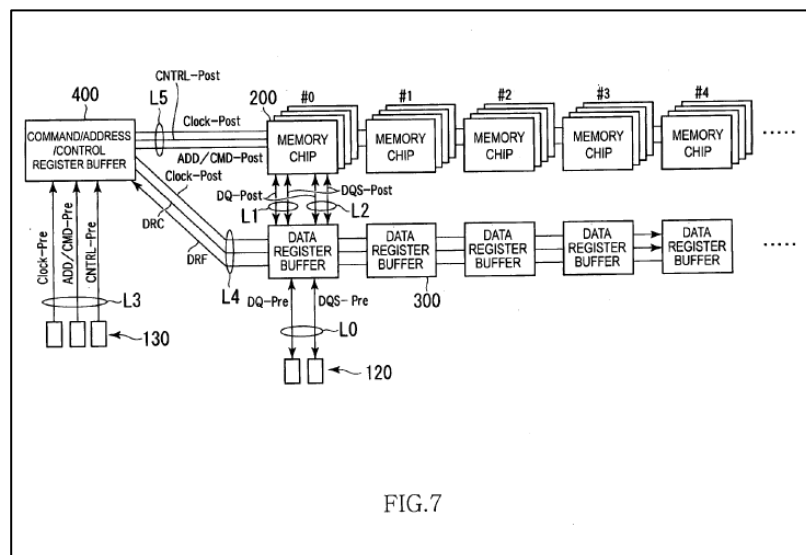
“The control signal generating circuit **430** is a circuit that generates the control signal DRC to be supplied to the data register buffer **300** based on the command/address/control signal supplied via the input terminal **401**, of which an operation is performed in synchronization with the internal clock LCLKCA. The control signal DRC for the data register buffer **300** is supplied to the data register buffer **300** via the output terminal **403**. The feedback signal DRF is

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	supplied to the control signal generating circuit 430 from the data register buffer 300 via the input terminal 404. The control signal DRC includes signals such as a signal indicating a direction of transmitting and receiving data, a signal for controlling an ODT timing at the data line L0 side of the data register buffer 300, a signal for controlling an ODT timing at the data lines L1 and L2 side, a signal for controlling on and off of the DLL circuit, a signal for controlling enable and disable of the data register buffer 300, and a signal for performing a mode switching of the data register buffer 300 and a mode register set and the like. A separate line can be allocated to each of these signals, or a single common line can be allocated to a plurality of these signals. Alternatively, these signals can be transmitted to the data register buffer 300 as commands.” Hiraishi at [0099-0100]. “As shown in FIG. 7, in the present embodiment, the data register buffer 300 intervenes between the data connectors. 120 and the memory chips 200. The data connectors 120 and the data register buffer 300 are connected to each other with the data line L0, and the data register buffer 300 and the memory chips 200 are connected to each other with the data line L1 or L2. In FIG. 7, a plurality of data transferred through the data line L0 is represented by data DQ-Pre, and a plurality of data transferred through the data lines L1 and L2 is represented by data DQ-Post. Similarly, a data strobe signal transferred through the data line L0 is represented by a data strobe signal DQS-Pre, and a data strobe signal transferred through the data line L1 or L2 is represented by a data strobe signal DQS-Post. Although the data DQ-Pre and the data DQ-Post have the same content, because the data DQ is buffered by the data register buffer 300, the timing is off between the data DQ-Pre and the data DQ-Post. The same is true for a relationship between the data strobe signal DQS-Pre and the data strobe signal DQS-Post. Therefore, in the present embodiment, it is required to perform a timing adjustment between the memory chips 200 and the data register buffer 300 and a timing adjustment between the data register buffer 300 and the memory controller in a separate manner. Details on the timing adjustments will be described later. As described above, in the present embodiment, the four memory chips 200 are allocated to a single data register buffer 300. The four memory chips 200 are memory chips that constitute different Ranks from each other, which are exclusively activated by the chip select (CS) signal or the clock enable (CKE) signal included in the control signal CTRL. The address signal ADD and the command signal CMD are commonly supplied to the four memory chips 200. The address signal ADD, the command signal CMD, the control signal CTRL, and the clock signal CK supplied to the memory chips 200 are supplied from

the command/address/control register buffer **400**. The control signal DRC supplied to the data register buffer **300** is also supplied from the command/address/control register buffer **400**.

As shown in FIG. 7, the command/address/control connectors **130** and the command/address/control register buffer **400** are connected to each other with the command/address/control line **L3**, the command/address/control register buffer **400** and the data register buffer **300** are connected to each other with a control line **L4**, and the command/address/control register buffer **400** and the memory chips **200** are connected to each other with a command/address/control line **L5**. In FIG. 7, a command/address/control signal transferred through the command/address/control line **L3** is represented by a command/address signal ADD/CMD-Pre, and a command/address signal transferred through the command/address/control line **L5** is represented by a command/address signal ADD/CMD-Post. Similarly, a control signal transferred through the command/address/control line **L3** is represented by a control signal CNTRL-Pre, and a control signal transferred through the command/address/control line **L5** is represented by a control signal CNTRL-Post.

The clock signal CK to be supplied to the memory chip **200** and the data register buffer **300** is supplied from the command/address/control register buffer **400**. In FIG. 7, a clock signal transferred through the command/address/control line **L3** is represented by a clock signal Clock-Pre, and a clock signal transferred through the command/address/control line **L5** is represented by a clock signal Clock-Post.” Hiraishi at [0103-0108].



Hiraishi at Fig. 7.

“As shown in FIGS. 8A and 8B, the 1-bit data is transferred via a predetermined connector **121** of the data connectors **120**. The connector **121** is

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	connected to the data register buffer 300 via a single data line L0. As explained above referring to FIG. 5, in the present embodiment, two data lines L1 and L2 are allocated to a single data line L0. Specifically, the data line L1 is commonly connected to the memory chips 200-0 and 200-1, and the data line L2 is commonly connected to the memory chips 200-2 and 200-3. With the above configuration, the load capacity of a single data line L1 or L2 is reduced, the number of branch points decreases, and a line length from a branch point is shortened. As a result, the signal quality of data transferred on the data lines L1 and L2 is enhanced. Specifically, terminals connected to the single data line L1 are only three terminals total including data input/output terminals of the memory chips 200-0 and 200-1 and a data output terminal of the data register buffer 300. Furthermore, because the memory chips 200-0 and 200-1 are arranged facing each other across the module substrate 110, as shown in FIG. 8A, if a branch point P is arranged in an area sandwiched by the memory chips 200-0 and 200-1, the line length from the branch point to each of the memory chips 200-0 and 200-1 is considerably shortened. In addition, because the memory chips 200-0 to 200-3 are mounted at positions close to each other, a perspective difference in edges of the memory chips 200-0 to 200-3 is also suppressed to the minimum.” Hiraishi at [0110-0111]. “The read data sequentially transferred in the above manner are supplied to the data register buffer 300, and after being buffered in a FIFO circuit included in the data register buffer 300, output to the data line L0. In the example, shown in FIG. 10, since the read data is input to the data register buffer 300, the read data is output with one cycle delay.” Hiraishi at [0119]. “In this manner, in the present embodiment, because the interleaving operation can be performed using the two data lines L1 and L2, it is possible to perform a read operation for a plurality of memory chips without interruption. As a result, the read data output from the data register buffer 300 can also be supplied to the memory controller without interruption, so that the usage efficiency of a bus can be enhanced. Although the data lines L1 and L2 are not simultaneously used in the present embodiment, if the data lines L1 and L2 are put together in a single data line, it is required to spare a time equal to or longer than one cycle between read data output from different memory chips. On the other hand, in the present embodiment, because the two data lines L1 and L2 are alternately used, it is not necessary to put a time between read data output from different memory chips. Although the read operation is explained as an example in FIG. 10, a similar interleaving operation can be applied for a write operation. The

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	operation of the memory module 100 according to the present embodiment is explained below in more detail. FIG. 11 is a timing chart for explaining a read operation of the memory module 100 according to the present embodiment. In the read operation, an active command ACT and a read command Read are issued in order from the memory controller 12. In the example shown in FIG. 11, the active command ACT reaches the command/address/control connectors 130 at a time T-5 that is synchronized with the clock signal CK, and the read command Read reaches the command/address/control connectors 130 at a time T0. The commands ACT and Read reaching the command/address/control connectors 130 are input to the command/address/control register buffer 400. At this moment, there occurs a predetermined time difference (Flight Time) between a timing at which the commands ACT and Read reaches the command/address/control connectors 130 and a timing at which the commands ACT and Read are input to the command/address/control register buffer 400. The command/address/control register buffer 400 registers the received commands ACT and Read with an input clock signal in the register circuit 410 shown in FIG. 6, and then outputs them to the memory chip 200. At this time, a synchronization with the output of the commands ACT and Read is taken by delaying the output of the clock signal CK by an amount equivalent to an additional ½ clock cycle. In addition, the command/address/control register buffer 400 supplies a read command Read to the data register buffer 300 as a part of the control signal DRC. The memory chip 200 receives the commands ACT and Read, and starts an actual read operation. At this moment, there occurs a predetermined time difference (Flight Time) between a timing at which the commands ACT and Read are output from the command/address/control register buffer 400 and a timing at which the commands ACT and Read are input to the memory chip 200. Because CL=5 in the example shown in FIG. 11, the memory chip 200 starts a burst output of read data DQ at a time T5 in five clock cycles after receiving the read command Read. In the example shown in FIG. 11, the burst length is 8 bits (BL=8). The read data DQ and a data strobe signal DQS burst output from the memory chip 200 are supplied to the data register buffer 300.

The data register buffer **300** loads the read data DQ that is output from the memory chip **200** in the FIFO (Read) circuit **302** with a data strobe signal DQS that is delayed by a predetermined phase amount (for example, phase difference of about 90 degrees). At this moment, there occurs a predetermined time difference (Flight Time) between a timing at which the read data DQ and the data strobe signal DQS are output from the memory chip **200** and a timing at which the read data DQ and the data strobe signal DQS are input to the data register buffer **300**.

Thereafter, the data register buffer **300** performs a re-timing in synchronization with the internal clock LCLKR using the FIFO (Read) circuit **302** to convert CL into CL=6, and outputs the read data DQ and the data strobe signal DQS. With this configuration, it becomes possible for the memory controller to receive the read data DQ in a correct manner.” Hiraishi at [0120-0130].

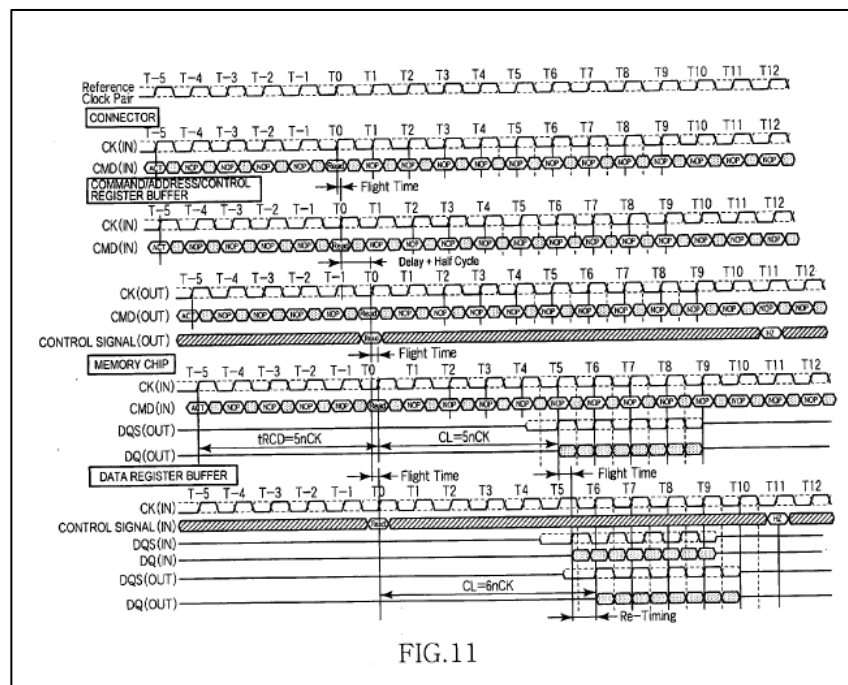
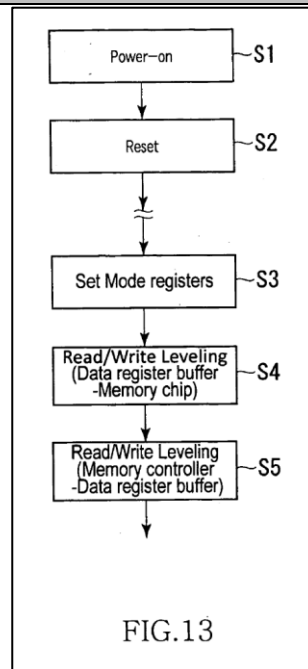


FIG. 11

Hiraishi at Fig. 11.

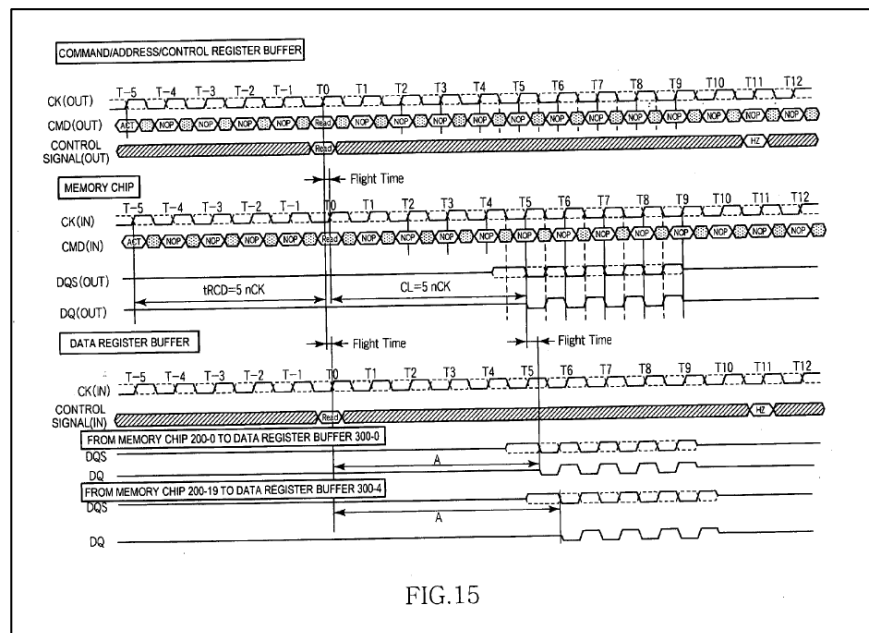
“In the write operation, the memory controller issues an active command ACT and a write command Write in order, and after a lapse of a write latency (WL) since the write command Write is issued, burst outputs write data. In the example shown in FIG. 12, the active command ACT reaches the command/address/control connectors **130** at the time T-5 that is synchronized with the clock signal CK, and the write command Write reaches the command/address/control connectors **130** at the time T0. In this example,

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	WL=4, so that write data DQ is input to the data connectors 120 from a time T4. Because a flow of the command is similar to that in the read operation shown in FIG. 11, redundant explanations will be omitted. The write data DQ reaching the data connectors 120 is input to the data register buffer 300. At this moment, there occurs a time difference (Flight Time) between a timing at which the write command reaches the command/address/control connectors 130 and a timing at which the write command (Direction Control) is input to the data register buffer 300. In consideration of this point, the memory controller outputs the write data DQ by delaying it by an amount equivalent to the Flight Time. The data register buffer 300 loads the received write data DQ in the FIFO (Write) circuit 301 with a data strobe signal DQS that is delayed by a predetermined phase amount (for example, phase difference of about 90 degrees). The data register buffer 300 then performs a re-timing in synchronization with the internal clock LCLKW using the FIFO (Write) circuit 301 to convert WL into WL=5, and outputs the write data DQ and the data strobe signal DQS. As described above, the write data is transferred from the data register buffer 300 to the memory chip 200 using either one of the two data lines L1 and L2. The data line to be used is determined by a designated Rank. The memory chip 200 receives the write data DQ that is burst output from the data register buffer 300, and writes it in the memory cell array. At this time, there occurs a predetermined time difference (Flight Time) between a timing at which the write data DQ and the data strobe signal DQS are output from the data register buffer 300 and a timing at which the write data DQ and the data strobe signal DQS are input to the memory chip 200. In consideration of this point, the data register buffer 300 outputs the write data DQ earlier by an amount equivalent to the Flight Time. With this configuration, it becomes possible for the memory chip 200 to receive the write data DQ in a correct manner.” Hiraishi at [0133-0136].



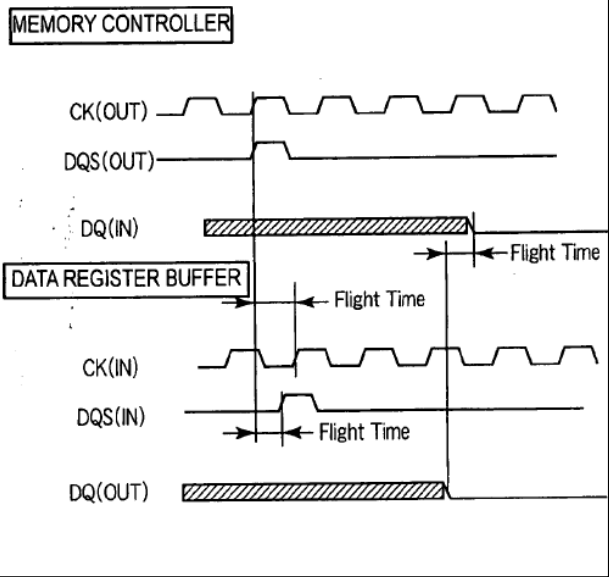
Hiraishi at Fig. 13.

“FIG. 15 is a timing chart for explaining the read leveling operation between the data register buffer 300 and the memory chip 200. This operation is performed by the read leveling circuit 323 shown in FIG. 5.” Hiraishi at [0147].



Hiraishi at Fig 15.

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	“In the read leveling operation between the data register buffer 300 and the memory chip 200, as shown in FIG. 15, the command/address/control register buffer 400 outputs the clock signal CK, and at the same time, issues the active command ACT and the read command Read. The clock signal CK is supplied to the memory chip 200 and the data register buffer 300, and the commands ACT and Read are supplied to the memory chip 200. The read command Read is also supplied to the data register buffer 300 as a part of the control signal DRC. In the example shown in FIG. 15, the active command ACT is issued at the time T-5 that is synchronized with the clock signal CK, and the read command Read is issued at the time T0. Therefore, a RAS-CAS delay (tRCD) is five clock cycles. The memory chip 200 receives the read command Read and performs an actual read operation. In the example shown in FIG. 15, the CAS latency is set to five clock cycles (CL=5), so that an output of read data DQ begins at the time T5. The read data DQ at the time of the read leveling is, for example, a signal in which a High level and a Low level are repeated in an alternate manner. The read data DQ output from the memory chip 200 reaches the data register buffer 300, by which the data register buffer 300 can find a time A from an input timing of the read command Read that is input as a part of the control signal DRC until the read data DQ is input. The time is measured for each of the memory chips 200, stored in the data register control circuit 320 in the data register buffer 300, and used in an adjustment of an activation timing of the input buffer circuit INB and the like. In FIG. 15, two cases are shown including a first case that the time A from the input of the read command Read until the input of the read data DQ is short (between the memory chip 200-0 and the data register buffer 300-0) and a second case that the time A is long (between the memory chip 200-19 and the data register buffer 300-4).” Hiraishi at [0148-0151]. “In the write leveling operation between the memory controller 12 and the data register buffer 300, as shown in FIG. 16A, the memory controller 12 outputs the clock signal and the data strobe signal DQS. The clock signal CK is supplied to the data register buffer 300 via the command/address/control register buffer 400, and the data strobe signal DQS is directly supplied to the data register buffer 300. Therefore, input timings of the clock signal CK and the data strobe signal DQS are not always the same on the data register buffer 300 side. In the example shown in FIG. 16A, on the data register buffer 300, a case that in which the logical level of the clock signal CK at the rising edge of the data

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	strobe signal DQS is “Low level”. In response to the logical level of the clock signal CK, the data register buffer 300 outputs a signal DQ of “Low level” from the input/output terminal 340. The signal DQ is supplied to the memory controller 12, by which the memory controller 12 can find a direction of phase shift of the clock signal CK and the data strobe signal DQS. The memory controller 12 changes an output timing of the data strobe signal DQS based on the direction of the phase shift. In the example shown in FIG. 16A, because the data strobe signal DQS reaches the data register buffer 300 earlier than the rising edge of the clock signal CK reaching the data register buffer 300, the memory controller 12 delays the output timing of the data strobe signal DQS.” Hiraishi at [0153-0155]. FIG.16A  The diagram illustrates the timing relationship between a Memory Controller and a Data Register Buffer. It shows several signals: CK(OUT) and DQS(OUT) from the Memory Controller; DQ(IN) and CK(IN) entering the Data Register Buffer; and DQ(OUT) leaving the Data Register Buffer. The DQ(IN) and DQ(OUT) signals are shown as shaded rectangular pulses. Arrows labeled 'Flight Time' indicate the delay between the DQ(IN) signal and the CK(IN) signal, and between the DQ(OUT) signal and the CK(OUT) signal. The diagram shows that the DQS(OUT) signal is delayed relative to the CK(OUT) signal to compensate for the flight time delay. Hiraishi at Fig 16A. “In the read leveling operation between the memory controller 12 and the data register buffer 300, as shown in FIG. 17, the memory controller 12 outputs the clock signal CK, and at the same time, issues an active command ACT and a read command Read. The clock signal CK is supplied to the data register buffer 300, and the commands ACT and Read are supplied to the data register buffer 300 via the command/address/control register buffer 400 as a part of the control signal DRC. In the example shown in FIG. 17, the active command ACT is issued at the time T-5 that is synchronized with the clock signal CK, and the read command

Read is issued at the time T0. Therefore, a RAS-CAS delay (tRCD) is five clock cycles.

The data register buffer **300** receives the read command Read, and after a lapse of a predetermined CAS latency, outputs dummy data DQ. The dummy data DQ is not the read data read out from the memory chip **200** but data that is automatically generated by the data register control circuit **320** in the data register buffer **300**. In the example shown in FIG. 17, the CAS latency is set to six clock cycles (CL=6), so that an output of the dummy data DQ begins at a time T6. The dummy data DQ is, for example, a signal in which a High level and a Low level are repeated in an alternate manner.

The dummy data DQ output from the data register buffer **300** reaches the memory controller **12**, by which the memory controller **12** can find a time B from an issuance timing of the read command Read until the read data DQ is input. The time is measured for each of the data register buffers **300**, stored in the internal circuit of the memory controller **12**, and used in an adjustment of an activation timing of an input buffer circuit (not shown) and the like. In FIG. 17, two cases are shown including a first case that the time B from the issuance of the read command Read until the input of the read data DQ is short (between the memory controller **12** and the data register buffer **300-0**) and a second case that the time B is long (between the memory controller **12** and the data register buffer **300-4**).” Hiraishi at [0158-0161].

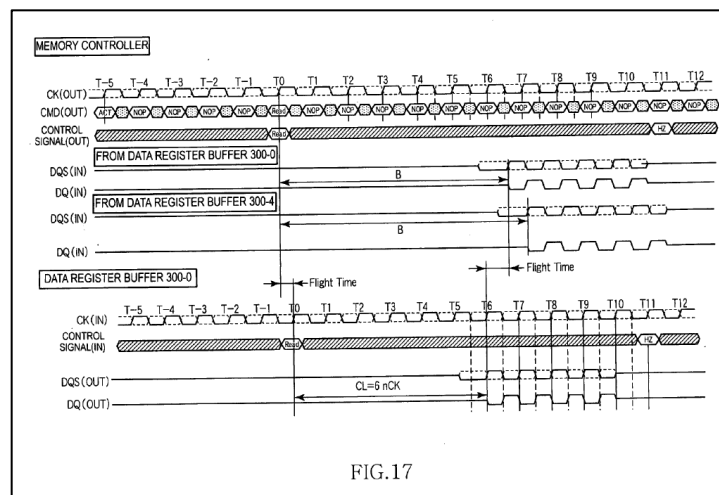


FIG.17

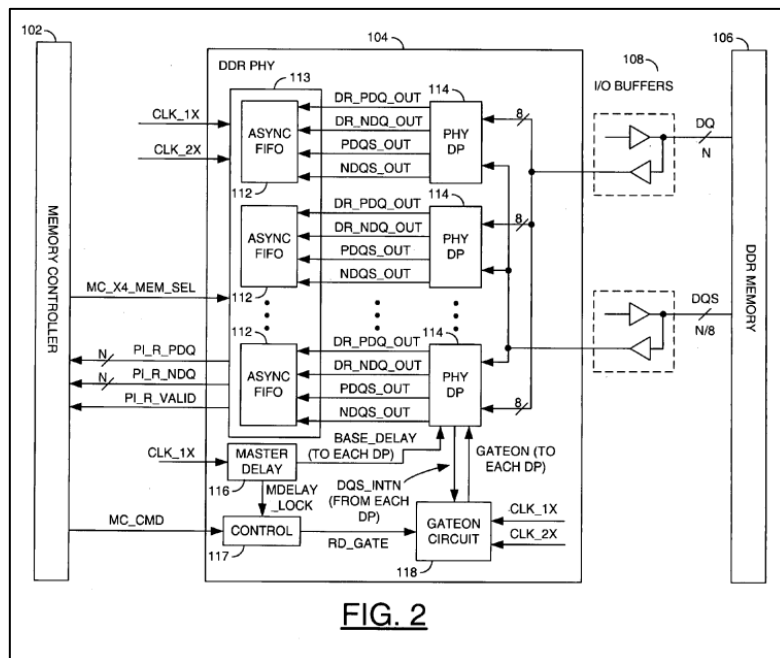
Hiraishi at Fig 17.

To the extent that this limitation is not present in Hiraishi, which I believe it is, it would have been obvious in view of Butt.

Butt discloses the data path including at least one tristate buffer (e.g., inside the I/O buffers 108) controlled by the command processing

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	circuit. Butt further discloses a delay circuit (e.g., including Master Delay/MDELAY 116 logic) configured to delay a signal through the data path by an amount determined by the command processing circuit. “A method for calibrating a data valid window including the steps of: (A) setting a base delay of one or more datapaths to a predetermined value, (B) determining an optimum offset delay value for each of the one or more datapaths based upon actual memory accesses and (C) delaying a read data strobe signal based upon the base delay and the optimum offset delay value for each of the one or more datapaths.” Butt at Abstract. The diagram, labeled FIG. 1, shows a system 100. Inside the system is an ASIC 110. Within the ASIC, there are three main blocks: a MEMORY CONTROLLER 102, a DDR PHY 104, and IO BUFFERS 108. These three blocks are connected to each other with bidirectional arrows. The IO BUFFERS 108 are connected to a block labeled DDR SDRAM 106. Two signal lines, labeled DQ and DQS, connect the IO BUFFERS 108 to the DDR SDRAM 106. Butt at Fig. 1. “Referring to FIG. 1, a block diagram is shown illustrating a system 100 in which one or more preferred embodiments of the present invention may be implemented. In one example, the system 100 may comprise a circuit (or block) 102, a circuit (or block) 104, a circuit (or block) 106 and a circuit (or block) 108. The circuit 102 may be implemented as a memory controller. The circuit 104 may be implemented as a memory interface. In one example, the circuit 104 may be implemented as a double data rate (DDR) physical layer (PHY) core. The circuit 106 may be implemented as one or more double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices. The circuit 108 may be implemented, in one example, as stub series terminated logic (SSTL) IO buffers. The circuit 104 may be coupled between the circuit 102 and the circuit 106. In one example, the circuit 104 may be coupled to the circuit 106 by the circuit 108. The circuit 104 may be configured to receive a plurality of data signals (e.g., DQ) and a plurality of read data strobe signals (e.g., DQS). In one example, the plurality of read data strobe signals may comprise a single read data strobe for each byte of the signals DQ. In another example (e.g., an x4 mode), the plurality of data strobe signals DQS may comprise a separate strobe signal (e.g., DQS_UN and DQS_LN, respectively) for each nibble (e.g., upper and lower) of the signal DQ. In one example, the circuits 102, 104 and 108 may be implemented (or instantiated) on an application specific integrated circuit

(ASIC) 110. However, the circuit 102 may be implemented separately and mounted on a common printed circuit board (PCB) along with the circuits 104, 106 and 108. The ASIC 110 may be implemented, in one example, as a platform (or structured) ASIC. In one example, the circuit 104 may be implemented based on diffused datapath (DP) and master delay modules. In another example, the circuit 104 may be implemented based on R-cell datapath and master delay modules. In one example, the circuit 104 may be implemented in an R-cell transistor fabric of the ASIC 110. As used herein, R-cell generally refer to an area of silicon containing one or more diffusions for forming the parts of N and/or P type transistors and the contact points where wires may be attached in subsequent manufacturing steps (e.g., to power, ground, inputs and outputs). Wire layers may be added to the R-cell transistor fabric to make particular transistors, logic gates, soft and firm IP blocks and/or storage elements.” Butt at [0015-0016].



Butt at Fig. 2.

“Referring to FIG. 2, a more detailed block diagram of the circuit 104 is shown illustrating example read data logic and signal paths in which a preferred embodiment of the present invention may be implemented. In one example, the circuit 104 may comprise a number of asynchronous (ASYNC) first-in first-out (FIFO) buffers 112, FIFO synchronization logic 113, a number of physical read datapaths (DPs) 114, a master delay (MDELAY) logic 116, a control logic 117 and a programmable gating signal generator 118. Each of the physical read datapaths 114 may be configured to receive (i) a respective portion of the read data signals DQ from the DDR memory 106, (ii) a respective read data strobe signal or signals DQS associated with the respective portion of the received

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	read data signals and (iii) a gating signal (e.g., GATEON) from the programmable gating signal generator 118. Each of the physical read datapaths 114 may communicate with a corresponding one of the asynchronous FIFOs 112 via a number of signals (e.g., DR_PDQ_OUT, DR_NDQ_OUT, PDQS_OUT, and NDQS_OUT). In one example, separate signals (e.g., PDQS_OUT_UN, NDQS_OUT_UN, PDQS_OUT_LN, and NDQS_OUT_LN) may be generated for each nibble of the DPs 114. In one example, the asynchronous FIFOs 112 may be configured to interface the physical read datapaths 114 with the memory controller 102. In general, the signals DQ and DQS may be presented to the DDR PHY 104 on a number of buses. The signals DQ and DQS may be broken out to multiple instantiations of DP hardmacros. The DPs may be configured via internal settings to delay the read data strobe signals DQS based on one or more control signals (or values) from the MDELAY circuit 116. Each of the DPs 114 may be configured to present the DQ data to a respective asynchronous FIFO 112 via the signals DR_PDQ_OUT and DR_NDQ_OUT, after the data is sampled using the delayed read data strobe signals DQS. The FIFOs 112 are generally configured to transfer the read data DQ from the read data strobe (or DQS) domain to the CLK_1X domain for presentation to the memory controller 102. The read data DR_PDQ_OUT and DR_NDQ_OUT are generally written to the FIFOs 112 in response to (e.g., clocked by) the signals PDQS_OUT and NDQS_OUT, respectively). The memory controller 102 may be configured to read the data DQ (e.g., via signals PI_R_PDQ and PI_R_NDQ) from the FIFOs 112 in response to the clock signal CLK_1X. In one example, the FIFOs 112 may be implemented as eight words deep. As briefly described above, the read datapaths 114 are generally programmable from when the data/strobe pairs DQ/DQS are received at the input to the circuit 104, to sampling the read data with the read data strobe signal DQS, and passing the data to the memory controller 102. The programmability of the read datapaths 114 generally provides flexibility for handling different column address strobe (CAS) latencies, burst lengths, device process variation, and/or propagation delays.” Butt at [0017-0020]. “The master delay (MDELAY) logic 116 is generally configured to calculate a delay value for generating a one-quarter cycle or one-fifth cycle delay with respect to the device reference clock (e.g., the signal CLK_1X). The calculated delay is generally used by the datapaths 114 to center a read data capture clock (e.g., the signal DQS) in a valid DDR device read data window. The calculated delay generally tracks process, voltage and temperature (PVT) corners for reliable read data latching. The MDELAY logic 116 may be configured to generate the one-quarter cycle or one-fifth cycle delay using a delay lock loop (DLL). Once the DLL is locked to the clock signal CLK_1X, a signal (e.g., MDELAY_LOCK) may be generated indicating the locked state. The signal MDELAY_LOCK may be presented to an input of the control logic 117 and/or the memory controller 102. The MDELAY logic 116 may be configured to

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	generate one or more control signals (or values) for transferring the delay settings (or values) to one or more slave delay cells (describe in more detail in connection with FIGS. 3A and 3B) in each of the DPs 114. The delay values, when transferred to each of the DPs 114, are generally referred to as base delays. In one example, a base delay may be implemented for each nibble of each DP byte. For example, a first base delay value (e.g., BASE_DELAY_UN) may be implemented for each upper nibble and a second base delay value (e.g., BASE_DELAY_LN) may be implemented for each lower nibble. The DPs 114 may also be programmed with offset delay values corresponding to each nibble (e.g., OFFSET_P_UN, OFFSET_N_UN, OFFSET_P_LN and OFFSET_N_LN). In one example, each of the DPs 114 may have a set of base delays that are independent of the other DPs 114. The offset delay values may be added to or subtracted from the respective base delay values. The control circuit 117 may be configured to generate one or more control signals for controlling and/or configuring the FIFOs 112 and datapaths 114. In one example, the control circuit 117 may be configured to generate a gating signal (e.g., RD_GATE) in response to a signal (e.g., MC_CMD) received from the controller 102. In one example, the circuit 117 may be configured to generate the signal RD_GATE in response to decoding a READ command in the signal MC_CMD. The signal RD_GATE is generally configured to prevent invalid states (e.g., when DQS is in a 3-state, or OFF, mode) from entering the circuit 113. The signal RD_GATE may be used to generate one or more gating signals. The programmable gateon generating circuit 118 may be configured to generate the signal GATEON in response to the signal RD_GATE, a first clock signal (e.g., CLK_1X), a second clock signal (e.g., CLK13 2X) and a data strobe signal (e.g., DQS_INTN) received from the DPs 114. The signal GATEON may be used to gate the read data strobe signal DQS received from the memory device 106. In one example, separate gating signals (e.g., GATEON_UN, GATEON_LN, etc.) may be generated for each nibble of the DPs 114. The signal DQS_INTN may be used to de-assert the signal GATEON. In one example, separate signals (e.g., DQS_INTN_UN and DQS_INTN_LN) may be generated for each nibble of the DPs 114. Although the circuit 118 is shown implemented separately from the DPs 114, it will be understood by those skilled in the art that the circuit 118 may be implemented as part of the DPs 114 (e.g., the signal GATEON may be generated within the DPs 114 or external to the DPs 114).” Butt at [0021-0024].

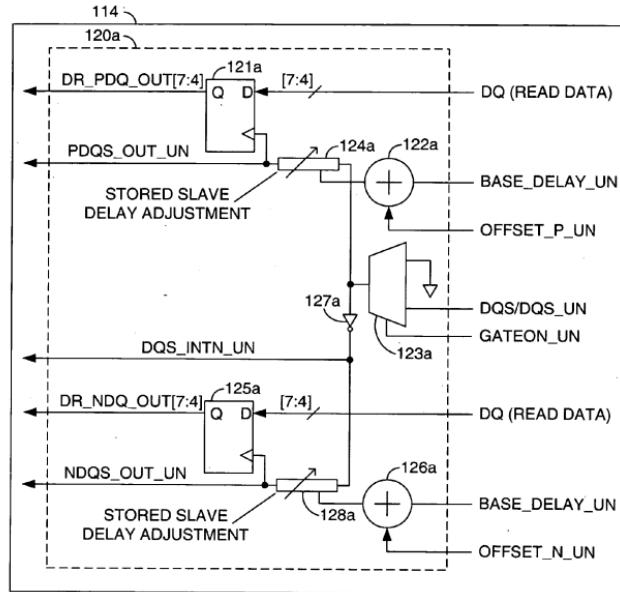


FIG. 3A

Butt at Fig. 3A.

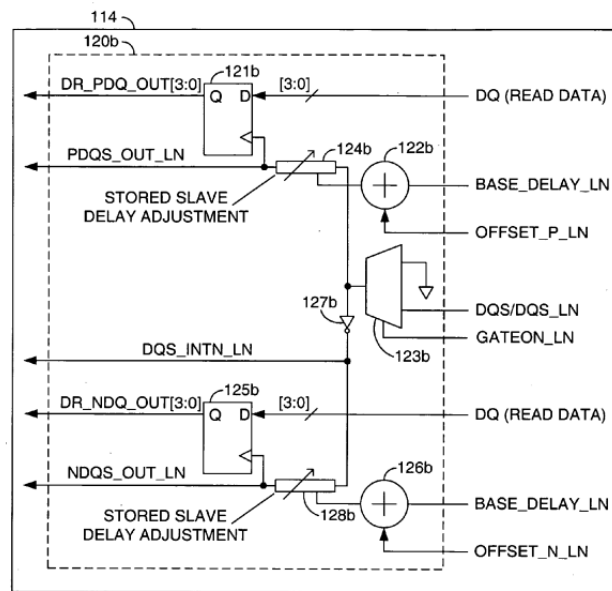


FIG. 3B

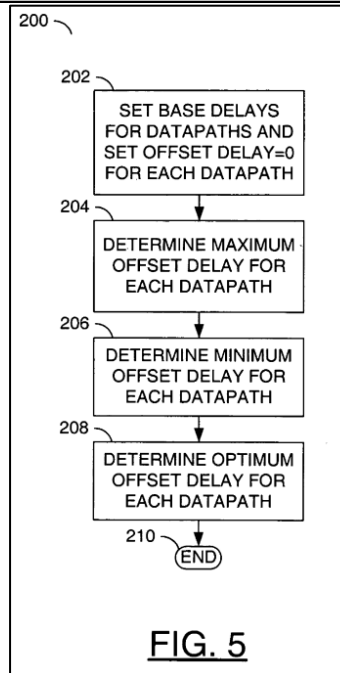
Butt at Fig. 3B.

“Referring to FIGS. 3(A-B), more detailed block diagrams of a datapath 114 of FIG. 2 are shown illustrating an example read data latching and gating circuit in accordance with a preferred embodiment of the present invention. In one

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	example, each datapath 114 may comprise an upper nibble pathway 120 a (FIG. 3A) and a lower nibble pathway 120 b (FIG. 3B). The upper nibble pathway 120 a may have a first input that may receive a number of bits of the signal DQ (e.g., bits 7:4), a second input that may receive the signal BASE_DELAY_UN, a third input that may receive the signal OFFSET_P_UN, a fourth input that may receive the signal OFFSET_N_UN, a fifth input that may receive the signal DQS (or the signal DQS_UN in the x4 mode), a sixth input that may receive a signal (e.g., GATEON_UN). The upper nibble pathway 120 a may also have a first output that may present a number of bits (e.g., the signal DR_PDQ_OUT[7:4]), a second output that may present a number of bits (e.g., the signal DR_NDQ_OUT[7:4]), a third output that may present a signal (e.g., PDQS_OUT_UN), a fourth output that may present a signal (e.g., NDQS_OUT_UN) and a fifth output that may present a signal (e.g., DQS_INTN_UN).” Butt at [0025]. “The upper nibble pathway 120 a may comprise a circuit (or block) 121 a, a circuit (or block) 122 a, a circuit (or block) 123 a, a circuit (or block) 124 a, a circuit (or block) 125 a, a circuit (or block) 126 a, a circuit (or block) 127 a and a circuit (or block) 128 a. The circuit 121 a may be implemented as one or more registers. The circuit 122 a may be implemented as an adder block. The circuit 123 a may be implemented as a multiplexer circuit. The circuit 124 a may be implemented as a slave delay adjustment block. The circuit 125 a may be implemented as one or more registers. The circuit 126 a may be implemented as an adder block. The circuit 127 a may be implemented as an inverter circuit. The circuit 128 a may be implemented as a slave delay adjustment block. The circuit 121 a may be configured to latch an upper nibble (e.g., bits 7:4) of the read data signal DQ in response to a clock input. The circuit 121 a may be further configured to present the latched read data as the signal DR_PDQ_OUT[7:4]. The circuit 122 a may be configured to generate a sum (or difference) of the signals BASE_DELAY_UN and OFFSET_P_UN. The circuit 123 a may be configured to select either the signal DQS (or the signal DQS_UN in the x4 mode) or a predetermined logic level (e.g., a LOW or logic 0) in response to the signal GATEON_UN. The circuit 124 a may be configured to delay the signal presented by the circuit 123 a based on the sum (or difference) generated by the circuit 122 a. An output of the circuit 124 a may present the signal PDQS_OUT_UN to the clock input of the circuit 121 a and the third output of the upper nibble pathway 120 a. The circuit 125 a may be configured to latch an upper nibble (e.g., bits 7:4) of the read data signal DQ in response to a clock input. The circuit 125 a may be further configured to present the latched read data as the signal DR_NDQ_OUT[7:4]. The circuit 126 a may be configured to generate a sum (or difference) of the signals BASE_DELAY_UN and OFFSETN_UN. The circuit 127 a may be configured to generate the signal DQS_INTN_UN as a digital complement of the signal presented by the circuit 123 a. The signal DQS_INTN_UN may be presented to an input of the circuit 128 a and the fifth output of the upper nibble pathway

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	120 a. The circuit 128 a may be configured to generate the signal NDQS_OUT_UN by delaying the signal DQS_INTN_UN based on the sum (or difference) generated by the circuit 126 a. An output of the circuit 128 a may present the signal NDQS_OUT_UN to the clock input of the circuit 125 a and the fourth output of the upper nibble pathway 120 a.” Butt at [0026-0028]. “The lower nibble pathway 120 b may have a first input that may receive a number of bits (e.g., bits 3:0) of the signal DQ, a second input that may receive the signal BASE_DELAY_LN, a third input that may receive the signal OFFSET_P_LN, a fourth input that may receive the signal OFFSET_N_LN, a fifth input that may receive the signal DQS (or the signal DQS_LN in the x4 mode), a sixth input that may receive a signal (e.g., GATEON_LN). The lower nibble pathway 120 b may also have a first output that may present a number of bits (e.g., the signal DR_PDQ_OUT[3:0]), a second output that may present a number of bits (e.g., the signal DR_NDQ_OUT[3:0]), a third output that may present the signal PDQS_OUT_LN, a fourth output that may present the signal NDQS_OUT_LN and a fifth output that may present the signal DQS_INTN_LN. The lower nibble pathway 120 b may comprise a circuit (or block) 121 b, a circuit (or block) 122 b, a circuit (or block) 123 b, a circuit (or block) 124 b, a circuit (or block) 125 b, a circuit (or block) 126 b, a circuit (or block) 127 b and a circuit (or block) 128 b. The circuit 121 b may be implemented as one or more registers. The circuit 122 b may be implemented as an adder block. The circuit 123 b may be implemented as a multiplexer circuit. The circuit 124 b may be implemented as a slave delay adjustment block. The circuit 125 b may be implemented as one or more registers. The circuit 126 b may be implemented as an adder block. The circuit 127 b may be implemented as an inverter circuit. The circuit 128 b may be implemented as a slave delay adjustment block. The circuit 121 b may be configured to latch a lower nibble (e.g., bits 3:0) of the read data signal DQ in response to a clock input. The circuit 121 b may be further configured to present the latched read data as the signal DR_PDQ_OUT[3:0]. The circuit 122 b may be configured to generate a sum (or difference) of the signals BASE_DELAY_LN and OFFSET_P_LN. The circuit 123 b may be configured to select either the signal DQS (or the signal DQS_LN in the x4 mode) or a predetermined logic level (e.g., a LOW or logic 0) in response to the signal GATEON_LN. The circuit 124 b may be configured to delay the signal presented by the circuit 123 b based on the sum (or difference) generated by the circuit 122 b. An output of the circuit 124 b may present the signal PDQS_OUT_LN to the clock input of the circuit 121 b and the third output of the lower nibble pathway 120 b. The circuit 125 b may be configured to latch a lower nibble (e.g., bits 3:0) of the read data signal DQ in response to a clock input. The circuit 125 b may be further configured to present the latched read data as the signal DR_NDQ_OUT[3:0]. The circuit 126 b may be configured to generate a sum (or difference) of the signals BASE_DELAY_LN and OFFSET_N_LN. The circuit 127 b may be configured to generate the signal DQS_INTN_LN as a digital complement of the signal

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	presented by the circuit 123 b. The signal DQS_INTN_LN may be presented to an input of the circuit 128 b and the fifth output of the lower nibble pathway 120 b. The circuit 128 b may be configured to generate the signal NDQS_OUT_LN by delaying the signal DQS_INTN_LN based on the sum (or difference) generated by the circuit 126 b. An output of the circuit 128 b may present the signal NDQS_OUT_LN to the clock input of the circuit 125 b and the fourth output of the lower nibble pathway 120 b.” Butt at [0029-0032]. “Referring to FIG. 4, a timing diagram is shown illustrating various signals implemented in the interface between the physical interface 104 and the DDR SDRAM device 106. The circuit 104 generally receives aligned DQ and DQS signals from the DDR SDRAM device(s) 106. As used herein, the term data eye is generally used to refer to a characteristic appearance of the read data signal waveforms, on the DQ lines. The term read training generally refers to a process performed, for example, at powerup or reset, to establish optimum DQS strobe settings. The circuits 124 a, 124 b, 128 a and 128 b within the datapath (DP) hardmacro are generally configured to shift the DQS strobe to be optimally positioned relative to DQ (valid read data). In one example, the circuits 124 a, 124 b, 128 a and 128 b may be configured to shift the DQS strobe by one-quarter or one-fifth cycle.” Butt at [0033]. “The present invention may be implemented in logic (e.g., hard intellectual property (IP), firm IP and/or soft IP) that may provide read data synchronization from the DQS domain on an external DDR SDRAM memory bus to a 1x clock domain (e.g., the signal CLK_1X) used by the DDR PHY 104 and the DDR memory controller 102. The read data strobe signal DQS may be used to clock in the read data. The present invention generally enables a reliable data read operation for high speed applications.” Butt at [0036].



Butt at Fig. 5.

“Referring to FIG. 5, a flow diagram is shown illustrating a process 200 in accordance with a preferred embodiment of the present invention. In one example, the process 200 may begin by setting base delays (e.g., BASE_DELAY_LN and BASE_DELAY_UN) in each of the datapaths 114 to a predetermined initial value and setting offset delays (e.g., OFFSET_P_LN, OFFSET_N_LN, OFFSET_P_UN and OFFSET_N_UN) for each of the datapaths 114 to zero (e.g., block 202). A write/read/compare test may be performed to verify that the memory device 106 may be read using the initial base delay and offset delay values.” Butt at [0037].

“In one example, the process of setting the initial base and offset delays may comprise the following steps:

1. Verifying that the MDELAY (Master Delay) circuit 116 has achieved DLL lock. In one example, verification may be performed by reading a first bit (e.g., L or lock) and a second bit (e.g., LF or lock failure) in a register of the MDELAY circuit 116. If the verification fails (e.g., the L bit is not one or the LF bit is not zero), the MDELAY circuit 116 may be reset to recover from the failure condition.
2. Transferring MDELAY DQS delay control values (the base delay values) to the DPs 114. In one example, the base delay values may be transferred by writing to one or more registers.
3. Setting a number of bits (e.g., base delay select bits) so the updated delay values may be loaded into the base delays of the DPs 114.

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	4. Setting the offset delay values in the DPs 114 to zero. In one example, the offset delay values in the DPs 114 may be set to zero by using a control register. In one example, a number of offset delays (e.g., four) may be implemented for each DP 114. The delay values may be initially set to zero after the reset. 5. Establishing pointers and storage locations for the minimum and maximum offset delay values to be determined by the process 200 and initializing the offset delay values appropriately (e.g., using signed 2's-complement format). For example, an offset delay value may be implemented for each nibble of each DP byte, and for each nibble a positive-edge strobe offset and a negative-edge strobe offset may be implemented. For example, four offset delay values per DP 114 may be implemented (e.g., OFFSET_N_LN, OFFSET_P_LN, OFFSET_N_UN and OFFSET_P_UN). 6. Verifying that valid DDR data may be read with the delay offset values set to zero. For example, a routine may be executed that writes to, reads from, and compares a selected data pattern to a selected range of the DDR memory 106. If valid data cannot be read with the delay offset values set to zero, the initial settings may not be sufficient. In one example, delay settings for the signal GATEON may be re-evaluated. However, high level system debugging may also be performed. In one example, a signal (e.g., an error signal) may be generated to inform the user.” Butt at [0038-0044]. “The process 200 generally continues by determining maximum offset delay values for each DP 114 (e.g., block 204). For example, maximum upper and lower nibble offset delay values may be determined for each DP 114 (e.g., using a positive adjustment routine). When maximum offset delay values have been determined for each of the datapaths, the process 200 generally determines minimum offset delay values for each DP 114 (e.g., the block 206). For example, minimum upper and lower nibble offset delay values may be determined for each DP 114 (e.g., using a negative adjustment routine). When both maximum and minimum offset delay values have been determined for each offset delay value of each of the DPs 114, the process 200 generally determines optimum offset delay values for each of the DPs 114 and loads (or programs) the optimum offset delay values into the DPs 114 (e.g., the block 208). In one example, the minimum and maximum values for each offset delay may be used to determine an average offset delay value (e.g., (max offset+min offset)/2) as the optimum offset value. The optimum values may be written, in one example, to a respective register (e.g., a DP Slave Delay register) using a control register (e.g., a DDR PHY Select Slave Delay register). When the optimum offset delay values are loaded into each of the DPs 114, the process 200 generally ends (e.g., block 210).” Butt at [0045-0046]. “Referring to FIG. 6, a more detailed flow diagram of the block 204 in FIG. 5 is shown illustrating a process for determining the maximum offset values. In one

example, the process for determining the maximum offset values may comprise the following steps:

1. Using a PAR (Positive Adjustment Routine), increment each offset delay value.
2. Programming the DP 114 with the selected new offset values.
3. Testing the read data at each increment.
4. Repeating step 1 through step 3, until the read test fails.
5. Recording the highest delay setting that yields valid data.

The highest delay setting that yields valid data is the maximum offset for the respective delay.

In one example, the process 204 may be implemented with a number of steps 220-236. The process 204 may begin by programming the datapaths with predetermined offset values (e.g., block 220). The process 204 may perform a test access on the memory 106 (e.g., blocks 222 and 224). When the memory test access fails, the process 204 may set the maximum offset delay value for the corresponding datapath 114 to the last value that passed the test (e.g., block 226). When the memory test access passes, the process 204 generally checks whether all delay values have been tested (e.g., block 228). When all the delay values have not been tested, the process 204 generally proceeds by incrementing the (e.g., block 230) and repeating the memory access test. When the last delay value for a particular datapath 114 has been tested, the process 204 generally determines whether all of the datapaths 114 have been tested (e.g., block 232). When all the datapaths 114 have not been tested, the process 204 moves to a next datapath 114 (e.g., block 234). When all datapaths 114 are tested, the process 204 generally ends (e.g., block 236)."

Butt at [0048-0054]; *see also* Butt at [0055-0060].

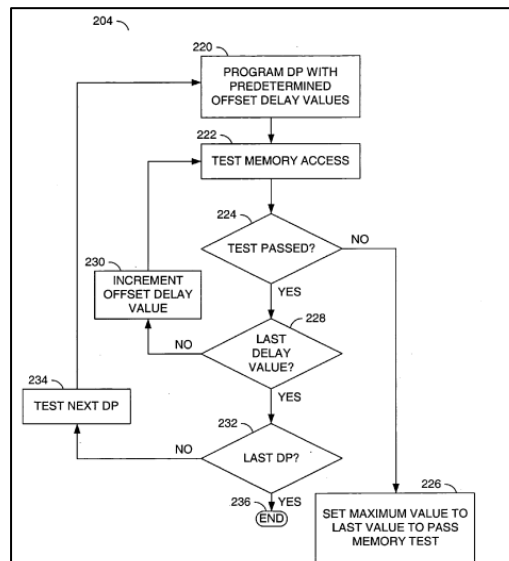
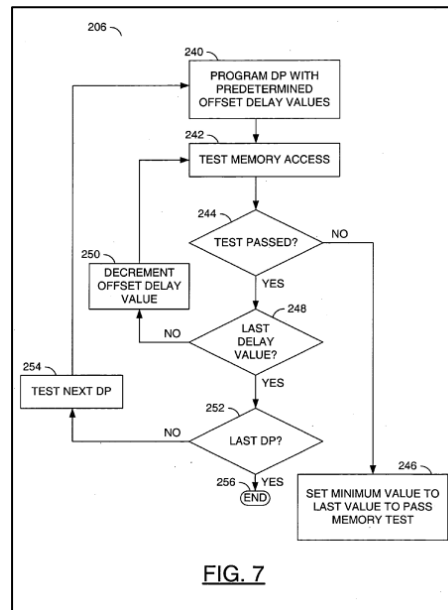


FIG. 6

Butt at Fig. 6.



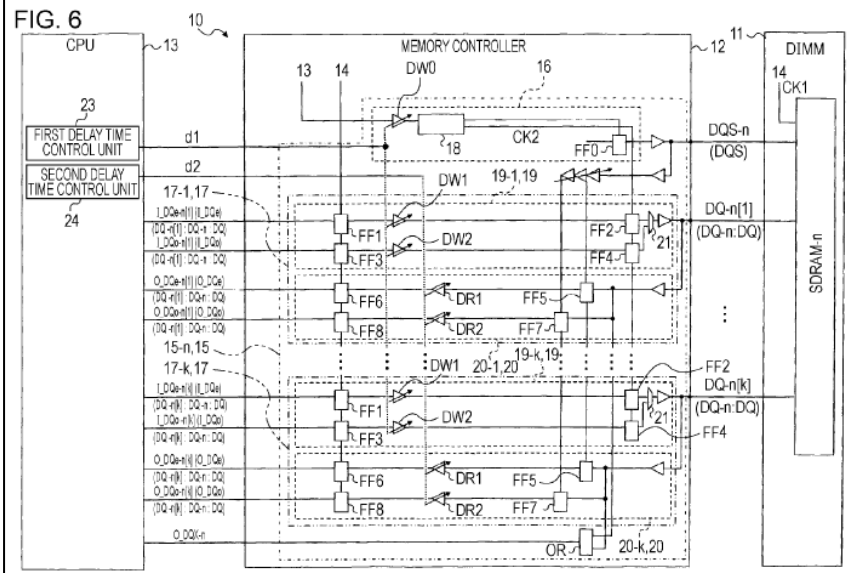
Butt at Fig. 7.

“In one example, the process 206 may be implemented with a number of steps 240-256. The process 206 may begin by programming the datapaths 114 with predetermined offset values (e.g., block 240). The process 206 may perform a test access on the memory 106 (e.g., blocks 242 and 244). When the memory test access fails, the process 206 may set the minimum offset delay value for the corresponding datapath 114 to the last value that passed the test (e.g., block 246). When the memory test access passes, the process 206 generally checks whether all delay values have been tested (e.g., block 248). When all the delay values have not been tested, the process 206 generally proceeds by decrementing the delay value (e.g., block 250) and repeating the memory access test. When the last delay value for a particular datapath 114 has been tested, the process 206 generally determines whether all of the datapaths 114 have been tested (e.g., block 252). When all the datapaths 114 have not been tested, the process 206 moves to a next datapath 114 (e.g., block 254). When all datapaths 114 are tested, the process 206 generally ends (e.g., block 256).” Butt at [0061].

To the extent that this limitation is not present in Hiraishi and/or Butt, which I believe it is, it would have been obvious in view of Tokuhiko.

“The term ‘write leveling function’ refers to the function of sampling the clock signal CK by using the data strobe signal DQS output from the memory controller 90, detecting the phase relationship between the data strobe signal DQS and the clock signal CK, and adjusting (compensating) a delay time of the data strobe signal DQS.” Tokuhiko at 2:13-18.

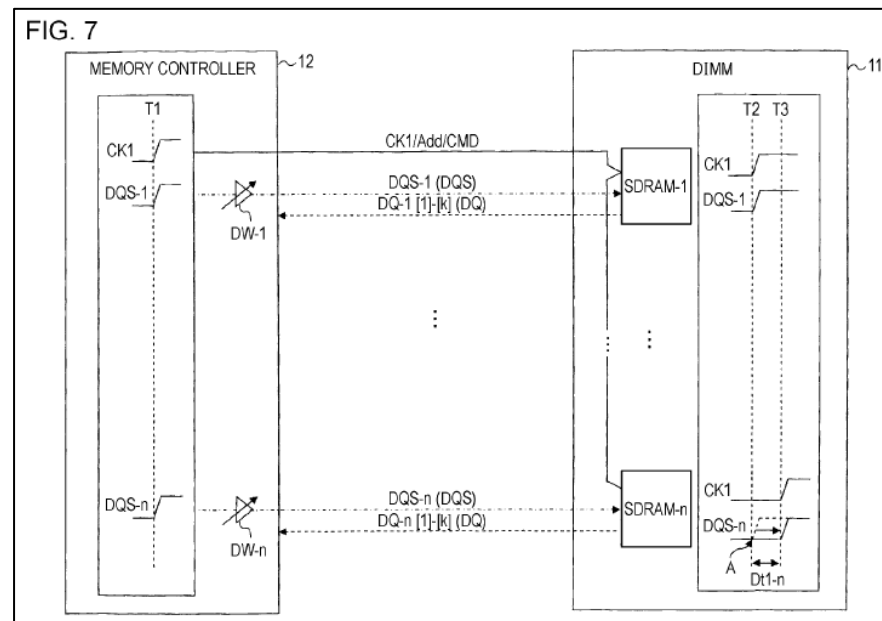
“In this embodiment, it is assumed that the same first delay time $Dt1$ is set for each of the plural SDRAMs of SDRAM-1 to SDRAM-n. More specifically, a



“In this embodiment, it is assumed that the same first delay time $Dt1$ is set for each of the plural SDRAMs of SDRAM-1 to SDRAM-n. More specifically, a

first delay time $Dt1-1$ is set for the three first variable delay circuits DW0, DW1 and DW2 which are included in the control circuit unit 15-1 shown in FIG. 5. Likewise, a first delay time $Dt1-n$ is set for the three first variable delay circuits DW0, DW1 and DW2 which are included in the control circuit unit 15-in shown in FIG. 6.” Tokuhiko at 9:33-40.

“For example, before the first delay time $Dt1$ is adjusted based on the write leveling function, as shown in FIG. 7, the clock signal CK1 and the data strobe signal DQS-1 are input to the 1-channel SDRAM-1 substantially at the same time (see a time “T2 in FIG. 7), while the clock signal CK1 is input (see a time “T3” in FIG.7) to the n-channel SDRAM-n with a delay of the time $Dt1-n$ after the input of the data strobe signal DQS-n (see the time “T2 and a point “A” in FIG. 7).” Tokuhiko at 13:30-37.



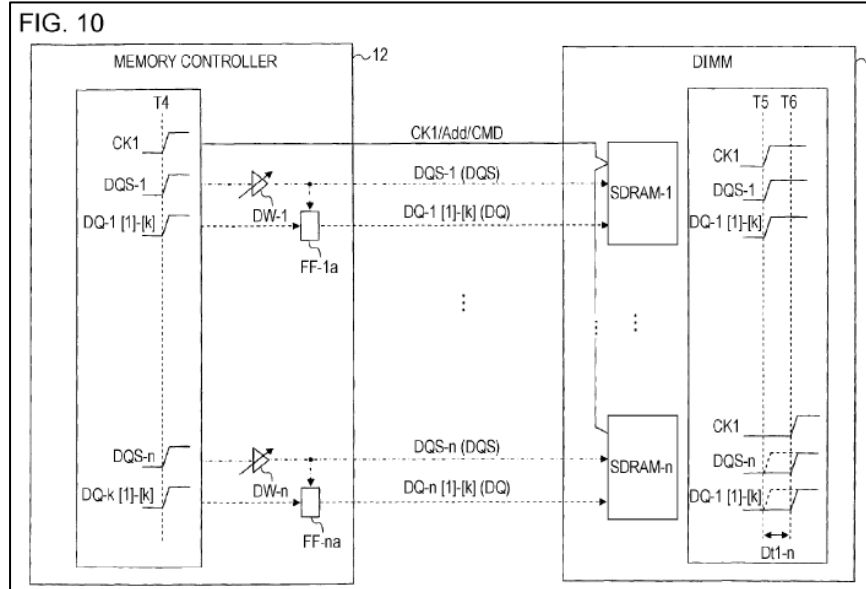
Tokuhiro at Fig. 7.

“Delay (R) $n = \max(\text{Delay}(W)) - \text{Delay}(W)_n$ (3-6)” Tokuhiko at 16:18.

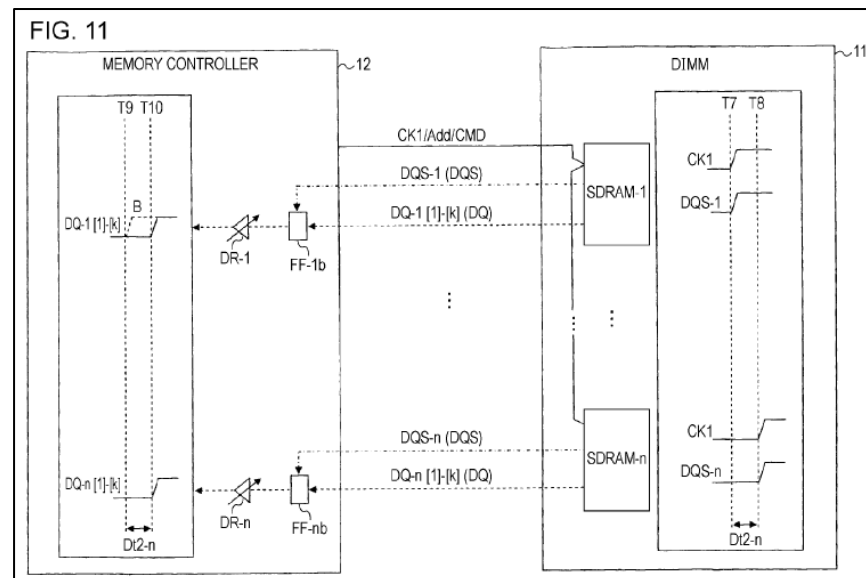
“Thus, the second delay times $Dt2-1$ to $Dt2-n$ corresponding respectively to the SDRAM-1 to the SDRAM-n are set so as to become shorter gradually in the order from the 1-channel SDRAM-1 toward the n-channel SDRAM-n.” Tokuhiko at 16:43-46.

“Thus, with the information processing apparatus 10 according to the first embodiment, for the plurality of SDRAMs of SDRAM-1 to SDRAM-n to which the clock signal line is wired through the daisy chain connection, the input times of the respective data signals DQ output from the SDRAM-1 to the SDRAM-n, to which the clock signal line is wired through the daisy chain

connection, can be easily matched with one another by setting, based on the first delay time Dt1 set by utilizing the write leveling function, the second delay time Dt2 for each data signal DQ input from the SDRAM in the read operation. Accordingly, a failure due to a delay in propagation of the data signal DQ can be prevented in control of the read operation.” Tokuhiro at 18:53-65.



Tokuhiro at Fig. 10.



Tokuhiro at Fig. 11.

“1. A memory control circuit having a write leveling function and controlling read/write operations by supplying a clock signal to a plurality of memories

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	through a clock signal line which is wired to the plurality of memories through daisy chain connection, the memory control circuit comprising: for each of the plurality of memories: a first variable delay unit delaying, in a write operation, a data strobe signal output to the memory by a first delay time that is set by utilizing the write leveling function; and a second variable delay unit delaying, in a read operation, a data signal input from the memory by a second delay time that is set based on the first delay time, wherein the first variable delay unit is constituted by a digital delay circuit which is made up of a plurality of unit circuits connected in series and which delays the data signal output to the memory by the first delay time by passing the data signal through a predetermined number of the unit circuits; and the second variable delay unit is constituted by the digital delay circuit which is made up of the plurality of unit circuits connected in series and which delays the data signal input from the memory by the second delay time by passing the data signal through a predetermined number of the unit circuits.” Tokuhiko at Claim 1. “7. A delay time control device setting a signal delay time in a memory control circuit having a write leveling function and controlling read/write operations by supplying a clock signal to a plurality of memories through a clock signal line which is wired to the plurality of memories through daisy chain connection, the delay time control device comprising: a first delay time controller setting a first delay time of a data strobe signal, which is output to each memory in a write operation, corresponding to each of the plurality of memories by utilizing the write leveling function; and a second delay time controller setting, based on the first delay time set by the first delay time controller, a second delay time of a data signal, which is input from each memory in a read operation, corresponding to each of the plurality of memories, wherein the first delay time controller delays the data signal output to the memory by the first delay time by passing the data signal through a part of a digital delay circuit which is made up of a plurality of unit circuits connected in series; and the second delay time controller delays the data signal input from the memory by the second delay time by passing the data signal through a part of the digital delay circuit which is made up of the plurality of unit circuits connected in series.” Tokuhiko at Claim 7. “9. The delay time control device according to claim 8, wherein the second delay time controller sets the second delay time corresponding to one of the memories such that a sum of the first delay time and the second delay time both corresponding to the one memory is equal to a preset value.”

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	Tokuhiro at Claim 9.
2. The memory module of claim 1, wherein the memory operations include a first memory operation and a second memory operation subsequent to the first memory operation, wherein the command signals include a first set of command signals for the first memory operation and a second set of command signals for the second memory operation, wherein the module control signals include a first set of module control signals output by the module control device in response to the first set of command signals and a second set of module control signals output by the module control device in response to the second set of command signals, wherein the at least one of the module control signals include at least one of the first set of module control signals, and wherein the signal through	Based on Netlist's apparent view of the scope of the '608 patent claims, as articulated in its Infringement Contentions and which I disagree with, it is my opinion that Hiraishi alone or in view of the knowledge of a POSITA or in combination with the referenced prior art discloses claim 2. See claim 1 analysis above. For example, Hiraishi discloses a first memory operation and a second subsequent memory operation (e.g., read/write memory operations), a first set of command signals for the first memory operation and a second set of command signals for the second memory operation (e.g., command signals received by command/address/control register 400), a first set of module control signals in response to the first set of command signals and second set of module control signals in response to the second set of command signals (e.g., signals generated by command/address/control register buffer 400 in response to command signals, for example control signal DRC), and a signal through the data path associated with the second memory operation (e.g., read/write memory operation). FIG. 1 Hiraishi at Fig. 1.

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the data path is a signal associated with the second memory operation.

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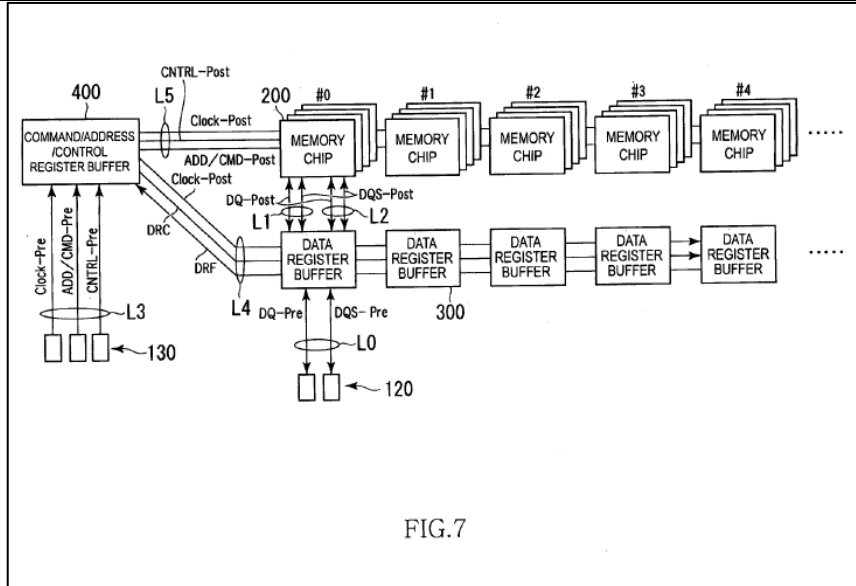


FIG. 7

Hiraishi at Fig. 7.

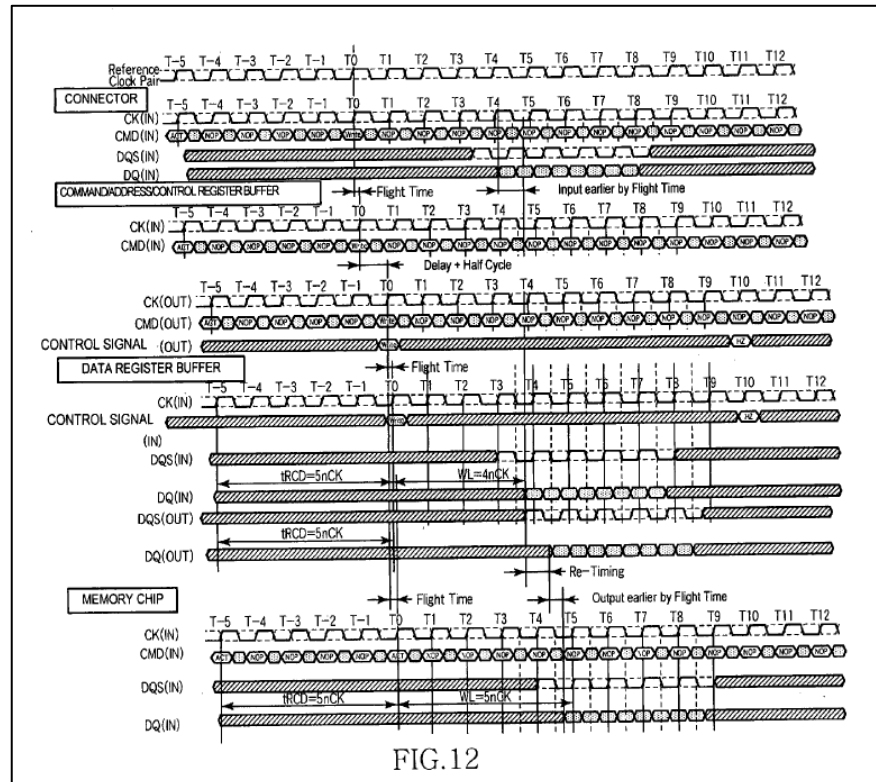


FIG. 12

Hiraishi at Fig. 12.

“As shown in FIG. 19, a read operation timing in a state where both the ODT function and the DLL circuit are set to on is basically the same as the operation timing shown in FIG. 11. In the example shown in FIG. 19, a read command

Read is issued for the Rank0 at the time T0, and another read command Read is issued for the Rank1 at the time T6. Because the memory chip 200 of the Rank0 and the memory chip 200 of the Rank1 are commonly connected to the data line L1, they cause an influence on each other.

Accordingly, in a period from the time T5 to the time T9 during which read data DQ is burst output from the memory chip 200 of the Rank0, an impedance of the data input/output terminal 204 of the memory chip 200 of the Rank1 is set to R_{tt_Nom} by the ODT function. Similarly, in a period from a time T11 to a time T15 during which read data DQ is burst output from the memory chip 200 of the Rank1, an impedance of the data input/output terminal 204 of the memory chip 200 of the Rank0 is set to R_{tt_Nom} by the ODT function.

In this manner, during the read data DQ is output from the memory chip 200 on one side, the memory chip 200 on the other side performs the ODT operation, which prevents a reflection of a signal. However, as described above, current consumption is generated due to the usage of the ODT function and the DLL circuit.” Hiraishi at [0173-0175].

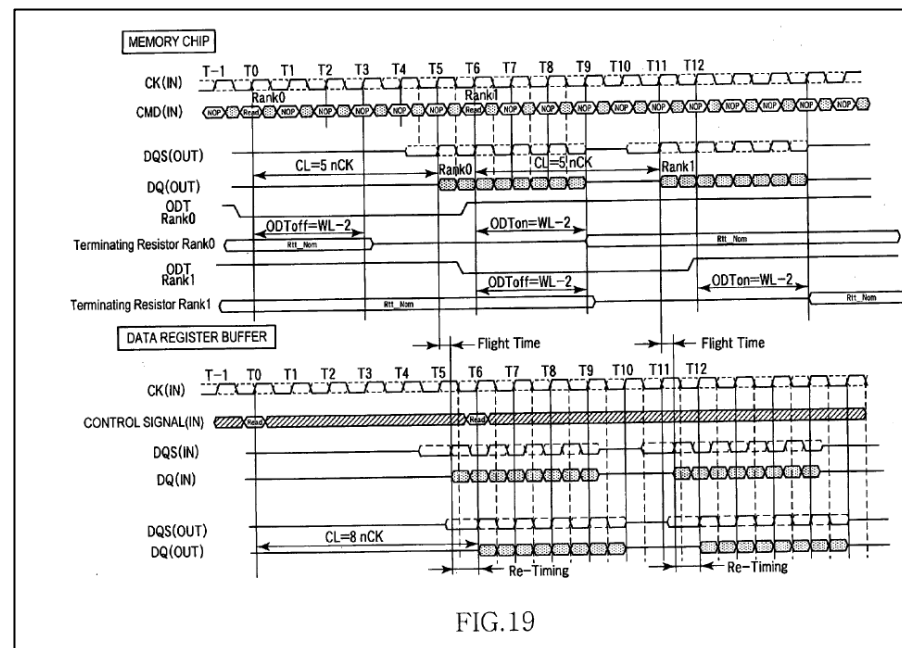


FIG. 19

Hiraishi at Fig. 19.

“FIG. 20 is a timing chart for explaining the read-to-read operation when both the ODT function and the DLL circuit are in an OFF state. As shown in FIG. 20, when the DLL circuit is set to off, an output timing of the read data DQ is asynchronous with the clock signal CK. However, in the present embodiment, because the distance between the memory chip 200 and the data register buffer 300 is considerably short, the data register buffer 300 can correctly

receive the read data DQ that is output in an asynchronous manner. In addition, because the memory chip of the Rank0 and the memory chip of the Rank1 are arranged at substantially the end of the data line L1, an influence of a reflection of a signal from the memory chip 200 on the non-operating side is considerably small. The read data DQ output in an asynchronous manner is subjected to a re-timing by the data register buffer 300, and then output to the memory controller 12.” Hiraishi at [00176-0177].

“As shown in FIG. 21, a write operation timing in a state where both the ODT function and the DLL circuit are set to on is basically the same as the operation timing shown in FIG. 12. In the example shown in FIG. 21, a write command Write is issued for the Rank0 at the time T0, and another write command Write is issued for the Rank1 at the time T6. As described above, because the memory chip 200 of the Rank0 and the memory chip 200 of the Rank1 are commonly connected to the data line L1, they cause an influence on each other. Accordingly, in a period from the time T5 to the time T9 during which write data DQ is burst input to the memory chip 200 of the Rank0, an impedance of the data input/output terminal 204 of the memory chip 200 of the Rank1 is set to Rtt_Nom by the ODT function. Similarly, in a period from the time T11 to the time T15 during which write data DQ is burst input to the memory chip 200 of the Rank1, an impedance of the data input/output terminal 204 of the memory chip 200 of the Rank0 is set to Rtt_Nom by the ODT function.” Hiraishi at [0180-0181].

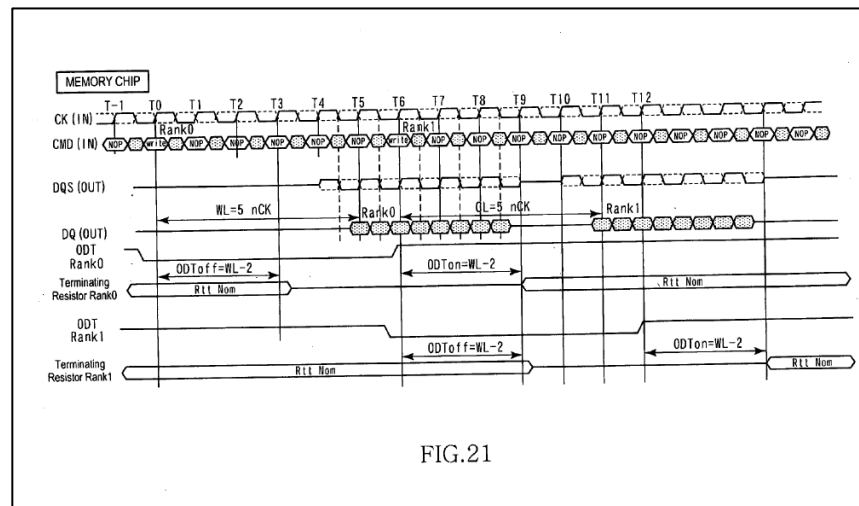
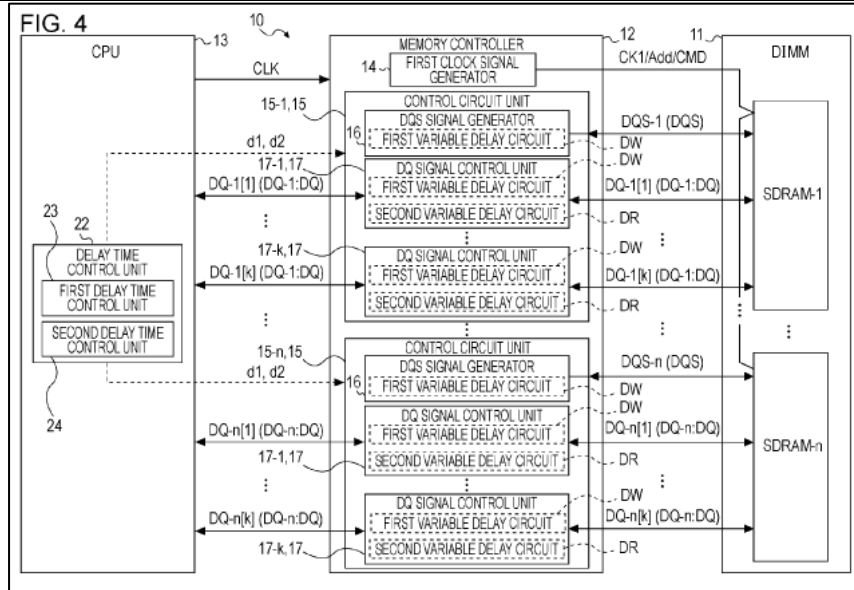


FIG.21

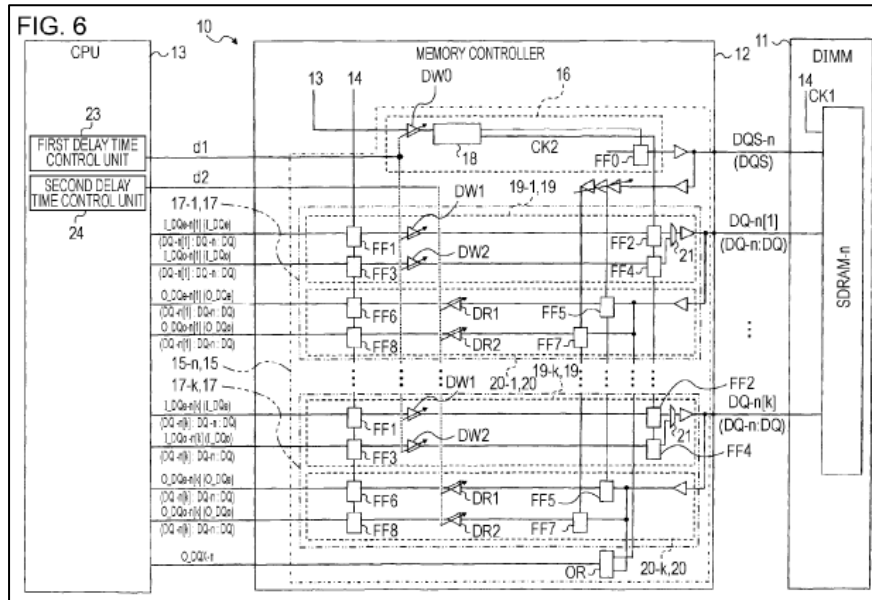
Hiraishi at Fig. 21.

To the extent that this limitation is not present in Hiraishi, which I believe it is, it would have been obvious in view of Tokuhiko.

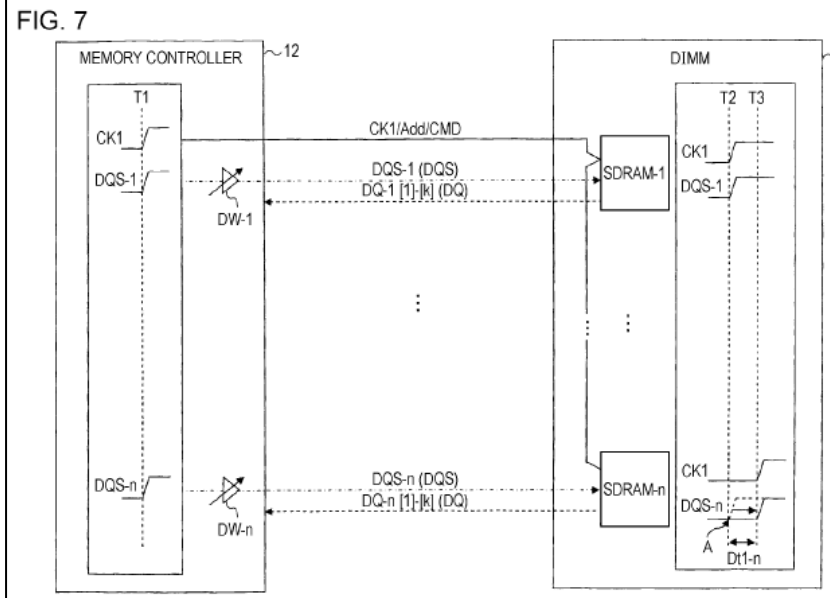
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	“Further, in the first embodiment, fly-by topology is employed for wiring between the memory controller 12 and the plural SDRAMs of SDRAM-1 to SDRAM-n. The term “fly-by topology” refers the daisy chain connection is used as part of the wiring between the memory controller 12 and the plural SDRAMs of SDRAM-1 to SDRAM-n.” Tokuhiro at 5:24-30. “Data signal line for interconnecting the memory controller 12 and the plural SDRAMs of SDRAM-1 to SDRAM-n are connected from the memory controller 12 respectively to the plural SDRAMs of SDRAM-1 to SDRAM-n in parallel. In the exemplary circuit diagram shown in FIG. 5, one DQS signal line (data signal line) for transmitting the data strobe signal DQS and a number k (k is a natural number of 2 or more) of DQ signal lines (data signal lines) for transmitting data signals DQ are connected from the memory controller 12 to each of the plural SDRAMs of SDRAM-1 to SDRAM-n in parallel. Further, those data signal lines are wired in lengths equal to one another (i.e. in the same length). In other words, the plurality of data signal lines connecting the memory controller 12 and the plural SDRAMs of SDRAM-1 to SDRAM-n have the same length.” Tokuhiro at 5:42-56. “The memory controller 12 is a DDR3 (Double Data Rate 3) memory interface for controlling read/write operations by supplying, through the clock signal line, the clock signal CK1 to the plural SDRAMs of SDRAM-1 to SDRAM-n to which the clock signal line is wired through the daisy chain connection. As shown in FIG. 4, by way of example, the memory controller 12 comprises the first clock signal generator 14 and a plurality of control circuit units 15-1 to 15-n.” Tokuhiro at 5:57-64. “The plural control circuit units 15-1 to 15-n are constituted corresponding to the plural SDRAMs of SDRAM-1 to SDRAM-n, respectively. In other words, as shown in FIG. 4, the memory controller 12 includes, for example, the control circuit unit 15-1 corresponding to SDRAM-1 and the control circuit unit 15-n corresponding to SDRAM-n.” Tokuhiro at 6:1-6.



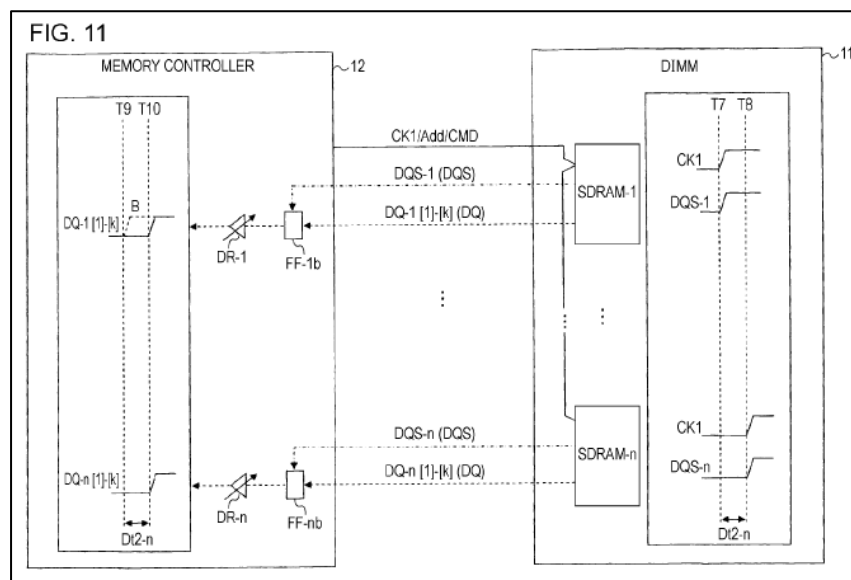
Tokuhiro at Fig. 4.



Tokuhiro at Fig. 6.



Tokuhito at Fig. 7.



Tokuhito at Fig. 11.

“1. A memory control circuit having a write leveling function and controlling read/write operations by supplying a clock signal to a plurality of memories through a clock signal line which is wired to the plurality of memories through daisy chain connection, the memory control circuit comprising:
for each of the plurality of memories:
a first variable delay unit delaying, in a write operation, a data strobe signal output to the memory by a first delay time that is set by utilizing the write leveling function; and

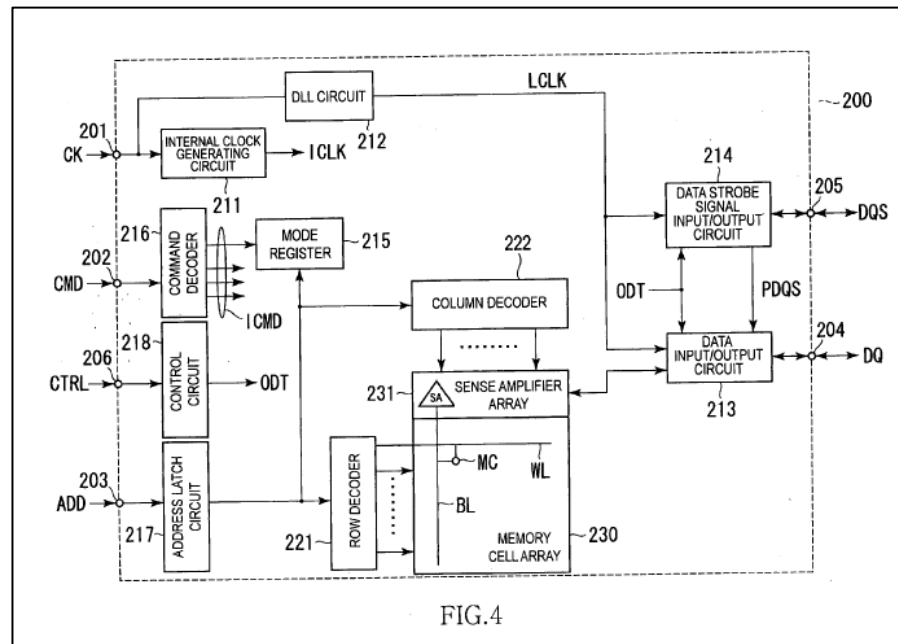
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	a second variable delay unit delaying, in a read operation, a data signal input from the memory by a second delay time that is set based on the first delay time, wherein the first variable delay unit is constituted by a digital delay circuit which is made up of a plurality of unit circuits connected in series and which delays the data signal output to the memory by the first delay time by passing the data signal through a predetermined number of the unit circuits; and the second variable delay unit is constituted by the digital delay circuit which is made up of the plurality of unit circuits connected in series and which delays the data signal input from the memory by the second delay time by passing the data signal through a predetermined number of the unit circuits.” Tokuhiro at Claim 1. “7. A delay time control device setting a signal delay time in a memory control circuit having a write leveling function and controlling read/write operations by supplying a clock signal to a plurality of memories through a clock signal line which is wired to the plurality of memories through daisy chain connection, the delay time control device comprising: a first delay time controller setting a first delay time of a data strobe signal, which is output to each memory in a write operation, corresponding to each of the plurality of memories by utilizing the write leveling function; and a second delay time controller setting, based on the first delay time set by the first delay time controller, a second delay time of a data signal, which is input from each memory in a read operation, corresponding to each of the plurality of memories, wherein the first delay time controller delays the data signal output to the memory by the first delay time by passing the data signal through a part of a digital delay circuit which is made up of a plurality of unit circuits connected in series; and the second delay time controller delays the data signal input from the memory by the second delay time by passing the data signal through a part of the digital delay circuit which is made up of the plurality of unit circuits connected in series.” Tokuhiro at Claim 7. “9. The delay time control device according to claim 8, rein the second delay time controller sets the second delay time corresponding to one of the memories such that a sum of the first delay time and the second delay time both corresponding to the one memory is equal to a preset value.” Tokuhiro at Claim 9. “10. The delay time control device according to claim 8, wherein the second delay time controller sets the second delay time corresponding to one of the memories such that a sum of the first delay time and the second delay time both corresponding to the one memory is equal to a sum of the first delay time and

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	the second delay time both corresponding to another one of the memories.” Tokuhiro at Claims 10. “11. The delay time control device according to claim 8, wherein the second delay time controller sets, as the second delay time corresponding to one of the memories, a difference between the first delay time corresponding to the one memory and a maximum delay time from among the plurality of first delay times corresponding to the plurality of memories.” Tokuhiro at Claim 11.
3. The memory module of claim 2, wherein the memory devices are arranged in a plurality of ranks and the respective set of memory devices include at least one memory device from each of the plurality of ranks, wherein the module command signals include a first set of module command signals output by the module control device in response to the first set of command signals and a second set of module command signals output by the module control device in response to the second set of command signals, and wherein the second set of module command signals include chip select signals that select the at least one memory device in	Based on Netlist’s apparent view of the scope of the ’608 patent claims, as articulated in its Infringement Contentions and which I disagree with, it is my opinion that Hiraishi alone or in view of the knowledge of a POSITA discloses claim 3. See claims 1-2 analysis above. For example, Hiraishi discloses memory devices arranged in a plurality of ranks (e.g., 4-rank configuration), a first and second module command signals output in response to a first and second set of command signals (e.g., signals generated by the command/address/control register buffer 400), and the second set of module command signals including chip select signals that select at least one memory device to perform the second memory operation (e.g., CS signal). FIG. 1 Hiraishi at Fig. 1. “As shown in FIG. 1, the memory module 100 according to the present embodiment includes a module substrate 110, a plurality of memory chips 200 mounted on the module substrate 110, a plurality of data register buffers 300, and a command/address/control register buffer 400.

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the respective set of memory devices from one of the plurality of ranks to perform the second memory operation.	In the present embodiment, the memory module 100 includes thirty-six memory chips 200. When it is necessary to specify each of the memory chips, the memory chips are respectively represented by memory chips 200-0 to 200-35. Furthermore, in the present embodiment, the memory module 100 includes nine data register buffers 300. When it is necessary to specify each of the data register buffers, the data register buffers are respectively represented by data register buffers 300-0 to 300-8. On the other hand, the command/address/control register buffer 400 is provided as a single unit. However, it is not essential to set the number of units of the command/address/control register buffer 400 to one, but two or more units of the command/address/control register buffer 400 can be mounted without any limitation.” Hiraishi at [0045-0046]. “The data connectors 120 are connectors for exchanging write data to be written in the memory chip 200 and read data read from the memory chip 200 between the memory module 100 and the memory controller. Although it is not particularly limited, the number of pins of the data connectors 120 is seventy two in the present embodiment. As shown in FIG. 1, among the seventy-two data connectors 120, data connectors corresponding to the memory chips 200-0 to 200-19 are arranged in an area 110a that is located substantially right below the memory chips 200-0 to 200-19, and data connectors corresponding to the memory chips 200-20 to 200-35 are arranged in an area 110 b that is located substantially right below the memory chips 200-20 to 200-35. The command/address/control connectors 130 are connectors for supplying a command signal, an address signal, a control signal, and a clock signal to be supplied to the command/address/control register buffer 400. As shown in FIG. 1, the command/address/control connectors 130 are arranged in an area 110 c that is located between the area 110 a and the area 110 b.” Hiraishi at [0048-0049]. “The memory chips 200 are, for example, DRAMs. The memory chips 200-0, 200-2, . . . with even branch numbers are mounted on one surface of the module substrate 110 (a first surface), and the memory chips 200-1, 200-3, . . . with odd branch numbers are mounted on the other surface of the module substrate 110 (a second surface). Two corresponding memory chips, for example, the memory chips 200-0 and 200-1 are mounted at positions facing each other across the module substrate 110, respectively.

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	The memory module 100 according to the present embodiment has a so-called 4-Rank configuration. The number of Ranks indicates the number of memory spaces that can be selected in an exclusive manner. Although the same address is assigned to each of the Ranks, one of the Ranks is selected by exclusively activating a chip select (CS) signal or a clock enable (CKE) signal. In the present embodiment, four memory chips 200 constitute a single group (a single set), and the four memory chips 200 constituting the single group belong to different Ranks from each other. For example, the memory chips 200-0 to 200-3 constitute a single group, and the memory chips 200-0 to 200-3 belong to different Ranks from each other. As shown in FIG. 1, the four memory chips 200 constituting a single group are connected to one of the data register buffers 300. For example, the group of the memory chips 200-0 to 200-3 is connected to the data register buffer 300-0. Among the memory chips 200-0 to 200-3, the memory chips 200-0 and 200-1 that are mounted on the upper side of the module substrate 110 are connected to the data register buffer 300-0 via a data line L1, and the memory chips 200-2 and 200-3 that are mounted on the lower side of the module substrate 110 are connected to the data register buffer 300-0 via a data line L2. An arrow of each of the data lines L1 and L2 shown in FIG. 1 indicates a line of 1 byte (8 bits). Both the data lines L1 and L2 are formed inside the module substrate 110.” Hiraishi at [0050-0053]. “An operation of the memory chip 200 is controlled based on the command signal, the address signal, the control signal, and the clock signal supplied from the command/address/control register buffer 400. Details on the memory chip 200 will be described later.” Hiraishi at [0054]. “The command/address/control register buffer 400 receives the command signal, the address signal, the control signal, and the clock signal (in some cases, collectively referred to as a command/address/control signal and the like) that are supplied from the command/address/control connectors 130 through an input terminal 401, buffers the signals, and supplies the signals to the memory chips 200. At the same time, the command/address/control register buffer 400 generates a control signal. The command/address/control signal to be supplied to the memory chips 200 are output through an output terminal 402, and the control signal to be supplied to the data register buffers 300 are output through an output terminal 403.

The output terminal **402** is provided at each of the left side and the right side of the command/address/control register buffer **400**. For example, the output terminal **402** at the left side is commonly connected to the memory chips **200-0** to **200-19** except for a control signal that is used to select the Rank. That is, the command signal, the address signal, and the clock signal are commonly supplied to the memory chips **200-0** to **200-19**. Similarly, the output terminal **403** is provided at each of the left side and the right side of the command/address/control register buffer **400**. For example, the output terminal **403** at the left side is commonly connected to the data register buffers **300-0** to **300-4**, so that the generated control signal is commonly supplied to the data register buffers **300-0** to **300-4**.” Hiraishi at [0060-0061].



Hiraishi at Fig. 4.

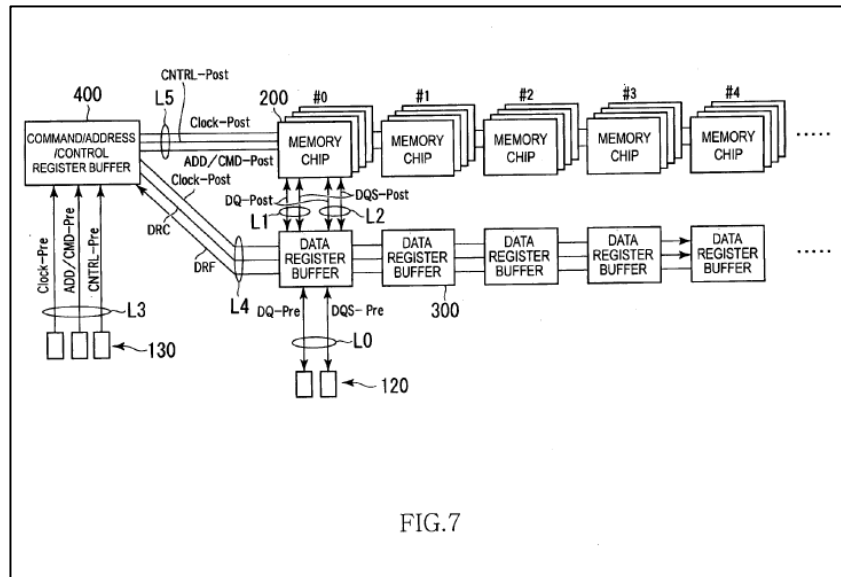
“It is selected based on a set content in a mode register whether to use the DLL circuit **212**. That is, when “DLL on mode” is set in a mode register **215**, the DLL circuit **212** is enabled, so that the internal clock LCLK is phase-controlled with respect to the clock signal CK. On the other hand, when “DLL off mode” is set in the mode register **215**, the DLL circuit **212** is disabled (the clock signal CK is shortcut), so that the internal clock LCLK is not phase-controlled with respect to the clock signal CK.

The command terminal **202** is a terminal to which a command signal CMD that includes a row address strobe (RAS) signal, a column

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	address strobe (CAS) signal, a write enable (WE) signal, and the like is supplied. The control terminal 206 is a terminal to which a control signal CTRL for each Rank, such as a chip select (CS) signal, a clock enable (CKE) signal, and an on die termination (ODT) signal, is supplied. By the chip select (CS) signal, a DRAM for which a command is to be issued is switched, and an activation of a clock system and a control of an on die termination in the DRAM are performed. The command signal CMD is supplied to a command decoder 216. The command decoder 216 is a circuit that generates various internal commands ICMD by storing, decoding, and counting the command signal in synchronization with the internal clock ICLK. The generated internal commands are supplied to various control circuits (not shown) including the mode register 215. The control signal CTRL is supplied to a control circuit 218. The control circuit 218 is a circuit that generates an internal control signal such as the ODT signal based on the control signal CTRL.” Hiraishi at [0075-0076]. “The row decoder 221 is a circuit that selects one of word lines WL included in a memory cell array 230. In the memory cell array 230, a plurality of word lines WL and a plurality of bit lines BL intersect with each other, and a memory cell MC is arranged at each intersection point (only a single word line WL, a single bit line BL, and a single memory cell MC are shown in FIG. 4). The bit line BL is connected to one of sense amplifiers SA that are included in a sense amplifier array 231. The column decoder 222 performs a selection of the sense amplifier SA. The selected sense amplifier SA is connected to the data input/output circuit 213. The internal clock LCLK and an internal data strobe signal PDQS are supplied to the data input/output circuit 213. In a read operation, the data input/output circuit 213 outputs read data in synchronization with the internal clock LCLK, and in a write operation, the data input/output circuit 213 loads write data in synchronization with the internal data strobe signal PDQS. With this arrangement, in the read operation, the read data read out from the memory cell array 230 is output from the data input/output terminal 204, and in the write operation, the write data received from the data input/output terminal 204 is supplied to the memory cell array 230. The data strobe terminal 205 is a terminal for performing input and output of the data strobe signal DQS, which is connected to the data strobe signal input/output circuit 214. The data strobe signal input/output circuit 214 generates the internal data strobe signal PDQS

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	described above, and supplies it to the data input/output circuit 213.” Hiraishi at [0078-0080]. “An output operation timing of the FIFO (Write) circuit 301 is defined by the internal clock LCLKW that is generated by the DLL circuit 310. An output operation timing of the FIFO (Read) circuit 302 is defined by the internal clock LCLKR that is generated by the DLL circuit 310. The DLL circuit 310 is a circuit that generates the internal clocks LCLKW and LCLKR based on the clock signal CK that is supplied from the command/address/control register buffer 400, having the same circuit configuration and function as that of the DLL circuit 212 provided in the memory chip 200. It is selected based on a set content in a data register control circuit 320 whether to use the DLL circuit 310. The DLL circuit 310 can be replaced with a PLL circuit. The data register control circuit 320 is a circuit that controls the operation of the data register buffer 300 based on a control signal DRC that is supplied from the command/address/control register buffer 400. Specifically, the data register control circuit 320 controls operations of an input buffer INB and an output buffer OUTB by generating a buffer control signal BC, and at the same time, controls operations of selectors 331 to 334 by generating a select signal SEL. Contents of controlling the output buffer OUTB include, for example, an adjustment of output impedance and an on/off control of an ODT operation. It is selected based on a set content in a mode register 321 that is included in the data register control circuit 320 whether to use the ODT function.” Hiraishi at [0087-0088]. “The selector 333 is a circuit that supplies data DQ that is an output of the FIFO (Write) circuit 301 to either one of the input/output terminals 341 and 342. The selector 334 is a circuit that selects data DQ input from either one of the input/output terminals 341 and 342 and supplies the selected data DQ to the FIFO (Read) circuit 302. The selectors 331 and 332 perform the similar functions as those of the selectors 333 and 334, respectively. Specifically, the selector 332 selects a data strobe signal DQS input from either one of the input/output terminals 351 and 352. A phase of the selected data strobe signal DQS is delayed by about 90 degrees by a delay circuit 372, and then the data strobe signal DQS is supplied to the FIFO (Read) circuit 302 as an input trigger signal. The selector 331 supplies the data strobe signal DQS that is supplied from the strobe generating circuit 374 to either one of the input/output terminals 351 and 352. A phase of the data strobe signal DQS generated by the strobe generating circuit 374 is delayed by

about **90** degrees with respect to the internal clock LCLKW by a delay circuit **370**. Each of the selections by the selectors **331** to **334** is specified by the select signal SEL that is an output of the data register control circuit **320**.” Hiraishi at [0091].



Hiraishi at Fig. 7.

“FIG. 7 is a connection diagram of the memory module 100 according to the present embodiment. As shown in FIG. 7, in the present embodiment, the data register buffer 300 intervenes between the data connectors 120 and the memory chips 200. The data connectors 120 and the data register buffer 300 are connected to each other with the data line L0, and the data register buffer 300 and the memory chips 200 are connected to each other with the data line L1 or L2. In FIG. 7, a plurality of data transferred through the data line L0 is represented by data DQ-Pre, and a plurality of data transferred through the data lines L1 and L2 is represented by data DQ-Post. Similarly, a data strobe signal transferred through the data line L0 is represented by a data strobe signal DQS-Pre, and a data strobe signal transferred through the data line L1 or L2 is represented by a data strobe signal DQS-Post.” Hiraishi at [0102-0103].

“As described above, in the present embodiment, the four memory chips **200** are allocated to a single data register buffer **300**. The four memory chips **200** are memory chips that constitute different Ranks from each other, which are exclusively activated by the chip select (CS) signal or the clock enable (CKE) signal included in the control signal CTRL. The address signal ADD and the command signal CMD are commonly supplied to the four memory chips **200**.

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	The address signal ADD, the command signal CMD, the control signal CTRL, and the clock signal CK supplied to the memory chips 200 are supplied from the command/address/control register buffer 400. The control signal DRC supplied to the data register buffer 300 is also supplied from the command/address/control register buffer 400.” Hiraishi at [0105-0106]. “As shown in FIG. 7, the command/address/control connectors 130 and the command/address/control register buffer 400 are connected to each other with the command/address/control line L3, the command/address/control register buffer 400 and the data register buffer 300 are connected to each other with a control line L4, and the command/address/control register buffer 400 and the memory chips 200 are connected to each other with a command/address/control line L5. In FIG. 7, a command/address/control signal transferred through the command/address/control line L3 is represented by a command/address signal ADD/CMD-Pre, and a command/address signal transferred through the command/address/control line L5 is represented by a command/address signal ADD/CMD-Post. Similarly, a control signal transferred through the command/address/control line L3 is represented by a control signal CNTRL-Pre, and a control signal transferred through the command/address/control line L5 is represented by a control signal CNTRL-Post.” Hiraishi at [0107]. “As shown in FIGS. 8A and 8B, the 1-bit data is transferred via a predetermined connector 121 of the data connectors 120. The connector 121 is connected to the data register buffer 300 via a single data line L0. As explained above referring to FIG. 5, in the present embodiment, two data lines L1 and L2 are allocated to a single data line L0. Specifically, the data line L1 is commonly connected to the memory chips 200-0 and 200-1, and the data line L2 is commonly connected to the memory chips 200-2 and 200-3. With the above configuration, the load capacity of a single data line L1 or L2 is reduced, the number of branch points decreases, and a line length from a branch point is shortened. As a result, the signal quality of data transferred on the data lines L1 and L2 is enhanced. Specifically, terminals connected to the single data line L1 are only three terminals total including data input/output terminals of the memory chips 200-0 and 200-1 and a data output terminal of the data register buffer 300. Furthermore, because the memory chips 200-0 and 200-1 are arranged facing each other across the module substrate 110, as shown in FIG. 8A, if a branch point P is arranged in an area sandwiched by the memory chips 200-0 and 200-1, the line length from the branch point to each of the memory chips 200-0 and 200-1 is considerably shortened. In addition,

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	because the memory chips 200-0 to 200-3 are mounted at positions close to each other, a perspective difference in edges of the memory chips 200-0 to 200-3 is also suppressed to the minimum.” Hiraishi at [0110-0111]. “FIGS. 9A and 9B are schematic diagrams for explaining a data transfer path for transferring 1-bit data when the data lines L1 and L2 are put together in a single data line, where FIG. 9A is a layout diagram and FIG. 9B is a connection diagram. As shown in FIGS. 9A and 9B, when the data lines L1 and L2 are put together in a single data line L1, the data register buffer 300 and the four memory chips 200-0 to 200-3 are commonly connected with the single data line L1. Therefore, as compared to the configuration shown in FIGS. 8A and 8B, the load capacity of the single data line L1 increases, the number of branch points increases, and the line length from the branch point also increases. Specifically, terminals connected to the single data line L1 become five terminals total including data input/output terminals of the memory chips 200-0 to 200-3 and the data output terminal of the data register buffer 300. In addition, because the configuration becomes such that the line is branched into two at a branch point P1 and further branched into two at a branch point P2, a line length from the branch point P1 to each of the memory chips 200-0 to 200-3 increases. On the other hand, in the present embodiment, because the two data lines L1 and L2 are employed, as shown in FIGS. 8A and 8B, the signal quality of data in the module substrate can be enhanced. Using the two data lines L1 and L2 doubles the number of lines for connecting the memory chips 200 and the data register buffer 300. However, in the present embodiment, because the memory chips 200 and the data register buffer 300 constituting the same group G are arranged in the direction of the short side on the module substrate 110 as explained referring to FIG. 1, there is an enough room for the line space. Therefore, even if the number of lines extending in the direction of the short side is doubled, it is possible to form the lines without difficulty. Meanwhile, when a layout is taken in which data are concentrated in the center of the module substrate, as in the case of the Fully Buffered memory module, it is required to form a plurality of long data lines in the direction of the long side of the module substrate. In such a layout, because the total length of the data lines increases by a considerable amount as compared to the layout of the present embodiment, it is required to take a measure such as significantly increasing the number of insulating layers forming the module substrate in order to double the number of the data lines.. However, according to the present embodiment, because it does not cause such a problem, it is possible to double the number of lines for connecting the memory chips 200 and the data register buffer 300 without increasing the number of insulating layers forming the module substrate 110.” Hiraishi at [0110-0115].

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	“FIG. 10 shows a consecutive read operation from a Rank0 to a Rank3 with a case that a burst length is 4 bits (BL=4) (or a case that a burst operation is stopped at 4 bits by a burst chop). In the example shown in FIG. 10, a read command is issued at times T0, T2, T4, and T6 that are synchronized with the clock signal CK in the order of the Rank0, the Rank2, the Rank1, and the Rank3. In response to these read commands, after a lapse of a predetermined CAS latency (in this example, CL=12), 4-bit read data DQ is burst output. As a result, in a period from a time T12 to a time T14, a data transfer is performed from the memory chip 200 of the Rank0 using the data line L1, in a period from the time T14 to a time T16, a data transfer is performed from the memory chip 200 of the Rank2 using the data line L2, in a period from the time T16 to a time T18, a data transfer is performed from the memory chip 200 of the Rank1 using the data line L1, and in a period from the time T18 to a time T20, a data transfer is performed from the memory chip 200 of the Rank3 using the data line L2. That is, the data lines L1 and L2 are used in an alternate manner.” Hiraishi at [0117-0118]. “In this manner, in the present embodiment, because the interleaving operation can be performed using the two data lines L1 and L2, it is possible to perform a read operation for a plurality of memory chips without interruption. As a result, the read data output from the data register buffer 300 can also be supplied to the memory controller without interruption, so that the usage efficiency of a bus can be enhanced. Although the data lines L1 and L2 are not simultaneously used in the present embodiment, if the data lines L1 and L2 are put together in a single data line, it is required to spare a time equal to or longer than one cycle between read data output from different memory chips. On the other hand, in the present embodiment, because the two data lines L1 and L2 are alternately used, it is not necessary to put a time between read data output from different memory chips. Although the read operation is explained as an example in FIG. 10, a similar interleaving operation can be applied for a write operation. The operation of the memory module 100 according to the present embodiment is explained below in more detail. FIG. 11 is a timing chart for explaining a read operation of the memory module 100 according to the present embodiment. In the read operation, an active command ACT and a read command Read are issued in order from the memory controller 12. In the example shown in FIG. 11, the active command ACT reaches the command/address/control connectors 130 at a time T-5 that is

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	synchronized with the clock signal CK, and the read command Read reaches the command/address/control connectors 130 at a time T0. The commands ACT and Read reaching the command/address/control connectors 130 are input to the command/address/control register buffer 400. At this moment, there occurs a predetermined time difference (Flight Time) between a timing at which the commands ACT and Read reaches the command/address/control connectors 130 and a timing at which the commands ACT and Read are input to the command/address/control register buffer 400. The command/address/control register buffer 400 registers the received commands ACT and Read with an input clock signal in the register circuit 410 shown in FIG. 6, and then outputs them to the memory chip 200. At this time, a synchronization with the output of the commands ACT and Read is taken by delaying the output of the clock signal CK by an amount equivalent to an additional $\frac{1}{2}$ clock cycle. In addition, the command/address/control register buffer 400 supplies a read command Read to the data register buffer 300 as a part of the control signal DRC. The memory chip 200 receives the commands ACT and Read, and starts an actual read operation. At this moment, there occurs a predetermined time difference (Flight Time) between a timing at which the commands ACT and Read are output from the command/address/control register buffer 400 and a timing at which the commands ACT and Read are input to the memory chip 200. Because CL=5 in the example shown in FIG. 11, the memory chip 200 starts a burst output of read data DQ at a time T5 in five clock cycles after receiving the read command Read. In the example shown in FIG. 11, the burst length is 8 bits (BL=8). The read data DQ and a data strobe signal DQS burst output from the memory chip 200 are supplied to the data register buffer 300. The data register buffer 300 loads the read data DQ that is output from the memory chip 200 in the FIFO (Read) circuit 302 with a data strobe signal DQS that is delayed by a predetermined phase amount (for example, phase difference of about 90 degrees). At this moment, there occurs a predetermined time difference (Flight Time) between a timing at which the read data DQ and the data strobe signal DQS are output from the memory chip 200 and a timing at which the read data DQ and the data strobe signal DQS are input to the data register buffer 300.” Hiraishi at [0120-0129].

'608 patent	35 U.S.C. §§ 102, 103 Analysis
	“The data register buffer 300 loads the received write data DQ in the FIFO (Write) circuit 301 with a data strobe signal DQS that is delayed by a predetermined phase amount (for example, phase difference of about 90 degrees). The data register buffer 300 then performs a re-timing in synchronization with the internal clock LCLKW using the FIFO (Write) circuit 301 to convert WL into WL=5, and outputs the write data DQ and the data strobe signal DQS. As described above, the write data is transferred from the data register buffer 300 to the memory chip 200 using either one of the two data lines L1 and L2. The data line to be used is determined by a designated Rank. The memory chip 200 receives the write data DQ that is burst output from the data register buffer 300, and writes it in the memory cell array. At this time, there occurs a predetermined time difference (Flight Time) between a timing at which the write data DQ and the data strobe signal DQS are output from the data register buffer 300 and a timing at which the write data DQ and the data strobe signal DQS are input to the memory chip 200. In consideration of this point, the data register buffer 300 outputs the write data DQ earlier by an amount equivalent to the Flight Time. With this configuration, it becomes possible for the memory chip 200 to receive the write data DQ in a correct manner.” Hiraishi at [0135-0136]. “The memory chip 200 receives the read command Read and performs an actual read operation. In the example shown in FIG. 15, the CAS latency is set to five clock cycles (CL=5), so that an output of read data DQ begins at the time T5. The read data DQ at the time of the read leveling is, for example, a signal in which a High level and a Low level are repeated in an alternate manner.” Hiraishi at [0150]. “As described above, the DLL circuit is a circuit that generates an internal clock signal of which a phase is controlled with respect to an external clock signal, which is used for matching the phases of the read data DQ and the data strobe signal DQS with the phase of the clock signal CK. In a recent high speed memory such as a DDR3 DRAM, a use of the DLL circuit is substantially essential. If the DLL circuit is not used, it is difficult to perform a data transfer in a proper manner. On the other hand, the DLL circuit has a problem of relatively large power consumption.” Hiraishi at [0163]. “However, in the memory module 100 according to the present embodiment, because the load capacities of the data lines L1 and L2 connected to the memory chip 200 are considerably small, even when a high speed memory such as a DDR3 DRAM is used, the ODT operation can be set off in an actual operation. Besides, because a

distance between the memory chip **200** and the data register buffer **300** is considerably short, even if a synchronization control is not performed using a DLL circuit, it is possible to perform a data transfer in a correct manner. That is, because both the ODT function and the DLL circuit can be set to off, it is possible to reduce the power consumption by a considerable amount. In addition, because the ODT function and the DLL circuit can be eliminated from the memory chip **200**, it is also possible to reduce the chip dimension.” Hiraishi at [0170].

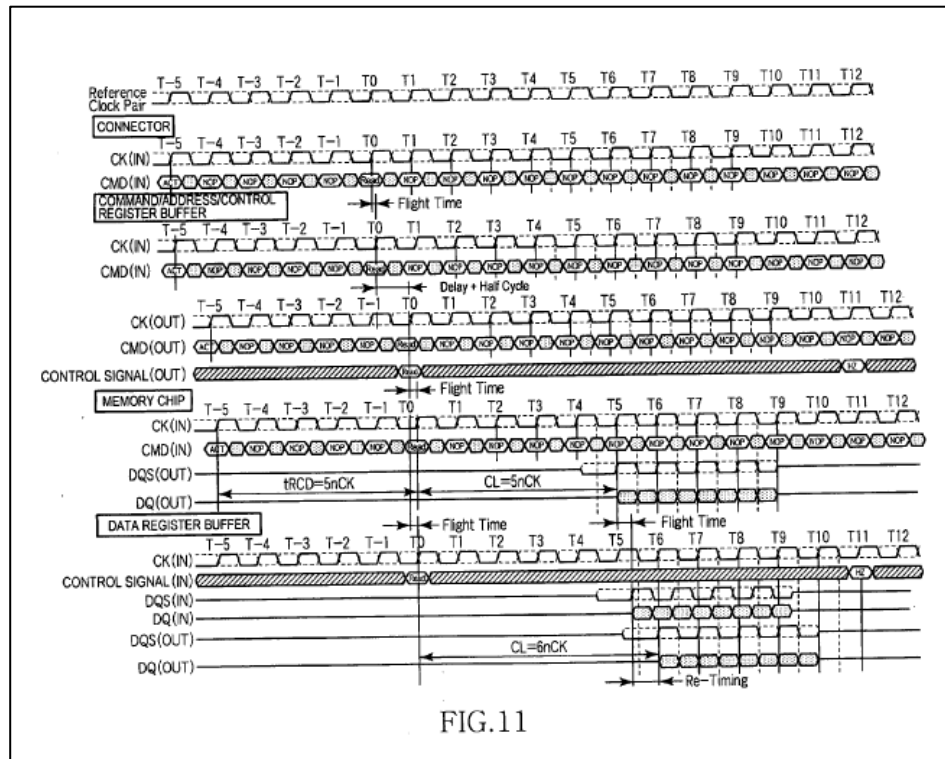
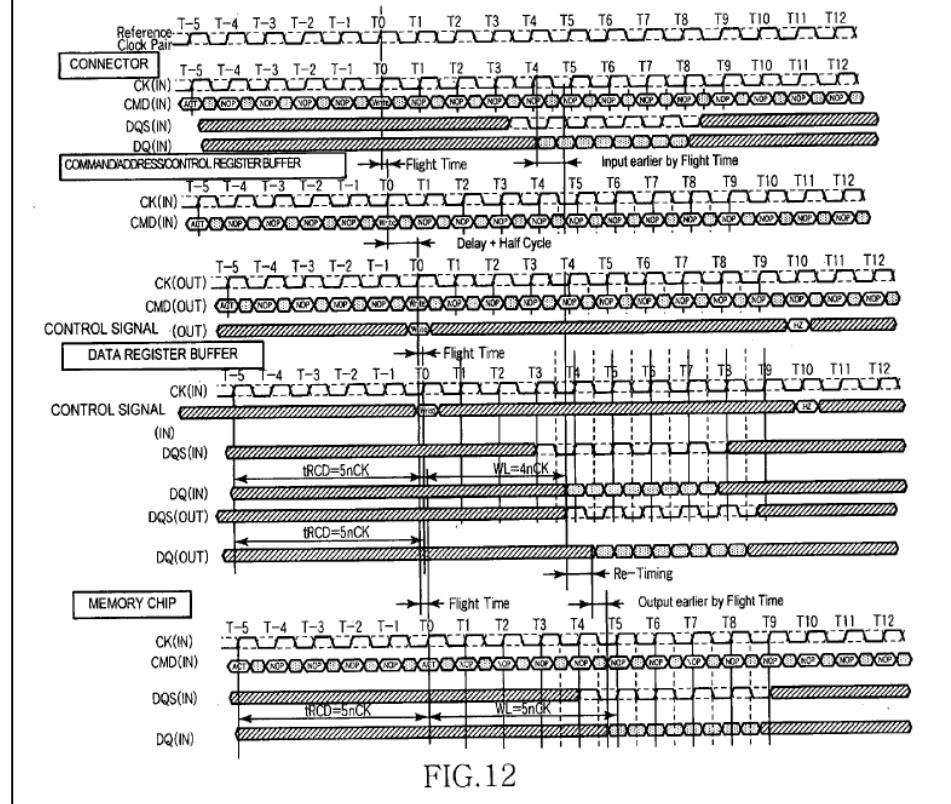


FIG.11

Hiraishi at Fig. 11.



Hiraishi at Fig. 12.

“As shown in FIG. 19, a read operation timing in a state where both the ODT function and the DLL circuit are set to on is basically the same as the operation timing shown in FIG. 11. In the example shown in FIG. 19, a read command Read is issued for the Rank0 at the time T0, and another read command Read is issued for the Rank1 at the time T6. Because the memory chip 200 of the Rank0 and the memory chip 200 of the Rank1 are commonly connected to the data line L1, they cause an influence on each other.

Accordingly, in a period from the time T5 to the time T9 during which read data DQ is burst output from the memory chip 200 of the Rank0, an impedance of the data input/output terminal 204 of the memory chip 200 of the Rank1 is set to Rtt_Nom by the ODT function. Similarly, in a period from a time T11 to a time T15 during which read data DQ is burst output from the memory chip 200 of the Rank1, an impedance of the data input/output terminal 204 of the memory chip 200 of the Rank0 is set to Rtt_Nom by the ODT function.

In this manner, during the read data DQ is output from the memory chip 200 on one side, the memory chip 200 on the other side performs the ODT operation, which prevents a reflection of a signal. However, as described above, current

consumption is generated due to the usage of the ODT function and the DLL circuit.” Hiraishi at [0173-0175].

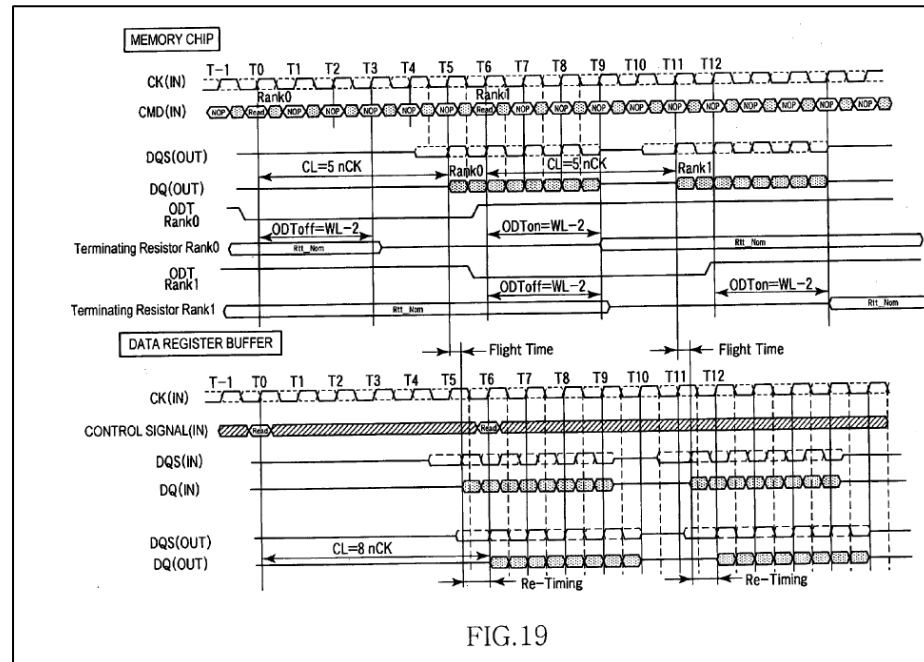


FIG.19

Hiraishi at Fig. 19.

“FIG. 20 is a timing chart for explaining the read-to-read operation when both the ODT function and the DLL circuit are in an OFF state.

As shown in FIG. 20, when the DLL circuit is set to off, an output timing of the read data DQ is asynchronous with the clock signal CK. However, in the present embodiment, because the distance between the memory chip **200** and the data register buffer **300** is considerably short, the data register buffer **300** can correctly receive the read data DQ that is output in an asynchronous manner. In addition, because the memory chip of the Rank0 and the memory chip of the Rank1 are arranged at substantially the end of the data line L1, an influence of a reflection of a signal from the memory chip **200** on the non-operating side is considerably small. The read data DQ output in an asynchronous manner is subjected to a re-timing by the data register buffer **300**, and then output to the memory controller **12**.” Hiraishi at [00176-0177].

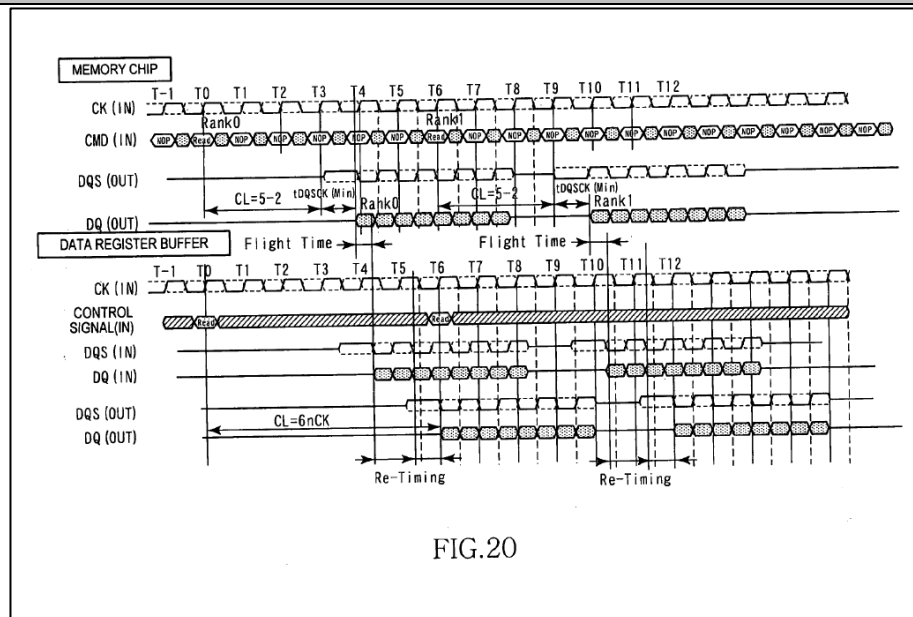
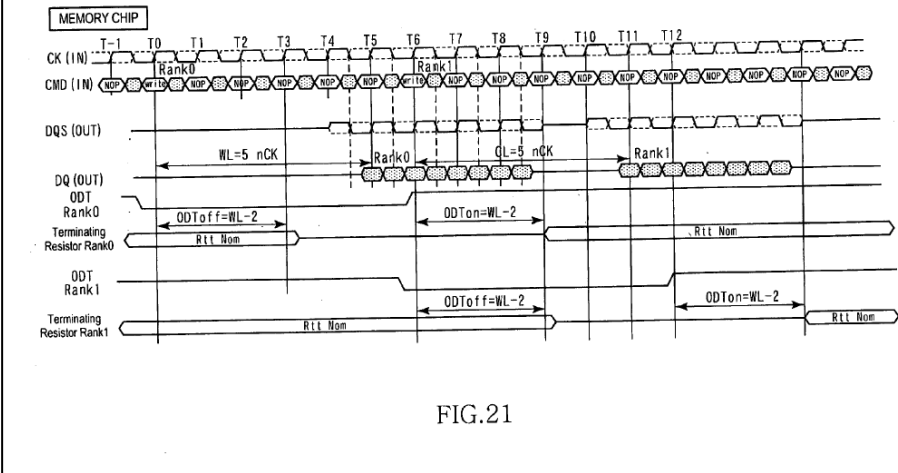


FIG.20

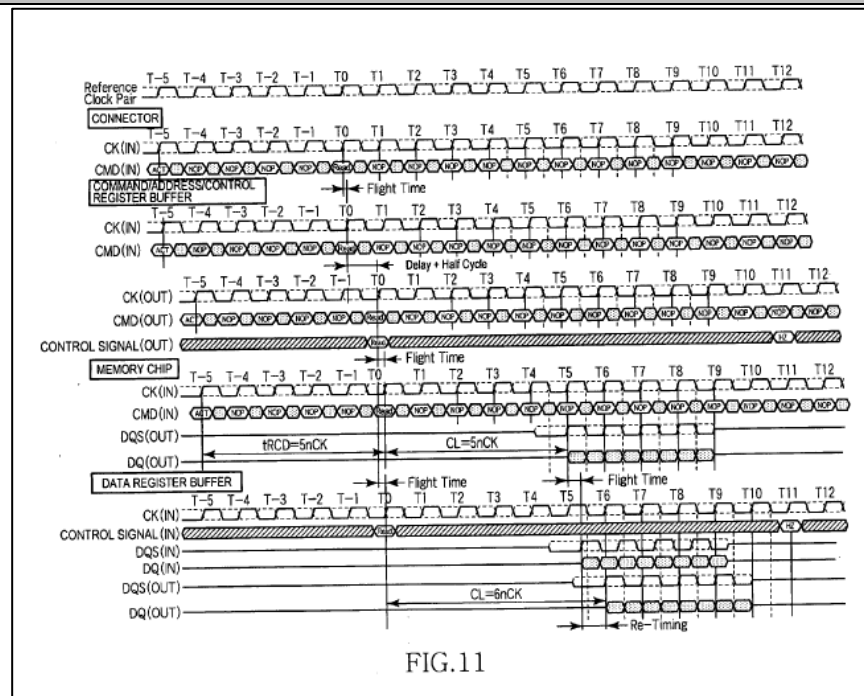
Hiraishi at Fig. 20.

“As shown in FIG. 21, a write operation timing in a state where both the ODT function and the DLL circuit are set to on is basically the same as the operation timing shown in FIG. 12. In the example shown in FIG. 21, a write command Write is issued for the Rank0 at the time T0, and another write command Write is issued for the Rank1 at the time T6. As described above, because the memory chip 200 of the Rank0 and the memory chip 200 of the Rank1 are commonly connected to the data line L1, they cause an influence on each other.

Accordingly, in a period from the time T5 to the time T9 during which write data DQ is burst input to the memory chip 200 of the Rank0, an impedance of the data input/output terminal 204 of the memory chip 200 of the Rank1 is set to Rtt_Nom by the ODT function. Similarly, in a period from the time T11 to the time T15 during which write data DQ is burst input to the memory chip 200 of the Rank1, an impedance of the data input/output terminal 204 of the memory chip 200 of the Rank0 is set to Rtt_Nom by the ODT function.”
Hiraishi at [0180-0181].

'608 patent	35 U.S.C. §§ 102, 103 Analysis
	 FIG.21 Hiraishi at Fig. 21.
4. The memory module of claim 1, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 1 byte.	Based on Netlist's apparent view of the scope of the '608 patent claims, as articulated in its Infringement Contentions and which I disagree with, it is my opinion that Hiraishi alone or in view of the knowledge of a POSITA discloses claim 4. See claim 1 analysis above. For example, Hiraishi discloses each buffer circuit having a data width of 1 byte and each memory device having a data width of 1 byte. "In the present embodiment, four memory chips 200 constitute a single group (a single set), and the four memory chips 200 constituting the single group belong to different Ranks from each other. For example, the memory chips 200-0 to 200-3 constitute a single group, and the memory chips 200-0 to 200-3 belong to different Ranks from each other. As shown in FIG. 1, the four memory chips 200 constituting a single group are connected to one of the data register buffers 300. For example, the group of the memory chips 200-0 to 200-3 is connected to the data register buffer 300-0. Among the memory chips 200-0 to 200-3, the memory chips 200-0 and 200-1 that are mounted on the upper side of the module substrate 110 are connected to the data register buffer 300-0 via a data line L1, and the memory chips 200-2 and 200-3 that are mounted on the lower side of the module substrate 110 are connected to the data register buffer 300-0 via a data line L2. An arrow of each of the data lines L1 and L2 shown in FIG. 1 indicates a line of 1 byte (8 bits). Both the data lines L1 and L2 are formed inside the module substrate 110." Hiraishi at [0052-0053].

'608 patent	35 U.S.C. §§ 102, 103 Analysis
	“A single data register buffer 300 is allocated for every four memory chips 200, as described above, so that nine data register buffers 300 are arranged along the X direction, which is the long side. The data register buffer 300 is a chip for buffering write data that is transferred via a data line L0 and outputting the write data to either one of the data lines L1 and L2, and at the same time, buffering read data that is transferred via either one of the data lines L1 and L2 and outputting the read data to the data line L0. The data line L0 is also formed inside the module substrate 110.” Hiraishi at [0055]. “The memory chip 200 is a DRAM, which includes, as shown in FIG. 4, a clock terminal 201, a command terminal 202, a control terminal 206, an address terminal 203, a data input/output terminal 204, and a data strobe terminal 205 as external terminals. Among these terminals, the clock terminal 201, the command terminal 202, the control terminal 206, and the address terminal 203 are connected to the command/address/control register buffer 400 via a command/address/control line L5 shown in FIG. 1. The data input/output terminal 204 and the data strobe terminal 205 are connected to the data register buffer 300 via the data line L1 or the data line L2 shown in FIG. 1. Although not shown in FIG. 1, the memory chip 200 further includes other terminals such as a power supply terminal.” Hiraishi at [0073]. “The FIFO circuits 301 and 302 shown in FIG. 5 are circuits that perform input and output of 1-bit data, so that in an actual case, the number of sets of the FIFO circuits 301 and 302 as many as a width of input/output data are provided. In the present embodiment, because a single data register buffer 300 inputs and outputs 1-byte data, 8 sets of the FIFO circuits 301 and 302 are required.” Hiraishi at [0085]. “Because CL=5 in the example shown in FIG. 11, the memory chip 200 starts a burst output of read data DQ at a time T5 in five clock cycles after receiving the read command Read. In the example shown in FIG. 11, the burst length is 8 bits (BL=8). The read data DQ and a data strobe signal DQS burst output from the memory chip 200 are supplied to the data register buffer 300.” Hiraishi at [0128].



Hiraishi at Fig. 11.

5. The memory module of claim 1, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 4 bits.

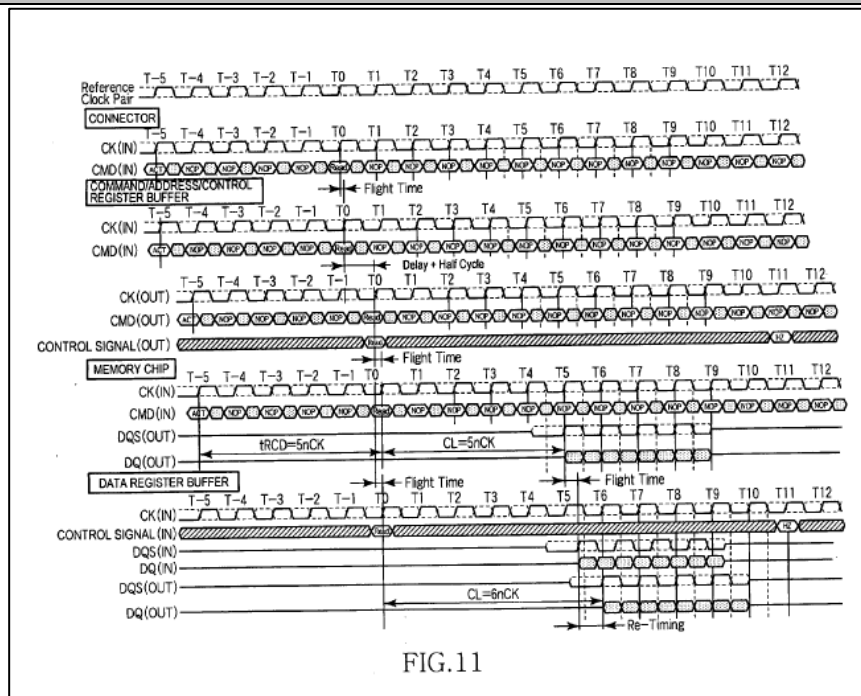
Based on Netlist's apparent view of the scope of the '608 patent claims, as articulated in its Infringement Contentions and which I disagree with, it is my opinion that Hiraishi alone or in view of the knowledge of a POSITA or in combination with the referenced prior art discloses claim 5.

See claim 1 analysis above.

"In the present embodiment, four memory chips **200** constitute a single group (a single set), and the four memory chips **200** constituting the single group belong to different Ranks from each other. For example, the memory chips **200-0** to **200-3** constitute a single group, and the memory chips **200-0** to **200-3** belong to different Ranks from each other.

As shown in FIG. 1, the four memory chips **200** constituting a single group are connected to one of the data register buffers **300**. For example, the group of the memory chips **200-0** to **200-3** is connected to the data register buffer **300-0**. Among the memory chips **200-0** to **200-3**, the memory chips **200-0** and **200-1** that are mounted on the upper side of the module substrate **110** are connected to the data register buffer **300-0** via a data line **L1**, and the memory chips **200-2** and **200-3** that are mounted on the lower side of the module substrate **110** are connected to the data register buffer **300-0** via a data line **L2**. An arrow of each of the data lines **L1** and **L2** shown in FIG. 1 indicates a line of 1 byte (8 bits). Both the data lines **L1** and **L2** are formed inside the module substrate **110**." Hiraishi at [0052-0053].

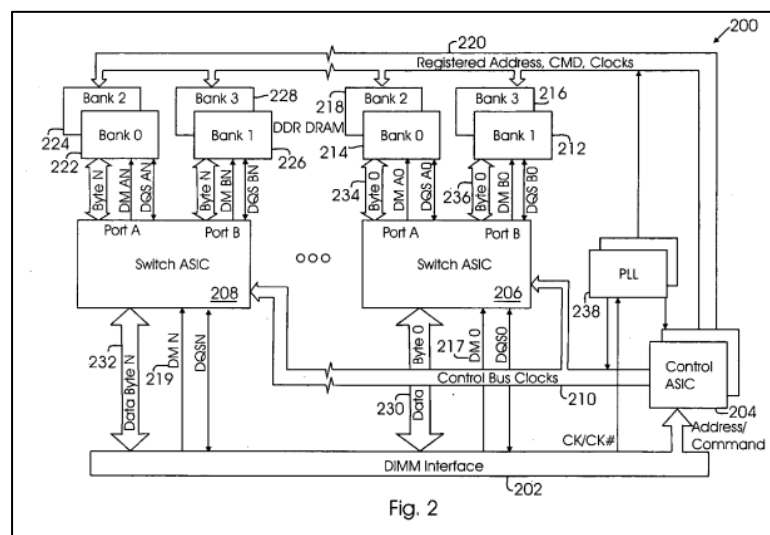
'608 patent	35 U.S.C. §§ 102, 103 Analysis
	“A single data register buffer 300 is allocated for every four memory chips 200, as described above, so that nine data register buffers 300 are arranged along the X direction, which is the long side. The data register buffer 300 is a chip for buffering write data that is transferred via a data line L0 and outputting the write data to either one of the data lines L1 and L2, and at the same time, buffering read data that is transferred via either one of the data lines L1 and L2 and outputting the read data to the data line L0. The data line L0 is also formed inside the module substrate 110.” Hiraishi at [0055]. “The memory chip 200 is a DRAM, which includes, as shown in FIG. 4, a clock terminal 201, a command terminal 202, a control terminal 206, an address terminal 203, a data input/output terminal 204, and a data strobe terminal 205 as external terminals. Among these terminals, the clock terminal 201, the command terminal 202, the control terminal 206, and the address terminal 203 are connected to the command/address/control register buffer 400 via a command/address/control line L5 shown in FIG. 1. The data input/output terminal 204 and the data strobe terminal 205 are connected to the data register buffer 300 via the data line L1 or the data line L2 shown in FIG. 1. Although not shown in FIG. 1, the memory chip 200 further includes other terminals such as a power supply terminal.” Hiraishi at [0073]. “The FIFO circuits 301 and 302 shown in FIG. 5 are circuits that perform input and output of 1-bit data, so that in an actual case, the number of sets of the FIFO circuits 301 and 302 as many as a width of input/output data are provided. In the present embodiment, because a single data register buffer 300 inputs and outputs 1-byte data, 8 sets of the FIFO circuits 301 and 302 are required.” Hiraishi at [0085]. “Because CL=5 in the example shown in FIG. 11, the memory chip 200 starts a burst output of read data DQ at a time T5 in five clock cycles after receiving the read command Read. In the example shown in FIG. 11, the burst length is 8 bits (BL=8). The read data DQ and a data strobe signal DQS burst output from the memory chip 200 are supplied to the data register buffer 300.” Hiraishi at [0128].



Hiraishi at Fig. 11.

A POSITA would have understood that a 1-byte (8-bit) memory device could be replaced with a pair of 4-bit wide memory devices given that this was a standard option at the time.

To the extent that this limitation is not obvious in view of Hiraishi, which I believe it is, it would have been obvious in view of Ellsberry.



Ellsberry at Fig. 2.

“FIGS. 7A-F illustrate an address mapping table, or bank switch state machine, that may be used by the control unit to map a received address (primary address space) to one of the memory banks (secondary address space) according to one embodiment of the invention. FIGS. 8A-B illustrate a command scheme for a control unit to operate multiple banks concurrently according to one embodiment of the invention.” Ellsberry at [0018-0019].

Configuration	Primary Address Space	RC Mode INVERT	Mode	PHY Bank Select	Secondary Address Space
DDR 1,2 X 256M (x4)	BA 0h - 3h Row 0000h - 1FFFh Column 000h - FFFh	X	COLUMN	COL A(12)	BA 0h - 3h Row 0000h-1FFFh Column 000h-7FFh
					BA 0h - 3h Row 0000h-1FFFh Column 800h-FFFh
DDR 1,2 X 256M (x8)	BA 0h - 3h Row 0000h - 1FFFh Column 000h - 7FFh	X	COLUMN	COL A(11)	BA 0h - 3h Row 0000h-1FFFh Column 000h-3FFh
					BA 0h - 3h Row 0000h-1FFFh Column 400h-7FFh
DDR 1,2 X 512M (x4)	BA 0h - 3h Row 0000h - 3FFFh Column 000h - FFFh	X	ROW	ROW A(13)	BA 0h - 3h Row 0000h-1FFFh Column 000h-FFFh
					BA 0h - 3h Row 2000h-3FFFh Column 000h-FFFh

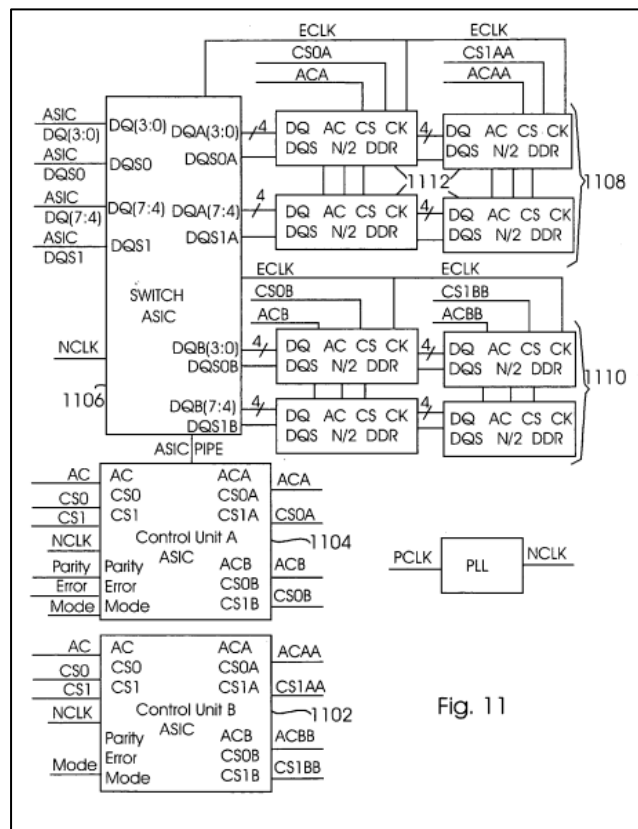
(a) (b) (c) (d) (e) (f) (g)

Fig. 7A

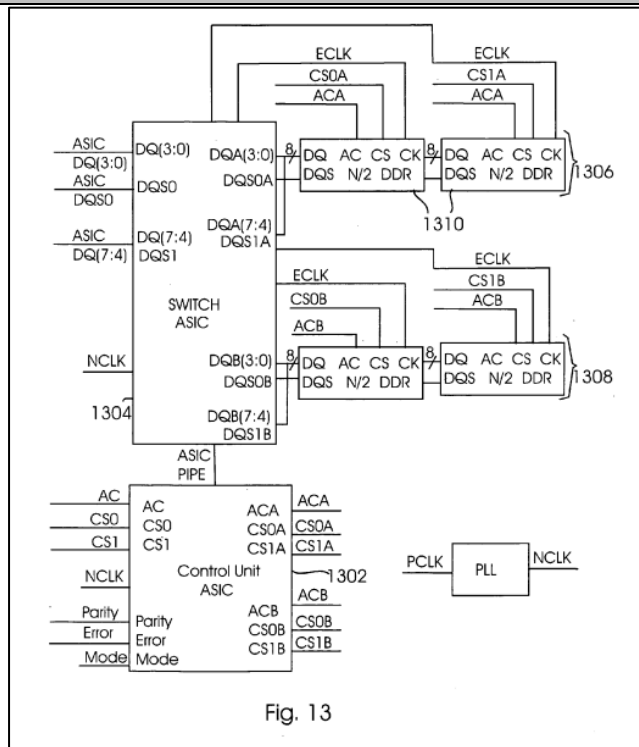
Ellsberry at Fig. 7A.

“According to one embodiment of the invention, the operation of the switch 206/208 and control unit 204 will vary depending on the memory addressing scheme (e.g., column or row addressing) implemented. In column mode operation, to meet system timing requirements, write-data is sent to both ports A and B of the switch 206/208 and control unit 204 uses the data mask (DM) signal to select the target memory device. That is, the DM signal indicates to which target memory device (e.g., Bank 0 214, Bank 1 212, Bank 2 218, or Bank 3 216) the data is written. Note that the DM signal 217/219 at the switch 206/208 is controlled by the control unit 204. Memory read operations, in column mode, work in a similar way as memory write operations. Both memory devices (e.g., Bank 0 214 and Bank 1 212), coupled to ports A and B, are read and the data from the selected target memory device is multiplexed onto the DIMM interface 202. That is, only the data read from the selected target memory device is sent to the DIMM interface 202. Alternatively, when row/bank mode addressing is used, read and write commands are sent only to the targeted memory device. A NOP (no-operation) command is sent to the non-targeted memory device. In one embodiment of the invention, a Serial Presence Detect (SPD) feature is implemented to collect and store the memory module configuration. The memory control configuration is communicated to the host system and stored. The memory module reports the total module

memory capacity and data width along with the individual emulated memory device capacity that is formed by two or more small-capacity memory devices. The Serial Presence Detect operation is a standard feature of many DIMM modules. In one embodiment of the invention, the control unit 204 is configurable via programmable pins (e.g., through logical pull-up or pull-down voltages, etc.) to have information about the type and size of memory devices coupled to the memory banks (e.g., Bank 0, Bank 1, Bank 2 and Bank 3). The control unit 204 is configured to recognize that a plurality of smaller-capacity memory devices is coupled to a particular memory bank switch. The control unit 204 then handles mapping the logical memory addresses it receives via the DIMM interface 202 to a corresponding bank for a particular memory bank coupled to the switches 206 and 208. This same principal is expanded when implementing a wider memory bus formed by several data groups composed of a plurality of memory bank switches and the associated memories." Ellsberry at [0033-0035].



Ellsberry at Fig. 11.



Ellsberry at Fig. 13.

Exhibit D

**UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION**

NETLIST, INC.,	)	
	)	
Plaintiff,	)	
	)	Case No. 2:22-cv-293-JRG
vs.	)	
	)	JURY TRIAL DEMANDED
SAMSUNG ELECTRONICS CO, LTD;	)	(Lead Case)
SAMSUNG ELECTRONICS AMERICA,	)	
INC.; SAMSUNG SEMICONDUCTOR	)	
INC.,	)	
	)	
Defendants.	)	

NETLIST, INC.,	)	
	)	
Plaintiff,	)	
	)	Case No. 2:22-cv-294-JRG
vs.	)	
	)	JURY TRIAL DEMANDED
MICRON TECHNOLOGY, INC.; MICRON	)	
SEMICONDUCTOR PRODUCTS, INC.;	)	
MICRON TECHNOLOGY TEXAS LLC,	)	
	)	
Defendants.	)	

**FIFTH AMENDED
DOCKET CONTROL ORDER**

Before this Court is the parties' Unopposed Joint Motion to Amend the Expert Discovery Deadline. Having considered the same, the Court is of the opinion the motion should be **GRANTED**. Accordingly, the deadlines in the above-captioned cases are amended as follows:

Current Deadline	Amended Deadline	Event
April 15, 2024	No change	*Jury Selection – 9:00 a.m. in Marshall, Texas

7 days before Jury Selection	No change	*Defendant to disclose final invalidity theories, final prior art references/combinations, and final equitable defenses
10 days before Jury Selection	No change	*Plaintiff to disclose final election of asserted claims
March 18, 2024	No change	* If a juror questionnaire is to be used, an editable (in Microsoft Word format) questionnaire shall be jointly submitted to the Deputy Clerk in Charge by this date.
March 11, 2024	No change	* Pretrial Conference – 9:00 am in Marshall, Texas before Judge Roy Payne
March 4, 2024	No change	*Notify Court of Agreements Reached During Meet and Confer The parties are ordered to meet and confer on any outstanding objections or motions <i>in limine</i> . The parties shall advise the Court of any agreements reached no later than 1:00 p.m. three (3) business days before the pretrial conference.
March 4, 2024	No change	*File Joint Pretrial Order, Joint Proposed Jury Instructions, Joint Proposed Verdict Form, Responses to Motions <i>in Limine</i> , Updated Exhibit Lists, Updated Witness Lists, and Updated Deposition Designations
February 26, 2024	No change	*File Notice of Request for Daily Transcript or Real Time Reporting. If a daily transcript or real time reporting of court proceedings is requested for trial, the party or parties making said request shall file a notice with the Court and e-mail the Court Reporter, Shelly Holmes, at shelly_holmes@txed.uscourts.gov .
February 20, 2024	No change	File Motions <i>in Limine</i> The parties shall limit their motions <i>in limine</i> to issues that if improperly introduced at trial would be so prejudicial that the Court could not alleviate the prejudice by giving appropriate instructions to the jury.
February 20, 2024	No change	Serve Objections to Rebuttal Pretrial Disclosures
February 12, 2024	No change	Serve Objections to Pretrial Disclosures; and Serve Rebuttal Pretrial Disclosures
January 29, 2024	No change	Serve Pretrial Disclosures (Witness List, Deposition Designations, and Exhibit List) by the Party with the Burden of Proof

January 30, 2024	No change	*Response to Dispositive Motions (including <i>Daubert</i> Motions). Responses to dispositive motions that were filed <u>prior</u> to the dispositive motion deadline, including <i>Daubert</i> Motions, shall be due in accordance with Local Rule CV-7(e), not to exceed the deadline as set forth in this Docket Control Order. Motions for Summary Judgment shall comply with Local Rule CV-56.
January 16, 2024	No change	*File Motions to Strike Expert Testimony (including <i>Daubert</i> Motions) No motion to strike expert testimony (including a <i>Daubert</i> motion) may be filed after this date without leave of the Court.
January 16, 2024	No change	*File Dispositive Motions No dispositive motion may be filed after this date without leave of the Court. Motions shall comply with Local Rule CV-56 and Local Rule CV-7. <u>Motions to extend page limits will only be granted in exceptional circumstances. Exceptional circumstances require more than agreement among the parties.</u>
January 9, 2024	February 16, 2024	Deadline to Complete Expert Discovery

(*) indicates a deadline that cannot be changed without an acceptable showing of good cause. Good cause is not shown merely by indicating that the parties agree that the deadline should be changed.

I. ADDITIONAL REQUIREMENTS

Mediation: While certain cases may benefit from mediation, such may not be appropriate for every case. The Court finds that the Parties are best suited to evaluate whether mediation will benefit the case after the issuance of the Court's claim construction order. Accordingly, the Court **ORDERS** the Parties to file a Joint Notice indicating whether the case should be referred for mediation **within fourteen days of the issuance of the Court's claim construction order.** As a part of such Joint Notice, the Parties should indicate whether they have a mutually agreeable mediator for the Court to consider. If the Parties disagree about whether mediation is appropriate, the Parties should set forth a brief statement of their competing positions in the Joint Notice.

Summary Judgment Motions, Motions to Strike Expert Testimony, and Daubert Motions: For each motion, the moving party shall provide the Court with two (2) hard copies of the completed briefing (opening motion, response, reply, and if applicable, sur-reply),

excluding exhibits, in D-three-ring binders, appropriately tabbed. All documents shall be single-sided and must include the CM/ECF header. These copies shall be delivered to the Court within three (3) business days after briefing has completed. For expert-related motions, complete digital copies of the relevant expert report(s) and accompanying exhibits shall be submitted on a single flash drive to the Court. Complete digital copies of the expert report(s) shall be delivered to the Court no later than the dispositive motion deadline.

Indefiniteness: In lieu of early motions for summary judgment, the parties are directed to include any arguments related to the issue of indefiniteness in their *Markman* briefing, subject to the local rules' normal page limits.

Lead Counsel: The Parties are directed to Local Rule CV-11(a)(1), which provides that “[o]n the first appearance through counsel, each party shall designate a lead attorney on the pleadings or otherwise.” Additionally, once designated, a party’s lead attorney may only be changed by the filing of a Motion to Change Lead Counsel and thereafter obtaining from the Court an Order granting leave to designate different lead counsel. The true lead counsel should be designated early and should not expect to parachute in as lead once the case has been largely developed.

Motions for Continuance: The following will not warrant a continuance nor justify a failure to comply with the discovery deadline:

- (a) The fact that there are motions for summary judgment or motions to dismiss pending;
- (b) The fact that one or more of the attorneys is set for trial in another court on the same day, unless the other setting was made prior to the date of this order or was made as a special provision for the parties in the other case;
- (c) The failure to complete discovery prior to trial, unless the parties can demonstrate that it was impossible to complete discovery despite their good faith effort to do so.

Amendments to the Docket Control Order (“DCO”): Any motion to alter any date on the DCO shall take the form of a motion to amend the DCO. The motion to amend the DCO shall include a proposed order that lists all of the remaining dates in one column (as above) and the proposed changes to each date in an additional adjacent column (if there is no change for a date the proposed date column should remain blank or indicate that it is unchanged). In other words, the DCO in the proposed order should be complete such that one can clearly see all the remaining deadlines and the changes, if any, to those deadlines, rather than needing to also refer to an earlier version of the DCO.

Proposed DCO: The Parties’ Proposed DCO should also follow the format described above under “Amendments to the Docket Control Order (‘DCO’).”

Joint Pretrial Order: In the contentions of the Parties included in the Joint Pretrial Order, the Plaintiff shall specify all allegedly infringed claims that will be asserted at trial. The Plaintiff shall also specify the nature of each theory of infringement, including under which subsections of 35 U.S.C. § 271 it alleges infringement, and whether the Plaintiff alleges divided infringement or infringement under the doctrine of equivalents. Each Defendant shall

indicate the nature of each theory of invalidity, including invalidity for anticipation, obviousness, subject-matter eligibility, written description, enablement, or any other basis for invalidity. The Defendant shall also specify each prior art reference or combination of references upon which the Defendant shall rely at trial, with respect to each theory of invalidity. The contentions of the Parties may not be amended, supplemented, or dropped without leave of the Court based upon a showing of good cause.

Trial: All parties must appear in person at trial. All non-individual (including but not limited to corporate) parties must appear at trial through the presence in person of a designated representative. Once they have appeared, any representative of a non-individual party shall not be replaced or substituted without express leave of Court.

So ORDERED and SIGNED this 12th day of January, 2024.



RODNEY GILSTRAP
UNITED STATES DISTRICT JUDGE

Exhibit E

From: Daniel Tishman <tishman@fr.com>
Sent: Thursday, February 22, 2024 8:53 PM
To: Tezyan, Michael; Carson, Rebecca; Kate Quisenberry
Cc: Zhao, Yanan; Rueckheim, Mike; Matthew Mosteller; Enzminger, David; #Netlist-Samsung293; jtruelove@mckoolsmith.com; Sam Baxter; FISH SERVICE Samsung/Netlist 22cv00293; tom@gillamsmithlaw.com; EXT Smith, Melissa (T-Mobile); Nester, Brian; Ahn, Alice; jromanow@cov.com; gschmidt@hilgersgraben.com; jhyland@hilgersgraben.com; Winston-Micron-Netlist; ce@wsfirm.com; andrea@wsfirm.com; wh@wsfirm.com; EXT Doan, Jennifer (Amazon); EXT Thane, Josh (Amazon); mhornok@haltomdoan.com; mthornberry@haltomdoan.com
Subject: RE: Netlist/Samsung EDTX 293 - McAlexander Deposition

Thanks Michael –

Mr. McAlexander can be available on March 8th. Please confirm as soon as possible.

Best regards,
Dan

Daniel Tishman :: Fish & Richardson P.C. :: +1 (202) 626-7725

From: Tezyan, Michael <mtezyan@irell.com>
Sent: Thursday, February 22, 2024 7:33 PM
To: Daniel Tishman <tishman@fr.com>; Carson, Rebecca <RCarson@irell.com>; Kate Quisenberry <quisenberry@fr.com>
Cc: Zhao, Yanan <yzhao@irell.com>; Rueckheim, Mike <MRueckheim@winston.com>; Matthew Mosteller <mosteller@fr.com>; Enzminger, David <DENzminger@winston.com>; #Netlist-Samsung293 <Netlist-Samsung293@irell.com>; jtruelove@mckoolsmith.com; Sam Baxter <sbaxter@mckoolsmith.com>; FISH SERVICE Samsung/Netlist 22cv00293 <FISHSERVICESamsung/Netlist22cv00293@fr.com>; tom@gillamsmithlaw.com; melissa@gillamsmithlaw.com; Nester, Brian <BNester@cov.com>; Ahn, Alice <aahn@cov.com>; jromanow@cov.com; gschmidt@hilgersgraben.com; jhyland@hilgersgraben.com; Winston-Micron-Netlist <Winston-Micron-Netlist@winston.com>; ce@wsfirm.com; andrea@wsfirm.com; wh@wsfirm.com; ~Doan, Jennifer <jdoan@haltomdoan.com>; jthane@haltomdoan.com; mhornok@haltomdoan.com; mthornberry@haltomdoan.com
Subject: RE: Netlist/Samsung EDTX 293 - McAlexander Deposition

Dan,

February 26th does not work for Netlist. Please provide an alternative date for Mr. McAlexander.

Thanks,
Michael

Michael Tezyan

Associate

IRELL & MANELLA LLP

1800 Avenue of the Stars, Suite 900

Los Angeles, CA 90067

Direct: (310) 203-7536 | Email: mtezyan@irell.com

From: Daniel Tishman <tishman@fr.com>
Sent: Monday, February 19, 2024 6:39 PM
To: Tezyan, Michael <mtezyan@irell.com>; Carson, Rebecca <RCarson@irell.com>; Kate Quisenberry <quisenberry@fr.com>
Cc: Zhao, Yanan <yzhao@irell.com>; Rueckheim, Mike <MRueckheim@winston.com>; Matthew Mosteller <mosteller@fr.com>; Enzminger, David <DEnzminger@winston.com>; #Netlist-Samsung293 <Netlist-Samsung293@irell.com>; jtruelove@mckoolsmith.com; ~Baxter, Samuel <sbaxter@mckoolsmith.com>; FISH SERVICE Samsung/Netlist 22cv00293 <FISHSERVICESamsung/Netlist22cv00293@fr.com>; tom@gillamsmithlaw.com; ~Smith, Melissa <melissa@gillamsmithlaw.com>; Nester, Brian <BNester@cov.com>; Ahn, Alice <aahn@cov.com>; jromanow@cov.com; gschmidt@hilgersgraben.com; jhyland@hilgersgraben.com; Winston-Micron-Netlist <Winston-Micron-Netlist@winston.com>; ce@wsfirm.com; andrea@wsfirm.com; wh@wsfirm.com; ~Doan, Jennifer <jdoan@haltomdoan.com>; jthane@haltomdoan.com; mhornok@haltomdoan.com; mthornberry@haltomdoan.com
Subject: RE: Netlist/Samsung EDTX 293 - McAlexander Deposition

Counsel:

Mr. McAlexander is available for a rescheduled deposition on February 26th.

Best regards,
Dan

Daniel Tishman :: Fish & Richardson P.C. :: +1 (202) 626-7725

From: Tezyan, Michael <mtezyan@irell.com>
Sent: Thursday, February 15, 2024 6:48 PM
To: Daniel Tishman <tishman@fr.com>; Carson, Rebecca <RCarson@irell.com>; Kate Quisenberry <quisenberry@fr.com>
Cc: Zhao, Yanan <yzhao@irell.com>; Rueckheim, Mike <MRueckheim@winston.com>; Matthew Mosteller <mosteller@fr.com>; Enzminger, David <DEnzminger@winston.com>; #Netlist-Samsung293 <Netlist-Samsung293@irell.com>; jtruelove@mckoolsmith.com; Sam Baxter <sbaxter@mckoolsmith.com>; FISH SERVICE Samsung/Netlist 22cv00293 <FISHSERVICESamsung/Netlist22cv00293@fr.com>; tom@gillamsmithlaw.com; melissa@gillamsmithlaw.com; Nester, Brian <BNester@cov.com>; Ahn, Alice <aahn@cov.com>; jromanow@cov.com; gschmidt@hilgersgraben.com; jhyland@hilgersgraben.com; Winston-Micron-Netlist <Winston-Micron-Netlist@winston.com>; ce@wsfirm.com; andrea@wsfirm.com; wh@wsfirm.com; ~Doan, Jennifer <jdoan@haltomdoan.com>; jthane@haltomdoan.com; mhornok@haltomdoan.com; mthornberry@haltomdoan.com
Subject: RE: Netlist/Samsung EDTX 293 - McAlexander Deposition

Dan,

Thanks for letting us know and hope Mr. McAlexander feels better soon.

Best,
Michael

Michael Tezyan

Associate

IRELL & MANELLA LLP

1800 Avenue of the Stars, Suite 900

Los Angeles, CA 90067

Direct: (310) 203-7536 | Email: mtezyan@irell.com

From: Daniel Tishman <tishman@fr.com>
Sent: Thursday, February 15, 2024 3:21 PM
To: Carson, Rebecca <RCarson@irell.com>; Kate Quisenberry <quisenberry@fr.com>
Cc: Zhao, Yanan <yzhao@irell.com>; Rueckheim, Mike <MRueckheim@winston.com>; Matthew Mosteller <mosteller@fr.com>; Enzminger, David <DEnzminger@winston.com>; #Netlist-Samsung293 <Netlist-Samsung293@irell.com>; jtruelove@mckoolsmith.com; ~Baxter, Samuel <sbaxter@mckoolsmith.com>; FISH SERVICE Samsung/Netlist 22cv00293 <FISHSERVICESamsung/Netlist22cv00293@fr.com>; tom@gillamsmithlaw.com; ~Smith, Melissa <melissa@gillamsmithlaw.com>; Nester, Brian <BNester@cov.com>; Ahn, Alice <aahn@cov.com>; jromanow@cov.com; gschmidt@hilgersgraben.com; jhyland@hilgersgraben.com; Winston-Micron-Netlist <Winston-Micron-Netlist@winston.com>; ce@wsfirm.com; andrea@wsfirm.com; wh@wsfirm.com; ~Doan, Jennifer <jdoan@haltomdoan.com>; jthane@haltomdoan.com; mhornok@haltomdoan.com; mthornberry@haltomdoan.com
Subject: Netlist/Samsung EDTX 293 - McAlexander Deposition

Counsel:

We just received an email with a link associated with tomorrow's deposition of Mr. McAlexander, so I wanted to make sure you all saw the email from yesterday indicating that he has fallen ill and will not be able to sit for deposition tomorrow. Please confirm receipt. We will follow up in due course with alternative dates.

Best regards,
Dan

Daniel Tishman :: Fish & Richardson P.C. :: +1 (202) 626-7725

From: Daniel Tishman
Sent: Wednesday, February 14, 2024 7:16 PM
To: 'Carson, Rebecca' <RCarson@irell.com>; Kate Quisenberry <quisenberry@fr.com>
Cc: Zhao, Yanan <yzhao@irell.com>; Rueckheim, Mike <MRueckheim@winston.com>; Matthew Mosteller <mosteller@fr.com>; Enzminger, David <DEnzminger@winston.com>; #Netlist-Samsung293 <Netlist-Samsung293@irell.com>; jtruelove@mckoolsmith.com; Sam Baxter <sbaxter@mckoolsmith.com>; FISH SERVICE Samsung/Netlist 22cv00293 <FISHSERVICESamsung/Netlist22cv00293@fr.com>; tom@gillamsmithlaw.com; melissa@gillamsmithlaw.com; Nester, Brian <BNester@cov.com>; Ahn, Alice <aahn@cov.com>; jromanow@cov.com; gschmidt@hilgersgraben.com; jhyland@hilgersgraben.com; Winston-Micron-Netlist <Winston-Micron-Netlist@winston.com>; ce@wsfirm.com; andrea@wsfirm.com; wh@wsfirm.com; ~Doan, Jennifer <jdoan@haltomdoan.com>; jthane@haltomdoan.com; mhornok@haltomdoan.com; mthornberry@haltomdoan.com
Subject: RE: Samsung/Netlist EDTX -293 - Expert Deposition Dates

Counsel:

Unfortunately, Mr. McAlexander has fallen ill and is unavailable for deposition on Friday February 16th. We are working with him to identify alternative dates and will follow up in due course.

Best regards,
Dan

Daniel Tishman :: Fish & Richardson P.C. :: +1 (202) 626-7725

From: Carson, Rebecca <RCarson@irell.com>
Sent: Friday, February 02, 2024 10:49 AM
To: Kate Quisenberry <quisenberry@fr.com>
Cc: Zhao, Yanan <yzhao@irell.com>; Daniel Tishman <tishman@fr.com>; Rueckheim, Mike <MRueckheim@winston.com>; Matthew Mosteller <mosteller@fr.com>; Enzminger, David <DEnzminger@winston.com>; #Netlist-Samsung293 <Netlist-Samsung293@irell.com>; jtruelove@mckoolsmith.com; Sam Baxter <sbaxter@mckoolsmith.com>; FISH SERVICE Samsung/Netlist 22cv00293 <FISHSERVICESamsung/Netlist22cv00293@fr.com>; tom@gillamsmithlaw.com; melissa@gillamsmithlaw.com; Nester, Brian <BNester@cov.com>; Ahn, Alice <aahn@cov.com>; jromanow@cov.com; gschmidt@hilgersgraben.com; jhyland@hilgersgraben.com; Winston-Micron-Netlist <Winston-Micron-Netlist@winston.com>; ce@wsfirm.com; andrea@wsfirm.com; wh@wsfirm.com; ~Doan, Jennifer <jdoan@haltomdoan.com>; jthane@haltomdoan.com; mhornok@haltomdoan.com; mthornberry@haltomdoan.com
Subject: Re: Samsung/Netlist EDTX -293 - Expert Deposition Dates

Hi Kate,

We can accept the dates for McAlexander and Halbert. We can also accept the date for Perryman but will need to start no earlier than 9 Pacific. Please let us know if that works.

Regards,
Rebecca

On Feb 2, 2024, at 7:17 AM, Kate Quisenberry <quisenberry@fr.com> wrote:

Rebecca,

Following up on the below, and in light of the postponement of the Micron trial, please confirm Dr. Perryman's deposition next week and the deposition of Samsung's other experts the following week.

Best,
Kate

Kathryn A. Quisenberry :: Fish & Richardson P.C. :: 713 654 5355

From: Kate Quisenberry <quisenberry@fr.com>
Date: Tuesday, January 30, 2024 at 10:14 AM
To: "Carson, Rebecca" <RCarson@irell.com>, "Zhao, Yanan" <yzhao@irell.com>, Daniel Tishman <tishman@fr.com>, "Rueckheim, Mike" <MRueckheim@winston.com>, Matthew Mosteller <mosteller@fr.com>
Cc: "Enzminger, David" <DEnzminger@winston.com>, #Netlist-Samsung293 <Netlist-Samsung293@irell.com>, "jtruelove@mckoolsmith.com" <jtruelove@mckoolsmith.com>, Sam Baxter <sbaxter@mckoolsmith.com>, FISH SERVICE Samsung/Netlist 22cv00293 <FISHSERVICESamsung/Netlist22cv00293@fr.com>, "tom@gillamsmithlaw.com" <tom@gillamsmithlaw.com>, "melissa@gillamsmithlaw.com" <melissa@gillamsmithlaw.com>, "Nester, Brian" <bnester@cov.com>, "Ahn, Alice" <aahn@cov.com>, "jromanow@cov.com" <jromanow@cov.com>, "gschmidt@hilgersgraben.com" <gschmidt@hilgersgraben.com>, "jhyland@hilgersgraben.com" <jhyland@hilgersgraben.com>, Winston-Micron-Netlist <Winston-Micron-Netlist@winston.com>, "ce@wsfirm.com" <ce@wsfirm.com>, "andrea@wsfirm.com" <andrea@wsfirm.com>, "wh@wsfirm.com" <wh@wsfirm.com>, "~Doan, Jennifer" <jdoan@haltomdoan.com>, "jthane@haltomdoan.com" <jthane@haltomdoan.com>, "mhornok@haltomdoan.com" <mhornok@haltomdoan.com>, "mthornberry@haltomdoan.com" <mthornberry@haltomdoan.com>

Subject: Re: Samsung/Netlist EDTX -293 - Expert Deposition Dates

Hi Rebecca,

Following up on the below, please confirm the dates for the depositions of Samsung's experts. In particular, Dr. Perryman is available on February 7 (next week) for deposition but is not available the week of February 12.

Best,
Kate

Kathryn A. Quisenberry :: Fish & Richardson P.C. :: 713 654 5355

From: Kate Quisenberry <quisenberry@fr.com>

Date: Tuesday, January 23, 2024 at 10:01 AM

To: "Carson, Rebecca" <RCarson@irell.com>, "Zhao, Yanan" <yzhao@irell.com>, Daniel Tishman <tishman@fr.com>, "Rueckheim, Mike" <MRueckheim@winston.com>, Matthew Mosteller <mosteller@fr.com>

Cc: "Enzminger, David" <DEnzminger@winston.com>, #Netlist-Samsung293 <Netlist-Samsung293@irell.com>, "jtruelove@mckoolsmith.com" <jtruelove@mckoolsmith.com>, Sam Baxter <sbaxter@mckoolsmith.com>, FISH SERVICE Samsung/Netlist 22cv00293 <FISHSERVICESamsung/Netlist22cv00293@fr.com>, "tom@gillamsmithlaw.com" <tom@gillamsmithlaw.com>, "melissa@gillamsmithlaw.com" <melissa@gillamsmithlaw.com>, "'Nester, Brian'" <bnester@cov.com>, "'Ahn, Alice'" <aahn@cov.com>, "'jromanow@cov.com'" <jromanow@cov.com>, "'gschmidt@hilgersgraben.com'" <gschmidt@hilgersgraben.com>, "'jhyland@hilgersgraben.com'" <jhyland@hilgersgraben.com>, Winston-Micron-Netlist <Winston-Micron-Netlist@winston.com>, "ce@wsfirm.com" <ce@wsfirm.com>, "andrea@wsfirm.com" <andrea@wsfirm.com>, "wh@wsfirm.com" <wh@wsfirm.com>, "~Doan, Jennifer" <jdoan@haltomdoan.com>, "'jthane@haltomdoan.com'" <jthane@haltomdoan.com>, "'mhornok@haltomdoan.com'" <mhornok@haltomdoan.com>, "'mthornberry@haltomdoan.com'" <mthornberry@haltomdoan.com>

Subject: Re: Samsung/Netlist EDTX -293 - Expert Deposition Dates

Hi Rebecca,

Further to the below, Samsung's other experts (Halbert and McAlexander) are available for deposition on February 16. Please confirm as soon as possible.

Best,
Kate

Kathryn A. Quisenberry :: Fish & Richardson P.C. :: 713 654 5355

From: Kate Quisenberry <quisenberry@fr.com>

Date: Monday, January 22, 2024 at 11:26 AM

To: "Carson, Rebecca" <RCarson@irell.com>, "Zhao, Yanan" <yzhao@irell.com>, Daniel Tishman <tishman@fr.com>, "Rueckheim, Mike" <MRueckheim@winston.com>, Matthew Mosteller <mosteller@fr.com>

Cc: "Enzminger, David" <DEnzminger@winston.com>, #Netlist-Samsung293 <Netlist-Samsung293@irell.com>, "jtruelove@mckoolsmith.com" <jtruelove@mckoolsmith.com>, Sam Baxter <sbaxter@mckoolsmith.com>, FISH SERVICE Samsung/Netlist 22cv00293 <FISHSERVICESamsung/Netlist22cv00293@fr.com>, "tom@gillamsmithlaw.com" <tom@gillamsmithlaw.com>, "melissa@gillamsmithlaw.com" <melissa@gillamsmithlaw.com>, "'Nester, Brian'" <bnester@cov.com>, "'Ahn, Alice'" <aahn@cov.com>, "'jromanow@cov.com'" <jromanow@cov.com>, "'gschmidt@hilgersgraben.com'" <gschmidt@hilgersgraben.com>, "'jhyland@hilgersgraben.com'" <jhyland@hilgersgraben.com>, Winston-Micron-Netlist <Winston-Micron-Netlist@winston.com>, "ce@wsfirm.com" <ce@wsfirm.com>, "andrea@wsfirm.com" <andrea@wsfirm.com>, "wh@wsfirm.com" <wh@wsfirm.com>, "~Doan, Jennifer" <jdoan@haltomdoan.com>, "'jthane@haltomdoan.com'" <jthane@haltomdoan.com>, "

""mhornok@haltomdoan.com"" <mhornok@haltomdoan.com>, ""mthornberry@haltomdoan.com""
<mthornberry@haltomdoan.com>

Subject: Re: Samsung/Netlist EDTX -293 - Expert Deposition Dates

Hi Rebecca,

Dr. Perryman is available for deposition on February 7. He is not available the week of February 12. We will follow up with the dates for the other Samsung experts as soon as possible.

Best,
Kate

Kathryn A. Quisenberry :: Fish & Richardson P.C. :: 713 654 5355

From: "Carson, Rebecca" <RCarson@irell.com>

Date: Friday, January 19, 2024 at 12:59 PM

To: Kate Quisenberry <quisenberry@fr.com>, "Zhao, Yanan" <yzhao@irell.com>, Daniel Tishman <tishman@fr.com>, "Rueckheim, Mike" <MRueckheim@winston.com>, Matthew Mosteller <mosteller@fr.com>

Cc: "Enzminger, David" <DEnzminger@winston.com>, #Netlist-Samsung293 <Netlist-Samsung293@irell.com>, "jtruelove@mckoolsmith.com" <jtruelove@mckoolsmith.com>, Sam Baxter <sbaxter@mckoolsmith.com>, FISH SERVICE Samsung/Netlist 22cv00293 <FISHSERVICESamsung/Netlist22cv00293@fr.com>, "tom@gillamsmithlaw.com" <tom@gillamsmithlaw.com>, "melissa@gillamsmithlaw.com" <melissa@gillamsmithlaw.com>, "Nester, Brian" <bnester@cov.com>, "Ahn, Alice" <aahn@cov.com>, "jromanow@cov.com" <jromanow@cov.com>, "gschmidt@hilgersgraben.com" <gschmidt@hilgersgraben.com>, "jhyland@hilgersgraben.com" <jhyland@hilgersgraben.com>, Winston-Micron-Netlist <Winston-Micron-Netlist@winston.com>, "ce@wsfirm.com" <ce@wsfirm.com>, "andrea@wsfirm.com" <andrea@wsfirm.com>, "wh@wsfirm.com" <wh@wsfirm.com>, "~Doan, Jennifer" <jdoan@haltomdoan.com>, "jthane@haltomdoan.com" <jthane@haltomdoan.com>, ""mhornok@haltomdoan.com"" <mhornok@haltomdoan.com>, ""mthornberry@haltomdoan.com"" <mthornberry@haltomdoan.com>

Subject: RE: Samsung/Netlist EDTX -293 - Expert Deposition Dates

Kate - February 15 should work for Ms. Kindler's deposition, assuming the Micron 1 trial does not get pushed to that week (it is currently set for the week of February 5). Could you please provide dates for the other Samsung experts?

Micron Counsel - Could you please provide dates for the Micron expert depositions?

Regards,
Rebecca

From: Kate Quisenberry <quisenberry@fr.com>

Sent: Tuesday, January 9, 2024 6:39 AM

To: Zhao, Yanan <yzhao@irell.com>; Daniel Tishman <tishman@fr.com>; Carson, Rebecca <RCarson@irell.com>; Rueckheim, Mike <MRueckheim@winston.com>; Matthew Mosteller <mosteller@fr.com>

Cc: Enzminger, David <DEnzminger@winston.com>; #Netlist-Samsung293 <Netlist-Samsung293@irell.com>; jtruelove@mckoolsmith.com; ~Baxter, Samuel <sbaxter@mckoolsmith.com>; FISH SERVICE Samsung/Netlist 22cv00293 <FISHSERVICESamsung/Netlist22cv00293@fr.com>; tom@gillamsmithlaw.com; ~Smith, Melissa <melissa@gillamsmithlaw.com>; 'Nester, Brian' <bnester@cov.com>; 'Ahn, Alice' <aahn@cov.com>; 'jromanow@cov.com' <jromanow@cov.com>; 'gschmidt@hilgersgraben.com' <gschmidt@hilgersgraben.com>; 'jhyland@hilgersgraben.com' <jhyland@hilgersgraben.com>; Winston-Micron-Netlist <Winston-Micron-Netlist@winston.com>; ce@wsfirm.com; andrea@wsfirm.com; wh@wsfirm.com; ~Doan, Jennifer <jdoan@haltomdoan.com>; 'jthane@haltomdoan.com' <jthane@haltomdoan.com>; 'mhornok@haltomdoan.com'

<mhornok@haltomdoan.com>; 'mthornberry@haltomdoan.com' <mthornberry@haltomdoan.com>

Subject: Re: Samsung/Netlist EDTX -293 - Expert Deposition Dates

Counsel:

Please let us know what time Netlist's experts (Mangione-Smith, Kennedy, and Gillingham) would like to begin their depositions. Please also note that Samsung intends to take each of these depositions remotely.

Ms. Kindler is available for deposition on February 15. Samsung will follow up with the remainder of its witnesses' availability shortly.

Best,
Kate

Kathryn A. Quisenberry :: Fish & Richardson P.C. :: 713 654 5355

From: "Zhao, Yanan" <yzhao@irell.com<<mailto:yzhao@irell.com>>>

Date: Sunday, January 7, 2024 at 3:51 PM

To: Daniel Tishman <tishman@fr.com<<mailto:tishman@fr.com>>>, "Carson, Rebecca"

<RCarson@irell.com<<mailto:RCarson@irell.com>>>, "Rueckheim, Mike"

<MRueckheim@winston.com<<mailto:MRueckheim@winston.com>>>, Matthew Mosteller

<mosteller@fr.com<<mailto:mosteller@fr.com>>>

Cc: "Enzminger, David" <DEnzminger@winston.com<<mailto:DEnzminger@winston.com>>>, Kate Quisenberry

<quisenberry@fr.com<<mailto:quisenberry@fr.com>>>, #Netlist-Samsung293 <Netlist-Samsung293@irell.com>>, "

jtruelove@mckoolsmith.com<<mailto:jtruelove@mckoolsmith.com>>>, Sam Baxter

<sbaxter@mckoolsmith.com<<mailto:sbaxter@mckoolsmith.com>>>, FISH SERVICE Samsung/Netlist 22cv00293

<FISHSERVICESamsung/Netlist22cv00293@fr.com<<mailto:FISHSERVICESamsung/Netlist22cv00293@fr.com>>>, "

tom@gillamsmithlaw.com<<mailto:tom@gillamsmithlaw.com>>>, "

tom@gillamsmithlaw.com<<mailto:tom@gillamsmithlaw.com>>>, "

melissa@gillamsmithlaw.com<<mailto:melissa@gillamsmithlaw.com>>>, "Nester, Brian"

<melissa@gillamsmithlaw.com<<mailto:melissa@gillamsmithlaw.com>>>, "Nester, Brian"

<bnester@cov.com<<mailto:bnester@cov.com>>>, "Ahn, Alice" <aahn@cov.com<<mailto:aahn@cov.com>>>, "

jromanow@cov.com<<mailto:jromanow@cov.com>>>, "gschmidt@hilgersgraben.com"

<gschmidt@hilgersgraben.com<<mailto:gschmidt@hilgersgraben.com>>>, "jhyland@hilgersgraben.com"

<jhyland@hilgersgraben.com<<mailto:jhyland@hilgersgraben.com>>>, Winston-Micron-Netlist <Winston-Micron-Netlist@winston.com>>, "

ce@wsfirm.com<<mailto:ce@wsfirm.com>>>, "ce@wsfirm.com" <<mailto:ce@wsfirm.com>>>, "

andrea@wsfirm.com<<mailto:andrea@wsfirm.com>>>, "andrea@wsfirm.com" <<mailto:andrea@wsfirm.com>>>, "

wh@wsfirm.com<<mailto:wh@wsfirm.com>>>, "wh@wsfirm.com" <<mailto:wh@wsfirm.com>>>, "

wh@wsfirm.com<<mailto:wh@wsfirm.com>>>, "~Doan, Jennifer"

<jdoan@haltomdoan.com<<mailto:jdoan@haltomdoan.com>>>, "jthane@haltomdoan.com"

<jthane@haltomdoan.com<<mailto:jthane@haltomdoan.com>>>, "mhornok@haltomdoan.com"

<mhornok@haltomdoan.com<<mailto:mhornok@haltomdoan.com>>>, "mthornberry@haltomdoan.com"

<mthornberry@haltomdoan.com<<mailto:mthornberry@haltomdoan.com>>>

Subject: RE: Samsung/Netlist EDTX -293 - Expert Deposition Dates

Thanks, Dan, Mike. We'll get the attached on file this evening.

Best,
Yanan

Yanan Zhao
Associate
Irell & Manella llp
1800 Avenue of the Stars, Suite 900
Los Angeles, CA 90067
DID: 310-277-1010 | yzhao@irell.com<mailto:yzhao@irell.com>

From: Daniel Tishman <tishman@fr.com<mailto:tishman@fr.com>>
Sent: Sunday, January 7, 2024 8:28 AM
To: Carson, Rebecca <RCarson@irell.com<mailto:RCarson@irell.com>>; Rueckheim, Mike <MRueckheim@winston.com<mailto:MRueckheim@winston.com>>; Matthew Mosteller <mosteller@fr.com<mailto:mosteller@fr.com>>
Cc: Zhao, Yanan <yzhao@irell.com<mailto:yzhao@irell.com>>; Enzminger, David <DEnzminger@winston.com<mailto:DEnzminger@winston.com>>; Kate Quisenberry <quisenberry@fr.com<mailto:quisenberry@fr.com>>; #Netlist-Samsung293 <Netlist-Samsung293@irell.com<mailto:Netlist-Samsung293@irell.com>>; jtruelove@mckoolsmith.com<mailto:jtruelove@mckoolsmith.com>; ~Baxter, Samuel <sbaxter@mckoolsmith.com<mailto:sbaxter@mckoolsmith.com>>; FISH SERVICE Samsung/Netlist 22cv00293 <FISHSERVICESamsung/Netlist22cv00293@fr.com<mailto:FISHSERVICESamsung/Netlist22cv00293@fr.com>>; tom@gillamsmithlaw.com<mailto:tom@gillamsmithlaw.com>; ~Smith, Melissa <melissa@gillamsmithlaw.com<mailto:melissa@gillamsmithlaw.com>>; 'Nester, Brian' <BNester@cov.com<mailto:BNester@cov.com>>; 'Ahn, Alice' <aahn@cov.com<mailto:aahn@cov.com>>; 'jromanow@cov.com' <jromanow@cov.com<mailto:jromanow@cov.com>>; 'gschmidt@hilgersgraben.com' <gschmidt@hilgersgraben.com<mailto:gschmidt@hilgersgraben.com>>; 'jhyland@hilgersgraben.com' <jhyland@hilgersgraben.com<mailto:jhyland@hilgersgraben.com>>; Winston-Micron-Netlist <Winston-Micron-Netlist@winston.com<mailto:Winston-Micron-Netlist@winston.com>>; ce@wsfirm.com<mailto:ce@wsfirm.com>; andrea@wsfirm.com<mailto:andrea@wsfirm.com>; wh@wsfirm.com<mailto:wh@wsfirm.com>; ~Doan, Jennifer <jdoan@haltomdoan.com<mailto:jdoan@haltomdoan.com>>; 'jthane@haltomdoan.com' <jthane@haltomdoan.com<mailto:jthane@haltomdoan.com>>; 'mhornok@haltomdoan.com' <mhornok@haltomdoan.com<mailto:mhornok@haltomdoan.com>>; 'mthornberry@haltomdoan.com' <mthornberry@haltomdoan.com<mailto:mthornberry@haltomdoan.com>>
Subject: RE: Samsung/Netlist EDTX -293 - Expert Deposition Dates

This is fine for Samsung, thanks Rebecca.

Dan

Daniel Tishman :: Fish & Richardson P.C. :: +1 (202) 626-7725
From: Carson, Rebecca <RCarson@irell.com<mailto:RCarson@irell.com>>
Sent: Saturday, January 06, 2024 7:55 PM
To: Rueckheim, Mike <MRueckheim@winston.com<mailto:MRueckheim@winston.com>>; Matthew Mosteller <mosteller@fr.com<mailto:mosteller@fr.com>>
Cc: Zhao, Yanan <yzhao@irell.com<mailto:yzhao@irell.com>>; Enzminger, David <DEnzminger@winston.com<mailto:DEnzminger@winston.com>>; Kate Quisenberry <quisenberry@fr.com<mailto:quisenberry@fr.com>>; #Netlist-Samsung293 <Netlist-Samsung293@irell.com<mailto:Netlist-Samsung293@irell.com>>; jtruelove@mckoolsmith.com<mailto:jtruelove@mckoolsmith.com>; Sam Baxter <sbaxter@mckoolsmith.com<mailto:sbaxter@mckoolsmith.com>>; FISH SERVICE Samsung/Netlist 22cv00293 <FISHSERVICESamsung/Netlist22cv00293@fr.com<mailto:FISHSERVICESamsung/Netlist22cv00293@fr.com>>; tom@gillamsmithlaw.com<mailto:tom@gillamsmithlaw.com>;

melissa@gillamsmithlaw.com<<mailto:melissa@gillamsmithlaw.com>>; 'Nester, Brian'
<BNester@cov.com<<mailto:BNester@cov.com>>>; 'Ahn, Alice' <aahn@cov.com<<mailto:aahn@cov.com>>>;
'jromanow@cov.com' <jromanow@cov.com<<mailto:jromanow@cov.com>>>; 'gschmidt@hilgersgraben.com'
<gschmidt@hilgersgraben.com<<mailto:gschmidt@hilgersgraben.com>>>; 'jhyland@hilgersgraben.com'
<jhyland@hilgersgraben.com<<mailto:jhyland@hilgersgraben.com>>>; Winston-Micron-Netlist <Winston-Micron-Netlist@winston.com<<mailto:Winston-Micron-Netlist@winston.com>>>; ce@wsfirm.com<<mailto:ce@wsfirm.com>>>;
andrea@wsfirm.com<<mailto:andrea@wsfirm.com>>; wh@wsfirm.com<<mailto:wh@wsfirm.com>>; ~Doan, Jennifer
<jdoan@haltomdoan.com<<mailto:jdoan@haltomdoan.com>>>; 'jthane@haltomdoan.com'
<jthane@haltomdoan.com<<mailto:jthane@haltomdoan.com>>>; 'mhornok@haltomdoan.com'
<mhornok@haltomdoan.com<<mailto:mhornok@haltomdoan.com>>>; 'mthornberry@haltomdoan.com'
<mthornberry@haltomdoan.com<<mailto:mthornberry@haltomdoan.com>>>
Subject: RE: Samsung/Netlist EDTX -293 - Expert Deposition Dates

Here is an updated motion on the DCO, which adds some language requested by Samsung about the currently-scheduled dates.

From: Rueckheim, Mike <MRueckheim@winston.com<<mailto:MRueckheim@winston.com>>>
Sent: Saturday, January 6, 2024 4:44 PM
To: Carson, Rebecca <RCarson@irell.com<<mailto:RCarson@irell.com>>>; 'Matthew Mosteller'
<mosteller@fr.com<<mailto:mosteller@fr.com>>>
Cc: Zhao, Yanan <yzhao@irell.com<<mailto:yzhao@irell.com>>>; Enzminger, David
<DEnzminger@winston.com<<mailto:DEnzminger@winston.com>>>; 'Kate Quisenberry'
<quisenberry@fr.com<<mailto:quisenberry@fr.com>>>; #Netlist-Samsung293 <Netlist-Samsung293@irell.com<<mailto:Netlist-Samsung293@irell.com>>>; 'jtruelove@mckoolsmith.com'
<jtruelove@mckoolsmith.com<<mailto:jtruelove@mckoolsmith.com>>>; ~Baxter, Samuel
<sbaxter@mckoolsmith.com<<mailto:sbaxter@mckoolsmith.com>>>; 'FISH SERVICE Samsung/Netlist 22cv00293'
<FISHSERVICESamsung/Netlist22cv00293@fr.com<<mailto:FISHSERVICESamsung/Netlist22cv00293@fr.com>>>;
'tom@gillamsmithlaw.com' <tom@gillamsmithlaw.com<<mailto:tom@gillamsmithlaw.com>>>; ~Smith, Melissa
<melissa@gillamsmithlaw.com<<mailto:melissa@gillamsmithlaw.com>>>; 'Nester, Brian'
<BNester@cov.com<<mailto:BNester@cov.com>>>; 'Ahn, Alice' <aahn@cov.com<<mailto:aahn@cov.com>>>;
'jromanow@cov.com' <jromanow@cov.com<<mailto:jromanow@cov.com>>>; 'gschmidt@hilgersgraben.com'
<gschmidt@hilgersgraben.com<<mailto:gschmidt@hilgersgraben.com>>>; 'jhyland@hilgersgraben.com'
<jhyland@hilgersgraben.com<<mailto:jhyland@hilgersgraben.com>>>; Winston-Micron-Netlist <Winston-Micron-Netlist@winston.com<<mailto:Winston-Micron-Netlist@winston.com>>>; ce@wsfirm.com<<mailto:ce@wsfirm.com>>>;
<andrea@wsfirm.com<<mailto:andrea@wsfirm.com>>>; 'wh@wsfirm.com' <wh@wsfirm.com<<mailto:wh@wsfirm.com>>>;
~Doan, Jennifer <jdoan@haltomdoan.com<<mailto:jdoan@haltomdoan.com>>>; 'jthane@haltomdoan.com'
<jthane@haltomdoan.com<<mailto:jthane@haltomdoan.com>>>; 'mhornok@haltomdoan.com'
<mhornok@haltomdoan.com<<mailto:mhornok@haltomdoan.com>>>; 'mthornberry@haltomdoan.com'
<mthornberry@haltomdoan.com<<mailto:mthornberry@haltomdoan.com>>>
Subject: Re: Samsung/Netlist EDTX -293 - Expert Deposition Dates

Sorry I'm away from my computer. Jan 11 works for Gillingham. Please resend the proposed dco

From: Carson, Rebecca <RCarson@irell.com<<mailto:RCarson@irell.com>>>
Sent: Saturday, January 6, 2024 4:19 PM
To: Rueckheim, Mike <MRueckheim@winston.com<<mailto:MRueckheim@winston.com>>>; 'Matthew Mosteller'
<mosteller@fr.com<<mailto:mosteller@fr.com>>>
Cc: Zhao, Yanan <yzhao@irell.com<<mailto:yzhao@irell.com>>>; Enzminger, David
<DEnzminger@winston.com<<mailto:DEnzminger@winston.com>>>; 'Kate Quisenberry'
<quisenberry@fr.com<<mailto:quisenberry@fr.com>>>; #Netlist-Samsung293 <Netlist-Samsung293@irell.com<<mailto:Netlist-Samsung293@irell.com>>>; 'jtruelove@mckoolsmith.com'

<jtruelove@mckoolsmith.com<mailto:jtruelove@mckoolsmith.com>>; ~Baxter, Samuel
<sbaxter@mckoolsmith.com<mailto:sbaxter@mckoolsmith.com>>; 'FISH SERVICE Samsung/Netlist 22cv00293'
<FISHSERVICESamsung/Netlist22cv00293@fr.com<mailto:FISHSERVICESamsung/Netlist22cv00293@fr.com>>;
'tom@gillamsmithlaw.com' <tom@gillamsmithlaw.com<mailto:tom@gillamsmithlaw.com>>; ~Smith, Melissa
<melissa@gillamsmithlaw.com<mailto:melissa@gillamsmithlaw.com>>; 'Nester, Brian'
<BNester@cov.com<mailto:BNester@cov.com>>; 'Ahn, Alice' <aahn@cov.com<mailto:aahn@cov.com>>;
'jromanow@cov.com' <jromanow@cov.com<mailto:jromanow@cov.com>>; 'gschmidt@hilgersgraben.com'
<gschmidt@hilgersgraben.com<mailto:gschmidt@hilgersgraben.com>>; 'jhyland@hilgersgraben.com'
<jhyland@hilgersgraben.com<mailto:jhyland@hilgersgraben.com>>; Winston-Micron-Netlist <Winston-Micron-
Netlist@winston.com<mailto:Winston-Micron-Netlist@winston.com>>; 'ce@wsfirm.com'
<ce@wsfirm.com<mailto:ce@wsfirm.com>>; 'andrea@wsfirm.com'
<andrea@wsfirm.com<mailto:andrea@wsfirm.com>>; 'wh@wsfirm.com' <wh@wsfirm.com<mailto:wh@wsfirm.com>>;
~Doan, Jennifer <jdoan@haltomdoan.com<mailto:jdoan@haltomdoan.com>>; 'jthane@haltomdoan.com'
<jthane@haltomdoan.com<mailto:jthane@haltomdoan.com>>; 'mhornok@haltomdoan.com'
<mhornok@haltomdoan.com<mailto:mhornok@haltomdoan.com>>; 'mthornberry@haltomdoan.com'
<mthornberry@haltomdoan.com<mailto:mthornberry@haltomdoan.com>>
Subject: RE: Samsung/Netlist EDTX -293 - Expert Deposition Dates

Hi Mike,

Given that the current expert fact discovery deadline is Tuesday, we really need Micron to provide a substantive response to us on these issues without further delay. Could you please let us know your position on the Gillingham depo date and the motion to amend the DCO?

If we don't hear from you by the end of today, we will need to file something unilaterally (or just jointly with Samsung), and let the court know that Micron is refusing to engage with us on these issues.

Regards,
Rebecca

From: Rueckheim, Mike <MRueckheim@winston.com<mailto:MRueckheim@winston.com>>
Sent: Friday, January 5, 2024 4:14 PM
To: Carson, Rebecca <RCarson@irell.com<mailto:RCarson@irell.com>>; 'Matthew Mosteller'
<mosteller@fr.com<mailto:mosteller@fr.com>>
Cc: Zhao, Yanan <yzhao@irell.com<mailto:yzhao@irell.com>>; Enzminger, David
<DEnzminger@winston.com<mailto:DEnzminger@winston.com>>; 'Kate Quisenberry'
<quisenberry@fr.com<mailto:quisenberry@fr.com>>; #Netlist-Samsung293 <Netlist-
Samsung293@irell.com<mailto:Netlist-Samsung293@irell.com>>; 'jtruelove@mckoolsmith.com'
<jtruelove@mckoolsmith.com<mailto:jtruelove@mckoolsmith.com>>; ~Baxter, Samuel
<sbaxter@mckoolsmith.com<mailto:sbaxter@mckoolsmith.com>>; 'FISH SERVICE Samsung/Netlist 22cv00293'
<FISHSERVICESamsung/Netlist22cv00293@fr.com<mailto:FISHSERVICESamsung/Netlist22cv00293@fr.com>>;
'tom@gillamsmithlaw.com' <tom@gillamsmithlaw.com<mailto:tom@gillamsmithlaw.com>>; ~Smith, Melissa
<melissa@gillamsmithlaw.com<mailto:melissa@gillamsmithlaw.com>>; 'Nester, Brian'
<BNester@cov.com<mailto:BNester@cov.com>>; 'Ahn, Alice' <aahn@cov.com<mailto:aahn@cov.com>>;
'jromanow@cov.com' <jromanow@cov.com<mailto:jromanow@cov.com>>; 'gschmidt@hilgersgraben.com'
<gschmidt@hilgersgraben.com<mailto:gschmidt@hilgersgraben.com>>; 'jhyland@hilgersgraben.com'
<jhyland@hilgersgraben.com<mailto:jhyland@hilgersgraben.com>>; Winston-Micron-Netlist <Winston-Micron-
Netlist@winston.com<mailto:Winston-Micron-Netlist@winston.com>>; 'ce@wsfirm.com'
<ce@wsfirm.com<mailto:ce@wsfirm.com>>; 'andrea@wsfirm.com'
<andrea@wsfirm.com<mailto:andrea@wsfirm.com>>; 'wh@wsfirm.com' <wh@wsfirm.com<mailto:wh@wsfirm.com>>;
~Doan, Jennifer <jdoan@haltomdoan.com<mailto:jdoan@haltomdoan.com>>; 'jthane@haltomdoan.com'
<jthane@haltomdoan.com<mailto:jthane@haltomdoan.com>>; 'mhornok@haltomdoan.com'

<mhornok@haltomdoan.com<<mailto:mhornok@haltomdoan.com>>>; 'mthornberry@haltomdoan.com'

<mthornberry@haltomdoan.com<<mailto:mthornberry@haltomdoan.com>>>

Subject: RE: Samsung/Netlist EDTX -293 - Expert Deposition Dates

Hi Rebecca, we're working on our response and will respond further tomorrow.

-Mike

Michael R. Rueckheim

Partner

Winston & Strawn LLP

D: +1 650-858-6433

M: +1 713-444-4447

[winston.com](http://www.winston.com)<<http://www.winston.com>>

<image001.jpg>

From: Carson, Rebecca <RCarson@irell.com<<mailto:RCarson@irell.com>>>

Sent: Friday, January 5, 2024 1:09 PM

To: 'Matthew Mosteller' <mosteller@fr.com<<mailto:mosteller@fr.com>>>; Rueckheim, Mike

<MRueckheim@winston.com<<mailto:MRueckheim@winston.com>>>

Cc: Zhao, Yanan <yzhao@irell.com<<mailto:yzhao@irell.com>>>; Enzminger, David

<DEnzminger@winston.com<<mailto:DEnzminger@winston.com>>>; 'Kate Quisenberry'

<quisenberry@fr.com<<mailto:quisenberry@fr.com>>>; #Netlist-Samsung293 <Netlist-Samsung293@irell.com>>; 'jtruelove@mckoolsmith.com'

<jtruelove@mckoolsmith.com<<mailto:jtruelove@mckoolsmith.com>>>; ~Baxter, Samuel

<sbaxter@mckoolsmith.com<<mailto:sbaxter@mckoolsmith.com>>>; 'FISH SERVICE Samsung/Netlist 22cv00293'

<FISHSERVICESamsung/Netlist22cv00293@fr.com<<mailto:FISHSERVICESamsung/Netlist22cv00293@fr.com>>>;

'tom@gillamsmithlaw.com' <tom@gillamsmithlaw.com<<mailto:tom@gillamsmithlaw.com>>>; ~Smith, Melissa

<melissa@gillamsmithlaw.com<<mailto:melissa@gillamsmithlaw.com>>>; 'Nester, Brian'

<BNester@cov.com<<mailto:BNester@cov.com>>>; 'Ahn, Alice' <aahn@cov.com<<mailto:aahn@cov.com>>>;

'jromanow@cov.com' <jromanow@cov.com<<mailto:jromanow@cov.com>>>; 'gschmidt@hilgersgraben.com'

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<ce@wsfirm.com<<mailto:ce@wsfirm.com>>>; 'andrea@wsfirm.com'

<andrea@wsfirm.com<<mailto:andrea@wsfirm.com>>>; 'wh@wsfirm.com' <wh@wsfirm.com<<mailto:wh@wsfirm.com>>>;

~Doan, Jennifer <jdoan@haltomdoan.com<<mailto:jdoan@haltomdoan.com>>>; 'jthane@haltomdoan.com'

<jthane@haltomdoan.com<<mailto:jthane@haltomdoan.com>>>; 'mhornok@haltomdoan.com'

<mhornok@haltomdoan.com<<mailto:mhornok@haltomdoan.com>>>; 'mthornberry@haltomdoan.com'

<mthornberry@haltomdoan.com<<mailto:mthornberry@haltomdoan.com>>>

Subject: RE: Samsung/Netlist EDTX -293 - Expert Deposition Dates

Micron Counsel: Could you please provide the courtesy of responding to my emails below? From: Carson, Rebecca Sent:

Friday, January 5, 2024 9:32 AM To: 'Matthew Mosteller' <mosteller@fr.com<<mailto:mosteller@fr.com>>>; Rueckheim,

Mike <MRueckheim@winston.com<<mailto:MRueckheim@winston.com>>>Cc: Zhao, Yanan <YZhao@irell.com&g

Micron Counsel: Could you please provide the courtesy of responding to my emails below?

From: Carson, Rebecca

Sent: Friday, January 5, 2024 9:32 AM

To: 'Matthew Mosteller' <mosteller@fr.com<<mailto:mosteller@fr.com>>>; Rueckheim, Mike <MRueckheim@winston.com<<mailto:MRueckheim@winston.com>>>

Cc: Zhao, Yanan <YZhao@irell.com<<mailto:YZhao@irell.com>>>; Enzminger, David

<DEnzminger@winston.com<<mailto:DEnzminger@winston.com>>>; Kate Quisenberry

<quisenberry@fr.com<<mailto:quisenberry@fr.com>>>; #Netlist-Samsung293 <Netlist-Samsung293@irell.com<<mailto:Netlist-Samsung293@irell.com>>>;

jtruelove@mckoolsmith.com<<mailto:jtruelove@mckoolsmith.com>>>; ~Baxter, Samuel

<sbaxter@mckoolsmith.com<<mailto:sbaxter@mckoolsmith.com>>>; FISH SERVICE Samsung/Netlist 22cv00293

<FISHSERVICESamsung/Netlist22cv00293@fr.com<<mailto:FISHSERVICESamsung/Netlist22cv00293@fr.com>>>;

tom@gillamsmithlaw.com<<mailto:tom@gillamsmithlaw.com>>>; ~Smith, Melissa

<melissa@gillamsmithlaw.com<<mailto:melissa@gillamsmithlaw.com>>>; Nester, Brian

<BNester@cov.com<<mailto:BNester@cov.com>>>; Ahn, Alice <aahn@cov.com<<mailto:aahn@cov.com>>>;

jromanow@cov.com<<mailto:jromanow@cov.com>>>;

gschmidt@hilgersgraben.com<<mailto:gschmidt@hilgersgraben.com>>>;

jhyland@hilgersgraben.com<<mailto:jhyland@hilgersgraben.com>>>; Winston-Micron-Netlist <Winston-Micron-Netlist@winston.com<<mailto:Winston-Micron-Netlist@winston.com>>>;

ce@wsfirm.com<<mailto:ce@wsfirm.com>>>; andrea@wsfirm.com<<mailto:andrea@wsfirm.com>>>;

wh@wsfirm.com<<mailto:wh@wsfirm.com>>>; ~Doan, Jennifer

<jdoan@haltomdoan.com<<mailto:jdoan@haltomdoan.com>>>;

jthane@haltomdoan.com<<mailto:jthane@haltomdoan.com>>>;

mhornok@haltomdoan.com<<mailto:mhornok@haltomdoan.com>>>;

mthornberry@haltomdoan.com<<mailto:mthornberry@haltomdoan.com>>>

Subject: RE: Samsung/Netlist EDTX -293 - Expert Deposition Dates

Micron Counsel: Please let us know by noon Pacific today whether January 11 works for Mr. Gillingham's deposition, as well as whether Micron is okay with the proposed amendment to the DCO to extend the expert discovery deadline that we circulated, so that we can get it on file today.

From: Matthew Mosteller <mosteller@fr.com<<mailto:mosteller@fr.com>>>

Sent: Friday, January 5, 2024 8:21 AM

To: Carson, Rebecca <RCarson@irell.com<<mailto:RCarson@irell.com>>>; Rueckheim, Mike

<MRueckheim@winston.com<<mailto:MRueckheim@winston.com>>>

Cc: Zhao, Yanan <yzhao@irell.com<<mailto:yzhao@irell.com>>>; Enzminger, David

<DEnzminger@winston.com<<mailto:DEnzminger@winston.com>>>; Kate Quisenberry

<quisenberry@fr.com<<mailto:quisenberry@fr.com>>>; #Netlist-Samsung293 <Netlist-Samsung293@irell.com<<mailto:Netlist-Samsung293@irell.com>>>;

jtruelove@mckoolsmith.com<<mailto:jtruelove@mckoolsmith.com>>>; ~Baxter, Samuel

<sbaxter@mckoolsmith.com<<mailto:sbaxter@mckoolsmith.com>>>; FISH SERVICE Samsung/Netlist 22cv00293

<FISHSERVICESamsung/Netlist22cv00293@fr.com<<mailto:FISHSERVICESamsung/Netlist22cv00293@fr.com>>>;

tom@gillamsmithlaw.com<<mailto:tom@gillamsmithlaw.com>>>; ~Smith, Melissa

<melissa@gillamsmithlaw.com<<mailto:melissa@gillamsmithlaw.com>>>; Nester, Brian

<BNester@cov.com<<mailto:BNester@cov.com>>>; Ahn, Alice <aahn@cov.com<<mailto:aahn@cov.com>>>;

jromanow@cov.com<<mailto:jromanow@cov.com>>>;

gschmidt@hilgersgraben.com<<mailto:gschmidt@hilgersgraben.com>>>;

jhyland@hilgersgraben.com<<mailto:jhyland@hilgersgraben.com>>>; Winston-Micron-Netlist <[Winston-Micron-](mailto:Winston-Micron-Netlist@winston.com)

Netlist@winston.com<<mailto:Winston-Micron-Netlist@winston.com>>>; ce@wsfirm.com<<mailto:ce@wsfirm.com>>;
andrea@wsfirm.com<<mailto:andrea@wsfirm.com>>; wh@wsfirm.com<<mailto:wh@wsfirm.com>>; ~Doan, Jennifer
<jdoan@haltomdoan.com<<mailto:jdoan@haltomdoan.com>>>;
jthane@haltomdoan.com<<mailto:jthane@haltomdoan.com>>;
mhornok@haltomdoan.com<<mailto:mhornok@haltomdoan.com>>;
mthornberry@haltomdoan.com<<mailto:mthornberry@haltomdoan.com>>
Subject: RE: Samsung/Netlist EDTX -293 - Expert Deposition Dates

Rebecca,

Samsung is available to take Mr. Gillingham's deposition on January 11th.

Regards,
Matt

<image002.jpg>

Matthew Mosteller | Fish & Richardson P.C.
1000 Maine Ave SW | Washington DC 20024
Direct: (202) 626-7751 | Main: (202) 783-5070
ü www.fr.com<<http://www.fr.com>> | • mosteller@fr.com<<mailto:mosteller@fr.com>>

From: Carson, Rebecca <RCarson@irell.com<<mailto:RCarson@irell.com>>>
Sent: Friday, January 5, 2024 10:54 AM
To: Rueckheim, Mike <MRueckheim@winston.com<<mailto:MRueckheim@winston.com>>>
Cc: Zhao, Yanan <yzhao@irell.com<<mailto:yzhao@irell.com>>>; Enzminger, David
<DEnzminger@winston.com<<mailto:DEnzminger@winston.com>>>; Kate Quisenberry
<quisenberry@fr.com<<mailto:quisenberry@fr.com>>>; #Netlist-Samsung293 <Netlist-Samsung293@irell.com<<mailto:Netlist-Samsung293@irell.com>>>;
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<FISHSERVICESamsung/Netlist22cv00293@fr.com<<mailto:FISHSERVICESamsung/Netlist22cv00293@fr.com>>>;
tom@gillamsmithlaw.com<<mailto:tom@gillamsmithlaw.com>>;
melissa@gillamsmithlaw.com<<mailto:melissa@gillamsmithlaw.com>>; Nester, Brian
<BNester@cov.com<<mailto:BNester@cov.com>>>; Ahn, Alice <aahn@cov.com<<mailto:aahn@cov.com>>>;
jromanow@cov.com<<mailto:jromanow@cov.com>>;
gschmidt@hilgersgraben.com<<mailto:gschmidt@hilgersgraben.com>>;
jhyland@hilgersgraben.com<<mailto:jhyland@hilgersgraben.com>>; Winston-Micron-Netlist <Winston-Micron-Netlist@winston.com<<mailto:Winston-Micron-Netlist@winston.com>>>; ce@wsfirm.com<<mailto:ce@wsfirm.com>>;
andrea@wsfirm.com<<mailto:andrea@wsfirm.com>>; wh@wsfirm.com<<mailto:wh@wsfirm.com>>; ~Doan, Jennifer
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mhornok@haltomdoan.com<<mailto:mhornok@haltomdoan.com>>;
mthornberry@haltomdoan.com<<mailto:mthornberry@haltomdoan.com>>
Subject: Re: Samsung/Netlist EDTX -293 - Expert Deposition Dates

Hi Mike - I believe Samsung wants to take the deposition before the msj/mts briefing deadline.

Mr. Gillingham is also available on January 11. Would that work for both Micron and Samsung?

On Jan 4, 2024, at 4:55 PM, Rueckheim, Mike <MRueckheim@winston.com<<mailto:MRueckheim@winston.com>>> wrote:

Sorry, we can't do Gillingham depo on Jan 8, please identify a day in February.

-Mike

From: Zhao, Yanan <yzhao@irell.com<<mailto:yzhao@irell.com>>>

Sent: Thursday, January 4, 2024 4:46:23 PM

To: Carson, Rebecca <RCarson@irell.com<<mailto:RCarson@irell.com>>>; Enzminger, David

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Subject: RE: Samsung/Netlist EDTX -293 - Expert Deposition Dates

Mike, David, please confirm whether Micron intends to take Mr. Gillingham's deposition on the same date on January 8 as soon as possible.

Best,

Yanan

Yanan Zhao

Associate

Irell & Manella llp

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From: Carson, Rebecca <RCarson@irell.com<<mailto:RCarson@irell.com>>>
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Subject: RE: Samsung/Netlist EDTX -293 - Expert Deposition Dates

David – We are fine providing a separate date for Dr. Groehn’s Micron deposition – we were simply trying to reduce scheduling conflicts/burdens by doing the depositions on the same day. I will check on alternate dates, but I don’t think January 10-11 will work. Please let me know if there are other date ranges you would like me to check for Dr. Groehn’s deposition. In addition, could you please promptly respond to the two other questions I have now asked multiple times:

(1) Does January 8 work for Micron for Dr. Gillingham’s deposition?

(2) Given that Micron is asking for dates in February for Netlist’s other experts, please confirm that Micron is also willing to postpone the depositions of Micron’s experts to February.

Regards,

Rebecca

From: Enzminger, David

<DEnzminger@winston.com<<mailto:DEnzminger@winston.com><<mailto:DEnzminger@winston.com>%3cmailto:DEnzminger@winston.com>>>

Sent: Wednesday, January 3, 2024 10:56 AM

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Subject: RE: Samsung/Netlist EDTX -293 - Expert Deposition Dates

With respect to Dr. Groehn, it isn't clear to me that Samsung and Micron are required to take his deposition on the same day. I that regard Micron is not available Jan 8-9. Please advise regarding Dr. Groehn's availability for Jan. 10-11.

From: Kate Quisenberry

<quisenberry@fr.com<<mailto:quisenberry@fr.com><<mailto:quisenberry@fr.com><<mailto:quisenberry@fr.com>>>>>>>

Sent: Tuesday, January 2, 2024 3:08 PM

To: Carson, Rebecca

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Subject: Re: Samsung/Netlist EDTX -293 - Expert Deposition Dates

Hi Rebecca, Confirmed that Samsung is available to take Dr. Groehn's deposition on January 8 and Dr. Mangione-Smith's deposition on January 12, assuming that date is for a Samsung-only deposition. With respect to the depositions of Samsung's experts, based on Netlist's failure to

Hi Rebecca,

Confirmed that Samsung is available to take Dr. Groehn's deposition on January 8 and Dr. Mangione-Smith's deposition on January 12, assuming that date is for a Samsung-only deposition.

With respect to the depositions of Samsung's experts, based on Netlist's failure to confirm Ms. Kindler's deposition on January 4, Samsung has allowed Ms. Kindler to release that date. Ms. Kindler is available for deposition on January 10. As Samsung previously indicated, Mr. Perryman is not available after January 5 because he has a trial beginning in another case on January 8. Mr. Perryman is traveling tomorrow morning for deposition preparation and for the deposition, so if Netlist does not intend to take Mr. Perryman's deposition on January 5, please confirm that by this evening. Mr. McAlexander and Dr. Halbert remain available on January 9. However, Mr. McAlexander is available on January 16 and Dr. Halbert on January 10, if Netlist would prefer.

As Samsung previously indicated, Samsung is willing to move for leave to allow certain depositions to occur a few days after the January 9 deadline (e.g., to accommodate depositions occurring on January 10 and January 12) but cannot agree to conduct half of the expert depositions a month after the close of expert discovery without also adjusting the other deadlines. There is considerable prejudice to Samsung in agreeing to conduct these depositions out of time. First, Netlist will have the benefit of Samsung's dispositive motion briefing before the depositions of Samsung's experts, which would provide Netlist with a strategic advantage. Second, Samsung will not have the benefit of its experts' depositions being completed in evaluating what motions to file and in responding to Netlist's motions. Third, Netlist's proposal requires Samsung's experts to prepare for their depositions over a month after their expert reports were submitted, which will require them to expend additional resources to refresh their recollections on issues that are currently fresh in their minds. It will be inefficient and costly to Samsung for its counsel and its experts to revisit the reports a month from now in preparation for depositions. Finally, Samsung is entitled to rely on the case schedule for purposes of planning its time and organizing its trial preparation. Samsung should not be forced to expend time and resources preparing its experts for deposition while also continuing dispositive motion briefing and beginning pretrial exchanges.

Netlist complains that its team is too busy to take the few expert depositions during the Court-ordered period that has been in place for since early November. First, given the significant number of attorneys representing Netlist at Irell &

Manella and McKool Smith, surely there are attorneys available to take four depositions of Samsung's experts within the expert discovery period. In fact, there are several attorneys on the proposed team--yourself included--who have appeared in our Netlist case and who have not appeared in the GComm case. Second, your email never explained why Netlist could not have raised these potential conflicts for weeks after Samsung timely offered these dates. Regardless, Micron agreed to push expert depositions to February, including those of Netlist's experts, meaning Netlist's counsel has more time available. Third, Fish & Richardson has accepted the Netlist deposition dates during the Court-order period even though Fish & Richardson also represents Samsung in that GComm trial. Fourth, Netlist has continued to push for the January date for the GComm trial without ever informing the Court of the supposed conflict with the Netlist schedule. Fifth, Judge Folsom offered a number of dates for the discovery hearing (including January 5, 12, 17, 18, and 25), and Netlist requested January 5 despite the fact that Samsung offered the deposition of Mr. Perryman on January 5 over a week earlier (on December 12).

Best,

Kate

Kathryn A. Quisenberry :: Fish & Richardson P.C. :: 713 654 5355

From: "Carson, Rebecca"

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Date: Tuesday, January 2, 2024 at 12:09 PM

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<mthornberry@haltomdoan.com<mailto:mthornberry@haltomdoan.com<mailto:mthornberry@haltomdoan.com%3cmailto:mthornberry@haltomdoan.com>>>
Subject: RE: Samsung/Netlist EDTX -293 - Expert Deposition Dates

Counsel,

As an update to the below, January 5 no longer works for Dr. Groehn's deposition, so we will need to move it to January 8.

Kate – Please confirm whether the new date for Dr. Groehn (January 8) works for Samsung, as well as whether the date we previously offered for Dr. Mangione-Smith (January 12) works. In addition, please provide a response to my email below by close of business today.

Mike – please confirm that Micron is willing to postpone the expert depositions for its experts until February (we assume so given that you are asking for February dates for Netlist's experts, but need confirmation), and also let us know whether Micron can go forward with the depositions of Dr. Groehn and/or Mr. Gillingham on January 8.

Regards,

Rebecca

From: Carson, Rebecca

Sent: Friday, December 29, 2023 3:57 PM

To: 'Rueckheim, Mike'

<MRueckheim@winston.com<mailto:MRueckheim@winston.com<mailto:MRueckheim@winston.com%3cmailto:MRueckheim@winston.com>>>; 'Kate Quisenberry'

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wh@wsfirm.com<mailto:wh@wsfirm.com<mailto:wh@wsfirm.com%3cmailto:wh@wsfirm.com>>>; ~Doan, Jennifer

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Subject: RE: Samsung/Netlist EDTX -293 - Expert Deposition Dates

Hi Mike,

Based on your email, can I assume that Micron is willing to postpone the expert depositions for its experts until February? If so, we will look into dates for Mr. Kennedy and Dr. Mangione-Smith in February for the Micron case.

Do the dates we offered for Dr. Groehn (January 5) and Mr. Gillingham (January 8) work for Micron?

Regards,

Rebecca

From: Rueckheim, Mike

<MRueckheim@winston.com<mailto:MRueckheim@winston.com<mailto:MRueckheim@winston.com%3cmailto:MRueckheim@winston.com>>>>

Sent: Friday, December 29, 2023 3:53 PM

To: Carson, Rebecca

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Subject: Re: Samsung/Netlist EDTX -293 - Expert Deposition Dates

Please also identify dates for Netlist expert depositions in February.

-Mike

From: Carson, Rebecca

<RCarson@irell.com<mailto:RCarson@irell.com<mailto:RCarson@irell.com%3cmailto:RCarson@irell.com>>>

Sent: Friday, December 29, 2023 3:40:54 PM

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<mthornberry@haltomdoan.com<mailto:mthornberry@haltomdoan.com<mailto:mthornberry@haltomdoan.com%3cmailto:mthornberry@haltomdoan.com>>>;
Subject: RE: Samsung/Netlist EDTX -293 - Expert Deposition Dates

Kate,

At the time we agreed to the current schedule in early November, we thought that doing the expert depositions in early January would be feasible. But there have been a number of developments since then that prevent us from being able to take the depositions during the current window. Indeed, since the amended DCO was entered on November 9: (1) Judge Gilstrap continued a trial originally scheduled for November involving a different Irell client and your client (Samsung) to January based on Samsung's multiple requests for a continuance (see attached order), (2) the PTAB scheduled oral argument on the '160 and '060 patents for January 11, (3) the Court set another PTC in the Netlist/Micron case for January 12, and (4) the Court set the discovery hearing in these matters for January 5.

In light of the above, we trust that Samsung will grant us the professional courtesy of postponing the depositions of its experts until early February. We do not think any other adjustments to the case schedule need to be made, as we are fine proceeding with the MSJ/Dauberts on the current schedule. Given that we are offering Netlist's experts for deposition before the MSJ/Daubert deadline, there would be no prejudice to Samsung. If you continue to oppose, please explain the basis for your opposition and identify any alleged prejudice or impact this would have on Samsung.

With respect to Dr. Groehn, we are fine with doing the depositions in a consecutive fashion if that is agreeable to Micron, on the condition that neither party will be able to use the other deposition. With respect to Mr. Gillingham, we will await confirmation from Micron as to whether that date works. Assuming it does, we are fine with limiting our deposition of Mr. Halbert to one day.

Due to personal reasons, Dr. Mangione-Smith is not available before January 9. He is available January 12. Please let us know if that date works for Samsung.

Regards,

Rebecca

From: Kate Quisenberry

<quisenberry@fr.com<mailto:quisenberry@fr.com<mailto:quisenberry@fr.com%3cmmailto:quisenberry@fr.com>>>

Sent: Friday, December 29, 2023 1:41 PM

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Subject: Re: Samsung/Netlist EDTX -293 - Expert Deposition Dates

Rebecca,

Thanks for your response. The parties have discussed proposed modifications to the case schedule a number of times, and as Samsung has repeatedly stated, there is no room in the current schedule to make significant adjustments without also moving the pretrial conference and trial. To that end, if Netlist wishes to propose a modified schedule, including the trial date, please let us know. Otherwise, our experts are ready and available to go forward with their depositions during the expert discovery window that has long been in place on the dates that we offered over two and a half weeks ago. If Netlist wishes to move for leave to modify the expert discovery period to extend it into February without moving the pretrial conference and trial (and the other intervening dates) by a similar amount, Samsung opposes such a request.

Samsung would be willing to attempt to accommodate slight changes in the schedule for one or two of its expert witnesses by a few days if needed. Within the framework of the current schedule, note that Mr. Perryman is not available after January 5, and with his and Ms. Kindler's deposition dates fast approaching (next week), travel arrangements and planning are already well underway. Please let us know by tomorrow if you are going forward with at least those two depositions.

With respect to Netlist's experts, Samsung accepts Dr. Groehn's deposition on January 5; however, we understand that Dr. Groehn submitted separate reports for Samsung and Micron based on each party's confidential financial information. Samsung can agree to consecutive depositions of Dr. Groehn on January 5 if the transcripts are separate and that arrangement is acceptable to Micron. In any event, Samsung will take Dr. Groehn's deposition on January 5. Samsung can accept a joint deposition of Mr. Gillingham on January 8 if that arrangement is acceptable to Micron, and if Netlist agrees to a single deposition of Mr. Halbert. Although Mr. Kennedy should have reserved time for his deposition before the January 9 expert discovery deadline, in the spirit of cooperation, Samsung accepts a Samsung-only deposition of Mr. Kennedy on January 12. Of course, a different day would be needed for any deposition related to Micron—assuming Netlist is relying on Mr. Kennedy in the Micron case. Finally, please provide a date for a Samsung-only deposition of Dr. Mangione-Smith as soon as possible that is within the current expert discovery period (i.e., this deposition must occur no later than January 9).

Best,

Kate

Kathryn A. Quisenberry :: Fish & Richardson P.C. :: 713 654 5355

From: "Carson, Rebecca"

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Date: Thursday, December 28, 2023 at 5:17 PM

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Subject: RE: Samsung/Netlist EDTX -293 - Expert Deposition Dates

[This email originated outside of F&R.]

Counsel,

With respect to the deposition dates for Samsung's and Micron's experts, we are not available to take the depositions in early January due to various scheduling conflicts, including the fact that that our team has multiple trials scheduled in January. Could you please provide alternate dates in early February?

With respect to Netlist's experts, we can offer Dr. Groehn for a joint Micron/Samsung deposition on January 5 and Dr. Gillingham for a joint Micron/Samsung deposition on January 8. Mr. Kennedy is travelling and is not available until January 12. Please let us know if that date works. We are still looking into Dr. Mangione-Smith's availability and will get back to you shortly.

Regards,

Rebecca

From: Kate Quisenberry

<quisenberry@fr.com<mailto:quisenberry@fr.com<mailto:quisenberry@fr.com%3cmmailto:quisenberry@fr.com>>>

Sent: Tuesday, December 26, 2023 1:34 PM

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Subject: Re: Samsung/Netlist EDTX -293 - Expert Deposition Dates

Counsel:

Following up on the below, please confirm the dates Samsung has provided for the depositions of its experts today. As you know, some of them are as soon as next week.

Please also provide dates for Netlist's experts today. There are only nine business days left in expert discovery and Netlist has not yet provided deposition dates for any of its experts.

Best,

Kate

Kathryn A. Quisenberry :: Fish & Richardson P.C. :: 713 654 5355

On Dec 20, 2023, at 3:16 PM, Kate Quisenberry
<quisenberry@fr.com<mailto:quisenberry@fr.com<mailto:quisenberry@fr.com>>>>
wrote:

Counsel:

Following up on the below, please confirm the dates Samsung has provided for the depositions of its experts and

provide deposition dates for Netlist's experts this week so that the parties can plan for their depositions ahead of the holidays.

Best,

Kate

Kathryn A. Quisenberry :: Fish & Richardson P.C. :: 713 654 5355

From: Kate Quisenberry

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Date: Sunday, December 17, 2023 at 7:17 PM

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Subject: Re: Samsung/Netlist EDTX -293 - Expert Deposition Dates

Counsel:

Further to my email below, Joseph McAlexander and John Halbert are available for deposition on January 9. Please confirm the dates Samsung has provided and provide deposition dates for Netlist's experts this week so that the parties can plan for their depositions ahead of the holidays.

Best,

Kate

Kathryn A. Quisenberry :: Fish & Richardson P.C. :: 713 654 5355

From: Kate Quisenberry

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Date: Tuesday, December 12, 2023 at 9:50 PM

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 Subject: Samsung/Netlist EDTX -293 - Expert Deposition Dates

Counsel:

Samsung's experts Lauren Kindler and Ray Perryman are available for deposition on January 4 and 5, respectively. We will follow up with dates for Joseph McAlexander and John Halbert shortly. Please confirm the dates for Ms. Kindler and Mr. Perryman and provide dates for Netlist's expert witnesses as soon as possible.

Best,

Kate

Kathryn A. Quisenberry :: Associate :: Fish & Richardson P.C.

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Exhibit F

From: Daniel Tishman <tishman@fr.com>
Sent: Tuesday, February 27, 2024 9:10 PM
To: Tezyan, Michael; FISH SERVICE Samsung/Netlist 22cv00293; EXT Smith, Melissa (T-Mobile); bnester@cov.com; jromanow@cov.com; aahn@cov.com; bfregil@omm.com; ametlitsky@omm.com; alucas@omm.com
Cc: #Netlist-Samsung293; jtruelove@mckoolsmith.com; Sam Baxter
Subject: RE: Netlist v. Samsung-293 | Deposition Scheduling

Thanks Michael – will confirm soon re Dr. Lee’s deposition date.

Mr. Ji is available on April 1.

Mr. McAlexander is available on March 14.

Please confirm if Netlist will move forward with these dates.

Best regards,
Dan

Daniel Tishman :: Fish & Richardson P.C. :: +1 (202) 626-7725

From: Tezyan, Michael <mtezyan@irell.com>
Sent: Tuesday, February 27, 2024 7:36 PM
To: Daniel Tishman <tishman@fr.com>; FISH SERVICE Samsung/Netlist 22cv00293 <FISHSERVICESamsung/Netlist22cv00293@fr.com>; melissa@gillamsmithlaw.com; bnester@cov.com; jromanow@cov.com; aahn@cov.com; bfregil@omm.com; ametlitsky@omm.com; alucas@omm.com
Cc: #Netlist-Samsung293 <Netlist-Samsung293@irell.com>; jtruelove@mckoolsmith.com; Sam Baxter <sbaxter@mckoolsmith.com>
Subject: RE: Netlist v. Samsung-293 | Deposition Scheduling

Dan,

Given Dr. Lee’s health issues, we propose conducting his deposition over two days. Dr. Lee is available for virtual deposition on 3/19 and 3/21, and will need a translator. Please let us know if those dates work for Samsung.

Also, please let us know when Mr. Ji and Mr. McAlexander are available for deposition.

Best,
Michael

Michael Tezyan

Associate

IRELL & MANELLA LLP

1800 Avenue of the Stars, Suite 900

Los Angeles, CA 90067

Direct: (310) 203-7536 | Email: mtezyan@irell.com

From: Daniel Tishman <tishman@fr.com>
Sent: Sunday, February 25, 2024 3:19 PM
To: Tezyan, Michael <mtezyan@irell.com>; FISH SERVICE Samsung/Netlist 22cv00293 <FISHSERVICESamsung/Netlist22cv00293@fr.com>; ~Smith, Melissa <melissa@gillamsmithlaw.com>; bnester@cov.com; jromanow@cov.com; aahn@cov.com; bfregil@omm.com; ametlitsky@omm.com; alucas@omm.com
Cc: #Netlist-Samsung293 <Netlist-Samsung293@irell.com>; jtruelove@mckoolsmith.com; ~Baxter, Samuel <sbaxter@mckoolsmith.com>
Subject: RE: Netlist v. Samsung-293 | Deposition Scheduling

Thanks Michael – we will investigate availability and follow up as soon as possible.

Best regards,
Dan

Daniel Tishman :: Fish & Richardson P.C. :: +1 (202) 626-7725

From: Tezyan, Michael <mtezyan@irell.com>
Sent: Sunday, February 25, 2024 6:09 PM
To: Daniel Tishman <tishman@fr.com>; FISH SERVICE Samsung/Netlist 22cv00293 <FISHSERVICESamsung/Netlist22cv00293@fr.com>; melissa@gillamsmithlaw.com; bnester@cov.com; jromanow@cov.com; aahn@cov.com; bfregil@omm.com; ametlitsky@omm.com; alucas@omm.com
Cc: #Netlist-Samsung293 <Netlist-Samsung293@irell.com>; jtruelove@mckoolsmith.com; Sam Baxter <sbaxter@mckoolsmith.com>
Subject: RE: Netlist v. Samsung-293 | Deposition Scheduling

Thanks Dan, we are investigating Dr. Lee's availability and will let you know.

Separately, to follow up on deposition scheduling for Mr. Ji and Mr. McAlexander, Netlist is not available on the dates offered by Samsung (Mar. 5 and Mar. 8 respectively). Can you please let us know the availability of these witnesses the week of Mar. 11?

Thanks,
Michael

Michael Tezyan

Associate

IRELL & MANELLA LLP

1800 Avenue of the Stars, Suite 900

Los Angeles, CA 90067

Direct: (310) 203-7536 | Email: mtezyan@irell.com

From: Daniel Tishman <tishman@fr.com>
Sent: Sunday, February 25, 2024 2:50 PM
To: Tezyan, Michael <mtezyan@irell.com>; FISH SERVICE Samsung/Netlist 22cv00293 <FISHSERVICESamsung/Netlist22cv00293@fr.com>; ~Smith, Melissa <melissa@gillamsmithlaw.com>; bnester@cov.com; jromanow@cov.com; aahn@cov.com; bfregil@omm.com; ametlitsky@omm.com; alucas@omm.com
Cc: #Netlist-Samsung293 <Netlist-Samsung293@irell.com>; jtruelove@mckoolsmith.com; ~Baxter, Samuel <sbaxter@mckoolsmith.com>
Subject: RE: Netlist v. Samsung-293 | Dkt. 659

Michael –

We don't oppose. Please let us know when Dr. Lee will be available for a deposition.

Best regards,
Dan

Daniel Tishman :: Fish & Richardson P.C. :: +1 (202) 626-7725

From: Tezyan, Michael <mtezyan@irell.com>

Sent: Sunday, February 25, 2024 4:19 PM

To: FISH SERVICE Samsung/Netlist 22cv00293 <FISHSERVICESamsung/Netlist22cv00293@fr.com>; melissa@gillamsmithlaw.com; bnester@cov.com; jromanow@cov.com; aahn@cov.com; bfregil@omm.com; ametlitsky@omm.com; alucas@omm.com; Daniel Tishman <tishman@fr.com>

Cc: #Netlist-Samsung293 <Netlist-Samsung293@irell.com>; jtruelove@mckoolsmith.com; Sam Baxter <sbaxter@mckoolsmith.com>

Subject: RE: Netlist v. Samsung-293 | Dkt. 659

[This email originated outside of F&R.]

Counsel,

Netlist intends to file a motion today to withdraw its objections to the Special Master's R&R as to the following motions: Dkt. 202 (Motion to compel Dr. Lee's deposition) and Dkt. 380 (Motion to correct/amend the Jan. 5 transcript).

Please confirm that Samsung does not oppose.

Thanks,
Michael

Michael Tezyan

Associate

IRELL & MANELLA LLP

1800 Avenue of the Stars, Suite 900

Los Angeles, CA 90067

Direct: (310) 203-7536 | Email: mtezyan@irell.com

From: Tezyan, Michael

Sent: Friday, February 23, 2024 2:36 PM

To: FISH SERVICE Samsung/Netlist 22cv00293 <FISHSERVICESamsung/Netlist22cv00293@fr.com>; ~Smith, Melissa <melissa@gillamsmithlaw.com>; bnester@cov.com; jromanow@cov.com; aahn@cov.com; bfregil@omm.com; ametlitsky@omm.com; alucas@omm.com; Daniel Tishman <tishman@fr.com>

Cc: #Netlist-Samsung293 <Netlist-Samsung293@irell.com>; Jennifer Truelove <jtruelove@McKoolSmith.com>; ~Baxter, Samuel <sbaxter@mckoolsmith.com>

Subject: Netlist v. Samsung-293 | Dkt. 659

Counsel,

Please see attached for service of Dkt. 659.

Best,
Michael

Michael Tezyan

Associate

IRELL & MANELLA LLP

1800 Avenue of the Stars, Suite 900

Los Angeles, CA 90067

Direct: (310) 203-7536 | Email: mtezyan@irell.com

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Exhibit G

From: Daniel Tishman <tishman@fr.com>
Sent: Tuesday, March 12, 2024 12:37 PM
To: Tezyan, Michael; jsheasby@irell.com; FISH SERVICE Samsung/Netlist 22cv00293; EXT Smith, Melissa (T-Mobile); bnester@cov.com; jromanow@cov.com; aahn@cov.com; bfregil@omm.com; ametlitsky@omm.com; alucas@omm.com
Cc: #Netlist-Samsung293; jtruelove@mckoolsmith.com; Sam Baxter
Subject: RE: Netlist v. Samsung-293 | Deposition Scheduling - McAlexander and Ji

Michael,

Your accusations regarding Mr. Ji's deposition are confounding—Samsung provided Mr. Ji's availability on February 19, and when Netlist rejected the offered date of March 5, we followed up on February 27, offering Mr. Ji for deposition on April 1 as an alternative. If Netlist wishes to go forward with the April 1 deposition, we can inquire if Mr. Ji is still available then. Please advise.

As for Mr. McAlexander, there is no legitimate basis for Netlist to delay his deposition pending Mr. Ji's deposition. Mr. Ji's testimony on the facts and circumstances relating to the negotiation of the JDLA have no bearing on the issues for which Mr. McAlexander is offering technical expert opinions. Given your unwillingness to take his deposition on March 14, when counsel for Netlist is available, we have released Mr. McAlexander for that date. We are investigating availability in early April and will follow up in due course.

Best regards,
Dan

Daniel Tishman :: Fish & Richardson P.C. :: +1 (202) 626-7725

From: Tezyan, Michael <mtezyan@irell.com>
Sent: Monday, March 11, 2024 2:07 PM
To: Daniel Tishman <tishman@fr.com>; jsheasby@irell.com; FISH SERVICE Samsung/Netlist 22cv00293 <FISHSERVICESamsung/Netlist22cv00293@fr.com>; melissa@gillamsmithlaw.com; bnester@cov.com; jromanow@cov.com; aahn@cov.com; bfregil@omm.com; ametlitsky@omm.com; alucas@omm.com
Cc: #Netlist-Samsung293 <Netlist-Samsung293@irell.com>; jtruelove@mckoolsmith.com; Sam Baxter <sbaxter@mckoolsmith.com>
Subject: RE: Netlist v. Samsung-293 | Deposition Scheduling - McAlexander and Ji

Dan,

It is unclear why you started a new email thread for this scheduling correspondence, other than to obfuscate the fact that our February 25 email asked for both Mr. McAlexander's and Mr. Ji's availability for the week of March 11. Regardless, please provide Mr. Ji's availability for this week or next week without further delay. If needed, we will contact the Court to get assistance scheduling Mr. Ji's deposition. We have been requesting Mr. Ji's availability for deposition for over a month, and Samsung's continued delay of his deposition without explanation prejudices Netlist. Samsung's previously offered date (March 5) obviously was not a workable date given that it was the day before the pre-trial conference.

As for Mr. McAlexander's deposition, it does not make sense to proceed with Mr. McAlexander's expert deposition while the deposition of one of Samsung's 30(b)(6) witnesses is outstanding. Please provide Mr. McAlexander's availability for early April.

Thanks,
Michael

Michael Tezian

Associate

IRELL & MANELLA LLP

1800 Avenue of the Stars, Suite 900

Los Angeles, CA 90067

Direct: (310) 203-7536 | Email: mtezian@irell.com

From: Daniel Tishman <tishman@fr.com>

Sent: Monday, March 11, 2024 9:04 AM

To: Sheasby, Jason <JSheasby@irell.com>; Tezian, Michael <mtezian@irell.com>; FISH SERVICE Samsung/Netlist 22cv00293 <FISHSERVICESamsung/Netlist22cv00293@fr.com>; ~Smith, Melissa <melissa@gillamsmithlaw.com>; bnester@cov.com; jromanow@cov.com; aahn@cov.com; bfregil@omm.com; ametlitsky@omm.com; alucas@omm.com

Cc: #Netlist-Samsung293 <Netlist-Samsung293@irell.com>; jtruelove@mckoolsmith.com; ~Baxter, Samuel <sbaxter@mckoolsmith.com>

Subject: RE: Netlist v. Samsung-293 | Deposition Scheduling - McAlexander

Jason:

Mr. McAlexander is being offered on March 14. Netlist requested a date for him during the week of March 11, and we have made arrangements accordingly. From your email, we understand that Netlist's counsel is available. If Netlist wishes to forfeit Mr. McAlexander's deposition, please let us know by the end of the day so that we can release him.

Mr. Ji is not being offered for deposition on March 14.

Best regards,
Dan

Daniel Tishman :: Fish & Richardson P.C. :: +1 (202) 626-7725

From: Sheasby, Jason <JSheasby@irell.com>

Sent: Friday, March 08, 2024 2:42 PM

To: Daniel Tishman <tishman@fr.com>; Tezian, Michael <mtezian@irell.com>; FISH SERVICE Samsung/Netlist 22cv00293 <FISHSERVICESamsung/Netlist22cv00293@fr.com>; melissa@gillamsmithlaw.com; bnester@cov.com; jromanow@cov.com; aahn@cov.com; bfregil@omm.com; ametlitsky@omm.com; alucas@omm.com

Cc: #Netlist-Samsung293 <Netlist-Samsung293@irell.com>; jtruelove@mckoolsmith.com; Sam Baxter <sbaxter@mckoolsmith.com>

Subject: Re: Netlist v. Samsung-293 | Deposition Scheduling - McAlexander

[This email originated outside of F&R.]

We want Hyun Ki Ji on this date.

From: Daniel Tishman <tishman@fr.com>

Date: Friday, March 8, 2024 at 11:39 AM

To: "Tezyan, Michael" <mtezyan@irell.com>, FISH SERVICE Samsung/Netlist 22cv00293

<FISHSERVICESamsung/Netlist22cv00293@fr.com>, Melissa ~Smith <melissa@gillamsmithlaw.com>, "bnester@cov.com" <bnester@cov.com>, "jromanow@cov.com" <jromanow@cov.com>, "aahn@cov.com" <aahn@cov.com>, "bfregil@omm.com" <bfregil@omm.com>, "ametilitsky@omm.com" <ametilitsky@omm.com>, "alucas@omm.com" <alucas@omm.com>

Cc: #Netlist-Samsung293 <Netlist-Samsung293@irell.com>, "jtruelove@mckoolsmith.com"

<jtruelove@mckoolsmith.com>, "~Baxter, Samuel" <sbaxter@mckoolsmith.com>

Subject: Netlist v. Samsung-293 | Deposition Scheduling - McAlexander

Counsel –

Will Netlist be going forward with Mr. McAlexander's deposition on March 14, as previously offered?

Best regards,

Dan

Daniel Tishman :: Fish & Richardson P.C. :: +1 (202) 626-7725

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Exhibit H

From: Daniel Tishman <tishman@fr.com>
Sent: Monday, April 8, 2024 10:26 PM
To: Tezyan, Michael; FISH SERVICE Samsung/Netlist 22cv00293; EXT Smith, Melissa (T-Mobile); bnester@cov.com; jromanow@cov.com; aahn@cov.com; bfregil@omm.com; ametlitsky@omm.com; alucas@omm.com
Cc: #Netlist-Samsung293; jtruelove@mckoolsmith.com; Sam Baxter
Subject: RE: Netlist v. Samsung-293: McAlexander Depo on April 3

Michael,

We are working to identify alternate dates, and will follow up in due course.

Best regards,
Dan

Daniel Tishman

Principal ■ Fish & Richardson P.C.

T: +1 (202) 626-7725 | tishman@fr.com

From: Tezyan, Michael <mtezyan@irell.com>
Sent: Friday, April 05, 2024 8:49 PM
To: Daniel Tishman <tishman@fr.com>; FISH SERVICE Samsung/Netlist 22cv00293 <FISHSERVICESamsung/Netlist22cv00293@fr.com>; melissa@gillamsmithlaw.com; bnester@cov.com; jromanow@cov.com; aahn@cov.com; bfregil@omm.com; ametlitsky@omm.com; alucas@omm.com
Cc: #Netlist-Samsung293 <Netlist-Samsung293@irell.com>; jtruelove@mckoolsmith.com; Sam Baxter <sbaxter@mckoolsmith.com>
Subject: RE: Netlist v. Samsung-293: McAlexander Depo on April 3

Dan,

Netlist is unavailable April 9. For scheduling purposes, please let us know the dates of Mr. McAlexander's conflicts that you reference below.

Best,
Michael

Michael Tezyan

Associate

IRELL & MANELLA LLP

1800 Avenue of the Stars, Suite 900

Los Angeles, CA 90067

Direct: (310) 203-7536 | Email: mtezyan@irell.com

From: Daniel Tishman <tishman@fr.com>
Sent: Thursday, April 4, 2024 6:48 AM
To: Tezyan, Michael <mtezyan@irell.com>; FISH SERVICE Samsung/Netlist 22cv00293

<FISHSERVICESamsung/Netlist22cv00293@fr.com>; ~Smith, Melissa <melissa@gillamsmithlaw.com>;
bnester@cov.com; jromanow@cov.com; aahn@cov.com; bfregil@omm.com; ametlitsky@omm.com; alucas@omm.com
Cc: #Netlist-Samsung293 <Netlist-Samsung293@irell.com>; jtruelove@mckoolsmith.com; ~Baxter, Samuel
<sbaxter@mckoolsmith.com>
Subject: RE: Netlist v. Samsung-293: McAlexander Depo on April 3

Michael –

Mr. McAlexander is available on April 9. Please let us know by noon tomorrow if Netlist accepts the date. After that, Mr. McAlexander has a significant amount of conflicts due to travel and trials that will make scheduling very difficult.

Best regards,
Dan

Daniel Tishman

Principal ■ Fish & Richardson P.C.

T: +1 (202) 626-7725 | tishman@fr.com

From: Tezyan, Michael <mtezyan@irell.com>
Sent: Friday, March 29, 2024 4:29 PM
To: Daniel Tishman <tishman@fr.com>; FISH SERVICE Samsung/Netlist 22cv00293
<FISHSERVICESamsung/Netlist22cv00293@fr.com>; melissa@gillamsmithlaw.com; bnester@cov.com;
jromanow@cov.com; aahn@cov.com; bfregil@omm.com; ametlitsky@omm.com; alucas@omm.com
Cc: #Netlist-Samsung293 <Netlist-Samsung293@irell.com>; jtruelove@mckoolsmith.com; Sam Baxter
<sbaxter@mckoolsmith.com>
Subject: RE: Netlist v. Samsung-293: McAlexander Depo on April 3

[This email originated outside of F&R.]

Counsel,

Netlist is not available on April 3. Can you please provide Mr. McAlexander's availability for the second week of April?

Thank you,
Michael

Michael Tezyan

Associate

IRELL & MANELLA LLP

1800 Avenue of the Stars, Suite 900

Los Angeles, CA 90067

Direct: (310) 203-7536 | Email: mtezyan@irell.com

From: Tezyan, Michael <mtezyan@irell.com>
Sent: Thursday, March 21, 2024 3:17 PM

To: Daniel Tishman <tishman@fr.com>; FISH SERVICE Samsung/Netlist 22cv00293 <FISHSERVICESamsung/Netlist22cv00293@fr.com>; ~Smith, Melissa <melissa@gillamsmithlaw.com>; bnester@cov.com; iromanow@cov.com; aahn@cov.com; bfregil@omm.com; ametlitsky@omm.com; alucas@omm.com
Cc: #Netlist-Samsung293 <Netlist-Samsung293@irell.com>; jtruelove@mckoolsmith.com; ~Baxter, Samuel <sbaxter@mckoolsmith.com>
Subject: RE: Netlist v. Samsung-293: McAlexander Depo on April 3

Counsel,

We are considering the dates you have offered for Mr. McAlexander (April 3) and Mr. Ji (April 1), but as Samsung is well aware, the C.D. Cal. trial may be continued to that week. We will follow up once we have more information.

Thanks,
Michael

Michael Tezyan

Associate

IRELL & MANELLA LLP

1800 Avenue of the Stars, Suite 900

Los Angeles, CA 90067

Direct: (310) 203-7536 | Email: mtezyan@irell.com

From: Daniel Tishman <tishman@fr.com>
Sent: Tuesday, March 19, 2024 2:51 PM
To: Tezyan, Michael <mtezyan@irell.com>; FISH SERVICE Samsung/Netlist 22cv00293 <FISHSERVICESamsung/Netlist22cv00293@fr.com>; ~Smith, Melissa <melissa@gillamsmithlaw.com>; bnester@cov.com; iromanow@cov.com; aahn@cov.com; bfregil@omm.com; ametlitsky@omm.com; alucas@omm.com
Cc: #Netlist-Samsung293 <Netlist-Samsung293@irell.com>; jtruelove@mckoolsmith.com; ~Baxter, Samuel <sbaxter@mckoolsmith.com>
Subject: Netlist v. Samsung-293: McAlexander Depo on April 3

Counsel:

Per your request, Mr. McAlexander is available for a deposition on April 3.

Please confirm that Netlist will go forward with his deposition.

Best regards,
Dan

Daniel Tishman :: Fish & Richardson P.C. :: +1 (202) 626-7725

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Exhibit I

From: Katherine Reardon <reardon@fr.com>
Sent: Monday, July 8, 2024 6:04 AM
To: Tezyan, Michael; Daniel Tishman; FISH SERVICE Samsung/Netlist 22cv00293; EXT Smith, Melissa (T-Mobile)
Cc: #Netlist-Samsung293; jtruelove@mckoolsmith.com
Subject: RE: Netlist v. Samsung-293: McAlexander Depo

Michael,

Mr. McAlexander is available for deposition on July 19.

Thanks,
Kate

Katherine H. Reardon :: Fish & Richardson P.C. :: 212 641 2235

From: Katherine Reardon <reardon@fr.com>
Sent: Monday, June 24, 2024 6:40 PM
To: Tezyan, Michael <mtezyan@irell.com>; Daniel Tishman <tishman@fr.com>; FISH SERVICE Samsung/Netlist 22cv00293 <FISHSERVICESamsung/Netlist22cv00293@fr.com>; melissa@gillamsmithlaw.com
Cc: #Netlist-Samsung293 <Netlist-Samsung293@irell.com>; jtruelove@mckoolsmith.com
Subject: RE: Netlist v. Samsung-293: McAlexander Depo

Michael,

We are still investigating alternative dates, including your July 19 proposal.

Thanks,
Kate

Katherine H. Reardon :: Fish & Richardson P.C. :: 212 641 2235

From: Tezyan, Michael <mtezyan@irell.com>
Sent: Monday, June 24, 2024 3:16 PM
To: Daniel Tishman <tishman@fr.com>; Katherine Reardon <reardon@fr.com>; FISH SERVICE Samsung/Netlist 22cv00293 <FISHSERVICESamsung/Netlist22cv00293@fr.com>; melissa@gillamsmithlaw.com
Cc: #Netlist-Samsung293 <Netlist-Samsung293@irell.com>; jtruelove@mckoolsmith.com
Subject: RE: Netlist v. Samsung-293: McAlexander Depo

Dan, following up, does July 19 work for McAlexander?

Thanks,
Michael

Michael Tezyan

Associate

IRELL & MANELLA LLP

1800 Avenue of the Stars, Suite 900

Los Angeles, CA 90067
Direct: (310) 203-7536 | Email: mtezyan@irell.com

From: Tezyan, Michael <mtezyan@irell.com>
Sent: Wednesday, June 19, 2024 9:11 AM
To: Daniel Tishman <tishman@fr.com>; Katherine Reardon <reardon@fr.com>; FISH SERVICE Samsung/Netlist 22cv00293 <FISHSERVICESamsung/Netlist22cv00293@fr.com>; ~Smith, Melissa <melissa@gillamsmithlaw.com>
Cc: #Netlist-Samsung293 <Netlist-Samsung293@irell.com>; jtruelove@mckoolsmith.com
Subject: RE: Netlist v. Samsung-293: McAlexander Depo

Dan,

Netlist is not available July 10. Does July 19 work? Please let us know.

Thanks,
Michael

Michael Tezyan

Associate

IRELL & MANELLA LLP

1800 Avenue of the Stars, Suite 900

Los Angeles, CA 90067

Direct: (310) 203-7536 | Email: mtezyan@irell.com

From: Daniel Tishman <tishman@fr.com>
Sent: Tuesday, June 18, 2024 7:45 PM
To: Tezyan, Michael <mtezyan@irell.com>; Katherine Reardon <reardon@fr.com>; FISH SERVICE Samsung/Netlist 22cv00293 <FISHSERVICESamsung/Netlist22cv00293@fr.com>; ~Smith, Melissa <melissa@gillamsmithlaw.com>
Cc: #Netlist-Samsung293 <Netlist-Samsung293@irell.com>; jtruelove@mckoolsmith.com
Subject: RE: Netlist v. Samsung-293: McAlexander Depo

Michael – Mr. McAlexander is available on July 10.

Best regards,
Dan

Daniel Tishman

Principal ■ Fish & Richardson P.C.

T: +1 (202) 626-7725 | tishman@fr.com

From: Daniel Tishman <tishman@fr.com>
Sent: Monday, June 17, 2024 11:33 AM
To: Tezyan, Michael <mtezyan@irell.com>; Katherine Reardon <reardon@fr.com>; FISH SERVICE Samsung/Netlist 22cv00293 <FISHSERVICESamsung/Netlist22cv00293@fr.com>; melissa@gillamsmithlaw.com
Cc: #Netlist-Samsung293 <Netlist-Samsung293@irell.com>; jtruelove@mckoolsmith.com
Subject: RE: Netlist v. Samsung-293: McAlexander Depo

Thanks Michael – we are working on gathering his availability and will follow up soon.

Best regards,
Dan

Daniel Tishman

Principal ■ Fish & Richardson P.C.

T: +1 (202) 626-7725 | tishman@fr.com

From: Tezyan, Michael <mtezyan@irell.com>

Sent: Monday, June 17, 2024 11:29 AM

To: Daniel Tishman <tishman@fr.com>; Katherine Reardon <reardon@fr.com>; FISH SERVICE Samsung/Netlist 22cv00293 <FISHSERVICESamsung/Netlist22cv00293@fr.com>; melissa@gillamsmithlaw.com

Cc: #Netlist-Samsung293 <Netlist-Samsung293@irell.com>; jtruelove@mckoolsmith.com

Subject: RE: Netlist v. Samsung-293: McAlexander Depo

[This email originated outside of F&R.]

Dan and Kate,

Following up on my email below – could you please let us know when Mr. McAlexander is available for deposition over Zoom?

Thanks,
Michael

Michael Tezyan

Associate

IRELL & MANELLA LLP

1800 Avenue of the Stars, Suite 900

Los Angeles, CA 90067

Direct: (310) 203-7536 | Email: mtezyan@irell.com

From: Tezyan, Michael <mtezyan@irell.com>

Sent: Wednesday, June 12, 2024 3:14 PM

To: Daniel Tishman <tishman@fr.com>; FISH SERVICE Samsung/Netlist 22cv00293 <FISHSERVICESamsung/Netlist22cv00293@fr.com>; ~Smith, Melissa <melissa@gillamsmithlaw.com>

Cc: #Netlist-Samsung293 <Netlist-Samsung293@irell.com>; jtruelove@mckoolsmith.com

Subject: Netlist v. Samsung-293: McAlexander Depo

Counsel,

Please let us know when Mr. McAlexander is available for deposition.

Thanks,
Michael

Michael Tezyan

Associate

IRELL & MANELLA LLP
1800 Avenue of the Stars, Suite 900
Los Angeles, CA 90067
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Exhibit J

UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

NETLIST, INC.,)
Plaintiff,)
vs.) CASE NO. 2:22cv293JRG
SAMSUNG ELECTRONICS CO.,)
LTD.,)
Defendant.)
_____)

CONFIDENTIAL - ATTORNEYS' EYES ONLY

CORRECTED TRANSCRIPT OF
REMOTE VIDEOTAPED DEPOSITION UPON ORAL
EXAMINATION OF JOSEPH McALEXANDER

FRIDAY, JULY 19, 2024

9:08 A.M. (Central Standard Time)

(All participants appeared remotely)

TAKEN AT THE INSTANCE OF THE PLAINTIFF

REPORTED BY:

MONNA J. NICKESON, RPR, CRR, CCR, CSR CA 14430

JOB: 6792757

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20

[REDACTED]

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[REDACTED]

BY MR. SHEASBY:

22

Q. Okay. And you looked at the patent

23

in preparation for your report, correct?

24

A. Yes.

25

Q. And the strobe signal line is part

1 of the data path, correct?

2 MR. DRYER: Objection. Form.

3 THE WITNESS: Well, the strobe
4 signal line is to -- it's part of the read
5 operation. It'll basically signal to the
6 particular buffer that it's located in when
7 it can then time the read.

8 BY MR. SHEASBY:

9 Q. Right. I'm asking, where is the
10 data path on Figure 3?

11 A. The data path is shown as Y0, Y1
12 through 320, going to DQ0, DQ1, and up through
13 Y minus, N minus 1, to DQ, N minus 1.

14 Q. Let me do it this way.

15 A. So if you look at the top three
16 circuits that are shown, from right to left, Y0
17 to DQ, Y1 to DQ1, Y, paren, N minus one, paren,
18 to DQ, paren, N minus one, paren, those three
19 upper blocks is your read path, is your path of
20 data. And down in the I.D. control block you
21 will see a YDQS input to a DQS output. That's
22 the strobe.

23 So you've got the lines at the top
24 are for your data and the strobe is line 324,
25 which is DQS line.

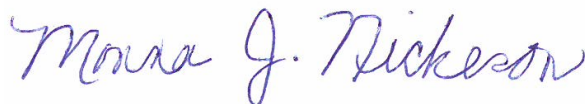
C E R T I F I C A T E

I, MONNA J. NICKESON, CCR, CSR, CLR, RPR, CRR, the undersigned Certified Court Reporter, authorized to administer oaths and affirmations in and for the states of Washington (3322), Oregon (16-0441), Idaho (1045), and California (14430), do hereby certify:

That the sworn testimony and/or proceedings, a transcript of which is attached, was given before me at the time and place stated therein; that the witness was duly sworn or affirmed to testify to the truth; that the testimony and/or proceedings were stenographically recorded by me and transcribed under my supervision. That the foregoing transcript contains a full, true, and accurate record of all the testimony and/or proceedings occurring at the time and place stated in the transcript.

That I am in no way related to any party to the matter, nor to any counsel, nor do I have any financial interest in the event of the cause.

IN WITNESS WHEREOF I have set my hand on
July 24, 2024.



MONNA J. NICKESON, CCR, CSR, CLR, RPR, CRR

Exhibit K

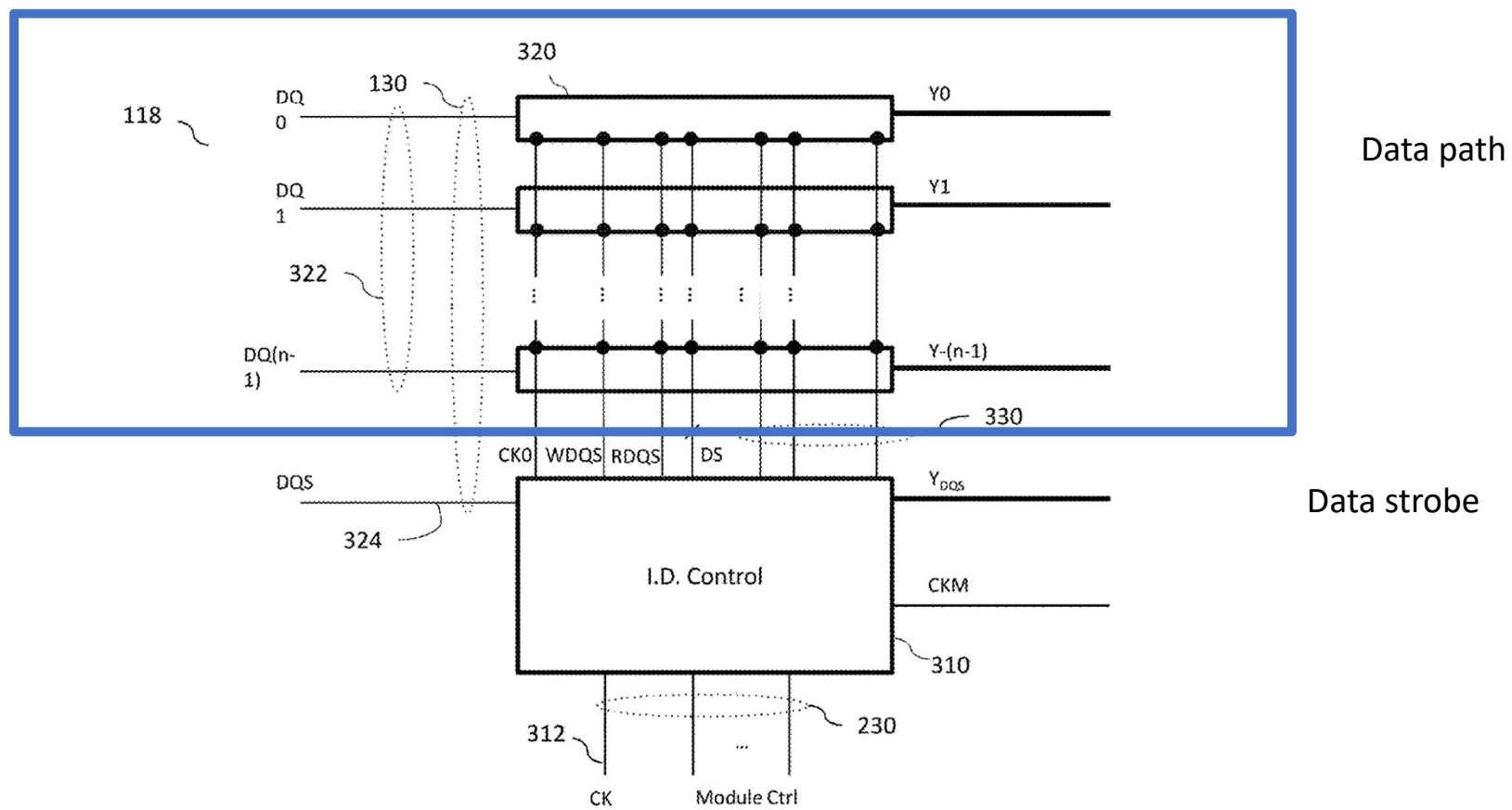


FIG. 3

Exhibit L

From: Lindsay, Jonathan <jlindsay@irell.com>
Sent: Thursday, August 8, 2024 5:27 PM
To: Daniel Tishman; jsheasby@irell.com; Eliot.Williams@BakerBotts.com; Katherine Reardon; FISH SERVICE Samsung/Netlist 22cv00293; melissa@gillamsmithlaw.com
Cc: DL Samsung Netlist IPRs; #NetlistIPR [Int]; #Netlist-Samsung293; jtruelove@mckoolsmith.com
Subject: RE: IPR2023-00847 (608 Patent) - Testimony of Joseph McAlexander

Follow Up Flag: Follow up
Flag Status: Flagged

Counsel,

We intend to seek leave to file a motion for supplemental information under 37 CFR § 42.123 of the designated testimony and exhibit. Please let us know if you oppose.

Regarding your requests to submit Exhibit D of Netlist's infringement contentions, Netlist's position is that the claimed "data path" of the '608 patent does not include a strobe signal line. And for completeness and to address your request, however, we would be happy to seek leave to submit the relevant portions of Dr. Mangione-Smith's infringement report to the Board, with third-party confidential information redacted out. Please let us know whether Samsung has any objections to submitting Dr. Mangione-Smith's report which reflects Netlist's infringement position that will be presented to the jury. If not, we can include that in our email request to the Board as well. We propose to submit the following paragraphs of Dr. Mangione-Smith's infringement report: 62, 66 with annotated write path, 71 with annotated read path, 77, 78, 83, 102-103 (making clear that "MDQ[3:0] and DQ[3:0] would be a data signal on the data path.").

Best regards,

Jonathan

From: Daniel Tishman <tishman@fr.com>
Sent: Thursday, August 8, 2024 11:31 AM
To: Sheasby, Jason <JSheasby@irell.com>; Lindsay, Jonathan <jlindsay@irell.com>; Eliot.Williams@BakerBotts.com; Katherine Reardon <reardon@fr.com>; FISH SERVICE Samsung/Netlist 22cv00293 <FISHSERVICESamsung/Netlist22cv00293@fr.com>; ~Smith, Melissa <melissa@gillamsmithlaw.com>
Cc: DL Samsung Netlist IPRs <dlsamsungnetlistiprs@BakerBotts.com>; #NetlistIPR [Int] <NetlistIPR@irell.com>; #Netlist-Samsung293 <Netlist-Samsung293@irell.com>; jtruelove@mckoolsmith.com
Subject: RE: IPR2023-00847 (608 Patent) - Testimony of Joseph McAlexander

Counsel:

Pursuant to Netlist's request, Samsung de-designates the following from Mr. McAlexander's deposition: page 91, line 22 to page 93, line 10, and Ex. 101.

Please confirm, as soon as possible, that Netlist will similarly de-designate Exhibit D to its infringement contentions (which Netlist previously insisted are confidential), so that Samsung can bring Netlists non-

confidential statements that the claimed “data path” of the ’608 patent can include a strobe signal to the PTAB’s attention.

Best regards,
Dan

Daniel Tishman

Principal ■ Fish & Richardson P.C.

T: +1 (202) 626-7725 | tishman@fr.com

From: Daniel Tishman <tishman@fr.com>

Sent: Wednesday, August 07, 2024 4:18 PM

To: jsheasby@irell.com; Lindsay, Jonathan <jlindsay@irell.com>; Eliot.Williams@BakerBotts.com; Katherine Reardon <reardon@fr.com>; FISH SERVICE Samsung/Netlist 22cv00293 <FISHSERVICESamsung/Netlist22cv00293@fr.com>; melissa@gillamsmithlaw.com

Cc: DL Samsung Netlist IPRs <dlsamsungnetlistiprs@BakerBotts.com>; #NetlistIPR [Int] <NetlistIPR@irell.com>; #Netlist-Samsung293 <Netlist-Samsung293@irell.com>; jtruelove@mckoolsmith.com

Subject: RE: IPR2023-00847 (608 Patent) - Testimony of Joseph McAlexander

Jason –

Please advise on the second part of my email by the end of the day. I’ve re-pasted it here for your convenience: “In the meantime, would you please advise whether Netlist contends that Exhibit D to its infringement contentions is confidential, and whether it may be used for other purposes (e.g., in the IPR proceedings)?”

If needed, we will seek appropriate relief from the Court.

Best regards,
Dan

Daniel Tishman

Principal ■ Fish & Richardson P.C.

T: +1 (202) 626-7725 | tishman@fr.com

From: Sheasby, Jason <JSheasby@irell.com>

Sent: Wednesday, August 07, 2024 3:51 PM

To: Daniel Tishman <tishman@fr.com>; Lindsay, Jonathan <jlindsay@irell.com>; Eliot.Williams@BakerBotts.com; Katherine Reardon <reardon@fr.com>; FISH SERVICE Samsung/Netlist 22cv00293 <FISHSERVICESamsung/Netlist22cv00293@fr.com>; melissa@gillamsmithlaw.com

Cc: DL Samsung Netlist IPRs <dlsamsungnetlistiprs@BakerBotts.com>; #NetlistIPR [Int] <NetlistIPR@irell.com>; #Netlist-Samsung293 <Netlist-Samsung293@irell.com>; jtruelove@mckoolsmith.com

Subject: Re: IPR2023-00847 (608 Patent) - Testimony of Joseph McAlexander

We will be moving in the PTAB to enforce Samsung’s obligation of disclosure, which it cannot seek to evade via a meritless designation of confidentiality.

Thanks
JS

From: Daniel Tishman <tishman@fr.com>
Date: Wednesday, August 7, 2024 at 12:48 PM
To: "Lindsay, Jonathan" <jlindsay@irell.com>, "Eliot.Williams@BakerBotts.com" <Eliot.Williams@BakerBotts.com>, Katherine Reardon <reardon@fr.com>, FISH SERVICE Samsung/Netlist 22cv00293 <FISHSERVICESamsung/Netlist22cv00293@fr.com>, Melissa ~Smith <melissa@gillamsmithlaw.com>
Cc: DL Samsung Netlist IPRs <dlsamsungnetlistiprs@BakerBotts.com>, "#NetlistIPR [Int]" <NetlistIPR@irell.com>, #Netlist-Samsung293 <Netlist-Samsung293@irell.com>, "jtruelove@mckoolsmith.com" <jtruelove@mckoolsmith.com>
Subject: RE: IPR2023-00847 (608 Patent) - Testimony of Joseph McAlexander

Hi Jonathan – it's not clear if you are requesting any particular relief in the EDTX (we had understood your email to be related to the IPR based on the subject line). Are you seeking to de-designate testimony in EDTX? Under the protective order in EDTX, a party can submit a written request to de-designate, and the party that made the confidentiality designation has 10 days in which to respond, and then they may seek relief from the Court if the matter can't be resolved within that time period. See Dkt. 60, ¶ 19. In any event, we will be in a position to get back to you soon—hopefully in the next day or two.

In the meantime, would you please advise whether Netlist contends that Exhibit D to its infringement contentions is confidential, and whether it may be used for other purposes (e.g., in the IPR proceedings)?

Best regards,
Dan

Daniel Tishman
Principal ■ Fish & Richardson P.C.
T: +1 (202) 626-7725 | tishman@fr.com

From: Lindsay, Jonathan <jlindsay@irell.com>
Sent: Wednesday, August 07, 2024 1:30 PM
To: Eliot.Williams@BakerBotts.com; Katherine Reardon <reardon@fr.com>; FISH SERVICE Samsung/Netlist 22cv00293 <FISHSERVICESamsung/Netlist22cv00293@fr.com>; melissa@gillamsmithlaw.com
Cc: DL Samsung Netlist IPRs <dlsamsungnetlistiprs@BakerBotts.com>; #NetlistIPR [Int] <NetlistIPR@irell.com>; #Netlist-Samsung293 <Netlist-Samsung293@irell.com>; jtruelove@mckoolsmith.com
Subject: RE: IPR2023-00847 (608 Patent) - Testimony of Joseph McAlexander

[This email originated outside of F&R.]

All,

The obligation to disclose inconsistent information in an IPR belongs to Samsung, not to a law firm. Mr. McAlexander was retained by Samsung and gave testimony which is inconsistent with positions Samsung is taking in the IPR. We've identified the testimony in question. This testimony is inconsistent with the arguments Samsung advanced in the Petition and Petitioner's Reply that the claimed "data path" of the 608 patent can include a DQS strobe signal line.

It is Samsung's self-executing obligation to de-designate the inconsistent testimony and serve it under 37 CFR § 42.51(b)(iii). It has not done so, which is the root cause of us now having to seek leave to file a motion to compel. Since all law firms representing Samsung in connection with the 608 patent were on the original email, I assume Samsung has been informed of the request. Since we have not received a response, we will email the Board noting Samsung refuses to take a position on the request.

Jonathan

From: Williams, Eliot D. <Eliot.Williams@BakerBotts.com>>
Sent: Tuesday, August 6, 2024 4:10 PM
To: Lindsay, Jonathan <jlindsay@irell.com>>; Katherine Reardon <reardon@fr.com>>; FISH SERVICE Samsung/Netlist 22cv00293 <FISHSERVICESamsung/Netlist22cv00293@fr.com>>; ~Smith, Melissa <melissa@gillamsmithlaw.com>>
Cc: DL Samsung Netlist IPRs <dlsamsungnetlistiprs@BakerBotts.com>>; #NetlistIPR [Int] <NetlistIPR@irell.com>>; #Netlist-Samsung293 <Netlist-Samsung293@irell.com>>; jtruelove@mckoolsmith.com <jtruelove@mckoolsmith.com>
Subject: RE: IPR2023-00847 (608 Patent) - Testimony of Joseph McAlexander

Jonathan,

Baker Botts is not counsel in the district court litigation and does not have this deposition transcript, which your email indicates "is marked confidential" pursuant to the Protective Order in the district court. After you resolve any Protective Order issues with counsel in the district court litigation, please send us the testimony in question and what you are proposing to do with it in IPR2023-00847 so that we can consider your request.

Regards,

Eliot D. Williams
BAKER BOTTS LLP ■
+1 202 639-1334 (Direct Dial)

From: Lindsay, Jonathan <jlindsay@irell.com>>
Sent: Tuesday, August 6, 2024 5:46 PM
To: Katherine Reardon <reardon@fr.com>>; FISH SERVICE Samsung/Netlist 22cv00293 <FISHSERVICESamsung/Netlist22cv00293@fr.com>>; EXT Smith, Melissa (T-Mobile) <melissa@gillamsmithlaw.com>>
Cc: Williams, Eliot D. <Eliot.Williams@BakerBotts.com>>; DL Samsung Netlist IPRs <dlsamsungnetlistiprs@BakerBotts.com>>; #NetlistIPR [Int] <NetlistIPR@irell.com>>; #Netlist-Samsung293 <Netlist-Samsung293@irell.com>>; jtruelove@mckoolsmith.com <jtruelove@mckoolsmith.com>
Subject: RE: IPR2023-00847 (608 Patent) - Testimony of Joseph McAlexander

[EXTERNAL EMAIL]
Counsel,

We still have not received a response. Please let us know if you oppose. If we do not hear back, will note your lack of a response when we contact the Board.

Jonathan

From: Lindsay, Jonathan
Sent: Thursday, August 1, 2024 11:47 AM
To: Katherine Reardon <reardon@fr.com>>; FISH SERVICE Samsung/Netlist 22cv00293 <FISHSERVICESamsung/Netlist22cv00293@fr.com>>; ~Smith, Melissa <melissa@gillamsmithlaw.com>>

Cc: Williams, Eliot D. <Eliot.Williams@BakerBotts.com<<mailto:Eliot.Williams@BakerBotts.com>>>; DL Samsung Netlist IPRs <dlsamsungnetlistiprs@BakerBotts.com<<mailto:dlsamsungnetlistiprs@BakerBotts.com>>>; #NetlistIPR [Int] <NetlistIPR@irell.com<<mailto:NetlistIPR@irell.com>>>; #Netlist-Samsung293 <Netlist-Samsung293@irell.com<<mailto:Netlist-Samsung293@irell.com>>>; jtruelove@mckoolsmith.com<<mailto:jtruelove@mckoolsmith.com>>>
Subject: IPR2023-00847 (608 Patent) - Testimony of Joseph McAlexander

Counsel,

We intend to seek leave to file a motion to compel relating to the testimony given by Joseph McAlexander on July 19, 2024 relating to the meaning of “data path” in the context of the ’608 patent. The testimony is found on page 91, line 22 to page 93, line 10, and Ex. 101. Although the transcript is marked confidential, this testimony is clearly not confidential and must be produced in IPR2023-00847 under PTAB rules as it is inconsistent with positions taken by Samsung in the IPR.

Please let us know if you oppose.

Jonathan M. Lindsay
Irell & Manella LLP
840 Newport Center Drive, Suite 400
Newport Beach, CA 92660
Direct: 949.760.5220

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