

Samsung Electronics Co., Ltd.
v.
Netlist, Inc.

IPR2023-00847
U.S. Patent No. 10,268,608 B2



Patent Owner's Demonstratives

Roadmap

- ▶ Overview of the '608 patent
- ▶ Netlist's arguments are not collaterally estopped based on IPR2022-00236
- ▶ Claim Construction: Claim 1's "data path" does not include strobe signal lines
- ▶ Ground 1: Hiraishi and Butt do not teach (1) claim 1's "delay circuit" and (2) determining "an amount" to delay a "signal through the data path" as required in claim 1
- ▶ Ground 2: Hiraishi, Butt, and Tokuhiro do not teach claim 1's "delay circuit," and a POSITA would not have combined the references as proposed
- ▶ Netlist's Motion to Strike: The Board should strike portions of Samsung's Reply

Overview of the '608 Patent

1. A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising:

a module board having edge connections for coupling to a module control device mounted on the module board and configured to receive system command signals for memory operations via the set of control/address signal lines and to output module command signals and module control signals in response to the system command signals, the module control device being further configured to receive a system clock signal and output a module clock signal; and

memory devices including a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data/strobe signal lines; and

a plurality of buffer circuits, each respective buffer circuit including a data path corresponding to each data signal line in the respective set of data/strobe signal lines, and a command processing circuit configured to decode the module control signals and to control the data path in accordance with the module control signals and the module clock signal, wherein the data path corresponding to the each data signal line includes at least one tristate buffer controlled by the command processing circuit and a delay circuit configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals.

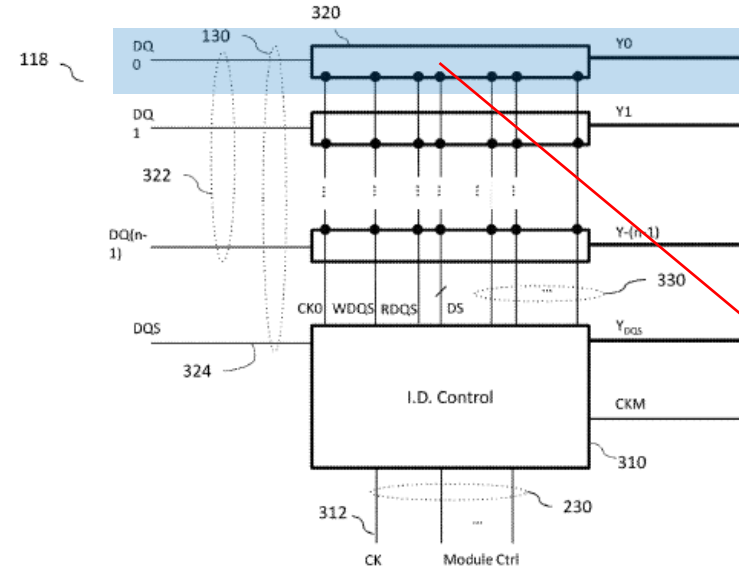


FIG. 3

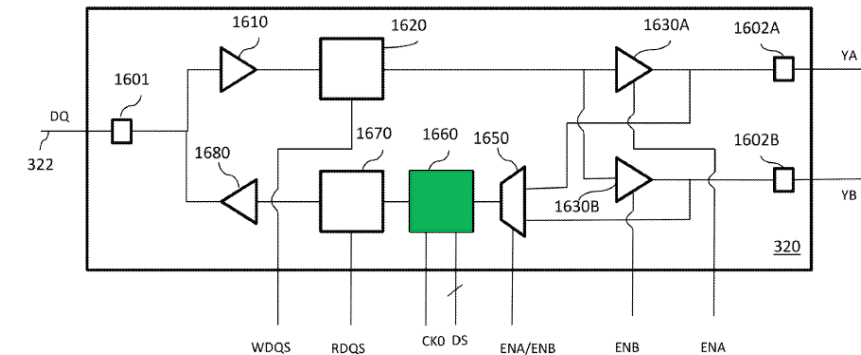


FIG. 16

EX1001, '608 patent, claim 1.

Claim 1 of the '608 Patent

1. A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising:

- a module board having edge connections for coupling to respective signal lines in the memory bus;
- a module control device mounted on the module board and configured to receive system command signals for memory operations via the set of control/address signal lines and to output module command signals and module control signals in response to the system command signals, the module control device being further configured to receive a system clock signal and output a module clock signal; and

memory devices mounted on the module board and configured to receive the module command signals and the module clock signal, and to perform the memory operations in response to the module command signals, the memory devices including a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data/strobe signal lines; and

a plurality of buffer circuits corresponding to respective sets of the plurality of sets of data/strobe signal lines, wherein each respective buffer circuit of the plurality of buffer circuits is mounted on the module board, coupled between a respective set of data/strobe signal lines and a respective set of memory devices, and configured to receive the module control signals and the module clock signal, the each respective buffer circuit including a data path corresponding to each data signal line in the respective set of data/strobe signal lines, and a command processing circuit configured to decode the module control signals and to control the data path in accordance with the module control signals and the module clock signal, wherein the data path corresponding to the each data signal line includes at least one tristate buffer controlled by the command processing circuit and a delay circuit configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals.

Netlist's arguments are not collaterally estopped

Four Factors of Collateral Estoppel

United States Court of Appeals for the Federal Circuit

GOOGLE LLC,
Appellant

v.

HAMMOND DEVELOPMENT INTERNATIONAL,
INC.,
Appellee

2021-2218

Appeal from the United States Patent and Trademark
Office, Patent Trial and Appeal Board in No. IPR2020-
00081.

Decided: December 8, 2022

J. MICHAEL JAKES, Finnegan, Henderson, Farabow,
Garrett & Dunner, LLP, Washington, DC, argued for ap-
pellant. Also represented by ERIKA ARNER, SYDNEY
KESTLE, KEVIN D. RODKEY, Atlanta, GA; DANIEL C.
TUCKER, Reston, VA.

TIMOTHY EDWARD GROCHOCINSKI, Nelson Bumgardner
Conroy PC, Orland Park, IL, argued for appellee. Also rep-
resented by CHARLES AUSTIN GINNINGS.

Board's decision in an IPR once it becomes final.”). The party seeking to invoke collateral estoppel must show:

(1) the issue is identical to one decided in the first action; (2) the issue was actually litigated in the first action; (3) resolution of the issue was essential to a final judgment in the first action; and (4) [the party against whom collateral estoppel is being asserted] had a full and fair opportunity to litigate the issue in the first action.

In re Freeman, 30 F.3d 1459, 1465 (Fed. Cir. 1994).

Collateral Estoppel Does Not Apply: Issues Are Not Identical

The claims of the '608 patent are materially different than the claims of the '035 patent

'608 patent, claim 1 (in part)

a plurality of buffer circuits corresponding to respective sets of the plurality of sets of data/strobe signal lines, wherein each respective buffer circuit of the plurality of buffer circuits is mounted on the module board, coupled between a respective set of data/strobe signal lines and a respective set of memory devices, and configured to receive the module control signals and the module clock signal, the each respective buffer circuit including a data path corresponding to each data signal line in the respective set of data/strobe signal lines, and a command processing circuit configured to decode the module control signals and to control the data path in accordance with the module control signals and the module clock signal, wherein the data path corresponding to the each data signal line includes at least one tristate buffer controlled by the command processing circuit and a delay circuit configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals.

'035 patent, claim 1 (in part)

a plurality of buffer circuits mounted on the module board in positions corresponding to respective sets of the plurality of sets of data/strobe signal lines, wherein each respective buffer circuit of the plurality of buffer circuits is coupled between a respective set of data/strobe signal lines and a respective set of memory devices, the each respective buffer circuit including data paths for transmitting respective data and strobe signals associated with the first memory operation and logic configured to respond to the module control signals by enabling the data paths, wherein the logic is further configured to obtain timing information based on one or more signals received by the each respective buffer circuit during a second memory operation prior to the first memory operation and to control timing of the respective data and strobe signals on the data paths in accordance with the timing information.

Collateral Estoppel Does Not Apply: Issues Are Not Identical

The unpatentability theories are different in this IPR than in IPR2022-00236

Osanai explains that in read leveling, the timing of read data output from the memory chips and the input timing of the read command is measured for each memory chip and “used in an adjustment of an activation timing of the input buffer circuit INB and the like.” Ex. 1005 ¶ 157. But, as Petitioner points out, Osanai does so “in consideration of a propagation time of a signal.” Ex. 1005 ¶ 146. Petitioner further indicates that Dr. Przybyski testified that the input buffers (INB) act as a gate allowing data and strobe signals to either pass through or not pass through. Ex. 1022, 70:10–22. We determine that these disclosures of Osanai are sufficient to teach controlling the timing of the data and strobe signals on the data paths on which those signals travel.

EX1066, '236 FWD, 35-36.

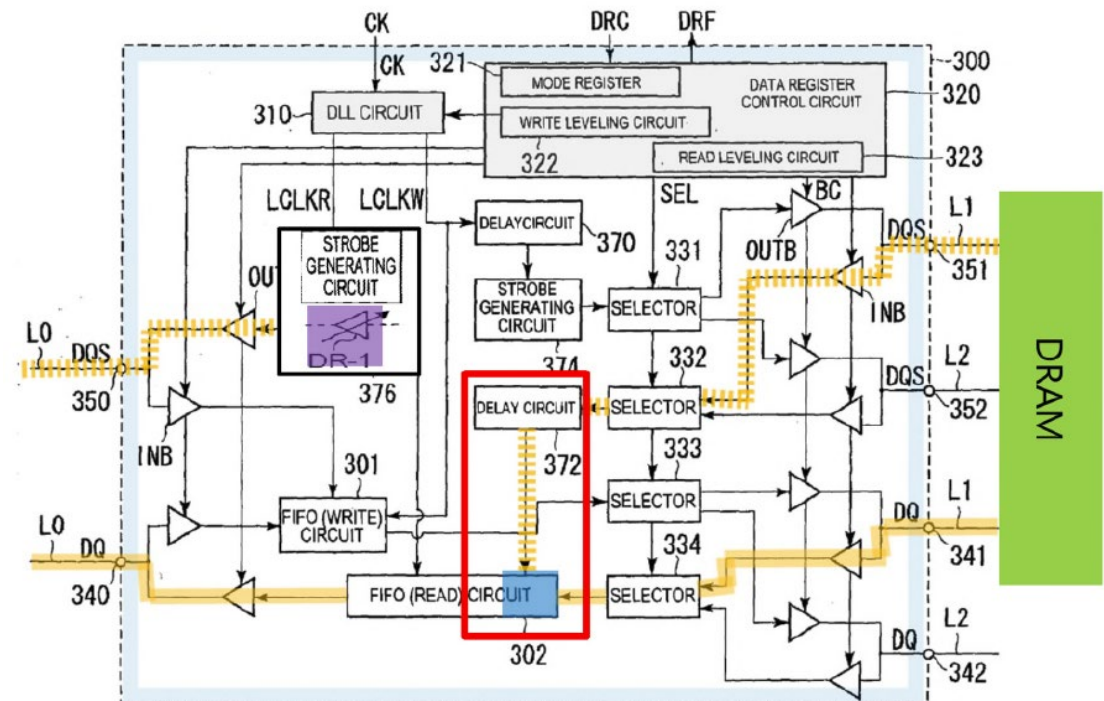


FIG. 5

Paper 1, Petition, 89 (annotating Hiraishi, FIG. 5).

Claim Construction:
Claim 1's "data path" does not include strobe signal lines

Claim 1's "data path"

'608 patent, claim 1 (in part):

clock signal, the each respective buffer circuit including a data path corresponding to each data signal line in the respective set of data/strobe signal lines, and a command processing circuit configured to decode the module control signals and to control the data path in accordance with the module control signals and the module clock signal, wherein the data path corresponding to the each data signal line includes at least one tristate buffer controlled by the command processing circuit and a delay circuit configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals.

Netlist's Construction: claim 1's data path does not include strobe signal lines

Samsung's Construction: claim 1's data path includes both data signal lines and strobe signal lines

Figure 3 Supports Netlist's Construction

“each respective buffer circuit including a data path corresponding to each data signal line in the respective set of data/strobe signal lines”

In one embodiment, as shown in FIG. 3, each group of signal lines 130 include a set of n data (DQ) signal lines 322 each for transmitting one of a set of data signals $DQ_0, DQ_1, \dots, DQ_{n-1}$, and at least one strobe (DQS) signal line 324 for transmitting at least one strobe signal DQS. Each set of module data/strobe lines Y include a set of n module data signal lines $Y_0, Y_1, \dots, Y_{n-1}$ and at least one module strobe signal line Y_{DQS} . When the subsets of memory devices are

'608 patent, EX1001, 10:31-38.

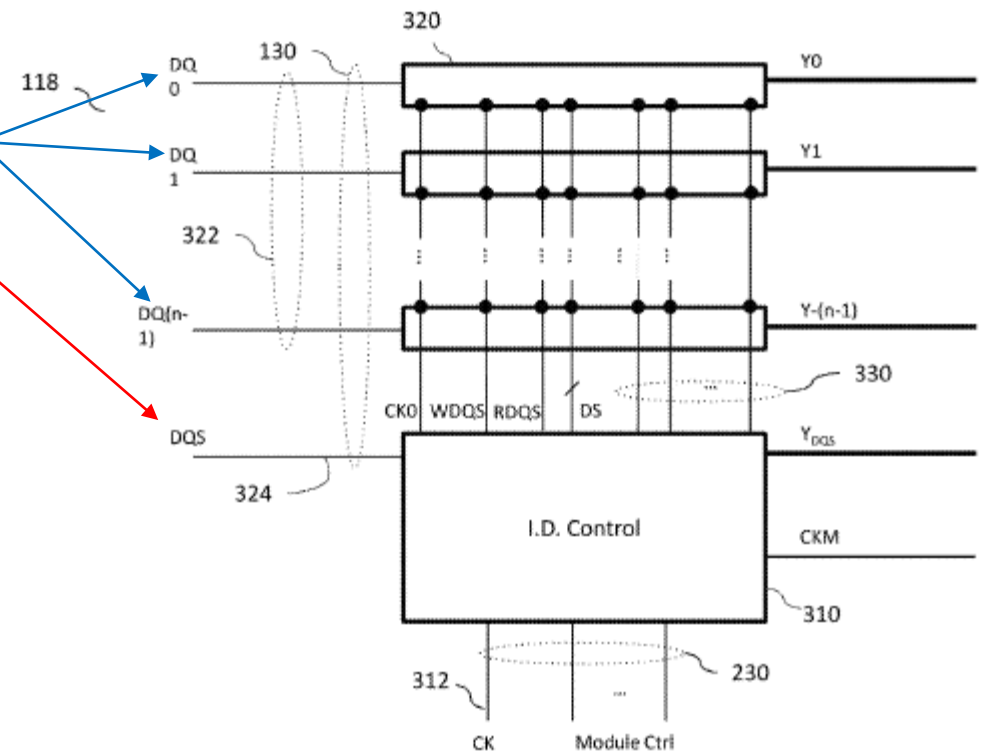


FIG. 3 EX1001, '608 patent, FIG. 3.

Samsung's DCT Expert Confirmed Netlist's Construction

15 A. So if you look at the top three
16 circuits that are shown, from right to left, Y0
17 to DQ, Y1 to DQ1, Y, paren, N minus one, paren,
18 to DQ, paren, N minus one, paren, those three
19 upper blocks is your read path, is your path of
20 data. And down in the I.D. control block you
21 will see a YDQS input to a DQS output. That's
22 the strobe.

23 So you've got the lines at the top
24 are for your data and the strobe is line 324,
25 which is DQS line.

Paper 35, PO. Mot. To Submit Supp. Information, Attachment A, 4.

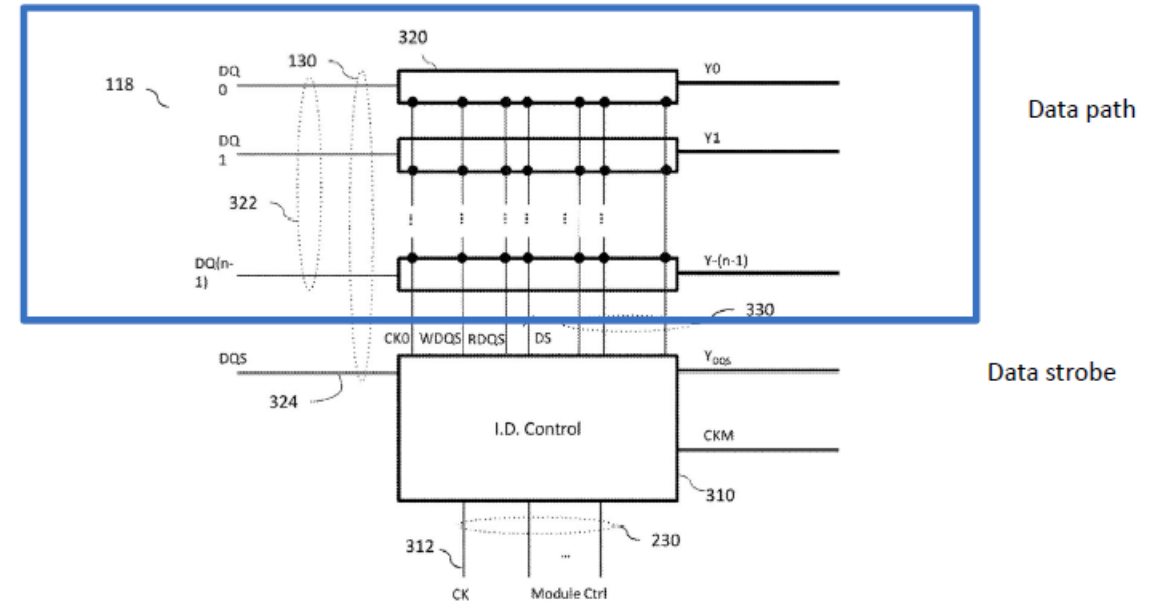


FIG. 3

EX1001, '608 patent, FIG. 3 (annotated).

Figure 16 Supports Netlist's Construction

DQ line YB_{DQ} . The DQ routing circuit 320 further includes a first write data path coupled between the first DQ pin 1601 and the second DQ pin 1602A and a second write data path coupled between the first DQ pin 1601 and the third DQ pin 1602B. The first write data path includes a write data buffer

The DQ routing circuit further includes a read data path coupled between the first DQ pin 1601 and a selected one of the second and third DQ pins 1602A and 1602B. In the read

EX1001, '608 patent, 17:29-33; 17:48-50, FIGs. 3, 16 (annotated).

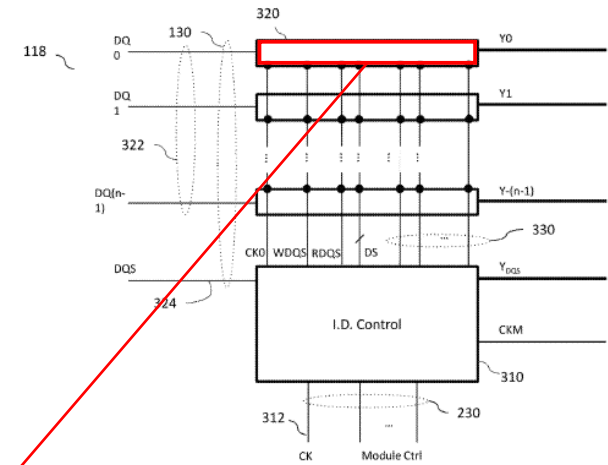


FIG. 3

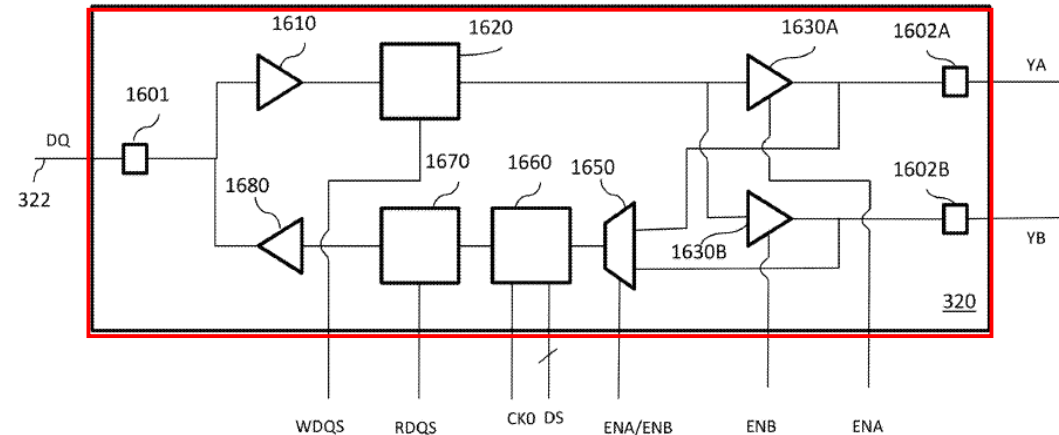


FIG. 16

Figure 15 Supports Netlist's Construction

module DQS line YB_{DQS} . The DQS routing circuit 620 further includes a first write strobe path coupled between the first DQS pin 1501 and the second DQS pin 1502A and a second write strobe path coupled between the first DQS pin 1501 and the third DQS pin 1502B. The first write strobe

The DQS routing circuit further includes a read strobe path coupled between the first DQS pin 1501 and a selected one of the second and third DQS pins 1502A and 1502B. In

EX1001, '608 patent, 6:53-57, 17:8-10, FIGs. 3, 15 (annotated).

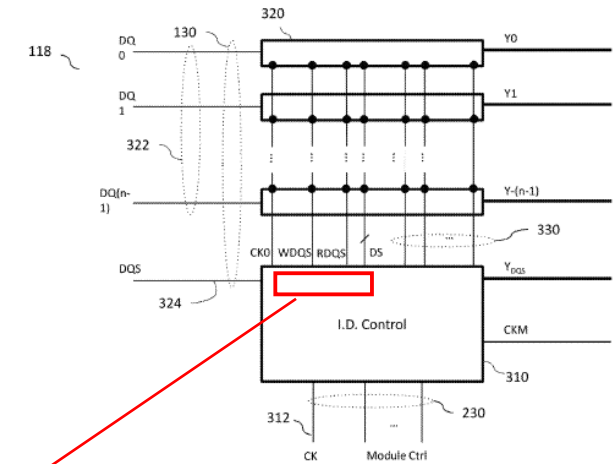


FIG. 3

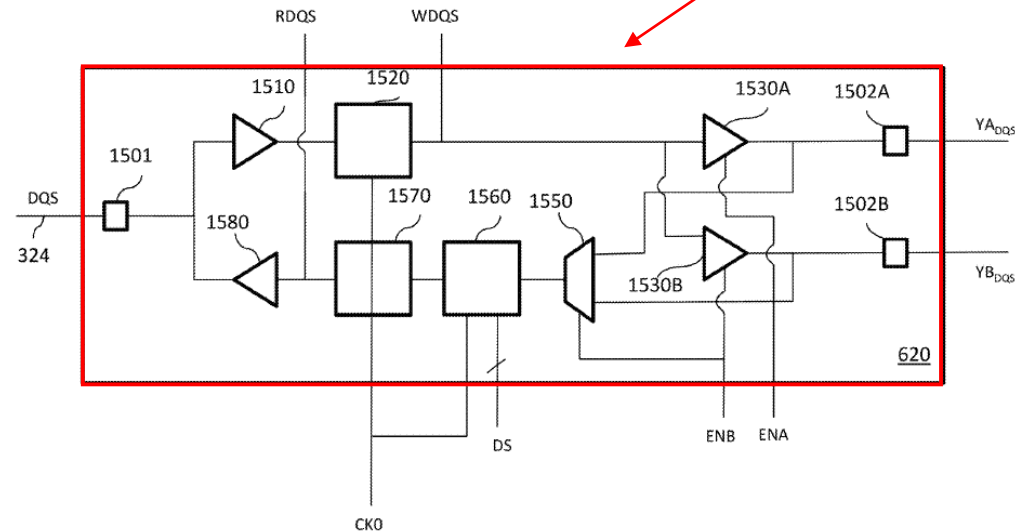


FIG. 15

Dependent Claim 10 Supports Netlist's Construction

No antecedent basis to claim 1's "data path"; claim 10 defines a new "data path"

10. The memory module of claim 9, wherein the each respective buffer circuit includes a first data path for transmitting a strobe signal associated with the second memory operation and a second data path for transmitting a first data signal associated with the second memory operation, the first data path including a sampler that samples the strobe signal in accordance with the local clock signal, and the second data path including a sampler that samples the first data signal in accordance with the sampled strobe signal.

Claim 1 of the '035 Patent Supports Netlist's Construction

'608 patent, claim 1 (in part)

a plurality of buffer circuits corresponding to respective sets of the plurality of sets of data/strobe signal lines, wherein each respective buffer circuit of the plurality of buffer circuits is mounted on the module board, coupled between a respective set of data/strobe signal lines and a respective set of memory devices, and configured to receive the module control signals and the module clock signal, the each respective buffer circuit including a data path corresponding to each data signal line in the respective set of data/strobe signal lines, and a command processing circuit configured to decode the module control signals and to control the data path in accordance with the module control signals and the module clock signal, wherein the data path corresponding to the each data signal line includes at least one tristate buffer controlled by the command processing circuit and a delay circuit configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals.

'035 patent, claim 1 (in part)

a plurality of buffer circuits mounted on the module board in positions corresponding to respective sets of the plurality of sets of data/strobe signal lines, wherein each respective buffer circuit of the plurality of buffer circuits is coupled between a respective set of data/strobe signal lines and a respective set of memory devices, the each respective buffer circuit including data paths for transmitting respective data and strobe signals associated with the first memory operation and logic configured to respond to the module control signals by enabling the data paths, wherein the logic is further configured to obtain timing information based on one or more signals received by the each respective buffer circuit during a second memory operation prior to the first memory operation and to control timing of the respective data and strobe signals on the data paths in accordance with the timing information.

Samsung's Construction Renders Superfluous "each data signal line in"

Samsung's Construction: "each respective buffer circuit including a data path corresponding to each data signal line in the respective set of data/strobe signal lines"

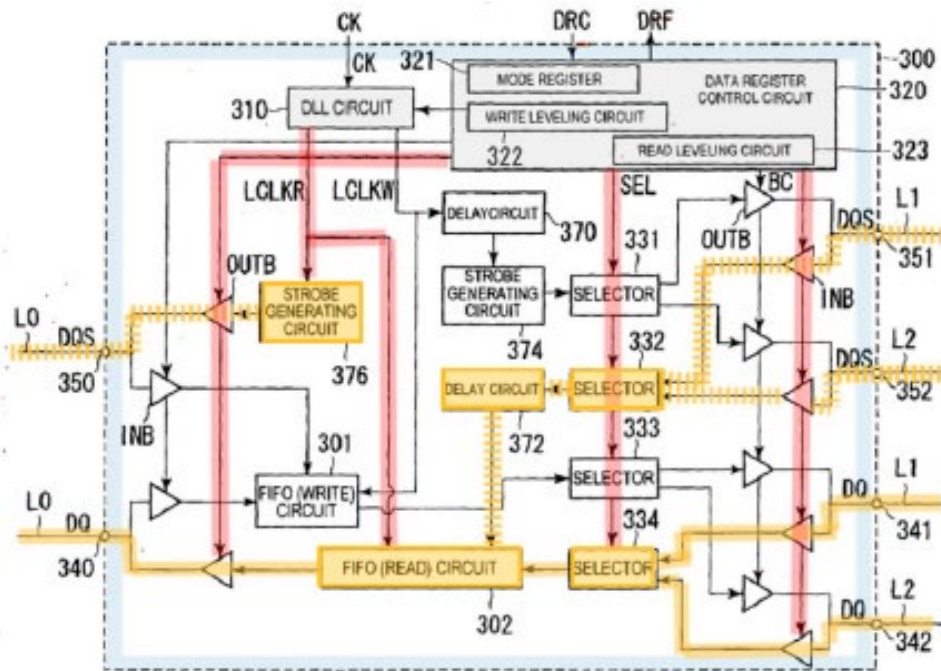


FIG.5

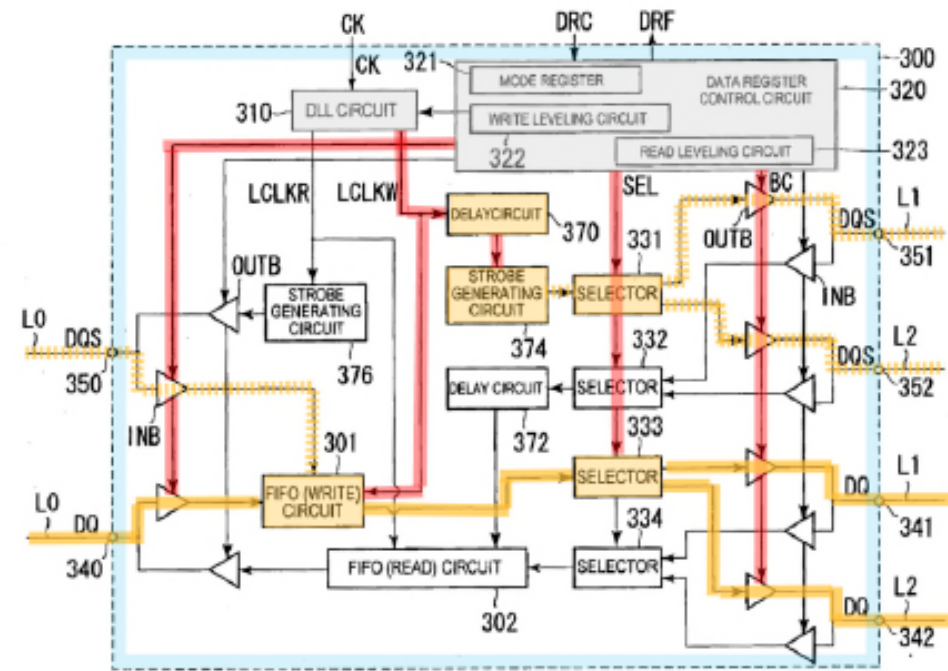


FIG.5

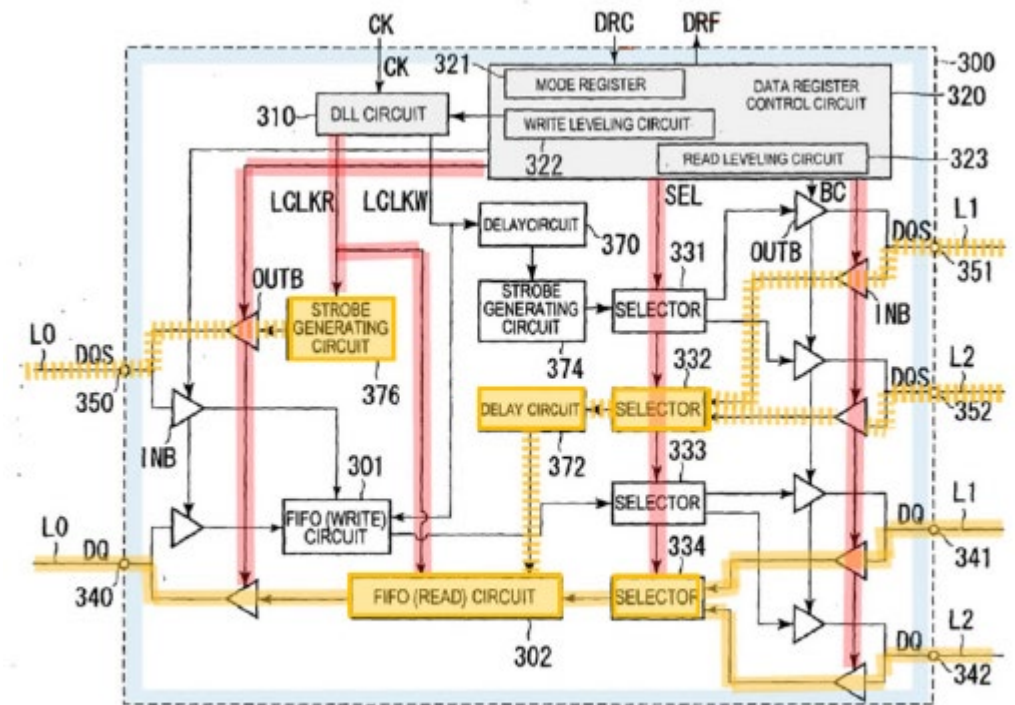
EX1005, Hiraishi, FIG. 5 (annotated).

Ground 1:
Hiraishi and Butt do not teach claim 1's "delay circuit"

Samsung's Original Unpatentability Theory (Element 1[f])

Samsung's original mapping of Hiraishi to claim 1's "data path"

Ground 1 discloses that *"the data path [orange] corresponding to the each data signal line includes at least one tristate buffer [e.g., output buffers OUTB and input buffers INB] controlled by the command processing circuit [including Data Register Control Circuit 320 and logic in DLL Circuit 310] and a delay circuit [including DLL Circuit 310, FIFO (Write) Circuit 301, FIFO (Read) Circuit 302, Delay Circuits 370 and 372, and Strobe Generating Circuits 374 and 376] configured to delay a signal through the data path [e.g., during a read or write operation] by an amount determined by the command processing circuit [e.g., during the Read/Write Leveling step S4 between the memory devices and the data buffer] in response to at least one of the module control signals [e.g., DRC]."* As



Samsung's Original Unpatentability Theory (Element 1[f])

Samsung's original mapping of Hiraishi to claim 1's "tristate buffer," "command processing circuit," and "delay circuit"

Ground 1 discloses that "the data path [orange] corresponding to the each data signal line includes at least one tristate buffer [e.g., output buffers OUTB and input buffers INB] controlled by the command processing circuit [including Data Register Control Circuit 320 and logic in DLL Circuit 310] and a delay circuit [including DLL Circuit 310, FIFO (Write) Circuit 301, FIFO (Read) Circuit 302, Delay Circuits 370 and 372, and Strobe Generating Circuits 374 and 376] configured to delay a signal through the data path [e.g., during a read or write operation] by an amount determined by the command processing circuit [e.g., during the Read/Write Leveling step S4 between the memory devices and the data buffer] in response to at least one of the module control signals [e.g., DRC]." As

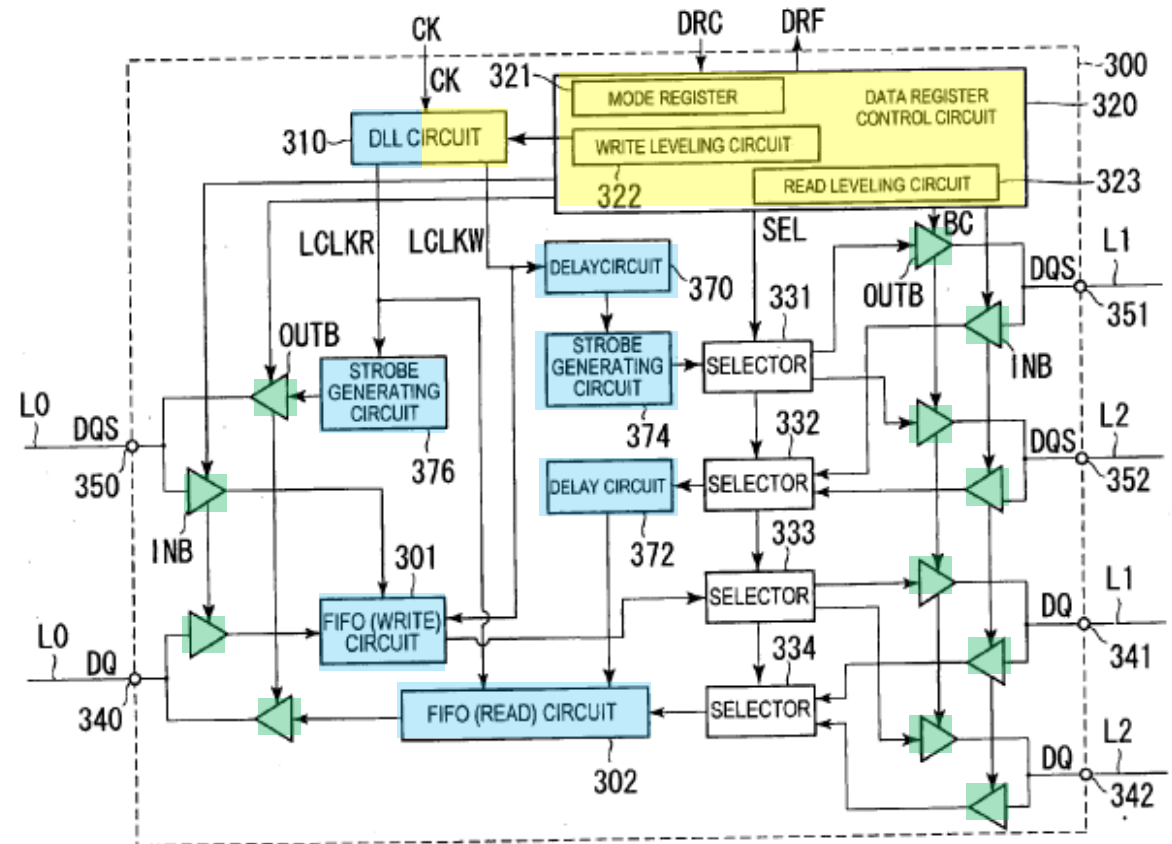


FIG.5

EX1005, Hiraishi, FIG. 5 (annotated).

Samsung's Original Unpatentability Theory (Element 1[f])

Samsung's original mapping of Hiraishi to claim 1's requirement to “delay a signal though the data path by an amount determined by the command processing circuit in response to at least one of the module control signals”

Ground 1 discloses that “the data path [orange] corresponding to the each data signal line includes at least one tristate buffer [e.g., output buffers OUTB and input buffers INB] controlled by the command processing circuit [including Data Register Control Circuit 320 and logic in DLL Circuit 310] and a delay circuit [including DLL Circuit 310, FIFO (Write) Circuit 301, FIFO (Read) Circuit 302, Delay Circuits 370 and 372, and Strobe Generating Circuits 374 and 376] configured to delay a signal through the data path [e.g., during a read or write operation] by an amount determined by the command processing circuit [e.g., during the Read/Write Leveling step S4 between the memory devices and the data buffer] in response to at least one of the module control signals [e.g., DRC].” As

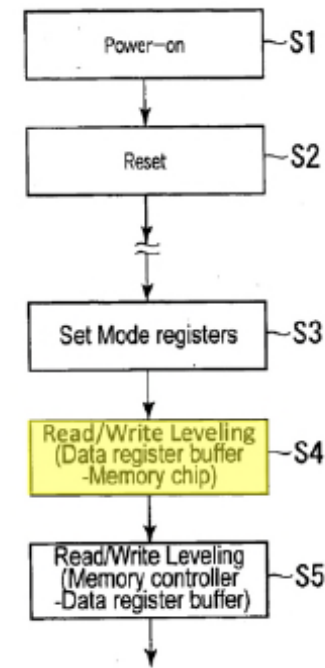


FIG.13

EX1005, Hiraishi, FIG. 13 (annotated).

Samsung's Original, Ground 1 Unpatentability Theory Fails

The alleged “delay circuit” of Hiraishi-Butt includes **circuits** that: (1) are not in the “data path” and (2) delay signals that are not “through the data path”

Ground 1 discloses that “the data path [orange] corresponding to the each data signal line includes at least one tristate buffer [e.g., output buffers OUTB and input buffers INB] controlled by the command processing circuit [including Data Register Control Circuit 320 and logic in DLL Circuit 310] and a delay circuit [including DLL Circuit 310, FIFO (Write) Circuit 301, FIFO (Read) Circuit 302, Delay Circuits 370 and 372, and Strobe Generating Circuits 374 and 376] configured to delay a signal through the data path [e.g., during a read or write operation] by an amount determined by the command processing circuit [e.g., during the Read/Write Leveling step S4 between the memory devices and the data buffer] in response to at least one of the module control signals [e.g., DRC].” As

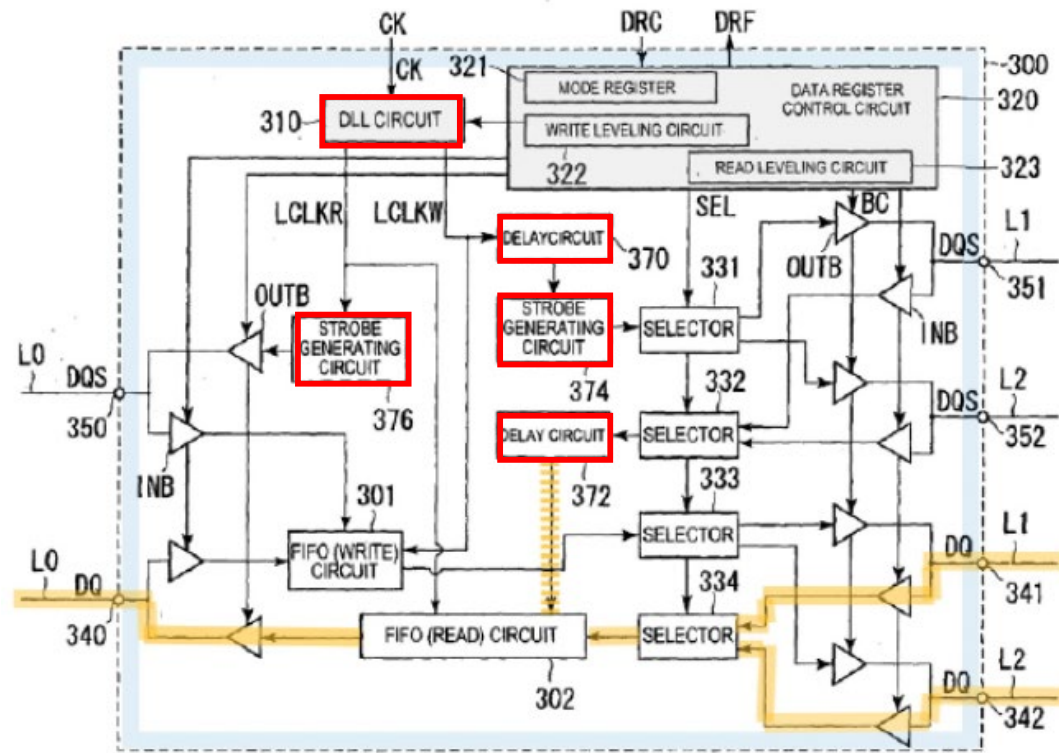


FIG. 5

EX1005, Hiraishi, FIG. 5 (annotated).

Samsung Did Not Allege that Hiraishi's FIFO is Claim 1's "delay circuit"

23 Q. Okay. So I'm trying to understand, so is the
24 delay circuit that reads on Claim 1's delay circuit in
25 your opinion, is that the combination of the components
1 that you list here?

2 A. Well, I believe that all of those different
3 parts make up the delay circuit, so I guess yes, it's a
4 combination of those. I mean, they all work together to
5 implement the delay circuit.

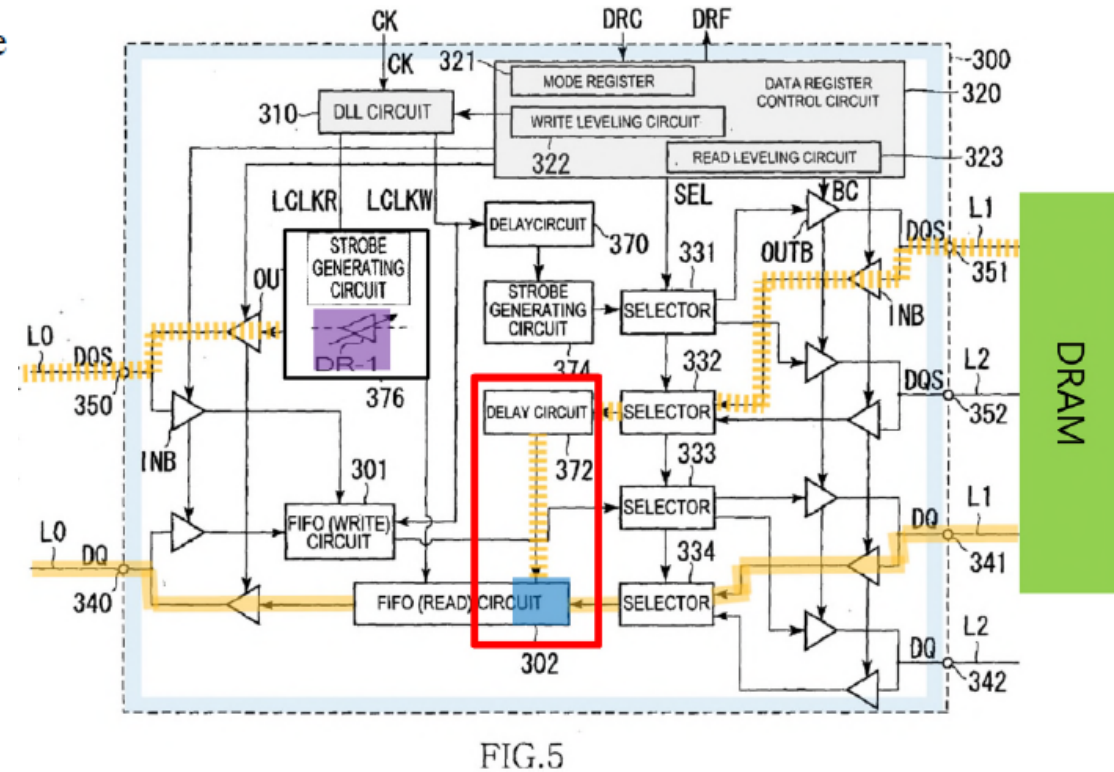
EX2012, Wedig Dep. Tr., 17:23-18:5.

Hiraishi's FIFO Does Not Satisfy Claim 1's "delay circuit"

For Ground 2, Dr. Wedig opined that Hiraishi's existing read FIFO would need to be adapted

showing read data output in synchronization with the corresponding strobe). I note that, in this implementation, Hiraishi's existing read FIFO circuit is adapted to delay the read data, so there is no need to add delay circuits to the data line (DQ).

EX1003, Wedig Decl., ¶ 262



Samsung Changed Theories

Samsung now argues that Hiraishi's FIFO is the claimed "delay circuit"

Petition's Read "Data Path" in Orange

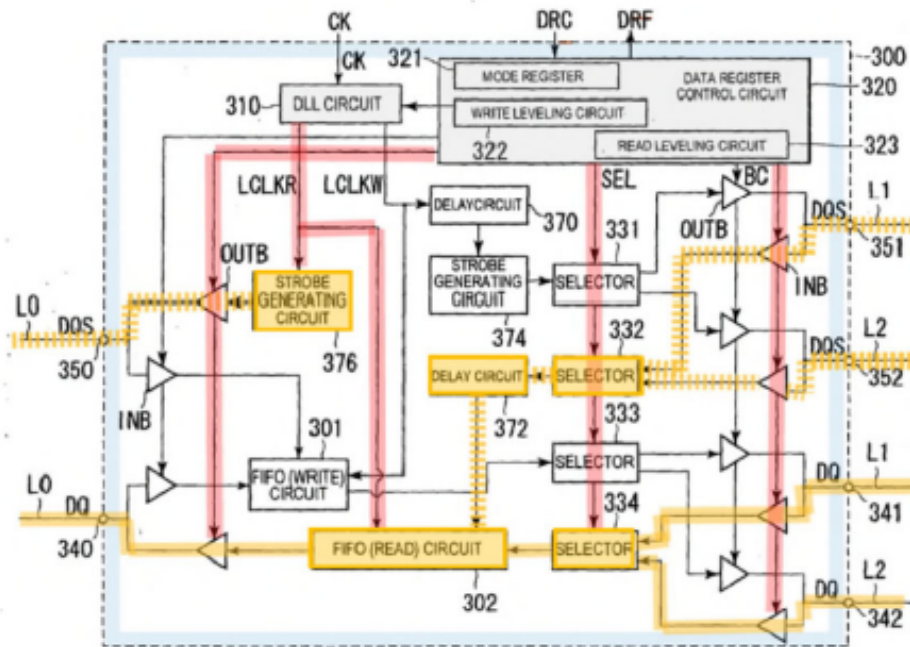


FIG. 5

Reply's Read "Data Path" in Orange

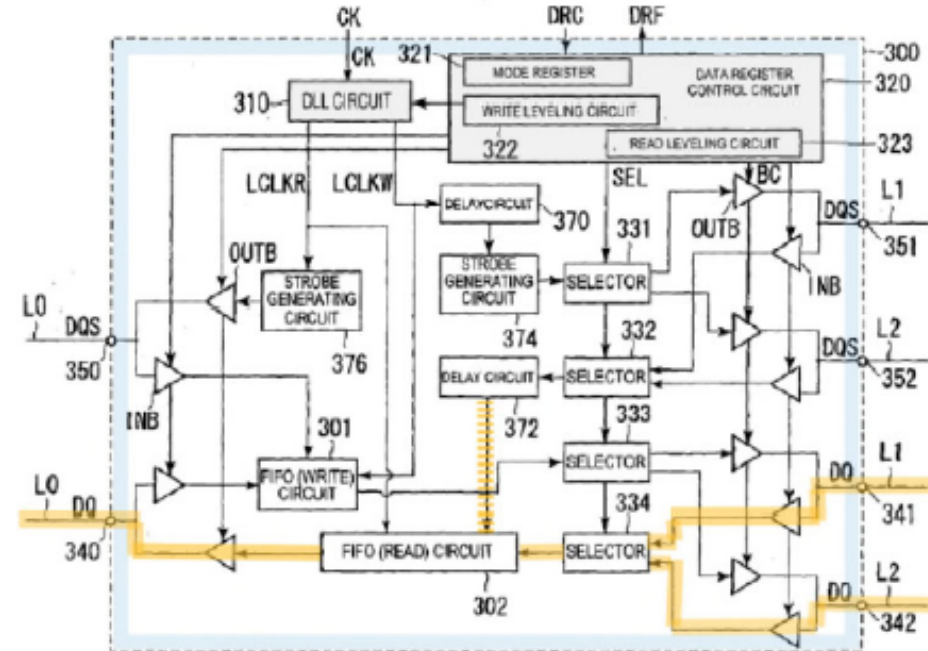


FIG. 5

Samsung's New Unpatentability Theory

For example, as shown above, Hiraishi's Read FIFO 302 is on the DQ data line and delays the DQ data signal, thus satisfying even Netlist's unreasonably narrow construction of "data path" and "delay circuit." Pet. 48-53; EX1005, [0130] ("re-timing...using the FIFO (Read) circuit 302"). The same is true in the write direction. Pet. 39-47; EX1005, [0135] ("re-timing...using the FIFO (Write) circuit 301").

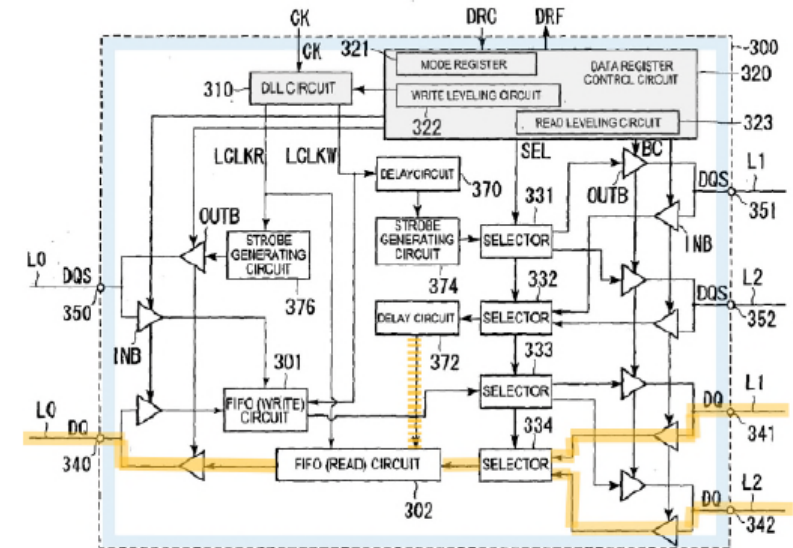


FIG. 5

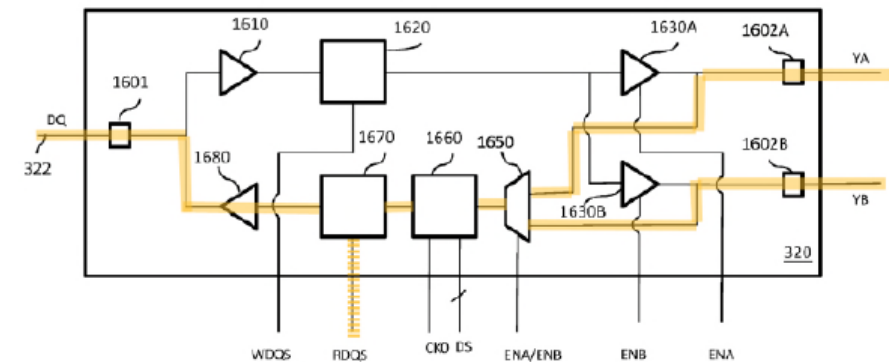


FIG. 16

EX1005, Hiraishi, FIGs. 5 and 16 (annotated).

Samsung's New Theory Fails

Hiraishi's FIFO circuit does not teach claim 1's “delay circuit” for at least three reasons:

1. Hiraishi's FIFOs do not operate in response to a “module control signal”; their output is timed by local clock signals derived from the clock signal received from command/address/control buffer 400 (which Petitioner maps to the claimed “module *clock* signal”).
2. Hiraishi's S4 operations (which Petitioner alleges determines the “amount” of delay in claim 1) are not performed based on a “system command signal.”
3. Using Butt to interpret Hiraishi (as Petitioner proposes), Hiraishi's local clock signals are free running clock signals; they are not the claimed “module control signals.”

Hiraishi FIFOs Do Not Operate in Response to a “module control signal”

FIFO’s output is timed by local clock signals derived from the clock signal received from command/address/control buffer 400, which Petitioner maps to the claimed “module clock signal”

[0087] An output operation timing of the FIFO (Write) circuit 301 is defined by the internal clock LCLKW that is generated by the DLL circuit 310. An output operation timing of the FIFO (Read) circuit 302 is defined by the internal clock LCLKR that is generated by the DLL circuit 310. The DLL circuit 310 is a circuit that generates the internal clocks LCLKW and LCLKR based on the clock signal CK that is supplied from the command/address/control register buffer 400, having the same circuit configuration and function as that of the DLL circuit 212 provided in the memory chip 200.

EX1005, Hiraishi, ¶ 87.

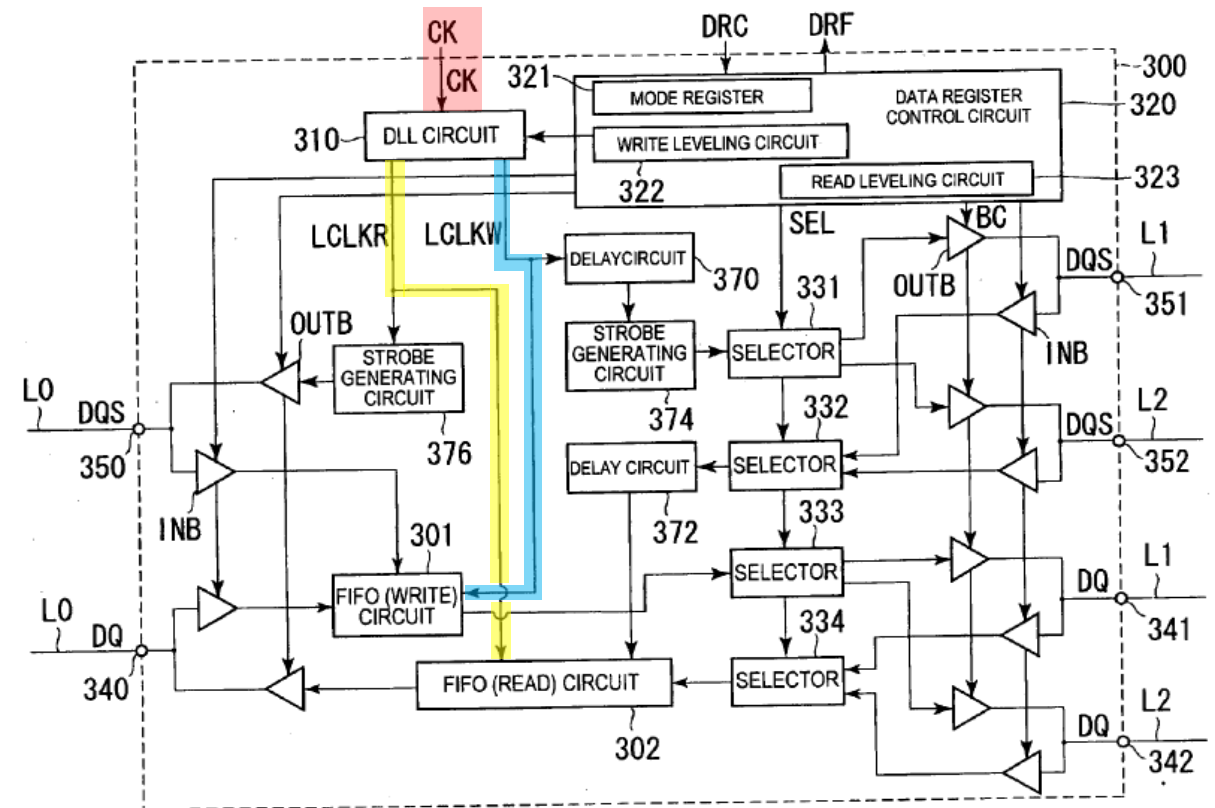


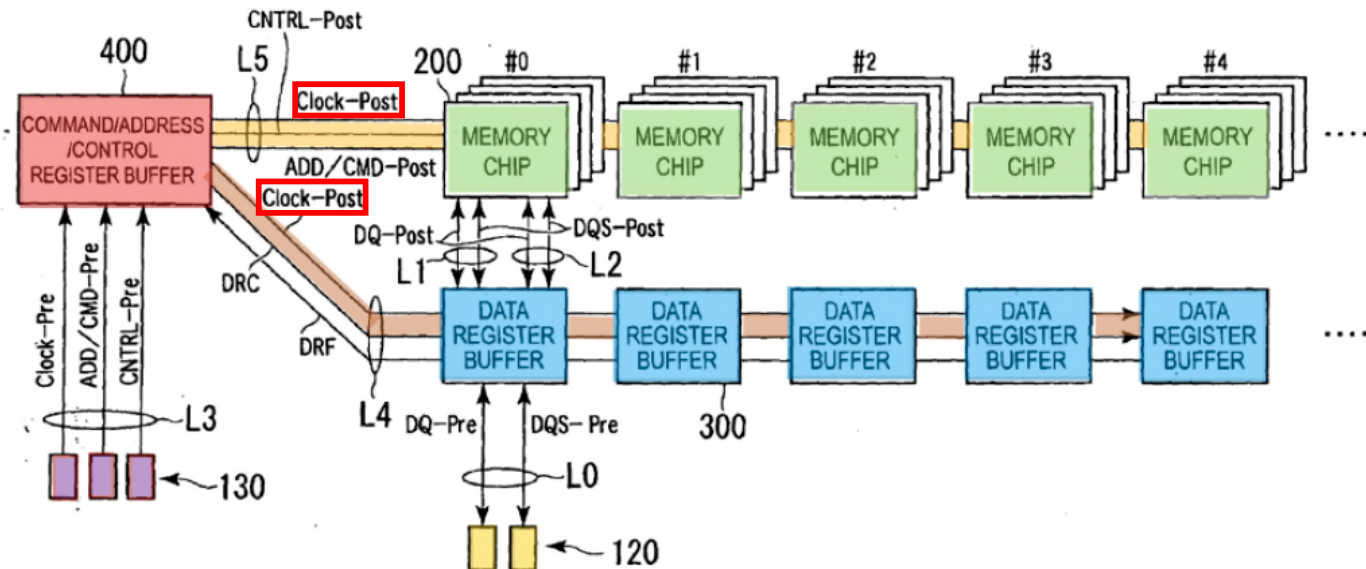
FIG.5

EX1005, Hiraishi, FIG. 5 (annotated).

Hiraishi FIFOs Do Not Operate in Response to a “module control signal”

FIFO's output is timed by local clock signals derived from the clock signal received from command/address/control buffer 400, **which Petitioner maps to the claimed “module clock signal”**

[received on command/address/control connectors 130 (Fig.7, purple)], *the module control device being further configured to receive a system clock signal [Clock-Pre in L3] and output a **module clock signal [Clock-Post in L4 and L5].***



Hiraishi's S4 Leveling is Not Performed Based on a "system command signal"

1. A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising:

a module board having edge connections for coupling to respective signal lines in the memory bus;

a module control device mounted on the module board and configured to receive system command signals for memory operations via the set of control/address signal lines and to output module command signals and module control signals in response to the system command signals, the module control device being further configured to receive a system clock signal and output a module clock signal; and

memory devices including a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data/strobe signal lines; and a plurality of buffer circuits corresponding to respective sets of the plurality of sets of data/strobe signal lines, wherein each respective buffer circuit of the plurality of buffer circuits is mounted on the module board, coupled between a respective set of data/strobe signal lines and a respective set of memory devices, and configured to receive the module control signals and the module clock signal, the each respective buffer circuit including a data path corresponding to each data signal line in the respective set of data/strobe signal lines, and a command processing circuit configured to decode the module control signals and to control the data path in accordance with the module control signals and the

circuit and a delay circuit configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals.

No "system command signal" in S4 leveling

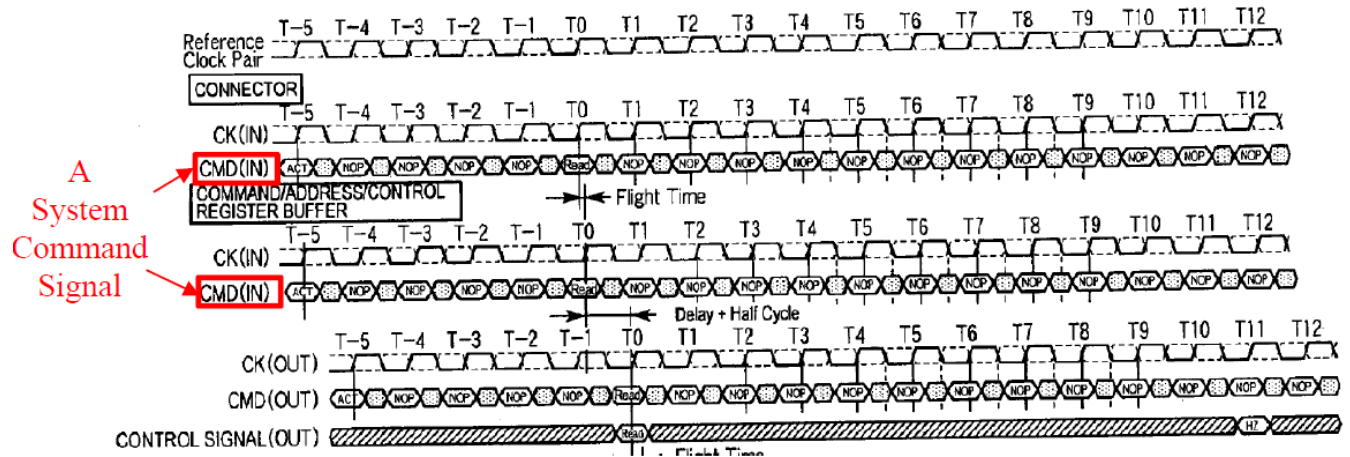


FIG. 11 (Partial) – Read Operation

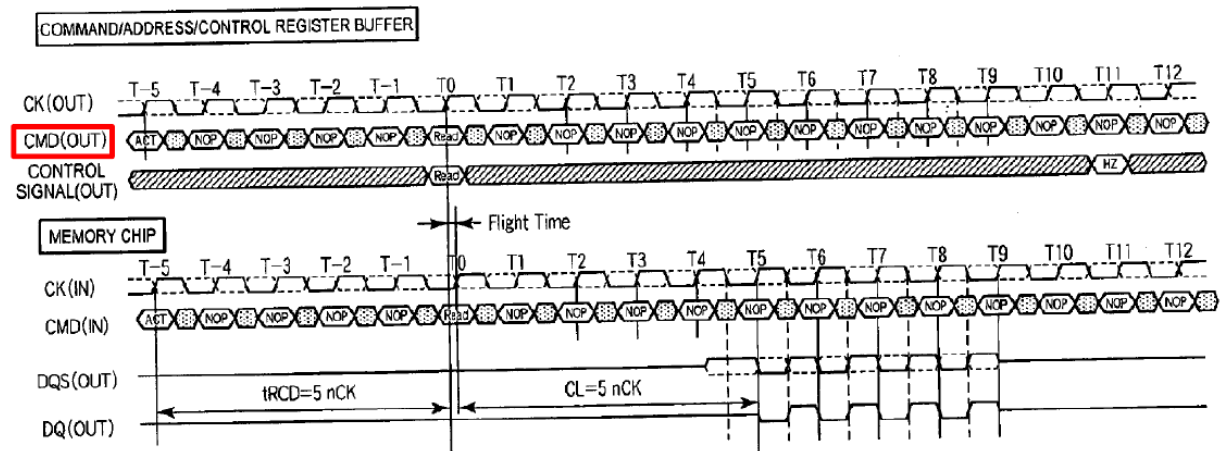


FIG. 15 (Partial) – Read Leveling

Hiraishi's Local Clock Signals are Free Running Clock Signals

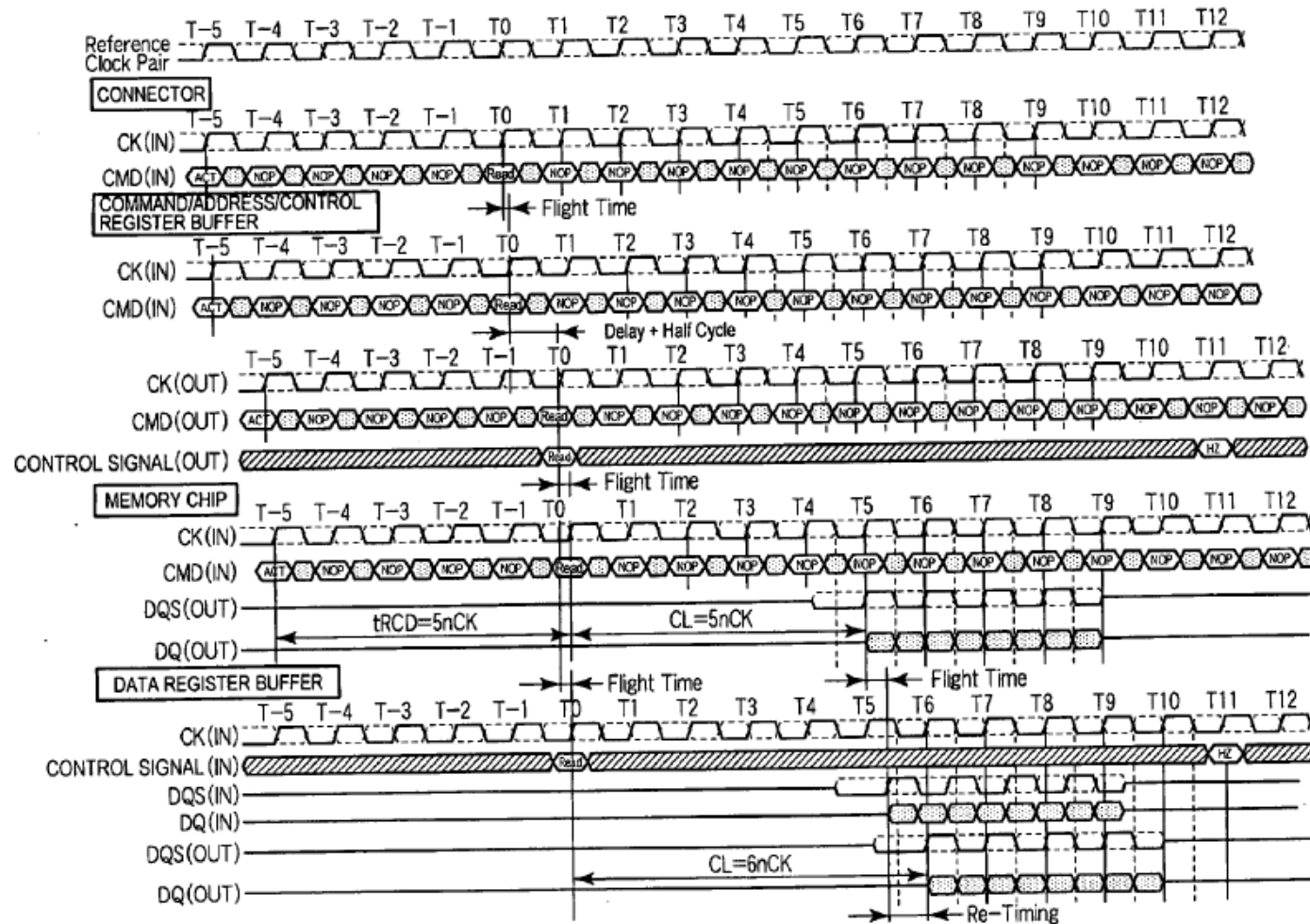


FIG.11

Ground 1:

Hiraishi and Butt do not teach determining “an amount” to delay a “signal through the data path”

Hiraishi's S4 Operations and Re-timing

Hiraishi's re-timing is not based on Hiraishi's S4 leveling, and neither the re-timing nor the S4 leveling independently satisfies element 1[f]

circuit and a delay circuit configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals.

How it works	Why it fails to satisfy Element 1[f]
S4 write leveling adjusts the timing of the strobe signal (DQS) to align with the clock	S4 write leveling does not cause a “delay circuit” to “delay a signal through the data path”
S4 read leveling adjusts the activation timing of Hiraishi's input buffers (which Petitioner maps to the claimed tristate buffers)	S4 read leveling does not cause a “delay circuit” to “delay a signal through the data path”
Re-timing addresses flight delays for write and read operations by simply resetting the internal latency to the next clock cycle	No delay “amount” is “determined by the command processing circuit” during re-timing

Hiraishi's S4 Write Leveling

S4 write leveling adjusts the timing of DQS to align with the clock → it does not cause a “delay circuit” to “delay a signal through the data path”

supplied to the memory chip 200 as described above. Because it takes a certain amount of propagation time until the data strobe signal DQS reaches the memory chip 200, input timings of the clock signal CK and the data strobe signal DQS are not always the same on the memory chip 200 side.

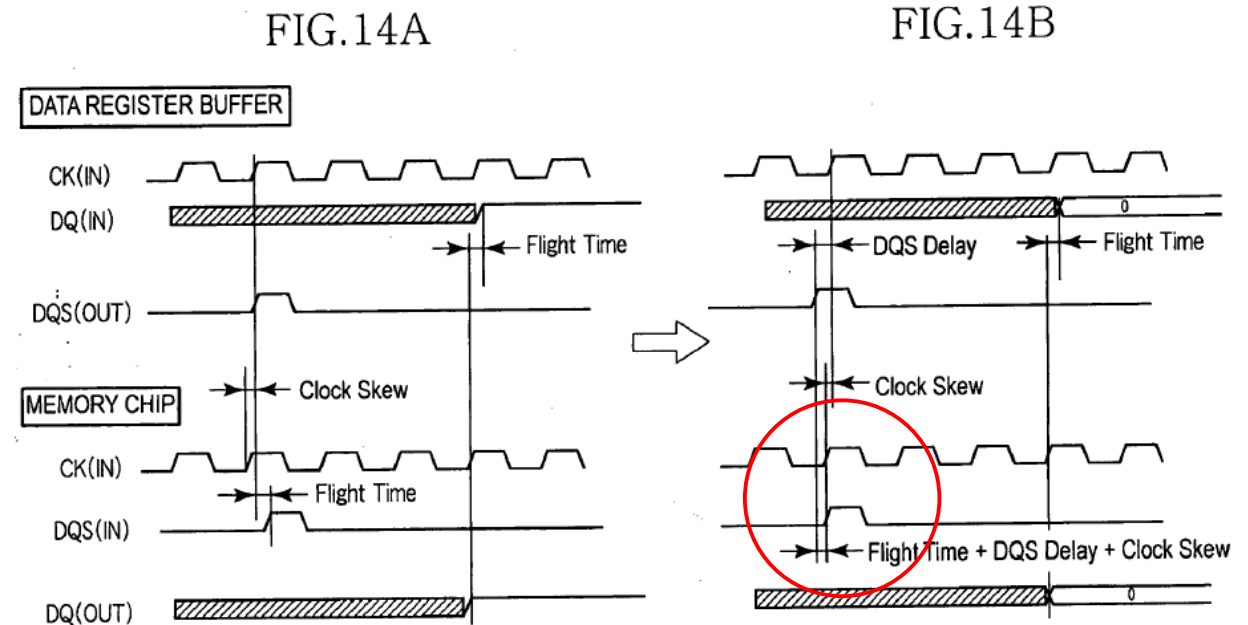
EX1005, Hiraishi, ¶ 143.

[0145] The write leveling circuit 322 of the data register buffer 300 changes an output timing of the data strobe signal DQS by displacing the internal clock LCLKW based on the direction of the phase shift. In the example shown in FIG.

EX1005, Hiraishi, ¶ 145.

register buffer 300. Upon completing the write leveling operation in this manner, the phases of the clock signal CK and the data strobe signal DQS input to the memory chip 200 are substantially matched with each other.

EX1005, Hiraishi, ¶ 146.



EX1005, Hiraishi, FIGs. 14A-14B (annotated).

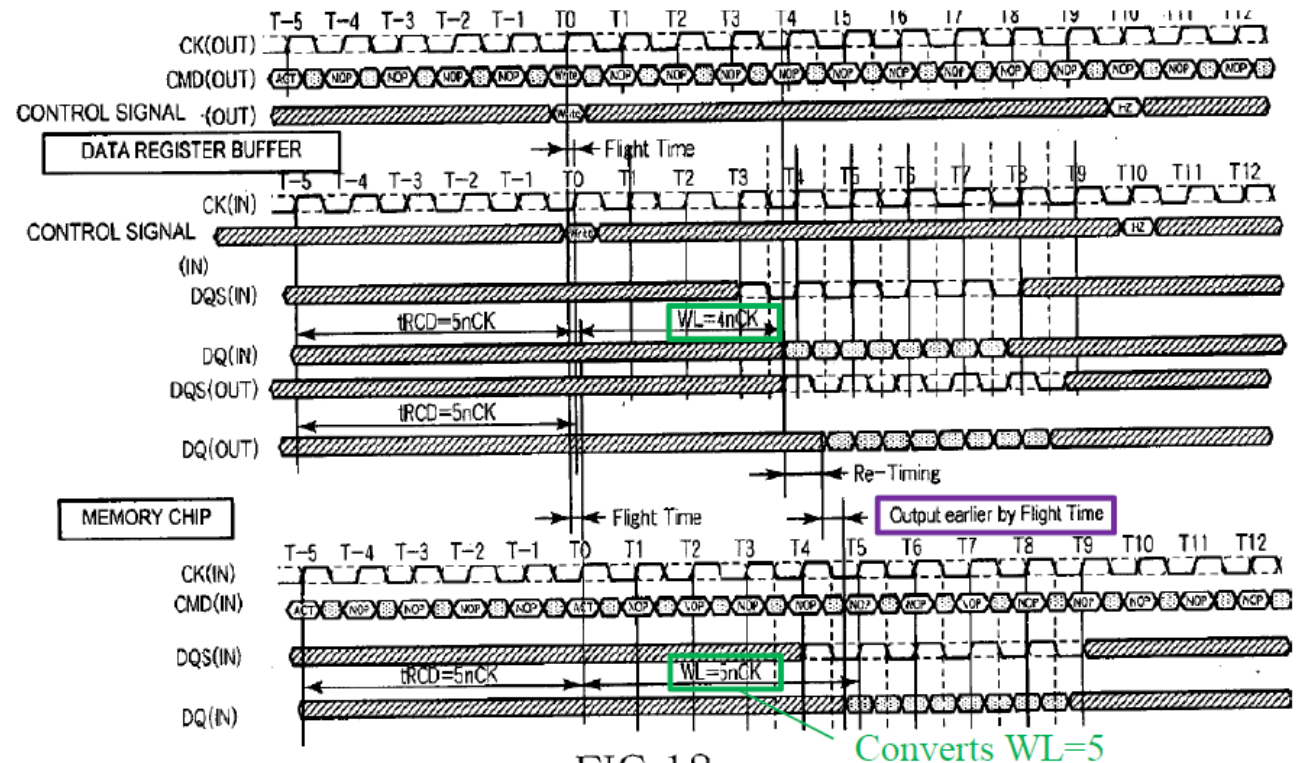
Hiraishi's WL Re-timing (Write Operations)

Hiraishi's WL re-timing addresses flight delays for write operations by simply resetting the internal latency to the next clock cycle → No delay “amount” is “determined by the command processing circuit” during re-timing

[0135] The data register buffer 300 loads the received write data DQ in the FIFO (Write) circuit 301 with a data strobe signal DQS that is delayed by a predetermined phase amount (for example, phase difference of about 90 degrees). The data register buffer 300 then performs a re-timing in synchronization with the internal clock LCLKW using the FIFO (Write) circuit 301 to convert WL into WL=5, and outputs the write data DQ and the data strobe signal DQS. As described above, the write data is transferred from the data register buffer 300 to the memory chip 200 using either one of the two data lines L1 and L2. The data line to be used is determined by a designated Rank.

[0136] The memory chip 200 receives the write data DQ that is burst output from the data register buffer 300, and writes it in the memory cell array. At this time, there occurs a predetermined time difference (Flight Time) between a timing at which the write data DQ and the data strobe signal DQS are output from the data register buffer 300 and a timing at which the write data DQ and the data strobe signal DQS are input to the memory chip 200. In consideration of this point, the data register buffer 300 outputs the write data DQ earlier by an amount equivalent to the Flight Time. With this configuration, it becomes possible for the memory chip 200 to receive the write data DQ in a correct manner.

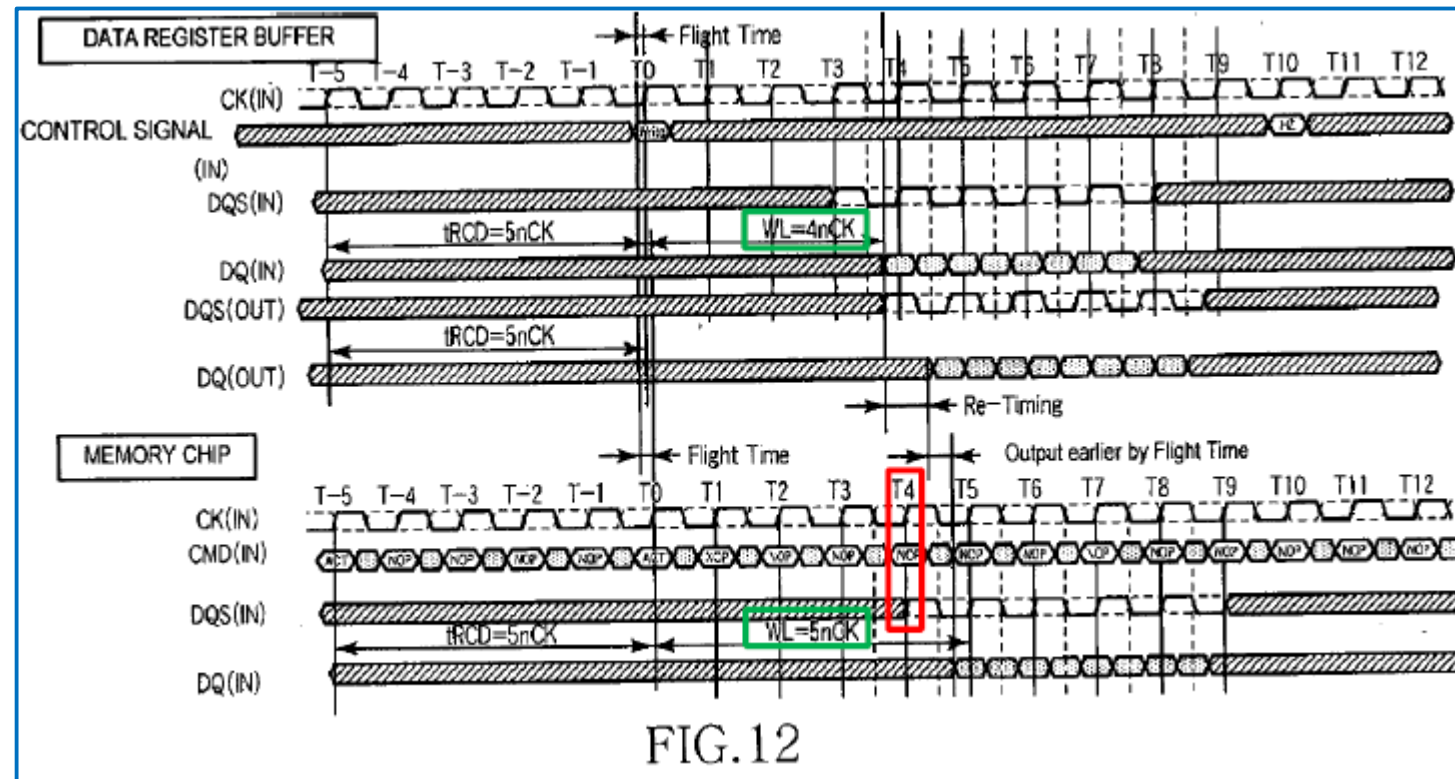
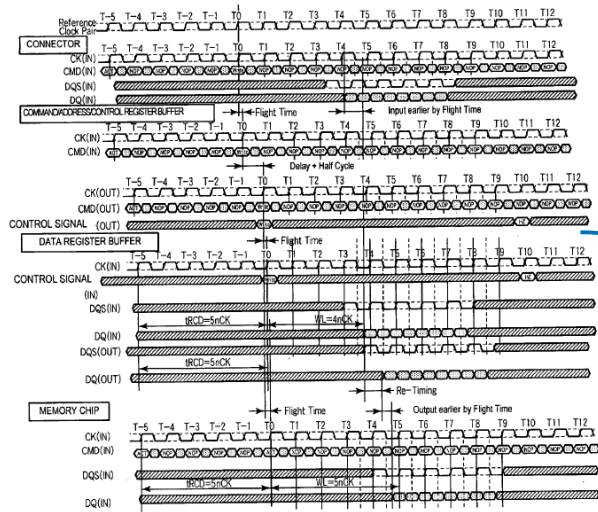
EX1005, Hiraishi, ¶¶ 135-136.



EX1005, Hiraishi, FIG. 12 (annotated).

Hiraishi's WL re-timing is not based on S4 write leveling

S4 write leveling aligns CK(IN) and DQS(IN) to memory chip (red)
WL re-timing resetting the internal latency to the next clock cycle (green)



EX1005, Hiraishi, FIG. 12 (annotated).

Hiraishi's S4 Read Leveling

S4 read leveling adjusts the activation timing of Hiraishi's input buffers → it does not cause a “delay circuit” to “delay a signal through the data path”

[0151] The read data DQ output from the memory chip 200 reaches the data register buffer 300, by which the data register buffer 300 can find a time A from an input timing of the read command Read that is input as a part of the control signal DRC until the read data DQ is input. The time is measured for each of the memory chips 200, stored in the data register control circuit 320 in the data register buffer 300, and used in an adjustment of an activation timing of the input buffer circuit INB and the like. In FIG. 15, two cases are shown including a first case that the time A from the input of the read command Read until the input of the read data DQ is short (between the memory chip 200-0 and the data register buffer 300-0) and a second case that the time A is long (between the memory chip 200-19 and the data register buffer 300-4).

EX1005, Hiraishi, ¶ 151.

23	Q. And so those tristate buffers, those OUTB and
24	INB buffers, are those part of the delay circuit as well?
25	A. No, they're not.

EX2012, Wedig Dep. Tr., 31:23-25.

Hiraishi's CL Re-timing (Read Operations)

CL re-timing addresses flight delays for read operations by simply resetting the internal latency to the next clock cycle → No delay “amount” is “determined by the command processing circuit” during re-timing

[0128] Because CL=5 in the example shown in FIG. 11, the memory chip 200 starts a burst output of read data DQ at a time T5 in five clock cycles after receiving the read command Read. In the example shown in FIG. 11, the burst length is 8 bits (BL=8). The read data DQ and a data strobe signal DQS burst output from the memory chip 200 are supplied to the data register buffer 300.

[0129] The data register buffer 300 loads the read data DQ that is output from the memory chip 200 in the FIFO (Read) circuit 302 with a data strobe signal DQS that is delayed by a predetermined phase amount (for example, phase difference of about 90 degrees). At this moment, there occurs a predetermined time difference (Flight Time) between a timing at which the read data DQ and the data strobe signal DQS are output from the memory chip 200 and a timing at which the read data DQ and the data strobe signal DQS are input to the data register buffer 300.

[0130] Thereafter, the data register buffer 300 performs a re-timing in synchronization with the internal clock LCLKR using the FIFO (Read) circuit 302 to convert CL into CL=6, and outputs the read data DQ and the data strobe signal DQS. With this configuration, it becomes possible for the memory controller to receive the read data DQ in a correct manner.

EX1005, Hiraishi, ¶¶ 128-130.

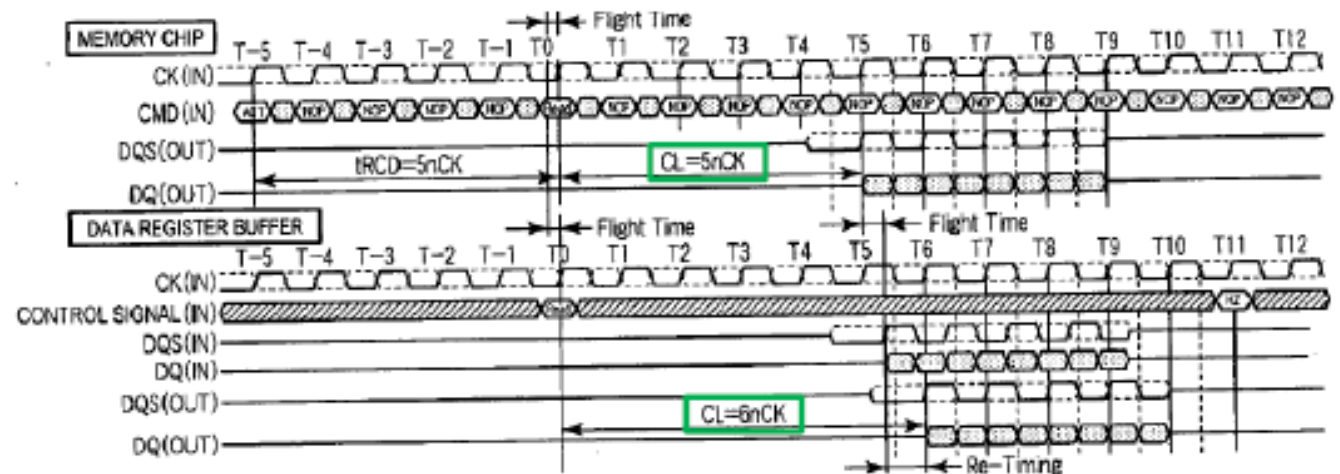


FIG. 11

EX1005, FIG. 11 (partially reproduced and annotated); EX2013, ¶139.

Hiraishi's CL re-timing is not based on S4 Read leveling

**S4 read leveling adjusts the activation timing of Hiraishi's input buffers (red);
CL re-timing resetting the internal latency to the next clock cycle (green)**

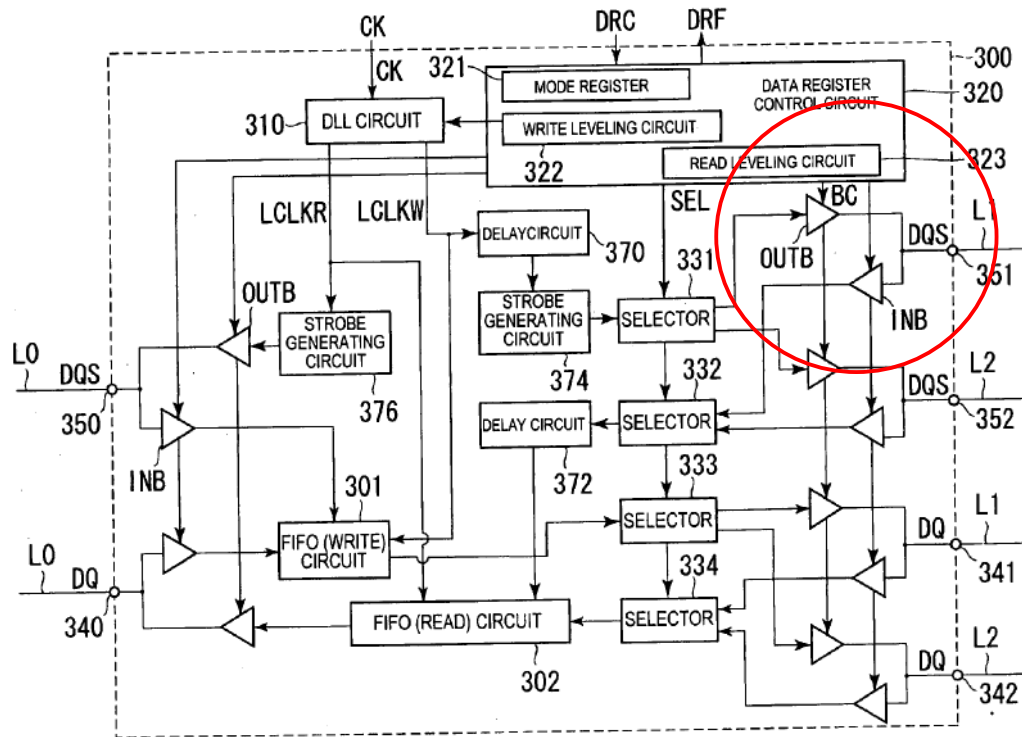


FIG.5

EX1005, Hiraishi, FIG. 5 (annotated).

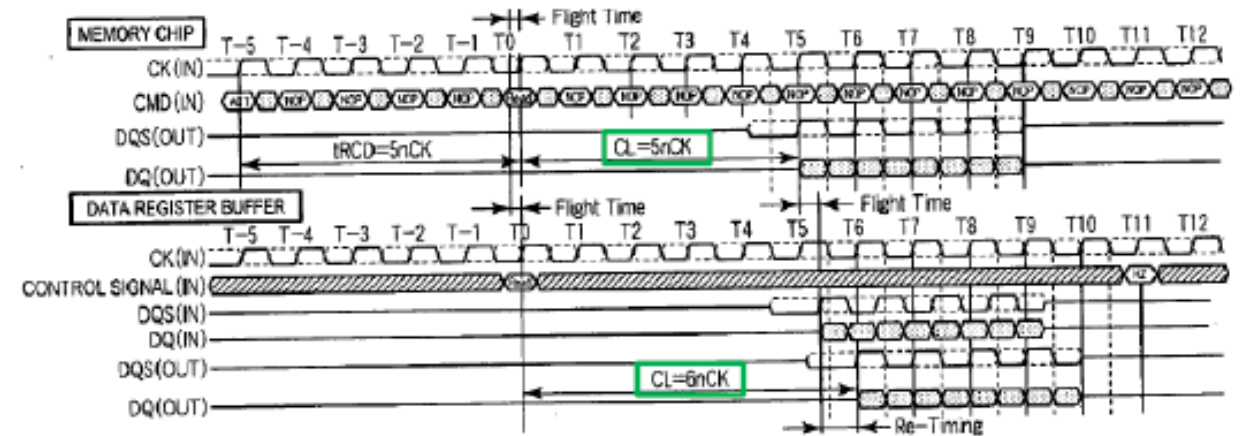


FIG.11

EX1005, FIG. 11 (partially reproduced and annotated); EX2013, ¶139.

Ground 2:
Hiraishi, Butt, and Tokuhiro do not render obvious claim 1's
“delay circuit”

Proposed Hiraishi-Tokuhiro combination does not teach a “delay circuit” in the “data path”



The block diagram illustrates a memory controller 300. It features a central processing unit containing a Mode Register, Write Leveling Circuit, Read Leveling Circuit, and Data Register Control Circuit. This unit is connected to a DLL Circuit (310) and a Delay Circuit (370). The controller also includes a Strobe Generating Circuit (376) and a Selector (331). Data paths are managed by FIFO (Write) and FIFO (Read) Circuits (301, 302). The system is interfaced with a memory array (340) through DQS and DQ signals, with L1 and L2 memory banks indicated. Control signals include CK, DRC, DRF, LCLKR, LCLKW, OUTB, INB, and DQS. Data signals include DQ, DQ0, and DQ1.

FIG.5

41

Ground 2:
A POSITA would not have combined Hiraishi, Butt, and
Tokuhiro as proposed

Samsung's Theory: FIFO Clocked Out by Strobe Signal

Q. Okay. Is the unlabeled line that comes out of the bottom of strobe-generating circuit 376 a delayed version of the LCLKR signal that's being provided by the DLL circuit to the strobe-generating circuit 376?

A. Not exactly. Can I explain what it is?

Q. Please.

A. What it is is the same -- it's essentially the same as what comes out to the left of the box from 376. It is a -- it's a signal that took LCLKR as input to help provide the activation timing, but then it has generated a strobe -- it generated a strobe signal. It delayed it, and then that is the signal that then goes down to the FIFO. So I could have shown it as attaching to the left side and coming over and coming down because it's the same signal.

Q. I see. That was not clear to me originally.

So just for the record so it's clear, the strobe-generating circuit 376 --

A. Uh-huh.

Q. -- is generating a strobe; correct? And that strobe is being then delayed by DR-1?

A. Uh-huh.

Q. And then that delayed strobe is being output in two places, one where the crosshatch orange goes out to 350 --

A. Uh-huh.

Q. -- and second, down to CLK the data out of the FIFO read circuit 302?

A. That's correct.

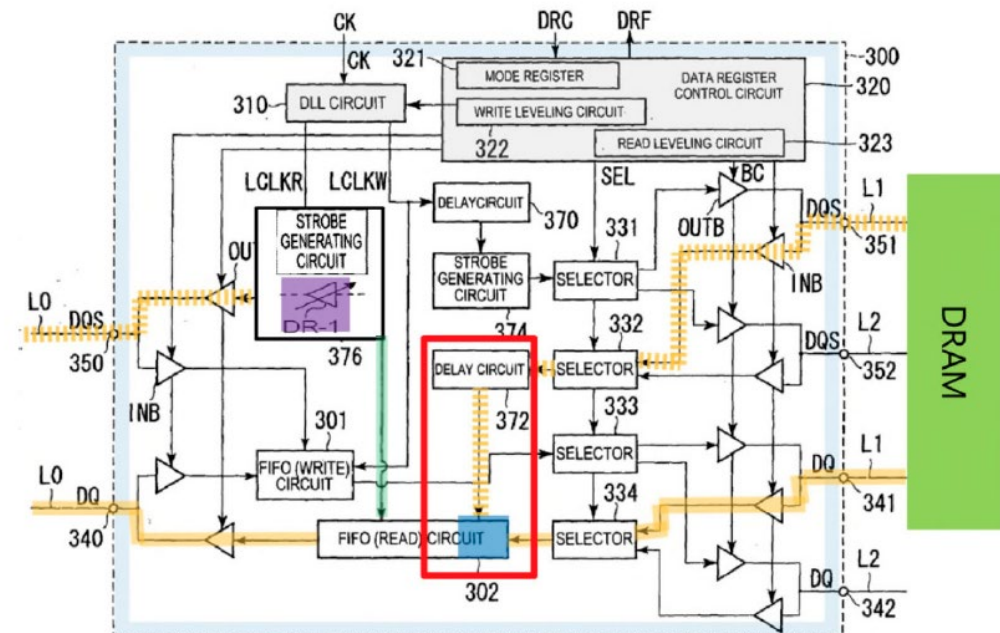


FIG.5 EX1005, Hiraishi, FIG. 5 (annotated).

EX2012, Wedig Dep. Tr., 90:15-91:18.

Samsung's Theory is Contrary to Hiraishi's and Tokhiro's Teachings

Hiraishi teaches the FIFO 302 is clocked out by LCLKR

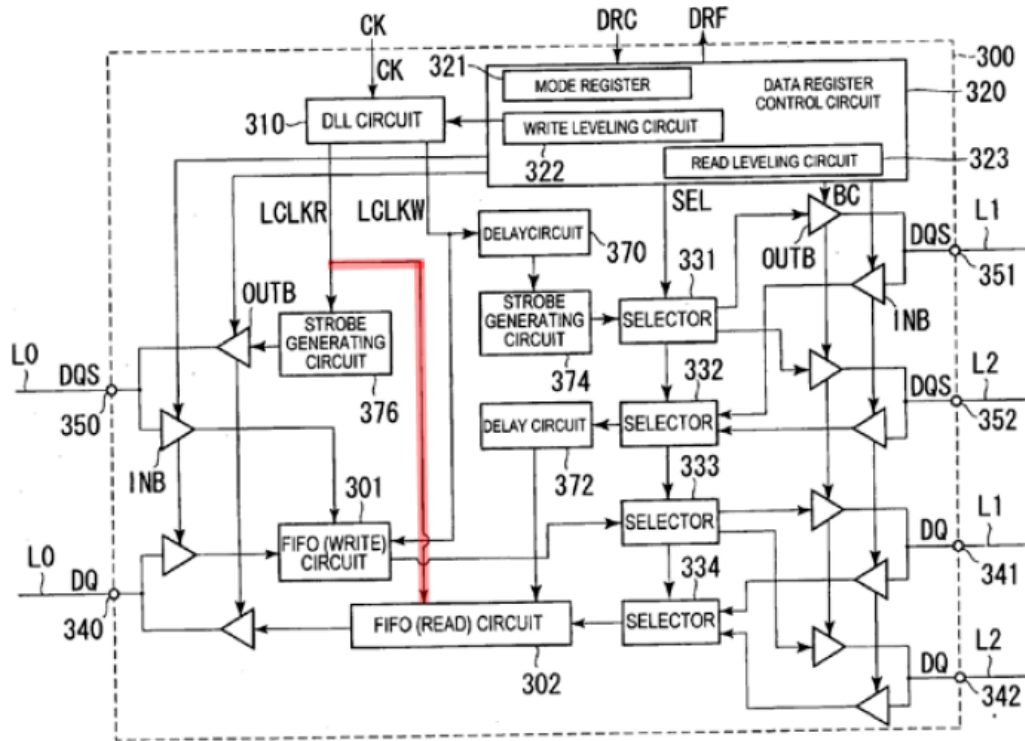


FIG. 5

generated by the DLL circuit 310. An output operation timing of the FIFO (Read) circuit 302 is defined by the internal clock LCLKR that is generated by the DLL circuit 310. The DLL

EX1005, Hiraishi, ¶ 87.

In Samsung's theory, FIFO 302 is clocked out by a strobe signal and FIFO 302 receives two strobe signals

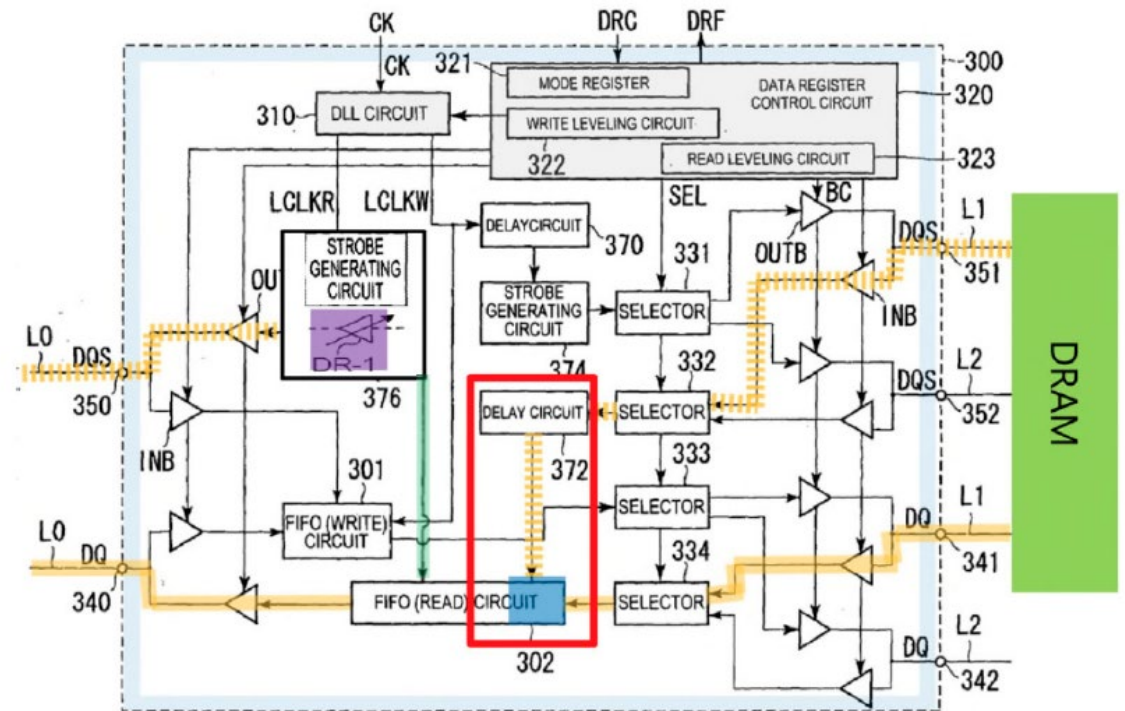
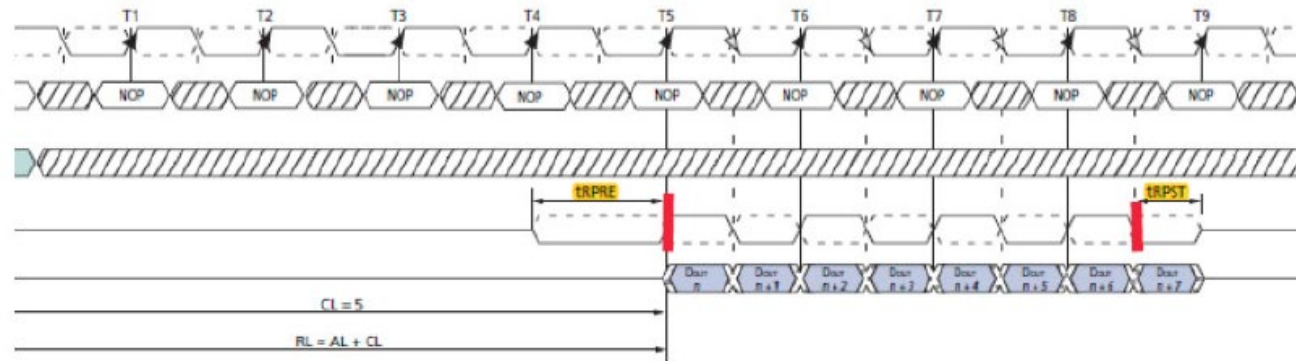


FIG. 5

EX1005, Hiraishi, FIG. 5 (annotated).

Cannot Clock Out FIFO Using Strobe Signal



BL8, RL = 5, AL = 0, CL = 5.

Dout n = data-out from column n .

NOP commands are shown for ease of illustration; other commands may be valid at these times.

BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ command at T0.

TRANSITIONING DATA

Figure 25 — READ Burst Operation RL = 5 (AL = 0, CL = 5, BL8)

EX1020, JEDEC Standard, 56 (annotated).

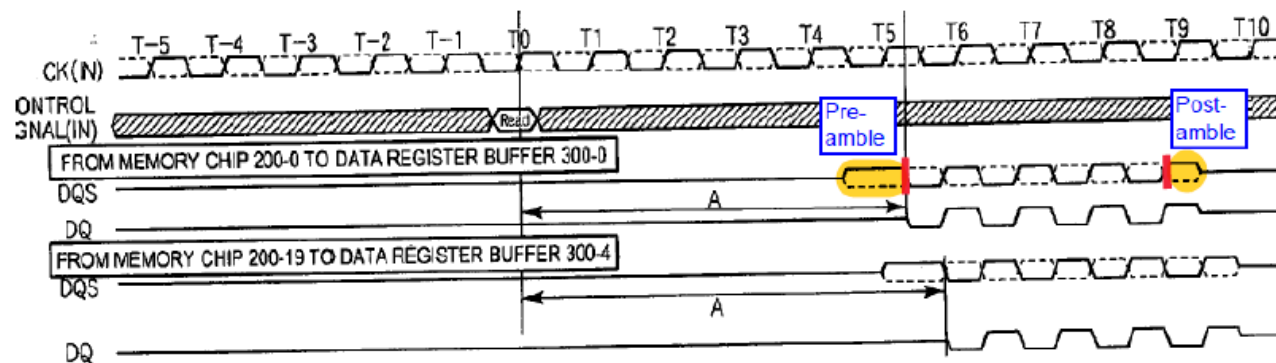


FIG.15

EX1005, Hiraishi, FIG. 15 (annotated).