

- [47] J. Arnold and W. Kleinfelder. *Splash 2: FPGAs in a Custom Computing Machine*. IEEE Computer Society, 1996. 25
- [48] K. Nakajima, H. Sato, H. Asami, M. Iida, K. Shindome, H. Mori, K. Takahashi, and Y. Mizukami. FPGA-based Parallel Machine : RASH. In *Proceedings of the 20th International Conference on Applied Informatics (AI2002)*, pages 269–273, February 2002. 25
- [49] R. Amerson, R. J. Carter, W. B. Culbertson, P. Kuekes, and G. Snider. Teramac – Configurable Custom Computing. In *Proceedings of the 3rd IEEE Workshop on FPGAs for Custom Computing Machines (FCCM1995)*, pages 32–38, April 1995. 25
- [50] T. J. Callahan, J. R. Hauser, and J. Wawrzyniek. The Garp Architecture and C Compiler. *IEEE Computer*, 33(4):62–69, April 2000. 26
- [51] C. R. Rupp, M. Landguth, T. Garverick, E. Gomersall, H. Holt, J. M. Arnold, and M. Gokhale. The NAPA Adaptive Processing Architecture. In *Proceedings 6th IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM1998)*, pages 28–37, April 1998. 26
- [52] P. M. Athanas and H. F. Silverman. Processor Reconfiguration Through Instruction-Set Metamorphosis. *IEEE Computer*, 26(3):11–18, March 1993. 26
- [53] M. Wazlowski, L. Agarwal, T. Lee, A. Smith, E. Lam, P. Athanas, H. Silverman, , and S. Ghosh. PRISM-II Compiler and Architecture. In *Proceedings of the 1st IEEE Workshop on FPGAs for Custom Computing Machines (FCCM1993)*, pages 9–16, April 1993. 26
- [54] F. Raimbault, D. Lavenier, S. Rubini, and B. Pottier. Fine Grain Parallelism on a MIMD Machine Using FPGAs. In *Proceedings of the 1st IEEE Workshop on FPGAs for Custom Computing Machines (FCCM1993)*, pages 2–8, April 1993. 26
- [55] R. Razdan and M. Smith. A High Performance Microarchitecture with Hardware Programmable Functional Units. In *Proceedings of the Annual International Symposium on Microarchitecture (MICRO-27)*, pages 172–180, 1994. 26
- [56] R. Witting and P. Chow. OneChip: An FPGA Processor with Reconfigurable Logic. In *Proceedings of the 4th IEEE Symposium on FPGAs for Custom Computing Machines (FCCM1996)*, pages 126–135, 1996. 26
- [57] S. Hauck, T. Fry, M. Hosler, and J. Kao. The Chimaera Reconfigurable Functional Unit. In *Proceedings of the 5th IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM1997)*, pages 87–96, April 1997. 26
- [58] Z. Ye, A. Moshovos, S. Hauck, and P. Banerjee. CHIMAERA: A High-Performance Architecture with a Tightly-Coupled Reconfigurable Functional Unit. In *Proceedings of the International Symposium on Computer Architecture (ISCA2000)*, pages 225–235, 2000. 26
- [59] T. Toi, N. Nakamura, Y. Kato, T. Awashima, K. Wakabayashi, and L. Jing. High-level Synthesis Challenges and Solutions for a Dynamically Reconfigurable Processor. In *Proceedings of the 2006 IEEE/ACM International Conference on Computer-Aided Design (ICCAD2006)*, pages 702–708, November 2006. 26, 31, 55, 79
- [60] K. Wakabayashi and T. Okamoto. C-Based SoC Design Flow and EDA Tools: An ASIC and System Vendor Perspective. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 19(12):1507–1522, December 2000. 26

- [61] B. Salefski and L. Caglar. Re-Configurable Computing in Wireless. In *Proceedings of the 38th Design Automation Conference (DAC2001)*, pages 178–183, June 2001. 27, 48
- [62] PACT Inc. *Video Decoding on XPP-III*, revision 1.1 edition, July 2006. 30
- [63] M. Motomura. A Dynamically Reconfigurable Processor Architecture. In *Proceedings of Microprocessor Forum*, October 2002. 30, 48, 50, 53, 87, 88
- [64] T. Sugawara, K. Ide, and T. Sato. Dynamically Reconfigurable Processor Implemented with IPFlex's DAPDNA Technology. *IEICE Transactions on Information & System*, E87-D(8):1997–2003, August 2004. 32, 48
- [65] T. Sato. Dynamic Reconfiguration and Its Granularity inside Future DAPDNA Architecture. In *Proceedings of International Symposium on Advanced Reconfigurable Systems*, pages 114–127, December 2005. 34
- [66] T. Sato. A Dual-Core Dynamically Reconfigurable Engine Employs 955 Parallel Processing Elements. In *Proceedings of Microprocessor Forum*, May 2007. 34, 48
- [67] T. Komada, T. Tsunoda, M. Takeda, H. Tanaka, Y. Akita, M. Sato, and M. Ito. Flexible Engine: A Dynamic Reconfigurable Accelerator with High Performance and Low Power Consumption. In *Proceedings of the 9th IEEE Symposium on Low-Power and High Speed Chips (COOL Chips IX)*, pages 393–408, April 2006. 34, 48, 88
- [68] T. Stansfield. Using Multiplexers for Control and Data in D-Fabrix. In *Proceedings of the 13th International Conference on Field Programmable Logic and Applications (FPL'03)*, pages 416–425, August 2003. 36, 48
- [69] A. Marshall, T. Stansfield, I. Kostarnov, J. Vuillemin, and B. Hutchings. A Reconfigurable Arithmetic Array for Multimedia Applications. In *Proceedings of the ACM/SIGDA 7th International Symposium on Field-Programmable Gate Arrays (FPGA1999)*, pages 135–143, February 1999. 36
- [70] T. Matsumoto, K. Kimura, H. Takano, T. Amatsubo, K. Mori, K. Senda, S. Inoue, and M. Matsui. Performance Evaluation of Reconfigurable Processing Array in Area Efficiency and Operating Frequency. In *Proceedings of the 9th IEEE Symposium on Low-Power and High Speed Chips (COOL Chips IX)*, pages 423–434, April 2006. 37
- [71] T. Kiyohara. Multimedia Processor-based Platform for a Wide Range of Digital Consumer Electronics. In *Proceedings of the 8th IEEE Symposium on Low-Power and High Speed Chips (COOL Chips XIII)*, pages 133–141, April 2005. 37
- [72] M. Nakajima, T. Yamamoto, M. Yamasaki, T. Hosoki, and M. Sumital. Low Power Techniques for Mobile Application SoCs Based on Integrated Platform UniPhier. In *Proceedings of the 12th Asia and South Pacific Design Automation Conference (ASPDAC2007)*, pages 649–653, January 2007. 37
- [73] B. Levine. Kilocore: Scalable, High-Performance, and Power Efficient Coarse-grained Reconfigurable Fabrics. In *Proceedings of International Symposium on Advanced Reconfigurable Systems*, pages 129–158, December 2005. 38, 48
- [74] H. Schmit, D. Whelihan, A. Tsai, M. Moe, B. Levine, and R. R. Taylor. PipeRench: A Virtualized Programmable Datapath in 0.18 Micron Technology. In *Proceedings of the 24th IEEE Custom Integrated Circuits Conference (CICC2002)*, pages 63–66, May 2002. 38

- [75] F. Veredas, M. Scheppler, W. Moffat, and B. Mei. Custom Implementation of the Coarse-Grained Reconfigurable ADRES Architecture for Multimedia Purposes. In *Proceedings of International Conference on Field Programmable Logic and Application (FPL'05)*, pages 106–111, August 2005. 39, 48, 53
- [76] Stretch Inc. http://www.stretchinc.com/_files/s6ArchitectureOverview.pdf. 41, 48
- [77] J. Arnold. S5: The Architecture and Development Flow of a Software Configurable Processor. In *Proceedings of the 4th IEEE International Conference on Field Programmable Technology (FPT2005)*, pages 120–128, December 2005. 42
- [78] M. Saito, H. Fujisawa, N. Ujiie, and H. Yoshizawa. Cluster Architecture for Reconfigurable Signal Processing Engine for Wireless Communication. In *Proceedings of the International Conference on Field Programmable Logic and Applications (FPL'05)*, pages 353–359, August 2005. 43, 48
- [79] H. Amano, Y. Hasegawa, S. Tsutsumi, T. Nakamura, T. Nishimura, V. Tanbunheng, A. Parimala, T. Sano, , and M. Kato. MuCCRA chips: Configurable dynamically-reconfigurable processors. In *Proceedings of Solid-State Circuits Conference (ASSCC'07)*, pages 384–387, November 2007. 44, 45, 48, 59
- [80] Y. Saito, M. Kato, S. Saito, T. Sano, Hirai K, T. Nishimura, T. Nakamura, S. Tsutsumi, Y. Hasegawa, and H. Amano. Practice Evaluation Dynamically Reconfigurable Processor MuCCRA-2. In *IEICE Technical Reports, RECONF2008-34*, pages 69–74, September 2008. (In Japanese). 45, 48
- [81] E. Ahmed and J. Rose. The Effect of LUT and Cluster Size on Deep-Submicron FPGA Performance and Density. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 12, 2004. 48
- [82] Y.Hasegawa, S.Abe, S.Kurotaki, V.Tuan, N.Katsura, T.Nakamura, T.Nishimura, and H.Amano. Performance and Power Analysis of Time-multiplexed Execution on Dynamically Reconfigurable Processor. In *Proceedings of the 20th International Parallel and Distributed Processing Symposium/ Reconfigurable Architecture Workshop (IPDPS2006)*, April 2006. 50, 63, 64, 88
- [83] Edward A. Lee and David G. Messerschmitt. Synchronous data flow. *Proceedings of IEEE*, 75(9):1235–1245, September 1987. 51
- [84] Edward A. Lee and Thomas M. Parks. Dataflow process networks. *Proceedings of IEEE*, 83(5):773–799, May 1995. 51
- [85] Gilles Kahn. The semantics of a simple language for parallel programming. In *Proceedings of the IFIP Congress 74*, pages 471–475. North-Holland Publishing Co., August 1974. 51
- [86] Joseph Buck, Soonhoi Ha, Edward A. Lee, and David G. Messerschmitt. Ptolemy: A framework for simulating and prototyping heterogeneous systems. *International Journal in Computer Simulation, special issue on "Simulation Software Development"*, 4(2):155–182, April 1994. 51
- [87] Ralf Niemann. *Hardware/Software co-design for data flow dominated embedded systems*. Kluwer Academic Publishers, 1998. 51
- [88] M.D. Galanis, A. Milidonis, G. Theodoridis, D. Soudris, and C.E. Goutis. A partitioning methodology for accelerating applications in hybrid reconfigurable platforms. In *Proceedings of the conference on Design, Automation and Test in Europe*, volume 3, pages 247–252, March 2005. 51
- [89] K. Bazargan, R. Kastner, and M. Sarrafzadeh. Fast Template Placement for Reconfigurable Computing Systems. *IEEE Design and Test of Computers*, 17(1):68–83, March 2000. 51

- [90] S.P.Fekete, E.Koehler, and J.Tech. Optimal FPGA Module Placement with Temporal Precedence Constraints. In *Proceedings of the conference on Design, Automation and Test in Europe*, pages 658–665, March 2001. 51
- [91] P-H.Yuh, C-L Yang, Y-W. Chang, and H-L Chen. Temporal Floorplanning Using 3D-subTCG. In *Proceedings of the 2004 conference on Asia South Pacific design automation: electronic design and solution fair*, pages 725–730, January 2004. 51
- [92] T. Sugawara, K. Ide, and T. Sato. Dynamically Reconfigurable Processor Implemented with IPFlex’s DAPDNA Technology. *IEICE Transactions on Information & Systems*, E87-D(8):1997–2003, May 2004. 53
- [93] B. Khailany, W.J. Dally, U.J. Kapasi, P. Mattson, J. Namkoong, J.D. Owens, B. Towles, A. Chang, and S. Rixner. Imagine: Media processing with streams. *IEEE Micro*, 21:35–46, March/April 2001. 53
- [94] Independent JPEG Group. <http://www.ijg.org/>. 61, 82
- [95] C. Berrou and A. Glavieux. Near optimum error correcting coding and decoding: Turbo codes. *IEEE Transactions Communications*, 44:1261–1271, October 1996. 61, 82
- [96] MPEG Software Simulation Group (MSSG). <http://www.mpeg.org/MPEG/MSSG>. 61, 82
- [97] J. Noguera and R.M. Badia. Multitasking on reconfigurable architectures:Microarchitecture support and dynamic scheduling. *ACM Transactions on Embedded Computing Systems*, 3(2):385–406, May 2004. 67
- [98] G. Brebner. The Swappable Logic Unit: A Paradigm for Virtual Hardware. In *IEEE Symposium on FPGAs for Custom Computing Machines*, pages 77–86, April 1997. 68
- [99] D. Koch, C. Haubelt, and J. Teich. Efficient hardware checkpointing: concepts, overhead analysis, and implementation. In *Proceedings of International Symposium on Field-Programmable Gate Arrays*, pages 188–196, February 2007. 68
- [100] S. A. Guccione, D. Levi, and P. Sundararajan. JBits: A Java-based interface for reconfigurable computing. In *Proceedings of Second Annual Military and Aerospace Applications of Programmable Devices and Technologies Conference (MAPLD)*, pages 301–302, September 1999. 68
- [101] H. Kalte and M. Porrmann. Context Saving and Restoring for Multitasking in Reconfigurable Systems. In *Proceedings of 15th International Conference on Field-Programmable Logic and Applications*, pages 223–228, August 2005. 68
- [102] S. Jovanovic, C. Tanougast, and S. Weber. A Hardware Preemptive Multitasking Mechanism Based on Scan-path Register Structure for FPGA-based Reconfigurable Systems. In *Proceedings of the Second NASA/ESA Conference on Adaptive Hardware and Systems*, pages 358–364, August 2007. 68
- [103] M. Ullmann, M. Hubner, B. Grimm, and J. Becker. An FPGA run-time system for dynamical on-demand reconfiguration. In *Proceedings of the 18th International Parallel and Distributed Processing Symposium (IPDPS’04) - Reconfigurable Architectures Workshop*, pages 135–142, April 2004. 68, 87, 88
- [104] K. Kim, R. Karri, and M. Potkonjak. Micropreemption Synthesis: An Enabling Mechanism for Multi-task VLSI Systems. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 25:19–30, January 2006. 68

- [105] J. Simonson and J.H. Patel. Use of Preferred Preemption Points in Cache-Based Real-Time Systems. In *Proceedings of 15th International Computer Performance and Dependability Symposium*, pages 316–325, April 1995. 70
- [106] V. Nollet, P. Coene, D. Verkest, S. Vernalde, and R. Lauwereins. Designing an operating system for a heterogeneous reconfigurable SoC. In *Proceedings of the 17th International Symposium on Parallel and Distributed Processing*, April 2003. 70, 88
- [107] E. A. Lee and D. C. Messerschmitt. Static Scheduling of Synchronous Data flow Programs for Digital Signal Processing. *IEEE Transactions on Computers*, 36(1):24–36, January 1987. 72
- [108] A.V. Aho, R. Sethi, and J.D. Ullman. *Compiler: Principles, Techniques, and Tools*. Addison Wesley, 1986. 76
- [109] V.Sreedhar, G.R. Gao, and Y. Lee. Identifying Loops Using DJ Graphs. *ACM Transactions on Programming Languages and Systems (TOPLAS)*, 18(6):649–658, November 1996. 76
- [110] Steven A. Guccione. Multicore Devices: A New Generation of Reconfigurable Architectures. In *Proceedings of the 8rd International Conference on Engineering of Reconfigurable Systems and Architectures (ERSA'2008)*, pages 3–11, July 2008. 86
- [111] Freescale Semiconductor. *Multi-Core Microprocessors in Embedded Applications*, 2005. White Paper. 86
- [112] Y. Kurose, I. Kumata, M. Okabe, H. Hanaki, K. Seno, K. Hasegawa, H. Ozawa, S. Horiike, T. Wada, S. Arima, K. Taniguchi, K. Ono, H. Hokazono, T. Hiroi, T. Hirano, and S. Takashima. A 90nm Embedded DRAM Single Chip LSI with a 3D Graphics, H.264 Codec Engine, and a Reconfigurable Processor. In *Proc. of the 16th Symp. on High Performance Chips (Hot Chips 16)*, August 2004. 86
- [113] Toshiba. *A Dynamically Reconfigurable Architecture for Stream Processing*, 2007. Tutorial at International Conference on Field-Programmable Technology 2007 (ICFPT'07). 86, 88
- [114] Sanyo. *Reconfigurable Architecture for Car Tuners*, 2007. Tutorial at International Conference on Field-Programmable Technology 2007 (ICFPT'07). 86, 88
- [115] P. Merino, J.C. Lopez, and M. Jacome. A Hardware Operating System for Dynamic Reconfiguration of FPGAs. In *Proceedings of the 8th International Workshop on Field-Programmable Logic and Applications (FPL'98)*, pages 431–435, August 1998. 87
- [116] P. Merino, M. Jacome, and J.C. Lopez. A Methodology for Task Based Partitioning and Scheduling of Dynamically Reconfigurable Systems. In *Proceedings of IEEE Symposium on FPGAs for Custom Computing Machines (FCCM)*, pages 324–325, April 1998. 87
- [117] A. Ahmadiania, C. Bobda, and J. Teich. Dynamic Scheduling and Placement Algorithm for Reconfigurable Hardware. In *Architecture of Computing Systems (ARCS)*, pages 125–139, April 2004. 87
- [118] T. Marescaux, A. Bartic, D. Verkest, S. Vernalde, and R. Lauwereins. Interconnection networks enable fine-grain dynamic multi-tasking on FPGAs. In *Proceedings of the 12th International Workshop on Field-Programmable Logic and Applications (FPL'02)*, pages 795–805, September 2002. 87, 88, 102
- [119] Herbert Walder and Marco Platzner. Reconfigurable Hardware Operating Systems: From Design Concepts to Realizations. In *Proceedings of the 3rd International Conference on Engineering of Reconfigurable Systems and Architectures (ERSA'2003)*, pages 284–287, June 2003. 87, 88

- [120] Gordon Brebner and Oliver Diessel. Chip-based Reconfigurable Task Management. In *Proceedings of the 11th International Conference on Field Programmable Logic and Applications (FPL'01)*, pages 182–191, August 2001. 87, 88
- [121] H. Walder and M. Platzner. Non-preemptive Multitasking on FPGA: Task Placement and Footprint Transform. In *Proceedings of the International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA'2002)*, pages 24–30, June 2002. 87, 88
- [122] H. Kalte, M. Koester, B. Kettelhoit, M. Porrmann, and U. Ruckert. A comparative study on system approaches for partially reconfigurable architectures. In *Proceedings of the 4rd International Conference on Engineering of Reconfigurable Systems and Architectures (ERSA'2004)*, pages 70–76, June 2004. 87
- [123] Luca Benini and Giovanni De Micheli. *Networks on chips: technology and tools*. Morgan Kaufmann Publishers, 2006. 87, 102
- [124] T. Marescaux, J-Y. Migmolet, A. Bartic, W. Moffa1, D. Verkest, S. Vernalde, and RLauwereins. Networks on Chip as Hardware Components of an OS for Reconfigurable System. In *Proceedings of the 13th International Workshop on Field-Programmable Logic and Applications (FPL'03)*, pages 256–259, September 2003. 88, 102
- [125] Y. Mignolet, S. Vernalde, D. Verkest, and R. Lauwereins. Enabling hardware-software multitasking on a reconfigurable computing platform for networked portable multimedia appliances. In *Proceedings of the International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA'2002)*, pages 116–122, June 2002. 88
- [126] B. Black, D.W. Nelson, C. Webb, and N. Samra. 3D Processing Technology and Its Impact on iA32 Microprocessors. In *Proceedings of the International Conference on Computer Design*, pages 316–318, October 2004. 102
- [127] S. Das, A. Fan, K.N. Chen, C.S. Tan, N. Checka, and R. Reif. Technology, Performance, and Computer-Aided Design of Three-Dimensional Integrated Circuits. In *Proceedings of the International Symposium on Physical Design*, pages 108–115, April 2004. 102
- [128] W.R. Davis, J. Wilson, S. Mick, J. Xu, H. Hua, C. Mineo, A.M. Sule, M. Steer, and P.D. Franzon. Demystifying 3D ICs: The Pros and Cons of Going Vertical. *IEEE Design and Test of Computers*, 22(6):498–510, November 2005. 102
- [129] F. Li, C. Nicopoulos, T. Richardson, Y. Xie, V. Narayanan, and M. Kandemir. Design and Management of 3D Chip Multiprocessors Using Network-in-Memory. In *Proceedings of the International Symposium on Computer Architecture*, pages 130–141, June 2006. 102

Publications

Journal Papers

- [1] Vu Manh Tuan, and Hideharu Amano, "A Mapping Method for Multi-process Execution on Dynamically Reconfigurable Processors", *IEICE Transaction on Information & Systems*, Vol. E91-D, No.9, pages 2312-2322, September 2008.
- [2] Vu Manh Tuan, and Hideharu Amano, "A Preemption Algorithm for a Multitasking Environment on Dynamically Reconfigurable Processors", *IEICE Transaction on Information & Systems*, Vol. E91-D, No.12, pages 2793-2803, December 2008.
- [3] Yohei Hasegawa, Shohei Abe, Syunsuke Kurotaki, Vu Manh Tuan, and Hideharu Amano, "Evaluation of Time-multiplexed Execution on the Dynamically Reconfigurable Processor", *IPSJ Transaction on Advanced Computing Systems (ACS)*, Vol. 47, No. SIG12 (ACS15), pages 171-181, September 2006. (In Japanese)
- [4] Masayasu Suzuki, Yohei Hasegawa, Shohei Abe, Vu Manh Tuan, and Hideharu Amano, "A Novel Cost-Effective Context Memory Structure for Dynamically Reconfigurable Processors", *IEICE Transaction on Information & Systems*, Vol. J89-D, No. 6, pages 1101-1109, June 2006. (In Japanese)

International Conference Papers

- [5] Vu Manh Tuan, Hiroki Matsutani, Naohiro Katsura, and Hideharu Amano, "Evaluation of a Multicore Reconfigurable Architecture with Variable Core Sizes", *In Proceeding of the 23th International Parallel and Distributed Processing Symposium (IPDPS 2009) / Reconfigurable Architectures Workshop (RAW2009)*, May 2009 (accepted).
- [6] Vu Manh Tuan, and Hideharu Amano, "A Method for Capturing State Data on Dynamically Reconfigurable Processors", *In Proceeding of 2008 International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA)*, pages 208-214, Las Vegas, July 2008.
- [7] Vu Manh Tuan, and Hideharu Amano, "A Mapping Method for Multi-Processing Execution on Dynamically Reconfigurable Processors", *In Proceeding of 2007 International Conference on Field-Programmable Technology (ICFPT2007)*, 357-360, Kitakyushu, December 2007.

- [8] Vu Manh Tuan, Yohei Hasegawa, and Hideharu Amano, "Performance Analysis of Multi-Process Execution Model on Dynamically Reconfigurable Processor", *In Proceeding of the 7th International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA2007)*, pages 203-206, Las Vegas, NV, June 2007
- [9] Yohei Hasegawa, Shohei Abe, Shunsuke Kurotaki, Vu Manh Tuan, Naohiro Katsura, Takuro Nakamura, Takashi Nishimura, and Hideharu Amano, "Performance and Power Analysis of Time-multiplexed Execution on Dynamically Reconfigurable Processor", *In Proceeding of the 20th International Parallel and Distributed Processing Symposium (IPDPS 2006) / Reconfigurable Architectures Workshop (RAW2006)*, Rhodes Island, Greece, April 2006.
- [10] Masayasu Suzuki, Yohei Hasegawa, Vu Manh Tuan, Shohei Abe, and Hideharu Amano, "A Cost Effective Context Memory Structure for Dynamically Reconfigurable Processors", *In Proceeding of the 20th International Parallel and Distributed Processing Symposium (IPDPS 2006) / Reconfigurable Architectures Workshop (RAW2006)*, Rhodes Island, Greece, April 2006.
- [11] Vu Manh Tuan, Yohei Hasegawa, Naohiro Katsura, and Hideharu Amano, "Performance-Cost Trade-off Evaluation for the DCT Implementation on the Dynamically Reconfigurable Processor", *In Proceeding of International Workshop on Applied Reconfigurable Computing (ARC2006)*, pages 115-121, Delft, Netherlands, March 2006.
- [12] Yohei Hasegawa, Shohei Abe, Shunsuke Kurotaki, Vu Manh Tuan, Naohiro Katsura, Takuro Nakamura, Takashi Nishimura, and Hideharu Amano, "Application-Based Performance and Power Analysis of Dynamically Reconfigurable Processor", *International Symposium on Advanced Reconfigurable Systems*, Kyoto, Japan, December 2005.

Domestic Conference Papers and Technical Reports

- [13] Vu Manh Tuan, Hiroki Matsutani, Naohiro Katsura, and Hideharu Amano, "Evaluation of a Multicore Reconfigurable Architecture", *IEICE Technical Reports, VLD2008-92*, pages 7-12, January 2009.
- [14] Vu Manh Tuan, and Hideharu Amano, "A Method for Saving and Restoring Context Data of Hardware Tasks on the Dynamically Reconfigurable Processor", *IEICE Technical Reports, RECONF2008*, pages 71-76, January 2008.
- [15] Yohei Hasegawa, Shohei Abe, Syunsuke Kurotaki, Vu Manh Tuan, and Hideharu Amano, "Evaluation of Time-multiplexed Execution on the Dynamically Reconfigurable Processor", *The 4th Symp. on Advanced Computing Systems and Infrastructures (SACIS2006)*, pages 135-142, May 2006. (In Japanese)
- [16] Yohei Hasegawa, Takashi Nishimura, Shohei Abe, Syunsuke Kurotaki, Vu Manh Tuan, and

- Hideharu Amano, "Application-Based Performance and Power Analysis on Dynamically Reconfigurable Processor", *The 27th Parthenon Symposium*, pages 3-10, December 2005. (In Japanese)
- [17] Yohei Hasegawa, Hideharu Amano, Shohei Abe, Syunsuke Kurotaki, and Vu Manh Tuan, "Performance and Power Analysis of Time-multiplexed Execution on Dynamically Reconfigurable Processor", *IEICE Technical Reports, RECONF2005-35*, pages 31-36, September 2005. (In Japanese)
- [18] Naohiro Katsura, Yohei Hasegawa, Vu Manh Tuan, Hiroki Matsutani, and Hideharu Amano, "Performance Evaluation of Multi-core DRP for Stream Application", *IEICE Technical Reports, RECONF2006-52*, pages 49-54, November 2006. (In Japanese)
- [19] Vu Manh Tuan, Yohei Hasegawa, Naohiro Katsura, and Hideharu Amano. Performance Evaluation of Hardware Multi-process Execution on the Dynamically Reconfigurable Processor, *IEICE Technical Reports, RECONF2006-31*, pages 25-30, September 2006.
- [20] Naohiro Katsura, Yohei Hasegawa, Vu Manh Tuan, and Hideharu Amano, "Implementation of Stream Application on Programmable Devices by C Level Design", *IEICE Technical Reports, RECONF2005-82*, pages 31-36, January 2006. (In Japanese)