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D20. R. Giorgi, F. Khalili, F. Montefoschi, M. Procaccini, X. Martorell, D. Jiménez-González, A. C., P. Gai, S. Garzarella, V. Amourianos, D. Theodoropoulos, D. Pnevmatikatos, D. Oro, D. Catani, D. Cardillo, C. Magnani, S. Viola, N. Bettin, A. Pomella, "Performance and Energy Evaluation of AXIOM", *AXIOM D7.3*, Siena, Italy, Feb 2018, pp. 1-54, (deliverable).

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D18. M. Caporali, A. Rovai, R. Giorgi, "Final Rep. on AXIOM Events", *AXIOM D2.4*, Siena, Italy, Feb 2018, pp. 1-28, (deliverable).

D17. R. Giorgi, S. Viola, "Design Space Exploration (DSE) on the prototype", *AXIOM D7.2*, Siena, Italy, Feb 2017, pp. 1-36, (deliverable).

D16. M. Caporali, A. Rovai, R. Giorgi, "Rep. on AXIOM Events", *AXIOM D2.2*, Siena, Italy, Feb 2017, pp. 1-59, (deliverable).

D15. R. Giorgi, "Design Space Exploration (DSE) on the prototype", *AXIOM D7.1*, Siena, Italy, Jan 2016, pp. 1-38, (deliverable).

D14. R. Giorgi, "Initial AXIOM Evaluation Platform (AEP) definition and initial tests", *AXIOM D7.1*, Siena, Italy, Jan 2016, pp. 1-38, (deliverable).

D13. D. Catani, C. Magnani, X. Martorell, N. Navarro, D. Jiminez-Gonzalez, C. Alvarez, P. Gai, C. Scordino, D. Pnevmatikatos, D. Theodoropoulos, A. Pomella, R. Giorgi, "Tech. specification of AXIOM boards", *AXIOM D6.1*, Siena, Italy, Jan 2016, pp. 1-23, (deliverable).

D12. D. Catani, C. Magnani, X. Martorell, N. Navarro, D. Jiminez-Gonzalez, C. Alvarez, P. Gai, C. Scordino, D. Pnevmatikatos, D. Theodoropoulos, A. Pomella, R. Giorgi, "Tech. specification of AXIOM boards", *AXIOM D6.1*, Siena, Italy, Oct 2015, pp. 1-23, (deliverable).

D11. S. Zuckerman, J. Arteaga, J. Suetterlein, H. Wei, E. Garcia, G. Gao, A. Scionti, R. Giorgi, "Evaluation of the Codelet Runtime System on a Teradevice", *TERAFLUX D9.3*, Siena, Italy, May 2014, pp. 1-53, (deliverable).

D10. A. Scionti, H. Kifle, S. Mazumdar, R. Giorgi, N. Navarro, R. Badia, M. Valero, S. Weis, T. Ungerer, G. Mathou, T. Trancoso, P. Evripidou, A. Fuchs, Y. Weinsberg, P. Faraboschi, B. Khan, Watson,F. I. Li, A. Cohen, S. Zuckermand, J. Arteaga, G. Gao, L. Morin, S. Girbal, "Final Rep. and Documentation", *TERAFLUX D7.5*, Siena, Italy, May 2014, pp. 1-100, (deliverable).

D9. A. Cohen, F. Gindraud, F. Li, A. Pop, R. Badia, N. Navarro, T. Patejko, I. Watson, B. Khan, M. Lujan, R. Giorgi, A. Mondelli, L. Morin, "Advanced Version of the Compilation Tools", *TERAFLUX D4.7*, Siena, Italy, May 2014, pp. 1-25, (deliverable).

D8. R. Badia, D. Jiminez, C. Alvarez, A. Grabade, S. Weis, T. Ungerer, Diavastos,G. A. Mathou, T. Trancoso, P. Evripidou, B. Khan, S. Khan, W. Toms, M. Lujan, I. Watson, R. Giorgi, A. Scionti, B. Jacob, "Evaluation of the TERAFLUX Abstraction Layer and Fine-tuned Model", *TERAFLUX D6.4*, Siena, Italy, May 2014, pp. 1-65, (deliverable).

D7. M. Solinas, A. Scionti, M. Mondelli, N. Ho, A. Portero, S. Kavvadias, M. Bianchini, R. Giorgi, A. Garbade, S. Weis, T. Ungerer, A. Pop, F. Li, A. Cohen, L. Eleftheriades, N. Masrujeh, G. Michael, L. Petrou, A. Diavastos, T. Trancoso, P. Evripidou, N. Navarro, R. Badia, M. Valero, P. Faraboschi, B. Khan, S. Khan, M. Lujan, I. Watson, "Rep. on knowledge transfer and training", *TERAFLUX D7.4*, Siena, Italy, Dec. 2012, pp. 1-50, (deliverable).

D6. R. Giorgi, A. Portero, A. Scionti, A. Garbade, S. Weis, T. Ungerer, "Power and Thermal Modeling and Fault-injection support", *TERAFLUX D7.3*, Siena, Italy, Mar. 2012, pp. 1-28, (deliverable).

D5. C. Christofi, A. Diavastos, G. Michael, G. Mathou, T. Trancoso, P. Evripidou, M. Solinas, A. Scionti, A. Mondelli, H. Nam, A. Portero, R. Giorgi, B. Khan, S. Khan, M. Lujan, I. Watson, F. Yazdanpanah, D. Jiminez, A. Alvarez, Y. Etsion, R. Badia, "Fine-tuned TERAFLUX Execution Model", *TERAFLUX D6.3*, Siena, Italy, Dec 2012, pp. 1-34, (deliverable).

D4. R. Giorgi, A. Portero, C. Concatto, R. Mameesh, Z. Yu, Y. Etsion and L. Villanova and N. Navarro and R. Badia and M. Valero and P. Faraboschi and A. Cohen and D. Shamia and A. Mendelson and A. Garbade and S. Weis and T. Ungerer and P. Trancoso and P. Evripidou and B. Khan and S. Khan and M. Lujan and C. Kirkham and I. Watson, "Definition of ISA extensions, custom devices and External COTSon API extensions", *TERAFLUX D7.2*, Siena, Italy, Mar. 2011, pp. 1-78, (deliverable).

D3. R. Badia, Y. Etsion, R. Gayatri, M. Pavlovic, T. Patejko, D. Goodman, C. Seaton, M. Lujan, I. Watson, A. Portero, R. Giorgi, A. Diavastos, C. Christofi, S. Arandi, G. Michael, T. Trancoso, P. Evripidou, S. Girbal, "Final report on the characterization and modeling", *TERAFLUX D2.2*, Siena, Italy, Dec 2011, pp. 1-43, (deliverable).

D2. S. Arandi, C. Kyriacou, G. Michael, G. Mathou, N. Masrujeh, T. Trancoso, P. Evripidou, R. Giorgi, Z. Yu, S. Collange, S. Scionti, B. Khan, S. Khan, M. Lujan, I. Watson, T. Ungerer, B. Fechner, A. Garbade, S. Weis, "Advanced TERAFLUX Architecture", *TERAFLUX D6.2*, Siena, Italy, Dec 2011, pp. 1-49, (deliverable).

D1. R. Badia, Y. Etsion, J. Labarta, N. Navarro, M. Pavlovic, C. Servat. H. and Villavieja, S. Girbal, M. Ansari, M. Lujan, C. Kirkham, I. Watson, R. Giorgi, A. Portero, A. Cohen, "Rep. on the reference set of applications chosen, and initial characterization of the applications", *TERAFLUX D2.1*, Siena, Italy, Dec 2010, pp. 1-44, (deliverable).

14 Intellectual Property

IP2. S. Bartolini, P. Bennati, R. Giorgi, "BlueSign 2", *SIAE 24-02-2006/001*, Reg. 24 Feb. 2006.

IP1. P. Bennati, T. Capasso, V. Di Massa, F. Giallombardo, R. Giorgi, M. Guerrini, E. Maggio, N. Nannetti, "BlueSign Translator", *SIAE 002568, Ord. D003454*, Reg. 21 Mar. 2003.

15 Educational and Research Software

SW8. 2019(June)The WebRISC-V: Web-based RISC-V pipeline simulator http://www.dii.unisi.it/~giorgi/WebRISC-V

- Simulates a RISC-V pipeline inside a web browser. The architectural elements are visualized while instructions pass through the pipeline.
- This is a Bachelor Thesis that I supervised (Gianfranco Mariotti) for the realization of this tool, which led to a publication at the Workshop on Computer Architecture Education.

SW7. 2015(May) FREESS: The Free SuperScalar simulator http://www.dii.unisi.it/~giorgi/freess

- Simulates a simple Superscalar processor step-by-step, visualizing the activity of renaming, instruction window, reorder buffer, load/store queues.
- I am the author of this educational tool for students. The tool is written from scratch.

SW6. 2013(Sep) The Dataflow Run Time (DRT) http://sourceforge.net/projects/drt/

- A runtime library to code and debug programs that are based on a Thread-Level-Parallelism Instruction Set Extension (TLP ISE).
- I am the author of this tool which allows to execute programs in a dataflow style by simpling adding a header and using few library calls.

SW5. 2013(Jun) COTSon Thread Scheduler Unit (TSU) http://sourceforge.net/p/cotson/code/HEAD/tree/branches/timing-unisi/tsu4/

- A functional and timing model for an x86_64 based full-system. It uses a custom Instruction Set Extension (ISE) to support a dataflow based execution model. The model is a plugin of the HP-Labs COTSon full-system simulator.
- I coordinated a large group of more than ten researchers within the TERAFLUX project, by providing the core idea of a dataflow based scheduler, constant supervision and the leadership of the project.

SW4. 2010(Jun) The ERA BENCHMARK-SUITE http://www.dii.unisi.it/~giorgi/ebs

- A benchmark suite for research on embedded system for mobile.

- I coordinated a large group of more than ten researchers within the ERA project, by providing the core of a public set of benchmarks for embedded applications for mobile platforms, constant supervision and the leadership of the project.

SW3. 2004(May)The WEBMIPS: Web-based MIPS simulator http://www.dii.unisi.it/~giorgi/WEBMIPS and a revived version in PHP coming from the WebRISC-V project (see above) http://www.dii.unisi.it/~giorgi/WebMIPS

- Simulates a MIPS pipeline inside a web browser. The architectural elements are visualized while instructions pass through the pipeline.
- This started as a student project and I supervised the realization of this tool which led to a highly cited publication.
- The WebMIPS is a PHP edition of WEBMIPS (originally written in ASP), realized as part of a Bachelor thesis.

SW2. 2003(Sep) The BASICRYPT BENCHMARK-SUITE http://www.dii.unisi.it/~giorgi/basicrypt

- A benchmark suite for research on Elliptic Curve Cryptography.
- I coordinated a group of researchers within a FIRB project, by providing the core of a public set of benchmarks for cryptography based on Elliptic Curves.

SW1. 2003(June) JCACHESIM cache+CPU web-based simulator http://www.dii.unisi.it/~giorgi/jcachesim

- Simulates a cache memory and its internal operation, while executing simple MIPS programs. It runs in a java enabled web browser.
- This project originated from a Master thesis that I supervised and migrated from an old MS-DOS interface the full capabilities to a Java applet, while adding the cross-compilation of MIPS code.

16 Public Talks

T47. 2019(Sep), (Italian Workshop on High Performance Computing, University of Bologna, Italy), "Data-Flow based HPC" (presentation)

T46. 2019(Jul), (High Performance Computing and Simulation Conference, Dublin, IE), "Bridging a Data-Flow Execution Model to a Simple Programming Model" (presentation)

T45. 2019(Jul), (Deptartment of COmputer Science, University of Pisa, Italy), "DataFlow-Threads (DF-Threads): An Execution Model for Scalable Systems " (presentation)

T44. 2019(Jun), (Workshop on Computer Architecture Education (WCAE-2019)), "WebRISC-V: a Web-Based Education-Oriented RISC-V Pipeline Simulation Environmen" (presentation)

T43. 2019(Mar), (Conference on Design, Automation and Test in Europe (DATE-2019)), "AXIOM: A Scalable, Efficient and Reconfigurable Embedded Platform" (presentation)

T42. 2019(Feb), (IEEE Euromicro Int.l Conf. on Parallel, Distributed, and Network-Based Processing), "Analyzing the Impact of Operating System Activity of different Linux Distributions in a Distributed Environment" (presentation)

T41. 2019(Jan), (11th Workshop on Rapid Simulation and Performance Evaluation: Methods and Tools), "A Design Space Exploration Tool Set for Future 1K-core High-Performance Computers" (presentation)

T40. 2018(Sep), (Third Italian Workshop on Embedded Systems), "The AXIOM-board: bringing programmability, acceleration, scalability into a 64-bit hand-size board" (presentation)

T39. 2018(Jan), (SHiP-CPS: Software-Hardware Platforms for Cyber-Physical Systems), "The AXIOM platform for Cyber-Physical Systems" (presentation)

T38. 2017(Sep), (Second Italian Workshop on Embedded Systems), "The AXIOM-board: bringing programmability, acceleration, scalability into a 64-bit hand-size board" (presentation)

T37. 2018(Jun), (Keynote Speech at IEEE MECO conference), "The AXIOM-board: bringing programmability, acceleration, scalability into a 64-bit hand-size board" (presentation)

T36. 2016(Sep), (First Italian Workshop on Embedded Systems), "AXIOM: A 64-bit scalable embedded system including Arduino socket and on-chip FPGA" (presentation)

T35. 2016(Sep), (VIMAR, Marostica, Italy), "AXIOM Operating System analysis" (presentation)

T34. 2016(Jun), (Barcelona Supercomputing Center, Barcelona, Spain), "AXIOM Design Exploration Tools" (presentation)

T33. 2016(Apr), (ARTEMIS Spring Event, Vienna, Austria), "The AXIOM Cyber Physical System" (presentation)

T32. 2015(May), (Barcelona Supercomputing Center, Barcelona, Spain), "The AXIOM project" (presentation)

T31. 2015(May), (Barcelona Supercomputing Center, Barcelona, Spain), "The COTSon simulation environment" (tutorial)

T30. 2015(Feb), (CEA conference, Dubai, UAE), "Accelerating Haskell on a Dataflow Architecture: a case study including Transactional Memory"

T29. 2014(Oct), (MPP Workshop, Paris, France), "An Introduction to DF-Threads and their Execution Model"

T28. 2014(Sep), (Istituto di Calcolo ad Alte Prestazioni, Napoli, Italy), "TERAFLUX: Harnessing 1 TERA devices in a single package"

T27. 2013(Aug), (Georgia Tech, Atlanta, GA, USA), "TERAFLUX overview and the T* instruction extension"

T26. 2013(Aug), (University of Delaware, DE, USA), "TERAFLUX Research Overview"

T25. 2013(Oct), (SoC conference,Tampere,FI), "The TERAFLUX Project OVERVIEW" (presentation)

T24. 2013(Oct), (SoC conference,Tampere,FI), "MANY-CORE CHIPS and New High-Performance Computing Platforms: Hardware Thread-Level Parallelism Support in Many-Core Architectures" (tutorial)

T23. 2013(Jun), (CASTNESS workshop, Barcelona, Spain), "The T* Instruction Set Extension" (presentation)

T22. 2013(May), (University of Pisa, Italy), "DATAFLOW: different answer to achieve Scalabilty" (tutorial)

T21. 2013(Mar), (DATE Conference, Grenoble, France), "Lessons learned from European Projects" (Panel)

T20. 2013(Feb), (University of Siena, Italy), "Creation and Management a Large Scale search Project"

T19. 2012(Jun), (), "TERAFLUX, Effective Operation of Dataflow Parallelism in Teradevices"

T18. 2012(May), (Computing Frontiers conference, Cagliari, Italy), "TERAFLUX: Exploiting Dataflow Parallelism Teradevice Computing"

T17. 2012(Jun), (CASTNESS workshop, Paris, France), "TERAFLUX, Effective Operation of Dataflow Parallelism in Teradevices"

T16. 2011(Oct), (DFM Workshop, Galveston, TX, USA), "Data Flow Execution models" (panelist)

T15. 2011(Apr), (ODES workshop, CGO Conference, Chamonix, France), "TERAFLUX: exploiting DATAFLOW parallelism" (Keynote speech)

T14. 2011(Jan), (CASTNESS workshop, Rome, Italy), "Overview of a TERAFLUX-like Architecture"

T13. 2010(Jun), (International Forum on Multicores), "Integrating multicore research and the COTSon simulation platform"

T12. 2010(May), (HiPEAC Computing Week, Edinburgh UK), "TERAFLUX: exploiting DATAFLOW parallelism"

T11. 2005(May), (Dept. of Electronics and Information Systems, Ghent, Belgium), "Tiled Architectures for Embedded Systems"

T10. 2004(Oct), (Dept. of Computer Engineering, Delft, Olanda), "Non- Conventional Microprocessor Architectures"

T9. 2004(Sep), (HiPEAC Workshop, Juan les Pins, France), "Embedded-System Research Overview"

T8. 2003(Nov), (University of Pisa, Italy), "Non-Conventional Microprocessor Architectures"

T7. 2002(Jan), (SSGRRw-2002 Conference, L'Aquila, Italy), "Non-Conventional Microprocessor Architectures"

T6. 2001(Nov), (SGS-Thomson Advanced Research Laboratory, Milan, Italy), "Architetture Non-Convenzionali per Microprocessore"

T5. 2000(Apr), (University of Siena, Italy), "Introduzione alla Architettura Scheduled Data-Flow -SDF"

T4. 1999(May), (Dept. of Electrical and Computer Engineering, University of Alabama in Huntsville, AL, USA), "Scheduled Dataflow Architecture: problems and issues"

T3. 1998(May), (University of Belgrade, Serbia, Yugoslavia), "Simulating Composite Workloads on Shared-Bus Symmetric Multiprocessors"

T2. 1997(Sep), (Facoltà di Ingegneria, Università di Salerno, Benevento), "Trace Factory: a Hybrid Approach to Trace Generation for Performance Evaluation of Shared Bus Multiprocessors"

T1. 1997(Aug), (Computer Science and Engineering Dept., University of Texas at Arlington, TX, USA), "Trace Driven Simulation of Shared-Bus Multiprocessors"

17 Supervised Collaborators/Students

1. Visiting Professor
   - 2012(Sep)-2014(May) Bruce Jacob (University of Maryland)
2. Researchers
   - 2012(Apr)-2014(Jan) Alberto Scionti
   - 2012(Apr)-2013(Apr) Marco Solinas
3. Postdocs
   - 2010(Jun)-2013(Jul) Antonio Portero

- 2012(Mar)-2013(Oct) Stamatis Kavvadias
- 2010(Jun)-2012(Jan) Yu Zhibin
- 2011(Sep)-2011(Dec) Sylvain Collange
- 2010(Jun)-2011(May) Rania Mameesh
- 2010(Jan)-2011(Jan) Vincenzo Di Massa
- 2010(Jan)-2011(Jan) Nikola Puzovic
- 2010(Apr)-2010(Jun) Andrea Casaccino
- 2007(Oct)-2008(Nov) Paolo Bennati

4. Ph.D. Students
   - 2018(Nov)-present Tutoring of Ph.D. student Amin Sahebi, ciclo XXXIV.
   - 2017(Oct)-present Tutoring of Ph.D. student Farnam Khalili Maybodi, ciclo XXXIII.
   - 2016(Oct)-present Tutoring of Ph.D. student Marco Procaccini, ciclo XXXII.
   - 2013(Nov)-2017(Jul) Tutoring of Ph.D. student Somnath Mazumdar, ciclo XXIX - Thesis title: "An Efficient NoC-based Framework to Improve Dataflow Thread Management at Runtime"
   - 2005(Nov)-2008(Nov) Tutoring of Ph.D. student Nikola Puzovic, ciclo XXI - Thesis title: "Implementing fine/medium grained TLP support in multi-core architectures"
   - 2005(Nov)-2008(Nov) Tutoring of Ph.D. student Zdravko Popovic, ciclo XXI - Thesis title: "Multithreaded Dataflow in Tiled Architectures"
   - 2004(Nov)-2007(Sep) Tutoring of Ph.D. student Paolo Bennati, ciclo XX - Thesis title: "Embedded Systems: Low-Power techniques and applications"
   - 2001(Nov)-2005(Apr) Co-Tutoring of Ph.D. Student Irina Branovic - Thesis title: "Architectural Support for Elliptic Curve Cryptography (ECC) "
5. Graduate Students
   - 2017(Sep)-2017(Oct) Tutoring of student Farnam Khalili Maybodi
   - 2016(Dec)-2017(Feb) Hosting of Ph.D. student Arthur Lorenzon, from UFRGS, Brazil - sponsored by a 3-month HiPEAC (H2020) mobility grant.
   - 2014(Nov)-2015(Oct) Tutoring of Ph.D. student Nitin Satpute, ciclo XXX.
   - 2012(Jan)-2014(Nov) Tutoring of Ph.D. student Cai Kang, ciclo XXVII.
   - 2014(Aug)-2014(Nov) Tutoring of student Amit Fuchs
   - 2013(Jul)-2014(Mar) Tutoring of student Haileyesus Kifle
   - 2013(Nov)-2014(Mar) Tutoring of student Daniele Colobraro
   - 2013(Apr)-2014(Jan) Tutoring of student Bogdan Azaric
   - 2012(Jun)-2012(Nov) Tutoring of student Eliana Sala Mariet
   - 2012(Jun)-2013(Aug) Tutoring of student Andrea Mondelli
   - 2012(Jan)-2013(Apr) Tutoring of student Ho Nam
   - 2010(Jul)-2011(Jan) Tutoring of student Caroline Concatto
   - 2008(Sep)-2009(Jun) Tutoring of student Andrea Righi
   - 2008(Feb)-2008(Sep) Tutoring of student Nenad Korolija
   - 2008(Feb)-2008(Sep) Tutoring of student Roberto D'Aprile
   - 2004(Sep)-2005(Oct) Tutoring of student Zdravko Popovic
   - Orientation Activity for potential students coming from High School.
   - Tutor for several Master Thesis, Faculty of Engineering, University of Siena.
6. Master Students
   - 2019 Gianfranco Mariotti (Bachelor), "Un Ambiente di Simulazione Accessibile via Web per lo Studio della Pipeline del Processore RISC-V".
   - 2015 Ettore Chimenti (Bachelor), "Porting di un sistema operativo GNU/Linux su Single-board computer ARM".
   - 2007 Giovanni Burresi (Bachelor), "Valutazione delle prestazioni di IBM Cell Processor nelle simulazioni finanziarie".
   - 2005 Fabio Antonio Cassini (Master), "Realizzazione del modulo aggiuntivo per un concentratore seriale su interfacce I^2C BUS e 1-wire bus".

- 2005 Gian Lorenzo Meocci (Bachelor), "Studio e implementazione di un sistema embedded adibito al controllo del traffico".
- 2004 Mauro Marchetti (Master), "Realizzazione di un sistema di supporto alle decisioni per investimenti in borsa basato su analisi tecnica e analisi delle notizie".
- 2004 Christos Ververidis (Master), "Analisi delle prestazioni di sistemi di elaborazione con cache: uno strumento visuale".
- 2001 Lorenzo Menconi (Master), "Progettazione di un sistema di supporto alle decisioni per l'investimento finanziario" (co-advisor).

18 Professional Activities

1. Founded initiatives
   - 2017 Founding member of the IEEE Special Technical Community "Parallel Model & System: Dataflow and beyond"
2. Project Evaluator
   - Independent Expert of the MIUR under the REPRISE database for evaluation of Fundamental Research and Industrial Research, June 2018.
   - Independent Expert of the European Commission for the evaluation of CHIST-ERA (Future and Emerging Technology) 2012 - FP7 (7th Framework Programme) March 2012.
   - Independent Expert of the European Commission for the evaluation of Call FET (Future and Emerging Technology) 2008 - FP7 (7th Framework Programme) Massive ICT. FP6 IST-FET-26825 SHAPES (Scalable Software Hardware Architecture Platform for Embedded Systems), November 2006 through January 2010.
   - Reviewer of NWO Projects (Netherlands Research Organization) and EU projects.
   - Consultant for the EU Call Objective ICT-2009.8.1: FET proactive 1: Concurrent Tera-device Computing, Brussels, Nov. 2008.
   - IEEE Judge (among the 8 coming from the Industry and the Academy) for IEEE Computer Science International Design Competition (CSIDC) 2001 (http://computer.org/csidc) sponsored by Intel, Toshiba, Ericsson, AMD, Microsoft, Lucent, EMC, Hewlett-Packard, Sun, Motorola, to assign prizes for 70'000 USD. June-July 2001.
3. Member of Ph.D. Graduation Committees
   - PhD Committee (2 candidates):Università degli Studi di Padova, Italy, Milan, Italy, October 2019.
   - PhD Committee (4 candidates):Politecnico di Milano, Milan, Italy, February 2019.
   - PhD External Evaluator:Istituto Nazionale di Fisica Nucleare, Rome, Italy, December 2017.
   - PhD External Evaluator:Universitat Politecnica de Valencia, Valencia, Spain, December 2016.
   - PhD Committee:Universitat Politecnica de Valencia, Valencia, Spain, December 2014.
   - PhD Committee:Universitat Politecnica de Catalunya, Barcelona, Spain, May 2014.
   - PhD Committee:Universitat Politecnica de Catalunya, Barcelona, Spain, September 2011.
   - PhD Committee:Chalmers University, Goteborg, Sweeden, June 2011.
   - PhD Committee:Universitat Politecnica de Catalunya, Barcelona, Spain, December 2009.
   - PhD Committee:IMT - Institute for Advanced Studies, Lucca, Italy, July 2009.
4. Member of Ph.D. Selection Committees
   - University of Florence, University of Pisa, University of Siena, "Smart Computing", Sept. 2015.
   - University of Siena, Dept. of Information Engineering, Sept. 2010.
   - University of Siena, Dept. of Information Engineering, Sept. 2008.
5. Journal Editorial Boards
   - 2017(Mar)-present Associate Editor of the International Journal of Embedded Systems (IJES).
   - 2014(Jan)-present Member of the editorial board of the International Journal of Embedded Systems (IJES).
   - Co-Guest Editor of ACM Computer Architecture News (official Newsletter of ACM Special Interest Group on Computer Architecture), number of December 2001, with emphasis on Compilation Techniques, Parallel Architectures and Frontiers Topics.
   - Guest Editor of IEEE-TCCA NEWSLETTER (official Newsletter of IEEE Special Interest Group in Computer Architecture), number of January 2001, with emphasis on MEmory DEcopupled Architectures in modern microprocessors.

- Co-Guest Editor of Journal of Embedded Computing, 2006 special issue on Embedded Single-Chip Multicore Architectures and related research - from System Design to Application Support.
- Journal Reviewer: IEEE Transaction on Computers, IEEE Transaction on Parallel and Distributed Systems, IEEE Micro, IEEE Concurrency, Computer Journal, Journal of System Architecture, IEEE Transaction on Circuits and Systems, Elsevier Microprocessor and Microsystems, ACM Transactions on Architecture and Code Optimization (TACO), Concurrency and Computation: Practice and Experience, Elsevier Parallel Computing, Journal of Parallel and Distributed Systems.

6. Keynote Speaker
   - **Keynote Speaker**: IEEE MECO Conference 2017, Bar, Montenegro, June 2017.
   - **Keynote Speaker**: SSGRR 2002w International Conference, L'Aquila, Italy, January 2002.

7. Chairing
   - **Program Chair**: 3rd Italian Workshop on Embedded Systems, Siena, Italy, September 2018.
   - **Program Chair**: Software/Hardware platforms for Cyber-Physical Systems Workshop, Manchester, UK, January 2018.
   - **General Chair**: ACM Computing Frontiers 2017, Siena, Italy, May 2017.
   - **Program Chair** of the European-Project track: DATE 2016, Dresden, Germany, March 2016.
   - **General Chair**: CASTNESS 2012, Paris, France, January 2012.
   - **General Co-Chair**: HiPEAC WRC 2011, Heraklion, Greece, January 2011.
   - **Program Co-Chair**: HiPEAC WRC 2010, Pisa, Italy, January 2010.
   - Publicity Chair: HiPEAC 2010, Pisa, Italy, January 2010.
   - Financial/Local Co-Chair: WAIFI-2008 Workshop, Siena, Italy, July 2008.
   - **Program Co-Chair**: ESA-05 Conference, Las Vegas, Nevada, USA, June 2005.
   - **General Chair**: MEDEA-2001 Workshop, Barcelona, Spain (EU), September 2001.
   - **Program Chair**: MEDEA-2000 Workshop, Philadelphia, Pennsylvania (USA), October 2000.
   - **General Chair and Founder**: MEDEA-2000 Workshop, Philadelphia, Pennsylvania (USA), October 2000.

8. Program Committee Membership

PC134. IEEE DFM-2021, Virtual, July 2021.
PC133. Field Programmable Logic Conference, FPL-2021, Dresden, DE, September 2021.
PC132. Architecture of Computing Systems, ARCS 2021, Virtual, June 2021.
PC131. Applied Reconfigurable Computing, ARC 2020, Rennes, France, June 2021.
PC130. IEEE MECO CPS & IoT, Budva, Montenegro, June 2021.
PC129. HiPEAC RAPIDO 2021, Budapest, HU, January 2021.
PC128. IEEE BIGDATASE-2020, Guangzhou, China, November 2020.
PC127. Field Programmable Logic Conference, FPL-2020, Goteborg, SW, September 2020.
PC126. ICPP Embedded Multicore Systems, EMS 2020, Edmonton, Canada, August 2020.
PC125. EUROMICRO DSD-2020, Portoroz, Slovenia, August 2020.
PC124. IEEE DFM-2020, Madrid, Spain, July 2020.
PC123. Workshop on Parallel Programming Models,, MPP 2020, New Orleans, Loiusiana, USA, May 2020.
PC122. Architecture of Computing Systems, ARCS 2020, Aachen, Germany, May 2020.
PC121. Applied Reconfigurable Computing, ARC 2020, Toledo, Spain, April 2020.
PC120. ACM SAC-2020 Special Track, Brno, Czech Republic, April 2020.
PC119. HiPEAC RAPIDO 2020, Bologna, IT, January 2020.
PC118. IEEE DFM-2019, Milwaukee, Wisconsin, USA, July 2019.
PC117. Field Programmable Logic Conference, FPL-2019, Barcelona, Spain, September 2019.
PC116. EUROMICRO DSD-2019, Kallithea, Chalkidiki, Greece, August 2019.
PC115. ICPP Embedded Multicore Systems, EMS 2019, Kioto, Japan, August 2019.
PC114. The 8th International Workshop on Advances in Parallel Programming Models and Frameworks for the Multi-/Many-core Era, Dublin, Ireland, July, 2019.
PC113. IEEE MECO-2019, Budva, Montenegro, June 2019.
PC112. Architecture of Computing Systems, ARCS 2019, Copenhagen, Denmark, May 2019.
PC111. Applied Reconfigurable Computing, ARC 2019, Darmstadt, Germany, April 2019.
PC110. HiPEAC RAPIDO 2019, Valencia, ES, January 2019.
PC109. ACM SAC-2019 Special Track, Limassol, Cyprus, April 2019.
PC108. The 18th IEEE International Conference on Scalable Computing and Communications, ScalCom-2018, Guangzhou, China, October 2018.
PC107. IEEE ReConFig 2018, Cancun, Maxico, December 2018.
PC106. Field Programmable Logic Conference, FPL-2018, Dublin, Ireland, August 2018.
PC105. ICPP Embedded Multicore Systems, EMS 2018, Eugene, Oregon, USA, August 2018.
PC104. EUROMICRO DSD-2018, Prague, Czech Republic, August 2018.

PC103. IEEE MECO-2018, Budva, Montenegro, June 2018.
PC102. Applied Reconfigurable Computing, ARC 2018, Santorini, May 2018.
PC101. ACM SAC-2018 Special Track, Pau, France, April 2018.
PC100. Architecture of Computing Systems, ARCS 2018, Braunschweig, Germany, April 2018.
PC99. HiPEAC RAPIDO 2018, Manchester, UK, January 2018.
PC98. HiPEAC WRC WRC 2018, Manchester, UK, January 2018.
PC97. IEEE ReConFig 2017, Cancun, Mexico, December 2017.
PC96. SBACPAD-2017, Campinas, Brazil, October 2017.
PC95. IEEE FPL-2017, Ghent, Belgium, September 2017.
PC94. ICPP Embedded Multicore Systems, EMS 2017, Bristol, UK, August 2017.
PC93. IEEE MSPDS 2017, Genova, Italy, July 2017.
PC92. IEEE MECO-2017, Bar, Montenegro, June 2017.
PC91. ACM SAC-2017 Special Track, Marrakesh, Morocco, April 2017.
PC90. Applied Reconfigurable Computing, ARC 2017, Delft, Netherlands, April 2017.
PC89. Architecture of Computing Systems, ARCS 2017, Vienna, Austria, April 2017.
PC88. HiPEAC Embedded 2017, Nurnberg, February 2017.
PC87. HiPEAC RAPIDO 2017, Stockholm, Sweden, January 2017.
PC86. HiPEAC WRC WRC 2017, Stockholm, Sweden, January 2017.
PC85. ICPP Embedded Multicore Systems, EMS 2016, Philadelphia, PA, USA, August 2016.
PC84. IEEE ReConFig 2016, Cancun, Mexico, November 2016.
PC83. IEEE DFM-2016, Haifa, Israel, September 2016.
PC82. IEEE FPL-2016, Lausanne, Switzerland, August 2016.
PC81. IEEE MECO-2016, Bar, Montenegro, June 2017.
PC80. ACM SAC-2016 Special Track, Pisa, Italy, April 2016
PC79. IEEE MSPDS 2016, Innsbruck, Austria, July 2016.
PC78. Architecture of Computing Systems, ARCS 2016, Nurnberg, April, 2016.
PC77. HiPEAC WRC 2016, Prague, Czech Republic, January 2016.
PC76. HiPEAC RAPIDO 2016, Prague, Czech Republic, January 2016.
PC75. IEEE DFM-2015, San Francisco, CA, USA, October 2015.
PC74. IEEE ICCD-2015, New York, USA, October 2015.
PC73. IEEE FPL-2015, London, UK, September 2015.
PC72. IEEE WCS-IOT 2015, London, UK, September 2015.
PC71. EUROMICRO DSD-2015, Funchal, Madeira, Portugal, August 2015.
PC70. IEEE M2A2-2015, New York, USA, August 2015.
PC69. WRC-2015 Workshop, Amsterdam, Netherlands, January 2015.
PC68. MULTIPROG-2015 Workshop, Amsterdam, Netherlands, January 2015.
PC67. ARCS-2015, Porto, Portugal, March 2015.
PC66. ACM SAC-2015 Special Track, Salamanca, Spain, April 2015.
PC65. IEEE ICPADS-2014, Hsinchu, Taiwan, December 2014.
PC64. IEEE ICCD-2014, Seoul, Korea, October 2014.
PC63. IEEE FPL-2014, Munich, Germany, September 2014.
PC62. IEEE DFM-2014, Edmonton (Alberta), Canada, August 2014.
PC61. IEEE M2A2-2014, Paris, France, August 2014.
PC60. 2014 ACM International Conference on Supercomputing (ICS), (External Review Committee), Munich, Germany, June 2014.
PC59. ACM SAC-2014 Special Track, Gyeongiu, South Korea, March 2014.
PC58. ARCS-2014, Lubeck, Germany, February 2014.
PC57. MULTIPROG-2014 Workshop, Vienna, Austria, January 2014.
PC56. IEEE ICPADS-2013, Seoul, Korea, December 2013.
PC55. IEEE ICCD-2013, Asheville, NC, USA, October 2013.
PC54. IEEE DFM-2013, Edinburgh, UK, September 2013.
PC53. IEEE FPL-2013, Porto, Portugal, August 2013.
PC52. IEEE M2A2-2013, Melbourne, Australia, July 2013.
PC51. HiPEAC WRC 2013, Berlin, Germany, January 2013.
PC50. ACM SAC-2013 Special Track, Trento, Italy, March 2013.
PC49. ARCS-2013, Prague, Czech Republic, February 2013.
PC48. MULTIPROG-2013 Workshop, Berlin, Germany, January 2013.
PC47. IEEE FPL-2012, Oslo, Norway, August 2012.
PC46. IEEE M2A2-2012 Workshop IEEE International Workshop on Multicore and Multithreaded Architectures and Algorithms, Madrid, Spain, July 2012.
PC45. IEEE ICCD-2012, Montreal, Quebec, Canada, September 2012.
PC44. Workshop on the Growing Problems with Scalable Heterogeneous Infrastructures (GSHI'12), Madrid, Spain, July 2012.
PC43. HiPEAC WRC 2012, Paris, France, January 2012.
PC42. ACM SAC-2012 Special Track, Trento, Italy, March 2012.
PC41. ARCS-2012, Munich, Germany, February 2012.
PC40. MULTIPROG-2012 Workshop, Paris, France, January 2012.
PC39. IEEE SEC-2011, Sydney, Australia, December 2011.

PC38. IEEE ICCD-2011, Amherst, MA, USA, October 2011.
PC37. IEEE FPL-2011, Chania, Greece, September 2011.
PC36. ACM SAC-2011 Special Track, TaiChung, Taiwan, March 2011.
PC35. ARCS-2011, Lake Como, Italy, February 2011.
PC34. MULTIPROG-2011 Workshop, Heraklion, Greece, January 2011.
PC33. IEEE ICCD-2010, Amsterdam, Netherlands, October 2010.
PC32. IEEE FPL-2010, Milano, Italy, August 2010.
PC31. MULTIPROG-2010 Workshop, Pisa, Italy, January 2010.
PC30. ACM SAC-2010 Special Track, Sierre, Switzerland, March 2010.
PC29. IEEE ICCD-2009, Lake Tahoe, California (USA), October 2009.
PC28. WoRMES 2009, Vancouver, Canada, August 2009.
PC27. ICPP 2009, Vienna, Austria, September 2009.
PC26. Computing Frontiers 2009, Ischia, Italy, May 2009.
PC25. ACM SAC-2009 Special Track, Honolulu, Hawaii (USA), March 2009.
PC24. MULTIPROG-2009 Workshop, Paphos, Cyprus, January 2009.
PC23. IEEE ICCD-2008, Lake Tahoe, California (USA), October 2008.
PC22. MEDEA-2008 Workshop, Toronto, Canada, October 2008.
PC21. IEEE SEC-2008, Beijing, China, October 2008.
PC20. MEDEA-2008 Workshop, Toronto, Canada, October 2008.
PC19. IEEE SEC-2008, Beijing, China, October 2008.
PC18. ACM SAC-2008 Special Track, Fortaleza, Brazil, March 2008.
PC17. MULTIPROG-2008 Workshop, Goteborg, Sweden, January 2008.
PC16. MEDEA-2007 Workshop, Brasov, Romania, September 2007.
PC15. HiPEAC 2007 Conference , Ghent, Belgium, January 2007.
PC14. ACM SAC-2007 Special Track, Seoul, Korea, March 2007.
PC13. MEDEA-2006 Workshop, Seattle, Washington, USA, September 2006.
PC12. ACM SAC-2006 Special Track, Dijon, France, April 2006.
PC11. HiPEAC 2005 Conference , Barcelona, Spain, November 2005.
PC10. MEDEA-2005 Workshop, Saint Loius, Missouri, USA, September 2005.
PC9. SCOPES-2005 Workshop, Dallas, Texas, USA, September 2005.
PC8. PDES-05 IEEE/IFIP Workshop, Fukuoka, Japan, July 2005.
PC7. ACM SAC-2005 Special Track, Santa Fe, New Mexico, USA, March 2005.
PC6. MEDEA-2004 Workshop, Antibes Juan-les-Pins, France, September 2004.
PC5. ACM SAC-2004 Special Track, Nycosia, CIPRO, March 2004.
PC4. MEDEA-2003 Workshop, New Orleans, Louisiana (USA), September 2003.
PC3. ACM SAC-2003 Special Track, Melbourne, Florida (USA), March 2003.
PC2. PACT-2002 Conference, Charlottesville, Virginia (USA), September 2002.
PC1. MEDEA-2002 Workshop, Charlottesville, Virginia (USA), September 2002.

19 Major Departmental Committees

- 2006 **President** of the Self-Evaluation Committee (RAV) for the Information Engineering Laurea.
- 2018(Oct)-present **Scientific Director of the University of Siena** in the Italian Academic Consortium for Informatics (CINI).
- 2018(Oct)-present **Delegate of the University of Siena (appointed by the Ministry)** in the Italian Academic Consortium for Informatics (CINI).
- 2018(Mar)-present **Department Deputy** for the University of Siena Alumni Association.
- 2015(Jun)-present **Member of Ph.D. Committee "Smart Computing"** (Uni. of Florence, Pisa, Siena).
- 2014-present Member of the Student Tutoring Committee for the University of Siena.
- 2019-present Member of the Orientation commission.
- 2010-present Member of Admission Committee to the Master Degrees.
- 2000-present President and member of several selection procedure for Ph.D. grants (2 times), Postdoc grants (5+ times), Post-laurea grants (5+ times).
- 2012(Nov) Member of Commission for ING-INF/05 (Computer Systems) selection call for researchers.
- 2012-2015 Member of Department Committee for the Management of Scientific spaces.
- 2002-2010 Member of Ph.D. Committee (Department of Information Engineering, Siena).
- 2001-2010 Member of Local Area Network Management (Department Information Engineering, Siena).

- 2006-2009 Member of the Evaluation Board for Master and Bachelor Degree in Computer Engineering (Faculty of Engineering, Siena).
- 2001-2009 **Technological Area Coordinator** for Master in New Technologies and Company Management (University of Siena).
- 2001-2009 Member of the Evaluation Board for Master in New Technologies and Company Management (University of Siena).
- 2005(Oct) Member of Commission for ING-INF/05 (Computer Systems) selection call for researchers.
- 2000-2005 Member of the Orientation and Tutoring commission.
- 2000-2005 Design and Maintenance of Orientation WEB Site, Faculty Engineering, Siena (www.ing.unisi.it/orientamento - www.ing.unisi.it/orientamento/initinere - www.ing.unisi.it/orientaing).

(continues)

20 Teaching

The following courses have been taught at the University of Siena at the School of Engineering, at the School of Economics and at the S.Chiara College. From year 2000 until now, more than 365 ECTS credits[1] have been taught (corresponding to an average of about 18 credits per year).

As Associate Professor:

Year	Course	ECTS credits	Level	School	Lang.
2019-2020	Advanced Computer Architecture	9	Master	Information Engineering	English
2019-2020	Computer Architecture	6	Bachelor	Information Engineering	Italian
2018-2019	Advanced Computer Architecture	9	Master	Information Engineering	English
2018-2019	Computer Architecture	6	Bachelor	Information Engineering	Italian
2017-2018	Advanced Computer Architecture	9	Master	Information Engineering	English
2017-2018	Computer Architecture	6	Bachelor	Information Engineering	Italian
2016-2017	Advanced Computer Architecture	9	Master	Information Engineering	English
2016-2017	Computer Architecture	6	Bachelor	Information Engineering	Italian
2015-2016	Advanced Computer Architecture	9	Master	Information Engineering	English
2015-2016	Computer Architecture	6	Bachelor	Information Engineering	Italian
2014-2015	Advanced Computer Architecture	9	Master	Information Engineering	English
2013-2014	Advanced Computer Architecture	9	Master	Information Engineering	English
2013-2014	Computer Architecture	6	Bachelor	Information Engineering	Italian
2012-2013	Advanced Computer Architecture	9	Master	Information Engineering	English
2012-2013	Computer Architecture	6	Bachelor	Information Engineering	Italian
2011-2012	Advanced Computer Architecture	9	Master	Information Engineering	Italian
2011-2012	Computer Architecture	6	Bachelor	Information Engineering	Italian
2010-2011	Advanced Computer Architecture	9	Master	Information Engineering	Italian
2010-2011	Computer Architecture	6	Bachelor	Information Engineering	Italian
2009-2010	Advanced Computer Architecture	6	Master	Information Engineering	Italian
2009-2010	Computer Architecture	6	Bachelor	Information Engineering	Italian
2008-2009	Advanced Computer Architecture	6	Master	Information Engineering	Italian
2008-2009	Computer Architecture	6	Bachelor	Information Engineering	Italian
2007-2008	**Low Power Architectures**	2	**Ph.D.**	Information Engineering	Italian
2007-2008	Advanced Computer Architecture	6	Master	Information Engineering	Italian
2007-2008	Information Security	3	Master	Management of Financial Inst.	Italian
2007-2008	Computer Architecture	6	Bachelor	Information Engineering	Italian
2006-2007	**Low Power Architectures**	2	**Ph.D.**	Information Engineering	Italian
2006-2007	Advanced Computer Architecture	6	Master	Information Engineering	Italian
2006-2007	Information Security	3	Master	Management of Financial Inst.	Italian
2006-2007	Computer Architecture	6	Bachelor	Information Engineering	Italian
2005-2006	Advanced Computer Architecture	6	Master	Information Engineering	Italian
2005-2006	Information Security	3	Master	Management of Financial Inst.	Italian
2005-2006	Computer Architecture	6	Bachelor	Information Engineering	Italian

As Assistant Professor:

Year	Course	ECTS credits	Level	School	Lang.
2004-2005	Advanced Computer Architecture	6	Master	Information Engineering	Italian
2004-2005	Operating Systems and Security	3	Master	Management of Financial Inst.	Italian
2004-2005	Computer Architecture	6	Bachelor	Information Engineering	Italian
2003-2004	Advanced Computer Architecture	12	Master	Information Engineering	Italian
2003-2004	C++ Programming Laboratory	2	Master	Information Engineering	Italian
2003-2004	Programming Fundamentals	3	Master	Digital Economy and E-business	Italian
2003-2004	Operating Systems and Security	3	Master	Management of Financial Inst.	Italian
2003-2004	Computer Architecture	6	Bachelor	Information Engineering	Italian
2003-2004	Informatics for Industrial Applications	6	Bachelor	Information Engineering	Italian
2002-2003	Advanced Computer Architecture	12	Master	Information Engineering	Italian
2002-2003	Computer Architecture Laboratory	2	Master	Information Engineering	Italian
2002-2003	Programming Fundamentals	3	Master	Digital Economy and E-business	Italian
2002-2003	Operating Systems and Security	3	Master	Management of Financial Inst.	Italian
2002-2003	Computer Architecture	6	Bachelor	Information Engineering	Italian
2002-2003	Informatics for Industrial Applications	6	Bachelor	Information Engineering	Italian
2001-2002	Advanced Computer Architecture	12	Master	Information Engineering	Italian
2001-2002	Computer Architecture Laboratory	2	Master	Information Engineering	Italian
2001-2002	Operating Systems and Security	3	Master	Management of Financial Inst.	Italian
2001-2002	Computer Architecture	6	Bachelor	Information Engineering	Italian
2001-2002	Informatics for Industrial Applications	6	Bachelor	Information Engineering	Italian
2001-2002	Database management	3	Bachelor	Management of Financial Inst.	Italian
2000-2001	Advanced Computer Architecture	12	Master	Information Engineering	Italian
2000-2001	Database management	3	Master	Management of Financial Inst.	Italian
2000-2001	Computer Architecture	6	Bachelor	Information Engineering	Italian
1999-2000	Advanced Computer Architecture	12	Master	Information Engineering	Italian
1999-2000	Computer Architecture	6	Bachelor	Information Engineering	Italian

International Teaching

[1] One ECTS credit corresponds to about 10 hours of teaching and 15 additional hours of personal study of the student.

Prof. Giorgi held invited lectures on "Multi-Core and Many-Core architectures" at the University of Tampere, Finland in October 2013.

21 Coordination of Teaching and Research Activities

- 2014-present **co-founder** of the "CompuThink Lab" as a representative of the "Computer Architecture Lab".
- 2001-2009 **Technological Area Coordinator** for Master in New Technologies and Company Management (University of Siena).
- 2007-present **co-responsible** of the "Computer Architecture Lab", with more than 30 workstations, major computing facilities and having equipment and donations from "AMD", "HP-Labs", "Intel", "NVIDIA", "SECO", "ST-Microelectronics", "Xilinx".

22 Citations by Patents

According to IEEExplore, Roberto Giorgi's papers have been cited by the following patents:

1. Dubrulle, Paul; Goubier, Thierry, and Stéphane Louise, "Speculative and iterative execution of delayed data flow graphs." U.S. Patent Application 10/394,729, filed August 27, 2019.
2. Manet, Philippe; Rousseau, Bertrand, "Tile-based processor architecture model for high-efficiency embedded homogeneous multicore platforms", Patent No. 9275002
3. Manet, Philippe; Rousseau, Bertrand, "A TILE-BASED PROCESSOR ARCHITECTURE MODEL FOR HIGH EFFICIENCY EMBEDDED HOMOGNEOUS MULTICORE PLATFORMS", Patent No. EP2531929
4. Manet, Philippe; Rousseau, Bertrand, "A TILE-BASED PROCESSOR ARCHITECTURE MODEL FOR HIGH EFFICIENCY EMBEDDED HOMOGNEOUS MULTICORE PLATFORMS", Patent No. WO2011092323
5. Rowlands, Joseph B., "BRIDGES PERFORMING REMOTE READS AND WRITES AS UNCACHEABLE COHERENT OPERATIONS", Patent No. 7752281
6. Sano, Barton J.; Rowlands, Joseph B.; Moll, Laurent R.; Gulati, Manu, "SYSTEMS USING MIX OF PACKET COHERENT AND NONCOHERENT TRAFFIC TO OPTIMIZE TRANSMISSION BETWEEN SYSTEMS", Patent No. 7424561
7. Sano, Barton J., "SYSTEM HAVING CONFIGURABLE INTERFACES FOR FLEXIBLE SYSTEM CONFIGURATIONS", Patent No. 7394823
8. Rowlands, Joseph B., "SYSTEM HAVING INTERFACES SWITCH AND MEMORY BRIDGE FOR CC NUMA OPERATION", Patent No. 7266587
9. Sano, Barton J.; Moll, Laurent R.; Gulati, Manu, "SYSTEMS INCLUDING PACKET INTERFACES SWITCHES AND PACKET DMA CIRCUITS FOR SPLITTING AND MERGING PACKET STREAMS", Patent No. 7227870
10. Sano, Barton J.; Rowlands, Joseph B.; Moll, Laurent R.; Gulati, Manu, "SYSTEMS USING MIX OF PACKET COHERENT AND NONCOHERENT TRAFFIC TO OPTIMIZE TRANSMISSION BETWEEN SYSTEMS", Patent No. 7206879
11. Rowlands, Joseph B., "SYSTEM HAVING ADDRESS BASED INTRANODE COHERENCY AND DATA BASED INTERNODE COHERENCY", Patent No. 7003631
12. Rowlands, Joseph B., "L2 CACHE MAINTAINING LOCAL OWNERSHIP OF REMOTE COHERENCY BLOCKS", Patent No. 6993631
13. Rowlands, Joseph B.; Keller, James B., "REMOTE LINE DIRECTORY WHICH COVERS SUBSET OF SHAREABLE CC NUMA MEMORY SPACE", Patent No. 6965973
14. Sano, Barton J.; Rowlands, Joseph B.; Keller, James B.; Moll, Laurent R.; Oner, Koray; Gulati, Manu, "SYSTEM HAVING INTERFACES AND SWITCH THAT SEPARATES COHERENT AND PACKET TRAFFIC", Patent No. 6941406
15. Sano, Barton J.; Oner, Koray; Moll, Laurent R.; Gulati, Manu, "SYSTEM HAVING TWO OR MORE PACKET INTERFACES A SWITCH AND A SHARED PACKET DMA CIRCUIT", Patent No. 6912602
16. Sano, Barton J.; Rowlands, Joseph B.; Keller, James B.; Moll, Laurent R.; Oner, Koray; Gulati, Manu, "SYSTEM HAVING INTERFACES AND SWITCH THAT SEPARATES COHERENT AND PACKET TRAFFIC", Patent No. 6748479
17. Rowlands, Joseph B., "System with address-based intranode coherency and data-based internode coherency", Patent No. EP1363191
18. Lin, Chi-Hung; Liao, Che-Yu; Chuang, Ching-Hsiang; Tung, Shing-Wu, "Hybrid simulation system and method", Patent No. 8645116

19. Attinella, John Eric, "CREATING A PHYSICAL TRACE FROM A VIRTUAL TRACE", Patent No. 7853928
20. Dageville, Benoit; Muthukrishnan, Sambavi; Zait, Mohamed, "TECHNIQUES FOR DETERMINING EFFECTS ON SYSTEM PERFORMANCE OF A MEMORY MANAGEMENT PARAMETER", Patent No. 7539608
21. Gupta, Vidyabhusan, "SYSTEM AND METHOD FOR DESIGNING AND OPTIMIZING THE MEMORY OF AN EMBEDDED PROCESSING SYSTEM", Patent No. 7412369

Appendix HIPEAC01

screenshot-web.archive.org-2022.03.27-06_47_34
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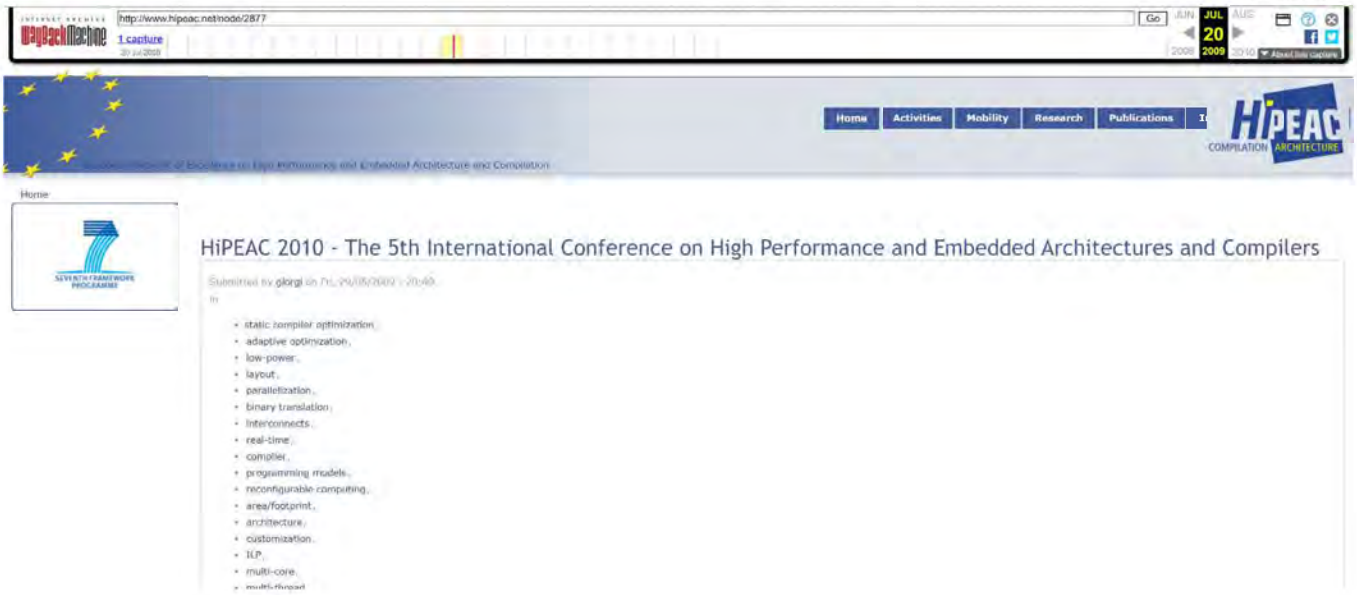

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HiPEAC 2010 - The 5th International Conference on High Performance and Embedded Architectures and Compilers

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in

- static compiler optimization,
- adaptive optimization,
- low-power,
- layout,
- parallelization,
- binary translation,
- interconnects,
- real-time,
- compiler,
- programming models,
- reconfigurable computing,
- area/footprint,
- architecture,
- customization,
- ILP,
- multi-core,
- multi-thread,
- parallel,
- program,
- reliability,
- run-time system,
- simulation and modeling,
- system characteristics,
- tools,
- security,
- memory system,
- I/O subsystem

From 25th Jan 10 To 27th Jan 10

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HiPEAC 2010 http://www.hipeac.net/conference/

The 5th International Conference on
High Performance and Embedded Architectures and Compilers

Pisa, ITALY, January 25-27, 2010

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C A L L F O R P A P E R S

IMPORTANT DATES

Abstract due: July 3 (11.59 PM, PDT), 2009
Paper due: July 10 (11.59 PM, PDT), 2009

SCOPE

The challenges faced by the high-performance general-purpose and embedded worlds are converging. The embedded market evolves rapidly, quickly expanding the capabilities of new devices, and the requirements of these new applications demand technologies that not long ago were in the realm of high-performance computing. Conversely, the energy and cost constraints typical of the embedded world are now also among the most important design criteria for general purpose computing systems. Because performance no longer automatically increases with advances in semiconductor technology, it has become essential to discover new paths to optimize performance, energy and cost across software and hardware.
The HiPEAC conference provides a forum for computer and compiler architects in the field of high performance architecture and compilation for embedded and general-purpose systems, with a special emphasis on cross-cutting research that can be applied to both. The conference aims at the dissemination of advanced scientific knowledge and the promotion of international contacts among scientists from academia and industry.

TOPICS

Topics of interest include, but are not limited to:

* Processor architecture and instruction-level parallelism
* Multi- and many-core architectures (e.g., homogeneous, heterogeneous MPSoC)
* Memory system design and optimization
* Power, performance and cost efficient processor designs
* Domain specific architectures (e.g., Network, Security or Graphics processors)
* Interconnection Networks
* Application specific architectures, ASIPs, accelerators, customized processors
* Reconfigurable architectures and tools for reconfigurable computing
* Compilation techniques for embedded processors
* Dynamic, adaptive and continuous optimization and compilation
* Back-end code generation and scheduling
* Binary translation and optimization
* Compilation and runtime support for multi- and many-core architectures
* Tools and techniques for simulation and performance analysis
* Program and workload characterization and profiling techniques
* Tools for analysis, design, testing and implementation of embedded systems

SUBMISSION

Preferably by July 3, 2009, submit an electronic copy of your paper (in PDF) not exceeding 16 pages and 5.000 words, as explained at:

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Appendix HIPEAC02

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Pisa, Italy

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- Pisa

Deadline: June 16th.

The 5th HiPEAC Conference (HiPEAC 2010) solicits proposals for workshops and tutorials to be organized in conjunction with the main conference. We welcome proposals on topics related to all aspects of research and development, in the field of high performance computer architecture and compilation for embedded systems, as well as general purpose research which is becoming increasingly relevant to the embedded domain.

A complete list of topics of interest can be found on the HiPEAC 2010 web site.

Please submit your workshop or tutorial proposal as an email to Sandro Bartolini (bartolini@dii.unisi.it). Submission deadline is June 16th, 2009 (although we would appreciate it if you could submit a proposal as soon as you can).

For workshops, please include concisely the following information in your proposal (no more than 2 pages):

- Title of the workshop
- Organizers and their affiliations
- Sample call for papers, including the workshop's main topics
- Expected duration of the workshop; i.e., 1/2 day, full day
- Expected workshop format, i.e., keynote+talks+panel, keynote+talks, talks only, etc.
- Planned number of papers and attendance (based on historical data or experience)
- Event sponsors

For tutorials, please include the following information in your proposal (no more than 2 pages):

- Title of the tutorial
- Organizers, presenters, and their affiliations
- Abstract of the tutorial
- A list of topics to be covered and some of their related bibliography
- Expected duration of the tutorial; i.e., 1/2 day or full day
- Expected tutorial format, i.e., talks, or talks + demo, etc.
- If the tutorial was previously held, the location (i.e., which conference), date, and number of attendees at the last tutorial

For additional information, please contact the HiPEAC 2010 Workshops and Tutorials chair (Sandro Bartolini, bartolini@dii.unisi.it) and/or visit the conference webpage.

- Login or register to post comments

Appendix WWW01

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WWW Computer Architecture Page

Designed by Derek Hower, Luke Yen, Min Xu, Milo Martin †, Doug Burger*, and Mark Hill

Computer Architecture Group
Computer Sciences Department
University of Wisconsin-Madison

†Computer and Information Science
University of Pennsylvania

*Department of Computer Sciences
University of Texas at Austin

Conferences

Google Map of conference locations - Created by Luis Ceze and Karin Strauss

2010 September
- PACT 2010 - Parallel Architectures and Compilation Techniques (PACT) in Vienna
- MCSoC-1 - 5th International Symposium on Embedded Multicore Systems-on-Chip, in conjuction with ICPP-2010

June
- ISCA 2010 - ISCA 2010: International Symposium on Computer Architecture
- SOCC 2010 ACM Symposium on Cloud Computing

May
- NOCS 2010 - 4th ACM/IEEE International Symposium on Networks-on-Chip

April
- LCTES 2010 - ACM SIGPLAN/SIGBED Conference on Languages, Compilers and Tools for Embedded Systems
- CGO 2010 - 8th International IEEE/ACM International Symposium on Code Generation and Optimization
- CF 2010 - ACM International Conference on Computing Frontiers
- CAC 2010 - 10th Workshop on Communication Architecture for Clusters

March
- ASPLOS XV - Fifteenth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS '10)
- Embedded Systems at 25th ACM SAC - Track on Embedded Systems at 25th ACM Symp. on Applied Computing

February
- PDP 2010 - 18th Euromicro Parallel, Distributed and network-based Processing 2010, Pisa, Italy

WWW Computer Architecture Page

Designed by Derek Hower, Luke Yen, Min Xu, Milo Martin†, Doug Burger*, and Mark Hill

Computer Architecture Group
Computer Sciences Department
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†Computer and Information Science
University of Pennsylvania

*Department of Computer Sciences
University of Texas at Austin

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Conferences

Google Map of conference locations - Created by Luis Ceze and Karin Strauss

2010 September
- PACT 2010 - Parallel Architectures and Compilation Techniques (PACT) in Vienna
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June
- ISCA 2010 - ISCA 2010: International Symposium on Computer Architecture
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April
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February
- PDP 2010 - 18th Euromicro Parallel, Distributed and network-based Processing 2010, Pisa, Italy

January
- HiPEAC 2010 - 5th International Conference on High Performance and Embedded Architectures and Compilers
  - GROW 2010 - 2nd International Workshop on GCC Research Opportunities (GROW'10)
  - Multiprog 2010 - Third Hipeac Workshop on Programmability Issues for Multi-Core Computers
  - WRC'10 - 4th HiPEAC Workshop on Reconfigurable Computing
  - SMART'10 - 4th Workshop on Statistical and Machine learning approaches to ARchitecture and compilaTion
- HPCA 2010 - 16th International Symposium on High-Performance Computer Architecture
  - LCA-GPGPU 1 - First workshop on language, compiler, and architecture support for GPGPU
  - SAW-1 workshop - 1st Workshop on SoC Architectures, Aeeclerators and Workloads
  - Workshop on High Performance Virtualization - Workshop on High Performance Virtualization: Architecture, Systems, Software and Analysis

2009 December
- MICRO - 42 - The 42nd Annual IEEE/ACM International Symposium on Microarchitecture (MICRO)
  - WBIA 2009 - Workshop on Binary Instrumentation Systems and Analaysis
  - NoCArc 2009 - Second International Workshop on Network on Chip Architectures

November
- CBHPC 2009 - 2009 Workshop on Component-Based High Performance Computing (CBHPC 2009)

October
- ANCS 2009 - ACM/IEEE Symposium on Architectures for Networking and Communications Systems
- SBAC - 09 - The 21st International Symposium on Computer Architecture and High Performance Computing
- ICCD 2009 - Int'l Conf. on Computer Design (ICCD)
- IISWC 2009 - IEEE International Symposium on Workload Characterization

September
- CFP: PACT'09 - The Eighteenth International Conference on Parallel Architectures and Compilation Techniques (PACT)
  - 10th MEDEA Workshop - MEmory performance: DEaling with Applications, systems and architecture
- MCSoC-09 - 4th Intl. Symposium on Embedded Multicore Systems-on-Chip

August
- HPPC 2009 - 3rd full-day Workshop on Highly Parallel Processing on a Chip
- HeteroPar'2009 - 7th International Workshop on Algorithms, Models and Tools for Parallel Computing on Heterogeneous Platforms (CFP)

July
- SDMAS'09 - Third International Workshop on Scalable Distributed and Multi/Many-core Applications and Systems
- SAMOS IX - International Symposium on Systems Architectures, Modeling and Simulation
- DAC - 46 - 46th Design Automation Conference
  - SASP -7 - 7th IEEE Symposium on Application Specific Processors

June
- CATARS-09 -Second Workshop on Compiler and Architectural Techniques for Application Reliability and Security -- To be held in conjunction with the39th International Conference on Dependable Systems and Networks (DSN)
- ICS-23 - ICS is the premier international forum for the presentation of research results in high-performance computing systems.
  - StreamPPOT - Embedded Streaming: Parallel Programming, Optimizations and Tools
- ISCA-2009
  - AMAS-BT - Arch/Uarch support for binary translation workshop
  - WIOSCA - 2009 -Fifth Annual Workshop on the Interaction between Operating Systems and Computer Architecture
  - WDDD - 2009 - The Annual Workshop on Duplicating, Deconstructing, and Debunking
  - PESPMA 2009 - 2nd Workshop on Parallel Execution of Sequential Programs on Multi-core Architectures
  - BiC 2009 - Workshop on Biomedicine in Computing: Systems, Architectures, and Circuits
  - CARD-2009 - Workshop on Computer Architecture Research Directions (with ISCA-09)
  - WEED 2009 - Workshop on Energy-efficient Design
- ARITH-19 - 19th IEEE International Symposium on Computer Arithmetic
- ISPDC'2009 - 8th International Symposium on Parallel and Distributed Computing
- ICS'09 - 23rd International Conference on Supercomputing - International Conference on Supercomputing

May
- ACM International Conference on Computing Frontiers
- JSSPP'09 - 14th Workshop on Job Scheduling Strategies for Parallel Processing
- RAW-2009 - 16th Reconfigurable Architectures Workshop

April
- ISPASS-2009 - International Symposium on Performance Analysis of Systems and Software
  - UCAS-5 - Fifth International Workshop on Unique Chips and Systems
  - Net-val-1 - The First Workshop on Performance Evaluation of Next-Generation Networks

March
- EMBS Track at ACM SAC 2009 - Track on EMBEDDED SYSTEMS: Applications, Solutions, and Techniques at ACM 24th Symp. on Applied Computing
- ASPLOS-14
  - GPGPU-2 - Workshop on General-Purpose Computation on Graphics Processing Units
  - WISH'09 - 1st Workship on Integrating Solid-State Memory into the Storage Hierarchy

February
- WHTRA - Workshop for HyperTransport Research and Applications
- HPCA 2009
  - DPC-1 - 1st JILP Data Prefetching Championship
  - CAECW-12 - The Twelfth Workshop on Computer Architecture Evaluation using Commercial Workloads

January
- SPEC 2009 Workshop
- International conference on VLSI Design and Embedded Systems
- HiPEAC-09 - 4th International Conference on High Performance and Embedded Architectures and Compilers
  - RAPIDO'09 - 1st Workshop on Rapid Simulation and Performance Evaluation: Methods and Tools (RADIDO'09)
  - SMART'09 - 3rd Workshop on Statistical and Machine learning approaches applied to ARchitectures and compilaTion

- Multiprog2007 - Second Hipeac Workshop on Programmability Issues for Multi-Core Computers

Archives:

- **Prior Years**

WWW Computer Architecture Page
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Computer Architecture Group
Computer Sciences Department
University of Wisconsin-Madison
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Appendix HIPEAC03

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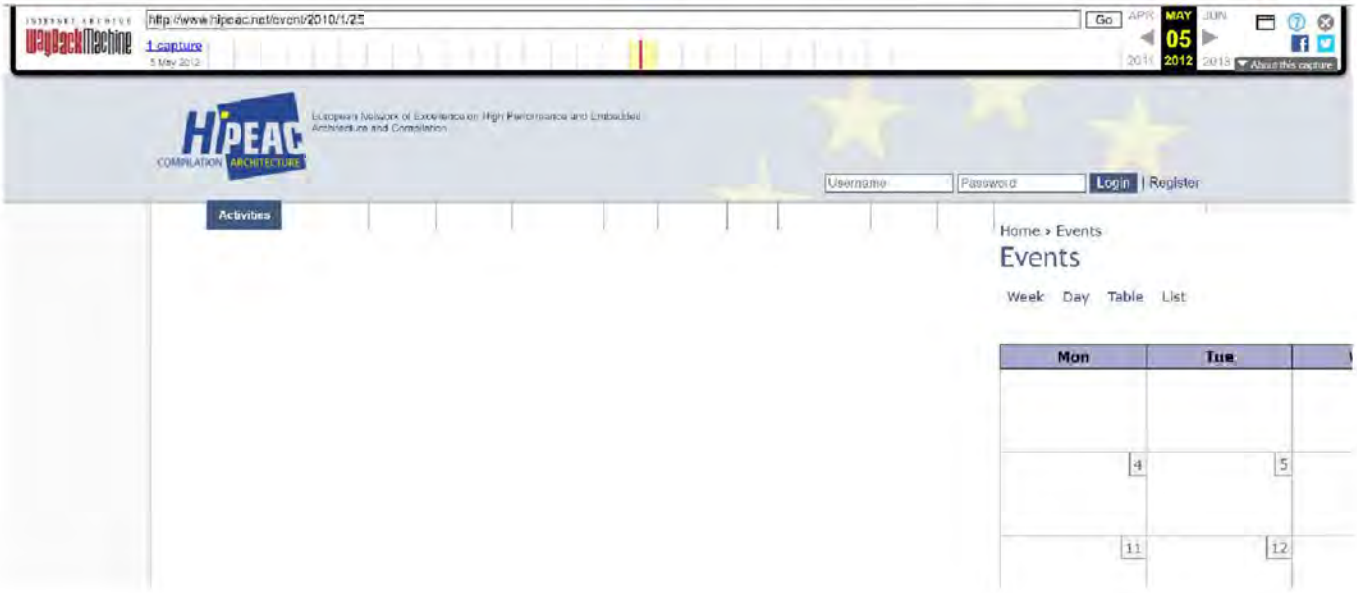

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25 ***HiPEAC 2010 - The 5th International Conference on High Performance and Embedded Architectures and Compilers*** all day	26 ***HiPEAC 2010 - The 5th International Conference on High Performance and Embedded Architectures and Compilers*** all day	27 ***HiPEAC 2010 - The 5th International Conference on High Performance and Embedded Architectures and Compilers*** End: 27/01/2010	28	29	30	31

Appendix PARTICIPANTS01

HÖGSKOLAN I HALMSTAD

Publications

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» Specifying Run-time Reconfiguration in Processor Arrays using High-...

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Specifying Run-time Reconfiguration in Processor Arrays using High-level language

- Zain-ul-Abdin
  Halmstad University, School of Information Science, Computer and Electrical Engineering (IDE), Halmstad Embedded and Intelligent Systems Research (EIS), Embedded Systems (CERES).
  (CC-Lab)
  ORCID ID: 0000-0002-4932-4036
- Svensson, Bertil
  Halmstad University, School of Information Science, Computer and Electrical Engineering (IDE), Halmstad Embedded and Intelligent Systems Research (EIS), Embedded Systems (CERES).
  (CC-Lab)
  ORCID ID: 0000-0001-6625-6533

2010 (English)

In: WRC 2010: 4th HiPEAC Workshop on Reconfigurable Computing, Pisa, 2010, p. 1-10

Conference paper, Published paper (Refereed)

Abstract [en]
The adoption of run-time reconfigurable parallel architectures for high-performance embedded systems is constrained by the lackof a unified programming model which can express both parallelism and reconfigurability. We propose to program an emerging class of reconfigurable processor arrays by using the programming model of occam-pi and describe how the extensions of channel direction specifiers, mobile data, dynamic process invocation, and process placement attributes can be used to express run-time reconfiguration in occam-pi. We present implementations of OCT algorithm to demonstrate the applicability of occam-pi to express reconfigurability. We concluded that occam-pi appears to be a suitable programming model for programming run-time reconfigurable processor arrays.

Place, publisher, year, edition, pages
Pisa, 2010. p. 1-10

National Category
Computer Sciences

Identifiers
URN: urn:nbn:se:hh:diva-5442
OAI: oai:DiVA.org:hh-5442
DiVA, id: diva2:345708

Conference
HiPEAC Workshop on Reconfigurable Computing

Available from: 2010-09-22 **Created:** 2010-08-26 **Last updated:** 2018-01-12

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In thesis
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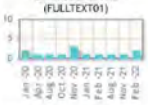

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http://www.ece.uah.edu/cv/Milenkovic_CV_March16_Web.pdf
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Tools

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3

Curriculum Vitae

Aleksandar MILENKOVIĆ

Electrical and Computer Engineering Department
University of Alabama in Huntsville
Huntsville, AL 35899

Phone: (256) 824 6830
Fax: (256) 824 6803
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Research Interests

Computer architecture, embedded systems, high-performance computing systems, performance evaluation, energy-efficient computing, secure processors, mHealth systems and applications, wireless sensor networks, reconfigurable computing, and VLSI.

Education

10/1999 Ph.D. in Computer Engineering and Science, **The University of Belgrade** . . . . . Belgrade, Serbia
Dissertation title: Cache injection in bus-based shared memory multiprocessors
Advisor: Prof. Veljko Milutinovic

2/1997 **M.Sc.** in Computer Engineering and Science, **The University of Belgrade** . . . . . Belgrade, Serbia
Thesis title: A quantitative analysis of wiring lengths in
2D and 3D VLSI implementations of 3D systolic arrays
Advisor: Prof. Veljko Milutinovic

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2/1997 **M.Sc.** in Computer Engineering and Science, **The University of Belgrade** . . . . . Belgrade, Serbia
Thesis title: A quantitative analysis of wiring lengths in
2D and 3D VLSI implementations of 3D systolic arrays
Advisor: Prof. Veljko Milutinovic
GPA: 10/10

4/1994 **Dipl. Ing.** in Electrical Engineering, **The University of Belgrade** . . . . . Belgrade, Serbia
Project: Design of an HDL based simulator for processor i960KB
GPA: 9.45/10

Work Experience

08/14 – present Professor of Electrical and Computer Engineering
The University of Alabama in Huntsville . . . . . Huntsville, AL

05/07 – 08/14 Associate Professor of Electrical and Computer Engineering
The University of Alabama in Huntsville . . . . . Huntsville, AL

08/01 – 05/07 Assistant Professor of Electrical and Computer Engineering
The University of Alabama in Huntsville . . . . . Huntsville, AL

12/00 – 08/01 Assistant Professor
School of Computing, Dublin City University . . . . . Dublin, Ireland

05/00 – 12/00 Assistant Professor
School of Electrical Engineering, The University of Belgrade . . . . . Belgrade, Serbia

10/94 – 05/00 Research/Teaching Assistant
School of Electrical Engineering, The University of Belgrade . . . . . Belgrade, Serbia

Research

The University of Alabama in Huntsville . . . . . Huntsville, AL
Laboratory for Advanced Computer Architectures and Systems (LaCASA), Founder, Directing research
Web: http://lacasa.uah.edu

mHealth: Computing infrastructure for mobile health and wellness monitoring, Co-founder, Directing research
Web: http://portal.mhealth.uah.edu

04/15 – present Hardware supported security enhancements in cyber-physical systems

08/12 – present Energy-efficiency in modern computing systems

Evaluating impact of frequency scaling in high-end processors

Energy-efficient in mobile computing platforms (developed a setup for measurement-based profiling of smartphone applications; developed analytical models for file data file uploads and downloads, developed environment of optimizing data transfers utilizing compression utilities).

08/12 – present mHealth – Computing Infrastructure for Mobile Health and Wellness Monitoring

Developing new wearable systems for mobility assessment (e.g., Smart Button)

Developing new algorithms for characterization of medical tests for mobility assessment (e.g., Smart Time-Up-Go test, Smart 30-seconds Chair Stand Test, and others)

08/08 – present Tracing and Debugging in Embedded Systems

Developed new techniques for program tracing and debugging in embedded systems
Developed new techniques for program tracing in multicores

08/03 – 06/10 Secure processors

Developed new architectural extensions to counter software and physical attacks
Developed hardware/software mechanisms for supporting code and data integrity and confidentiality

08/04 – 08/11 Wireless sensor networks

TinyHMS: Tiny wireless sensors for health monitoring (co-lead with Dr. Jovanov)
Energy efficiency in wireless distributed sensor networks (co-lead with Dr. Raskovic, Dr. Jovanov)
Reconfigurable wireless sensor platforms, IP cores for security, error correction, DSP

08/02 – present Techniques for Architecture Exploration (Simulation, Measurement, Performance Analysis)

08/02 – 08/04 Architectural analysis using on-chip performance monitoring registers and microbenchmarks

05/02 – 08/03 Cache replacement policies in high-performance and embedded processors

The University of Belgrade . . . . . Belgrade, Serbia

01/97 – 12/99 Techniques for tolerating memory latency in SMPs (cache injection, data forwarding, prefetching)

01/98 – 12/98 Multiprocessor simulation (led development of trace-driven simulator Limes)

10/94 – 10/96 Cache coherence protocols in SMPs/DSMs (Lead: Prof. V. Milutinovic)

10/94 – 03/97 Potentials of 3D VLSI

Publications

P. Patents

P#1. [USPTO'09] Frank E. Levine, **Aleksandar Milenković**, Milena Milenković,
"Data and Instruction Address Compression," USPTO #7,496,902, issued on February 24, 2009 (filed March 2005).

A. Patent Applications

A#1. [USPTO'13b] Emil Jovanov, **Aleksandar Milenković**, Mladen Milosevic,
"Systems and methods for automatically quantifying mobility," Patent Application, UAH-0118 February 2013, submitted to USPTO in February 2014.

PA. Provisional Patent Applications/UAH Disclosure

PA#2. [USPTO'13a] **Aleksandar Milenković**, Mladen Milosevic, Emil Jovanov, "Smartphone Instrumentation and Monitoring of Wheelchairs and Wheeled Apparatuses," Provisional patent applications UAH-0117,

January 2013.

J. Refereed Journal Articles

The University of Alabama in Huntsville . . . . . Huntsville, AL

J#24. [Elsevier.JSA'15] Amrish K. Tewar, Albert R. Myers, **Aleksandar Milenković**, "mcfTRaptor: Toward unobtrusive on-the-fly control-flow tracing in multicores," *Journal of Systems Architecture*, Vol. 61, No. 10, November 2015, pp. 601-614, doi: 10.1016/j.sysarc.2015.07.005.

J#23. [IEEE.TC'14] Vladimir Uzelac, **Aleksandar Milenković**, Milena Milenković, Martin Burtscher, "Using Branch Predictors and Variable Encoding for On-the-fly Program Tracing," *IEEE Transactions on Computers*, Vol. 63, No. 4, April 2014, pp. 1008-1020, doi: 10.1109/TC.2012.267.

J#22. [ACM.TECS'13] Vladimir Uzelac, **Aleksandar Milenković**, "Hardware-Based Load Value Trace Filtering for On-the-Fly Debugging," *ACM Transactions on Embedded Computing Systems*, Vol. 12, No. 2s, May 2013, doi: 10.1145/2465787.2465799.

J#21. [Springer.JMS'11] Emil Jovanov, **Aleksandar Milenković**, "Body Area Networks for Ubiquitous Healthcare Applications: Opportunities and Challenges," *Journal of Medical Systems*, Vol. 35, No. 5, October 2011, pp. 1245-1254, doi: 10.1007/s10916-011-9661-x.

J#20. [IEEE.TC'11] **Aleksandar Milenković**, Vladimir Uzelac, Milena Milenković, Martin Burtscher "Caches and Predictors for Real-time, Unobtrusive, and Cost-Effective Program Tracing in Embedded Systems," *IEEE Transactions on Computers*, Vol. 60, No. 7, July 2011, pp. 992-1005. doi: 10.1109/TC.2010.146.

J#19. [IEEE.TCASI'10] Ashkan Ashrafi, Reza Adhami, **Aleksandar Milenković**, "A Direct Digital Frequency Synthesizer Based on the Quasi Linear Interpolation Method," *IEEE Transactions on Circuits and Systems I*, Vol. 57, Issue 4, April 2010, pp. 863-872, doi: 10.1109/TCSI.2009.2027645.

J#18. [Elsevier.MICPRO'09] Austin Rogers, **Aleksandar Milenković**, "Security extensions for integrity and confidentiality in embedded processors," *Microprocessors and Microsystems*, Vol. 33, Issues 5-6, August 2009, pp. 333-414, doi: 10.1016/j.micpro.2009.06.002.

J#17. [Wiley.CAEE'08] Jovan Djordjevic, Bosko Nikolic, Tanja Borozan, **Aleksandar Milenković**, "CAL2: Computer Aided Learning in Computer Architecture Laboratory," *Computer Applications in Engineering Education*, Vol. 16, Issue 3, 2008, pp. 172-188, doi: 10.1002/cae.20141.

J#16. [ACM.TOMACS'07] **Aleksandar Milenković,** Milena Milenković, "An Efficient Single-Pass Trace Compression Technique Utilizing Instruction Streams," Vol. 17, Issue 1, *ACM Transactions on Modeling and Computer Simulation*, January 2007, ACM Press, pp. 1-27, doi: 10.1145/1189756.1189758.

J#15. [Elsevier. COMPCOMM'06] **Aleksandar Milenković**, Chris Otto, Emil Jovanov, "Wireless Sensor Networks for Personal Health Monitoring: Issues and an Implementation," *Computer Communications (Special issue: Wireless Sensor Networks: Performance, Reliability, Security, and Beyond)*, Vol. 29, No. 13-14, Elsevier, 2006, pp. 2521-2533, doi: 10.1016/j.comcom.2006.02.011.

J#14. [IOS.JEC'06] **Aleksandar Milenković**, Milena Milenković, Emil Jovanov, "An Efficient Runtime Instruction Block Verification for Secure Embedded Systems," *Journal of Embedded Computing*, Vol. 2, No. 1, IOS Press, Amsterdam, The Netherlands, September 2006, pp. 57-76.

J#13. [Rinton.JMM'06] Chris Otto, **Aleksandar Milenković**, Corey Sanders, Emil Jovanov, "System Architecture of a Wireless Body Area Sensor Network for Ubiquitous Health Monitoring," *Journal of Mobile Multimedia*, Vol. 1, No. 4, 2006, pp. 307-326.

J#12. [IEEE.TE'05] Jovan Djordjevic, Bosko Nikolic, **Aleksandar Milenković**, "Flexible Web-based Educational System for Teaching Computer Architecture and Organization," *IEEE Transactions on Education*, Vol. 48, No. 2, 2005, pp 264-273, doi: 10.1109/TE.2004.842918.

J#11. [ACM.CAN'05] Milena Milenković, **Aleksandar Milenković**, Emil Jovanov, "Using Instruction Block Signatures to Counter Code Injection Attacks," *Computer Architecture News*, Vol. 33, No. 1, March 2005, pp. 108-117, doi: 10.1145/1055626.1055641.

J#10. [BioMED.JNER'05] Emil Jovanov, **Aleksandar Milenković**, Chris Otto, Piet C. de Groen, "A Wireless Body Area Network of Intelligent Motion Sensors for Computer Assisted Physical Rehabilitation," *Journal of NeuroEngineering and Rehabilitation*, 2:6, March 1, 2005, doi:10.1186/1743-0003-2-6. [http://www.jneuroengrehab.com/content/2/1/6]

J#9. [Wiley.SPE'04] Milena Milenković, **Aleksandar Milenković**, Jeffrey Kulick, "Microbenchmarks for Determining Branch Predictor Organization," *Software Practice & Experience*, Vol. 34, No. 4, April 2004, pp. 465-487, doi: 10.1002/spe.v34:5.

J#8. [IEEE.CAL'03] **Aleksandar Milenković**, Milena Milenković, "Stream-Based Trace Compression," *Computer Architecture Letters*, Vol. 2, Sep. 2003, doi: 10.1109/L-CA.2003.7.

J#7. [Elsevier.MICPRO'02] **Aleksandar Milenković**, Veljko M. Milutinovic "A Performance Evaluation of Cache Injection in Bus-based Shared Memory Multiprocessors," *Microprocessors and Microsystems*, Vol. 26, No. 2, March 2002, pp. 51-61, doi: 10.1016/S0141-9331(01)00146-6.

The University of Belgrade . . . . . Belgrade, Serbia

J#6. [IEEE.CONC'00] **Aleksandar Milenković**, "Achieving High Performance in Bus-Based Shared Memory Multiprocessors," *IEEE Concurrency*, Vol. 8, No. 3, July-September 2000, pp. 36-44, doi: 10.1109/4434.865891.

J#5. [IEEE.MICRO'00] Jovan Djordjevic, **Aleksandar Milenković**, and Nenad Grbanovic, "An Integrated Environment for Teaching Computer Architecture," *IEEE Micro*, Vol. 20, No. 3, 2000, pp. 66-74, doi: 10.1109/40.846311.

J#4. [Elsevier.MEJ'98] **Aleksandar Milenković** and Veljko M. Milutinovic, "A Quantitative Analysis of Wiring Lengths in 2D and 3D VLSI," *Microelectronics Journal*, Vol. 29, no. 6, 1998, pp. 313-322, doi: 10.1016/S0026-2692(97)00043-8.

J#3. [IASTED.IJCA'97b] Salim Lakhani, Y. Wang, **Aleksandar Milenković**, and Veljko M. Milutinovic, "3D Convolution on a 3D Systolic Arrays: Another Point of View," *International Journal of Computers and Applications*, Vol. 19, no. 3, 1997, pp. 130-134.

J#2. [IASTED.IJCA'97a] Salim Lakhani, Veljko M. Milutinovic, **Aleksandar Milenković**, D. Meyer, and Branislava Perunicic, "Stochastic Modeling and Analysis of Propagation Delays in Processing Units," *International Journal of Computers and Applications*, Vol. 19, no. 2, 1997, pp. 61-69.

J#1. [Elsevier.MEJ'96] Salim Lakhani, Y. Wang, **Aleksandar Milenković**, and Veljko M. Milutinovic, "2D Matrix Multiplication on a 3D Systolic Arrays," *Microelectronics Journal*, Vol. 27, no.1, February 1996, pp. 11-22, doi: 10.1016/0026-2692(95)00008-9.

C. Refereed Conference/Workshop Papers

The University of Alabama in Huntsville . . . . . Huntsville, AL

C#56. [IEEE.HealthCom'15b] Armen Dzhagaryan, **Aleksandar Milenković**, "On Effectiveness of Lossless Compression in Transferring mHealth Data," in the *Proceedings of the 17th International Conference on E-health, Networking, Application & Services (HealthCom'15)*, October 14-17, 2015, Boston, MA.

C#55. [IEEE.HealthCom'15a] Armen Dzhagaryan, **Aleksandar Milenković**, Emil Jovanov, Mladen Milosevic, "Smart Button: A Wearable System for Assessing Mobility in Elderly," in the *Proceedings of the 17th International Conference on E-health, Networking, Application & Services (HealthCom'15)*, October 14-17, 2015, Boston, MA.

C#54. [IEEE.ICCCN'15] Armen Dzhagaryan, **Aleksandar Milenković**, Martin Burtscher, "Quantifying Benefits of Lossless Compression Utilities on Modern Smartphones," to appear in *Proceedings of the 24th International Conference on Computer Communications and Networks (IC3N'15)*, August 3-6, Las Vegas, NV. (acceptance rate ~25%, **best paper nominee**)

C#53. [ACM.SE'14] Armen Dzhagaryan, **Aleksandar Milenković**, "Impact of Thread and Frequency Scaling on Performance and Energy in Modern Multicores: A Measurement-based Study, " in the *Proceedings of the 52nd Annual ACM Southeast Conference (ACMSE'14)*, March 28-29, Kennesaw,

GA.

C#52. [IEEE.MASCOTS'13] **Aleksandar Milenković**, Armen Dzhagaryan, Martin Burtscher, "Performance and Energy Consumption of Lossless Compression/Decompression Utilities on Mobile Computing Platforms," in the *Proceedings of the IEEE 21st International Symposium on Modeling, Analysis and Simulation of Computer and Telecommunication Systems (MASCOTS 2013)*, August 14-16, 2013, San Francisco, CA. (44 out of 163, ~27% acceptance rate).

C#51. [IEEE.EMBC'13] Emil Jovanov, Mladen Milosevic, **Aleksandar Milenković**, "Mobile System for Assessment of Physiological Response to Posture Transitions," in the *Proceedings of the 35th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC'13)*, July 3-7, Osaka, Japan.

C#50. [IEEE.BSN'13b] Mladen Milosevic, Emil Jovanov, **Aleksandar Milenković**, "Quantifying Timed-Up-and-Go Test: A Smartphone Implementation," in the *Proceedings of the 10th Annual Body Sensor Networks Conference 2013 (BSN'13)*, May 6-9, Boston, MA, pp. 302-307.

C#49. [IEEE.BSN'13a] **Aleksandar Milenković**, Mladen Milosevic, Emil Jovanov, "Smartphones for Smart Wheelchairs," in the *Proceedings of the 10th Annual Body Sensor Networks Conference 2013 (BSN'13)*, May 6-9, Boston, MA, pp. 404-409.

C#48. [IEEE.ISPASS'13] Armen Dzhagaryan, **Aleksandar Milenković**, Martin Burtscher, "Energy Efficiency of Lossless Data Compression on a Mobile Device: An Experimental Evaluation," in the *Proceedings of the 2013 International Symposium on Performance Analysis of Systems and Software (ISPASS'13)*, April 21-23, Austin, TX, pp. 126-127 (poster paper, 23+12p out of 87).

C#47. [ACM.SE'13] Mladen Milosevic, Armen Dzhagaryan, Emil Jovanov, **Aleksandar Milenković**, "An Environment for Automated Power Measurements on Mobile Computing Platforms," in the *Proceedings of the 51st Annual ACM Southeast Conference (ACMSE'13)*, April 04-06, Savannah, GA.

C#46. [IEEE.bioCAS'11] Mladen Milosevic, Emil Jovanov, **Aleksandar Milenković**, "Rapid Processor Customization for Design Optimization: a Case Study of ECG R-Peak Detection," in the *Proceedings of the 2011 Annual IEEE Biomedical Circuits and Systems (BioCAS) Conference*, November 14-16, San Diego, CA, pp. 209-212. (31o+72p/199; ~56% acceptance rate)

C#45. [IEEE.SSST'11] Nason Tackett, Emil Jovanov, **Aleksandar Milenković**, "An Implementation of Time Synchronization in Low-Power Wireless Sensor Networks," in the *Proceedings of the 2011 Joint IEEE International Conference on Industrial Technology (ICIT-2011) and 43rd Southeastern Symposium on System Theory (SSST-2011)*, March 2011, Auburn, AL.

C#44. [ACM.CASES'10b] Vladimir Uzelac, **Aleksandar Milenković**, "Hardware-Based Data Value and Address Trace Filtering Techniques," in the *Proceedings of the International Conference on Compilers, Architectures and Synthesis of Embedded Systems* (CASES'10), October 24-29, Scottsdale, AZ, pp. 117-126. (**best paper award**)

C#43. [ACM.CASES'10a] Vladimir Uzelac, **Aleksandar Milenković**, Milena Milenković, Martin Burtscher, "Real-time Unobtrusive Program Execution Trace Compression Using Branch Predictor Events," in the *Proceedings of the International Conference on Compilers, Architectures and Synthesis of Embedded Systems (CASES'10)*, October 24-29, Scottsdale, AZ, pp. 97-106.

C#42. [IEEE.ICCD'09] Vladimir Uzelac, **Aleksandar Milenković**, Milena Milenković, Martin Burtscher "Real-time, Unobtrusive, and Efficient Program Execution Tracing with Stream Caches and Last Stream Predictors," in the *Proceedings of the 27th IEEE International Conference on Computer Design (ICCD'09)*, October 4-7, Lake Tahoe, CA. (70 out of 200, ~35% acceptance rate)

C#41. [IEEE.DAC'09] Vladimir Uzelac, **Aleksandar Milenković**, "A Real-Time Program Trace Compressor Utilizing Double Move-to-Front Method," in the *Proceedings of the 46th Design Automation Conference (DAC'09)*, July 26-31, San Francisco, CA, pp. 738-743. (148 out of 682, ~21% acceptance rate)

C#40. [IEEE.ERSA'09] Austin Rogers, **Aleksandar Milenković**, "An Implementation of Security Extensions for Data Integrity and Confidentiality in Soft Core Processors," in the *Proceedings of the Engineering of*

Reconfigurable Systems and Algorithms - ERSA'09, July 13-16, Las Vegas, NV.

C#39. [IEEE.ISPASS'09] Vladimir Uzelac, **Aleksandar Milenković**, "Experiment Flows and Microbenchmarks for Reverse Engineering of Branch Predictor Structures," in the *Proceedings of the 2009 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS'09)*, April, 2009, Boston, MA. (~25% acceptance rate)

C#38. [IEEE.SSST'09] Dejan Raskovic, Venkatramana Revuri, David Giessel, **Aleksandar Milenković**, "Embedded Web Server for Wireless Sensor Networks," in the *Proceedings of the 41st IEEE Southeastern Symposium on System Theory (SSST'09)*, Tullahoma, TN, USA, March 15-17, 2009, pp. 154-158.

C#37. [IEEE.SSST'08] Joel L. Wilder, Vladimir Uzelac, **Aleksandar Milenković**, Emil Jovanov, "Runtime Hardware Reconfiguration in Wireless Sensor Networks," in the *Proceedings of the 40th IEEE Southeastern Symposium on System Theory (SSST'08)*, New Orleans, LA, March 2008, pp. 154-158.

C#36. [IEEE.SSST'08] Joel L. Wilder, **Aleksandar Milenković**, Emil Jovanov, "Smart Wireless Vehicle Detection System," in the *Proceedings of the 40th IEEE Southeastern Symposium on System Theory (SSST'08)*, New Orleans, LA, March 2008, pp. 159-163.

C#35. [IEEE.ICCD'07] Austin Rogers, Milena Milenković, **Aleksandar Milenković**, "A Low Overhead Hardware Technique for Software Integrity and Confidentiality," in the *Proceedings of the 2007 IEEE International Conference on Computer Design (ICCD'07)*, Olympic Valley, CA, October 7-10, 2007, pp. 113-120. (~30% acceptance rate)

C#34. [IEEE.ISCAS'07] Ashkan Ashrafi, **Aleksandar Milenković**, Reza Adhami, "A 1GHz Direct Digital Frequency Synthesizer Based on the Quasi-Linear Interpolation Method," in the *Proceedings of the 2007 IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 2766-2769.

C#33. [IEEE.DCC'07] Milena Milenkovic, **Aleksandar Milenković**, Martin Burtscher, "Algorithms and Hardware Structures for Unobtrusive Real-Time Compression of Instruction and Data Address Traces," in the *Proceedings of the 2007 Data Compression Conference (DCC'07)*, Snowbird, UT, March 27–29, IEEE Computer Society, pp. 55-65.

C#32. [IEEE.ISSS-MDBS'06] Chris A. Otto, Emil Jovanov, **Aleksandar Milenković**, "A WBAN-based System for Health Monitoring at Home," in the *Proceedings of the 3rd IEEE-EMBS International Summer School and Symposium on Medical Devices and Biosensors (ISSS-MDBS 2006)*, September 2006.

C#31. [ACM.CASES'05] Milena Milenković, **Aleksandar Milenković**, Emil Jovanov, "Hardware Support for Code Integrity in Embedded Processors," in the *Proceedings of the International Conference on Compilers, Architectures and Synthesis of Embedded Systems (CASES'05)*, San Francisco, CA, Sept. 24 – Sept. 27, 2005, pp. 55-65. (~30% acceptance rate)

C#30. [IEEE.EMBS'05b] Emil Jovanov, **Aleksandar Milenković**, Chris Otto, Piet de Groen, Bruce Johnson, Steve Warren, Gueseppe Taibi, "A WBAN System for Ambulatory Monitoring of Physical Activity and Health Status: Applications and Challenges," in the *Proceedings of the 27th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBS)*, Shanghai, China, September 2005.

C#29. [IEEE.EMBS'05a] Steve Warren, Jeffrey Lebak, Jianchu Yao, Jonathan Creekmore, **Aleksandar Milenković**, Emil Jovanov, "Interoperability and Security in Wireless Body Area Network Infrastructures," in the *Proceedings of the 27th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBS)*, Shanghai, China, September 2005.

C#28. [IEEE.SSST'05b] **Aleksandar Milenković**, Milena Milenković, Emil Jovanov, Dennis Hite, Dejan Raskovic, "An Environment for Runtime Power Monitoring of Wireless Sensor Network Platforms," in the *Proceedings of the 37th IEEE Southeastern Symposium on System Theory (SSST'05)*, Tuskegee, AL, March 2005, pp. 406-410.

C#27. [IEEE.SSST'05a] Dennis Cox, Emil Jovanov, **Aleksandar Milenković**, "Time Synchronization for ZigBee Networks," in the *Proceedings of the 37th IEEE Southeastern Symposium on System Theory (SSST'05), Tuskegee*, AL, March 2005, pp. 135-138.

C#26. [ACM.SE'05]	Chris Otto, John P. Gober, Reggie W. McMurtrey, **Aleksandar Milenković**, Emil Jovanov, "An Implementation of Hierarchical Signal Processing on a Wireless Sensor in TinyOS Environment," in the *Proceedings of the 43rd ACM Southeastern Conference*, Kennesaw, GA, March 2005, Vol. 2, pp. 49-53.
C#25. [ACM.WASSA'04]	Milena Milenković, **Aleksandar Milenković**, Emil Jovanov, "Using Instruction Block Signatures to Counter Code Injection Attacks," in the *Proceedings of the Workshop on Architectural Support for Security and Anti-Virus (WASSA)* (held in conjunction with 11th ASPLOS), Boston, Massachusetts, USA, October 9, 2004, pp. 104–113.
C#24. [IEEE.EMBS'04]	Emil Jovanov, **Aleksandar Milenković**, S. Basham, D. Clark, D. Kelley, "Reconfigurable Intelligent Sensors for Health Monitoring: A Case Study of Pulse Oximeter Sensor," in the *Proceedings of the 26th Annual International Conference of the IEEE Engineering in Medicine and Biology Society, San Francisco*, California, September 2004, pp. 4759–4762.
C#23. [ACM.SE'04d]	Swathi T. Gurumani, **Aleksandar Milenković**, "Execution Characteristics of SPEC CPU2000 Benchmarks: Intel C++ vs. Microsoft VC++", in the *Proceedings of the 42nd ACM Southeast Conference*, April 2-3, 2004, Huntsville, AL, pp. 261-266.
C#22. [ACM.SE'04c]	Milena Milenković, **Aleksandar Milenković**, Emil Jovanov, "A Framework For Trusted Instruction Execution Via Basic Block Signature Verification," in the *Proceedings of the 42nd ACM Southeast Conference*, April 2-3, 2004, Huntsville, AL, pp. 191-196.
C#21. [ACM.SE'04b]	H. Al-Zoubi, **Aleksandar Milenković**, Milena Milenković, "Performance Evaluation of Cache Replacement Policies for the SPEC CPU2000 Benchmark Suite," in the *Proceedings of the 42nd ACM Southeast Conference*, April 2-3, 2004, Huntsville, AL, pp. 267-272.
C#20. [ACM.SE'04a]	Zexin Pan, Wendy D. Pan, **Aleksandar Milenković**, "Complexity-Distortion Tradeoffs in Variable Complexity 2-D DCT," in the *Proceedings of the 42nd ACM Southeast Conference, April 2-3, 2004, Huntsville*, AL, pp. 460-465.
C#19. [IEEE.WWC'03]	**Aleksandar Milenković**, Milena Milenković, "Exploiting Streams in Instruction and Data Address Trace Compression," in the *Proceedings of the IEEE 6th Annual Workshop on Workload Characterization*, Austin, TX, USA, October 27, 2003, pp. 99-107.
C#18. [ISCA.PDCS'03]	**Aleksandar Milenković**, Milena Milenković, Jeffrey Kulick, "N-Touple Compression: A Novel Method for Compression of Branch Instruction Traces," in the *Proceedings of the 16th International Conference on Parallel and Distributed Computing Systems (PDCS-2003)*, Reno, Nevada, USA, August 13-15, 2003, pp. 49-55.
C#17. [IEEE.MSE'03]	**Aleksandar Milenković**, David Fatzer, "Teaching IP Core Development: An Example," in the *Proceedings of the 2003 International Conference on Microelectronic Systems Education*, Anaheim, California, USA, June 1-2, 2003, pp. 16-17.
C#16. [IEEE.SSST'03]	**Aleksandar Milenković**, Milena Milenković, and Nelson Barnes, "A Performance Evaluation of Memory Hierarchy in Embedded Systems," in the *Proceedings of the 35th IEEE Southeastern Symposium on System Theory*, Morgantown, West Virginia, USA, 16-18 March 2003, pp. 427-431.
C#15. [DoD.HPC'02]	Kenneth G. LeSueur, Emil Jovanov, and Aleksandar Milenkovic, "Lookup Table Based Real-Time Non-Uniformity Correction Of Infrared Scene Projectors," in the *Proceedings of the 12th Annual DoD High Performance Computing Modernization User Group Conference*, Austin, Texas, June 2002.
C#14. [WWD'02]	Milena Milenković, **Aleksandar Milenković**, and Jeffrey Kulick, "Demystifying Intel Branch Predictors," in the *Proceedings of the Workshop on Duplicating, Deconstructing, and Debunking (held in conjunction with 29th ISCA)*, Anchorage, Alaska, May 2002.
C#13. [WCAE'02]	**Aleksandar Milenković**, Bosko Nikolic, Jovan Djordjevic, "CASTLE: Computer Architecture Self-Testing and Learning System," in the *Proceedings of the Workshop on Computer Architecture Education (held in conjunction with 29th ISCA)*, Anchorage, Alaska, May 2002.

C#12. [IEEE.MASCOTS'00] Darko Marinov, Davor Magdic, **Aleksandar Milenković**, Jelica Protic, Igor Tartalja, and V. M. Milutinovic, "SCOWL: A Tool for Characterization of Parallel Workload and its Use on Splash-2 Application Suite," in the *Proceedings of the 8th International Symposium on Modeling, Analysis and Simulation of Computer and Telecommunication Systems (MASCOTS)*, San Francisco, California, August/September 2000, pp. 207-213.

C#11. [Springer.EuroPar'00] **Aleksandar Milenković** and Veljko M. Milutinovic, "Cache Injection: A Novel Technique for Tolerating Memory Latency in Bus-Based SMPs," *Lecture Notes in Computer Science, vol. 1900,* in the *Proceedings of the 6th International Euro-Par Conference*, Munich, Germany, August/September 2000, pp. 558-566.

C#10. [Springer.PPAM'99] Igor Ikodinovic, **Aleksandar Milenković**, Veljko M. Milutinovic, and Davor Magdic, "Limes: A Multiprocessor Simulation Environment for PC Platforms," in the *Proceedings of the 3rd International Conference on Parallel Processing and Applied Mathematics (PPAM'99)*, Kazimierz Dolny, Poland, September 14-17, 1999, pp. 398-412.

C#9. [WCAE'99] Jovan Djordjevic, **Aleksandar Milenković**, Ivan Todorovic, and Darko Marinov, "CALKAS: A Computer Architecture Learning and Knowledge Assessment System," in the *Proceedings of the 4th Annual Workshop on Computer Architecture Education, (held in conjunction with 5th HPCA)*, Orlando, Florida, USA, January 1999.

C#8. [IEEE.APADS'98] **Aleksandar Milenković** and Veljko M. Milutinovic, "Cache Injection on Bus-based Multiprocessors," in the *Proceedings of the Workshop on Advances in Parallel and Distributed Systems, (held in conjunction with 17-th IEEE Symposium on Reliable Distributed Systems),* West Lafayette, Indiana, October 1998.

C#7. [ISCEE'98] Jovan Djordjevic, Miroslav Bojovic, and **Aleksandar Milenković**, "An Integrated Educational Environment for Computer Architecture and Organization," in the *Proceedings of the International Symposium on Computer Employment and Education (ISCEE'98)*, Amiens, France, October 1998.

C#6. [WCAE'98isca] Jovan Djordjevic, **Aleksandar Milenković**, and Slobodan Prodanovic, "A Hierarchical Memory System Environment," in the *Proceedings of the Workshop on Computer Architecture Education (held in conjunction with 25th ISCA)*, Barcelona, Spain, June 1998.

C#5. [WCAE'98hpca] Jovan Djordjevic, **Aleksandar Milenković**, Nenad Grbanovic, and Miroslav Bojovic, "An Educational Environment for Teaching a Course in Computer Architecture and Organization," in the *Proceedings of the 4th Annual Workshop on Computer Architecture Education, (held in conjunction with 4th HPCA)*, Las Vegas, Nevada, January 1998.

C#4. [IEEE.HICSS'98b] Darko Marinov, Davor Magdic, **Aleksandar Milenković**, Jelica Protic, Igor Tartalja, and V. M. Milutinovic, "An Approach to Characterization of Parallel Applications for DSM Systems," in the *Proceedings of the 31st HICSS*, IEEE Computer Society Press, Vol. 7, January 1998, pp. 782-784.

C#3. [IEEE.HICSS'98a] **Aleksandar Milenković** and Veljko M. Milutinovic, "Lazy Prefetching," in the *Proceedings of the 31st HICSS*, IEEE Computer Society Press, Vol. 7, January 1998, pp. 780-782.

C#2. [IEEE.MIEL'97] **Aleksandar Milenković** and Veljko M. Milutinovic, "A Quantitative Analysis of Wiring Lengths in 2D and 3D VLSI Implementations of 3D Systolic Arrays," in the *Proceedings of the MIEL'97*, Vol. 2, Nis, Yugoslavia, September 1997, pp. 833-837.

C#1. [IEEE.MASCOTS'97] Veljko M. Milutinovic, **Aleksandar Milenković**, and Gad Sheaffer, "The Cache Injection Control Architecture: Initial Performance Analysis," in the *Proceedings of the 5th International Symposium on Modeling, Analysis and Simulation of Computer and Telecommunication Systems (MASCOTS)*, Haifa, Israel, January 1997.

B. Books

The University of Belgrade . . . . . Belgrade, Serbia

B#1. [AM.IntroCE] Jelica Protic, **Aleksandar Milenković**, *Introduction to Computer Engineering: Problems and Solutions* (in Serbian), Academic Mind, Belgrade, Serbia, 2000.

BC. Book Chapters

The University of Alabama in Huntsville . . . . . Huntsville, AL

BC#5. [JBL'14] Mladen Milosevic, Emil Jovanov, **Aleksandar Milenkovic**, Mobile Health Applications, in *Applied Clinical Informatics in Nursing,* editors: Susan Alexander, Karen Frith, Haley Hoy, Jones and Bartlett Learning, Burlington, MA, 2014, ISBN-13: 9781284049961.

BC#4 [Wiley.Ecy.CSE'09] **Aleksandar Milenković**, Addressing: Direct and Indirect, *Wiley's Encyclopedia of Computer Science and Engineering*, Editor: Benjamin Wah, Wiley, 2009.

BC#3. [Elsevier'08] Dejan Rašković, **Aleksandar Milenković**, Dr. Piet C. De Groen, Emil Jovanov, *From Telemedicine To Ubiquitous M-Health: The Evolution Of E Health Systems*, in *Biomedical Information Technology*, Edited by David Dagan Feng, Elsevier, 2008.

The University of Belgrade . . . . . Belgrade, Serbia

BC#2. [Wiley'00b] Igor Ikodinovic, Zoran Dimitrijevic, Davor Magdic, **Aleksandar Milenković**, Jelica Protic, and Veljko Milutinovic, "Limes: A Multiprocessor Simulation Environment for PC Platforms," in *Surviving the Design of Microprocessor and Multimicroprocessor Systems* by V. Milutinovic, John Wiley & Sons, Inc., USA, 2000.

BC#1. [Wiley'00a] Darko Marinov, Davor Magdic, **Aleksandar Milenković**, Jelica Protic, and Veljko Milutinovic, "The Scowl Tool for PC-Based Characterization of Parallel Applications," in *Surviving the Design of Microprocessor and Multimicroprocessor Systems* by V. Milutinovic, John Wiley & Sons, Inc., USA, 2000.

O. Other Publications (Editor Reviewing)

The University of Alabama in Huntsville . . . . . Huntsville, AL

O#10. [ACM.XRDS'13] Mladen Milosevic, **Aleksandar Milenkovic,** Emil Jovanov, "mHealth @ UAH: computing infrastructure for mobile health and wellness monitoring," XRDS: Crossroads, The ACM Magazine for Students, Vol. 20, No. 2, December 2013, pp. 43-49. doi: 10.1145/2539269.

O#9. [CSCN'12] Mladen Milosevic, Michael T. Shrove, **Aleksandar Milenkovic**, Emil Jovanov, "Smartphone Application Framework for Research in Wellness and Healthcare, " in the *Proceedings of the 2012 Southeastern Workshop on Cognitive Sensing, Computing & Networking and their Applications in Human-Cyber-Physical Systems*, Tuscaloosa, AL, August 2012, pp. 77.

O#8. [IEEE.IFLSA'11] Emil Jovanov, Mladen Milosevic, **Aleksandar Milenkovic**, Michael T. Shrove, Karen Frith, Fay Anderson, "Personalized Assessment of Occupational Stress of Nurses," in the *Proceedings of the 9th International Forum on Life Science Automation*, Washington, DC, December 2011, pp. 25.

O#7. [IEEE.EMBSunc'11] Michael T. Shrove, Mladen Milosevic, Bruce Johnson, **Aleksandar Milenkovic**, Emil Jovanov, "iCareWell: Real-time Wellness Monitor," *1st IEEE EMBS Unconference on Wearable & Ubiquitous Technology for Health and Wellness*, Boston, MA, USA, August 30, 2011, pp. 24.

O#6. [Redstone'07] **Aleksandar Milenković**, Jeffrey Kulick, Rhonda Gaede, "Tamper Protection of Hardware/Software Systems Using Dynamic Re-configuration of FPGAs,"*Reconfigurable Systems, Microsystems, and Nanotechnology Conference*, May 8-10, 2007, Redstone Arsenal, AL.

O#5. [Redstone'07] Joel Wilder, Vladimir Uzelac, **Aleksandar Milenković**, Emil Jovanov "Wireless Sensor Networks for Updating Reprogrammable Logic Designs in Real-time," *Reconfigurable Systems, Microsystems, and Nanotechnology Conference*, May 8-10, 2007, Redstone Arsenal, AL.

O#4. [Un.of.Houston'07] Xiaofang Chen, Emil Jovanov, **Aleksandar Milenković**, "A Real-Time Step Detection Using A Single 3d Accelerometer On The Upper-Trunk," *Proceedings of the Mini-Symposium on Digital Healthcare at 24th Annual Houston Conference on Biomedical Engineering Research*, Houston, TX, February 2007, pp. 239, 2007.

The University of Belgrade . . . . . Belgrade, Serbia

O#3. Jovan Djordjevic, **Aleksandar Milenković**, Igor Todorovic, Darko Marinov,

[IEEE.TCCA'00]	"CALKAS: A Computer Architecture Learning and Knowledge Assessment System," *IEEE TCCA Newsletter*, July 2000, pp. 26–29.
O#2. [IEEE.TCCA'99b]	Jovan Djordjevic, **Aleksandar Milenković**, Nenad Grbanovic and Miroslav Bojovic, "An Educational Environment for Teaching a Course in Computer Architecture and Organization," *IEEE TCCA Newsletter*, July 1999, pp. 5–7.
O#1. [IEEE.TCCA'99a]	Jovan Djordjevic, **Aleksandar Milenković** and Slobodan Prodanovic, "A Hierarchical Memory System Environment," *IEEE TCCA Newsletter*, February 1999, pp. 60–62.

Invited lectures, colloquia

The University of Alabama in Huntsville . . . . . Huntsville, AL

[T#10.NCHPAD'13]	**Aleksandar Milenković,** Emil Jovanov, "*mHealth – Computing Infrastructure for Mobile Health and Wellness Monitoring*," the National Center for Health, Physical Activity and Disability in Birmingham, AL, 2013 (research collaborative between UAB and Lakeshore Foundation, http://nchpad.org/).
[T#9.UAH'13]	**Aleksandar Milenković,** Emil Jovanov, "*mHealth – Computing Infrastructure for Mobile Health and Wellness Monitoring*," Honors Lecture Series, Huntsville, AL, March 21st, 2013.
[T#8.UB'12]	**Aleksandar Milenković,** "*Embedded Computer Systems: Debuggability and Energy Efficiency,*" University of Belgrade, Belgrade, Serbia, June 29, 2012. (over 40 attendees).
[T#7.Tensilica'09]	**Aleksandar Milenković,** "*Algorithms and Hardware Structures for Real-time, Unobtrusive, and Cost-effective Program Tracing*," (over 50 attendees), Tensilica, San Jose, CA, July 2009.
[T#6.UB'09]	**Aleksandar Milenković,** "*Computer Architectures for Increased Programmers' Productivity*," University of Belgrade, Serbia, (over 50 attendees), June 2009.
[T#5.Cornell'07]	**Aleksandar Milenković**, "*Instruction and Data Address Trace Compression*," Cornell University, May 2007.
[T#4.UB'05]	**Aleksandar Milenković**, "*Fundamental Metrics in Computer Engineering*," University of Belgrade, Serbia and Montenegro, May 2005 **(sponsored by WUS Austria's Brain Gain Program)**.
[T#3.UB'05]	**Aleksandar Milenković**, "*LaCASA Laboratory Research Overview*," University of Belgrade, Serbia and Montenegro, May 2005 **(sponsored by WUS Austria's Brain Gain Program)**.
[T#2.TxState'05]	**Aleksandar Milenković**, "*LaCASA Laboratory Research Overview,*" Texas State University, San Marcos, April 2005.
[T#1.UTK'02]	**Aleksandar Milenković,** "*Architecture-Aware Compilers*," University of Tennessee in Knoxville, May 2002.

Grants

RG. Research Grants

The University of Alabama in Huntsville . . . . . Huntsville, AL

09/01/2015-08/31/2016	David Coe, Jeffrey Kulick, Sun-il Kim, Letha Etzkorn, Aleksandar Milenkovic, **Dielectric: Lightweight Virtualization for Insulating Cyber Physical and Cloud Applications**, NSA/DHS, total: $299,622.
09/01/2012-08/31/2016	**Aleksandar Milenković (PI),** Martin Burtscher (coPI), Real-Time Unobtrusive Tracing in Multicore Embedded Systems, **NSF Award No. CNS-1217470**, UAH portion $321,388, total: $494,348.
08/15/2012-12/31/2015	**Aleksandar Milenković (PI),** Emil Jovanov (coPI), II-NEW: mHealth - Computing Infrastructure for Mobile Health and Wellness Monitoring, **NSF, Award No. CNS-1205439**, total: $232,723.
09/01/2009-12/31/2010	**Aleksandar Milenković (PI),** II-NEW: Acquisition of FPGA-Based Emulation Hardware for Research

in Computer Systems Architecture, **NSF, Award No. CNS-0855237**, total: $161,868.

08/15/2009-02/28/2010 Jeffrey Kulick (PI), Rhonda Gaede (coPI), Earl Wells (coPI), **Aleksandar Milenković** (coPI), Performance Analysis, Subcontract: Performance Analysis and Compiler Optimization on Multicore Processors, SAIC Inc. contract, $9,374 Milenkovic's share, total: ~$250,000.

09/01/2008 – 08/31/09 **Aleksandar Milenković (PI),** Enabling Computer Architecture Research in Multi-Core Era @ UAHuntsville, ECE Research Enhancement, total: $20,000.

09/01/2007 – 08/31/2010 John Gregory (PI), Robert Lindquist (coPI), **Aleksandar Milenković (coPI)**, Junpeng Guo (coPI), Emil Jovanov (coPI), Claudiu Muntele (coPI), Jennifer English (coPI), David Coe (coPI), Robert Zimmerman, "Device Realization for Sensor Health Monitoring of Space Transportation Systems," **NASA 07-EPSCoR-0003**, total: $748,500.

08/01/2004 – 07/31/2007 Dejan Raskovic (PI), **Aleksandar Milenković (coPI)**, Denise Thorsen (coPI), Emil Jovanov (coPI), "IIS: Energy Efficiency in Distributed Sensor Networks," **NSF Award no. 0434156**, total: $434,600 = $199,660+$100,000+$135,000 (two supplemental awards).

01/2002 – 09/2002 **Aleksandar Milenković (PI),** "Cache Replacement Policies for Future Processors," UAH Mini-Grant Award, total: $5,170.

TG. Teaching Grants

The University of Alabama in Huntsville . . . . . Huntsville, AL

04/04/2013 – 04/03/2014 **Aleksandar Milenković (PI)**, Earl Wells (coPI), CUDA Teaching Center, NVIDIA, April 2013 – April 2014; unrestricted gift in money and equipment (~ $5,000).

01/02/2003 – 09/30/2003 **Aleksandar Milenković (PI),** "Building Systems on a Chip Using IP Soft Cores," UAH Instructional Mini-Grant ($3,000).

01/02/2002 – 09/30/2002 **Aleksandar Milenković (PI),** "CASTLE: Computer Architecture Self-Testing and Learning," UAH Instructional Mini-Grant ($3,000).

EG. Equipment Grants (Hardware/Software)

The University of Alabama in Huntsville . . . . . Huntsville, AL

05/2015 **Aleksandar Milenkovic (PI), Hardware Donation – Intel,** 10 Galielo 2 Boards (~500).

02/2014 **Aleksandar Milenković (PI), Hardware Donation – Intel;** 10 Intel Galileo Boards (~ $500).

05/10/2013 – 05/09/2014 **Aleksandar Milenković (PI), Software Donation – Tensilica;** Xtensa Processor Generator (XPG) login; (10 floating licenses).

09/10/2013 – 09/09/2014 **Aleksandar Milenković (PI), Software Donation - Intel;** Intel® Software Development Suite Classroom use license; 25 Floating seats

12/2013 **Aleksandar Milenković (PI), Hardware Donation – Altera;** DE2-115, DE0-Nano boards (~$400).

08/15/2013 **Aleksandar Milenković (PI), Software Donation – Altera;** Quartus 2 and Nios II EDS Software Development Suites; 25 Floating seats;

09/10/2012 – 09/09/2013 **Aleksandar Milenković (PI), Software Donation - Intel;** Intel® Software Development Suite Classroom use license; 25 Floating seats

05/10/2012 – 05/09/2013 **Aleksandar Milenković (PI), Software donation – Tensilica;** Xtensa Processor Generator (XPG) login; (10 floating licenses)

05/10/2011 – 05/09/2012 **Aleksandar Milenković (PI), Software donation – Tensilica;** Xtensa Processor Generator (XPG) login; (10 floating licenses)

09/10/2011 **Aleksandar Milenković (PI), Software donation - Texas Instruments;** Code Composer, Academic Edition, (100 floating licenses)

09/10/2011 – **Aleksandar Milenković (PI), Software Donation - Intel;** Intel® Software Development Suite

09/09/2012	Classroom use license; 25 Floating seats
09/10/2010 – 09/09/2011	**Aleksandar Milenković (PI), Software Donation - Intel;** Intel® Software Development Suite Classroom use license; 25 Floating seats
11/2009	**Aleksandar Milenković (PI); Xilinx**; Xilinx XUP-FPGA-LX155T; Xilinx University Program LX155T FPGA chip donation for BEE3 system (4 per system) 8
03/01/2010 – 02/28/2011	**Aleksandar Milenković (PI), BEEcube**; BEECube Platform Studio; 1 year time based single node-lock seat software license
09/10/2009 – 09/09/2010	**Aleksandar Milenković (PI), Intel;** Intel® Software Development Suite Classroom use license; 25 Floating seats
01/18/2009 – 05/05/2010	**Aleksandar Milenković (PI),** Tensilica; Xtensa Processor Generator (XPG) login;
04/01/2003 – 09/30/2003	**Aleksandar Milenković (PI),** Xilinx Donation (Software) ($4,490)
04/01/2002 – 03/13/2003	**Aleksandar Milenković (PI),** Xilinx Donation (Hardware) ($244,295)

IG. Grants from Industry

The University of Belgrade . . . . . Belgrade, Serbia

03/99 – 09/99	PTT Network analysis and capacity planning (JP PTT Serbia)
01/00 – 06/00	Development analysis (HIP - Cybernetic Center, Pancevo, Serbia, 2000)
01/97 – 03/98	Reflective memory optimization for DSM-based disk IO pumps (Encore, FL)
01/96 – 09/96	DARTS: Digital Audio System (RTS, Belgrade, Serbia)

Teaching Experience

The University of Alabama in Huntsville . . . . . Huntsville, AL

Taught Graduate (5xx, 6xx, 7xx) and Undergraduate Courses (3xx, 4xx), Created a new undergraduate course Introduction to Embedded Computer Systems (CPE 323), Created a new Embedded Systems Laboratory (CPE 325), Developed Advanced Computer Systems Architecture (CPE 631), Developed VLSI Design (CPE/EE 427/527).

S'09	CPE 730 ST: Computer Architecture
F'14, F'09, S'08	CPE 619 Modeling and Analysis of Computer and Communication Systems `http://www.ece.uah.edu/~milenka/cpe619-08S/`
S'16, S'15, S'14, S'13, S'12, S'11 S'10, F'08, S'08, S'07, S'06, S'05, S'04, S'03, S'02, F'01	CPE 631 Advanced Computer Systems Architecture `http://www.ece.uah.edu/~milenka/cpe631-10S/`
F'04, F'02, S'02	CPE 626 Advanced VLSI Systems `http://www.ece.uah.edu/~milenka/cpe626-04F/`
F'15, F'13	CPE 423/523 Hardware/Software Co-design
F'15, F'14, S'14, F'13, SM'13, S'13, F'12, S'12, S'11, S'10, F'09, S'09, F'08, F'07	CPE 323 Introduction to Embedded Computer Systems `http://www.ece.uah.edu/~milenka/cpe323-10S/`
S'07, F'06, S'06, F'05, S'05, S'04, F'03	CPE/EE 521 (CPE/EE 421) Microcomputers `http://www.ece.uah.edu/~milenka/cpe421-06S/`
S'14, F'12, F'10 F'06, F'05, F'04, F'03, F'02, F'01	CPE/EE 527 (CPE/EE 427) VLSI Design I `http://www.ece.uah.edu/~milenka/cpe427-06S/`

Sm'03, Sm'02	CPE/EE 522 (CPE/EE 422) Advanced Logic Design `http://www.ece.uah.edu/~milenka/cpeee_422522_03S/`
S'03, S'02	CPE/EE 528 (CPE/EE 428) VLSI Design II `http://www.ece.uah.edu/~milenka/cpe528-03S/`

School of Computing, Dublin City University . . . . . Dublin, Ireland
Taught Undergraduate Courses

S'01	CA 226 Advanced Computer Architectures
S'01	CA 100 Programming Languages

School of Electrical Engineering, University of Belgrade . . . . . Belgrade, Serbia
Taught Undergraduate Courses

S'00	Fundamentals of Computer Engineering
S'00	Multiprocessors

Assisted in teaching graduate and undergraduate courses (gave oral recitations, prepared and graded class projects and exams). Developed laboratory exercises. Supervised undergraduate senior project designs. Co-supervised seven undergraduate 5th year theses. Co-led the development of an educational environment for teaching computer architecture: RTL design, graphic simulator, and Web based system for knowledge assessment.

Y'95 – Y'00	Fundamentals of Computer Engineering (Freshman level)
Y'94 – Y'00	Computer Architecture (Junior level)
Y'94 – Y'00	VLSI (Senior level)
Y'94 – Y'00	Microprocessors and interfacing (Senior level)

Students

Current Students

The University of Alabama in Huntsville . . . . . Huntsville, AL

Name	*Degree*	*Expected graduation*
Richard Tuggle	Ph.D. Student	?
Armen Dzhagaryan	Ph.D. Candidate	F'16
Mounika Ponugoti	M.S. Student	F'16
Ryan Cowart	M.S. Student	S'17

Theses/Dissertations Supervised

The University of Alabama in Huntsville . . . . . Huntsville, AL

	Student	Title	
[AT'15]	Amrish K. Tewar	Experimental Evaluation of Techniques for Capturing and Compressing Hardware Traces in Multicores	Master thesis, The University of Alabama in Huntsville, March 2015.
[AM'14]	Albert Myers	A Binary Instrumentation Tool Suite for Capturing and Compressing Traces for Multithreaded Software	Master thesis, The University of Alabama in Huntsville, March 2014.
[MM'13]	Mladen Milosevic	Energy-Efficient Distributed Wearable Physiological	Doctoral Dissertation, The

	(principal advisor Dr. Jovanov)	Monitoring: Framework and Implementations	University of Alabama in Huntsville, May 2013.
[AD'13]	Armen Dzhagaryan	Performance And Energy Efficiency Of Common Compression/Decompression Utilities: An Experimental Study In Mobile And Workstation Computer Platforms	Master thesis, The University of Alabama in Huntsville, February 2013.
[VU'10]	Vladimir Uzelac	Algorithms and Hardware Structures for Real-time Compression of Program Traces	Doctoral Dissertation, The University of Alabama in Huntsville, March 2010.
[JS'10]	John Stenmark	Program Execution Trace Compression Analysis Tool	Master thesis, The University of Alabama in Huntsville, February 2010.
[AR'10]	Austin Rogers	Designing Cost-Effective Secure Processors For Embedded Systems: Principles, Challenges, And Architectural Solutions	Doctoral Dissertation, The University of Alabama in Huntsville, January 2010.
[VU'08]	Vladimir Uzelac	Microbenchmarks and Mechanisms For Reverse Engineering Of Modern Branch Predictor Units	Master thesis, The University of Alabama in Huntsville, January 2008.
[RT'07]	Richard Tuggle	Multiple Path Management Protocol For the Real-time Distributed Control of Sensors and Effectors	Master thesis, The University of Alabama in Huntsville, October 2007.
[AR'07]	Austin Rogers	Low Overhead Hardware Techniques for Software and Data Integrity and Confidentiality in Embedded Systems	Master thesis, The University of Alabama in Huntsville, September 2007.
[CO'06]	Chris Otto (*principal advisor Dr. Jovanov*)	An Implementation of a Wireless Body Area Network for Ambulatory Health Monitoring	Master thesis, The University of Alabama in Huntsville, March 2006.
[MM'05]	Milena Milenkovic (*principal advisor Dr. Jovanov*)	Architectures for Run-time Verification of Code Integrity	Doctoral Dissertation, The University of Alabama in Huntsville, March 2005.

Alumni

The University of Alabama in Huntsville . . . . . Huntsville, AL

Name	*Degree*	*First job*	*Graduated*
Amrish K. Tewar	M.S. in CPE	Mathworks, Boston, MA	S'15
Albert Myers	M.S. in CPE	AMRDEC, Huntsville, AL	S'14
Sunny Patel (won the Outstanding CPE and Outstanding College of Engineering Student Awards)	B.Sc. in CPE	CFD Research, Huntsville, AL	S'14
Mladen Milosevic	Ph.D. in CPE	Philips Research, Briarclif, NY	Sm'13
Wil C. Gilmore	B.Sc. in CPE	Lockheed Martin, Huntsville, AL	S'13
Fasil Mulat	B.Sc. in EE	Grad student at Auburn University	S'11
Nason Tackett	B.Sc. in CPE	Hear Technologies, Huntsville, AL	S'10
Vladimir Uzelac	PhD in CPE	Tensilica, San Jose, CA	S'10
John Stenmark	M.S. in CPE	Dynetics, Huntsville, AL	S'10

Austin Rogers	Ph.D. in CPE	Dynetics, Huntsville, AL	S'10
Elise Haley (won CoE SURF award in Summer'06)	B.Sc. in CPE	Boeing, Huntsville, AL	S'07
Jim Marks (won UAH SURF in Summer'06)	B.Sc. in CPE	Raytheon, Huntsville, AL	S'07
John Bland	B.Sc. in CPE	Software Engineering Directorate, Huntsville, AL	S'07
Chris Otto (*advisor Dr. Jovanov*) (won 2nd award at Alabama Launchpad 2007)	M.S. in CPE	Lewis Innovative, Inc., Huntsville, AL; Halo Research	S'06
David Wachira (won CoE, UAH SURF award in Sm'05)	B.Sc. in EE	Adtran, Huntsville, AL	F'05
Brian Trotter	B.Sc. in EE	Dynetics, Huntsville, AL	F'05
Milena Milenkovic *(advisor Dr. Jovanov)*	Ph.D. in CPE	IBM, Austin, TX	S'05
Austin Rogers	B.Sc. in EE	Dynetics, Huntsville, AL	S'04

The University of Belgrade . . . . . Belgrade, Serbia

Zoran Dimitrijevic (co-advised with Dr. Milutinovic)	B.Sc. in CPE	Ph.D. student at UCSB (now with Google)	S'00
Igor Ikodinovic	B.Sc. in CPE	University of Belgrade (now with AMD, Canada)	S'99
Darko Marinov (co-advised with Dr. Milutinovic)	B.Sc. in CPE	Ph.D. student at MIT (now professor at UIUC, USA)	S'99
Davor Magdic (co-advised with Dr. Milutinovic)	B.Sc. in CPE	Ph.D. student at UCSB (now with Texas Instruments)	S'98

Professional Service

Editorial board

[Hindawi. IJDSN] International Journal of Distributed Sensor Networks (06/2010 – 06/2013)

Reviewer, Journals

[ACM.TECS'16] ACM Transactions on Embedded Systems, February 2016.

[ACM.TACO'15] ACM Transactions on Architecture and Code Optimization, October 2015.

[ACM.TECS'15] ACM Transactions on Embedded Systems, February 2015.

[IIS.JISE'14] Academia Sinica Institute of Information Science, Journal of Information Science and Engineering, September 2014

[IEEE.Sensors'14] IEEE Sensors Journal, August 2014

[ACM.TECS'14] ACM Transactions on Embedded Computing Systems, March 2014.

[Hidawi. IDJSN'12/'13] International Journal of Distributed Sensor Networks

[IOS.JAISE'13] Journal of Ambient Intelligence and Smart Environments (IOS Press), February 2012.

[IEEE.TITB'12] IEEE Transactions on Information Technology in BioMedicine; April 2012, October 2012.

[IEEE.TE'11]	IEEE Transactions on Education, November 2011.
[ACM.TECS'11]	ACM Transactions on Embedded Computer Systems, November 2011.
[ACM.TSN'11]	ACM Transactions on Sensor Networks, June 2011.
[IEEE.TITB'11]	IEEE Transactions on Information Technology in BioMedicine; March 2011.
[IEEE.TE'10]	IEEE Transactions on Education; September 2010.
[IEEE.TBCAS'10]	IEEE Transactions of Biomedical Circuits and Systems, August 2010.
[InderScience. IJHPSA'10]	International Journal of High Performance Systems Architecture (IJHPSA), September 2009.
[IEEE.TITB'09]	IEEE Transactions on Information Technology in Biomedicine, August 2009.
[IEEE.TC'09]	IEEE Transactions on Computers, May 2009.
[IEEE.TVLSI'09]	IEEE Transactions on VLSI, May 2009.
[ACM.CCR'09]	ACM Sigcomm Computer Communications Review, April 2009.
[IEEE.TITB'09]	IEEE Transactions on Information Technology in Biomedicine, April 2009.
[IEEE.TMC'08]	IEEE Transactions on Mobile Computing, September 2008.
[IEEE.TC'08]	IEEE Transactions on Computers, September 2008.
[IEEE.TE'08]	IEEE Transactions on Education, June 2008.
[IEEE.TITB'08]	IEEE Transactions on Information Technology in Biomedicine, April 2008.
[IEEE.TE'08]	IEEE Transactions on Education, February 2008.
[Elsevier.MEJ'08]	Elsevier Microelectronics Journal, January 2008.
[IEEE.TBCS'07]	IEEE Transactions on Biomedical Circuits and Systems. September 2007.
[IEEE.TITB'07]	IEEE Transactions on Information Technology in Biomedicine, May 2007.
[ACM.TCS'07]	ACM Transactions on Computer Systems, May 2007.
[Elsevier. COMMCOMP'06]	Elsevier Computer Communications, November 2006.
[IEEE.TVLSI'06]	IEEE Transactions on VLSI, October 2006.
[IEEE.TITB'06]	IEEE Transactions on Information Technology in Biomedicine, October 2006.
[IE.IJSN'06]	International Journal on Sensor Networks, Indersciences Enterprise, Ltd., August 2006.
[IEEE.TC'06]	IEEE Transactions on Computers, August 2006.
[IEEE.TE'06]	IEEE Transactions on Education, August 2006.
[IEEE.TVLSI'06]	IEEE Transactions on VLSI, June 2006.
[ACM.TACO'06]	ACM Transactions on Architecture and Code Optimization, April 2006.
[IEEE.TC'06]	IEEE Transactions on Computers, February 2006.
[IEEE.TE'05]	IEEE Transactions on Education, November 2005.
[Elsevier. COMMCOMP'05]	Elsevier Computer Communications, October 2005.
[IEEE.COMM'05]	IEEE Communications Magazine, September 2005.
[IOS.JEC'05]	Journal on Embedded Computing, March 2005.
[IEEE.TVLSI'05]	IEEE Transactions on VLSI, March 2005.
[IEEE.TE'04]	IEEE Transactions on Education, November 2004.

[IEEE.TVLSI'04]	IEEE Transactions on VLSI, October 2004.
[IEEE.TE'04]	IEEE Transactions on Education, August 2004.
[IEEE.TITB'04]	IEEE Transactions on Information Technology in BioMedicine, March 2004.
[IEEE.TITB'03]	IEEE Transactions on Information Technology in BioMedicine, November 2003.
[BCS.BCJ'03]	The British Computer Journal, 2003.
[IEEE.CONC'00]	IEEE Concurrency, special issue on Caching in Distributed Systems, June 2000.
[IEEE.Micro'00]	IEEE Micro, special issue on Computer Architecture Education, 2000.
[IEEE.PIEEE'99]	Proceedings of the IEEE, special issue on Distributed Shared Memory, 1999.

Reviewer, Conferences

[HiPEAC-WRC'16]	10th HiPEAC Workshop on Reconfigurable Computing (WRC 2013), Berlin, Germany, January 19, 2016 (http://paginas.fe.up.pt/~specs/events/wrc2016/).
[IEEE.HealthCm'15]	17th International Conference on E-health, Networking, Application & Services (HealthCom'15), October 14-17, 2015, Boston, MA.
[IEEE.EMBC'15]	37th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC'15).
[ACM/IEEE. WCAE'15]	Workshop on Computer Architecture Education, Held in conjunction with 42nd International Symposium on Computer Architecture, Portland, OR, Saturday, 13 June 2015 http://www4.ncsu.edu/~efg/wcae2015.html
[IEEE.UbiHealth'15]	UbiHealth Tech 2015: 2nd International Symposium on Future Information and Communication Technologies for Ubiquitous Health Care, May 28–October 30, 2015 Beijing, China. http://www.ubi-health.org/
[IEEE.MSE'15]	International Conference on Microelectronic Systems Education, Pittsburgh, PA, May 20-21, 2015 (http://www.mseconference.org/; https://mse.soe.ucsc.edu/committees).
[IEEE.EMBC'14]	36th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC'14).
[ACM.PPoPP'13]	PPoPP 2014: 19th ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming.
[IEEE/ACM. BodyNets'13]	BodyNets 2013: 8th International Conference on Body Area Networks, September 30–October 2, 2013 Boston, Massachusetts, United States.
[IEEE.MSE'13]	International Conference on Microelectronic Systems Education, June 2-3, Austin, Texas (http://www.mseconference.org/).
[IEEE.EMBC'13]	35th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC'13).
[HiPEAC-WRC'13]	7th HiPEAC Workshop on Reconfigurable Computing (WRC 2013), Berlin, Germany, January 21, 2013 (http://www.cad.polito.it/research/!_EVENTS/WRC_2013/WRC_2013_-_Home_Page.html).
[IEEE.EMBC'12]	IEEE Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBS).
[HiPEAC-WRC'12]	6th HiPEAC Workshop on Reconfigurable Computing (WRC 2012), Paris, France, January 2012 (http://www.cad.polito.it/~sterpone/WRC_2012/WRC_2012_-_Home_Page.html).
[IEEE.EMBS'11]	IEEE Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBS).
[IEEE.VTC'11]	IEEE Vehicular Technology Conference, May 2011.
[ACM.DAC'11]	ACM Design Automation Conference, January 2011.
[IEEE.MSE'11]	Microelectronics System Education (MSE'09), San Diego, CA, Jun 2011.
[ACM.WCAE'11]	Workshop on Computer Architecture Education Held in conjunction with High Performance Computer Architecture 17, San Antonio, TX, February 2011.
[HiPEAC-WRC'11]	5th HiPEAC Workshop on Reconfigurable Computing (WRC 2011), Heraklion, Crete, Greece, January 2011 (http://hipeac.ac.upc.edu/WRC/HiPEACRC_WS_2011/).

[IEEE'SSST.10]	IEEE Southeastern Symposium on System Theory, Tyler, TX, March 2010.
[HiPEAC-WRC'10]	WRC 2010 4th HiPEAC Workshop on Reconfigurable Computing, Pisa, Italy, January 2010 (http://ce.et.tudelft.nl/HiPEACRC_WS/HiPEACRC_WS_2010/).
[MEDEA'09]	Memory performance: Dealing with Applications, Systems and Architecture, held in conjunction with MEDEA 2009 Workshop, held in conjunction with PACT 2009 Conference Sept. 12-16 2009, Raleigh, North Carolina.
[IEEE.MSE'09]	2009 International Conference on Microelectronic Systems Education, 25-27 July 2009, San Francisco, CA.
[IEEE.MEDEA'08]	Memory performance: Dealing with Applications, Systems and Architecture, held in conjunction with PACT 2008 Conference, Oct. 25-28 2008, Toronto, Canada.
[IEEE.SSST'09]	IEEE Southeastern Symposium on System Theory. 41st IEEE Southeastern Symposium on System Theory (SSST'09), Tullahoma, TN, USA, March 15-17, 2009.
[WCAE'08]	WCAE-08: Workshop on Computer Architecture Education Held in conjunction with the 34th International Symposium on Computer Architecture, Beijing, China, June 21, 2008.
[IEEE.SECON'08]	IEEE SoutheastCon 2008.
[IEEE.SAMOS'08]	SAMOS VIII: International Symposium on Systems, Architectures, MOdeling and Simulation Samos, Greece, July 21-24, 2008.
[MEDEA'07]	Memory performance: Dealing with Applications, Systems and Architecture, held in conjunction with PACT 2007 Conference, Sept. 15-19 2007, Brasov, Romania.
[WCAE'07]	WCAE-07: Workshop on Computer Architecture Education Held in conjunction with the 34th International Symposium on Computer Architecture San Diego, CA, June 9, 2007.
[IEEE.SAMOS'07]	SAMOS VII: International Symposium on Systems, Architectures, MOdeling and Simulation Samos, Greece, July 16-19, 2007.
[IEEE.MSE'07]	MSE 2007: 2007 International Conference on Microelectronic Systems Education June 3-4, 2007, San Diego, California.
[MEDEA'06]	Memory performance: Dealing with Applications, Systems and Architecture, held in conjunction with PACT 2006 Conference, Sept. 16-20 2006, Seattle, WA.
[WCAE'06]	Workshop on Computer Architecture Education, Boston, MA, June 2006.
[ERSA'06]	Engineering of Reconfigurable Systems and Algorithms, The 2006 International MultiConference in Computer Science & Computer Engineering, June 2006, Las Vegas, Nevada.
[MEDEA'05]	Memory performance: Dealing with Applications, Systems and Architecture, held in conjunction with PACT 2005 Conference, Sept. 17- 21, 2005, Saint Louis, Missouri.
[ERSA'05]	Engineering of Reconfigurable Systems and Algorithms, The 2005 International MultiConference in Computer Science & Computer Engineering, June 2005, Las Vegas Nevada.
[IEEE.MSE'05]	International Conference on Microelectronic Systems Education, June 2005, Anaheim, California.
[IEEE. Globecom'05]	Globecom 2005, Computer and Network Security.
[ACMSE'05]	ACM South East Conference, March 2005, Kennesaw, Georgia.
[ERSA'04]	Engineering of Reconfigurable Systems and Algorithms, The 2004 International MultiConference in Computer Science & Computer Engineering, June 21-24, 2004, Las Vegas, Nevada.
[ACMSE'04]	ACM South East Conference 2004, Huntsville, Alabama, April 1-2, 2004.
[PDCS'03]	ISCA's 16th International Conference on Parallel and Distributed Computing Systems, Reno, NV, 2003.
[MEDEA'02]	Workshop on Chip Multiprocessors: Processor Architecture and Memory Hierarchy Related Issues, 2002.
[MICRO'02]	35th Annual International Symposium on Microarchitecture, 2002.
[HICSS'01]	34th Hawai`i International Conference on System Sciences), 2001.

[ETRAN'97-99]	A major Yugoslav Conference For Electronics, Telecommunications, Computers, Automation, and Nuclear Engineering.

Program Committee Member (Conferences/Workshops)

[HiPEAC-WRC'16]	10th HiPEAC Workshop on Reconfigurable Computing (WRC 2013), Berlin, Germany, January 19, 2016 (http://paginas.fe.up.pt/~specs/events/wrc2016/).
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[IEEE.EMBC'15]	37th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC'15).
[ACM/IEEE. WCAE'15]	Workshop on Computer Architecture Education, Held in conjunction with 42nd International Symposium on Computer Architecture, Portland, OR, Saturday, 13 June 2015 http://www4.ncsu.edu/~efg/wcae2015.html
[IEEE.UbiHealth'15]	UbiHealth Tech 2015: 2nd International Symposium on Future Information and Communication Technologies for Ubiquitous Health Care, May 28–October 30, 2015 Beijing, China. http://www.ubi-health.org/
[IEEE.MSE'15]	International Conference on Microelectronic Systems Education, Pittsburgh, PA, May 20-21, 2015 (http://www.mseconference.org/; https://mse.soe.ucsc.edu/committees).
[IEEE.EMBC'14]	Associate Editor, 36th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC'14).
[IEEE/ACM. BodyNets'13]	BodyNets 2013: 8th International Conference on Body Area Networks, September 30–October 2, 2013 Boston, Massachusetts, United States.
[IEEE.MSE'13]	International Conference on Microelectronic Systems Education, June 2-3, Austin, Texas (http://www.mseconference.org/).
[IEEE.EMBS'13]	Associate Editor, 35th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC'13).
[HiPEAC-WRC'13]	7th HiPEAC Workshop on Reconfigurable Computing (WRC 2013), Berlin, Germany, January 21, 2013 (http://www.cad.polito.it/research/!_EVENTS/WRC_2013/WRC_2013_-_Home_Page.html).
[IEEE.EMBS'12]	Associate Editor, IEEE Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBS).
[HiPEAC-WRC'12]	6th HiPEAC Workshop on Reconfigurable Computing (WRC 2012), Paris, France, January 2012 (http://www.cad.polito.it/~sterpone/WRC_2012/WRC_2012_-_Home_Page.html).
[IEEE.EMBS'11]	Associate Editor, IEEE Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBS).
[IEEE.MSE'11]	Microelectronics System Education (MSE'09), San Diego, CA, Jun 2011.
[ACM.WCAE'11]	Workshop on Computer Architecture Education Held in conjunction with High Performance Computer Architecture 17, San Antonio, TX, February 2011.
[HiPEAC-WRC'11]	5th HiPEAC Workshop on Reconfigurable Computing (WRC 2011), Heraklion, Crete, Greece, January 2011 (http://hipeac.ac.upc.edu/WRC/HiPEACRC_WS_2011/).
[HiPEAC-WRC'10]	WRC 2010 4th HiPEAC Workshop on Reconfigurable Computing, Pisa, Italy, January 2010 (http://ce.et.tudelft.nl/HiPEACRC_WS/HiPEACRC_WS_2010/).
[MEDEA'09]	Memory performance: Dealing with Applications, Systems and Architecture, held in conjunction with MEDEA 2009 Workshop, held in conjunction with PACT 2009 Conference, Sept. 12-16 2009, Raleigh, North Carolina.
[MSE'09]	2009 International Conference on Microelectronic Systems Education, 25-27 July 2009, San Francisco, CA.
[WCAE'09]	Workshop on Computer Architecture Education Held in conjunction with the 42nd Annual International Symposium on Microarchitecture, New York, NY, December 2009.

[WCAE'08]	WCAE-08: Workshop on Computer Architecture Education Held in conjunction with the 34th International Symposium on Computer Architecture, Beijing, China, June 21, 2008.
[IEEE.SAMOS'08]	SAMOS VIII: International Symposium on Systems, Architectures, MOdeling and Simulation Samos, Greece, July 21-24, 2008.
[MEDEA'07]	Memory performance: Dealing with Applications, Systems and Architecture, held in conjunction with PACT 2007 Conference, Sept. 15-19 2007, Brasov, Romania.
[WCAE'07]	WCAE-07: Workshop on Computer Architecture Education Held in conjunction with the 34th International Symposium on Computer Architecture San Diego, CA Saturday, June 9, 2007.
[IEEE.SAMOS'07]	SAMOS VII: International Symposium on Systems, Architectures, MOdeling and Simulation Samos, Greece, July 16-19, 2007.
[IEEE.MSE'07]	MSE 2007: 2007 International Conference on Microelectronic Systems Education June 3-4, 2007, San Diego, California.
[MEDEA'06]	Memory performance: Dealing with Applications, Systems and Architecture, held in conjunction with PACT 2006 Conference, Sept. 16-20 2006, Seattle, WA.
[WCAE'06]	Workshop on Computer Architecture Education, Boston, MA, June 2006.
[ERSA'06]	Engineering of Reconfigurable Systems and Algorithms, The 2006 International MultiConference in Computer Science & Computer Engineering, June 2006, Las Vegas, Nevada.
[MEDEA'05]	Memory performance: Dealing with Applications, Systems and Architecture, held in conjunction with PACT 2005 Conference Sept. 17- 21 2005, Saint Louis, Missouri.
[IEEE.MSE'05]	International Conference on Microelectronic Systems Education, June 2005, Anaheim, California, http://www.mseconference.org/.
[ERSA'05]	Engineering of Reconfigurable Systems and Algorithms, The 2005 International MultiConference in Computer Science & Computer Engineering, June 2005, Las Vegas, Nevada.
[MEDEA'03]	MEDEA Workshop On Chip Multiprocessors: Processor Architecture and Memory Hierarchy related Issues, Held in conjunction with PACT, September 2003, New Orleans, Louisiana, http://garga.iet.unipi.it/medea03/.
[MEDEA'02]	MEDEA Workshop On Chip Multiprocessors: Processor Architecture and Memory Hierarchy related Issues, Held in conjunction with PACT, September 2002, Charlottesville, Virginia, http://garga.iet.unipi.it/medea/.

Panels, External Reviewer for Funding Agencies, Book Publishers

[NSF'15]	**Panelist** for NSF, January 2015.
[AAA'14]	**External reviewer** for the American Association for the Advancement of Science (AAAS) – Research Competitiveness Program (KACST), December 2014.
[AAA'13]	**External reviewer** for the American Association for the Advancement of Science (AAAS) – Research Competitiveness Program (KACST), November 2013.
[AAAS'12]	**External reviewer** for the American Association for the Advancement of Science (AAAS) – Research Competitiveness Program (KACST), March 2012.
[US.VA'11]	**External reviewer,** The Department of Veteran Affairs, December 2011.
[NL.SWT'11]	**Consultant,** Technology Foundation STW, The Netherlands, June 2011.
[NL.SWT'10]	**Consultant,** Technology Foundation STW, The Netherlands, January 2011.
[Sg.MoH'10]	**External reviewer,** Ministry of Health, Singapore, September 2010.
[NSF'09]	**Panelist** for NSF, November 2009.
[Cons.SV'08]	**Consultant, Senior Vitals Inc.,** May/June 2008.
[AWP'08]	**Reviewer** for a VLSI book for Addison Wesley Publishing, March 2008.
[HK'07]	**Reviewer** for Innovation and Technology Commission of the Hong Kong Special Administration Region Government, November 2007.
[TE'07]	**Reviewer** for a microprocessor textbook for Thompson Engineering, December 2006.

[OUP'06]	**Reviewer** for a microprocessor textbook for Oxford University Press, December 2006.
[Wiley'06]	**Reviewer** for The Handbook of Computer Networks, February 2006.
[OUP'05]	**Reviewer** for a microprocessor textbook for Oxford University Press, November 2005.
[MTC'04]	**External reviewer** for Maryland Technological Corporation, August 2004.
[NSF'04]	**Ad-hoc reviewer** for NSF, August 2004.
[NSF'04]	**Panelist** for NSF, May 2004.
[SFI'04]	**External reviewer** for Science Foundation IRELAND (SFI), February 2004

University Service

ECE.SC'15	2015/2016	ECE Dept. Search Committee Chair
CoE.PTAC'15	2015/2016	College of Engineering, Promotion and Tenure Award Committee
UAH.IIDR'15	2015	UAH IIDR Program Committee Member
CoE.PTAC'14	2014/2015	College of Engineering, Promotion and Tenure Award Committee
ECE.SC'14	2014/2015	ECE Dept. Search Committee Member (3 new positions)
CPE.PC	2011-present	Computer Engineering Program Coordinator
CoE.CC	2013-present	College of Engineering, Curriculum Committee (Undergrad/Grad)
ECE.HKN	2005-present	Eta Kappa Nu Theta Eta Chapter Academic Advisor
UAH.SNT'9	2009-2011	Faculty Senate, ECE representative
UAH.S-PC	2009-2011	Faculty Senate, Personnel Committee
UAH.GC	2009-2011	Graduate Council (CoE representative)
ECE.ISC	2010	ECE Chair Internal Search Committee (Committee Chair)

Honors, Awards, Special Recognitions

[IEEE.ICCCN'15]	Best paper nominee
[IEEE.HSV'15]	IEEE Huntsville Section Outstanding Educator 2015, February 2015.
[CoE.OSFA'14]	The College of Engineering National Engineer's Week Outstanding Senior Faculty Award, February 2014.
[CoE.OF'13]	The College of Engineering Outstanding Faculty Award, May 2013.
[ACM.CASES'10]	Best paper award at ACM CASES'10, October 2010.
[CoE.OAP'05]	The College of Engineering Outstanding Assistant Professor Award, February 2005.
[SSF'89-94]	Serbia Science Foundation Scholarship.
[SerMPA'87]	Mihailo Petrovic Alas Diploma; Highest High School award in Serbia for achievements in mathematics and physics.
[SerVSK'87]	Vuk Stefanovic Karadzic Diploma; Highest High School award in Serbia for overall academic achievements.
[YuPhys'86]	3rd Place in Physics Competition in former Yugoslavia.

Memberships

IEEE, IEEE Computer Society (elected Senior Member in 2010)
ACM, ACM SIGARCH (Special Interest Group on Computer Architecture),
ACM SIGBED (Special Interest Group on Embedded Systems), Tau Beta Pi, Eta Kappa Nu (Advisor).

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Miquel Pericàs, Ph.D.

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Publications

Complete List of Publications (cronological order)

1. ***Performance and Power Evaluation of Clustered VLIW Processors with Wide Functional Units.*** Miquel Pericàs, Eduard Ayguadé, Javier Zalamea, Josep Llosa and Mateo Valero. Proceedings of SAMOS'03 Workshop, Samos, 2003. Download
2. ***Power-Performance Trade-Offs in Wide and Clustered VLIW Cores for numerical Computations***. Miquel Pericàs, Eduard Ayguadé, Javier Zalamea, Josep Llosa and Mateo Valero. Intl' Symposium on High Performance Computing (ISHPC-V). Tokyo, 2003. Download.
3. ***Power-Performance Trade-Offs in Wide and Clustered VLIW Cores for numerical Computations.*** Miquel Pericàs, Eduard Ayguadé, Javier Zalamea, Josep Llosa and Mateo Valero. Lecture Notes on Computer Science Volume 2858/2003. pp. 113-126
4. ***High-Performance Low-Power VLIW Cores for Numerical Computations.*** Miquel Pericàs, Eduard Ayguadé, Javier Zalamea, Josep Llosa and Mateo Valero. International Journal of High Performance Computing and Networking 2004 - Vol. 1, No.4. pp. 171 - 179
5. ***Performance and Power Evaluation of Clustered VLIW Processors with Wide Functional Units.*** Miquel Pericàs, Eduard Ayguadé, Javier Zalamea, Josep Llosa and Mateo Valero. Lecture Notes in Computer Science. Volume 3133/2004, 2004. pp. 88-97.
6. ***Power-Efficient VLIW Design using Clustering and Widening***. Miquel Pericàs, Eduard Ayguadé, Javier Zalamea, Josep Llosa and Mateo Valero. International Journal of Embedded Systems. Volume 31204 (to appear)

Miquel Pericàs, Ph.D.

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Publications

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1. ***Performance and Power Evaluation of Clustered VLIW Processors with Wide Functional Units.*** Miquel Pericàs, Eduard Ayguadé, Javier Zalamea, Josep Llosa and Mateo Valero. Proceedings of SAMOS'03 Workshop. Samos, 2003. Download
2. ***Power-Performance Trade-Offs in Wide and Clustered VLIW Cores for numerical Computations.*** Miquel Pericàs, Eduard Ayguadé, Javier Zalamea, Josep Llosa and Mateo Valero. Intl' Symposium on High Performance Computing (ISHPC-V). Tokyo, 2003. Download.
3. ***Power-Performance Trade-Offs in Wide and Clustered VLIW Cores for numerical Computations.*** Miquel Pericàs, Eduard Ayguadé, Javier Zalamea, Josep Llosa and Mateo Valero. Lecture Notes on Computer Science Volume 2858/2003. pp. 113-126
4. ***High-Performance Low-Power VLIW Cores for Numerical Computations.*** Miquel Pericàs, Eduard Ayguadé, Javier Zalamea, Josep Llosa and Mateo Valero. International Journal of High Performance Computing and Networking 2004 - Vol. 1, No.4 pp. 171 - 179
5. ***Performance and Power Evaluation of Clustered VLIW Processors with Wide Functional Units.*** Miquel Pericàs, Eduard Ayguadé, Javier Zalamea, Josep Llosa and Mateo Valero. Lecture Notes in Computer Science. Volume 3133/2004, 2004. pp. 88-97.
6. ***Power-Efficient VLIW Design using Clustering and Widening.*** Miquel Pericàs, Eduard Ayguadé, Javier Zalamea, Josep Llosa and Mateo Valero. International Journal of Embedded Systems. Volume 31204 (to appear).
7. ***Scalable Distributed Register File.*** Ruben Gonzalez, Adrian Cristal, Miquel Pericàs, Alex Veidenbaum and Mateo Valero. Workshop on Complexity Effective Design (WCED). June 2004. Download
8. ***An Optimized Front-End Physical Register File with Banking and Writeback Filtering.*** Miquel Pericàs, Ruben Gonzalez, Adrian Cristal, Alex Veidenbaum and Mateo Valero. Workshop on Power Aware Computer Systems. December 2004. PDF PS
9. ***An Asymmetric Clustered Processor based on Value Content.*** Ruben Gonzalez, Adrian Cristal, Alex Veidenbaum, Miquel Pericas and Mateo Valero. International Conference on Supercomputing. June 2005
10. ***Kilo-Instruction Processors: Overcoming the Memory Wall.*** Adrian Cristal, Oliverio J. Santana, Francisco J. Cazorla, Marco Galluzzi, Tanausú Ramirez, Miquel Pericàs and Mateo Valero. IEEE MICRO. Vol 25, Nr 3. pp 48-57. May/June 2005
11. ***Exploiting Execution Locality with a Decoupled Kilo-Instruction Processor.*** Miquel Pericàs, Ruben Gonzalez, Adrian Cristal, Daniel A. Jimenez and Mateo Valero. International Symposium on High Performance Computing (ISHPC-VI) 2005
12. ***The Decoupled State/Execute Architecture.*** Miquel Pericàs, Ruben Gonzalez, Adrian Cristal, Alex Veidenbaum and Mateo Valero. International Symposium on High Performance Computing (ISHPC-VI) 2005
13. ***Chained In-Order/Out-of-Order DoubleCore Architecture.*** Miquel Pericàs, Ruben Gonzalez, Adrian Cristal, Daniel A. Jimenez and Mateo Valero. SBAC-PAD 2005 Download
14. ***A Decoupled KILO-Instruction Processor.*** Miquel Pericàs, Ruben Gonzalez, Adrian Cristal, Daniel A. Jimenez and Mateo Valero. HPCA-12 (2006) Download
15. ***An Optimized Front-End Physical Register File with Banking and Writeback Filtering.*** Miquel Pericàs, Ruben Gonzalez, Adrian Cristal, Alex Veidenbaum and Mateo Valero. Lecture Notes in Computer Science. Volume 3471 / 2005. Pages 1 - 14
16. ***A Flexible Heterogeneous Multi-Core Architecture.*** Miquel Pericàs, Ruben Gonzalez, Francisco J. Cazorla, Adrian Cristal, Daniel A. Jimenez and Mateo Valero. Parallel Architecture and Compiler Techniques (PACT-2007) Download
17. ***Vectorized AES Core for high-throughput secure environments.*** Miquel Pericàs, Ricardo Chaves, Georgi N. Gaydadjiev, Mateo Valero and Stamatis Vassiliadis. The Future of Computing - essays in memory of Stamatis Vassiliadis (2007) Download
18. ***Exploiting Execution Locality with a Decoupled Kilo-Instruction Processor.*** Miquel Pericàs, Ruben Gonzalez, Adrian Cristal, Daniel A. Jimenez and Mateo Valero. Lecture Notes in Computer Science. Volume 4759/2008. pp. 56-67
19. ***The Decoupled State/Execute Architecture.*** Miquel Pericàs, Ruben Gonzalez, Adrian Cristal, Alex Veidenbaum and Mateo Valero. Lecture Notes in Computer Science. Volume 4759/2008. pp. 68-78
20. ***Vectorized AES Core for high-throughput secure environments.*** Miquel Pericàs, Ricardo Chaves, Georgi N. Gaydadjiev, Mateo Valero and Stamatis Vassiliadis. VECPAR 2008. Tolouse, June 2008
21. ***A two-level Load/Store Queue based on Execution Locality.*** Miquel Pericas, Adrian Cristal, Ruben Gonzalez, Alex Veidenbaum, Daniel A. Jimenez and Mateo Valero. The 35th International Symposium on Computer Architecture (ISCA-35). Beijing. 2008 Download
22. ***Affordable KILO-Instruction Processors.*** Miquel Pericas. PhD Thesis. December 2008. Download
23. ***Exploiting Memory Customization in FPGA for 3D Stencil Computations.*** Muhammad Shafiq, Miquel Pericàs, Raul de la Cruz, Mauricio Araya-Polo, Nacho Navarro and Eduard Ayguadé. The 2009 International Conference on Field-Programmable Technology (FPT'09). Sydney, December 2009.
24. ***Row-interleaved streaming data flow implementation of Sparse Matrix Vector Multiplication in FPGA.*** Branimir Dickov, Miquel Pericàs, Nacho Navarro and Eduard Ayguadé. WRC 2010 - 4th HiPEAC Workshop on Reconfigurable Computing. Pisa, January 2010.
25. ***FEM : A Step Towards a Common Memory Layout for FPGA Based Accelerators.*** Muhammad Shafiq, Miquel Pericàs, Nacho Navarro and Eduard Ayguadé. FPL2010 The 20th International Conference on Field Programmable Logic and Applications. Milano. August-September 2010 Download
26. ***Assessing Accelerator-Based HPC Reverse Time Migration.*** Mauricio Araya-Polo, Javier Cabezas, Mauricio Hanzich, Miquel Pericàs, Felix Rubio, Isaac Gelado, Muhammad Shafiq, Enric Morancho, Nacho Navarro, Eduard Ayguadé, José Maria Cela and Mateo Valero. IEEE Transactions on Parallel and Distributed Systems. January 2011 (vol. 22 no. 1) pp. 147-162
27. ***Reconfigurable Memory Controller with Programmable Pattern Support.*** Tassadaq Hussain, Miquel Pericàs and Eduard Ayguadé. Workshop on Reconfigurable Computing 2011 (WRC 2011) Download
28. ***A Template System for the Efficient Compilation of Domain Abstractions onto Reconfigurable Computers.*** Muhammad Shafiq, Miquel Pericàs and Eduard Ayguadé. Workshop on Reconfigurable Computing (WRC 2011) Download
29. ***TARCAD: A Template Architecture for Reconfigurable Accelerator Designs.*** Muhammad Shafiq, Miquel Pericàs, Nacho Navarro and Eduard Ayguadé. The 9th IEEE Symposium on Application Specific Processors (SASP 2011) (to appear)

Some technical reports:

1. ***Banked Front-End Register File.*** Miquel Pericàs, Ruben Gonzalez, Adrian Cristal, Alex Veidenbaum and Mateo Valero. Technical Report. Reference: UPC-DAC-2004-35. October 2004
2. ***A Flexible Heterogeneous Multi-Core Architecture.*** Miquel Pericas, Adrian Cristal, Francisco J. Cazorla, Ruben González, Daniel A. Jimenez, Mateo Valero. Technical Report. Reference: UPC-DAC-RR-CAP-2006-15. August 2006
3. ***A Reconfigurable Heterogeneous Multi-Core Architecture.*** Miquel Pericas, Adrian Cristal, Francisco J. Cazorla, Ruben González, Daniel A. Jimenez, Mateo Valero. Technical Report. Reference: UPC-DAC-RR-CAP-2007-1. February 2007

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Ioannis Sourdis' Professional Activities

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Professional Activities

Organizing Committees

Program co-chair: 2nd HiPEAC Workshop on Reconfigurable Computing, 2008.

General co-chair: 3rd HiPEAC Workshop on Reconfigurable Computing, 2009.

Publicity chair: 4th HiPEAC Workshop on Reconfigurable Computing, 2010.

Local Arrangements co-chair: 28th IEEE Int'l Conf. on Computer Design 2010.

TRACK-chair: IEEE FPL 2011, track: ``Self-aware and adaptive systems", 2011.

Publicity chair: Int. Conf. on Embedded Computer Systems: Architectures, Modeling, and Simulation (SAMOS) 2012.

Technical Program Committees

Ioannis Sourdis' Professional Activities

Professional Activities

Organizing Committees

Program co-chair: 2nd HiPEAC Workshop on Reconfigurable Computing, 2008.
General co-chair: 3rd HiPEAC Workshop on Reconfigurable Computing, 2009.
Publicity chair: 4th HiPEAC Workshop on Reconfigurable Computing, 2010.
Local Arrangements co-chair: 28th IEEE Int'l Conf. on Computer Design 2010.
TRACK-chair: IEEE FPL 2011, track: ``Self-aware and adaptive systems", 2011.
Publicity chair: Int. Conf. on Embedded Computer Systems: Architectures, Modeling, and Simulation (SAMOS) 2012.

Technical Program Committees

HiPEAC Workshop on Reconfigurable Computing, (2008-present).
17th European Signal Processing Conference 2009.
Design, Automation and Test in Europe Conference (DATE) 2010-present.
Int. Conf. on Frontier of Computer Science and Technology (FCST) 2010-present.
IEEE/IFIP Int. Conf. on VLSI and SoC (VLSI-SoC) 2010-present.
IEEE Int. Conf. on Field Programmable Logic and Applications (FPL) 2011-present.
Int. Symp. on Circuits and Systems (ISCAS) 2012-present.
Int. Conf. on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS, IEEE) 2012-present.
Manufacturable and Dependable Multicore Architectures at Nanoscale Workshop (Median) 2012-present.
Int. Conf. on Supercomputing (ICS, ACM) 2012-present.

Referee

IEEE Transactions on Computers.
IEEE/ACM Transactions on Networking.
IEEE Micro.
IEEE Journal on Selected Areas in Communications, JSAC.
IEEE Transactions on Very Large Scale Integration Systems.
IEEE Transactions on Parallel and Distributed Systems.
IEEE Transactions on Dependable and Secure Computing.
IEEE Transactions on Information Forensics and Security.
IEEE Computer Architecture Letters.
IEEE Communication Letters.
ACM Trans on Reconfigurable Technology and Systems.
ACM Transactions on Architecture and Code Optimization.
Computer Networks.
ACM SIGCOMM Computer Communication Review.
Transactions on HiPEAC.
ACM Trans. On Embedded Computing Systems
Journal of Embedded Computing.
Journal of VLSI Signal Processing.
Journal of Systems Architecture.
IET Computers & Digital Techniques.
Int. Journal of Electronics.
EURASIP Journal on Embedded Systems.
European Conference on Parallel Computing, Euro-Par (2005).
IEEE International Conference on Application-specific Systems, Architectures and Processors, ASAP (2005, 2006).
Embedded Computer Systems: Architectures, MOdeling, and Simulation, SAMOS (2005, 2006, 2007).
Computing Frontiers, CF (2005-2009).
The 33rd Annual International Symposium on Computer Architecture, ISCA (2006).
ACM International Conference on Supercomputing, ICS (2006, 2007).
Workshop on Applied Reconfigurable Computing, ARC (2006).
Reconfigurable Architectures Workshop, RAW (2005, 2006).
Int. Conference on Field Programmable Logic and Applications, FPL (2003, 2005, 2006, 2007).
Design, Automation and Test in Europe, DATE (2006, 2007).
IEEE Int. Symp. on Circuits and Systems (ISCAS 2006, 2007).
IEEE Computer Society Annual Symposium on VLSI, ISVLSI (2006, 2007).
Int. Conf. on High Performance Embedded Architectures & Compilers, HiPEAC (2006).
Reconfigurable and Adaptive Architecture Workshop, RAAW (2007).
Architecture of Computing Systems, ARCS (2007).
IEEE International Parallel & Distributed Processing Symposium, IPDPS (2007).
Int. Conf. on Parallel Processing, ICPP (2007).
Int. Workshop on Embedded Single and Multicore Systems on Chips, MCSoC (2007).
Int. Conf. on Compilers, Architecture, and Synthesis for Embedded Systems, CASES (2007).
Workshop on Design, Architecture and Simulation of Chip Multi-Processors, dasCMP (2008).
ACM/IEEE Symposium on Architectures for Networking and Communications Systems, ANCS (2008).
IEEE LAN/MAN Workshop (2007).
European Signal Processing Conference (2009).

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Universidade de Lisboa

Curriculum Vitae of Professor

(First two pages *resume*)

Leonel Augusto Pires Seabra de Sousa

Universidade de Lisboa

Curriculum Vitae of Professor

(First two pages *resume*)

Leonel Augusto Pires Seabra de Sousa

Electrical and Computer Engineering Department, IST
INESC-ID, Rua Alves Redol, 9, 1000-029 Lisboa, Portugal
email: las@inesc-id.pt
web page: http://sips.inesc-id.pt/las

November 2015

Resume

Education

2004 Habilitation (Agregação) in Electrical and Computer Engineering (ECE), Instituto Superior Técnico (IST), Technical University of Lisbon (TU Lisbon), Portugal.

1996 PhD in Electrical and Computer Engineering, IST, TU Lisbon, Portugal.

1989 MSc in Electrical and Computer Engineering, IST, TU Lisbon, Portugal.

1984 Licenciatura (5 years) in Electronics and Telecommunications, Universid. de Aveiro, Portugal.

Positions and Experience

2017–*present* Head of the ECE Department at IST, Universidade de Lisboa.

2010–*present* Full Professor (Professor Catedrático) with the ECE Department at IST, Universidade de Lisboa.

2013–2016 Vice-President of the Scientific Council of IST, responsible for the PhD programs and research.

2009-2013 Chair of the Board of Directors of INESC-ID.

2008-2013 Director of the ECE BSc and MSc programs (2008-2013) and

1998–*present* Senior Researcher at INESC-ID.

Work Experience, Research Interests and Achievements

Supervised or co-supervised 15 PhD theses and more than 40 MSc theses, already finished.

Responsible for and taught at IST the courses "Advanced Computer Architecture", "Multimedia Architectures and Specialized Processors", "High Performance Computing Architectures" at the graduate level, and "Computer Electronics", "Electronics Systems for Signal Processing" at the undergraduate level.

Research interests include digital systems design and signal processing, architectures and circuits for general purpose and specialized processing, and high performance and parallel computing.

Principal investigator (PI) in 4 multiannual research projects funded by the Portuguese Foundation for Science and Technology and participated in more than 20 other funded research projects.

Participated in the evaluation committee and acted as an external reviewer of more than 50 PhD theses, in Portugal and in five other countries.

Contributed to more than 80 papers in scientific journals and 150 in international conferences, which receive a significant number of citations.

More than 30 invited invited talks given in universities, industries and conferences.

Professional Services

Associated Editor of the IEEE Transactions on Multimedia, IEEE Transactions on Circuits and Systems for Video Technology, IEEE Access, Springer J. of Real-Time Image Processing and IET Electronics Letters

Editor in Chief of the EURASIP Journal on Embedded Systems, a SpringerOpen journal.

General-Chair of several Conferences, such as EUSIPCO 2014, HiPEAC WRC 2010, ISPDC 2009,

Program (Co-)Chair of IEEE BigMM 2017, IEEE ISM 2015, HeteroPar 2009, HiPEAC WRC 2009, SBAC-PAD 2014 ("Software" track), Euro-Par 2012 ("Scheduling and Load Balancing" topic), and SAMOS 2010 ("Applications, Systems, Architectures, and Processors" track).

Awards and Distinctions

2015 Selected ACM *Distinguished Scientist*.

2013 Elevated to Fellow of the IET.

2013, 2010 Best Paper and Poster Awards at the Conference on Design and Architectures for Signal and Image Processing (DASIP).

2011 "Stamatis Vassiliadis" Best Paper Award at the 11th International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS XI).

2010 Supervisor of the PhD thesis awarded with second placed in the **Fraunhofer Portugal Challenge**.

2009 Distinguished with an honorable mention for the impact of the publications in international scientific journals during the period 2004-2008 (award UTL/Santander Totta).

2008, 2004 Supervisor of the best MSc (2007/08) and Licenciatura (2003/04) theses at IST in the areas of Electrical and Computer Engineering and Informatics (award *Prof. Luís Vidigal*).

10 of the most important recent publications

2017 A. Ilic, F. Pratas and L. Sousa, "Beyond the Roofline: Cache-aware Power and Energy-Efficiency Modeling for Multi-cores", IEEE Transactions on Computers, vol. 66, n. 1, pp. 52-58.

2016 L. Sousa, S. Antão and P. Martins, "Combining Residue Arithmetic to Design Efficient Cryptographic Circuits and Systems", IEEE Circuits and Systems Magazine, vol. 16, n. 4, pp. 6-32.

2016 J. Andrade, G. Falcão, V. Silva and L. Sousa, "A Survey on Programmable LDPC Decoders,"IEEE Access, vol. 4, pp. 6704-6718.

2014 S. Momcilovic, A. Ilic, N. Roma and L. Sousa, "Dynamic load balancing for real-time video encoding on heterogeneous CPU+GPU systems," IEEE Transactions on Multimedia, vol. 16, no. 1, pp. 108– 121.

2014 A. Ilic, F. Pratas and L. Sousa, "Cache-aware roofline model: Upgrading the loft," IEEE Computer Architecture Letters, vol. 13, no. 1, pp. 21–24.

2011 G. Falcão, L. Sousa and V. Silva, "Massively LDPC decoding on multicore architectures," IEEE Transactions on Parallel and Distributed Systems (TPDS), vol. 22, no. 2, pp. 309—322.

2006 R. Chaves, G. Kuzmanov, L. Sousa and S. Vassiliadis, "Improving SHA-2 hardware implementations," in Proceedings of the Workshop on Cryptographic Hardware and Embedded Systems (CHES), Springer, LNCS, pp. 298–310.

2006 O. Sinnen, L. Sousa and F. Sandnes, "Towards a realistic task scheduling model," IEEE Transactions on Parallel and Distributed Systems, vol. 17, no. 3, pp. 263–275.

2005 O. Sinnen and L. Sousa, "Communication contention in task scheduling," IEEE Transactions on Parallel and Distributed Systems, vol. 16, no. 6, pp. 503–515.

2000 L. Sousa, "A general method for eliminating redundant computations in video coding," IEE Electronics Letters, vol. 36, no. 4, pp. 306–307.

1 Experience

Current Activities

Current position	Full Professor in the Electrical and Computer Engineering (ECE) Department at Instituto Superior Técnico(IST), Universidade de Lisboa (UL), in Portugal, since December 2010.
Teaching	Lecturer of basic and advanced courses on embedded systems, computer architectures, and parallel systems, included in the ECE M.Sc., and ECE and Computer Science Ph.D. programs at IST.
Research	Head a of a research group at *Instituto de Engenharia de Sistemas e Computadores, Investigação e Desenvolvimento* (INESC-ID), currently supervising 4 PhD students (supervised 14 PhD students that already finished), member of the EU FP7 Network of Excellence HiPEAC3, member of the management committee and Working Group Leader of the EU COST action Network for Sustainable Ultrascale Computing (NESUS), and Principal Investigator of the project *Stretching the Limits of Parallel Processing on Heterogenous Computing Systems* funded by the Portuguese Foundation for Science and Technology.
Conselor	One of the 14 members of the Scientific Council for Exact Sciences and Engineering of the Portuguese Foundation for Science and Technology (FCT), with the mission of providing the FCT Board with strategic advice and recommendations on developing, implementing and modifying science and technology in Portugal; Vice-Head of the Scientific Board of IST, a board composed by 20 elected members that plays a major role in the governance of IST.
Evaluator	Head of the National Panel for the final scientific evaluation of all projects in the area of Electrical Engineering funded by the FCT (2014-2016); evaluator of research project proposals of the H2020 program sponsored by the European Commission; reviewer and opponent on several these PhD defenses on international universities.
Speaker	Invited or keynote speaker on more than thirty conferences, universities and companies.
Professional service	Editor-in-Chief of the Springer EURASIP *Journal of Embedded Systems*, and Associate Editor of the IEEE *Transactions on Multimedia*, IEEE *Transactions on Circuits and Systems for Video Technology*, IEEE *Access*, and Springer *Journal of Real Time Image Processing*; involved in the organization of several international conferences (e.g. in 2014 in ICCD, SAMOS, Computing Frontiers, IPDPS, ICPP, Europar, EUSIPCO, SBAC-PAD); member of several international technical committees.

Previous Positions and Visiting Positions

Visit	Visiting Professor of the Electrical and Computer Engineering Department at Carnegie Mellon University, Pittsburgh, USA, Fall Semester 2016/2017. Faculty of Electrical Engineering, Mathematics and Computer Science of TU Delft (2002/03 spring semester).
Visit	JSPS Invitation Fellowship for Research in Japan (Short-term) and Visiting Professor of the Computer Science Departmente at the University of Tsukuba, Japan. "This fellowship program is to invite overseas researchers with excellent records of research achievements

for short-term visits to Japan and provide them opportunities for discussions, opinion exchanges, lectures and other activities". June-August 2016.

Positions — Chair of INESC-ID, a not for profit, privately owned institution of public interest, dedicated to advanced research and development in the domains of electronics, telecommunications and information technologies, with more than 100 PhD researchers and owned by IST (2009-2013); Coordinator of the M.Sc. and B.Sc. programs in ECE at IST, which totalize more than 1500 students (2008-2012).

Visit — Visiting Professor in the Computer Engineering Lab at the Faculty of Electrical Engineering, Mathematics and Computer Science of TU Delft (2002/03 spring semester).

2 Academic Degrees

- Habilitation (Agregação in Portugal) in Electrical and Computer Engineering, at IST, in 2004. *Thesis title*: Architectures and Algorithms for Signal Processing in Real Time.
- Ph.D. degree in Electrical and Computer Engineering, at IST, in 1996. *Thesis title*: Parallel Image Processors with Orthogonal Access to Shared Memory.
- M.Sc. in Electrical and Computer Engineering, at IST, in 1989. *Thesis title*: Algorithms and Architecture for the Digital Signal Processing System APICE.
- Licenciatura in Electronics and Telecommunications at University of Aveiro, in 1984.

3 Teaching

My teaching experience comprises: the development of new advanced postgraduate courses in the area of Computer Engineering; the coordination, for five years, of the MSc and BSc programs in Electrical and Computer Engineering (ECE) at IST, with a total of more than 1500 students; and the teaching of courses in this area. I have developed pedagogical material to the courses that I taught, which has been used through the years.

Teaching — I have taught courses on Computer Organization, Computer Architecture, Embedded Systems, and Parallel Computing Architectures over the past 15 years. Notwithstanding I have introduced several courses in the M.Sc. and Ph.D. ECE programs, I have also taught courses on Embedded Systems, namely the *Computer Electronics* course and the *Basic Electronics* courses.

New courses — I have designed and introduced the following new courses in the IST MS.C and Ph.D. Programs in ECE: *Advanced Computer Architectures*, started in 2003/2004 and has been running in the M.Sc. program all spring semesters; *Specialized Digital Processors*, launched as an elective course in 1997/98 and offered in the program till 2002/2003; and *High Performance Computing Architectures*, a course that is running in the PhD program since 2006/2007. I have developed advanced lab tutorials for courses in computer architecture and embedded systems, an example can be found in *A Lab Project on the Design and Implementation of Programmable and Configurable Embedded Systems*, one of the most popular articles of the *IEEE Transactions on Education*.

Curriculum Design — I was also involved in curriculum design, 2006/2007, on adapting the ECE integrated M.Sc. Program according to the Bologna declaration. Being in charge of coordinating the M.Sc. and

the B.Sc. ECE programs in IST since 2009, in 2011/2012 I redesigned the ECE M.Sc. Program, namely the organization of the specialization areas and the courses offered in each one of those areas.

Textbooks I am co-author of the textbook *Bioelectronic Vision Retina Models, Evaluation Metrics, and System Design*, series on Bioengineering and Biomedical Engineering, vol. 3, World Scientific, a textbook for advanced undergraduate and graduate students in biomedical engineering, and electrical and computer engineering. This book provides a technical perspective of the functional and structural retina models, and provides insight about the models used on hardware implementations.

4 Research Focus and Achievements

The focus of my research has been on computer architecture and high performance computing, namely the design of highly efficient architectures, algorithms and circuits for current and emergent applications. My research work has evolved by taking a holistic system perspective that addresses the interaction between applications, algorithms, software and hardware platforms, and how it impacts the performance and tradeoffs across different hardware and software solutions. Among others, there are two key topics in which I have made cutting-edge research contributions: Hardware Accelerators, and Parallel Heterogeneous Systems.

- *Parallel Heterogeneous Systems*
  - Communication-aware static task scheduling algorithms for multicore and distributed systems: in a ground work, it was shown the impact of communication for task scheduling in cluster systems [?], and new system model and scheduling algorithms were proposed [?]. These contributions have a significant impact in static task scheduling and they represent an unavoidable research basis for current scientific studies in parallel and distributed systems (more than 250 citations in the Scholar).
  - Insightful performance modeling of multi-core architectures: this recent contribution tackles the important topic of roofline modeling for multi-cores (very much used, more than 100 citations just in 2014). To overcome serious limitations of the original model, the Cache-Aware Roofline Model (CARM) [?] explicitly considers a complete memory hierarchy when describing the performance of multi-core architectures.
  - On-the-fly performance modeling and dynamic load balancing for heterogeneous systems: these contributions also led to development of several on-the-fly performance modeling and scheduling algorithms for heterogeneous multi-core systems, namely for parallel CPU+GPU systems and highly heterogeneous multi-cluster environments; these algorithms have been applied for a plethora of different applications, such as video encoding, data-base applications, linear algebra and digital signal processing [?, ?], [?].
- *Hardware Accelerators*
  - Pioneer work on programming models and tools for stream-based computing, when in early 2000's, GPU programming and execution models were proposed for the first time (as the forerunners to nowadays common concepts), e.g. *flow-model* for stream computing and the programming tool and run-time system Caravela [?], with its extension to GPU-based distributed computing [?]. This work opened gates to the use of GPUs beyond their graphics purposes, e.g., for solving regular and irregular Low-Density Parity-Check (LDPC) [?, ?], [?, ?].

- Theoretical formulation of computational redundancy in predictive video coding approaches [?]: served as the basis for further investigation and practical application to exploit redundancy in all current video encoding standards Discrete Cosine Transform (DCT) based or integer DCT-based transforms [?].
- Design of specific programmable and dedicated accelerators, mostly for signal processing and cryptography: fully exploiting data and spatial parallelism [?] [W.16] [?] and also parallelism at arithmetic level, for example by investigating Residue Number Systems (RNS) based parallel cryptographic systems [?, ?], and energy-efficiency in embedded systems [?] [?].

5 Publications

190 publications in DBLP, more than 1400 citations registered in Scopus (h-index 19), and more than 3000 in the Google Scholar (h-index 27), the most relevant are listed below.

5.1 Textbook

[B.1] J. Martins and L. Sousa, *Bioelectronic Vision: Retina Models, Evaluation Metrics, and System Design*, volume 3 of *Series on Bioengineering & Biomedical Engineering*, World Scientific, London, March 2009.

5.2 Journal papers

5.3 Conference papers (refereed)

5.4 Workshop papers (refereed)

[W.1] S. Momcilovic, N. Roma and L. Sousa, "Multi-level parallelization of advanced video coding on hybrid CPU+GPU platforms," in *International Workshop on Algorithms, Models and Tools for Parallel Computing on Heterogeneous Platforms (HeteroPar)*, August 2012.

[W.2] A. Ilic and L. Sousa, "Simultaneous multi-level divisible load balancing for heterogeneous desktop systems," in *ISPA 2012, International Workshop on Heterogeneus Architectures and Computing*, March 2012, pp. 683–690.

[W.3] A. Ilic and L. Sousa, "Scheduling divisible loads on heterogeneous desktop systems with limited memory," in *Workshop on Algorithms, Models and Tools for Parallel Computing on Heterogeneous Platforms (HeteroPar)*, July 2011.

[W.4] P. Petrides, F. Pratas, L. Sousa and P. Trancoso, "Virtualization for morphable multi-cores," in *Workshop on Parallel Programming and Run-time Management Techniques for Many-core Architectures*, January 2011.

[W.5] R. Ramalho, P. Tomás and L. Sousa, "Efficient independent component analysis on a GPU," in *Proceedings of the International Workshop on Frontier of GPU Computing (FGC)*, IEEE Computer Society Press, July 2010.

[W.6] A. Rodrigues, N. Roma and L. Sousa, "p264: Open platform for designing parallel H.264/AVC video encoders on multi-core systems," in *Proceedings of the International Workshop on Network and Operating Systems Support for Digital Audio and Video (NOSSDAV)*, ACM, June 2010, pp. 81–86.

[W.7] A. Ilic and L. Sousa, "Collaborative execution environment for heterogeneous parallel systems," in *Proceedings of the 12th Workshop on Advances in Parallel and Distributed Computational Models (APDCM/IPDPS 2010)*, May 2010.

[W.8] F. Pratas, R. Mata and L. Sousa, "Iterative induced dipoles computation for molecular mechanics on GPUs," in *Proceedings of the 3rd Workshop on General Purpose Processing on Graphics Processing Units (co-located with ASPLOS)*, ACM, February 2010, pp. 111–120.

[W.9] S. Momcilovic and L. Sousa, "Development and evaluation of scalable video motion estimators on GPU," in *Proceedings of the Workshop on Signal Processing Systems (SiPS)*, IEEE, October 2009, pp. 291–296.

[W.10] F. Pratas and L. Sousa, "Applying the stream-based computing model to design hardware accelerators: A case study," in *Proceedings of the International Workshop on Systems, Architectures, Modeling, and Simulation*, Springer, July 2009, LNCS, pp. 237–246.

[W.11] T. Tulabandhula, S. Antão and L. Sousa, "A class of software-hardware processors for fingerprint matching on the fourier domain," in *Proceedings of the 3rd HiPEAC Workshop on Reconfigurable Computing*, January 2009.

[W.12] S. Yamagiwa and L. Sousa, "Design and implementation of a tool for modeling and programming deadlock free meta-pipeline applications," in *Proceedings of the 10th Workshop on Advances on Parallel and Distributed Processing Symposium (APDCM/IPDPS)*, IEEE, April 2008.

[W.13] S. Momcilovic and L. Sousa, "A parallel algorithm for advanced video motion estimation on multi-core architectures," in *Proceedings of the International Workshop on Multi-Core Computing Systems (MuCoCoS)*, IEEE, March 2008, pp. 831–836.

[W.14] G. Fernandes, S. Yamagiwa, V. Silva and L. Sousa, "Stream-based LDPC decoding on GPUs," in *Proceedings of the First Workshop on General Purpose Processing on Graphics Processing Units*, September 2007.

[W.15] S. Momcilovic, N. Roma and L. Sousa, "An ASIP approach for adaptive motion estimation on AVC," in *Proceedings of the IEEE 3rd Conference on PhD Research in Microelectronics and Electronics (PRIME)*, July 2007, pp. 165–168.

[W.16] R. Chaves, G. Kuzmanov, L. Sousa and S. Vassiliadis, "Improving SHA-2 hardware implementations," in *Proceedings of the Workshop on Cryptographic Hardware and Embedded Systems (CHES)*, Springer, October 2006, LNCS, pp. 298–310.

[W.17] T. Dias, N. Roma and L. Sousa, "Low power distance measurement unit for real-time hardware motion estimators," in *Proceedings of the International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS)*, Springer, September 2006, volume 4148 of *Lecture notes in Computer Science*, pp. 247–255.

[W.18] R. Chaves, G. Kuzmanov, L. Sousa and S. Vassiliadis, "Rescheduling for optimized SHA-1 calculation," in *Proceedings of the SAMOS Workshop on Computer Systems Architectures Modelling and Simulation*, Springer, July 2006, volume 4017 of *LNCS*, pp. 425–434.

[W.19] R. Chaves, G. Kuzmanov, S. Vassiliadis and L. Sousa, "Reconfigurable memory based AES co-processor," in *Proceedings of IEEE 20th International Parallel & Distributed Processing Symposium, 13th Reconfigurable Architectures Workshop*, IEEE Computer, April 2006.

[W.20] R. Piedade and L. Sousa, "Configurable embedded core for controlling electro-mechanical systems," in *Proceedings of the Applied Reconfigurable Computing Workshop (ARC)*, Springer Verlag, February 2006, volume 3985 of *Lecture notes on Computer Science*, pp. 18–23.

[W.21] T. Dias, N. Roma and L. Sousa, "Efficient motion vector refinement architecture for sub-pixel motion estimation systems," in *Proceedings of IEEE Workshop on Signal Processing Systems (SiPS)*, Atenas, Grécia, November 2005, pp. 313–318.

[W.22] O. Sinnen and L. Sousa, "Task scheduling: Considering the processor involvement in communication," in *Proceedings of the IEEE International Workshop on Algorithms, Models and Tools for Parallel Computing on Heterogeneous Networks (HeteroPar)*, Cork, Irlanda, July 2004, pp. 328–335.

[W.23] O. Sinnen and L. Sousa, "Comparison of contention aware list scheduling heuristics for cluster computing," in *Proceedings of the Workshop on Scheduling and Resource Management for Cluster Computing (ICPP)*, IEEE Computer Society Press, Valência, Espanha, September 2001, pp. 382–387.

[W.24] N. Roma and L. Sousa, "Parameterizable hardware architectures for automatic synthesis of motion estimation processors," in *Proceedings of IEEE Workshop on Signal Processing Systems (SiPS)*, Antuérpia, Bélgica, September 2001, pp. 428–439.

[W.25] N. Roma and L. Sousa, "On the development and evaluation of specialized processors for computing high-order 2-D image moments in real-time," in *Proceedings of the International Workshop on Computer Architectures for Machine Perception*, IEEE, Padova, Itália, September 2000, pp. 170–179.

[W.26] J. Brito and L. Sousa, "A video codec based on the TMS320C6X DSP," in *Proceedings of the European DSP Education and Research Conference*, Texas Instruments, Paris, França, September 2000.

[W.27] L. Sousa and N. Roma, "On the design of low-power array architectures for motion estimation," in *Proceedings of the IEEE 3rd Workshop on Multimedia Signal Processing*, Copenhaga, Dinamarca, September 1999, pp. 679–684.

[W.28] A. Abreu, N. Roma, J. Gerald and L. Sousa, "Digital video transmission through the electrical power lines," in *Proceedings of the European DSP Education and Research Conference*, Texas Instruments, Paris, França, September 1998, pp. 16–21.

[W.29] A. Costa, J. Bárrios, L. Sousa and M. Piedade, "Low and intermediate parallel image processing for transputer base systems," in *Proceedings of the European Workshops on Parallel Computing*, Barcelona, Espanha, March 1992, pp. 393–396.

[W.30] O. Mealha, J. Delgado and L. Sousa *et al*, "PARSEC-parallel computing in signal processing and environments for concurrent systems," in *Proceedings of the Second Workshop of the Parallel Computing Action*, Directorate General XXIII, Commission of the European Communities, December 1990, pp. 378–395.

5.5 Book Chapters

[BC.1] N. Pinckney, D. Harris, N. Jiang, K. Kelley, S. Antao and L. Sousa, *Circuits and Systems for Security and Privacy*, CRC Press, chapter Public Key Cryptography, pp. 109–182, May 2016.

[BC.2] R. Chaves, L. Sousa, N. Sklavos, A. Fournaris, G. Kalogeridou, P. Kitsos and F. Sheikh, *Circuits and Systems for Security and Privacy*, CRC Press, chapter Secure Hashing: SHA-1, SHA-2, and SHA-3, pp. 81–107, May 2016.

[BC.3] J. Andrade, G. Falc ao, V. Silva, S. Yamagiwa and L. Sousa, *Encyclopedia of Computer Science and Technology*, Taylor and Francis Group, chapter Accelerating Conventional Processing Using GPU Clusters: LDPC Decoders, 2015.

[BC.4] L. Kuan, P. Tomás and L. Sousa, *Numerical Computations with GPUs*, Springer, chapter Finite-Difference in Time-Domain scalable implementations on CUDA and OpenCL, July 2014.

[BC.5] A. Ilic and L. Sousa, *High-Performance Computing on Complex Environments*, Wiley, chapter 14: Efficient Multilevel Load Balancing on Heterogeneous CPU + GPU Systems, pp. 261–279, June 2014.

[BC.6] D. Clarke, A. Ilic, A. Lastovetsky, V. Rychkov, L. Sousa and Z. Zhong, *High-Performance Computing on Complex Environments*, Wiley, chapter 13: Design and Optimization of Scientific Applications for Highly Heterogeneous and Hierarchical HPC Platforms Using Functional Computation Performance Models, pp. 237–257, June 2014.

[BC.7] S. Ant ao, R. Chaves and L. Sousa, *Embedded Systems: Hardware, Design and Implementation*, John Wiley & Sons, chapter 14: Reconfigurable Architecture for Cryptography over Binary Finite Fields, pp. 319–362, January 2013.

[BC.8] A. Ilic, F. Pratas, P. Trancoso and L. Sousa, *High Performance Computing: From Grids and Clouds to Exascale*, IOS Press, chapter High-Performance Computing on Heterogeneous Systems: Database Queries on CPU and GPU, pp. 202–222, September 2011.

[BC.9] P. Tomás, A. Ilic and L. Sousa, *Biomedical Diagnostics and Clinical Technologies: Applying High-Performance Cluster and Grid Computing*, IGI Global, chapter 9: Massive Data Classification of Neural Responses, February 2010.

[BC.10] G. Falc ao, V. Silva and L. Sousa, *GPU Computing Gems*, Morgan Kaufmann, chapter 39: Parallel LDPC Decoding, December 2010.

[BC.11] Gabriel Falc ao, Vitor Silva, José Marinho and Leonel Sousa, *WIMAX New Developments*, IN-TECH, chapter 6: LDPC Decoders for the WiMAX (IEEE 802.16e) based on Multicore Architectures, pp. 133–150, December 2009.

[BC.12] M. Piedade, J. Gerald, L. Sousa and G. Tavares, *VLSI Circuits for Biomedical Applications*, Artech House, chapter 2: Visual Cortical Neuroprosthesis: A System Approach, pp. 25–43, April 2008.

[BC.13] S. Yamagiwa and L. Sousa, *Concurrent & Parallel Computing: Theory, Implementation and Applications*, Nova Science Publishers, chapter 1. Caravela: A High Performance Stream-based Concurrent Computing Platform, pp. 1–37, 2008.

[BC.14] N. Roma, T. Dias and L. Sousa, *New Algorithms, Architectures and Applications for Reconfigurable Computing*, Lysaght P. e Rosenstiel W. (Eds.), Springer-Verlag, chapter 5. Customisable and Reduced Hardware Motion Estimation Processors, pp. 55–66, 2005.

[BC.15] L. Sousa, P. Tomás, F. Pelayo, A. Martinez, C. Morillas and S. Romero, *New Algorithms, Architectures and Applications for Reconfigurable Computing*, Lysaght P. e Rosenstiel W. (Eds.), Springer-Verlag, chapter 22. Bioinspired Stimulus Encoder for Cortical Visual Neuroprostheses, pp. 279–290, 2005.

[BC.16] L. Sousa and N. Roma, *SOC Design Methodologies*, Kluwer Academic Publishers, volume 218 of *IFIP International Federation for Information Processing*, chapter A New VLSI Architecture for Full Search Block Matching Motion Estimation, pp. 253–264, 2002.

[BC.17] L. Sousa and M. Piedade, *Parallel Algorithms for Digital Image Processing, Computer Vision and Neural Networks*, Ioannis Pitas (Ed.), John Wiley & Sons, Nova Iorque, chapter Low Level Parallel Image Processing, pp. 25–52, 1993.

5.6 Edited Books, Proceedings, and Special Issues

[E.1] Amir Molahosseini, Leonel Sousa and Chip Hong Chang (eds.), *Embedded Systems Design with Special Arithmetic and Number Systems*, Springer, 2016, in Press.

[E.2] Farhana Sheikh and Leonel Sousa (eds.), *Circuits and Systems for Security and Privacy*, CRC Press, May 2016, ISBN 9781482236880.

[E.3] YongHong Tian, Min Chen and Leonel Sousa (eds.), *Ubiquitous Multimedia: Emerging Research on Multimedia Computing*, volume 23, IEEE MultiMedia, February 2016.

[E.4] Min Chen, Leonel Sousa and YongHong Tian (eds.), *Special Issue of ISM'16*, volume 10, Int. J. Semantic Computing, August 2016.

[E.5] Leonel Sousa and Nuno Roma (eds.), *Special Issue The Circuits and Systems for HEVC and 3D/SVC*, Journal of Real Time Image Processing, Springer, 2016.

[E.6] Y. Robert, Leonel Sousa and Denis Trystram (eds.), *Special Issue Follow-on of ISPDC'2009 and HeteroPar'2009*, volume 37, Parallel Computing, Elsevier, August 2011.

[E.7] H. Lin, M. Alexander, M. Forsell, A. Knüpfer, R. Prodan, L. Sousa and A. Streit (eds.), *Euro-Par 2009 - Parallel Processing Workshops*, volume 6043 of *Lecture Notes in Computer Science*, Springer, June 2010.

[E.8] L. Sousa and Yves Robert (eds.), *Proceedings of the Eighth International Symposium on Parallel and Distributed Computing*, IEEE Computer Society, July 2009, ISBN 978-0-7695-3680-4.

[E.9] L. Sousa, N. O'Connor, M. Mattavelli and A. Nunez (eds.), *EURASIP Journal of Embedded Systems*, Editor responsável pelo número especial em *Embedded Systems for Portable and Mobile Video Platforms*, February 2007.

6 Supervision Ph. D. and (before Bologna) Master Theses

6.1 PhD Theses

2016 Lídia Kuan, "Exploiting Parallel Heterogeneous Systems for Scientific Computations", Electrical and Computer Engineering Department (DEEC), IST (co-supervisor). First Employment: RiskCo, Portugal.

2015 Tiago Dias, "High Performance and Scalable Unified Architectures for Transform and Quantization in H.264/AVC Codecs", Electrical and Computer Engineering Department (DEEC), IST (co-supervisor). First Employment: Instituto Politécnico de Lisboa, Portugal.

2015 Pedro Matutino, "Residue Number Systems: Efficient Architectures and Circuits", Electrical and Computer Engineering Department (DEEC), IST. First Employment: Instituto Politécnico de Lisboa, Portugal.

2014 Aleksandar Ilic, "Heterogeneous Systems: Load Balancing and Performance Modeling", Electrical and Computer Engineering Department (DEEC), IST. First Employment: Pos-Doc at INESC-ID, Portugal.

2013 Samuel Antão, "High-performance and Embedded Systems for Cryptography", Electrical and Computer Engineering Department (DEEC), IST. First Employment: IBM Thomas J. Watson Research Center, NY, USA.

2013 João Martins, "Computational Models, Neuronal Metrics and System Identification in Bioelectronic Vision", (main advisor, co-advisor Prof. José Caeiro) Electrical and Computer Engineering Department (DEEC), IST. First Employment: Instituto Politécnico de Beja, Portugal.

2012 Frederico Pratas, "Stream-based Computing and Fine-grained Parallelism: from Algorithms to Reconfigurable Hardware", (main advisor, co-advisor Prof. Pedro Trancoso) Electrical and Computer Engineering Department (DEEC), IST. First Employment: Intel Labs Barcelona (ILBA), Spain.

2011 José Germano, "A Hand-held Microsystem for Biological Analysis: Electronics, Signal Acquisition and Processing for Information Extraction", Electrical and Computer Engineering Department (DEEC), IST. First Employment: Post-Doc at INESC-ID, Portugal.

2011 José Sarmento, "Optimized Digital Clock and Data Recovery Architectures", DEEC, IST. First Employment: Synopsis Portugal.

2011 Svetislav Momcilovic, "Parallel Video Coding on Multicore Platforms", DEEC, IST. First Employment: Post-Doc at INESC-ID, Portugal.

2010 Gabriel Fernandes, "Parallel Algorithms and Architectures for LDPC Decoding"(main advisor, co-advisor Prof. Vitor Silva), Electrical and Computer Engineering Department, Universidade de Coimbra. First Employment: Assistant Professor at Universidade de Coimbra.

2009 Pedro Tomás, "Neural Code: Tunning and Assessment of Retina Models", DEEC, IST. First Employment: Assistant Professor at DEEC, IST.

2008 Nuno Roma, "Transform domain video transcoding systems for static and dynamic video composition", DEEC, IST. First Employment: Assistant Professor at the Informatics and Computer Engineering Department (DEIC), IST.

2007 Ricardo Chaves, "Secure Computing on Reconfigurable Systems"(co-advisor), Faculty Electrical Engineering, Mathematics and Computer Science, Technical University of Delft. First Employment: Assistant Professor at the Informatics and Computer Engineering Department (DEIC), IST.

2003 Oliver Sinnen, "Accurate Task Scheduling for Parallel Systems", DEEC, IST. First Employment: Lecturer at the Department of Electrical and Computer Engineering (ECE), University of Auckland, New Zealand.

6.2 Master Theses (before-Bologna, half-way between MSc. and Ph. D.)

2007 Sérgio Martins, "Non-Linear Functionals for Retina Models", Master in Electrical and Computer Engineering, IST.

2007 Sérgio Capela, "Stochastic Integrate-and-Fire Retina Model", Master in Electrical and Computer Engineering, IST.

2007 Miguel Nuno Ribeiro, "A Configurable Processing Platform and its Application to Video Coding", Master in Electrical and Computer Engineering, IST.

2006 João Martins, "Computational Retina Models for Bioelectronic Vision", Master in Electrical and Computer Engineering, IST.

2006 Gustavo Rocha, "Graph Generation from Software Descriptions", Master in Electrical and Computer Engineering, IST.

2005 José Germano , "Portable System for DNA Analysis based on a Biochip"(co-supervised with Prof. Moisś Piedade), Master in Electrical and Computer Engineering, IST.

2005 Pedro Tomás, "Algorithms and Tools for Automatic Generation of DSP Hardware Structures", Master in Electrical and Computer Engineering, IST.

2004 Ricardo Guapo, "Programming and Evaluation of the Berkeley Socket Interface on the Maestro2 Communication System", Master in Electrical and Computer Engineering, IST.

2003 Tiago Dias, "High Performance VLSI Motion Estimation Processors: Data Reuse and Sub-Pixel Accuracy", Master in Electrical and Computer Engineering, IST.

2002 Ricardo Chaves, "RDSP: Processador Digital de Sinal com Suporte para Aritmética por Resíduos"(thesis written in portuguese), Master in Electrical and Computer Engineering, IST.

2002 José Salvado, "Codificação de Vídeo por Decomposição 3D baseada na Transformada de Ôndulas"(thesis written in portuguese), Master in Electrical and Computer Engineering, IST.

2001 Oliver Sinnen, "Experimental Evaluation of Task Scheduling Accuracy", Master in Electrical and Computer Engineering, IST.

2000 Nuno Roma, "Processadores Dedicados para Estimação de Movimento em Sequências de Vídeo"(thesis written in portuguese), Master in Electrical and Computer Engineering, IST.

7 Professional Services

7.1 Involvement on scientific and technical strategic discussions

2016 State of the Art and Research Roadmap for NESUS-WG1

2016 Co-organizer of the Tematic Session "Industry Activities related to Computing Systems in Portugal"as part of the programme of the Computing System Week (CSW) of the HiPEAC European Network of Excellence, Porto.

2015 Panelist in the panel "(Micro)Electronics Industry and University - interfaces questioned"in the *XXX Conference on Design of Circuits and Integrated Systems*, November in Estoril, Portugal, together with Michel Renovell, Antonio Torralba, Teresa Riesgo and Nuno Paulino.

2008 Participation in the Round table discussion: "Parallel and Distributed Computing in the Chip Multi-Processor System Era", in the *7th International Symposium on Parallel and Distributed Computing*, July in Krakow, Poland, together with Michael J. Flynn, Dean Tullsen and John Morrison.

2006 Involvement in the preparation of the document of the Thematic Group 7 "Tera-Device Computing and Beyond", which provides the European Commission with the vision, and also the major challenges

of computer engineering in Europe.

7.2 Editorial Services

2016 IEEE Transactions on Multimedia (TMM) Best Paper Award Selection Committee.

2016 Guest Co-Editor for the Special Issue of the IEEE Multimedia on "Ubiquitous Multimedia: Emerging Research on Multimedia Computing", with Min Chen and Yonghong Tian.

2016 Guest Co-Editor for the Special Issue of the International Journal of Semantic Computing (IJCS), extended best papers from ISM'2015, with Min Chen and Yonghong Tian.

2016 Guest Editor for the Special Issue of the Springer Journal of Real-Time Image Processing on "Real-Time Energy-Aware Circuits and Systems for HEVC and for its 3D and SVC Extensions", with Nuno Roma.

2015- Editor-in-Chief of the EURASIP Journal on Embedded Systems (JES), SpringerOpen Journal.

2015- Associate Editor and Member of the Editorial Board of the IET Electronics Letters.

2015 Nominated by the IEEE Computer Society Technical Committee on Multimedia Computing (TCMC) for the committee to select Special Issues and Survey/overview proposals to the IEEE Transactions on Multimedia (TMM).

2015 IEEE Transactions on Multimedia (TMM) Best Paper Award Selection Committee.

2014- Associate Editor and Member of the Editorial Board of the IEEE Transactions on Multimedia (TMM).

2014- Associate Editor and Member of the Editorial Board of the IEEE Transactions on Circuits and Systems for Video Technology (TCSVT).

2014- Associate Editor of the IEEE *Access*.

2013- Associate Editor of the Journal of Real-Time Image Processing, Springer.

2005-2014 Associate Editor of the EURASIP Journal on Embedded Systems (JES), SpringerOpen Journal.

2011 Guest editor for "Follow-on of ISPDC'2009 and HeteroPar'2009", volume 37, number 8 of the *Parallel Computing* journal, Elsevier, together with Y. Robert and Denis Trystram.

2010 Editor for "Euro-Par 2009 - Parallel Processing Workshops", Lecture Notes in Computer Science, volume 6043, Springer, together with H. Lin, M. Alexander, M. Forsell, A. Knüpfer, R. Prodan and A. Streit.

2009 Editor of the "Proceedings of the Eighth International Symposium on Parallel and Distributed Computing", IEEE Computer Society, with Yves Robert.

2007 Guest editor for "Embedded Systems for Portable and Mobile Video Platforms", special issue of the EURASIP Journal on Embedded Systems, together with N. O'Connor, M. Mattavelli and A. Nunez.

7.3 Chairmanship, and Steering Committee Appointments

2017 Program Co-Chair of the IEEE 3rd International Conference on Multimedia Big Data (BigMM 2017), California, USA.

2016 Publicity Committee Co-Chair of the IEEE International Symposium on Multimedia, San Jose, California, USA.

2015 Program Co-Chair of the IEEE International Symposium on Multimedia, Miami, Florida, USA.

2015 Co-Chair of the Special Session of ISCAS'15 on "Special Session on "Efficient Circuits and Systems for HEVC and its 3D Encoding Extension", Lisboa, Portugal.

2014 General Chair of 22th European Signal Processing Conference (EUSIPCO), EURASIP, Lisboa, Portugal.

2014 Track Chair of the the 25th International Symposium on Computer Architecture and High Performance Computing, Paris, France.

2013 Program Co-Chair of The Workshop on Power and Energy Aspects of Computation, co-located with the 10th International Conference on Parallel Processing and Applied Mathematics (PPAM), Warsaw, Poland.

2011 General Chair of Topic 3, *Scheduling and Load Balancing*, Euro-Par, Bordeaux, France.

2010 Co-Chair of The Applications, Systems, Architectures, and Processors Track, of the International Symposium on Systems, Architectures, MOdeling and Simulation, (IC-SAMOS), IEEE, Samos, Greece.

2010 General Co-Chair of the 4th HiPEAC Workshop on Reconfigurable Computing (WRC), co-located with the International Conference on High Performance Embedded Architectures & Compilers, Pisa, Italy.

2009 General Chair of the 8th International Symposium on Parallel and Distributed Computing (ISPDC), Lisboa, Portugal.

2009 Program Chair of the International Workshop on Algorithms, Models and Tools for Parallel Computing on Heterogeneous Networks (HeteroPar), co-located with Euro-Par, Delft, Netherlands.

2009 Program Co-Chair of the 3rd HiPEAC Workshop on Reconfigurable Computing, co-located with the International Conference on High Performance Embedded Architectures & Compilers, Paphos, Cyprus.

2011- Member of the Advisory Board of the EuroPar.

2010- Member of Steering Committee of the International Workshop on Algorithms, Models and Tools for Parallel Computing on Heterogeneous Platforms (HeteroPar).

2008-2011 Member of Steering Committee of the International Symposium on Parallel and Distributed Computing (ISPDC).

2008 International Liaison Co-Chair of the 5th International Conference on Ubiquitous Intelligence and Computing, Oslo, Norway.

7.4 Program Committee Membership

I have served on more than 100 Program and Technical Committees of Conferences and Workshops, some of the most relevant are listed below.

- IEEE IPDPS (International Parallel and Distributed Processing Symposium): 2014, 2013, 2012, 2010, 2007, 2003.
- IEEE International Conference on Computer Design (ICCD): 2015, 2014, 2013, 2012, 2011, 2010.
- IEEE/ACM International Conference on High Performance Computing (HiPC): 2016, 2015, 2014, 2012, 2011, 2010.
- ACM International Conference on Computing Frontiers: 2017, 2016, 2015, 2014, 2011
- IEEE International Conference on Parallel and Distributed Systems (ICPADS): 2008, 2006.
- International Conference on Parallel Processing (ICPP): 2014-2011.
- ACM International Conference on Supercomputing (ICS): 2006.
- IEEE International Symposium on Systems, Architectures, MOdeling and Simulation Workshop on Embedded Computer Systems: Architectures, Modeling, and Simulation (IC-SAMOS): 2016, 2015, 2014, 2013, 2012, 2011, 2010, 2009.
- Euro-Par: 2015, 2014, 2011.
- International Conference on Architecture of Computing Systems (ARCS): 2017, 2016, 2015, 2014, 2013, 2012, 2011, 2010, 2009.
- Euromicro Conference on Digital System Design: Architectures Methods and Tools (DSD): 2016-2010.
- International Symposium on Parallel and Distributed Computing (ISPDC): 2016-2009.
- International Conference on Parallel Processing and Applied Mathematics (PPAM): 2017, 2015, 2013, 2011, 2009.
- The First IEEE International Conference on Multimedia Big Data (BigMM): 2016, 2015
- IEEE International Symposium on Multimedia (ISM): 2015, 2014
- Wireless Innovation Forum Conference on Communications Technologies and Software Defined Radio (WinnComm): 2016, 2015, 2014, 2013
- 12th International Meeting on High Performance Computing for Computational Science (VECPAR): 2016
- IEEE International Conference on Acoustics, Speech and Signal Processing (ICASSP), track "Design and Implementation of Signal Processing Systems (DISPS)": 2016
- IEEE International Workshop on Signal Processing Systems (SiPS): 2016.
- HiPEAC Workshops WRC, PARMA-DITAM, and CS2 co-located with the HiPEAC conference: 2016-2014.

7.5 Reviewing for Scientific Journals and Textbooks

- Referee for the IEEE Transactions on Computers, IEEE Transactions on Parallel and Distributed Systems, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, IEEE Transactions on Circuits and Systems for Video Technology, IEEE Transactions on Circuits and Systems I: Regular Papers, IEEE Transactions on Circuits and Systems II: Express Briefs, IEEE Transactions on Signal Processing, IEEE Signal Processing Letters, IEEE Signal Communication Letters, ACM Journal of Experimental Algorithmics, IET Electronics Letters, IET Image Processing, IET Circuits, Devices & Systems, Springer Transactions on High-Performance Embedded Architectures and Compilers, Elsevier Journal of Parallel and Distributed Computing, Elsevier Signal Processing, Springer Journal of Supercomputing, Elsevier Journal of Systems Architecture, Elsevier The Journal of Systems and Software, Springer The Journal of Signal Processing Systems, Elsevier Journal of Real-Time Image Processing, Elsevier Integration, the VLSI Journal, Elsevier Computers and Mathematics with Applications, John Wiley & Sons International Journal of Circuit Theory and Applications.
- Review of textbooks for the IST Press (Academic Publisher, IST).

7.6 Professional Admissions and Promotions

12/2016 Member of the Committee to select and admit an Associate Professor for the Department of Electrical and Computer Engineering, Scientific Area of Electronics, IST, UL, Portugal.

01/2016 Member of the Committee to select and admit an Associate Professor for the Department of Electrical and Computer Engineering, Faculdade de Ciências e Tecnologia, Universidade de Coimbra, Portugal.

12/2014 Member of the Committee to select and admit a Full Professor for the Department of Computer Science and Computer Engineering, Scientific Area of Computer Architecture and Operating Systems, IST, UL, Portugal.

12/2014 Member of the Committee to select and admit an Assistant Professor for the Department of Electrical and Computer Engineering, Scientific Area of Computer Architecture, IST, UL, Portugal.

12/2013 Member of the Committee to select and admit an Associate Professor for the Department of Electrical and Computer Engineering, Scientific Area of Electronics, IST, UL, Portugal.

4/2013 External Advisor for a promotion to Associate Professor, University College Dublin, Ireland.

7.7 Reviewing/Referring of Theses

06/09/2016 Jury of the Ph.D. dissertation of Nuno Miguel Lourenço Diegues, "Algorithms for Enhancing the Performance Robustness of Transactional Memory Systems", at Department of Computer Science and Engineering, IST, UL, Portugal.

29/04/2016 Jury Member of the Ph.D. dissertation of Hamid Arabnejad, "QoS based workflow scheduling on heterogeneous resources", Department of Electrical and Computer Engineering, Faculdade de Engenharia da Universidade do Porto, Portugal.

14/03/2016 Jury member of Dr. Octavian Adrian Postolache's Habilitation (Agregação in Portugal) at Department of Computer Science and Engineering, IST, UL, Portugal.

11/03/2016 Jury Member of the Ph.D. dissertation of Purnachand Nalluri, "A Fast Motion Estimation Algorithm and its VLSI Architecture for High Efficient Video Coding", Departamento de Eletrónica, Telecomunicações e Informática, Universidade de Aveiro, Portugal.

29/02/2016 Jury Member of the Qualifier Exam for the PhD of Roberto de Matos,"Unidade Aritmética Completa baseada em RNS para Alplicações com Ampla Faixa Dinâmica", Universidade Federal de Santa Catarina, Florianópolis, Brasil.

12/02/2016 Head of the Jury of the Ph.D. dissertation of Valter António Louzeiro Sádio, "Optimization of Charge Pump DC-DC Converters for Mobile Applications", at Department of Electrical and Computer Engineering, IST, UL, Portugal.

29/01/2016 Jury Member of the Ph.D. dissertation of Sergio Santander Jiménez,"Multiobjective Analysis and Inference of Phylogenetic Hypotheses by Means of Parallel and Bioinspired Computing", Universidade de Extremadura (opponent), Spain.

26/01/2016 Jury Member of the Ph.D. dissertation of João Maria Duarte Andrade, "Design Space Exploration of LDPC Decoders on Programmable and Reconfigurable Architectures", at Department of Electrical and Computer Engineering, Universidade de Coimbra (opponent), Portugal.

23/10/2015 Jury Member of the Ph.D. dissertation of Rui Jorge Melo Teixeira, "Camera Calibration and Real-Time Image Processing in Heterogeneous Architectures – Application in Medical Endoscopy", at Department of Electrical and Computer Engineering, Universidade de Coimbra (opponent), Portugal.

09/10/2015 Jury Member of the Ph.D. dissertation of Rui Jorge Melo Teixeira, "Combining Predictive and Distributed Video Coding", at Department of Electrical and Computer Engineering, IST, UL, Portugal.

14/09/2015 Jury of the Habilitation (Agregação in Portugal) of Dr. João Manuel Paiva Cardoso at Department of Electrical and Computer Engineering, Faculdade de Engenharia da Universidade do Porto, Portugal.

23/07/2015 Head of the Jury of the Habilitation (Agregação in Portugal) of Dr. Pedro Manuel Santos de Carvalho at Department of Electrical and Computer Engineering, IST, UL, Portugal.

19/06/2015 Jury Member of the Ph.D. dissertation of Unai Lopez Novoa, "Contributions to the Efficient Use of General Purpose Coprocessors: Kernel Density Estimation as a Case Study", Universidad del País Vasco(opponent), Spain.

29/12/2014 Head of the Jury of the Ph.D. dissertation of Luís Filipe Soldado Granadeiro Rosado, "New Eddy Current Probes and Digital Signal Processing Algorithms for Friction Stir Welding Testing", at Department of Electrical and Computer Engineering, IST, UL, Portugal.

29/12/2014 Head of the Jury of the Ph.D. dissertation of Tiago Miguel Lopes Marta da Costa, "Integrated Circuits for Interfacing Magnetoresistive Sensors: Applications to Biomedical Analysis and Eddy Current Testing", at Department of Electrical and Computer Engineering, IST, UL, Portugal.

12/12/2014 Head of the Jury of the Ph.D. dissertation of Carlos João Oliveira Moreira, "Digital Control in Integrated DC-DC Converters", at Department of Electrical and Computer Engineering, IST, UL, Portugal.

05/12/2014 Jury Member of the Ph.D. dissertation of Jorge Sevilla Cedillo, "A New Digital Repository for Hyperspectral Images based on Spectral Unmixing and Implemented on GPUs", Universidade de Extremadura (opponent), Spain.

04/12/2014 Head of the Jury of the Ph.D. dissertation of José Fernando de Jesus da Rocha, "Limitação da Tensão nos Dispositivos de Conversores CC-CC Integrados", at Department of Electrical and Computer Engineering, IST, UL, Portugal.

17/11/2014 Head of the Jury of the Ph.D. dissertation of Nuno Miguel da Luz Neves Guerreiro, "Fault list compression for cost-effective analog and mixed-signal fault simulation", at Department of Electrical and Computer Engineering, IST, UL, Portugal.

24/09/2014 Head of the Jury of the Ph.D. dissertation of Victor Manuel Antunes da Silva, "Reconfigurable Hardware using Magnetic Tunneling Junction Memories", at Department of Electrical and Computer Engineering, IST, UL, Portugal.

19/09/2014 Head of the Jury of the Ph.D. dissertation of Maria Luísa Pedro Brito da Torre Caeiro, "Common Radio Resource Management in Virtual Heterogeneous Networks", at Department of Electrical and Computer Engineering, IST, UL, Portugal.

08/09/2014 Head of the Jury of the Habilitation (Agregação in Portugal) of Dr. Nuno Horta at Department of Electrical and Computer Engineering, IST, UL, Portugal.

23/05/2014 Head of the Jury of the Ph.D. dissertation of Nuno Nogueira Dias, "High-Efficiency in Multi-Mode Integrated DC-DC Conversion", at Department of Electrical and Computer Engineering, IST, UL, Portugal.

31/03/2014 Head of the Jury of the Habilitation (Agregação in Portugal) of Dr. Horácio Neto at Department of Electrical and Computer Engineering, IST, UL, Portugal.

26/02/2014 Head of the Jury of the Ph.D. dissertation of António Couto Pinto, "A Flash ADC Architecture Tolerant to High Offset Voltage Comparators", at Department of Electrical and Computer Engineering, IST, UL, Portugal.

18/12/2013 Head of the Jury of the Ph.D. dissertation of Eduardo Pinheiro, "Unobstructive Vital Signs Monitoring of Wheelchair Users", at Department of Electrical and Computer Engineering, IST, UL, Portugal.

1/9/2013 Examiner of the Ph.D. dissertation of Jeremy Low Yung Shern, "VLSI Efficient RNS Scalers and Arbitrary Modulus Residue Generators", Nanyang Technological University, Singapore.

16/9/2013 Jury Member of the Ph.D. dissertation of Nelson Silva, "Reconfigurable Transmitters for Software Defined Radio", Universidade de Aveiro (opponent), Portugal.

13/12/2012 Jury member at Dr. José Monteiro's Habilitation (Agregação in Portugal) at Department of Computer Science and Engineering, IST, UL, Portugal.

1/4/2012 Examiner of the Ph.D. dissertation of Ramya Muralidharan, "Novel modulo multipliers for moduli $2^n - 1, 2^n, 2^n + 1$", Nanyang Technological University, Singapore.

6/6/2011 Jury Member of the Ph.D. dissertation of Arnaldo Azevedo, "Efficient Execution of Video Applications on Heterogeneous Multi- and Many-Core Processors", Computer Engineering, Delft University of Technology (opponent), The Netherlands.

21/12/2010 Jury Member of the Ph.D. dissertation of Kazeem Gbolagade, "Effective Reverse Conversion in Residue Number System Processors", Computer Engineering, Delft University of Technology (opponent), The Netherlands.

15/11/2010 Jury Member of the Ph.D. dissertation of João Ascenço, "Distributed Video Coding: Improving the RD Performance", Department of Electrical and Computer Engineering, IST, UL (opponent), Portugal.

2/07/2010 Jury Member of the Ph.D. dissertation of José Caeiro, "Detecção e Agrupamento de Contornos"(thesis written in portuguese), Department of Electrical and Computer Engineering, IST, UL, Portugal.

26/2/2010 Reviewer of the Ph.D. dissertaion of Otoniel Granado, "Fast and Efficient Coding Tools for Digital Image and Video Signals", *Departamento de Física Y Arquitectura de Computadores*, Universidad Miguel Hernández, Spain.

13/10/2008 Jury Member of the Ph.D. dissertation of Filipa Duarte, "A Cache-based Hardware Accelerator for Memory Data Movements", Computer Engineering, Delft University of Technology (opponent), The Netherlands.

15/09/2008 Jury Member of the Ph.D. dissertation of Sandra Jardim, "Algoritmos para Representação Esparsa e Robusta de Sinais"(thesis written in portuguese), Department of Electrical and Computer Engineering, IST, UL, Portugal.

29/8/2008 Jury Member of the Ph.D. dissertation of Daniel Larkin, "Energy Efficient Hardware Acceleration of Semantic Video Object Processing on Mobile Computing Platforms", School of Electronic Engineering, Dublin City University (opponent), Ireland.

18/7/2007 Jury Member of the Ph.D. dissertation of Paulo Nunes, "Rate Control for Object-based Video coding", Department of Electrical and Computer Engineering, IST, UL (opponent), Portugal.

8/6/2007 Jury Member of the Ph.D. dissertation of Arnaldo Oliveira, "Especialização e Síntese de Processadores para Aplicação em Sistemas de Tempo-Real"(thesis written in portuguese), Informatics, Telecommunications, and Electronics Department, Universidade de Aveiro (opponent), Portugal.

15/5/2006 Jury Member of the Ph.D. dissertation of Jaime Cardoso, "Metadata Assisted Image Segmentation", Department of Electrical and Computer Engineering, Faculdade de Engenharia da Universidade do Porto (opponent), Portugal.

19/11/2004 Jury Member of the Ph.D. dissertation of Pyrrhos Stathis, "Sparse Matrix Vector Processing Formats", Computer Engineering, Delft University of Technology (opponent), The Netherlands.

7/6/2004 Jury Member of the equivalence of the Ph. D. of José Rogado, "Aspects Materiels et Logiciels de la conception d'un systeme micro-ordinateur 16 bits", Department of Computer Science and Engineering, IST, UL, Portugal.

25/11/2002 Jury Member of the Ph.D. dissertation of Ana Freitas, "Estimação da Potência em Circuitos Digitais utilizando Técnicas de Enumeração Implícita"(thesis written in portuguese), Department of Electrical and Computer Engineering, IST, UL, Portugal.

2/4/2001 Jury Member of the Ph.D. dissertation of João Paiva Cardoso, "Compilação de Algoritmos em Java para Sistemas Computacionais Reconfiguráveis com Exploração de Paralelismo ao Nível das

Operações"(thesis written in portuguese), Department of Electrical and Computer Engineering, IST, UL, Portugal.

12/1/2001 Jury Member of the Ph.D. dissertation of Jorge Barbosa, "Paralelismo em Processamento e Análise de Imagens Médicas (thesis written in portuguese), Department of Electrical and Computer Engineering, Faculdade de Engenharia da Universidade do Porto (opponent), Portugal.

15/10/1997 Jury Member of the Ph.D. dissertation of José Neto Fernandes, "A Interpretação de Imagens Texturadas"(thesis written in portuguese), Department of Electrical and Computer Engineering, IST, UL, Portugal.

7.8 Reviewing of Grant Proposals and Projects

2016 Member of the evaluation panel in the area of ICT for the call for project proposals targeting 'Forcing Ahead with Research' from the Academy of Finland.

2014-16 Head of the National Panel for the final scientific evaluation of all projects in the area of Electrical Engineering funded by the FCT.

2014-16 Member of the National Panel for the scientific evaluation of the execution of the strategic plans of the research institutions for the year of 2014 funded by the FCT, in the areas of Computer Science and Electrical Engineering.

2015 Evaluator of Research Project Proposals to the H2020 program from the European Commission.

2015 Evaluator of Proposals of Projects under Scientific Bilateral Cooperation Agreements supported by FCT, namely within the scope of the FCT/CAPES (Brasil) Agreement.

2013 Evaluator of Applications to the "The Investigator Programme"of the Portuguese National Foundation for Science and Technology (FCT), which will contract 150 researchers at national level in three categories: Starting, Development and Consolidation of the research career.

2012 Member of the National Evaluation Panel for Fellowships and Grants in Computers Science and Electrical Engineering, Portuguese National Foundation for Science and Technology.

2012 Review of research grant proposals for the European Commission, EU Objective *ICT-2011.9.1: FET-Open - Challenging current Thinking* (FP7).

2012 Review of research grant proposals for the eScience Open Call for Converging Sciences, NWO, Netherlands.

2012 Review of research grant proposals for the Czech Science Foundation, the main public funding agency in the Czech Republic supporting all areas of basic scientific research.

2012 Review of research grant proposals for the Research Grants Council (RGC) of Hong Kong.

2011 Review of research grant proposals for the Research Grants Council (RGC) of Hong Kong.

2010 Review of research grant proposals for *Associate Teams program, l'Institut National de Recherche en Informatique et en Automatique* (INRIA), Paris, France.

2009 Review of research grant proposals for the *Earlier Carrer Research Excellence Award*, University of Auckland, New Zealand.

2008 Review of research grant proposals for the *Earlier Carrer Research Excellence Award*, University of Auckland, New Zealand.

2007 Review of research grant proposals for the European Commission, EU program *Information and Communication Technologies - Future & Emerging Technologies* (FP7-ICT-2007-C) (FP7).

2007 Review of research grant proposals for Programa Operacional Ciência e Inovação 2010, medida V.5 "Investigação, desenvolvimento tecnológico e inovação em cooperação europeia e internacional", Portuguese Foundation for Science and Technology (FCT).

2005 Review of research grant proposals for *Associate Teams program, l'Institut National de Recherche en Informatique et en Automatique* (INRA), Paris, France.

2004 Review of research grant proposals for the 2nd edition of the I&D Program of the Electrical and Computer Engineering Department of the Faculty of Engineering, University of Porto, Portugal.

7.9 Juries for awards

2016 Member of the jury for awarding the "ANACOM-URSI Portugal Prize", valued at five thousand euros, for the best research work in the area of radio electricity, with the aim of stimulating creativity and rigour in scientific research work in Portugal.

2015 Member of the jury for awarding the "ANACOM-URSI Portugal Prize", valued at five thousand euros, for the best research work in the area of radio electricity, with the aim of stimulating creativity and rigour in scientific research work in Portugal.

2015 Member of the jury for awarding the best PhD thesis at IST in the years 2013-2014 in the areas of Electrical Engineering, Commputer Science, Physics and Mathematics, "Abreu Faro Prize".

2014 Member of the jury for awarding the "ANACOM-URSI Portugal Prize", valued at five thousand euros, for the best research work in the area of radio electricity, with the aim of stimulating creativity and rigour in scientific research work in Portugal.

2013 Member of the jury for awarding the "ANACOM-URSI Portugal Prize", valued at five thousand euros, for the best research work in the area of radio electricity, with the aim of stimulating creativity and rigour in scientific research work in Portugal.

2012 Member of the jury for awarding the "ANACOM-URSI Portugal Prize", valued at five thousand euros, for the best research work in the area of radio electricity, with the aim of stimulating creativity and rigour in scientific research work in Portugal.

7.10 Institutional Services

2016-2018 Member of the of the NATO Science for Peace and Security (SPS) Programme's 'Independent Scientific Evaluation Group' (ISEG).

2014-2016 Coordinator of the Committee for evaluating the scientific execution and outcome of all the research projects in the area of Electrical Engineering funded by the Portuguese Foundation for Science and Technology (FCT).

2013-2016 Member of the Scientific Council for the Exact Sciences and Engineering, composed by only 14 members chosen at National level, of the Portuguese Foundation for Science and Technology (FCT).

2012- Chair of the Commission D, in Electronics and Photonics, of the URSI-Portugal.

2009-2013 Chair of INESC-ID, a not for profit, privately owned institution of public interest, dedicated to advanced research and development in the domains of electronics, telecommunications and information technologies, with more than 1000 PhD researchers and owned by IST.

2015-2020 Member of Research Core Team and Management Committee of the Advanced Integrated Microsystems PhD Program, funded by the the Portuguese Foundation for Science and Technology (FCT) with a set of scholarships for 4 consecutive years.

2012-214 Member of the Scientific Council of the Doctoral Program in Electrical and Computer Engineering (PDEEC) at IST.

2002-2004 Member of the Scientific Committee of the Master in Electrical and Computer Engineering, responsible for the specialization in Electronics, IST.

2008-2012 Coordinator of the MSc and BSc programs in ECE at IST, with more than 1500 students.

2008-2012 Member of the Coordinating Committee of Pedagogical Council of IST.

2010-2012 Member of the Commission's strategy of the Department of Electrical and Computer Enginering, IST.

2004-2008 Member of the Board of Directors of INESC-ID.

2012-2016 Vice-President of the Scientific Council of IST, with responsibility for research and doctoral programs.

2009-2012 One of the 20 members of the Scientific Council of IST, that play an important role in the governance of IST

2006-2007 Member of the Scientific Council of IST, that play an important role in the governance of IST

2013-2016 Chair of the Executive Board of the Electronics' Scientific Area in the Electrical and Computer Engineering Department, IST.

2001-2003 Member of the Executive Board of the Electronics' Scientific Area in the Electrical and Computer Engineering Department, IST.

8 International Talks and Tutorials

02/10/2016 "Performance, Power and Energy-Efficiency Insightful Modeling of Multi-Cores", tutorial on The 34th IEEE International Conference on Computer Design Computer Architecture (ICCD), Phoenix, USA.

27/09/2016 "CARM: Cache-aware Roofline model for Multicores", Computer Architecture Lab at Carnegie Mellon, Pittsburgh, USA.

15/07/2016 "Balancing Performance, Power and Energy-Efficiency on Multi-cores towards Exascale Computing", University of Tokyo, Japan.

29/06/2016 "Cache-aware Modeling of Multi-cores: Performance, Power and Energy-Efficiency", invited talk, School of Computer Science and Systems Engineering at Kyushu Institute of Technology, Fukuoka, Japan.

25/05/2016 "Towards Asymmetric Post-Quantum Embedded Encryption", Invited Talk, Emerging Technologies: Communications, Microsystems, Optoelectronics, Sensors, Montreal, Canada.

12/04/2016 "Heterogeneous Systems for Multimedia and Cryptography", Distinguished Lecture Series, Singapore University of Technology and Design (SUTD), Singapore.

3/04/2016 "Application-aware Task Management for Emerging Embedding Systems", invited lecture in **Universidade Federal de Santa Catarina** (CTC-UFSC), IEEE Technical Chapter IM09/CAS04/COM19, Florianopolis, Brasil.

29/02/2016 "Cache-Aware Roofline Model: Performance, Power and Energy-Efficiency", 3 hours Tutorial on the VII IEEE Latin American Symposium on Circuits and Systems (LASCAS 2016), Florianopolis, Brasil.

23/11/2015 "CARM: Cache-Aware Performance, Power and Energy-Efficiency Roofline Modeling", in **Compiler, Architecture and Tools Conference** (CATC), Intel, Haifa, Israel.

30/10/2015 "Application Guided Task Management on Heterogeneous Embedded Systems", in **Workshop on Intelligent Solutions in Embedded Systems** (WISES), Invited Presentation, Ancona, Italy.

9/7/2015 "Energy-aware Task Management for Heterogeneous Low-Power Systems", in **Algorithms and Scheduling Techniques to Manage Resilience and Power Consumption in Distributed Systems**, Dagstuhl Seminar 15281, Germany.

26/9/2014 "Public-Key Cryptography on SIMD Embedded Engines", invited talk in the Centro de Investigación en Tecnoloxías da Información (CITIUS) Universidade de Santiago de Compostela. Spain.

1/7/2014 "Coping with Complexity: CPUs, GPUs and Real-world Applications", invited talk in the 9th *Scheduling in Aussois Workshop*, CNRS/INRIA, Lyon, France.

9/6/2014 "Modeling and Load Balancing for Multicore Systems", invited talk in the Department of Electrical and Computer Engineering (ECE), University of Auckland, New Zealand.

10/2/2014 "Overhauling Multicores Performance: Modeling and Load Balancing", keynote speaker in the 12th International Conference on Parallel and Distributed Computing and Networks, Innsbruck, Austria.

10/9/2013 "Monitoring Performance and Power for Application Characterization with Cache-aware Roofline Model", keynote speaker in the 10th International Conference on Parallel Processing and Applied Mathematics (PPAM), Warsaw, Poland.

26/6/2013 Organizes and chairs the breakout session on "Future Computing", integrated in the "*FET-Flagship HBP: Workshop on Human Brain Project: A roadmap for Portugal*".

24/5/2013 "Stream-based computing: Principles and case studies", invited talk in the Universidad Caceres, Spain.

6/2/2013 "Stream-based computing and fine-grained parallelism", invited talk in the Graduate School of Systems and Information Engineering, University of Tsukuba, Japan.

24/6/2011 "Distributed Computing on Highly Heterogeneous Systems", invited talk in the International Advanced Workshop on High Performance Computing, GRIDS and clouds (HPC 2011), Cetraro, Italy.

30/5/2011 *"Bandwidth-Aware Scheduling for On-Chip Cluster Architectures", invited talk in the 4th Scheduling in Aussois Workshop, CNRS/INRIA, Aussois, France.*

1/11/2010 *"RNS: Fundamentals and Applications", invited talk, Faculty of Electronic Engineering, University of Niš, Serbia.*

24/6/2010 *"Efficient Execution on Heterogeneous Systems", invited talk in the International Advanced Workshop on High Performance Computing, GRIDS and clouds (HPC 2010), Cetraro, Italy.*

2/6/2010 *"Cooperative Execution on Heterogeneous Multicore Systems", invited talk in the 3rd Scheduling in Aussois Workshop, CNRS/INRIA, Aussois, France.*

4/2/2010 *"Foreseeing the Role of Reconfiguration in Multicore Architectures", keynote speaker in the VI Jornadas sobre Sistemas Reconfiguráveis (REC'2010), Universidade de Aveiro, Portugal.*

16/12/2009 *"AES and EC Cryptographic Processor with Runtime Configuration", invited talk in the 17th International Conference on Advanced Computing and Communication, Bangalore, India.*

26/8/2009 *"Extending the application of GPUs beyond processing accelerators", Computer Engineering Colloquium, TU Delft, Netherlands.*

29/1/2009 *"Customizable Elliptic Curve Cryptography for Reconfigurable Devices", talk in the HiPEAC Reconfigurable Computing Cluster meeting, Paphos, Cyprus.*

20/11/2008 *"C(G)PUs: Arquitectura e Programação de Processadores Multicore", keynote speaker in the Quartas Jornadas de Engenharia de Electrónica e Telecomunicações e de Computadores, ISEL, Lisboa, Portugal.*

14/11/2008 *"Any-Core Memory-Centric Architecture for Advanced Video Coding", invited talk, Departamento Electrónica e Computación of Universidade de Santiago de Compostela, Spain.*

11/6/2008 *"What is so special in the Tomasulo hardware algorithm?", Seminar in the Seminal Seminar series, IST TagusPark, Portugal.*

26/8/2008 *"Stream-based concurrent computational models and programming tools", Invited talk in the Parallel Routines Optimization and Applications, Universidad de Murcia, Ministerio de Educación y Ciencia, Murcia, Spain.*

17/4/2007 *"Caravela: A Distributed Stream-Based Computing Platform", talk in the Compiler and Architecture Seminar, IBM Research Lab in Haifa, Israel.*

2/3/2007 *"Caravela distributed computing using stream-based processing", invited talk, Faculdade de Engenharia da Universidade do Porto, organizada em conjunto com o Instituto de Engenharia Biomédica.*

1/10/2003 *"Sistema de Visão Artificial não Invasivo", invited talk in the 2º Encontro de Engenharia Biomédica, Faculdade de Medicina da Universidade de Lisboa and IST, Portugal.*

9 Awarded Research Grants

9.1 Research funding

The first name corresponds to the Principal Investigator (PI).

2013-2016 Leonel Sousa (Member of the *Management Committee, Leader of Working Group 1 on "State of the art and continuous learning in Ultra Scale Computing Systems*), *et al.*, *Network for Sustainable Ultrascale Computing* (NESUS), EU ICT COST Action I1305.

2013-2016 Leonel Sousa, *Stretching the Limits of Parallel Processing on Heterogenous Computing Systems* (P2HCS), research project funded by the Portuguese Foundation for Science and Technology (FCT) (PTDC/EEI-ELC/3152/2012)- 153k €.

2012-2014 Leonel Sousa, NVIDIA CUDA Research Center INESC-ID/IST, one of 70 NVIDIA partners around the world - hardware and software donations and direct technology support.

2012- Leonel Sousa, Maxeler University Program INESC-ID/IST, - hardware and software donations, direct technology support, internships for students and collaborative research.

2011-2013 Nuno Roma, Leonel Sousa, *Heterogeneous Multicore Architecture for Biological Sequence Analysis* (HELIX), research project funded by the Portuguese Foundation for Science and Technology (FCT) (PTDC/EEA-ELC/ 113999/2009)- 200k €.

20011-2013 Sara Madeira, Leonel Sousa, *Understanding NEUROdegenerative diseases through CLINical and OMICS data integration* (NEUROCLINOMICS), research project funded by the FCT (PTDC/EEA-ELC/ 113999/2009)- 150k€.

2004-2015 Member of the *European Network of Excellence on High-Performance and Embedded Architecture and Compilation* (HiPEAC), FP7 - Information Society Technologies.

2010-2012 Ivan Milentijevic, Leonel Sousa, *et al.*, (PI, at national level) *National Platform for Knowledge Triangle in Serbia* (KNOWTS), Tempus Project, TEMPUS European (EU) Project (158881-TEMPUS-1-2009-1-RS-TEMPUS-JPHES).

2008-2013 Emmanuel Jeannot, Leonel Sousa (PI, at national level), *et al.*, *Open European Network for High Performance Computing on Complex Environments*, EU ICT COST Action IC0805.

2009-2010 Leonel Sousa, Jean-Claude Bajard, *Cryptographic Sistems based on Modular Arithmetic* (SCry-BAM), Research Program between Portugal and France- 6k€.

2009-2012 Harry Thewissen, Leonel Sousa, *et al.*, *Nanoelectronics for Safe, Fuel Efficient and Environment Friendly Automotive Solutions* (SE2A), EU *ENIAC Joint Undertaking*.

2008-2010 Moisés Piedade, Leonel Sousa, *Intracortical Neuronal Stimulator* (ICONS), research project funded by the FC)- 150k€.

2007-2009 João Lemos, Leonel Sousa, *Integrated Design for Automation of Anaesthesia* (IDEA), research project funded by the FCT (PTDC/EEA-ACR/69288/2006)- 100k€.

2005-2007 Leonel Sousa, *Adaptive H.264/AVC Motion Estimation Processor for Mobile and Battery Supplied Devices* (AMEP), research project funded by the FCT (FCT POSI/EEA-CPS/60765/2004)- 100k€.

2005-2008 Leonel Sousa, *Retina Neural Code: Accurate Modelling towards an Artificial Visual System* (RNC), research project funded by the FCT (FCT POSI/EEA-CPS/61779/2004)- 70k€.

2005-2006 Paulo Freitas, Leonel Sousa, *Magnetoresistive Biochip Microarray Platform for Biomolecular Recognition* (Biochip), research project funded by the FCT (FCT POSI/EEA-ESE/58523/2004)- 120k€.

2005 Leonel Sousa *Multimedia System for 3G Mobile Applications* (IVR), project funded by INOV - 10k€.

2002-2005 Eduardo Fernandez, Leonel Sousa, *al.*, *Cortical Visual Neuroprosthesis for the Blind* (CORTIVIS), EU project *key action 6* (QLK6-CT-2001-00279)- 200k€(budget for Portugal) .

2002-2004 Leonel Sousa, *Optimized and Reconfigurable Processing Structures for Motion Estimation* (COSME), research project funded by the FCT (FCT POSI/CHS/40877/2001) - 70k€.

1997-1999 *Developing Knowledge on ATM Technologies* (ATLANTIS), SINDEPEDIP, Medida 4.4, acção B 25/00167, Portuguese Ministry of Industry, responsible for the video coding component of the project - 40k€(800k PTE).

1990-1992 *Parallel Computing in Signal Processing and Environments for Concurrent Systems* (PARSEC-4121), EU "Parallel Computing Action" from the ESPRIT (ESPRIT PCA 4121).

9.2 Awards and Honors

2015 Selected ACM *Distinguished Scientist.*

2014 Designated Member of the *Design and Implementation of Signal Processing Systems Technical Committee* (DISP TC), IEEE Signal Processing Society.

2014 Designated Member of the IEEE *VLSI Systems & Applications Technical Committee* (VSATC), IEEE Circuits and Systems Society.

2013 Promoted to Fellow of the *Institution of Engineering and Technology* (IET), UK.

2010 Supervisor of the PhD thesis that got the second award of the 2010 **Fraunhofer Portugal Challenge**: "Flexible LDPC Decoders on Multicore Architectures", from Gabriel Falcão Fernandes (5k€).

2012-2010 Member of the Advisory Board of the *Computing Now*, from the IEEE Computer Society.

2009 **Best Researcher**, INESC -ID annual award to recognize the merit of their best researchers,the first edition of the award was exactly in 2009 (1k€). Jury of the prize: Prof. Srini Devadas (MIT), Prof. José Carlos Príncipe (University of Florida), Morris Sloman (Imperial College), and Franco Maloberti (University of Pavia).

2009, 2007 Two Honorable Mentions in the Scientific UTL/Santander Awards, which distinguish researchers or postdoctoral grantees from the Technical University of Lisbon that have published in the last five years in journals with more impact, based on the analysis provided by the ISI Web of Science.

2009 Supervisor of the MSc thesis awarded as the best MSc thesis in Instituto Superior Técnico in 2007/08 in the areas of Electrical and Computer Engineering and Informatics (award *Professor Luís Vidigal*, 5k€). Thesis "Portable Embedded Systems: Efficient Units for Data Processing and Cryptography", performed by Samuel Antão.

2009 Elevated to Senior Member of the *Association for Computing Machinery* (ACM).

2009 Designated member of the *International Federation for Information Processing* (IFIP), in the *Computer Systems Technology* Technical Committee (TC 10), *Concurrent Systems* Working Group (WG 10.3).

2004 Supervisor of the graduation thesis awarded as the best graduation thesis in Instituto Superior Técnico in 2002/2003 in the areas of Electrical and Computer Engineering and Informatics (award *Professor*

Luís Vidigal, 5k€). Thesis "Bio-Inspired Processing Module for the Development of an Artificial Retina", performed by Pedro Tomás.

2003 Elevated to Senior Member of the *Institute of Electrical and Electronics Engineers* (IEEE).

2003 Awarded with a scholarship from FCT, for a period of 6 months, to visit the *Delft University of Technology*, Delft, Holand.

1990 Awarded with a scholarship from NATO, for a period of 1 month, NATO Advanced Study Institute, University of Dundee, Scotland.

Best paper and poster awards:

2013 T. Dias, N. Roma, and L. Sousa, **Best Paper Award**, "High Performance Multi-Standard Architecture for DCT Computation in H.264/AVC High Profile and HEVC Codecs", Conference on Design and Architectures for Signal and Image Processing (DASIP2013),

2011 T. Dias, S. Lopez, N. Roma, and L. Sousa, "High Throughput and Scalable Architecture for Unified Transform Coding in Embedded H.264/AVC Video Coding Systems", **'Stamatis Vassiliadis' Best Paper Award**, 11th International Conference on Embedded Computer Systems: Architecture, Modeling and Simulation (SAMOS XI), IEEE.

2010 T. Dias, N. Roma, and L. Sousa, **Best Poster Award**, "Hardware/Software Co-design of H.264/AVC Encoders for Multi-core Embedded Systems", Conference on Design and Architectures for Signal and Image Processing (DASIP2010),

2009 S. Antão, R. Chaves and L. Sousa, **HiPEAC Paper Award**, "Compact and Flexible Microcoded Elliptic Curve Processor for Reconfigurable Devices", The 17th Symposium on Field-Programmable Custom Computing Machines (FCCM), IEEE.

Selected Publications

M. A. Şarkışla and A. Yurdakul, "SIMDify: Framework for SIMD-Processing with RISC-V Scalar Instruction Set," 19th Australasian Parallel and Distributed Computing (AusPDC'21), 1 - 5 February 2021, online.

Ö. F. Irmak and A. Yurdakul, "An Embedded RISC-V Core with Fast Modular Multiplication", arXiv:2009.14685, 2020.

N. Hilal and A. Yurdakul, "Model-based Design of a Roadside Unit for Emergency and Disaster Management," 3rd International W Intelligent Transportation and Connected Vehicles Technologies (ITCVT 2020), April 20, 2020, Budapest, Hungary

K. R Özyılmaz and A. Yurdakul, "IoT Blockchain Integration: A Security Perspective," in Security Analytics for Internet of Everythi Taylor & Francis Group, USA, February 2020.

İ. Taştan, M. Karaca and A. Yurdakul, "Approximate CPU Design for IoT End-Devices with Learning Capabilities," in Special Issue Techniques for Embedded Systems and Network-on-Chip Architectures, Electronics, vol 9., issue. 1, article no: 125, January 2020.

K. R. Özyılmaz and A. Yurdakul, "Designing a blockchain-based IoT infrastructure with Ethereum, Swarm and LoRa: The Software High-Availability with Security Minimal Risks," IEEE Consumer Electronics Magazine, vol. 8, pp. 28-34, March 2019.

K. R. Özyılmaz, M. Doğan and A. Yurdakul, "IDMoB: IoT Data Marketplace on Blockchain," Crypto Valley Conference on Blockcha (CVCBT'18), June 20-23, 2018, Zug, Switzerland.

A. V. Nurdağ, B. Arnrich and A. Yurdakul, "WiP: Daily Life Oriented Indoor Localization By Fusion Of Smartphone Sensors And W International Conference on Smart Computing (SMARTCOMP'18), June 18-20, 2018, Taormina, Italy.

M. Tükel, A. Yurdakul and B. Örs, "Customizable embedded processor array for multimedia applications," Integration-The VLSI Jo January 2018.

K. R. Özyılmaz and A. Yurdakul, "WiP: Integrating Low-Power IoT devices to a Blockchain-Based Infrastructure," International Co Embedded Software (EMSOFT'17), Oct. 15-20, 2017, Seoul, South Korea.

A. Yurdakul, "WiP: From SQL to Database Processors: A Retargetable Query Planner," Forum on Specification & Design Language 20, 2017, Verona, Italy.

B. Salami, G. A. Malazgirt, O. Arcas-Abella, A. Yurdakul and N. Sönmez, "AxleDB: A novel programmable query processing platfor Microprocessors and Microsystems: Embedded Hardware Design, vol. 51, pp. 142-164, June 2017.

G. A. Malazgirt and A. Yurdakul, "Prenaut: Design space exploration for embedded symmetric multiprocessing with various on-chi Journal of Systems Architecture: Embedded Software Design, vol. 72, pp. 3-18, January 2017.

M. Schmid, C. Schmitt, F. Hannig, G. A. Malazgirt, N. Sonmez, A. Yurdakul and A. Cristal, "Big Data and HPC Acceleration with Vi for Software Programmers, 2016, Springer, ISBN: 978-3-319-26406-6

S. Bayar and A. Yurdakul, "An Efficient Mapping Algorithm on 2-D Mesh Network-on-Chip with Reconfigurable Switches," 11th In Conference on Design &Technology of Integrated Systems in Nanoscale Era (DTIS'16), April 12-14, 2016, İstanbul, Turkey.

N. Aras and A. Yurdakul, "A New Multi-objective Mathematical Model for the High-level Synthesis of Integrated Circuits," Applied Modelling, Volume 40, Issue 3, pp. 2274-2290, 1 February 2016.

G. A. Malazgirt, D. Candaş and A. Yurdakul, "Taxim: A Toolchain for Automated and Configurable Simulation for Embedded Multi 4th International Workshop on High Performance Energy Efficient Embedded Systems (HIP3ES'16), Jan 18, 2016, Prag, Czech Re

G. A. Malazgirt, A. Yurdakul and S. Niar, "Customizing VLIW Processors from Dynamically Profiled Execution Traces," Microproce Microsystems: Embedded Hardware Design, vol. 39, no. 8, pp. 656–673, November 2015.

S. Bayar and A. Yurdakul, "PFMAP: Exploitation of Particle Filters for Network-on-chip Mapping," IEEE Transactions on VLSI De pp. 2116 - 2127, October 2015.

G. A. Malazgirt, B. Kıyan, D. Candaş, K. Erdayandı and A. Yurdakul, "Exploring Embedded Symmetric Multiprocessing with Variou Architectures," 13th International Conference on Embedded and Ubiquitous Computing (EUC'15), October 21-23, 2015, Porto, Por

G. A. Malazgirt, N. Sönmez, A. Yurdakul, O. Unsal and A. Cristal, "High Level Synthesis Based Hardware Accelator Design for Proc 12th FPGA World Conference (FPGAWORLD'15), September 8-10, 2015, Stockholm-Copenhag, Sweden-Denmark.

G. A. Malazgirt, N. Sönmez, A. Yurdakul, O. Unsal and A. Cristal, "Accelerating Complete Decision Support Queries Through High-Technology," 23rd ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA'15), February 22-25, 2015, I USA.

S. Niar, A. Yurdakul, O. Unsal, T. Tugcu and A. Yuceturk, "A Dynamically Reconfigurable Architecture for Emergency and Disaster ITS," 3rd International Conference on Connected Vehicles and Expo (ICCVE'14), Nov 3-7, 2014, Vienna, Austria.

G. A. Malazgirt, H.E. Yantir, A. Yurdakul and S. Niar, "Application Specific Multi-port Memory Customization in FPGAs," 24th Int Conference on Field Programmable Logic and Applications (FPL'14), September 2 - 4, 2014, Munich, Germany.

G. A. Malazgirt, A. Yurdakul and S. Niar, "WiP: MIPT: Rapid Exploration and Evaluation for Migrating Sequential Algorithms to M International Conference on High Performance Computing & Simulation (HPCS'14), July 21 - 25, 2014, Bologna, Italy.

H. E. Yantır and A. Yurdakul, "An Efficient Heterogeneous Register File Implementation for FPGAs," IEEE 21st Reconfigurable Ar Workshop (RAW'14), 19-20 May 2014, Phoenix, USA.

H. E. Yantır, S. Bayar and A. Yurdakul, "Efficient Implementations of Multi-pumped Multi-port Register Files in FPGAs," 16th EUI Conference on Digital System Design (DSD'13), September 4–6, 2013, Santander, Spain.

D. Fennibay, A. Yurdakul and A. Şen, "Introducing A Heterogeneous Simulation and Modeling Framework for Automation System Transactions on Computer Aided Design of Integrated Circuits and Systems, vol. 31, pp 1642-1655, November 2012.

G. A. Malazgirt, E. Çulha, A. Sen, İ. F. Başkaya and A. Yurdakul, "A Verifiable High Level Data Path Synthesis Framework," 15th EU Conference on Digital System Design (DSD'12), September 5–8, 2012, Izmir, Turkey.

S. Bayar and A. Yurdakul, "A Dynamically Reconfigurable Communication Architecture For Multicore Embedded Systems," Journa Architecture, vol. 58, pp. 140-159, February 2012.

S. Bayar, M. Tükel and A. Yurdakul, "A Self-Reconfigurable Platform for General Purpose Image Processing Systems on Low-Cost 6th International Workshop on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoc'11), June 20-22, 2011, Montpe

A. Yurdakul, B. Kurumahmut, G Kabukcu, "Generic Model for Application-Specific Processors on Reconfigurable Fabric," in Advar Methods from Modeling Languages for Embedded Systems and SoC's, Vol. 63, August 2010.

D. Fennibay, A. Yurdakul and A. Şen, "Introducing Hardware-in-Loop Concept to the Hardware/Software Co-design of Real-time I Proceedings of the 7th IEEE International Conference on Embedded Software and Systems (ICESS'10), June 29-July 1, 2010, Brad Kingdom.

D. Fennibay, A. Yurdakul and A. Şen, "Hardware-in-the-loop for hardware/software co-design of real-time embedded systems," D Designing for Embedded Parallel Computing Platforms: Architectures, Design Tools, and Applications, March 8-12, 2010, Frankfu

R. Ghamari and A. Yurdakul, "Register File Design in Automatically Generated ASIPs," 4th HiPEAC Workshop on Reconfigurable (WRC'10), Jan 23, 2010, Pisa, Italy.

B. Kurumahmut, G. Kabukcu, R. Ghamari and A. Yurdakul, "Design Automation Model for Application-Specific Processors on Rec Proceedings of Forum on Specification & Design Languages (FDL'09) , Sept. 22-24, 2009, Sophia Antipolis, France.

M. Erkoç and A. Yurdakul, "Halftoning Soft Cores for Low-Cost Digital Displays," Proceedings of 24th International SympoSİUm c Information Sciences (ISCIS'09), Sept. 14-16, 2009, Northern Cyprus.

M. Aktan, A. Yurdakul and G. Dündar, "An Algorithm for the Design of Low-Power Hardware Efficient FIR Filters," IEEE Transact Systems-I, vol. 55, no. 6, pp. 1536-1545, July 2008.

S. Bayar and A. Yurdakul, "Self-Reconfiguration on Spartan-III FPGAs with Compressed Partial Bitstreams via a Parallel Configura (cPCAP) Core," Proceedings of 4th conference on Ph.D. Research in Microelectronics and Electronics (PRIME'08), İstanbul, Turke

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G. Kabukcu and A. Yurdakul, "Low-Cost Solution to On-Line CFA Demosaicking," International Journal of Imaging Systems and T no. 4, pp. 232-243, December 2007.

N. Sönmez and A. Yurdakul, "SIxD: A Configurable Application-Specific SISD/SIMD Soft-Core," International Symposium on Syst (SoC'06), Tampere, Finland, 2006.

A. Yurdakul, "Multiplierless Implementation of 2D FIR Filters," Integration-The VLSI Journal, Volume 38, Issue 4 , pp 597-613, A

A. Özpınar and A. Yurdakul, "Configurable Design and Implementation of the Rijndael Algorithm-AES," 6th EUROMICRO Confer System Design (DSD'03), Antalya, Turkey, 2003.

A. Yurdakul and G. Dündar, "A Fast and Efficient Algorithm for the Multiplierless Realization of Linear DSP Transforms," IEE-Pro Devices, and Systems, vol 149, pp 205-211, 2002.

A. Yurdakul, "An Efficient Algorithm for the Multiplierless Realization of 2-D Linear Transforms," IEEE 10th Digital Signal Proces (DSP'02), Atlanta, USA, 2002.

J. O. Coleman and A. Yurdakul, "Fractions in the Canonical-Signed-Digit Number System," 35th Conference on Information Scien (CISS'01), Baltimore, Maryland, USA, 2001.

A. Yurdakul, "A Synthesis Tool for the Multiplierless Realization of FIR-Based Multirate DSP Systems," IEEE International Sympo Systems (ISCAS'00), vol. 4, pp. 69-72, Geneva, Switzerland, May 28-31, 2000.

A. Yurdakul and G. Dündar, "Multiplierless Realization of Linear DSP Transforms by Using Common Two-Term Expressions," Klu Signal Processing, vol. 22, pp 163-172, 1999.

A. Yurdakul and G. Dündar, "Statistical Methods for the Estimation of Quantization Effects in FIR-Based Multirate Systems," IEEI Signal Processing, vol. 47, pp 1749-1753, June 1999.

A. Yurdakul and G. Dündar, "A New Hybrid Algorithm for Over-the-Cells Routing," 8th Mediterranean Electrotechnical Conferenc vol. 3, pp. 480-483, Bari, Italy, 1996.

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