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NOTICE OF ALLOWANCE AND FEE(S) DUE

146018 7590 01/19/2021
Gardella Grace P.A.
80 M Street SE, 1st Floor
Washington, DC 20003

EXAMINER

ZHAO, BING

ART UNIT

PAPER NUMBER

2198

DATE MAILED: 01/19/2021

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/034,404	09/28/2020	Mark Henrik Sandstrom	P50206US09	4271

TITLE OF INVENTION: MANAGING RESOURCE SHARING IN A MULTI-CORE DATA PROCESSING FABRIC

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	\$600	\$0.00	\$0.00	\$600	04/19/2021

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

146018 7590 01/19/2021
Gardella Grace P.A.
80 M Street SE, 1st Floor
Washington, DC 20003

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/034,404	09/28/2020	Mark Henrik Sandstrom	P50206US09	4271

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nonprovisional	SMALL	\$600	\$0.00	\$0.00	\$600	04/19/2021

EXAMINER	ART UNIT	CLASS-SUBCLASS
ZHAO, BING	2198	718-104000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1	_____
2	_____
3	_____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☐ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies _____

4b. Method of Payment: (Please first reapply any previously paid fee shown above)

- ☐ Electronic Payment via EFS-Web ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)
- ☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____	Date _____
Typed or printed name _____	Registration No. _____



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Gardella Grace P.A. 80 M Street SE, 1st Floor Washington, DC 20003			ZHAO, BING	
			ART UNIT	PAPER NUMBER
			2198	
DATE MAILED: 01/19/2021				

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b) (2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 17/034,404	Applicant(s) Sandstrom, Mark Henrik	
	Examiner BING ZHAO	Art Unit 2198	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 12/29/2020 and telephone interviews ending on 12/18/2020.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on ____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are See Continuation Sheet. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov**.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
Certified copies:
a) ☐ All b) ☐ Some *c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
* Certified copies not received: ____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date ____.
Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892) 2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date <u>12/22/20(2), 12/29/20</u> . 3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material ____. 4. ☒ Interview Summary (PTO-413), Paper No./Mail Date. <u>20201219</u> .	5. ☒ Examiner's Amendment/Comment 6. ☒ Examiner's Statement of Reasons for Allowance 7. ☐ Other _____.
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/BING ZHAO/ Primary Examiner, Art Unit 2198	/BING ZHAO/ Primary Examiner, Art Unit 2198
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Continuation of 3. The allowed claim(s) is/are: 12-17, 20-32 and 35-37 renumbered as 1-22

DETAILED ACTION

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

1. Authorization for this examiner's amendment was given in a telephone interview with Ms. Natalie J. Grace, Reg. # 65803 on 12/18/2020.

2. **This listing of claims will replace all prior versions of claims:**

Claim 1-11. (Cancelled)

Claim 12 (Currently Amended). A method for task-switching on a multi-user parallel processing hardware architecture comprising a plurality of ~~programmable~~ reconfigurable logic-based processing units, the method comprising:

linking, through a first set of inter-task communication paths of the multi-user parallel processing architecture, a first set of ~~programmable~~ reconfigurable logic-based processing units of the plurality of ~~programmable~~ reconfigurable logic-based processing units into a first multi-stage program instance configured to execute a corresponding set of interdependent processing stages of a first program, wherein each of the first set of ~~programmable~~ reconfigurable logic-based processing units is programmed to perform a respective task of a plurality of first

tasks of the first program corresponding to a respective processing stage of the
first multi-stage program instance;

linking, through a second set of inter-task communication paths of the multi-user
parallel processing architecture, a second set of ~~programmable~~ reconfigurable
logic-based processing units of the plurality of ~~programmable~~ reconfigurable
logic-based processing units into a second multi-stage program instance
configured to execute a corresponding set of interdependent processing stages
of a second program, wherein each of the second set of ~~programmable~~
reconfigurable logic-based processing units is programmed to perform a
respective task of a plurality of second tasks of the second program
corresponding to a respective processing stage of the second multi-stage
program instance;

maintaining, in a storage, a first location for a first reconfigurable logic-based
processing unit of the first set of reconfigurable logic-based processing units
executing the first multi-stage program instance such that a first one or more ~~first~~
users and/or ~~first~~ programs are enabled to communicate directly with the first
multi-stage program instance;

maintaining, in the storage, a second location for a second reconfigurable logic-
based processing unit of the second set of reconfigurable logic-based processing
units executing the second multi-stage program instance such that a second one
or more ~~second~~ users and/or ~~second~~ programs are enabled to communicate
directly with the second multi-stage program instance; and

in response to an increased demand for the second program, reallocating, by a controller comprising software and/or hardware logic configured to implement a load-adaptive allocation policy, at least one processing unit of the first set of ~~programmable~~ reconfigurable logic-based processing units, the reallocating resulting in

- (1) switching the at least one of the first set of processing units from performing ~~any given~~ a task of the plurality of first tasks to performing ~~any given one~~ one task of the plurality of second tasks, wherein switching comprises ~~matching~~ updating a first ~~type~~ programming configuration of the at least one of the first set of processing units to a ~~type~~ programming configuration demanded by the ~~given one~~ one task, and
- (2) adjusting, in storage, at least one of the first location or the second location to enable, through the respective location, direct communication to the other multi-stage program instance of the first multi-stage program instance or the second multi-stage program instance;

wherein the load-adaptive allocation policy is configured to facilitate minimizing reconfiguring the plurality of reconfigurable logic-based processing units.

Claim 13 (Previously Presented). The method of claim 12, wherein at least one of the first program and the second program is a data processing service.

Claim 14 (Currently Amended). The method of claim 13, wherein the data processing service is available for use by ~~[[a]]~~ an external user or program of at least one of a) the first one or more users and/or programs or b) the second one or more users and/or

programs communicating with the respective program via a network connection with the multi-user parallel processing architecture.

Claim 15 (Previously Presented). The method of claim 12, wherein the at least one processing unit comprises at least one Field Programmable Gate Array (FPGA).

Claim 16 (Currently Amended). The method of claim 12, wherein the plurality of ~~programmable~~ reconfigurable logic-based processing units is included in an array of processing units.

Claim 17 (Previously Presented). The method of claim 16, wherein the load-adaptive allocation policy is configured to facilitate load balancing across the array of processing units.

Claim 18 (Cancelled).

Claim 19 (Cancelled).

Claim 20 (Currently Amended). The method of claim 12, wherein the controller is configured to monitor availability of the plurality of ~~programmable~~ reconfigurable logic-based processing units.

Claim 21 (Currently Amended). The method of claim 12, further comprising monitoring a first characteristic corresponding to at least one of the first program and the first set of ~~programmable~~ reconfigurable logic-based processing units, wherein the increased demand is determined at least in part by the monitoring of the first characteristic.

Claim 22 (Previously Presented). The method of claim 21, wherein the first characteristic comprises a data processing load.

Claim 23 (Previously Presented). The method of claim 21, wherein the first characteristic comprises a readiness to execute of one or more tasks of the plurality of first tasks.

Claim 24 (Currently Amended). A system for task-switching on a multi-user parallel processing hardware architecture comprising a plurality of ~~programmable~~ reconfigurable logic-based processing units, the system comprising:

the plurality of ~~programmable~~ reconfigurable logic-based processing units;
a reconfigurable cross-connect for establishing communication links between pairs of processing units of the plurality of ~~programmable~~ reconfigurable logic-based processing units; and
hardware logic and/or software logic configured to link, through the reconfigurable cross-connect, a first set of ~~programmable~~ reconfigurable logic-based processing units of the plurality of ~~programmable~~

reconfigurable logic-based processing units into a first multi-stage program instance configured to execute a corresponding set of interdependent processing stages of a first program, wherein each of the first set of ~~programmable~~ reconfigurable logic-based processing units is programmed to perform a respective task of a plurality of first tasks of the first program corresponding to a respective processing stage of the first multi-stage program instance,

link, through the reconfigurable cross-connect, a second set of ~~programmable~~ reconfigurable logic-based processing units of the plurality of ~~programmable~~ reconfigurable logic-based processing units into a second multi-stage program instance configured to execute a corresponding set of interdependent processing stages of a second program, wherein each of the second set of ~~programmable~~ reconfigurable logic-based processing units is programmed to perform a respective task of a plurality of second tasks of the second program corresponding to a respective processing stage of the second multi-stage program instance,

maintain, in a storage, a first location for a first reconfigurable logic-based processing unit of the first set of reconfigurable logic-based processing units executing the first multi-stage program instance such that a first one or more ~~first~~ users and/or ~~first~~ programs are enabled to communicate directly with the first multi-stage program instance,

maintain, in the storage, a second location for a second reconfigurable logic-based processing unit of the second set of reconfigurable logic-based

processing units executing the second multi-stage program instance such that a second one or more ~~second~~ users and/or ~~second~~ programs are enabled to communicate directly with the second multi-stage program instance, and in response to an increased demand for the second program, reallocate, according to a load-adaptive allocation policy, at least one processing unit of the first set of ~~programmable~~ reconfigurable logic-based processing units, the reallocating resulting in

(1) switching the at least one of the first set of processing units from performing ~~any given~~ a task of the plurality of first tasks to performing ~~any given~~ one task of the plurality of second tasks, wherein switching comprises ~~matching~~ updating a first ~~type~~ programming configuration of the at least one of the first set of processing units to a ~~type~~ programming configuration demanded by the ~~given one~~ task, and

(2) adjusting, in storage, at least one of the first location or the second location to enable, through the respective location, direct communication to the other multi-stage program instance of the first multi-stage program instance or the second multi-stage program instance;

wherein the load-adaptive allocation policy is configured to facilitate minimizing reconfiguring the plurality of reconfigurable logic-based processing units.

Claim 25 (Currently Amended). The system of claim 24, wherein the plurality of ~~programmable~~ reconfigurable logic-based processing units is included in an array of processing units.

Claim 26 (Previously Presented). The system of claim 25, wherein the array of processing units comprises a plurality of central processing units (CPUs) and/or graphics processing units (GPUs).

Claim 27 (Previously Presented). The system of claim 24, wherein at least one of the first program and the second program executes a data processing service.

Claim 28 (Currently Amended). The system of claim 24, further comprising a network connection for providing communication between an external user or program of at least one of a) the first one or more users and/or programs or b) the second one or more users and/or programs and the data processing service.

Claim 29 (Previously Presented). The system of claim 28, wherein providing communication comprises providing communication to the external user or program without awareness of the first location or the second location by the external user or program.

Claim 30 (Previously Presented). The system of claim 24, wherein the at least one processing unit comprises at least one Field Programmable Gate Array (FPGA).

Claim 31 (Currently Amended). The system of claim 24, wherein the plurality of ~~programmable~~ reconfigurable logic-based processing units is included in an array of processing units.

Claim 32 (Previously Presented). The system of claim 31, wherein the load-adaptive allocation policy is configured to facilitate load balancing across the array of processing units.

Claim 33 (Cancelled).

Claim 34 (Cancelled).

Claim 35 (Currently Amended). The system of claim 24, further comprising monitoring a first characteristic corresponding to at least one of the first program and the first set of ~~programmable~~ reconfigurable logic-based processing units, wherein
the increased demand is determined at least in part by the monitoring of the first
characteristic.

Claim 36 (Previously Presented). The system of claim 35, wherein the first characteristic comprises a data processing load.

Claim 37 (Previously Presented). The system of claim 35, wherein the first characteristic comprises a readiness to execute of one or more tasks of the plurality of first tasks.

Reason for Allowance

3. The following is an examiner's statement of reasons for allowance:

The prior arts of record when taken individually or in combination do not expressly teach or render obvious the limitations recited in claims 12 and 24, **when taken in the context of the claim as a whole**.

The closest prior art of record, **Nollet et al (U.S. Pu. 2009/0187756)**, **Young et al (U.S. Pat. 7669035)**, **Creamer et al (U.S. Pat. 8713574)**, **Yancey et al (U.S. Pat. 7444454)** and **Nordquist (U.S. Pat. 7447873)**, disclose different portions of the limitations of claim 12 and 24 (**Nollet**: Figs. 1-3, 6-12, 15A,B, [0012], [0014], [0024], [0026], [0029], , [0034], [0035], [0055], [0057], [0086], [0087], [0096]-[0098], [0102], [0108], [0160], [0161] teaches a plurality of *FPGAs/reconfigurable* devices being connected together in different topologies and communicate to one another through the *buses* of the topologies; the FPGAs are used to execute *tasks of applications*, that have a plurality of tasks that are linked together; the tasks can be *relocated* on different FPGAs based on *monitored* execution status of the tasks; **Young**: Figs. 5A-14C, col 10 lines 19-63, col 13 line 65 – col 14 line 40, col 15 line 15 – col 16 line 32: allocation of FPGAs involves creating different groupings of FPGAs based on task demands; the different groupings of FPGAs are linked together in hardware; **Creamer**: col 3 lines 55-

59, col 4 lines 38-65, col 5 lines 12-35, col 6 lines 1-40: teaches *reconfigurable cores* are dynamically chosen for a task in a way to minimize reconfiguration through using of already configured cores; **Yancey** abstract Figs. 1, 2, 7, 9, 10, 11 col 2 lines 45-67, col 3 lines 14-30, col 6 lines 1-12, 33-37, col 9 lines 9-30, col 10 lines 26-50, col 11 lines 39-50, col 12 lines 7-67, col 14 lines 1-29 set of computation cores can have *reconfigurable hardware architecture (RHA)*, such as *FPGAs*, that each have their own associated *memory resources*; these cores are connected by *multiplexers*, and when *data is ready* appropriate multiplexers connects a *FIFO* containing the data to a proper *destination FPGA*; **Nordquist**: Fig. 3, col 7 lines 35-42, col 8 lines 32-35, col 10 lines 20-23; Fig. 5 *VS, GS, PS, buffers*, col 7 lines 54-56, col 8 lines 27-30, col 9 lines 47-56, col 10 lines 1-23; col 10 lines 23-39, col 8 lines 31-35, col 10 lines 2-5, col 11 lines 20-21, 30-34, 65 – col 12 line 3, col 12 lines 30-35, 42-47, 53-59; col 13 lines 5-25, col 17 lines 31-52, col 13 lines 35-42, col 14 lines 15-37; col 17 lines 13-20, 25-30, col 18 lines 19-47 teaches memory resources being directly used by applications, where each application of the applications contains multiple application threads; the application threads has associated data buffers that stores input data for the threads and the input data are muxed to cores of the allocated cores); they however do not anticipate or render obvious the overall combined structure and features set forth in the independent claim 12 and 24, when viewed as an order whole of the different portions of the limitations contained therein.

These limitations are in conjunction with all the other limitations that are not specifically recited in the quotes. Thus for at least the foregoing reasons, the prior art of

record neither anticipates nor render obvious the present invention as set forth in the independent claims as a whole.

4. Any comments considered necessary by Applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement for Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BING ZHAO whose telephone number is (571)270-1745. The examiner can normally be reached on 9am - 5:30pm.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at <http://www.uspto.gov/interviewpractice>.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, An Meng-Ai can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/BING ZHAO/
Primary Examiner, Art Unit 2198