

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,
Petitioner,

v.

MASAHIRO IIDA,
Patent Owner.

Case No. IPR2023-00864
U.S. Patent No. 6,812,737

**PETITION FOR INTER PARTES REVIEW
UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. § 42.1 et seq.**

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1003	Declaration of Stephen W. Melvin, Ph.D.
1004	Curriculum Vitae of Stephen W. Melvin, Ph.D.
1005	Japanese Unexamined Patent Application Publication No. H09-121153A (“Fujii”), certified translation, and declaration of translator
1006	Vaughn Betz et al., <i>Architecture and CAD for Deep-Submicron FPGAs</i> (Kluwer Academic Publishers 1999) (“Betz”)
1007	U.S. Patent No. 6,097,212 (“Agrawal”)
1008	U.S. Patent No. 5,926,036 (“Cliff”)
1009	Declaration of Agnes O. Villero Regarding Betz, Brown-FPGA, Trimberger, and Bhat
1010	Prosecution History of Japanese Patent Application No. 2001-199644 (which issued as Japanese Patent No. 3580785B2), certified translation, and declaration of translator
1011	Stephen D. Brown et al., <i>Field-Programmable Gate Arrays</i> (Kluwer Academic Publishers 1992) (“Brown-FPGA”)
1012	Stephen M. Trimberger et al., <i>Field-Programmable Gate Array Technology</i> (Springer Science+Business Media New York 1994) (“Trimberger”)
1013	Stephen Brown & Jonathan Rose, “FPGA and CPLD Architectures: A Tutorial,” <i>IEEE Design and Test of Computers</i> , vol. 13, no. 2, 42-57 (Dec. 1996) (“Brown-Rose”) (from pages 4-19 of Declaration of Gordon MacPherson at Ex.1014)
1014	Declaration of Gordon MacPherson regarding Stephen Brown & Jonathan Rose, “FPGA and CPLD Architectures: A Tutorial,” <i>IEEE Design and Test of Computers</i> , vol. 13, no. 2, 42-57 (Dec. 1996)
1015	Jianshe He & Jonathan Rose, “Advantages of Heterogeneous Logic Block Architectures for FPGAs,” <i>Proceedings of IEEE Custom</i>

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	<i>Integrated Circuits Conference - CICC '93</i> (1993) (“He”) (from pages 4-8 of Declaration of Gordon MacPherson at Ex.1016)
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1017	Jonathan Rose et al., “Architecture of Field-Programmable Gate Arrays,” <i>Proceedings of the IEEE</i> , vol. 81, no. 7, 1013-29 (July 1993) (“Rose”) (from pages 4-20 of Declaration of Gordon MacPherson at Ex.1018)
1018	Declaration of Gordon MacPherson regarding Jonathan Rose et al., “Architecture of Field-Programmable Gate Arrays,” <i>Proceedings of the IEEE</i> , vol. 81, no. 7, 1013-29 (July 1993)
1019	Satwant Singh et al., <i>The Effect of Logic Block Architecture on FPGA Performance</i> , IEEE Journal of Solid-State Circuits, vol. 27, no. 3, 281-87 (Mar. 1992) (“Singh”) (from pages 4-10 of Declaration of Gordon MacPherson at Ex.1020)
1020	Declaration of Gordon MacPherson regarding Satwant Singh et al., <i>The Effect of Logic Block Architecture on FPGA Performance</i> , IEEE Journal of Solid-State Circuits, vol. 27, no. 3, 281-87 (Mar. 1992)
1021	Narasimha B. Bhat, “Novel Techniques for High Performance Field Programmable Logic Devices,” Technical Report no. UCB/ERL M93/80, Electronic Research Laboratory, University of California, Berkeley (Nov. 1993) (“Bhat”)
1022	Donald W. Cherepacha, Master’s Thesis, <i>A Field-Programmable Gate Array Architecture Optimized for Datapaths</i> , Department of Electrical and Computer Engineering, University of Toronto (1994) (“Cherepacha”)
1023	Paul Chow et al., “The Design of a SRAM-Based Field-Programmable Gate Array—Part II: Circuit Design and layout,” in <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , vol. 7, no. 3, pp. 321-330, Sept. 1999 (“Chow”) (from pages 4-13 of Declaration of Gordon MacPherson at Ex.1024)

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1024	Declaration of Gordon MacPherson regarding Paul Chow et al., “The Design of a SRAM-Based Field-Programmable Gate Array—Part II: Circuit Design and layout,” in <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , vol. 7, no. 3, pp. 321-330, Sept. 1999
1025	U.S. Patent No. 5,905,385 (“Sharpe-Geisler”)
1026	Excerpt of Tom M. Apostol, <i>Calculus, Volume I</i> (Wiley 1967) (“Apostol”)
1027	<i>Principles and Structures of FPGAs</i> (Hideharu Amano, ed., Springer 2018) (“Amano”)
1028	Jason Cong et al., “Technology Mapping For k/m -Macrocell Based FPGAs,” in <i>Proceedings of the 2000 ACM/SIGDA 8th Int’l Symposium on Field Programmable Gate Arrays</i> , 51-59 (Feb. 2000) (“Cong”)
1029	Plaintiff’s Preliminary Infringement Contentions in <i>Iida v. Intel Corp.</i> , No. 6:22-cv-00662-ADA (W.D. Tex.)
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1031	Intel’s Opening Claim Construction Brief in <i>Iida v. Intel Corp.</i> , No. 6:22-cv-00662-ADA (W.D. Tex.)
1032	Iida’s Responsive Claim Construction Brief in <i>Iida v. Intel Corp.</i> , No. 6:22-cv-00662-ADA (W.D. Tex.)
1033	Declaration of Dr. Marwan Hassoun in support of Professor Masahiro Iida’s Responsive Claim Construction Brief in <i>Iida v. Intel Corp.</i> , No. 6:22-cv-00662-ADA (W.D. Tex.)
1034	Intel’s Reply Claim Construction Brief in <i>Iida v. Intel Corp.</i> , No. 6:22-cv-00662-ADA (W.D. Tex.)
1035	Iida’s Sur-Reply Claim Construction Brief in <i>Iida v. Intel Corp.</i> , No. 6:22-cv-00662-ADA (W.D. Tex.)
1036	Joint Claim Construction Statement in <i>Iida v. Intel Corp.</i> , No. 6:22-cv-00662-ADA (W.D. Tex.)
1037	USPTO Memorandum, Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation (June

Exhibit No.	Description
	21, 2022), available at https://www.uspto.gov/sites/default/files/documents/interim_proc_discretionary_denials_aia_parallel_district_court_litigation_memo_20220621_.pdf (“Guidance Memo”)
1038	U.S. District Courts – National Judicial Caseload Profile (Dec. 2022), obtained at https://www.uscourts.gov/statistics-reports/analysis-reports/federal-court-management-statistics , per Guidance Memo at n.4
1039	Scheduling Order dated Oct. 14, 2022, in <i>Iida v. Intel Corp.</i> , No. 6:22-cv-00662-ADA (W.D. Tex.)
1040	Japanese Patent No. 3580785B2, certified translation, and declaration of translator
1041	Iida’s Brief filed March 20, 2023, in <i>Masahiro Iida v. Intel Corporation and Intel K.K.</i> , filed July 4, 2022, in the Department of Intellectual Property Rights, Tokyo District Court, certified translation, and declaration of translator, certified translation, and declaration of translator
1042	Order to Stay Case dated March 14, 2023, in <i>Iida v. Intel Corp.</i> , No. 6:22-cv-00662-ADA (W.D. Tex.)
1043	Andrew S. Tanenbaum, <i>Structured Computer Organization</i> (2d ed. 1984) (“Tanenbaum”)
1044	Neil H.E. Weste & Kamran Eshraghian, <i>Principles of CMOS VLSI Design: A Systems Perspective</i> (1985) (“Weste”)

Petitioner Intel Corporation (“Petitioner”) requests *inter partes* review (“IPR”) of claims 1-16 (“challenged claims”) of U.S. Patent No. 6,812,737 (Ex.1001, “’737-patent”).

I. INTRODUCTION

The ’737 patent relates to “a look up table of M inputs and N outputs, which has a plurality of LUT units” and a circuit for “controlling an internal configuration of the plurality of LUT units.” ’737-patent, Abstract, 2:4-8. This Petition demonstrates that the challenged claims are unpatentable as obvious.

II. MANDATORY NOTICES

A. Real Party-in-Interest

Petitioner is the real party-in-interest.

B. Related Matters

1. U.S. District Court for the Western District of Texas

Patent Owner has asserted the ’737 patent against Petitioner in *Iida v. Intel Corp.*, No. 6:22-cv-00662-ADA (W.D. Tex.) (“District Court Case”), which currently is pending.

2. Tokyo District Court

The ’737 patent claims priority to a Japanese application that issued as Japanese Patent No. 3,580,785 (“JP ’785 patent”). Patent Owner has asserted the JP ’785 patent against Petitioner in the Tokyo District Court, Intellectual Property

Division, in *Iida v. Intel Corp. and Intel K.K.*, Case No. 19129 (Wa) of 2022 (“Japanese Case”). The case is currently pending.

C. Counsel and Service Information - §42.8(b)(3), (4)

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A power of attorney is submitted with the Petition. Counsel for Petitioner consents to service of all documents via electronic mail at the following email address: Intel-Iida-IPR@mto.com.

III. CERTIFICATION OF GROUNDS FOR STANDING

Petitioner certifies that the ’737 patent is available for IPR and that Petitioner is not barred or estopped from requesting IPR of the challenged claims on the grounds identified below. 37 C.F.R. §42.104(a).

IV. OVERVIEW OF CHALLENGE AND RELIEF REQUESTED

A. Prior Art Printed Publications

The '737 patent claims priority to June 29, 2001.¹ Petitioner's challenge is based on the following references:

- **Fujii** - Japanese Unexamined Patent Application Publication No. H09-121153A to Fujii et al. (Ex.1005) was filed on October 25, 1995, and published on May 6, 1997. It is prior art under 35 U.S.C. §102(b).²
- **Betz** - Vaughn Betz et al., *Architecture and CAD for Deep-Submicron FPGAs* (1999 Kluwer Academic Publishers) (Ex.1006), is prior art under §102(b). Betz bears a copyright date of 1999, and its cover material shows it was published by a recognizable and reputable publisher as part of an International Series in Engineering and Computer Science. Ex.1009, ¶¶4-9.
- **Chow** - Paul Chow et al., "The Design of a SRAM-Based Field-Programmable Gate Array—Part II: Circuit Design and layout," in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 7, no. 3, pp. 321-330, Sept. 1999 (Ex.1023) is prior art under §102(b). Chow is an article that was published by

¹ Petitioner reserves the right to challenge the priority date in other proceedings.

² Cites to 35 U.S.C. §§102 and 103 are to the pre-America Invents Act statutes.

IEEE in September 1999 and was publicly available no later than September 30, 1999. Ex.1024, ¶¶6-11.

B. Relief Requested

Petitioner requests cancellation of the challenged claims as unpatentable under 35 U.S.C. §103. The specific grounds of the challenge are set forth below and are supported by the Declaration of Stephen W. Melvin, Ph.D. (Ex.1003) (“Melvin”).

Ground Number and References		Claims
1	Fujii in view of Betz	1-5, 7-11, 13-16
2	Fujii in view of Betz and the general knowledge of a POSA	6, 12
3	Fujii in view of Betz and Chow	1-5, 7-11, 13-16
4	Fujii in view of Betz, the general knowledge of a POSA, and Chow	6, 12

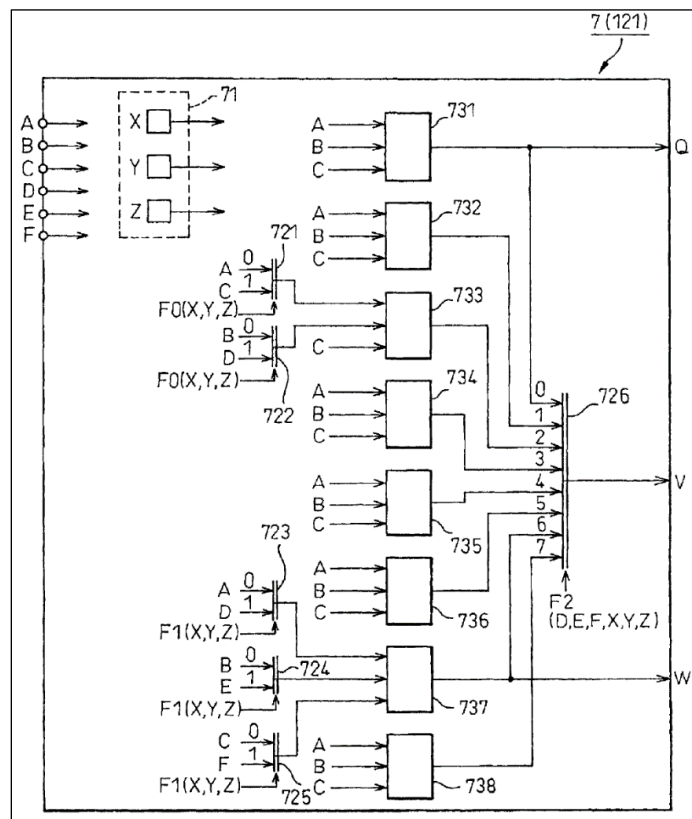
V. THE '737 PATENT

A. Preferred Embodiments

The '737 patent relates to look-up tables (“LUTs”) used to implement logic circuits in programmable logic circuit devices, also known as programmable logic devices (“PLDs”), including Field Programmable Gate Arrays (“FPGAs”). '737-patent, Abstract, 1:13-28. The '737 patent acknowledges that the “[b]asic architecture of such a[n] FPGA has been previously disclosed” ('737-patent, 1:28-30), so it omits FPGA architecture details, e.g., details about routing wires, switch

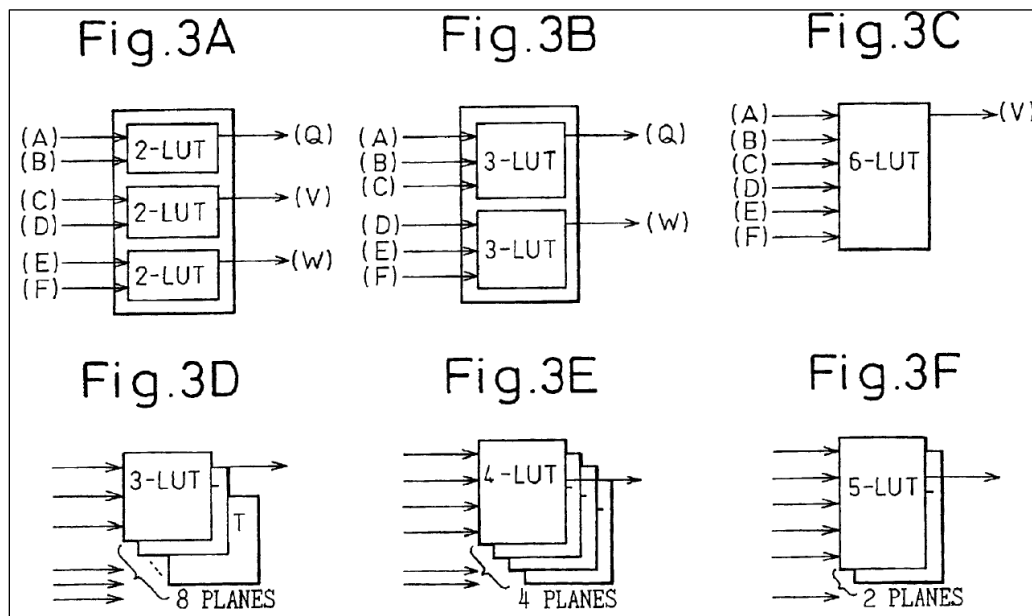
circuits, connection blocks, and input/output (“I/O”) blocks. ’737-patent, 3:54-4:3 (“The present invention relates mainly to the configuration of LUT **121**” in FIG.1, rather than to FPGA **100**); Melvin, ¶57. The patent also admits that a “[m]ulti-context and cluster architecture of plural LUTs in FPGA” was previously disclosed. ’737-patent, 1:30-32.

The ’737 patent purports to address the problem of how, “in a circuit having input bit number less than M, one LUT needs to be assigned to this circuit, leading to [an] unnecessary increase of implementation area (logic and routing circuitry area; circuit area).” ’737-patent, 1:59-63; Melvin, ¶58. FIG.6 depicts a preferred embodiment of the ’737 patent’s alleged invention:



'737-patent, FIG.6, 2:64-67, 3:11-16, 3:46-48, 5:24-61, 6:15-7:21. FIG.6 shows a “6-input 3-output LUT 7 (121)” that contains “a mode changing memory 71, selectors 721~726, and 3-input 1-output LUT units (memory array) 731~738.”

'737-patent, 5:24-29. Selectors 721-725 are “for selecting input signal[s]” to the “LUT units.” '737-patent, 5:26-61, 6:15-7:21, FIG.6. Selector 726 is “for selecting output signal[s]” from the “LUT units.” '737-patent, 5:55-60. “[B]y varying the values (X, Y, Z) of mode changing memory (71),” which control selectors 721-726, “the 6-input 3-output LUT can be set to different internal configurations as shown in FIGS. 3A to 3F,” reproduced below. '737-patent, 4:15-17, 4:18-47, 6:15-7:21.



Such techniques were not new. For example, Sharpe-Geisler (cited at '737-patent, 1:30-32), had explained that it was known that (1) a look-up table with M

inputs may be composed of two smaller look-up tables of $M-1$ inputs each and (2) two look-up tables of M inputs each may be combined to form a look-up table of $M+1$ inputs. Sharpe-Geisler, 1:65-2:16; *see* Rose, 1021. Fujii, discussed below, had disclosed a K -input programmable logic element PL1 that was divided into “plural memory circuit groups,” each of which implemented a logic circuit of fewer than K inputs, allowing PL1 to implement multiple functions and leave less memory unused. Fujii, ¶¶6, 9-10, 12, 14, 50, 78, 99, 102. PL1 therefore is “capable of efficiently realizing a desired logic function by using fewer logic elements and less memory.” Fujii, ¶¶9, 102. Unlike the ’737 patent, the prior art details *how* look-up tables were partitioned into smaller look-up tables, thereby increasing their flexibility and efficiency. Melvin, ¶¶59-62.

B. Prosecution History

The application that issued as the ’737 patent was filed on June 28, 2002. ’737-patent, 1. It claimed priority to Japanese Patent Application No. 2001-199644, which was filed on June 29, 2001, and which issued as the JP ’785 patent. ’737-patent, 1; Ex.1040, 1.

The Reasons for Allowance stated that, “although the prior art of record discloses [a] control circuit having a memory for controlling a plurality of selectors for selecting LUTs’ input signals,” that art failed to teach an “internal

configuration control circuit controlling and defining an internal configuration of the plurality of LUT units.” Ex.1002, 196.

No reference relied upon as invalidating grounds here was before the Examiner during prosecution, nor were similar disclosures discussed. ’737-patent, cover at (56); Ex.1002.

VI. PERSON OF ORDINARY SKILL IN THE ART (“POSA”)

A POSA would have had a bachelor’s degree in electrical engineering, computer engineering, or an equivalent degree, and one year of professional experience relating to PLDs or FPGAs. More education could substitute for experience, and vice versa. This person would have been capable of understanding and applying the ’737 patent’s teachings and would have had a working knowledge of PLDs, including prior art describing look-up table designs. Melvin, ¶¶29-34; Ex.1033, ¶32.

VII. CLAIM INTERPRETATION

In an IPR, claims are construed under *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (*en banc*). See 37 C.F.R. §42.100(b). No term needs to be construed to resolve this Petition; the challenged claims are unpatentable under either party’s proposed constructions. Melvin, ¶¶68-74.

In the District Court Case, Patent Owner and Petitioner have briefed two claim-construction issues. The parties’ positions are below. See Exs.1031-1036.

Claim Term	Patent Owner's Proposal	Petitioner's Proposal
“look up table of M inputs and N outputs” (claims 1, 7, 13, and claims that depend therefrom)	Plain-and-ordinary meaning	“component that is composed of memories and is capable of implementing an arbitrary logic circuit of M inputs on at least one of N outputs” ³
“LUT units” (all claims)	Plain-and-ordinary meaning	Indefinite Otherwise, if not indefinite, each “LUT unit” is a “component that is composed of memories and is capable of implementing an arbitrary logic circuit of its inputs with at least one output” ⁴

A. “look up table of M inputs and N outputs”

The '737 patent defines “*look up table of M inputs and N outputs*” in two parts. First, it defines a “*look up table*” as “a major component of a programmable logic circuit device (PLD or FPGA)” that “*is composed of memories, and is*

³ In district court, Petitioner dropped language from its proposal that would have required the “*look up table of M inputs and N outputs*” to be part of a PLD.

Ex.1034, 2 n.1.

⁴ See *supra* note 3.

capable of implementing an arbitrary logic circuit.” ’737-patent, 1:25-28.⁵

Second, the patent defines “*M inputs and N outputs*,” stating:

[T]he number of bits *M* of input signal for the logic circuit that can be implemented corresponds to the number of bits of the address of memory composing the LUT, and the number of bits *N* of output signal corresponds to the number of output bits of the memory. Thus, a logic circuit that can be implemented in one LUT ***is an arbitrary logic circuit of M inputs and N outputs***. Such a LUT ***is*** denoted in the present specification as *M-input N-output LUT*.

’737-patent, 1:46-54.

Although Patent Owner contends that this term does not require construction, the parties agree that the plain meaning of “*look up table of M inputs and N outputs*” is a component that is composed of memories and is capable of implementing an arbitrary logic circuit of *M* inputs on at least one of *N* outputs. See Ex.1032, 3-4, 7-11; Ex.1035, 1-2; Ex.1033, ¶¶21, 23. This is consistent with the ’737 patent’s preferred embodiments, which are “6-input 3-output” look-up tables with 64 memory bits (i.e., each of the eight “LUT units” 731-738 in FIG.6 has 8 memory bits, and each of the four “LUT units” 831-834 in FIG.9 has 16 memory bits). ’737-patent, 3:46-53, 5:24-32, 5:62-6:14, 7:21-31, 7:45-8:21, FIGS.6-12. These memory bits are sufficient to implement any function of 6 inputs

⁵ Emphasis added unless otherwise noted.

on one output ($2^6 \times 1 = 64$ bits required), but they cannot implement any function of 6 inputs on three outputs ($2^6 \times 3 = 192$ bits required). Melvin, ¶72.

In sum, a “*look up table of M inputs and N outputs*” is a “component that is composed of memories and is capable of implementing an arbitrary logic circuit of M inputs on at least one of N outputs.” Melvin, ¶¶71-73.

B. “LUT units”

In the District Court Case, Petitioner argues that “*LUT units*” are smaller look-up tables into which a larger “*look up table*” may be divided.⁶ See Ex.1031, 13-15. Patent Owner contends the plain-and-ordinary meaning of “LUT unit” is “an individual LUT that cannot be fractured or divided *into smaller LUT units*.” Ex.1035, 3 (emphasis in original). As discussed more fully below, *see infra* [1A], the Board need not resolve this dispute because the challenged claims are unpatentable under either construction. Melvin, ¶74. Petitioner reserves the right to respond to any claim construction argument Patent Owner makes.

⁶ Petitioner further argued that, under the plain meaning of “LUT units,” the claims are indefinite because a single implementation can infringe and not infringe the claims simultaneously. Ex.1031, 13-19; Ex.1034, 4-10.

VIII. GROUND 1

Fujii in combination with Betz renders obvious claims 1-5, 7-11, and 13-16. Melvin, ¶75.

A. Overview of Fujii and Betz

1. Fujii (Ex.1005)⁷

Fujii and the '737 patent relate to the same problem: implementing a small function in a larger LUT means that some memory circuits go unused. Fujii, ¶¶5-6; '737-patent, 1:59-63, 4:18-25. Fujii addresses this problem by providing a K-input programmable logic element divided into “plural memory circuit groups.” Fujii, claim 1, ¶¶12, 14, 54, 80. Each memory circuit group implements an arbitrary logic circuit of less than K inputs, allowing the programmable logic element to implement a plurality of logic circuits. *See* Fujii, ¶¶12, 14, 54, 80. Thus, that element realizes a “desired logic function” using “fewer logic elements and less memory,” Fujii, Abstract, ¶¶9, 102, increasing utilization and reducing power consumption, Melvin, ¶¶77-79.

⁷ Exhibit 1005 contains the English-language translation of Fujii that is relied upon here; an affidavit (i.e., declaration) under 37 C.F.R. §§42.63(b), 42.2; and a copy of the original publication in Japanese.

Fujii switches between operations (i.e., use modes that can implement certain-sized functions using the plural memory circuit groups, *see infra* [1B]) of programmable logic element PL1 using “control signals” A and B. *See, e.g.*, Fujii, ¶¶11-12, 36-39, 42, 45, 51; FIGS.1, 6; Melvin, ¶80.

2. Betz (Ex.1006)

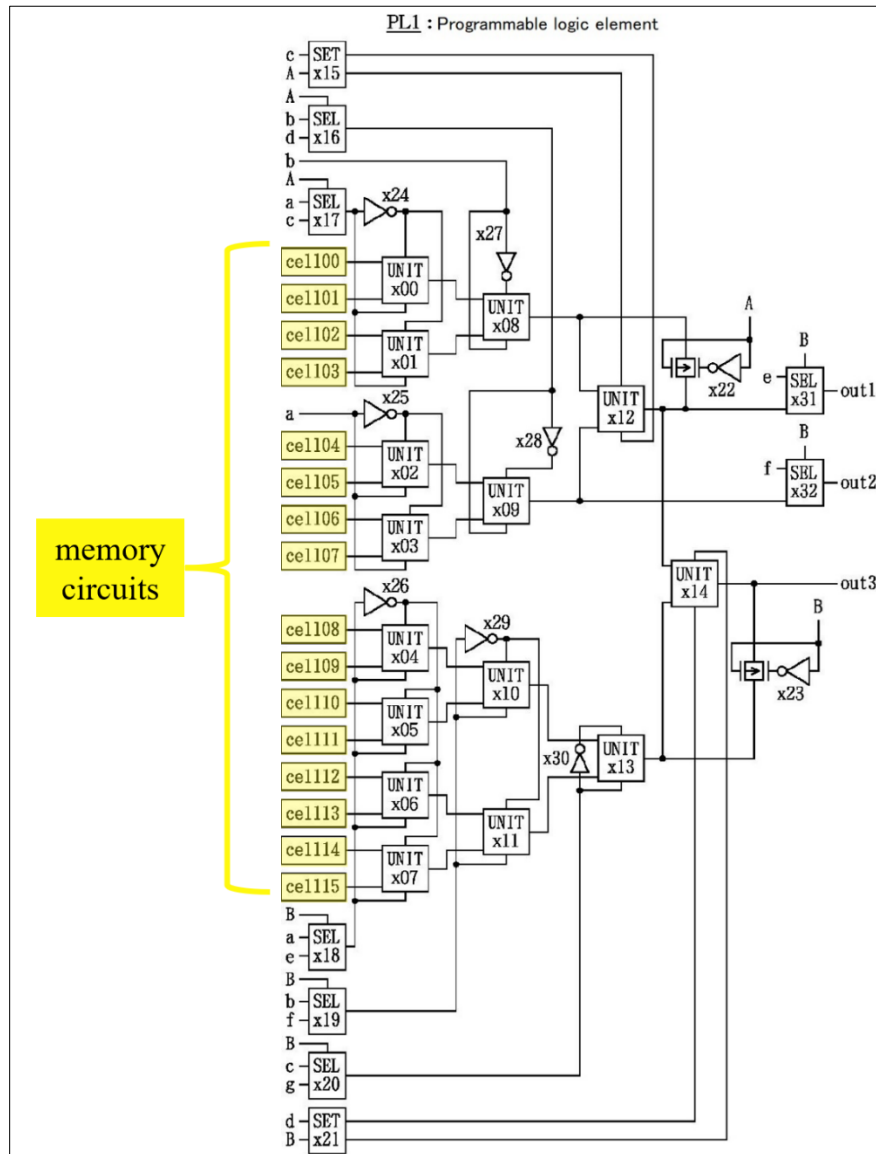
Betz is a book on FPGA architectures and CAD tools. One author of Betz, Jonathan Rose, was a well-known researcher in the programmable-hardware field. Betz provides an overview of FPGAs, including logic block and routing architecture. Betz, 2-7, 11-18, 105-149, 207-17; Melvin, ¶¶81-82.

B. Independent Claim 1

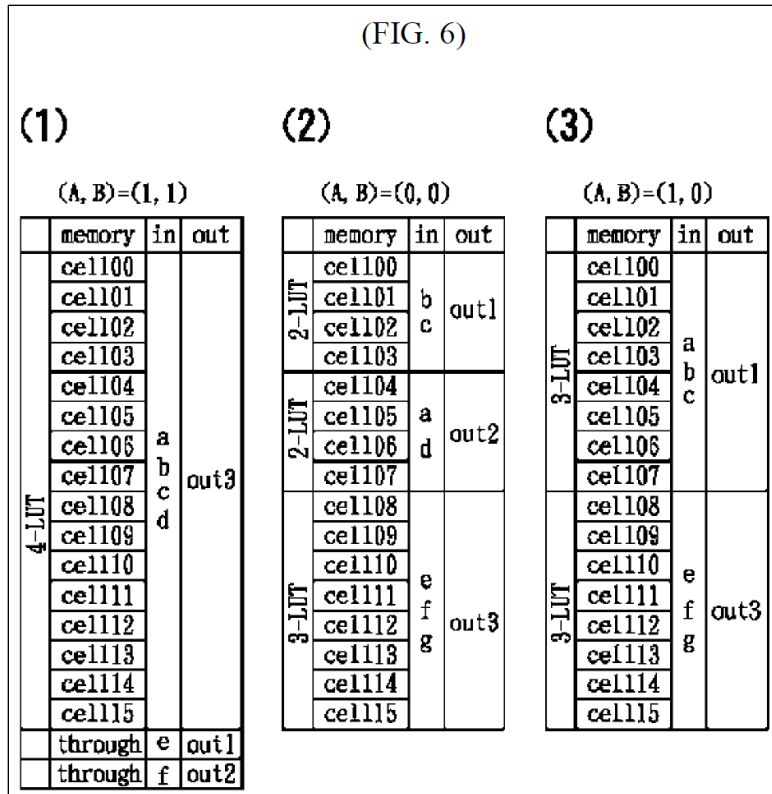
1. [1PRE] “A look up table of M inputs and N outputs, comprising”

Fujii discloses “[a] look up table of M inputs and N outputs” under the parties’ agreed-upon interpretation of that phrase: a “component that is composed of memories and is capable of implementing an arbitrary logic circuit of M inputs on at least one of N outputs.” Melvin, ¶¶83-89; *see supra* §VII.A. In particular, Fujii discloses PL1. Fujii, FIG.1 (depicting PL1); *see also* Fujii, FIGS.8 (depicting PL2, which is substantially similar in structure and function); 15 (depicting PL3, which is substantially similar in structure and function).

PL1 is a “component that is composed of memories” because it has “16 memory circuits.” Fujii ¶¶12, 14. Fujii’s FIG.1 (below) depicts PL1 and illustrates its memory circuits (yellow):



See Fujii ¶¶11, 31-33. Fujii’s FIG.6 (below) also lists these memory circuits as part of PL1:



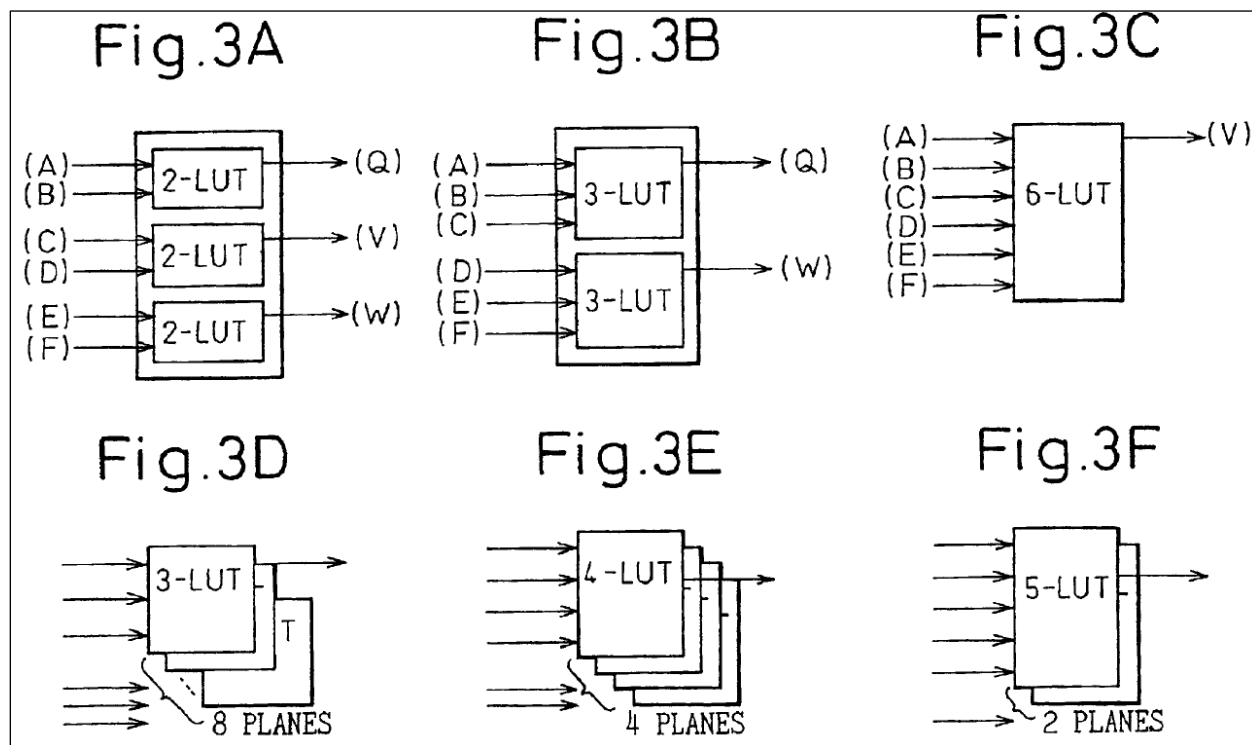
Fujii, ¶¶36-38 (“In FIG. 6...cell00 to cell15 indicate memory circuits to be used.”);
 Melvin, ¶¶83-84.

PL1 is “capable of implementing an arbitrary logic circuit of M inputs on at least one of N outputs,” as required by the parties’ interpretation. PL1 has “16 [i.e., 2⁴] memory circuits,” Fujii, ¶¶12, 14, allowing it to be “capable of implementing an arbitrary logic function of” up to and no more than 4 “inputs” (i.e., the use mode shown in FIG.6(1) implements an arbitrary logic function of a, b, c, and d). Fujii, ¶¶5-6, 14, 38, FIG.6(1). Thus, PL1 is a look-up table of 4 inputs. Notably, neither the claim language nor the parties’ agreed-upon interpretation precludes the “*look up table*” from having more inputs than the M inputs required to implement an

arbitrary logic circuit. So the fact that PL1 has additional inputs (e, f, g) that go unused in use mode 6(1) is irrelevant under either the parties' agreed-upon interpretation or the claim language, as Patent Owner has recognized. *See* Ex.1041 (“[T]hroughout the entire claims, there is no language stipulating that ‘input ...signals of said plurality of LUT units’ must match the ‘M inputs’ inputted into the ‘lookup table’ as a whole....[I]t is fine if all M inputs are the ‘input...signals of said plurality of LUT units’ of the ‘input and output signals of said plurality of LUT units’, and it is also fine if they are not.”); Melvin, ¶86.

PL1 also has three “*outputs*”, out1, out2, and out3, that output the values of selected memory bits according to the use modes shown in FIG.6. Fujii, ¶¶34-35, 37-38, 40-44, 47-48, FIGS.1, 6; *see also* ’737-patent, 1:55-58, 6:54-60, 7:17-20. Neither the claim language nor the parties’ agreed-upon interpretation precludes the “*look up table*” from having more outputs than required to implement an arbitrary logic circuit of M inputs on one output. The fact that PL1 cannot implement an arbitrary logic circuit of four inputs on each of its outputs (it performs such a function only on out3, *see* FIG.6(1)) is consistent with the ’737 patent’s preferred embodiments (FIGS.6, 9), which each have 3 outputs (Q, V, W) but are capable of implementing an arbitrary logic circuit of 6 inputs on only a single output. *Compare* ’737-patent, 3:46-53, 5:24-32, 5:62-6:14, 6:24-50, 7:21-31, 7:45-8:21, FIGS.6-12 *with* Fujii, ¶5; *see also supra* §VII.A. As shown in FIG.3

(below), the preferred embodiments can only perform an arbitrary function of 6 inputs on a single output (FIG.3C):



See '737-patent, 4:39-40, 6:54-60. Thus, Fujii's PL1 is "capable of implementing an arbitrary logic circuit of M inputs [4 inputs] on at least one of its N outputs [3 outputs]." Melvin, ¶87.

In sum, Fujii discloses a component ["PL1"] that is composed of memories ["16 memory circuits"] and is capable of implementing an arbitrary logic circuit of M inputs ["out3 corresponds to the output terminal of a four-input programmable logic element"] on at least one of N outputs ["PL1 has...up to three output terminals"]. Fujii, ¶¶5, 12-14, 40. Thus, Fujii's PL1 is "[a] look up table of M

inputs and N outputs” under the parties’ agreed-upon interpretation of that phrase. Melvin, ¶88.

Alternatively, if the claim is interpreted such that the “*look up table of M inputs and N outputs*” need not be capable of implementing an arbitrary logic circuit of M inputs, PL1 also could be considered a look-up table of up to 7 inputs (a, b, c, d, e, f, g) and three outputs (out1, out2, out3). Fujii, ¶38, FIGS.1, 6. Even under this interpretation, PL1 remains “[a] *look up table of M inputs and N outputs*[.]” Melvin, ¶89.

2. [1A] “a plurality of LUT units; and”

Fujii discloses this limitation by teaching that PL1 has “plural memory circuit groups.” *E.g.*, Fujii, claim 1, ¶¶12, 14. For example, PL1 has “three memory circuit groups each composed of 8, 4, and 4 memory circuits.” Fujii, ¶12. Under either party’s construction, these memory circuit groups are a “plurality of LUT units.” Melvin, ¶¶90-99; *see also* Fujii, ¶54, FIG.8 (substantially similar “memory circuit groups” in PL2); Fujii, ¶80, FIG.15 (substantially similar “memory circuit groups” in PL3).

Fujii discloses “plural memory circuit groups” within PL1’s 2^K memory circuits:

[A] second operation of selecting one output signal from the output signals of the 2^{X_i} memory circuits and outputting the selected output signal as an output signal of the programmable logic element, *by*

dividing the 2^K memory circuits into plural memory circuit groups, where the sequence from $i=1$ to $i=n$ of the sequence $\{2^{X_i}\}$ ($2^{X_i} \leq 2^{X_{i+1}}$) is equal to $2^{[K]}$,⁸ the memory circuit group is composed of 2^{X_i} ($i=1, 2, \dots, n$) memory circuits, and X_i ⁹ input signals that do not overlap each other among the input signals are used as selection signals.

Fujii, ¶14, ¶¶12-13. Each memory circuit group has X_i input signals and 2^{X_i} memory circuits and, therefore, has sufficient memory to implement an arbitrary logic circuit of X_i inputs on at least one output. Fujii, ¶5; Melvin ¶91. Moreover, Fujii describes that the X_i input signals are “appl[ied]” to their memory group. Fujii, ¶¶12, 54, 80.

Thus, Fujii discloses “a plurality of LUT units” under Petitioner’s construction of “LUT units”: it discloses components [“plural memory circuit groups”] that are each composed of memories [2^{X_i} ($i=1, 2, \dots, n$) memory circuits”] and are capable of implementing an arbitrary logic circuit of their inputs

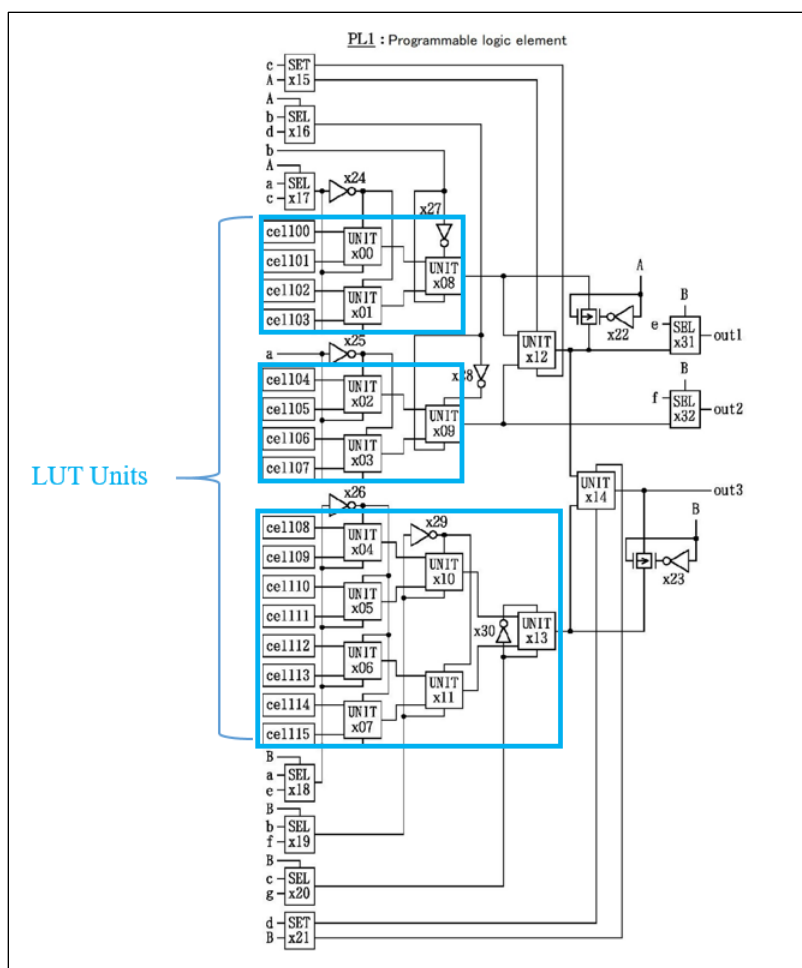
⁸ The text “equal to $2K$ ” is a typographical error that should read “equal to 2^K ”. Melvin, ¶91 n.7.

⁹ The text “ X_i ” in this quote and elsewhere in Fujii indicates that “ X ” is a variable indicating the number of input signals applied to each memory circuit group, and the letter “ i ” is an index (which can also be written as a subscript) used to distinguish the plurality of memory circuit groups. Melvin, ¶91 n.8.

[“ X_i input signals” for “selecting one output signal from the output signals of the 2^{X_i} memory circuits”] with at least one output [“outputting the selected output signal as an output signal of the programmable logic element”]. Melvin, ¶92.

For PL1, “the 16 storage elements are divided into 4+4+8 (divided into $2^2+2^2+2^3$), and the sequence $\{2^{[X]_i}\}^{10}$ in this case is $\{2^2, 2^2, 2^3\}$.” Fujii, ¶¶45, 51. PL1 therefore has three memory circuit groups, namely a top “2-LUT” with four memory circuits, a middle “2-LUT” with four memory circuits, and a bottom “3-LUT” with eight memory circuits. *See* Fujii, FIG.6(2). These three “*LUT units*” are shown in annotated FIG.1 below:

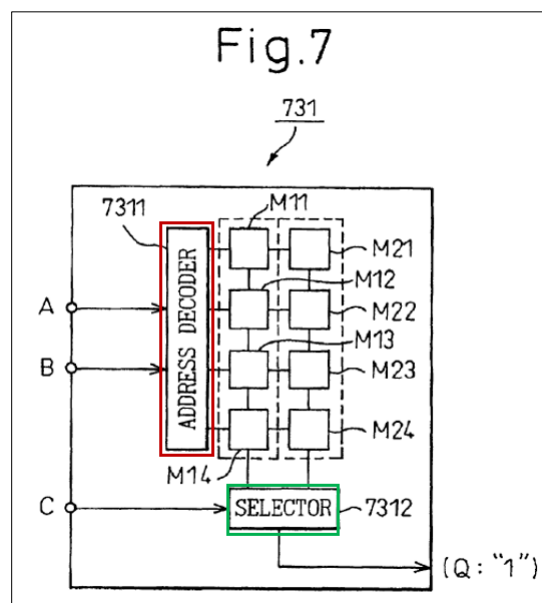
¹⁰ The lowercase “x” is a typographical error that should be a capital “X”. Melvin, ¶93, n.9.



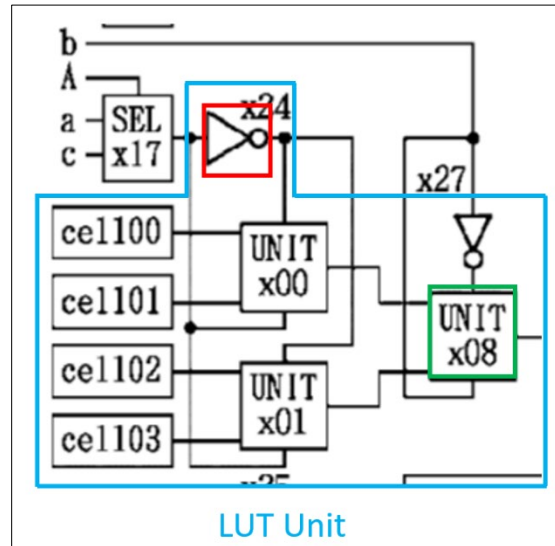
Fujii, FIG.1 (annotated); FIG.6(2). Although not entirely within the blue boxes (drawn as rectangles in full FIG.1 for convenience), the “*LUT units*” include inverters x24-30. These “*LUT units*” constitute a “*plurality of LUT units*” under Petitioner’s proposed construction. Melvin, ¶93.

Fujii’s “three memory circuit groups” (Fujii, ¶12) also constitute “*a plurality of LUT units*” under Patent Owner’s proposed construction. Melvin, ¶¶94-99. As discussed above (§VII.B), Patent Owner interprets “*LUT unit*” to mean “an individual LUT that cannot be fractured or divided into smaller units.” Ex.1032,

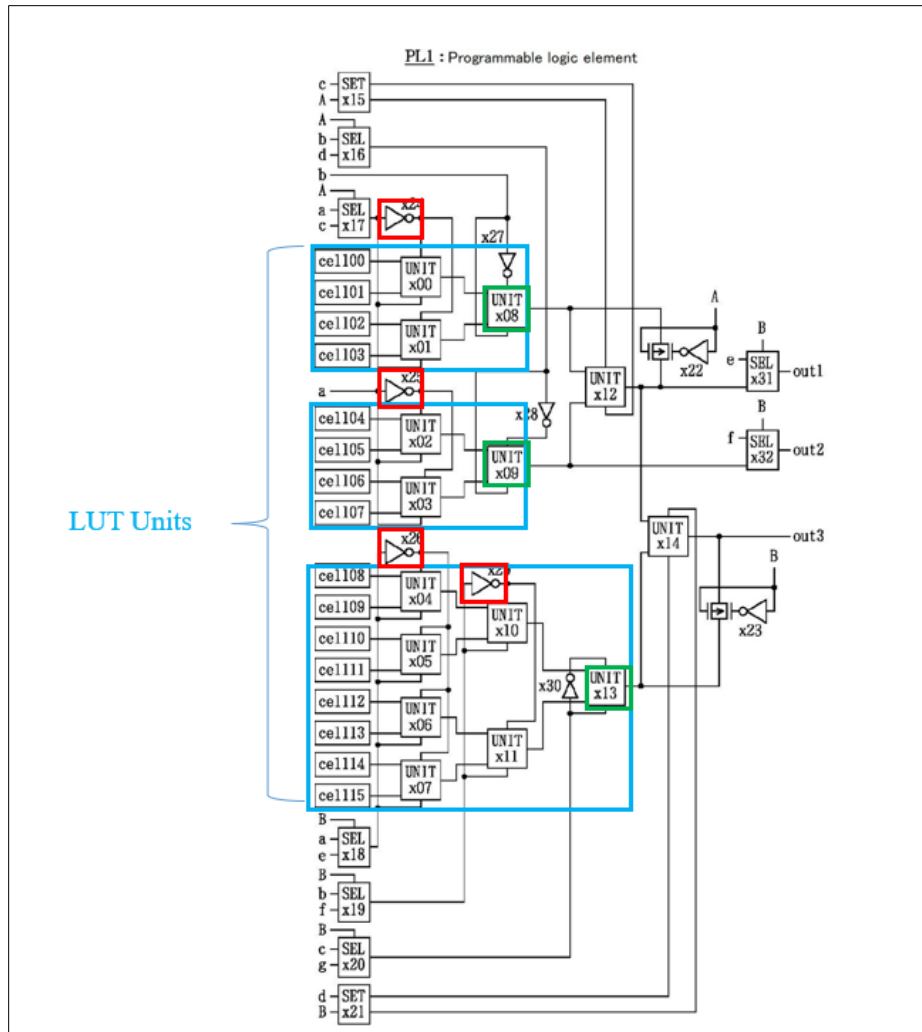
14. Patent Owner also has argued that “whether a given look up table of M inputs and N outputs comprises a plurality of LUT units is not a matter of how simplified block diagrams of look up tables are *viewed*, but rather how look up tables are actually *implemented*.” Ex.1032, 14 (emphasis in original). Patent Owner contends that FIGS.6-11 of the ’737 patent show “exemplary” “*LUT units*[.]” See Ex.1032, 13-14, 17. It follows that Patent Owner believes the “*LUT units*” in FIGS.6-11 “cannot be fractured or divided into smaller units,” Ex.1032, 14, apparently because those figures show shared hardware (an address decoder) that is used to designate memory units. Melvin, ¶96. For example, the LUT unit in FIG.7 uses one address decoder (7311, red) to “decode[] 2 bit input signal A, B” and “designate” two memory units, one from M11-14 and one from M21-24. ’737-patent, 6:1-4. Then, a selector (7312, green) “selects one” of those two units “to output” data (’737-patent, 6:4-6):



PL1's plural memory circuit groups likewise use shared hardware. Similarly, the top 2-LUT “*LUT unit*” in Fujii uses a single inverter x24 (red), shared between selectors x00 and x01, in selecting two memory circuits. Fujii, ¶¶25, 60. Then, a selector x08 (green) selects between those two memory circuits to output data:



Fujii, FIG.1 (annotated and excerpted), ¶31. The middle 2-LUT “*LUT unit*” and bottom 3-LUT “*LUT unit*” also use shared inverters (red) in selecting two memory circuits, which are then selected by a selector (green):



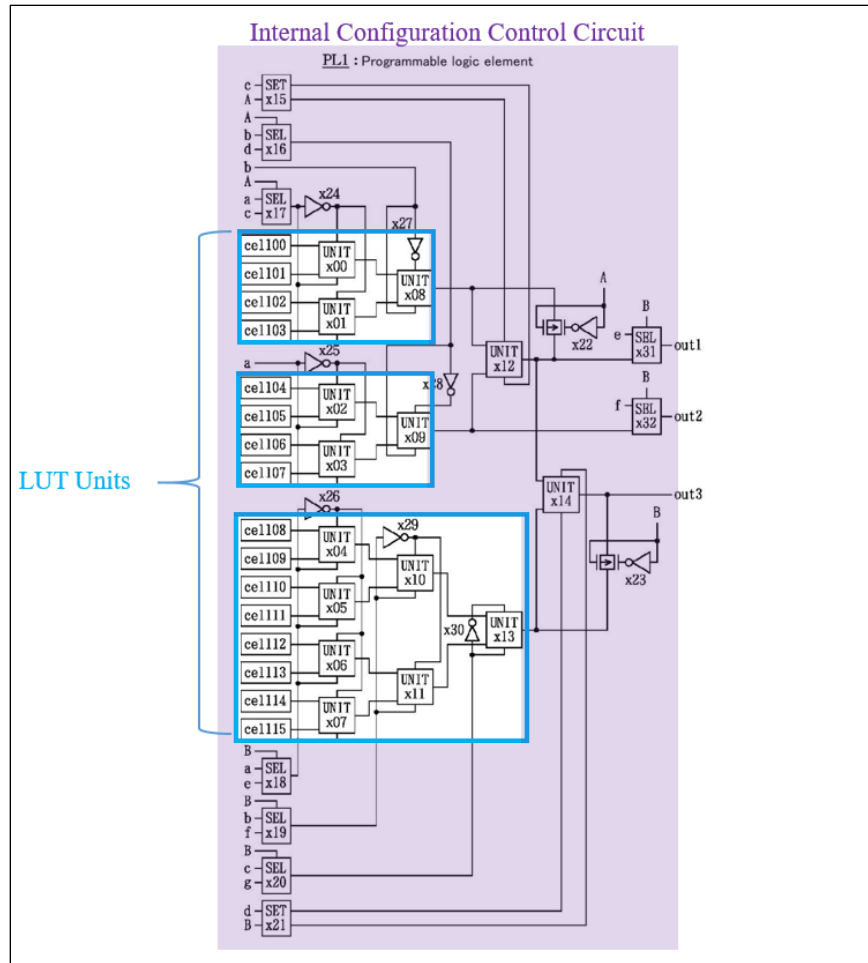
Fujii, FIG.1 (annotated), ¶¶24-27, 30-32, 34. Accordingly, if the '737 patent's preferred embodiments of "*LUT units*" "cannot be fractured or divided into smaller units," the same is true of Fujii's three memory circuit groups.

PL1 therefore comprises "three memory circuit groups each composed of 8, 4, and 4 memory circuits, selecting 3 input signals, 2 input signals, and 2 input signals" (Fujii, ¶12), which are "*a plurality of LUT units*" under either party's proposed construction of "*LUT units*["."

3. [1B] “an internal configuration control circuit controlling an internal configuration of said plurality of LUT units,”

Fujii discloses “*an internal configuration control circuit controlling an internal configuration of said plurality of LUT units*” because it discloses a circuit that allows PL1 to “switch[] between three operations” or “use mode[s].” See Fujii, ¶¶12, 14, 38, 51; see also Fujii, ¶¶54-55, 71-79, FIG.8 (substantially similar circuits and “operations” in PL2); Fujii, ¶¶80, 94-97, FIG.15 (substantially similar circuits and “operations” in PL3); Melvin, ¶¶100-107. This mode switching constitutes “*controlling an internal configuration of said plurality of LUT units*,” making the circuit “*an internal configuration control circuit[.]*”

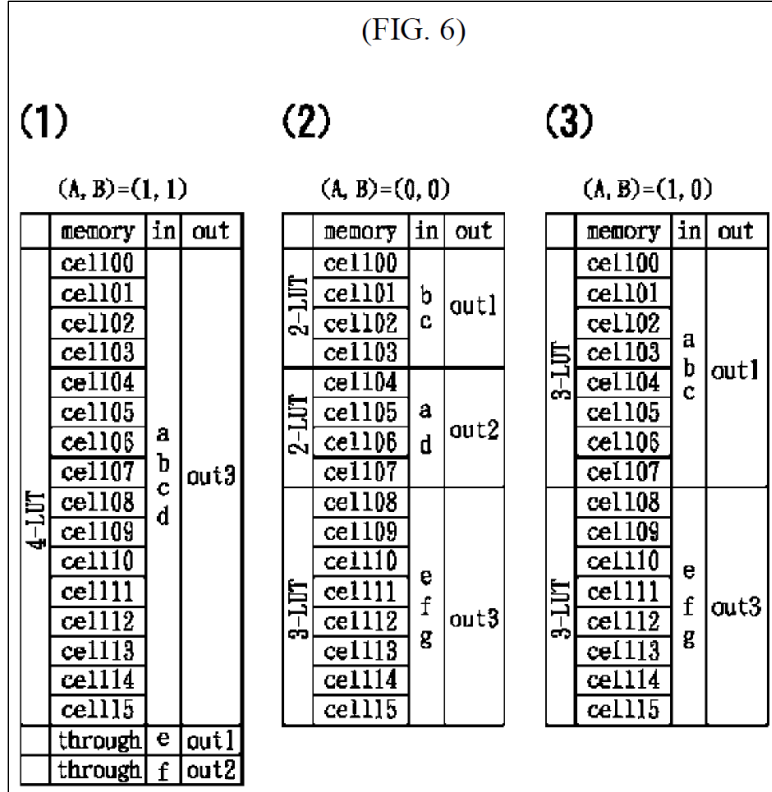
First, Fujii discloses control signals, selectors, control circuits, CMOS transfer gates, and the wires connecting those components to each other and/or other components within PL1. Fujii, ¶12 (“PL1 switches between the following operations by two control signals[.]”), Fujii, ¶15 (noting PL1 includes selectors x12, x14, “selectors x16 to x20, x31, x32, CMOS transfer gates x22, x23, [and] control circuits x15, x21”). A POSA would have understood these components to constitute a circuit (in purple below):



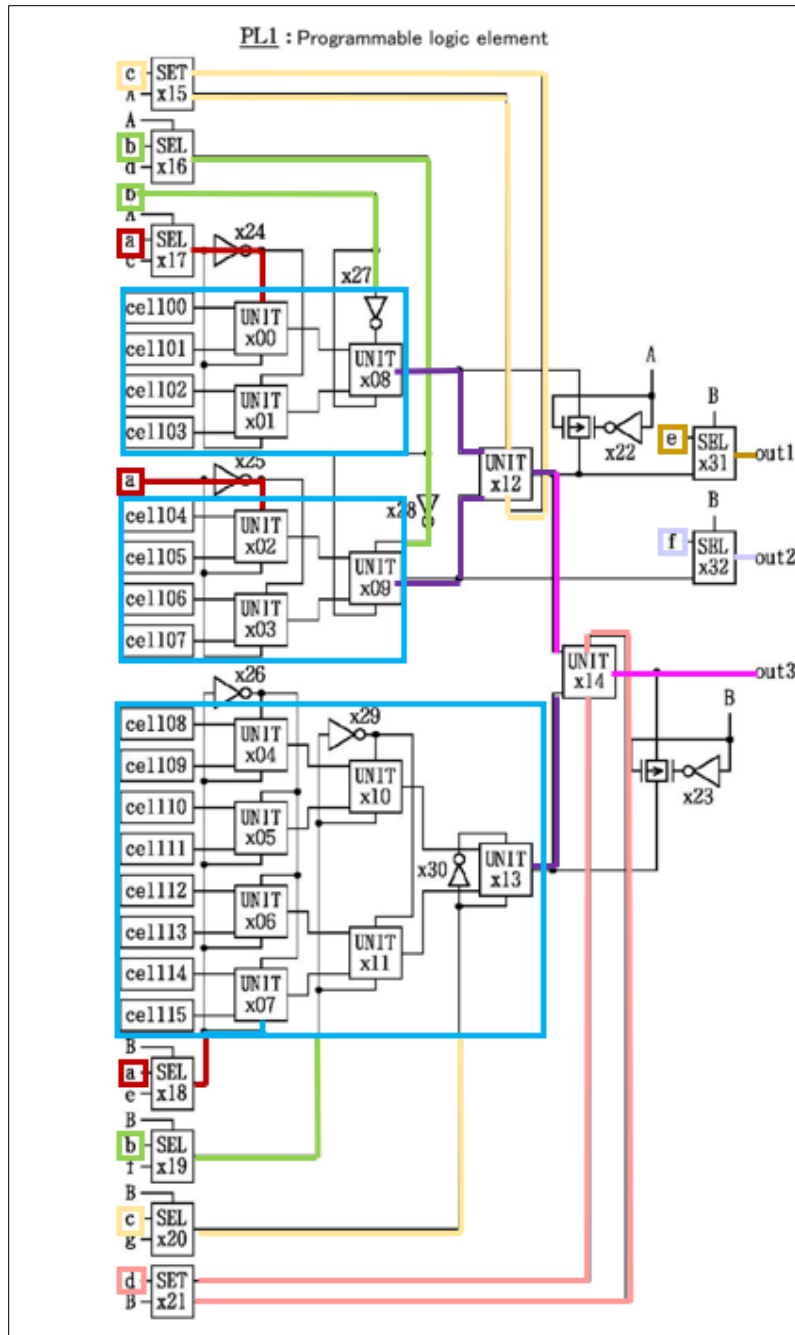
Fujii, FIG.1 (annotated).¹¹

Second, this circuit represents “an internal configuration control” circuit for “controlling an internal configuration of said plurality of LUT units.” The circuit shaded in purple above allows PL1 to “switch[] between three operations” or “use mode[s],” as shown in FIG.6 below. *Fujii*, ¶¶12, 14, 38, 51.

¹¹ Inverters x24-x30 are part of the “LUT units[.]” See *supra* [1A].



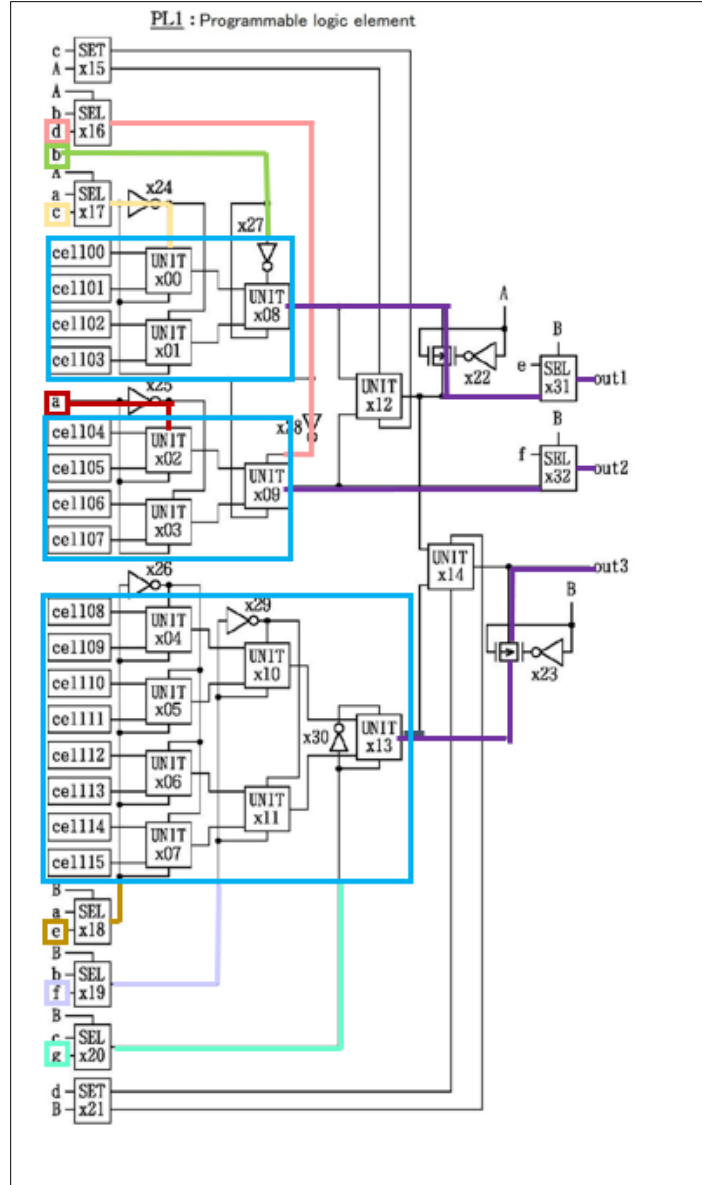
In a **first use mode** (see FIG.6(1)), control signals A and B are both 1, thereby setting PL1 to use mode 6(1). Based on the operation of selectors, CMOS transfer gates, and other components, PL1 operates as a 4-input look-up table. Fujii ¶40, ¶¶37-41, FIGS.1, 6(1). To do so, the three memory circuit groups (“*LUT units*”) collectively implement a single 4-input, 1-output look-up table on out3:



Fujii, FIG.1 (annotated). Selectors x16-x20, controlled by control signal A or B, ensure that the same input signals (a and b) are “appl[ied]” to “each memory circuit group.” See Fujii, ¶¶12, 24-28, 39, FIG.1 (annotated), see FIG.6(1). Then, in accordance with control signals A and B and input signals c and d, selectors x12

and x14 select the outputs of the “*LUT units*” (purple lines) such that “out3 corresponds to the output terminal of a four-input programmable logic element having the signals a, b, c, and d as input signals.” Fujii, ¶¶40, 12, 37-39, FIG.1 (annotated), see FIG.6(1). “[T]he input terminals e and f are connected to the output terminals out1 and out2 by the selectors x31 and x32.” Fujii, ¶41; Melvin, ¶103.

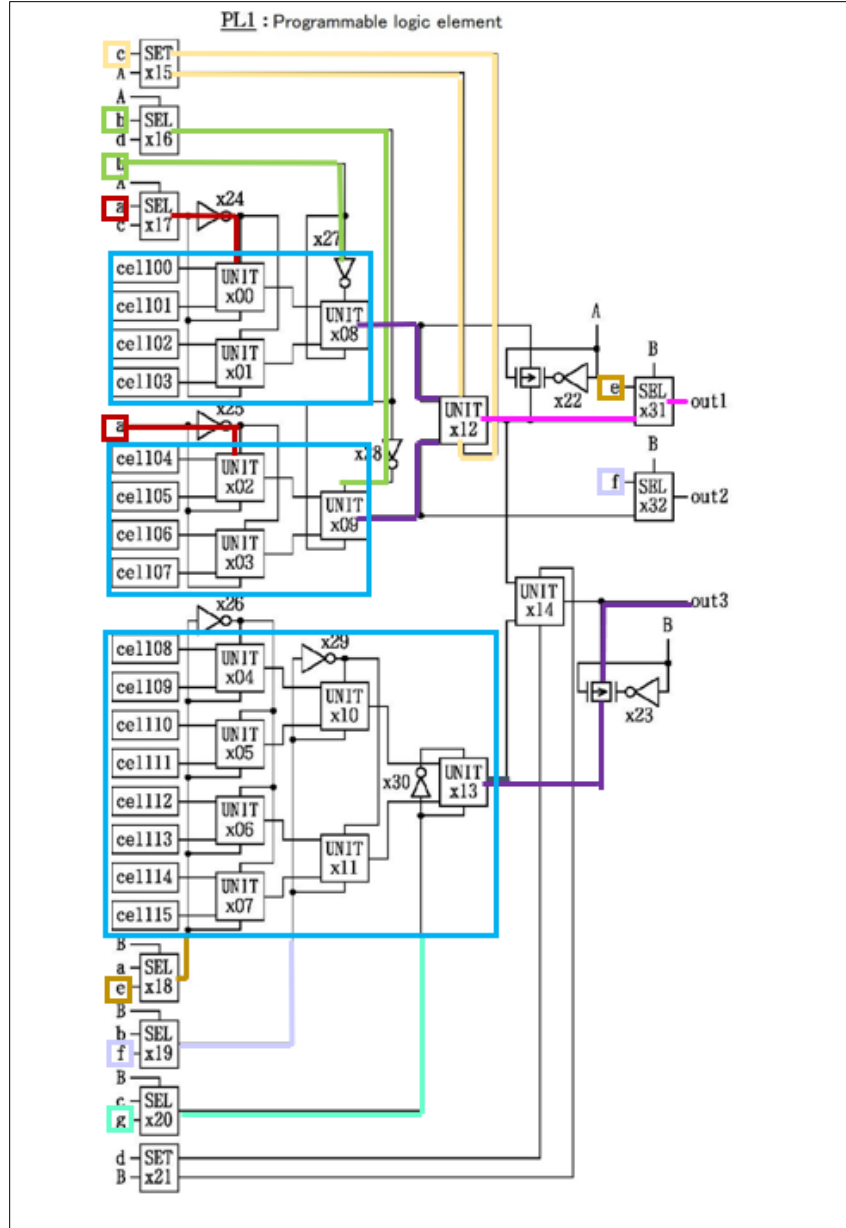
In a **second use mode** (see FIG.6(2)), control signals A and B are both 0, thereby setting PL1 to use mode 6(2). Based on the operation of selectors, CMOS transfer gates, and other components, PL1 operates as two 2-input look-up tables and one 3-input look-up table. Fujii, ¶¶36-37, 45-48, FIGS.1, 6(2). To do so, the three memory circuit groups (“*LUT units*”) are used separately:



Fujii, FIG.1 (annotated). Selectors x16-x20, controlled by control signal A or B, ensure that different input signals (a-g) are “appl[ied]” to “each memory circuit group.” See Fujii, ¶¶12, 24-28, 45-46, FIG.1 (annotated), see FIG.6(2). Then, in accordance with control signals A and B, selectors x31 and x32 select the outputs of the top and middle 2-LUTs, and the output of the bottom 3-LUT is passed through CMOS transfer gate x23 (purple lines). As a result, “the output terminal

out1 corresponds to the output of a two-input programmable logic element...; the output terminal out2 corresponds to the output terminal of a two-input programmable logic element...; and the output terminal out3 corresponds to the output of a three-input programmable logic element[.]” Fujii, ¶¶48, 12, 47, FIG.1 (annotated), FIG.6(2); Melvin, ¶104.

In a **third use mode** (see FIG.6(3)), control signal A is 1 and control signal B is 0, thereby setting PL1 to use mode 6(3). Based on the operation of selectors, CMOS transfer gates, and other components, PL1 operates as two 3-input look-up tables. Fujii, ¶¶36-37, 42-44, FIGS.1, 6(3). That is, the top and middle 2-LUT memory circuit groups (“*LUT units*”) are used to implement a single 3-LUT:

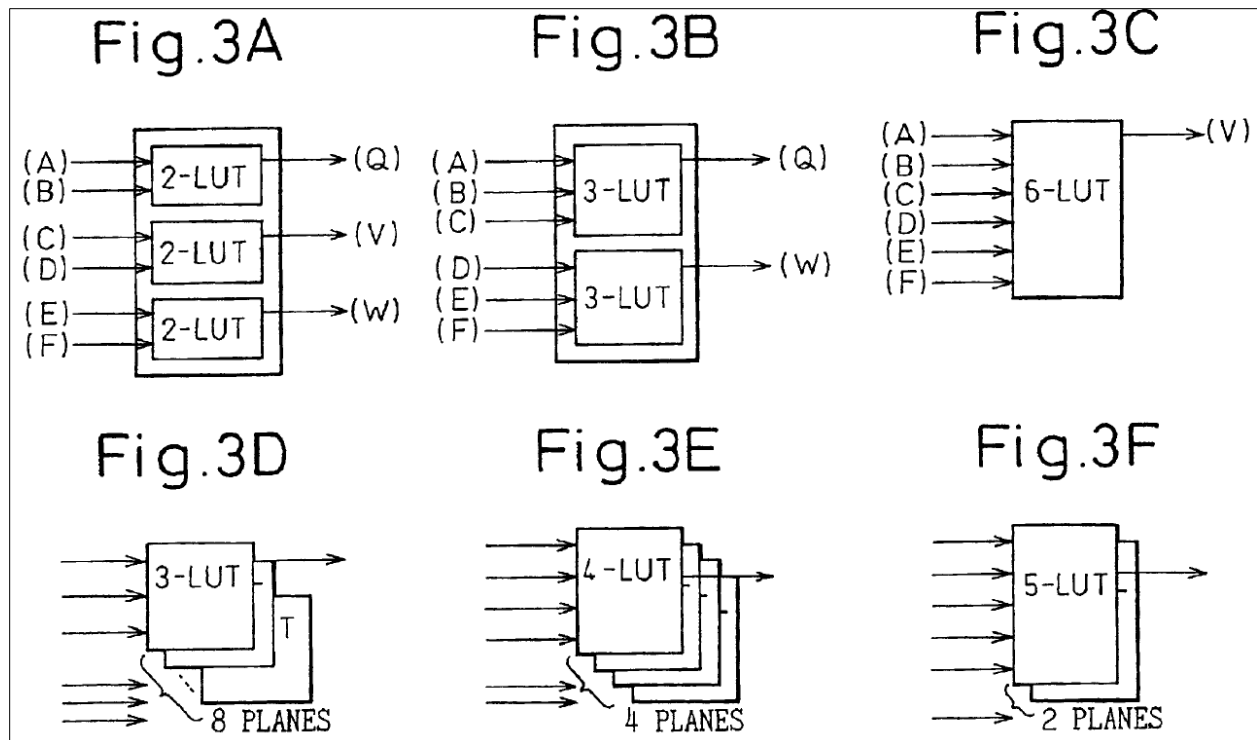


Fujii, FIG.1 (annotated). Selectors x16 and x17, controlled by control signal A, ensure that the same input signals (a-b) are “appl[ied]” to the top and middle 2-LUTs. Fujii, ¶¶12, 24-28, 42, FIG.6(3). In accordance with control signals A and B and input signal c, selector x12 selects the outputs of the top and middle 2-LUTs, and the output of the bottom 3-LUT is passed through CMOS transfer gate x23

(purple lines). As a result, “out1 acts as the output terminal of the [three]¹²-input programmable logic element,” Fujii, ¶43, and “out3 acts as the output terminal of the three-input programmable logic element,” Fujii, ¶44. *See also* Fujii, ¶¶12, 47, FIGS.1, 6(2); Melvin, ¶105.

This mode-switching is not materially different from the “*controlling an internal configuration of said plurality of LUT units*” described in the ’737 patent. The patent describes “internal configurations” as “configuration modes” that are switched by varying values of a memory. *See* ’737-patent, 7:17-20 (“[The 6-input 3-output LUT...may be used in various modes of *internal configuration* by varying the values X, Y, Z of the mode changing memory.”), 6:15-19 (“*internal configurations (configuration modes)*”). Figures 3A through 3F show “different modes of internal configuration of [a] 6-input 3-output LUT”:

¹² “[F]our” is a typographical error that should be “three[.]” Melvin, ¶105 n.11; Fujii, ¶43 (indicating input signals “a, b, and c” are applied to the top 3-LUT).



Similarly, Fujii’s three modes are internal configurations of the “*LUT units*” that are switched by varying values of control signals as shown in FIG.6. Melvin, ¶106.

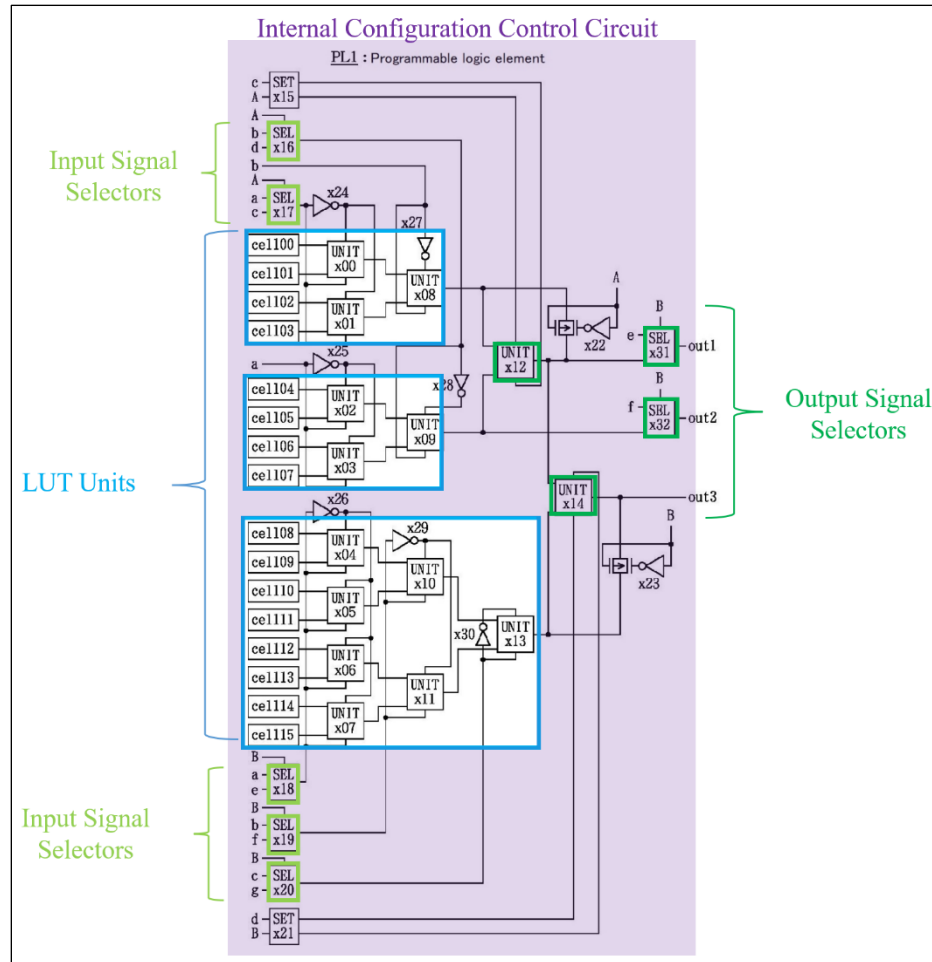
Thus, Fujii discloses an “*internal configuration control circuit* [the control signals, selectors, control circuits, CMOS transfer gates, and wires connecting those components to each other and/or other components within PL1] *controlling an internal configuration of said plurality of LUT units* [by switching between the three use modes shown in FIG.6].” Melvin, ¶¶100-107.

4. [1C] “wherein said internal configuration control circuit comprises a plurality of selectors selecting I/O signals of said plurality of LUT units, and”

Fujii discloses this limitation because it discloses selectors x16-x20 that select input signals of the “*plurality of LUT units*” in PL1 and selectors x12, x14,

x31, and x32 that select output signals of the “*plurality of LUT units*” in PL1. Fujii, ¶¶59-64, 67-68, FIG.8 (substantially similar selectors in PL2); Fujii, ¶¶86-87, 90-92, FIG.15 (substantially similar selectors in PL3); Melvin, ¶¶108-113. These selectors are part of “*said internal configuration control circuit.*” See *supra* [1B].

Annotated FIG.1 below shows each of the input signal selectors (light green) and output signal selectors (green) “*selecting I/O signals of said plurality of LUT units*”:



On the input side, based on the value of control signal A, selector x16 selects between inputs b and d to selector x09 (part of the middle 2-LUT “*LUT unit*” (see [1A])). Fujii, ¶24, FIGS.1, 6(2). Similarly, based on the value of control signal A, selector x17 selects between inputs a and c to selectors x00 and x01 (part of the top 2-LUT “*LUT unit*” (see [1A])). Fujii, ¶25, FIGS.1, 6(2). Likewise, based on the value of control signal B, selectors x18, x19, and x20 select between inputs to the bottom 3-LUT “*LUT unit*” (see [1A])). Fujii, ¶¶26-28, FIGS.1, 6. Each of these inputs is an input signal and, thus, an “*I/O signal*.” Fujii, ¶¶37-38, FIG.6, Explanation of References; Melvin, ¶¶109-110.

On the output side, when selector x12 is active—i.e., when the value of control signal A is 1, such that “selector x12” has not been rendered “non-conductive regardless of the selection signal” (Fujii, ¶19)—it selects between the outputs of selectors x08 and x09—each of which is part of a “*LUT unit*” (the top 2-LUT and middle 2-LUT, respectively). Fujii, ¶¶39-40, 42-44, FIGS.1, 6(1), 6(3). Similarly, when selector x14 is active—i.e., when the value of control signal B is 1, such that “selector x14” has not been rendered “non-conductive regardless of the selection signal”—it selects between the output of selector x12 and the output of selector x13 (the output of the bottom 3-LUT), the latter of which is an output of a “*LUT unit*.” Fujii, ¶¶39-40, FIGS.1, 6(1). Also, in Mode 6(2), selector x31 selects between input signal e and the output of selector x08, the latter of which is an

output from a “*LUT unit*” (i.e., the top 2-LUT). Fujii, ¶¶45-48, FIGS.1, 6(2).

Likewise, in Mode 6(2), based on the value of control signal B, selector x32 selects between input signal f and the output from selector x09, the latter of which is an output from a “*LUT unit*” (i.e., the middle 2-LUT). Fujii, ¶¶45-48, FIGS.1, 6(2).

Each output from a “*LUT unit*” is a signal and, thus, an “*I/O signal*.” Melvin, ¶¶111-112.

These selectors are part of the “*internal configuration control circuit controlling an internal configuration of said plurality of LUT units*.” See *supra* [1B]. Thus, Fujii’s “*internal configuration control circuit comprises a plurality of selectors [selectors x12, x14, x16-x20, x31, x32] selecting I/O signals [e.g., selector x16 selects between inputs b and d and selector x12 selects between outputs of the top and middle 2-LUTs] of said plurality of LUT units[.]*”

5. [1D] [wherein said internal configuration control circuit comprises . . .] “a selector control circuit having a memory, controlling said plurality of selectors in accordance with data stored in said memory, and defining the internal configuration of said plurality of LUT units.”

Fujii in combination with Betz (“Fujii-Betz”) renders this element obvious. Melvin, ¶¶114-127.

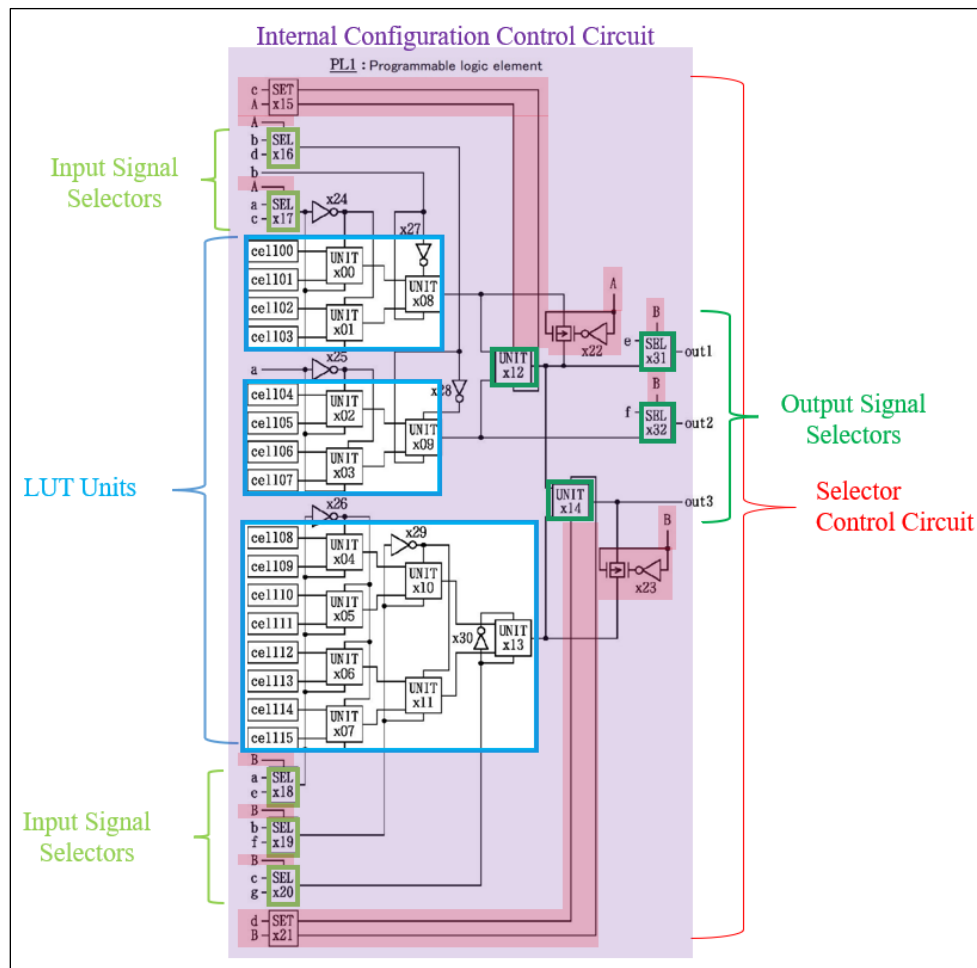
First, Fujii discloses “*a selector control circuit..., controlling said plurality of selectors..., and defining the internal configuration of said plurality of LUT units*” because it discloses control signals A and B, control circuits x15 and x21,

CMOS transfer gates x22 and x23, and the wires connecting those control signals and components to each other and/or other components in the internal configuration control circuit (*see supra* [1B]). Fujii, ¶¶12, 15, 36-48, 51, FIG.1; Melvin, ¶115; *see also* Fujii, ¶¶54-55, 71-79, FIG.8 (substantially similar circuits in PL2); Fujii, ¶¶80, 94-97, FIG.15 (substantially similar circuits in PL3). As discussed above, these components in the “*selector control circuit*” are part of “*said internal configuration control circuit*” (*see supra* [1B]) that “*define[s] an internal configuration of said plurality of LUT units,*” because these components (as part of the internal configuration control circuit) define PL1’s use modes.

Control signals A and B, along with the other circuitry listed above, define PL1’s use modes by controlling selectors. *See supra* [1B], [1C]. For example, depending on the values of control signals A and B, control circuits x15 and x21 in conjunction with transfer gates x22 and x23 determine whether selector x12 and selector x14 operate as part of selection circuits and are connected to outputs (out1 and out3, respectively). Fujii, ¶¶19, 30, 34-35, 39, 42, 45, 47, FIGS.1, 6; Melvin, ¶116. Moreover, depending on the values for control signals A and B, selectors x16-x20 select inputs to the “*LUT units*” and selectors x31 and x32 select outputs from the “*LUT units.*” *See supra* [1C].

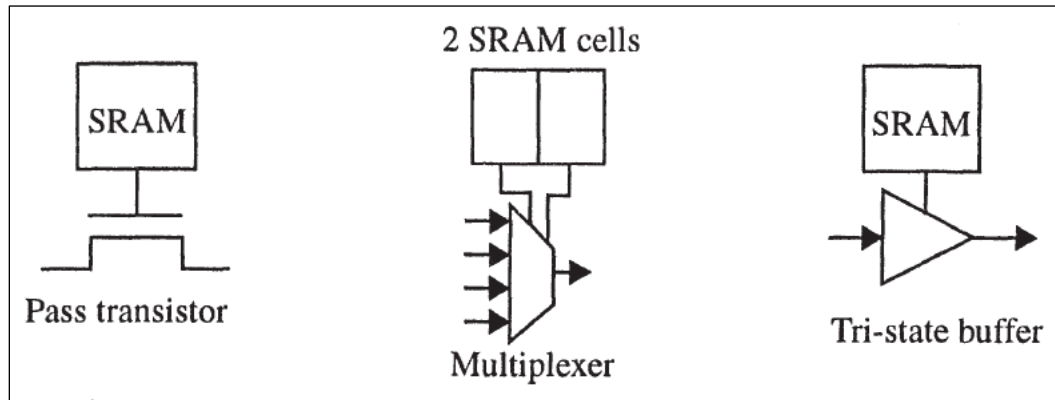
These components form “*a selector control circuit*” that controls “*said plurality of selectors*” and “*defin[es] the internal configuration of said plurality of*

LUT units,” because they establish what use modes PL1 operates in, and those modes are controlled by selectors that are controlled by the values of control signals A and B. *See supra* [1B] (describing how PL1 switches use modes); [1C] (describing control of selectors); Melvin, ¶117. Annotated FIG.1 below shows the “selector control circuit” (in red) of PL1:

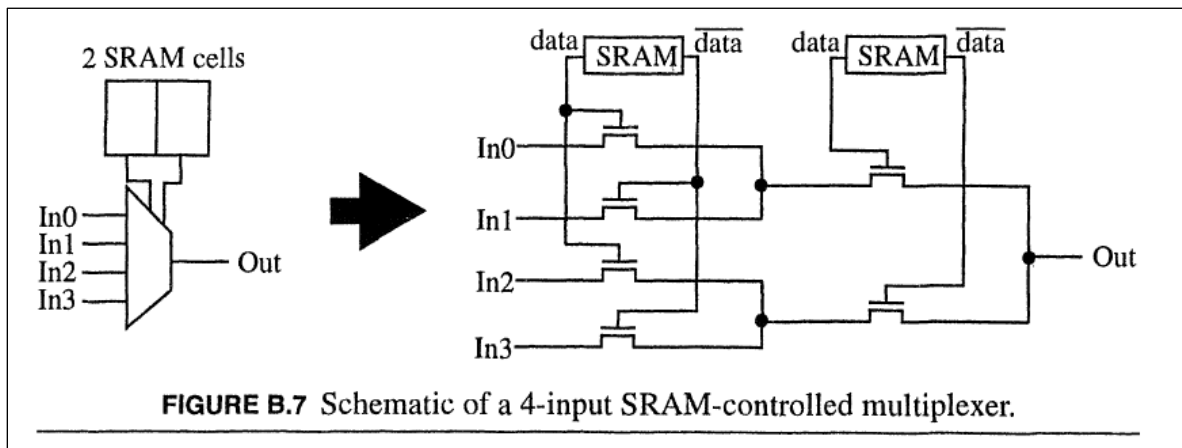


Second, Betz discloses “having a memory” and “controlling [a] plurality of selectors in accordance with data stored in said memory[.]” In particular, Betz’s FIG.2.2 shows three types of switches controlled in accordance with data stored in

memory, e.g., controlling a 4-to-1 multiplexer in accordance with data stored in 2 SRAM cells:

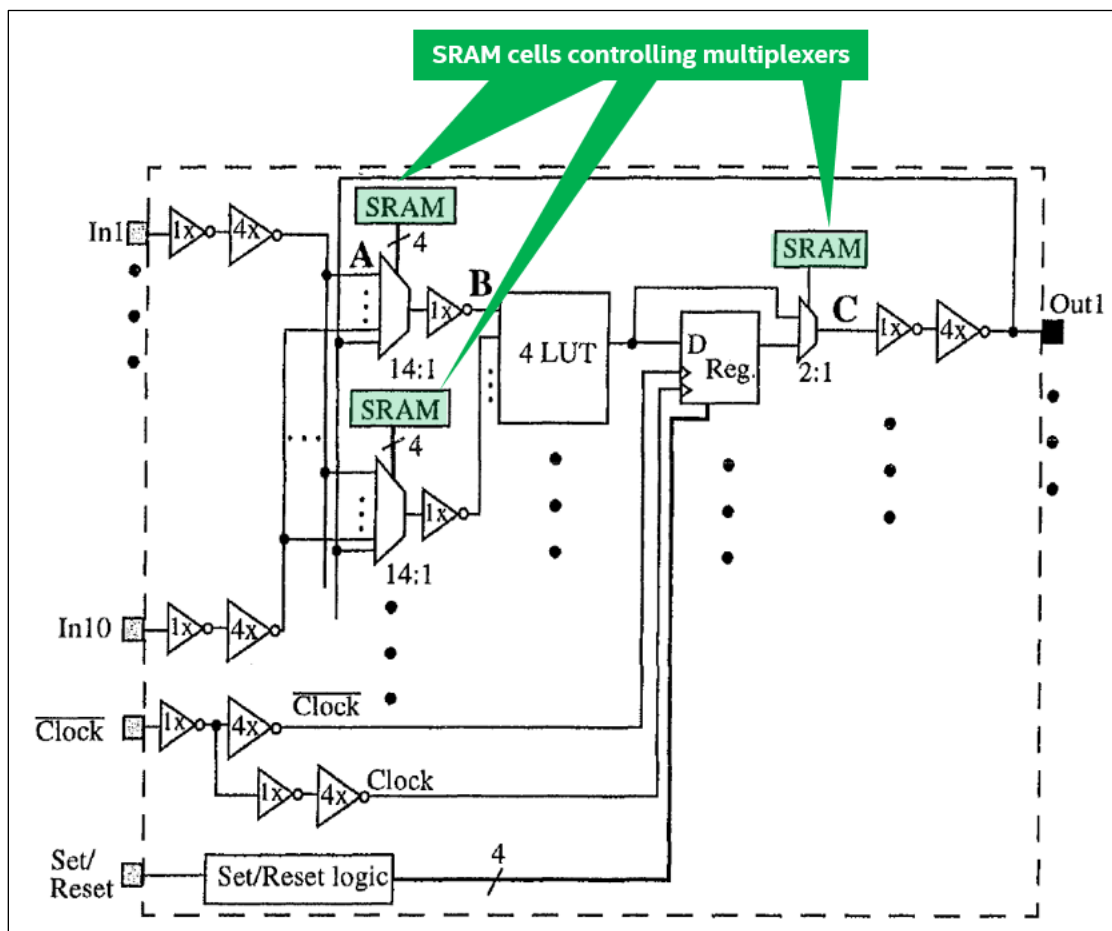


See also Betz, 12, 209, FIG.B.2 (pass transistor); Trimberger, 19-21 & FIG.2.3.2.c (2-to-1 multiplexer controlled by SRAM-based configuration memory); Brown-FPGA pp. 15-16, Fig. 2.2 (SRAM-based transmission gate and multiplexer). Betz's FIG.B7 shows that each SRAM cell contains "data" in memory that is used to control the switches:



See also Betz, 208, 213, FIG.B.1; Melvin, ¶118.

Betz also teaches that it was known to implement SRAM-based switches to control selection of inputs and outputs of look-up tables within a logic block. Betz, 214, FIG.B.8; Melvin, ¶119. For example, FIG.B.8 has a “logic block” with four “4-input look-up table[s]” (one labeled “4 LUT” below) and sixteen 14-to-1 multiplexers at the inputs of the 4-LUTs and four 2-to-1 multiplexers at the outputs of each “4-LUT.” Betz, 214-216.



Betz, 214, FIG.B.8 (annotated). Each SRAM cell (green) to the left of the illustrated “4 LUT” uses 4 data bits to control a 14-to-1 multiplexer, which selects inputs to the “4 LUT.” Betz, 214, FIG.B.8. The SRAM cell (green) to the right of

the illustrated “4 LUT” uses 1 data bit to control a 2-to-1 multiplexer, which selects an output from the “4 LUT.” Betz, 214, FIG.B.8. Each SRAM cell is located within Betz’s logic block. Betz, FIG.B.8.

Betz therefore teaches “*having a memory*” [SRAM cells within the logic block] and “*controlling [a] plurality of selectors* [the 14-to-1 multiplexers at the inputs to the “4 LUTs” and the 2-to-1 multiplexers at the output of the “4 LUTs”] *in accordance with data stored in said memory* [the data stored in each SRAM cell].” Melvin, ¶120.

A POSA would have been motivated to modify Fujii’s “*selector control circuit*” that controls a “*plurality of selectors*” and “*defin[es] the internal configuration of said plurality of LUT units*” to “*control said plurality of selectors in accordance with data stored in said memory*” as taught in Betz. Indeed, Betz provides express motivation to modify Fujii by teaching that the use of SRAM cells to control programmable switches is “the most popular” of the “three different approaches to making FPGAs programmable[.]” Betz, 11-13; *see also* Trimberger, 15-21 (“SRAM-programmable FPGAs have become very popular.”); Brown-FPGA, 15-16 & FIG.2.2, 21 (“[S]tatic RAM programming technology [was] used in FPGAs produced by several companies” as of 1992.); Melvin, ¶121.

Moreover, Fujii does not specify implementation details regarding the source of control signals A and B, which are used to control the “*plurality of*

selectors.” See supra [1B], [1C]. Thus, a POSA would have been motivated to consult other references, including Betz, to fill in those details. In particular, a POSA would have consulted Betz because it “provides background information about FPGA architecture” (Betz, 11), and PL1 is used in FPGA architecture (Fujii, ¶¶3, 5, 6, 102). Moreover, Betz provides implementation details for SRAM-controlled switches, and control signals A and B are used to control similar switches, i.e., selectors (multiplexers), transfer gates (switches), and control circuits (switches). *Compare* Fujii, FIG.2, ¶16 (“FIG. 2 is a circuit diagram showing a concrete example of selector x16[.]”) *with* Weste, 17, FIG.1.10(c) (showing same CMOS 2-input “multiplexer”); *compare* Fujii, FIG.1 (transfer gates x22, x23) *with* Weste, 8, FIG.1.3 (same complementary “switch”); *compare* Fujii, FIG.3, ¶18 (control circuit x15) *with* Weste, 14-15 (“compound gate is formed by using...switch structures”). Thus, a POSA would have consulted Betz for details about the source of control signals A and B, i.e., that one or both of those signals could be stored in data in SRAM cells. Melvin, ¶122.

Separately, there were well-known advantages in using SRAM technology because “it provides an FPGA that can be re-configured (in-circuit) very quickly and it can be produced using a standard CMOS process technology.” Brown-FPGA, 16. This would have also motivated the use of SRAM technology in the manner described above. Melvin, ¶123.

These reasons, separately and collectively, would have motivated a POSA to modify Fujii in light of the teachings in Betz.

Moreover, a POSA would have had a reasonable expectation of success in modifying Fujii in this way because, as discussed above, Betz teaches the use of SRAM-based switches to control selection of inputs and outputs of look-up tables within a logic block similar to Fujii's PL1, which already uses switches in that same way. Betz, 214, FIG.B.8. Indeed, Betz teaches that SRAM-controlled switches were "the most popular technology" at the time for FPGAs. Betz, 11-12. Also, PL1 uses CMOS process technology (Fujii, ¶¶15, 20, 22, 33-35, 39, 42, 47, p.10 (describing FIG.4)), and SRAM programming technology "can be produced using a standard CMOS process technology" (Brown-FPGA, 16); Melvin, ¶125.

Modifying Fujii in this way amounts to use of a known technique (Betz's SRAM-based switches to control selection of inputs and outputs of look-up tables) to improve a similar device (PL1, which addresses the same problem of controlling selection of inputs and outputs of look-up tables) in the same way ("provid[ing] an FPGA that can be re-configured (in-circuit) very quickly," *see* Brown-FPGA, 16). *See Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th 1373, 1380-81 (Fed. Cir. 2023); Melvin, ¶126.

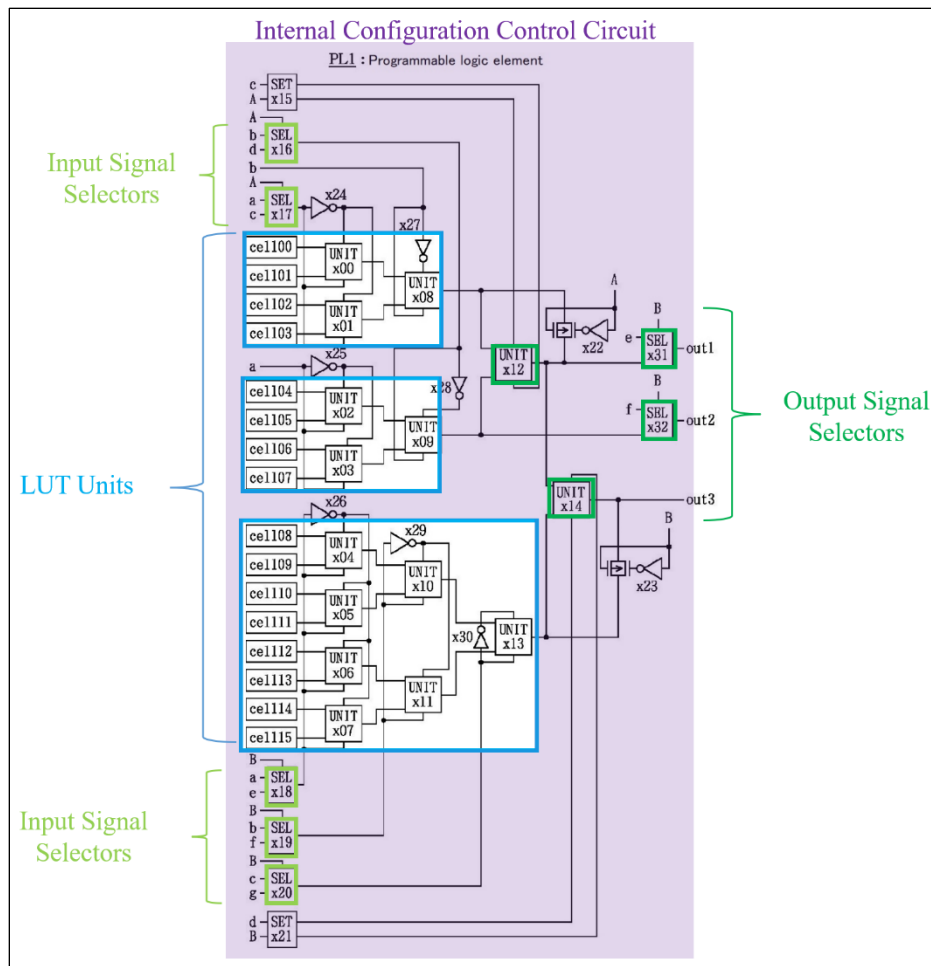
Fujii-Betz therefore teaches this element because, when the values of one or both of control signals A and B in Fujii's internal configuration control circuit (*see*

[1B], [1C]) are stored in SRAM cells as taught in Betz, PL1 comprises “*a selector control circuit having a memory, controlling said plurality of selectors in accordance with data stored in said memory, and defining the internal configuration of said plurality of LUT units.*”

C. Claim 2

- 1. [2A] “The look up table as claimed in claim 1, wherein said plurality of selectors include: an input signal selector provided at an input of at least one of said LUT units to select an input signal; and”**

Fujii discloses this limitation because, as discussed above ([1C]) and shown in annotated FIG.1 below, selectors x16-x20 are each provided at an input of at least one of the “*LUT units*” in PL1 to select an input signal. Melvin, ¶128. Annotated FIG.1 below shows each “*input signal selector*” (light green):

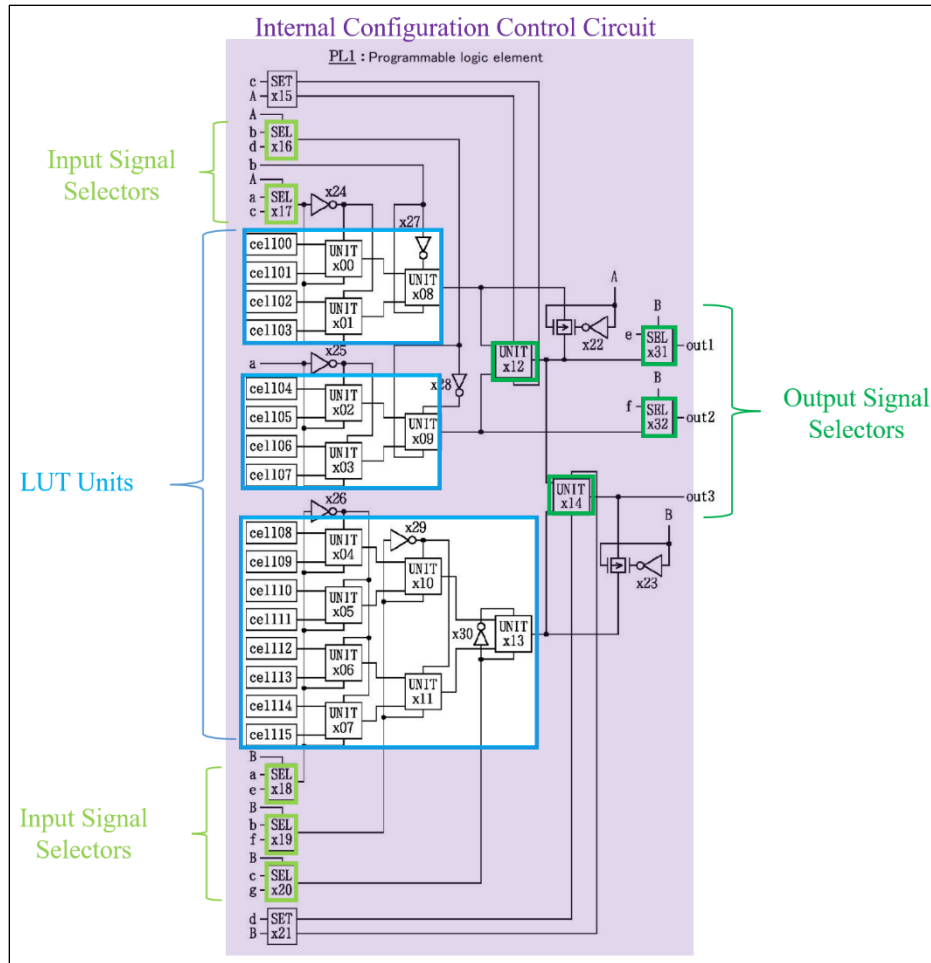


See also Fujii, FIGS.8 (substantially similar for PL2), 15 (substantially similar for PL3).

2. [2B] [wherein said plurality of selectors include: . . .] “an output signal selector provided at an output of said LUT units selecting an output signal,”

Fujii discloses this limitation because, as discussed above ([1C]) and shown in annotated FIG.1 below, selectors x12, x14, x31, and x32 are each provided at an output of the “LUT units” in PL1 to select an output signal. Melvin, ¶129.

Annotated FIG.1 below shows each “output signal selector” (green):



See also Fujii, FIGS.8 (substantially similar for PL2), 15 (substantially similar for PL3).

3. [2C] “said input signal selector and said output signal selector being controlled in accordance with the data stored in said memory.”

Fujii-Betz renders this limitation obvious. As discussed above ([1D]), Betz teaches controlling input selectors and output selectors with data stored in memory composed of SRAM cells. As explained ([1D]), it would have been obvious to modify Fujii to store control signal A, control signal B, or both as data in memory

located within PL1 to control selectors, including an input signal selector and output signal selector as identified in [2A]-[2B]. Melvin, ¶130. Therefore, Fujii-Betz discloses “*said input signal selector and said output signal selector being controlled in accordance with the data stored in said memory.*” See also *supra* [1D] (substantially similar for PL2 and PL3).

D. Claim 3

1. **[3A] “The look up table as claimed in claim 1, wherein said plurality of selectors include: an input signal selector provided at an input of at least one of said LUT units to select an input signal; and”**

Fujii discloses this limitation. As discussed above ([2A]), selectors x16-x20 in PL1 are each “*an input signal selector provided at an input of at least one of said LUT units to select an input signal.*” Melvin, ¶131; see also *supra* [2A] (substantially similar for PL2 and PL3).

2. **[3B] [wherein said plurality of selectors include: . . .] “an output signal selector provided at an output of said LUT units selecting an output signal,”**

Fujii discloses this limitation. As discussed above ([2B]), selectors x12, x14, x31, and x32 are each “*an output signal selector provided at an output of said LUT units selecting an output signal.*” Melvin, ¶132; see also *supra* [2B] (substantially similar for PL2 and PL3).

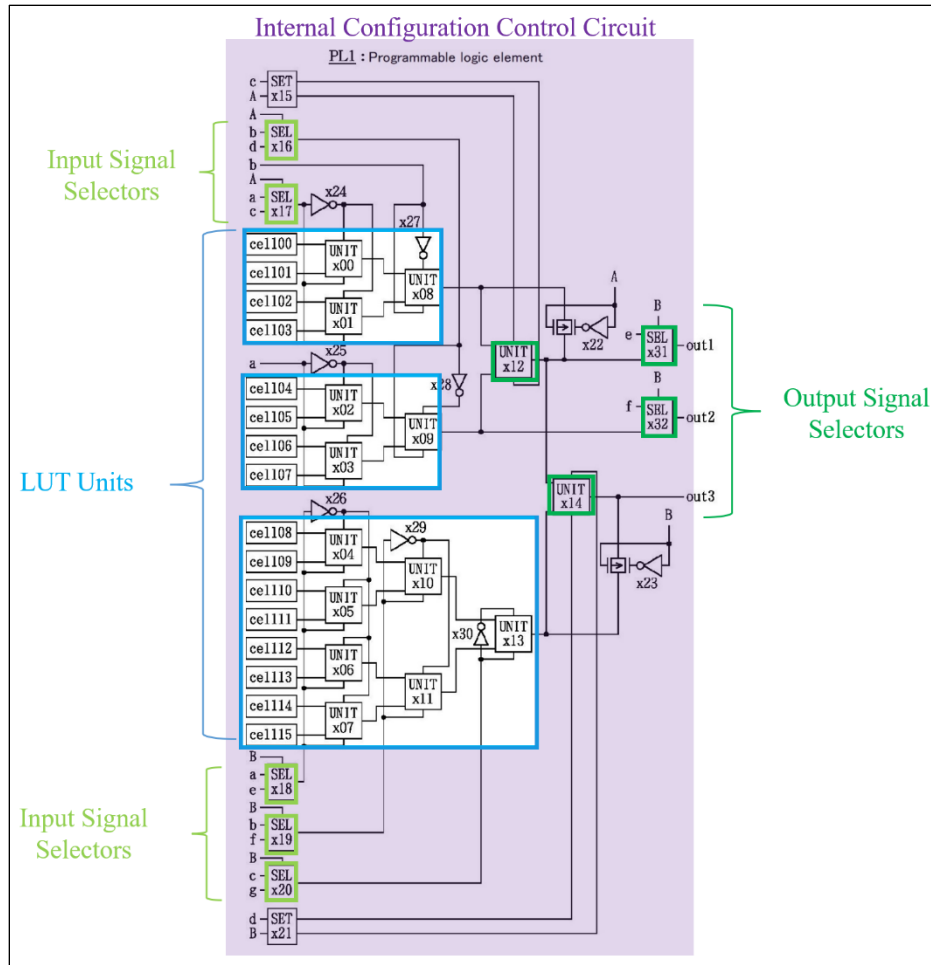
3. [3C] “said input signal selector and said output signal selector being controlled in accordance with the input signal.”

Fujii-Betz renders this limitation obvious. Melvin, ¶¶133-138. Fujii discloses controlling output signal selectors x12 and x14 in accordance with input signals c and d, respectively. *See, e.g.*, Fujii, ¶¶18-19, 29-30, 39, 42, p.10 (labelling “a, b, c, d, e, f, and g...input signals”). Input signal c and control signal A are input into control circuit x15, which determines whether selector x12 is rendered non-conductive or is used as a selection circuit. Fujii, ¶¶15, 18-19, 29, 39, 42, 47. Similarly, input signal d and control signal B are input into control circuit x21, which determines whether selector x14 is rendered non-conductive or is used as a selection circuit. Fujii, ¶¶15, 18-19, 30, 39, 42, 47.

It would have been obvious to modify Fujii’s PL1 to use one of input signals a-g to control one or more input signal selectors discussed above. *See supra* [2A], [3A]. This would have been a simple substitution of one known element (one of Fujii’s input signals) for another known element (control signal A or B), each of which controls both input and output selectors, as discussed above ([1B], [1C], [2A]-[2B]) to obtain predictable results (the use of a signal entering PL1 to control input selectors). Moreover, a skilled artisan would have had a reasonable expectation of success in making this modification given the disclosures in Fujii and Betz. Melvin, ¶134.

Thus, Fujii-Betz renders obvious “*said input signal selector* [input selectors x16-x20] *and said output signal selector* [output selectors x12 and x14] *being controlled in accordance with the input signal* [e.g., input signal c or d].”

Alternatively, control signals A and B are “*input signals*” that control input and output selectors as discussed above. *See supra* [1B]-[1C], [2A]-[2B]. Fujii discloses that PL1 “*inputs* at least one control signal” (Fujii, ¶14; *see also* Fujii, claim 1, ¶12), making those control signals “input signals.” *See also* ’737-patent, FIGS.6, 9 (showing input selectors controlled exclusively by X, Y, and Z). Further, as discussed above ([2A]-[2C], [3A]-[3B]), and as shown in annotated FIG.1 below, control signal A controls input signal selectors x16-x17 and output signal selector x12 (via control circuit x15), while control signal B controls input signal selectors x18-x20 and output signal selectors x14 (via control circuit x21) and x31-x32. Thus, Fujii discloses “*said input signal selector* [any one of selectors x16-x20] *and said output signal selector* [any one of selectors x12, x14, x31, and x32] *being controlled in accordance with the input signal* [control signals A or B or input signals c or d].”



Fujii, FIG.1 (annotated). Further, as discussed above ([1D]), when the value of exactly one of control signals A or B is set using data stored in SRAM cells (*see Betz*), the selectors controlled by that control signal (A or B) also are controlled “*in accordance with data stored in said memory,*” thereby satisfying the limitations in both [1D] and [3C]. Melvin, ¶¶136-137; *see supra* [1D].

E. Claim 4: “The look up table as claimed in claim 1, wherein said look up table of M inputs and N outputs is a 6-input 3-output look up table.”

This limitation would have been obvious in light of the teachings of Fujii. Based on Fujii’s express teachings, it would have been obvious to modify PL1 to constitute a “6-input 3-output look up table.” Melvin, ¶¶139-145.

Fujii’s teachings expressly apply to a programmable logic element with a variable number of K input signals:

That is, the programmable logic element PL1 wherein more than *K input signals* are input, [the element] *is provided with 2^K memory circuits*, outputs at least one output signal, inputs at least one control signal, and has at least one selection circuit, characterized in that the following operations are switched by the above control signal[.]

Fujii, ¶14 (first brackets in original), ¶¶5-6, claim 1. In one operation mode, PL1 can implement an arbitrary logic circuit of K inputs. Fujii, ¶14. Fujii also teaches that the number of K inputs “is often 3-5” (Fujii, ¶5), necessarily contemplating K=6 as a less often number only one away from those “often” used. Melvin, ¶140.

Given these teachings, a POSA would have been motivated to modify PL1 to be capable of implementing an arbitrary logic circuit of six inputs (K=6 instead of K=4) by increasing the number of memory circuits in PL1 to 2⁶ (64) memory circuits (instead of 2⁴). It was well known that wider look-up tables (i.e., look-up tables capable of implementing an arbitrary logic circuit of more inputs) provided

advantages over smaller look-up tables for certain applications. *See, e.g.*, Trimberger, 66 (explaining that, compared to “[n]arrower” 4-input look-up tables, “wider lookup tables would allow faster functions of more variables”). A 6-input look-up table offers speed advantages. He, Abstract (noting 5-, 6-, and 7-input look-up tables are “superior in terms of system speed” compared to 4-LUTs); Brown-FPGA, 108-09 (noting that, in some cases, 5-, 6-, and 7-input LUTs offer the best performance); Singh at 285 (“[T]he five- and six-input lookup tables are good choices for” some “realistic values for routing delay.”). To utilize these speed benefits, a POSA would have been motivated to modify PL1 to be capable of implementing an arbitrary logic circuit of six inputs (i.e., $K=6$). This would also be a simple substitution ($K=6$ for $K=4$) of known elements (the number of input signals and the corresponding number of memory circuits) to obtain predictable results (PL1 capable of implementing an arbitrary logic circuit of 6 inputs). A POSA would have had a reasonable expectation of success in achieving this modification because, as discussed above, Fujii expressly teaches that PL1 may have any number of input signals (more than K) and a corresponding number of memory circuits (2^K). Melvin, ¶141.

Moreover, this modified version of PL1 would have exactly three outputs. The disclosed embodiment of PL1 has three output terminals (out1, out2, out3), *see* Fujii ¶¶34-35, 37-38, 40-48, FIGS.1, 6(1)-6(2), and modifying that disclosed

embodiment of PL1 to have $K=6$ (64 memory circuits) without changing the number of outputs would have been routine. Fujii itself shows various programmable logic elements (PL2 and PL3) with different values for K (4 and 3, respectively) and the same number of outputs (2). Fujii ¶¶53-55, 79-81, FIGS.8, 13, 15, 20. Melvin, ¶142.

Additionally, Fujii teaches that PL1 with any number of input signals (more than K) still contains “plural memory circuit groups,” which are “*LUT units*” (see *supra* [1A]). Fujii, ¶14. It also “inputs at least one control signal” and has operations (i.e., modes) that “are switched by [that] control signal[,]” Fujii, ¶14, thereby “*controlling an internal configuration of said plurality of LUT units*” as described above ([1B]). This requires selecting different outputs from the “*LUT units*” to be “an output signal of the programmable logic element,” see Fujii, ¶14(i)-(ii), which requires at least one output signal selector as described above ([1B]-[1D], [2B]). Because PL1 inputs more than K inputs and has “a first operation using the K input signals as the selection signal of [a] selection circuit,” PL1 must have at least one input signal selector to ensure K inputs enter the selection circuit as described above ([1B]-[1D], [2A]). Fujii, ¶14; Melvin, ¶¶143-144.

Fujii therefore renders obvious “*said look up table [PL1] of M inputs [$K=6$] and N outputs [out1, out2, out3] is a 6-input 3-output look up table.*”

Alternatively, to the extent the claim is construed to mean the “*look up table of M inputs and N outputs*” requires only a minimum of M inputs and N outputs and need not be capable of implementing an arbitrary logic circuit of its inputs with at least one output, PL1 is a look-up table of at least 6 inputs (a-g) and three outputs (out1, out2, out3). Fujii, ¶¶35-41, FIGS.1, 6(2). Under this alternative construction, PL1 remains “[t]he look up table as claimed in claim 1, wherein said look up table of M inputs and N outputs is a 6-input 3-output look up table.” Melvin, ¶145.

F. Claim 5: “The look up table as claimed in claim 4, wherein said 6-input 3-output look up table comprises eight 3-input 1-output LUT units.”

As described above, Fujii-Betz renders obvious “[t]he look up table as claimed in claim 4.” See *supra* [4]. Claim 5’s additional limitations would have been obvious in light of Fujii. Melvin, ¶¶146-151. Based on Fujii’s express disclosures, it would have been obvious to implement the 6-input 3-output PL1 discussed above ([4]) using “*eight 3-input 1-output LUT units.*”

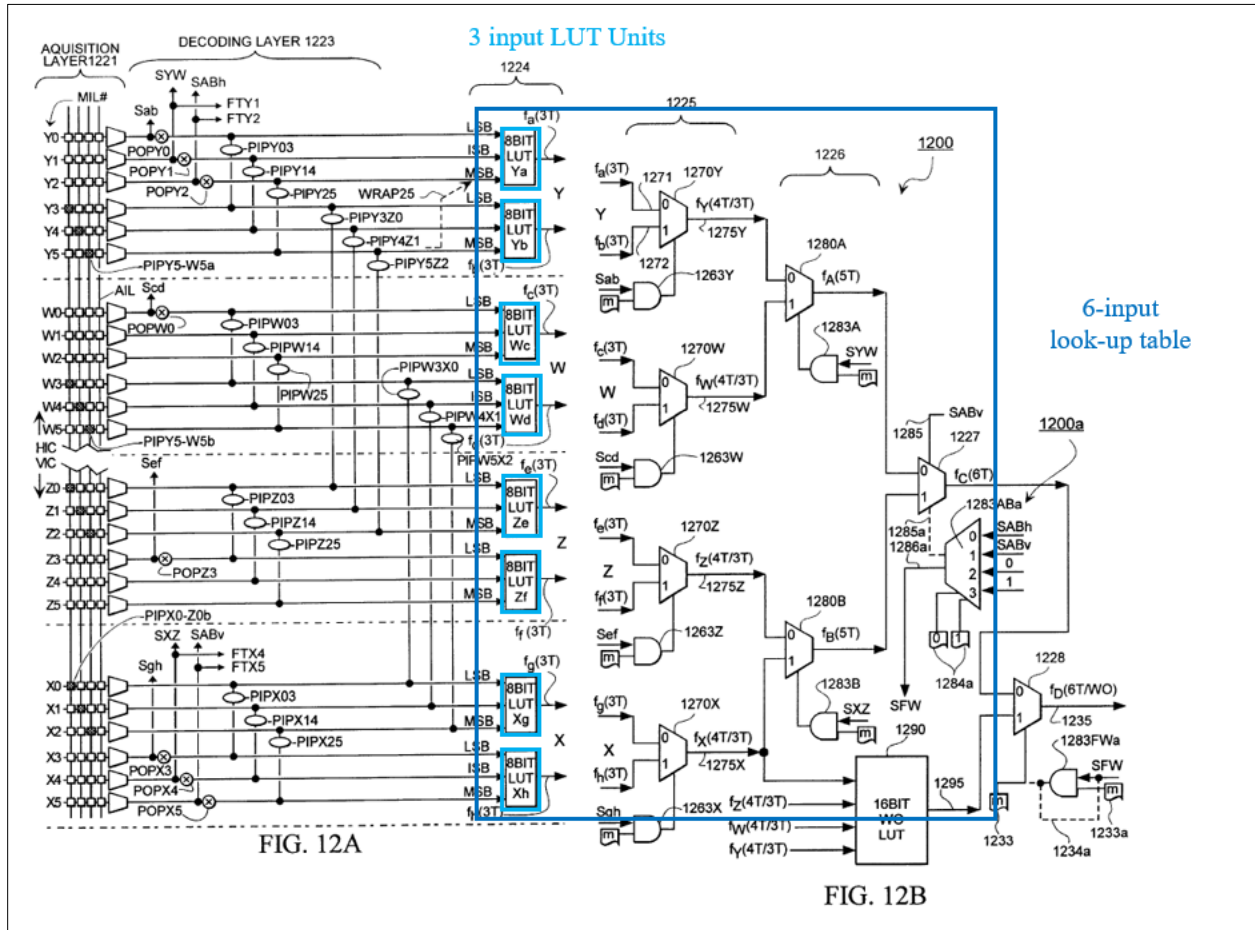
As noted (*supra* [4]), Fujii teaches that PL1 may have any number of input signals, i.e., more than “K input signals,” and a corresponding number of memory circuits, i.e., “ 2^K memory circuits.” Fujii, ¶¶5, 14, claim 1. Fujii further teaches that those “ 2^K memory circuits” may be “divided...into plural memory circuit groups” in various ways with each memory circuit group having “ 2^{X_i} memory circuits,”

where “X” is the number of input signals to a particular memory circuit group and “i” is an index, ranging from 1 to “n” (the total number of memory circuit groups), identifying a particular memory circuit group. Fujii, ¶14. Fujii expressly contemplates that each memory circuit group may have the same number of input signals (X_i) and, thus, the same number of memory circuits. Fujii, ¶14 (“where the sequence from $i=1$ to $i=n$ of the sequence $\{2^{X_i}\}$ ($2^{X_i} \leq 2^{X_{i+1}}$) is equal to $2^{[K]}$,” meaning “ 2^{X_i} ” may be equal to “ $2^{X_{i+1}}$ ”). Indeed, Fujii’s programmable logic element PL2 uses two 3-input, 1-output memory circuit groups. Fujii, ¶100 (“[T]he sequence $\{2^{X_i}\}$ in this case is $\{2^3, 2^3\}$.”), FIGS.8, 13. As explained, the plurality of memory circuit groups, each having X_i input signals and 2^{X_i} memory circuits, is a “*plurality of LUT units.*” See *supra* [1A], [4].

Given this teaching, a POSA would have been motivated to implement the modified PL1 described above ([4]) using eight memory circuit groups (i.e., $n=8$), each of which implements an arbitrary logic circuit of three inputs (i.e., $X_i=3$ for all i) on at least one output. Melvin, ¶148. This would have been a simple substitution ($n=8$ and $X_i=3$ for the undefined “n” and “ X_i ” in [4]) of known elements (input signals and corresponding memory circuit groups) to obtain predictable results. Moreover, Fujii expressly discloses an embodiment (PL2) in which $X_i=3$ for each memory circuit group ($i=1 \dots n$). Fujii, ¶100, FIG.13(1). This would have motivated

a POSA to implement the 6-input, 3-output PL1 in the same way, using $X_i=3$ for each memory circuit group ($i=1 \dots 8$).

It was well known and predictable that a 6-input look-up table could be constructed using eight 3-input, 1-output look-up tables. See Agrawal, 55:34-41, 57:44-58:18. Agrawal discloses “a plurality of eight” LUTs, each of which is a “3-input LUT.” Agrawal, 55:34-38. Through two layers of “function synthesis” (1225, 1226) (Agrawal, 56:22-56) and a 2-to-1 multiplexer (1227) (Agrawal, 57:58-58:18), these “3-input LUT[s]” can be combined to implement an arbitrary logic circuit of 6 inputs on one output ($f_c(6T)$) as shown below:



Agrawal, FIGS.12A-12B (combined and annotated), col. 55-58; Melvin, ¶149.

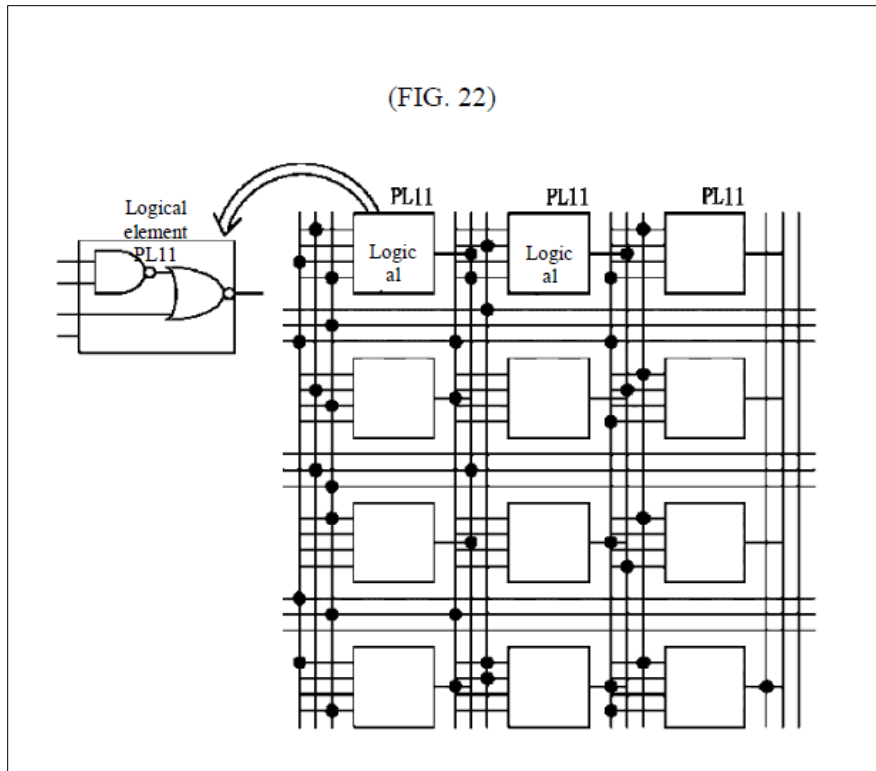
Moreover, a POSA would have had a reasonable expectation of success in so modifying PL1. Fujii expressly discloses that PL1's " 2^K memory circuits" may be "divided...into plural memory circuit groups" in various ways with each memory circuit group having " 2^{X_i} memory circuits," where X_i might be the same for every memory circuit group in PL1. Fujii, ¶14. Fujii also expressly discloses an embodiment (PL2) where $X_i=3$ for each memory circuit group ($i=1 \dots n$). Fujii, ¶100, FIG.13(1). Melvin, ¶150.

Fujii therefore renders obvious "[t]he look up table as claimed in claim 4, wherein said 6-input 3-output look up table comprises eight 3-input 1-output LUT units."

G. Independent Claim 7

1. Motivation to Combine the Fujii-Betz PL1 with Betz's FPGA Architecture

Fujii explains that PL1 is part of "an FPGA in which K-input LUTs are used as programmable logic elements and a plurality of these LUTs are arranged in an array" (Fujii, ¶6) and provides a "configuration example of an FPGA" in FIG. 22.



Fujii, FIG.22, ¶¶1-5, 11, 102. Yet Fujii lacks implementation details about FPGA architecture. A POSA would have been motivated to consult other references, including Betz, to fill in those details. In particular, a POSA would have been motivated to combine the Fujii-Betz PL1 (i.e., PL1 as modified by Betz such that the values of one or both of control signals A and B are stored in SRAM cells (*see supra* [1D])) with Betz’s disclosure of FPGA architecture. *See* Betz, 12-18; Melvin, ¶152.

Fujii expressly provides such a motivation because the stated “Effect of the Invention” is that “one programmable logic element can function as a programmable logic element with different numbers of inputs,” thereby “allow[ing] arbitrarily non-uniform sizes of programmable logic elements *on the*

FPGA, and the desired logic circuit can be achieved with fewer logic elements and fewer memories.” Fujii, ¶102. A POSA would have consulted Betz because it “provides background information about FPGA architecture” (Betz, 11), and PL1 is used in FPGA architecture (Fujii, ¶¶3, 5, 6, 102). Melvin, ¶152.

Moreover, Betz uses “LUT-based logic blocks” in its FPGA architecture (Betz, 13), similar to the LUT-based logic blocks in Fujii (Fujii, ¶6 (describing “an FPGA in which K-input LUTs are used as programmable logic elements and *a plurality of these LUTs are arranged in an array.*”)). Indeed, Fujii describes an improvement to LUT-based logic blocks:

The present invention, when realizing the desired logic function, is to provide a programmable logic element capable of efficiently realizing a desired logic function by using fewer logic elements and less memory according to the logic function to be realized.

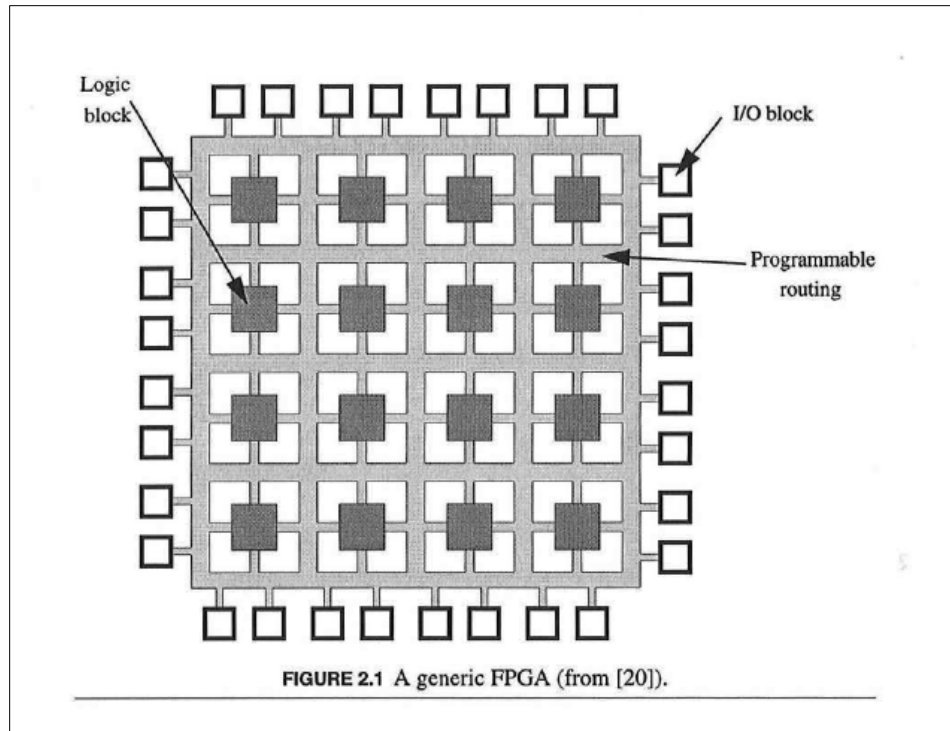
Fujii, ¶9; *see also* Fujii, ¶10, 102. A POSA, therefore, would have been motivated to apply Fujii’s known technique (the Fujii-Betz PL1) to improve a known device (Betz’s FPGA architecture) in the same way (providing a programmable logic element capable of using fewer logic elements and less memory). This also amounts to a simple substitution of one known element (the Fujii-Betz PL1) for another (the LUT in Betz’s LUT-based logic block) to obtain predictable results. Melvin, ¶¶154-155.

A POSA would have had a reasonable expectation of success in making this combination. The modified Fujii-Betz PL1 (e.g., [1PRE]-[1D]), would have worked for its intended purpose with Betz's FPGA architecture. And combining the Fujii-Betz PL1 with Betz's FPGA architecture would have led to predictable results, namely "fewer logic elements and less memory according to the logic function to be realized" in that FPGA. Fujii, ¶9; Melvin, ¶156.

2. [7PRE] "A programmable logic circuit device comprising:"

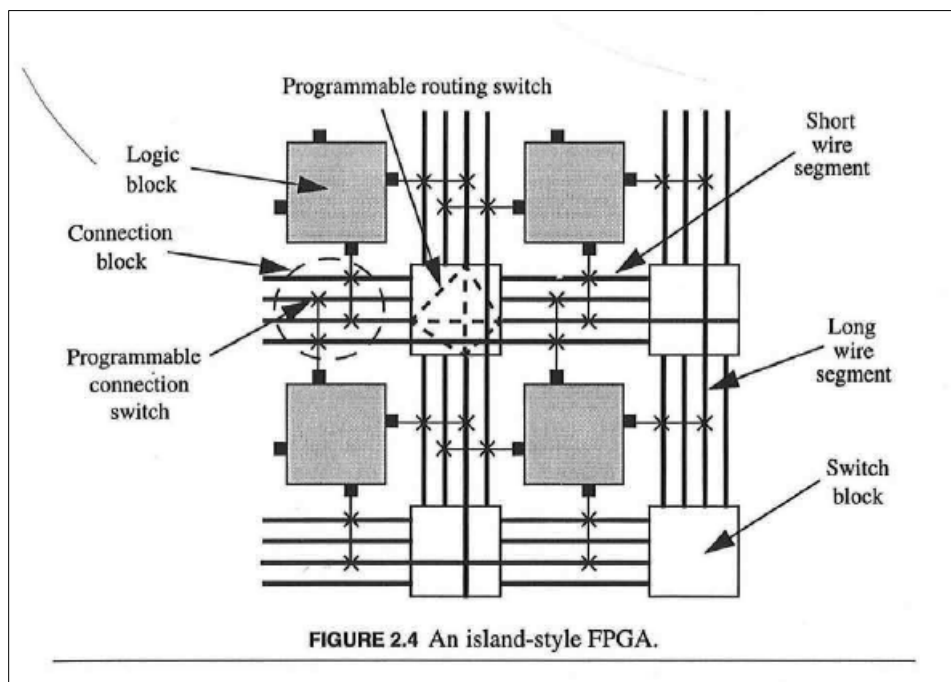
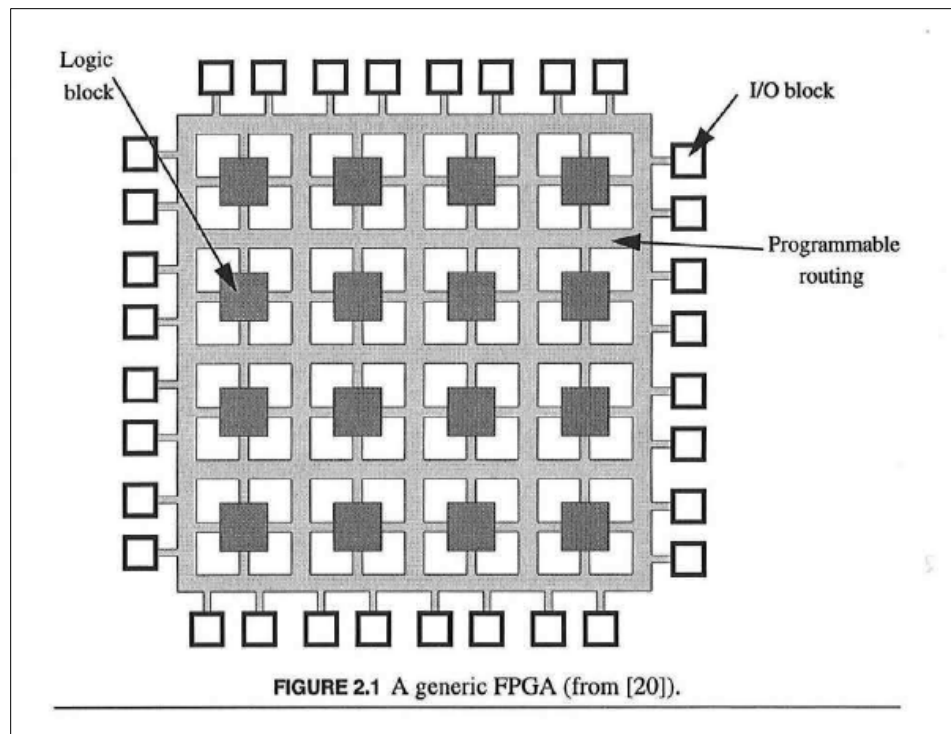
Betz discloses this limitation. Melvin, ¶¶157-158. Betz discloses a "generic FPGA" that includes "logic blocks, I/O blocks, and programmable routing." Betz, 11-12, FIG.2.1. An FPGA is a type of "*programmable logic circuit device*." '737-patent, 1:13-24 ("Such a *programmable logic circuit device* is known as PLD (Programmable Logic Device) or *FPGA* (Field Programmable Gate Array).").

Betz uses "island-style FPGAs" throughout its description of FPGA architecture in §2.1. Betz, 14 ("[W]e will almost exclusively investigate island-style routing architecture," with an exception for "some of the results" in Chapter 5 not relevant here). An example of such an FPGA is shown in FIG.2.1:



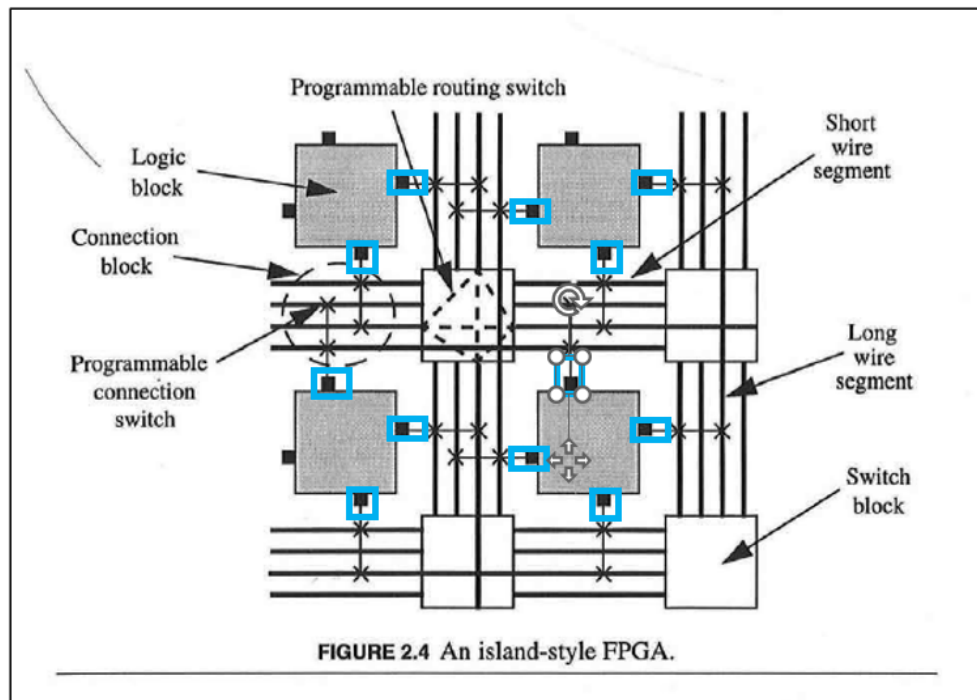
3. [7A] “a plurality of logic blocks;”

Betz discloses this limitation. Melvin, ¶159. Betz discloses a plurality of “LUT-based *logic blocks*,” Betz, 13, which are one of the “fundamental components” of an FPGA, Betz, 11. “A circuit is implemented in an FPGA by programming each of the[se] logic blocks to implement a small portion of the logic required by the circuit.” Betz, 11-15, FIGS. 2.1, 2.4. Betz’s “*plurality of logic blocks*” is shown below in FIG.2.1 and FIG.2.4.



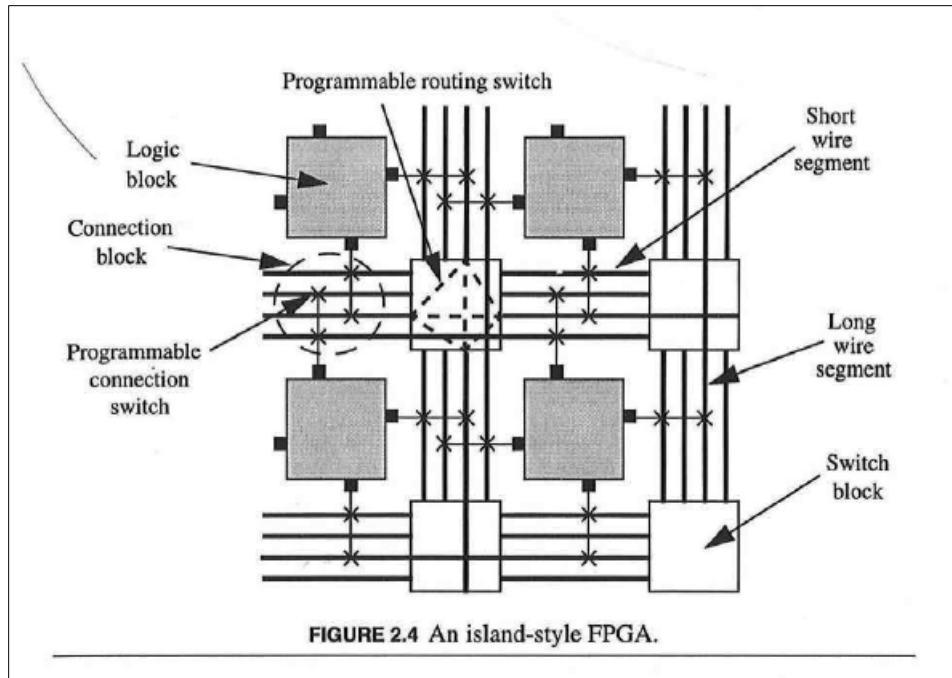
4. [7B] “a plurality of routing wires connected to each of said logic blocks;”

Betz discloses this limitation. Melvin, ¶160. Betz discloses that its “*logic blocks are surrounded* by routing channels of pre-fabricated *wiring segments on all four sides.*” Betz, 14. In addition, “[a] logic block input or output, which we call a pin, can connect to some or all of the wiring segments in the channel adjacent to it.” Betz, 14-15 (“The number of wires in each channel to which a *logic block pin* can connect is called the connection block flexibility, or F_c .”). As shown in FIG.2.4 below, Betz’s FPGA thus has “a plurality of routing wires [“short wire segment[s]” and “long wire segment[s]”] connected to each of said logic blocks [via logic block pins (in blue)].” Betz, 14-15, FIGS.2.4, 1.2, 1.3.



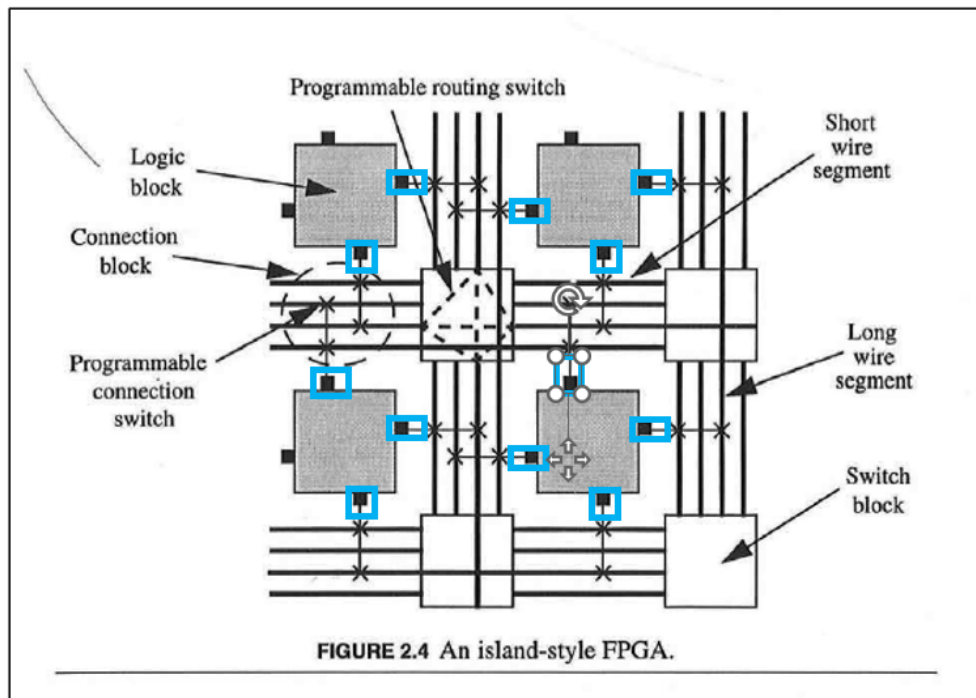
5. [7C] “a plurality of switch circuits provided at an intersection of each of said routing wires;”

Betz discloses this limitation. Melvin, ¶161. Betz teaches that, “[a]t every intersection of a horizontal channel and a vertical channel, there is a *switch block*....This is simply a set of programmable switches that allow some of the wire segments incident to the switch block to be connected to others; note that for clarity only a few of the programmable switches contained by switch blocks are shown in Figure 2.4.” Betz, 14. The “channel[s]” Betz references are made of the “wiring segments” used for routing. Betz, 14; *see supra* [7B]. As shown in FIG.2.4, Betz thus discloses “a plurality of switch circuits [“switch block[s]” each with a “[p]rogrammable routing switch”] *provided at an intersection of each of said routing wires* [“short wire segment[s]” and “long wire segment[s]”].” Betz, 14-15, FIG.2.4.



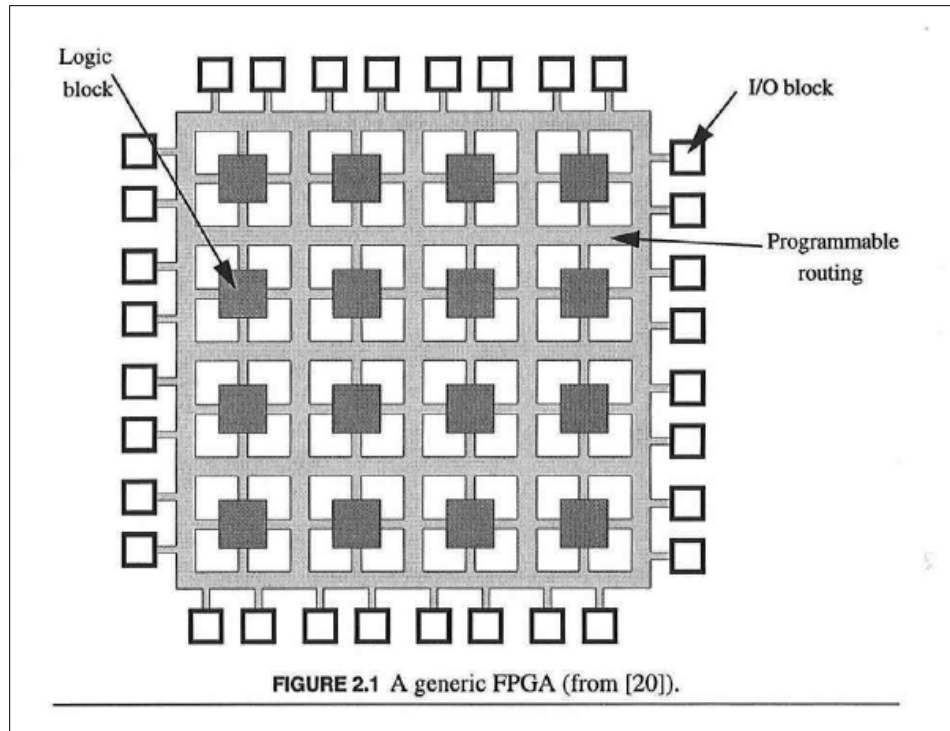
6. [7D] “a plurality of connection blocks provided between an I/O line of each of said logic blocks and each of said routing wires; and”

Betz discloses this limitation. Melvin, ¶162. Betz discloses that “[a] logic block input or output, which we call a pin, can connect to...*all of the wiring segments* in the channel adjacent to it via a *connection block*...of programmable switches.” Betz, 14. As shown in FIG.2.4, Betz thus discloses “a plurality of connection blocks [“[c]onnection block[s]”] provided between an I/O line of each of said logic blocks [the logic block pins (in blue)] and each of said routing wires [“short wire segment[s]” and “long wire segment[s]”].” Betz, 14-15, FIGS.2.4, 1.2, 1.3.



7. [7E] “an I/O block performing an input/output operation with external equipment,”

Betz discloses this limitation. Melvin, ¶163. Betz discloses “I/O blocks” that “act as either an input pad or an output pad, as required by the circuit” (Betz, 11), as shown in FIG.2.1 below.

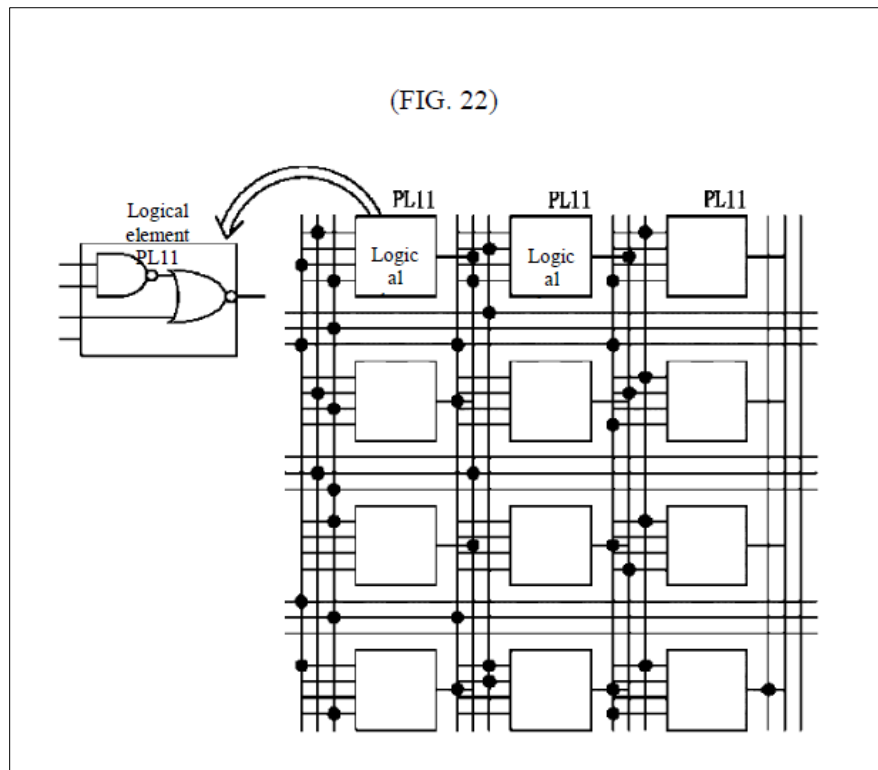


These I/O blocks are connected to pins on the device, Betz, 51, so they are necessarily used for “*performing an input/output operation with external equipment.*” See also Betz, 2-3 (describing how FPGAs “can be programmed” and “reprogramm[ed],” which necessarily requires performing input/output operations with external equipment), 208 (describing programmable SRAM cells); Trimberger, 15 (“An SRAM-programmable FPGA is programmed by loading *configuration memory cells* from ***an external source.***”). Betz thus discloses “*an I/O block [“I/O block”] performing an input/output operation with external equipment.*”

8. [7F] “wherein each of said logic blocks has a look up table of M inputs and N outputs, comprising:”

As noted, Betz uses “LUT-based logic blocks,” Betz, 13. A POSA would have been motivated to substitute the Fujii-Betz PL1 (i.e., PL1 as modified by Betz such that the values of one or both of control signals A and B are stored in SRAM cells (*see supra* [1D])) for the LUT(s) in each of those blocks (*see supra* VIII.G.1).
Melvin, ¶¶164-166.

Fujii itself uses the same programmable logic element (e.g., PL11) in each logic block of its FPGA, as shown in the “configuration example of an FPGA” in FIG.22. Fujii, ¶¶1-6, 9-10, 102, FIG.22.



As described above in claim 1, the Fujii-Betz PL1 is “*a look up table of M inputs and N outputs.*” A POSA therefore would have been motivated to use the Fujii-Betz PL1 in each of Betz’s logic blocks. Doing so would have been consistent with Fujii’s teaching that “one programmable logic element can function as a programmable logic element with different numbers of inputs,” thereby “allow[ing] arbitrarily non-uniform sizes of programmable logic elements on the FPGA, and the desired logic circuit can be achieved with fewer logic elements and fewer memories.” Fujii, ¶102.

Accordingly, “*each of said logic blocks [in Betz’s modified FPGA] has a look up table of M inputs and N outputs [the Fujii-Betz PL1].*”

9. [7G] “a plurality of LUT units; and”

This limitation is substantially similar to [1A] and disclosed by Fujii. *See supra* [1A].

10. [7H] “an internal configuration control circuit controlling an internal configuration of said plurality of LUT units,”

This limitation is substantially similar to [1B] and disclosed by Fujii. *See supra* [1C].

11. [7I] “wherein said internal configuration control circuit comprises a plurality of selectors selecting I/O signals of said plurality of LUT units, and”

This limitation is substantially similar to [1C] and disclosed by Fujii. *See supra* [1C].

12. [7J] **“a selector control circuit having a memory, controlling said plurality of selectors in accordance with data stored in said memory, and defining the internal configuration of said plurality of LUT units.”**

This limitation is substantially similar to [1D] and rendered obvious by Fujii-Betz. *See supra* [1D].

H. Claim 8

1. [8A] **“The programmable logic circuit device as claimed in claim 7, wherein said plurality of selectors include: an input signal selector provided at an input of at least one of said LUT units to select an input signal; and”**

This limitation is substantially similar to [2A] and disclosed by Fujii. *See supra* [2A].

2. [8B] **“an output signal selector provided at an output of said LUT units selecting an output signal,”**

This limitation is substantially similar to [2B] and disclosed by Fujii. *See supra* [2B].

3. [8C] **“said input signal selector and said output signal selector being controlled in accordance with the data stored in said memory.”**

This limitation is substantially similar to [2C] and rendered obvious by Fujii-Betz. *See supra* [2C].

I. Claim 9

1. [9A] **“The programmable logic circuit device as claimed in claim 7, wherein said plurality of selectors include: an**

input signal selector provided at an input of at least one of said LUT units to select an input signal; and”

This limitation is substantially similar to [3A] and disclosed by Fujii. *See supra* [3A].

2. [9B] “an output signal selector provided at an output of said LUT units selecting an output signal,”

This limitation is substantially similar to [3B] and disclosed by Fujii. *See supra* [3B].

3. [9C] “said input signal selector and said output signal selector being controlled in accordance with the input signal.”

This limitation is substantially similar to [3C] and rendered obvious by Fujii-Betz. *See supra* [3C].

J. Claim 10: “The programmable logic circuit device as claimed in claim 7, wherein said look up table of M inputs and N outputs is a 6-input 3-output look up table.”

Fujii-Betz renders obvious the programmable logic circuit device as claimed in claim 7. *See supra* [7PRE]-[7J]. This limitation is substantially similar to claim 4 and would have been obvious in light of Fujii. *See supra* [4].

K. Claim 11: “The programmable logic circuit device as claimed in claim 10, wherein said 6-input 3-output look up table comprises eight 3-input 1-output LUT units.”

Fujii-Betz renders obvious the programmable logic circuit device as claimed in claim 10. *See supra* [7PRE]-[7J], [10]. This limitation is substantially similar to claim 5 and would have been obvious in light of Fujii. *See supra* [5].

L. Independent Claim 13

1. [13PRE] “A method of configuring a look up table of M inputs and N outputs, comprising:”

Fujii discloses this limitation. Fujii’s PL1 is “*a look-up table of M inputs and N outputs.*” *See supra* [1PRE]; Fujii, FIG.1. Moreover, Fujii discloses components that define and control an internal configuration of “*LUT units*” of the look-up table. *See supra* [1A]-[1D]. A POSA would have understood that defining and/or controlling an internal configuration of the “*LUT units*” constitutes “[*a*] method of configuring a look up table of M inputs and N outputs.” Melvin, ¶179; *see also supra* [1PRE]-[1D] (substantially similar for PL2 and PL3).

2. [13A] “providing a plurality of LUT units, and”

As discussed above, Fujii discloses a “*plurality of LUT units*” in PL1. *See supra* claim 1[B]. Likewise, Fujii discloses “*providing a plurality of LUT units.*” Melvin, ¶180; *see also supra* [1B] (substantially similar for PL2 and PL3).

3. [13B] “selectively controlling I/O signals of said plurality of LUT units to set a predetermined mode of an internal configuration.”

Fujii-Betz renders obvious this limitation. Melvin, ¶181. Fujii discloses that, “A and B are control signals for determining the *use mode* of the programmable logic circuit PL1.” Fujii, ¶38, FIG.6. As discussed ([1A]-[1D]), control signals A and B “*set*” the use mode of PL1 by controlling selectors and other hardware that, in turn, “*selectively control[] I/O signals of said plurality of LUT units*” to define the internal configuration of “*LUT units*” in each use mode. These use modes are each a “*predetermined mode of an internal configuration[]*” See *supra* [1B]-[1D]; Fujii, ¶¶12-14, 36-48, FIGS.1, 6. Thus, Fujii-Betz renders obvious “*selectively controlling I/O signals of said plurality of LUT units to set a predetermined mode of an internal configuration.*” See also *supra* [1A]-[1D] (substantially similar for PL2 and PL3).

M. Claim 14: “The method of configuring a look up table as claimed in claim 13, wherein the I/O signals of said plurality of LUT units are selectively controlled in accordance with data stored in the corresponding look up table.”

Fujii-Betz renders obvious this limitation. Melvin, ¶182. As discussed ([1C]-[1D], 13[B]), “*the I/O signals of said plurality of LUT units are selectively controlled*” by selectors that are controlled by control signals A and B to “*determin[e] the use mode of the programmable logic circuit PL1.*” Fujii, ¶¶36-48, FIGS.1, 6. As explained ([1D]), it would have been obvious to apply the teachings

of Betz to modify PL1 to set the values of one or both of control signals A and B using data stored in memory composed of SRAM cells within PL1. *See supra* [1D]. By so doing, “*the I/O signals of said plurality of LUT units are selectively controlled*” by selectors controlled by control signals A and B as shown in FIG.6 “*in accordance with data stored* [the values of A and/or B stored in SRAM] *in the corresponding look up table* [Fujii’s PL1].” *See also supra* [1C]-[1D], 13[B] (substantially similar for PL2 and PL3).

N. Claim 15: “The method of configuring a look up table as claimed in claim 13, wherein an input signal input to at least one of said LUT units and an output signal output from said LUT units are selectively controlled in accordance with data stored in the corresponding look up table.”¹³

Fujii-Betz renders obvious this limitation. Melvin, ¶183. As discussed ([1B]-[1C], [2A]-[2B]), Fujii teaches that control signals A and B control input selectors x16-x20, each of which selectively controls “*an input signal input to at least one of said LUT units,*” as well as output selectors x12, x14, x31, and x32, each of which selectively controls “*an output signal output from said LUT units.*” *See supra* [1C]-[1D], [2A]-[2B], [13B]. As discussed ([1C]-[1D], [2A]-[2B], 13[B]), “*an input signal input to at least one of said LUT units and an output signal output from said*

¹³ As corrected by the Certificate of Correction entered April 26, 2005. *See* ’737-patent (last page).

LUT units are selectively controlled” by control signals A or B to “determin[e] the use mode of the programmable logic circuit PL1.” Fujii, ¶¶36-48, FIGS.1, 6. As explained ([1D], [2C]), it would have been obvious to apply the teachings of Betz to modify PL1 to set the values of one or both of control signals A and B using data stored in memory composed of SRAM cells within PL1. *See supra* [1D]. By so doing, “*an input signal input to at least one of said LUT units and an output signal output from said LUT units are selectively controlled*” by input selectors x16-20 and output selectors x12, x14, x31, and x32, which in turn are controlled by control signals A or B as shown in FIG.6 “*in accordance with data stored [the values of A and/or B in SRAM] in the corresponding look up table [Fujii’s PL1].*” *See also supra* [1B]-[1D], [2A]-[2B], [13B] (substantially similar for PL2 and PL3).

O. Claim 16: “The method of configuring a look up table as claimed in claim 13, wherein an input signal input to at least one of said LUT units and an output signal output from said LUT units are selectively controlled in accordance with a predetermined function of the input signal.”¹⁴

Fujii-Betz renders obvious this limitation. Melvin, ¶¶184-186; *see also supra* [3C] (substantially similar for PL2 and PL3). As discussed above ([14]-

¹⁴ As corrected by the April 26, 2005, Certificate of Correction. *See* ’737-patent (last page).

[15]), Fujii-Betz teaches that “*an input signal input to at least one of said LUT units and an output signal output from said LUT units are selectively controlled*” by selectors that are controlled by control signals A and B. As noted ([3C]), output selectors x12 and x14 are controlled in accordance with input signals c and d in selecting between output signals. Fujii ¶¶18-19, 29-30, 39, 42, FIG.3. As discussed above ([3C]), it would have been obvious to modify PL1 to use one or more of input signals a-g (e.g., c or d) to control at least one of input selectors x16-x20. By so doing, “*an input signal input to at least one of said LUT units and an output signal output from said LUT units are selectively controlled*” by one of input signals a-g.

Alternatively, as explained ([3C]), control signals A and B are each an “*input signal*.”

Additionally, a POSA would have understood that one type of “*predetermined function of the input signal*” is the identity function. See Apostol, 50-51 (“Suppose that $f(x) = x$ for all real x . This function is often called the *identity function*.”); Tanenbaum, 66, FIG.3-6 (illustrating the “*Identity law*,” including well-known functions “ $1A = A$ ” and “ $0 + A = A$ ”); Melvin, ¶186.

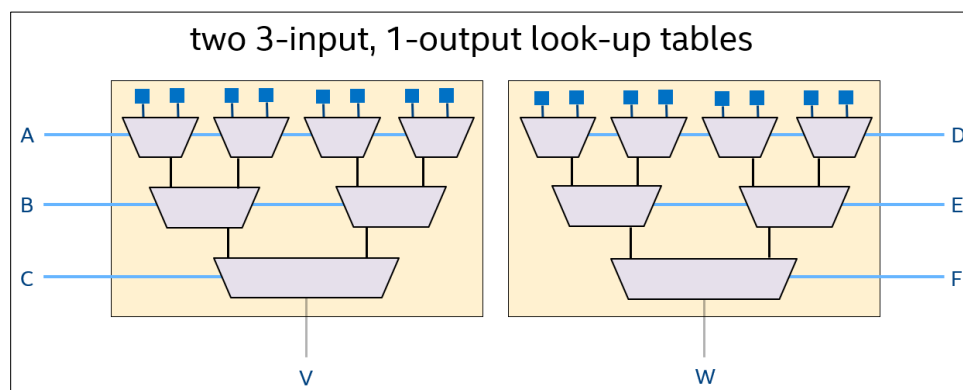
IX. GROUND 2

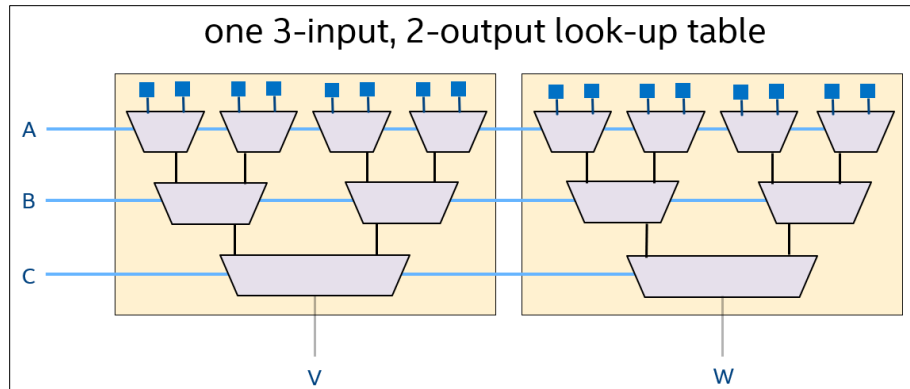
Fujii in combination with Betz and the general knowledge of a POSA renders obvious claims 6 and 12. Melvin, ¶187.

A. Claim 6: “The look up table as claimed in claim 4, wherein said 6-input 3-output look up table comprises four 3-input 2-output LUT units.”

As described above, Fujii-Betz renders obvious “[t]he look up table as claimed in claim 4.” Claim 6’s additional limitations would have been obvious in light of Fujii and the general knowledge of a POSA as of the effective filing date of the ’737 patent. *See Koninklijke Philips N.V. v. Google LLC*, 948 F.3d 1330, 1337 (Fed. Cir. 2020) (holding general knowledge can be used “when determining whether it would have been obvious to modify the prior art.”). In particular, it would have been obvious to modify the 6-input, 3-output PL1 with eight 3-input, 1-output “*LUT units*” discussed above ([5]) to comprise “*four 3-input 2-output LUT units*.” Melvin, ¶¶188-193.

As of the effective filing date, it would have been well understood by a POSA, as a matter of logic, that a 3-input, 2-output “*LUT unit*” can be made of two 3-input, 1-output “*LUT units*” with common inputs:





Melvin, ¶¶189-190. It was well known that “that the memory cells” used to construct look-up tables “are restructurable (by means of programmable switches), so that LUTs with varying number of inputs can be implemented.” Bhat, 35. “If there are 32 [2^5] memory cells,” for example, “these can be structured as a 5-input, 1-output LUT, or a **4-input, 2-output LUT**, or a 3-input, 4-output LUT, and so on. Additionally, **two 4-input, 1-output LUTs** (with no common inputs) and four 3-input, 1-output LUTs, and so on, are possible.” Bhat, 35. In the same way, sixteen memory bits can be structured as two 3-input, 1-output lookup tables or one 3-input, 2-output look-up table that can implement an arbitrary logic circuit of its inputs on both of its outputs independently.

A skilled artisan would have been motivated to modify the Fujii-Betz PL1 (*see supra* [1D], [5]) in this way because it would have involved a simple substitution (four 3-input, 2-output “*LUT units*” instead of eight 3-input, 1-output “*LUT units*”) of known elements (configurations of 16 memory cells) to obtain predictable results (a “*LUT unit*” that can perform an arbitrary function of three

inputs on each of its two outputs). Moreover, a POSA would have been motivated to implement the 6-input, 3-output look-up table in PL1 with “*four 3-input 2-output LUT units*” in order to “efficiently implement[]” the “small fanin functions” known to be used by “many logic circuits.” He, 3. In particular, there are a limited set of look-up tables that can efficiently perform small fanin functions—namely “2 or 3-input LUTs” (He, 3), and a POSA would have been motivated to use “*3-input, 2-output LUT units*.” It was well known that 3-input look-up tables could be designed to have more than one output. Brown-FPGA, 99. Thus, “*3-input, 2-output LUT units*” would have been among the limited set of small look-up tables capable of implementing small fanin functions efficiently. It would have been obvious to try all of those small look-up tables to optimize the speed and area of the modified logic element. See He, 1-4 (optimization study); Melvin, ¶191.

A POSA would have had a reasonable expectation of success in making this modification. Melvin, ¶192. As discussed ([5]), a POSA would have had a reasonable expectation of success in modifying the 6-input, 3-output PL1 to comprise “*eight 3-input 1-output LUT units*.” As discussed above (*supra* p.78), a POSA would have also understood that a 3-input, 2-output look-up table comprises two 3-input, 1-output look-up tables with common inputs. Melvin, ¶¶189-190. Methods of common inputs between look-up tables were well known and could be accomplished in many routine ways, e.g., a pre-look-up-table decoding section or

B. Claim 12: “The programmable logic circuit device as claimed in claim 10, wherein said 6-input 3-output look up table comprises four 3-input 2-output LUT units.”

Fujii-Betz renders obvious “[t]he programmable logic circuit device as claimed in claim 10.” *See supra* [7PRE]-[7J], [10]. Claim 12’s additional limitations are substantially similar to those in claim 6 and would have been obvious in light of Fujii and the general knowledge of a POSA. *See supra* [6].

X. GROUND 3 AND GROUND 4

To the extent the phrase “a memory” in the challenged claims (*see* [1D] and [7J]) requires a single memory, Fujii in combination with Betz and Chow (Ground 3) and Fujii in combination with Betz, the general knowledge of a POSA, and Chow (Ground 4) render those claims obvious. Melvin, ¶¶195-198. For the reasons discussed above, Fujii in combination with Betz renders obvious all other limitations in claims 1-5 7-11, and 13-16, *see supra* §VIII, and Fujii in combination with Betz and the general knowledge of a POSA renders obvious all other limitations in claims 6 and 12, *see supra* §IX.

Chow discloses a single memory to program multiple configuration bits together in an SRAM-based FPGA. Chow, 325 (“Three techniques for programming the configuration bits were identified. The simplest is to connect all of the bits into a long shift register.”); *see also* Chow, Abstract; Melvin, ¶196.

A POSA would have been motivated to control the SRAM-based switches taught by Betz using data stored in a single memory within PL1 as disclosed in Chow, because doing so would have made it easier to program and re-program the values of control signals A and B in Fujii's PL1 when programming the logic element PL1 by a user with the desired logic circuit, including setting the desired use mode. *See* Chow, 325-26 & FIG.12 (describing as the "simplest" method of programming configuration bits in an SRAM-based FPGA "connect[ing] all of the bits into a long shift register"); *see also* Sharpe-Geisler, 3:16-27, 3:40-54, 4:56-5:29, FIG.6 (describing how multiple pass gates are "controlled from a single memory cell bit 606"); *see also* Brown-FPGA, 1-4 (explaining that memories in programmable devices "can be erased and re-programmed many times"); Fujii, ¶¶1, 2, 38; Betz, 11-12 (SRAM cells used to "configure the programmable...logic blocks"). This combination also would have merely amounted to use of a known technique (programming a shift register with configuration bits) to improve a similar device (Fujii-Betz PL1) in the same way (implementing the simplest technique to program the configuration bits). Melvin, ¶197.

A POSA would have had a reasonable expectation of success in making this combination. Chow describes "connect[ing] all of the bits into a long shift register" as the "simplest" method of programming configuration bits in an SRAM-based

FPGA, so a POSA would have expected success in using the simplest method available. Melvin, ¶198.

XI. THE BOARD SHOULD INSTITUTE IPR

A. The Board Should Not Deny Institution Under §325

Non-institution under §325(d) would be improper. The Office has not considered the prior art and grounds in this Petition, which are materially different from and not cumulative of what was considered. Moreover, this is Petitioner's first petition directed to any claims of the '737 patent.

B. The Board Should Not Deny Institution Under *Fintiv*

The *Fintiv* factors support institution. ***First***, the District Court Case has been stayed since March 14, 2023, pending a decision on Petitioner's motion to transfer venue. Ex.1042. Petitioner intends to move to extend the stay (or for a new stay) no later than institution and before trial in the District Court Case. While the Board does not infer how the district court would rule on a request to stay pending IPR, the soon-pending motion increases the likelihood of a stay. *Hulu, LLC v. SITO Mobile R&D IP, LLC*, IPR2021-00298, Paper 11 at 10-11 (May 19, 2021).

Second, this Petition is filed in April 2023, so any final written decision (FWD) must issue by October 2024. While trial in the District Court Case is set for April 2024 (Ex.1039), given the current stay, it would be unreasonably speculative to assume the district court trial will occur then. Moreover, the Guidance Memo

requires consideration of median time-to-trial, which in the Western District of Texas is 29.5 months (Ex.1038, 37). The District Court Case was filed on June 24, 2022, resulting in an expected trial date (December 2024) that falls after the FWD deadline. Moreover, if the district court proceedings are transferred or the stay extended, that would increase the time-to-trial.

Third, minimal investment has been made in the district court toward assessing the '737 patent. By the time of institution (October 2023), even assuming the court reinstitutes its previous scheduling order (an unreasonable assumption), fact discovery will still be open and no summary judgment motions will have been filed. Ex.1039. The pending stay will only delay progress in district court.

Fourth, “there is a reasonable likelihood that the Board will address the overlapping validity issues prior to the district court reaching them at trial..., thereby providing the possibility of simplifying issues for trial.” *Juniper Networks, Inc. v. Packet Intelligence LLC*, IPR2020-00339, Paper 21 at 18 (P.T.A.B. Sept. 10, 2020).

Fifth, the Board should give little weight to Petitioner’s status as a defendant in the District Court Case. *See Weatherford U.S., L.P., v. Enventure Global Tech., Inc.*, IPR2020-01684, Paper 16 at 11-13 (P.T.A.B. April 14, 2021).

Sixth, “other circumstances” weigh against discretionary denial. This Petition establishes “a compelling unpatentability challenge,” which “alone

demonstrates that the Board should not discretionarily deny institution under *Fintiv*.” Ex.1037, 4-5; *see also Commscope Techs. LLC, v. Dali Wireless, Inc.*, No. IPR2022-01242, Paper 23 at 3-4 (P.T.A.B. Feb. 27, 2023). The evidence in support of this petition is substantial. As just one example of Petitioner’s compelling evidence of the ’737 patent’s unpatentability, Petitioner has shown that Fujii and the ’737 patent address the same problem in the same way, by allowing a single programmable logic element to implement multiple small functions and leave less memory unused. *See* Fujii ¶¶10-11; ’737-patent, 1:59-63. Fujii in combination with Betz discloses all the limitations of claims 1-5, 7-11, 13-16, and Fujii in combination with Betz and the general knowledge of a POSA discloses the remaining limitations in claims 6 and 12. *See* Grounds 1-2. This evidence, “if unrebutted in trial, would plainly lead to a conclusion that one or more claims are unpatentable,” so the Board must decline to exercise its discretion under §314(a). Guidance Memo, 4; *PopSockets LLC v. Flygrip, Inc.*, IPR2022-00938, Paper 8 (P.T.A.B. Nov. 1, 2022).

XII. CONCLUSION

The Board should institute review and cancel claims 1-16 of the '737 patent.

Dated: April 20, 2023

Respectfully submitted,

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Counsel for Petitioner

XIII. APPENDIX: CLAIM LISTING

The following claim listing assigns element labels (e.g., [1PRE], [1A], etc.) to certain claims for convenience of reference.

CLAIM 1
[1PRE] A look up table of M inputs and N outputs, comprising:
[1A] a plurality of LUT units; and
[1B] an internal configuration control circuit controlling an internal configuration of said plurality of LUT units,
[1C] wherein said internal configuration control circuit comprises a plurality of selectors selecting I/O signals of said plurality of LUT units, and
[1D] a selector control circuit having a memory, controlling said plurality of selectors in accordance with data stored in said memory, and defining the internal configuration of said plurality of LUT units.
CLAIM 2
[2A] “The look up table as claimed in claim 1, wherein said plurality of selectors include: an input signal selector provided at an input of at least one of said LUT units to select an input signal; and”
[2B] “an output signal selector provided at an output of said LUT units selecting an output signal,”
[2C] “said input signal selector and said output signal selector being controlled in accordance with the data stored in said memory.”
CLAIM 3
[3A] The look up table as claimed in claim 1, wherein said plurality of selectors include: an input signal selector provided at an input of at least one of said LUT units to select an input signal; and
[3B] an output signal selector provided at an output of said LUT units selecting an output signal,
[3C] said input signal selector and said output signal selector being controlled in accordance with the input signal.
CLAIM 4
[4] The look up table as claimed in claim 1, wherein said look up table of M inputs and N outputs is a 6-input 3-output look up table.
CLAIM 5
[5] The look up table as claimed in claim 4, wherein said 6-input 3-output look up table comprises eight 3-input 1-output LUT units.
CLAIM 6

[6] The look up table as claimed in claim 4, wherein said 6-input 3-output look up table comprises four 3-input 2-output LUT units.
CLAIM 7
[7PRE] A programmable logic circuit device comprising:
[7A] a plurality of logic blocks;
[7B] a plurality of routing wires connected to each of said logic blocks;
[7C] a plurality of switch circuits provided at an intersection of each of said routing wires;
[7D] a plurality of connection blocks provided between an I/O line of each of said logic blocks and each of said routing wires; and
[7E] an I/O block performing an input/output operation with external equipment,
[7F] wherein each of said logic blocks has a look up table of M inputs and N outputs, comprising:
[7G] a plurality of LUT units; and
[7H] an internal configuration control circuit controlling an internal configuration of said plurality of LUT units,
[7I] wherein said internal configuration control circuit comprises a plurality of selectors selecting I/O signals of said plurality of LUT units, and
[7J] a selector control circuit having a memory, controlling said plurality of selectors in accordance with data stored in said memory, and defining the internal configuration of said plurality of LUT units.
CLAIM 8
[8A] The programmable logic circuit device as claimed in claim 7, wherein said plurality of selectors include: an input signal selector provided at an input of at least one of said LUT units to select an input signal; and
[8B] an output signal selector provided at an output of said LUT units selecting an output signal,
[8C] said input signal selector and said output signal selector being controlled in accordance with the data stored in said memory.
CLAIM 9
[9A] The programmable logic circuit device as claimed in claim 7, wherein said plurality of selectors include: an input signal selector provided at an input of at least one of said LUT units to select an input signal; and
[9B] an output signal selector provided at an output of said LUT units selecting an output signal,
[9C] said input signal selector and said output signal selector being controlled in accordance with the input signal.
CLAIM 10

[10] The programmable logic circuit device as claimed in claim 7, wherein said look up table of M inputs and N outputs is a 6-input 3-output look up table.
CLAIM 11
[11] The programmable logic circuit device as claimed in claim 10, wherein said 6-input 3-output look up table comprises eight 3-input 1-output LUT units.
CLAIM 12
[12] The programmable logic circuit device as claimed in claim 10, wherein said 6-input 3-output look up table comprises four 3-input 2-output LUT units.
CLAIM 13
[13PRE] A method of configuring a look up table of M inputs and N outputs, comprising:
[13A] providing a plurality of LUT units, and
[13B] selectively controlling I/O signals of said plurality of LUT units to set a predetermined mode of an internal configuration.
CLAIM 14
[14] The method of configuring a look up table as claimed in claim 13, wherein the I/O signals of said plurality of LUT units are selectively controlled in accordance with data stored in the corresponding look up table.
CLAIM 15
[15] The method of configuring a look up table as claimed in claim 13, wherein an input signal input to at least one of said LUT units and an output signal output from said LUT units ¹⁵ are selectively controlled in accordance with data stored in the corresponding look up table.
CLAIM 16
[16] The method of configuring a look up table as claimed in claim 13, wherein an input signal input to at least one of said LUT units and an output signal output from said LUT units ¹⁶ are selectively controlled in accordance with a predetermined function of the input signal.

¹⁵ As corrected by the Certificate of Correction entered April 26, 2005.

¹⁶ As corrected by the Certificate of Correction entered April 26, 2005.

CERTIFICATE OF SERVICE ON PATENT OWNER
UNDER 37 C.F.R. §42.105

I hereby certify that on April 20, 2023, I caused a true and correct copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 6,812,737 and supporting exhibits to be served via Federal Express Next Day Delivery on the Patent Owner at the following correspondence address of record as listed on the USPTO Patent Center:

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CERTIFICATION OF WORD COUNT

Pursuant to 37 C.F.R. §42.24(d), the undersigned certifies that the foregoing Petition for *Inter Partes* Review contains 13,935 words excluding a table of contents, a table of authorities, Mandatory Notices under §42.8, a certificate of service or word count, or appendix of exhibits or claim listing, but including annotations added to figures. Petition has relied on the word count feature of the word processing system used to create this paper in making this certification, manually adding to that the number of words present in annotations to figures.

Dated: April 20, 2023

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