

UTILITY PATENT APPLICATION

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First Named Inventor or Application Identifier:
Toshinori SUEYOSHI, et al.

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APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

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1. ☒ Fee Transmittal Form
2. ☒ Specification, Claims & Abstract[Total Pages: 22]
3. ☒ Drawing(s) (35 USC 113)[Total Sheets: 14] [FIGS. 1-15]
4. ☒ Oath or Declaration[Total Pages: 3]
 - a. ☒ Newly executed (original or copy)
 - b. ☐ Copy from a prior application (37 CFR 1.63(d))
 - i. ☐ DELETION OF INVENTOR(S)
Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
5. ☐ Verified Statement Claiming Small Entity Status
6. ☐ Application Data Sheet. See 37 C.F.R. 1.76
7. ☒ Applicant claims foreign priority benefit to: Japanese Application 2001-199644 filed June 29, 2001
8. ☐ CD-Rom or CD-R in duplicate, large table or Computer Program (Appendix)
9. ☐ Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)
 - a. ☐ Computer Readable Form (CRF)
 - b. ☐ Specification Sequence Listing on:
 - i. ☐ CD-ROM or CD-R (2 copies); or
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 - c. ☐ Statement verifying identity of above copies
10. ☐ For publication of assignee information under 37 CFR 1.215(b), list the assignee as . The Assignment papers will be filed later.

ACCOMPANYING APPLICATION PARTS

11. ☒ Assignment (cover sheet & document(s)) to SEMICONDUCTOR TECHNOLOGY ACADEMIC RESEARCH CENTER of Yokohama, Japan
 - ☒ for publication of assignee information under 37 CFR 1.215(b)
12. ☐ 37 CFR 3.73(b) Statement (when there is an assignee) ☐ Power of Attorney
13. ☐ English Translation Document (if applicable)
14. ☒ Information Disclosure Statement (IDS)/PTO-1449 ☒ Copies of IDS Citations
15. ☐ Preliminary Amendment
16. ☒ Return Receipt Postcard (MPEP 503) (Should be specifically itemized)
17. ☒ Certified Copy of Priority Document(s) (if foreign priority is claimed)
18. ☐ Request and Certification for Nonpublication under 35 U.S.C. 122(b)(2)(B)(i). Applicant must attach form PTO/SB/35 or its equivalent
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FEE CALCULATION (fees effective 10/01/01)

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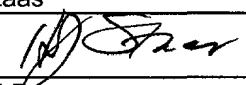
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PROGRAMMABLE LOGIC CIRCUIT DEVICE HAVING LOOK UP TABLE
ENABLING TO REDUCE IMPLEMENTATION AREA

5 BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to an architectural technology for configuring a look up table that enables implementation area to be reduced.

10 2. Description of the Related Art

Recently, a programmable logic circuit device has attracted much attention as a device that can realize various logic circuits which meets diverse needs of users by programming internal circuits. Such a programmable logic circuit device is known as PLD (Programmable Logic Device) or FPGA (Field Programmable Gate Array), and recently is increasingly used not only for trial fabrication of hardwares, but also for constructing a large scale circuit (for example, a microprocessor) that has various functions in itself. These programmable logic circuits comprise look up tables (LUT: Look Up Table) as major components, and reduction of circuit area of such LUTs is strongly desired.

A look up table (LUT) as a major component of a programmable logic circuit device (PLD or FPGA) is composed of memories, and is capable of implementing an arbitrary logic circuit. Basic architecture of such a FPGA has been previously disclosed, for example, in U.S. Patent No. 4,706,216, and U.S. Patent No. 4,870,302. Multi-context and cluster architecture of plural LUTs in FPGA has been disclosed, for example, in U.S. Patent No. 5,778,439 and U.S. Patent No. 5,905,385, etc. With regard to evaluation of LUT used in FPGA (for example, evaluation of functionality and area, as well as performance evaluation, and evaluation of cluster architecture), study results are found in, for example, J. Rose et al., "Architecture of Field Programmable Gate

Arrays: The Effect of Logic Block Functionality on Area Efficiency", IEEE J. Solid State Circuits, vol. 25, no. 5, pp. 1217 - 1225, Oct. 1990, J. Rose et al., "The Effect of Logic Block Architecture on FPGA Performance", IEEE J. Solid State Circuits, vol. 27, no. 3, pp. 281-287, Mar. 1992, and E. Ahmed et al., "The Effect of LUT and Cluster Size on Deep Sub-micron FPGA Performance and Density", FPGA 2000, Monterey, CA USA, 2000.

In a programmable logic circuit device, the number of bits M of input signal for the logic circuit that can be implemented corresponds to the number of bits of the address of memory composing the LUT, and the number of bits N of output signal corresponds to the number of output bits of the memory. Thus, a logic circuit that can be implemented in one LUT is an arbitrary logic circuit of M inputs and N outputs. Such a LUT is denoted in the present specification as M-input N-output LUT.

Conventionally, in FPGA for example, the input number M and output number N are both fixed value. Any logic circuit is divided in circuit unit of M inputs and N outputs, and is implemented using plural LUTs.

Therefore, in a conventional FPGA, even if circuit division results in a circuit having input bit number less than M, one LUT needs to be assigned to this circuit, leading to unnecessary increase of implementation area (logic and routing circuitry area; circuit area).

SUMMARY OF THE INVENTION

An object of the present invention is to reduce the circuit area of a look up table (LUT) and hence of a programmable logic circuit device. Another object of the present invention is to reduce power consumption of a programmable logic circuit device.

According to the present invention, there is provided a look up table of M inputs and N outputs, comprising a plurality of LUT units; and an internal

configuration control circuit controlling an internal configuration of the plurality of LUT units.

Further, according to the present invention, there is provided a programmable logic circuit device

5 comprising a plurality of logic blocks; a plurality of routing wires connected to each of the logic blocks; a plurality of switch circuits provided at an intersection of each of the routing wires; a plurality of connection blocks provided between an I/O line of each of the logic

10 blocks and each of the routing wires; and an I/O block performing an input/output operation with external equipment, wherein each of the logic blocks has a look up table of M inputs and N outputs, comprising a plurality of LUT units; and an internal configuration control

15 circuit controlling an internal configuration of the plurality of LUT units.

The internal configuration control circuit may comprise a plurality of selectors selecting I/O signals of the plurality of LUT units; and a selector control

20 circuit controlling the selectors and defining the internal configuration of the plurality of LUT units. The selector control circuit may comprise a memory, and control the plurality of selectors in accordance with data stored in the memory.

The plurality of selectors may include an input signal selector provided at an input of at least one of the LUT units to select an input signal; and an output signal selector provided at an output of the LUT units selecting an output signal, the input signal selector and

25 the output signal selector being controlled in accordance with the data stored in the memory. The plurality of selectors may include an input signal selector provided at an input of at least one of the LUT units to select an input signal; and an output signal selector provided at

30 an output of the LUT units selecting an output signal, the input signal selector and the output signal selector being controlled in accordance with the input signal.

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The look up table of M inputs and N outputs may be a 6-input 3-output look up table. The 6-input 3-output look up table may comprise eight 3-input 1-output LUT units. The 6-input 3-output look up table may comprise
5 four 3-input 2-output LUT units.

In addition, according to the present invention, there is also provided a method of configuring a look up table of M inputs and N outputs, comprising the steps of providing a plurality of LUT units; and selectively
10 controlling I/O signals of the plurality of LUT units to set a predetermined mode of an internal configuration.

The I/O signals of the plurality of LUT units may be selectively controlled in accordance with data stored in the corresponding look up table. An input signal input
15 to at least one of the LUT units and an output signal output from the LUT unit may be selectively controlled in accordance with data stored in the corresponding look up table. An input signal input to at least one of the LUT units and an output signal output from the LUT unit may
20 be selectively controlled in accordance with a predetermined function of the input signal.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be more clearly understood from the description of the preferred
25 embodiments as set forth below with reference to the accompanying drawings, wherein:

Fig. 1 is a block diagram showing an example of FPGA to which the present invention is applied;

Fig. 2 is a block diagram showing a 6-input 3-output LUT as an example of LUTs in the FPGA;
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Figs. 3A, 3B, 3C, 3D, 3E, and 3F are block diagrams showing the mode of internal configuration of the 6-input 3-output LUT shown in Fig. 2;

Fig. 4 is a view useful for explaining an example of
35 the method of mapping circuits in a look up table;

Fig. 5 is a block diagram showing a 6-input 3-output LUT as an example of a LUT in FPGA according to the

present invention in conjunction with input/output signal;

Fig. 6 is a block diagram showing an example of the internal configuration of the 6-input 3-output LUT shown in Fig. 5;

Fig. 7 is a block diagram showing an example of 3-input 1-output LUT unit in the 6-input 3-output LUT of Fig. 6;

Fig. 8 is a block diagram showing another example of 3-input 1-output LUT unit in the 6-input 3-output LUT of Fig. 6;

Fig. 9 is a block diagram showing another example of the internal configuration of the 6-input 3-output LUT shown in Fig. 5;

Fig. 10 is a block diagram showing an example of 3-input 2-output LUT unit in the 6-input 3-output LUT of Fig. 9;

Fig. 11 is a block diagram showing another example of 3-input 2-output LUT unit in the 6-input 3-output LUT of Fig. 9;

Fig. 12 is a block diagram showing still another example of 3-input 2-output LUT unit in the 6-input 3-output LUT of Fig. 9;

Fig. 13 is a block diagram showing an example of configuration of a 8 operation ALU circuit (ALU 16);

Fig. 14 is a view showing difference of the area ratio for ALU 16 shown in Fig. 13 when implemented with LUT in conventional FPGA compared to LUT in FPGA according to the present invention; and

Fig. 15 is a view showing difference of the number of bits of configuration data for ALU 16 shown in Fig. 13 when implemented with LUT in conventional FPGA compared to LUT in FPGA according to the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Now, a look up table, a programmable logic circuit device comprising a look up table and a method for configuring a look up table according to the present

invention will be described in detail below with reference to appended drawings.

Fig. 1 is a block diagram showing an example of FPGA to which the present invention is applied. In Fig. 1, reference numeral 100 denotes FPGA as an example of a programmable logic circuit device, 101 is an I/O block, 102 is a logic block (CLB: Configurable Logic Block), 103 is a connection block (C), 104 is a switch matrix (S), and 105 denotes routing wires.

As shown in Fig. 1, FPGA 100 is comprised of logic blocks (CLB) 102 arranged in the form of array, routing wire (channel area) 105 surrounding these CLB 102, and I/O blocks 101. At the intersection of the routing wire 105, switch matrices (S) 104 are disposed for connecting these components, and connection block (C) 103 is disposed between the I/O line of each CLB 102 and the routing wire 105. Each CLB 102 is comprised of a look up table (LUT) 121, latches 122, and selectors 123. The present invention relates mainly to the configuration of LUT 121.

Fig. 2 is a block diagram showing a 6-input 3-output LUT as an example of a LUT in a FPGA. This is an example of a LUT 121 in Fig. 1. Thus, the LUT shown in Fig. 2 corresponds to the configuration of a case of M-input N-output LUT in which $M = 6$, $N = 3$. The case of $M = 6$, $N = 3$ is only an example, and value of M and N is not limited to this case, but may include various other values, and may include the case $M = N$, or $M < N$.

Figs. 3A to 3F are block diagrams showing different modes of internal configuration of the 6-input 3-output LUT shown in Fig. 2, and showing that, as will be described in detail later, by varying the values (X, Y, Z) of mode changing memory (71), the 6-input 3-output LUT can be set to different internal configurations as shown in Figs. 3A to 3F.

Specifically, Fig. 3A shows a case where the 6-input 3-output LUT is set to a mode of three 2-input 1-output

LUT. In conventional FPGA (conventionally composed by using 4-input 1-output LUT as a unit), for example, three LUTs (4-input 1-output LUT) are required to assign three 2-input 1-output circuits to LUTs. In the configuration shown in Fig. 3A, only one 6-input 3-output LUT needs to be used for this purpose.

Area ratio of 4-input 1-output LUT to 6-input 3-output LUT including routing channel area is about 1 : 1.5. Therefore, as compared to the conventional configuration using three 4-input 1-output LUTs, the configuration shown in Fig. 3A can reduce the circuit area ratio to about $(1 \times 3) : 1.5$, that is, to about 1 : 0.5. Thus, reduction of circuit area of maximum 50% can be achieved.

Fig. 3B shows a case where the LUT is set to a mode of two 3 input 1 output LUTs. In this case, as compared to the conventional configuration where two 4-input 1-output LUTs are used, the circuit area ratio can be reduced to $(1 \times 2) : 1.5$, that is, 1 : 0.75. Thus, reduction of circuit area of maximum 25% can be achieved.

Further, Fig. 3C shows a case where the 6-input 3-output LUT is set to a mode of 6-input 1-output LUT.

Fig. 3D shows a case where the 6-input 3-output LUT is set to a mode of 3-input 1-output LUT $\times$ 8 planes.

Fig. 3E shows a case where the 6-input 3-output LUT is set to a mode of 4-input 1-output LUT $\times$ 4 planes, and Fig. 3F shows a case where the 6-input 3-output LUT is set to a mode of 5-input 1-output LUT $\times$ 2 planes.

Fig. 4 is a view useful for explaining the mapping method of circuits in the look up table, which shows the reason why mode setting of Figs. 3D to 3F above is possible.

As shown in Fig. 4, in the mapping method which utilizes, for example, the control structure of if ~, else, case, etc., in RTL (Register Transfer Level)

description of HDL (Hardware Description Language), since it is guaranteed that conditional branching is not explicitly simultaneous operation, processing within each condition is mapped to each context. Switching between contexts is performed, for example, by a signal from a control circuit implemented in other LUT (look up table).

In such a case, as shown in above described Figs. 3D to 3F, plural LUTs can be configured with one LUT. Specifically, in the case shown in Fig. 3D, eight 3-input 1-output LUTs can be configured with one LUT (in Fig. 3D, one 6-input 3-output LUT). In the case shown in Fig. 3E, four 4-input 1-output LUTs can be configured with one LUT, and in the case shown in Fig. 3F, two 5-input 1-output LUTs can be configured with one LUT.

Specifically, in the configuration shown in Fig. 3E, for example, as compared to conventional configuration using four 4-input 1-output LUTs, the circuit area ratio can be reduced to about $(1 \times 4) : 1.5$, that is, 1 : 0.375. Thus, reduction of implementation area (circuit area) of maximum about 62% can be achieved. In other words, the LUTs shown in Fig. 3E (LUTs configured with one 6-input 3-output LUT) can be configured in implementation area of about 32% of conventional LUTs (four 4-input 1-output LUTs), and can also substantially decrease the power consumption.

Also, if the case where an ALU circuit of 8 operations is implemented with conventional 4-input 1-output LUTs, is compared with the case where the 6-input 3-output LUT is used as 4-input 1-output LUT $\times$ 4 planes for implementing same ALU circuit, circuit area can be reduced to about 75%, and achieve considerable improvement in packaging efficiency.

Fig. 5 is a block diagram showing a 6-input 3-output LUT 7 as an example of LUT in FPGA according to the present invention in conjunction with the I/O signals. This corresponds to the 6-input 3-output LUT as shown in

Fig. 2 with six input signals A, B, C, D, E, F and three output signals Q, V, W added thereto.

Fig. 6 is a block diagram showing an example of internal configuration of the 6-input 3-output LUT shown in Fig. 5.

As shown in Fig. 6, the 6-input 3-output LUT 7 (121) is comprised of a mode changing memory 71, selectors 721 ~ 726, and 3-input 1-output LUT units (memory array) 731 ~ 738. The mode changing memory 71 stores 3 bits data X, Y, Z designated by a user so as to set the relation between 6 bit input A ~ F and 3 bit output Q, V, W in accordance with user's request.

A predetermined signal within 6 bit input signal is input to each selector (selector for selecting input signal) 721 ~ 725, so as to select input signal in accordance with data stored in the mode changing memory 71. That is, signals A, C are input to the selector 721, and signals B, D are input to selector 722, and one of the signals is selected by selection signal F0 (X, Y, Z) specified by data X, Y, Z, and is output, respectively. Similarly, signals A, D are input to the selector 723, and signals B, E are input to the selector 724, and signals C, F are input to the selector 725, and one of the signals is selected by selection signal F1 (X, Y, Z) specified by data X, Y, Z, and is output, respectively.

Each of 3-input 1-output LUT units 731 ~ 738 is comprised of an address decoder, a memory and a selector, as described later, and outputs 1 bit signal in response to 3 bit input signal, respectively. Thus, signals A, B, C are input to each of LUT units 731, 732, 734 ~ 736 and 738, and one of the signals A or C and one of the signals B or D selected by selection signal F0, and the signal C is input to the LUT unit 733, and one of the signals A or D, and one of the signals B or E, and one of the signals C or F, selected by the selection signal F1 is input to

the LUT unit 737. Output signals from the LUT units 731 ~ 738 are input to a selector (selector for selecting output signal) 726, and one of the signals is selected by selection signal F2 (D, E, F, X, Y, Z) specified by signals D, E, F and data X, Y, Z, and is output as signal V. The signal Q is the output signal from the LUT unit 731, and the signal W is the output signal from the LUT unit 737.

Fig. 7 is a block diagram showing an example of 3-input 1-output LUT unit 731 in the 6-input 3-output LUT 7 of Fig. 6. All of the 3-input 1-output LUT units 731 ~ 738 are of similar configuration.

The LUT unit 731 shown in Fig. 7 is comprised of an address decoder 7311, a selector 7312, and two sets of 4 bit memory unit groups M11 ~ M14, M21 ~ M24. The address decoder 7311 decodes 2 bit input signal A, B to designate each one of the memory unit groups M11 ~ M14 and M21 ~ M24, and further according to the input signal C, selects one of the sets M11 ~ M14 or M21 ~ M24 to output data.

Fig. 8 is a block diagram showing another example of 3-input 1-output LUT unit 731 in the 6-input 3-output LUT 7 of Fig. 6.

The LUT unit 731 shown in Fig. 8 is comprised of an address decoder 7313, and 8 bit memory unit groups M31 ~ M38. The address decoder 7313 decodes the 3 bit input signals A, B, C, to designate one of the memory unit groups M31 ~ M38, and output the data (Q).

The relation of the 3 bit data X, Y, Z, designated by the mode changing memory 71 in the 6-input 3-output LUT shown in Fig 6 as described above and the corresponding internal configurations (configuration modes) will be explained below with reference to Figs. 3A ~ 3F.

First, when, as shown in Fig. 3A, the 6-input 3-output LUT 7 (121) is set to the mode of three 2-input 1-

output LUTs, the selection signal F0 and F1 select an input "1" at each of the selectors 721, 722 and 723 ~ 725, and further, the selection signal F2 selects an input "2" at the selector 726.

5 That is, the user designates the 3 bit data X, Y, Z to be stored in the mode changing memory 71 such that the selection signal F0 (X, Y, Z) and F1 (X, Y, Z) selects an input "1" at each of the selectors 721, 722 and 723 ~ 725, and that the selection signal F2 (D, E, F, X, Y, Z) selects an input "2" at the selector 726.

10 Thus, by using the LUT unit 731 to which signals A, B, C are input and which outputs signal Q, the LUT unit 733 to which the signals C, D via the selectors 721, 722 and the direct signal C are input and which outputs the signal V via the selector 726, and the LUT unit 737 to which the signals D, E, F are input via the selectors 723 ~ 725 and which outputs the signal W, the three 2-input 1-output LUTs as shown in Fig. 3A can be configured. Although the input signal C in the LUT unit 731, one of the input signal C in the LUT unit 733, and the input signal D in the LUT unit 737 via the selector 723 are extra input signals in each of the LUT units, there is no problem about it.

25 Next, when, as shown in Fig. 3B, the 6-input 3-output LUT 7 is set to the mode of two 3-input 1-output LUTs, the 3 bit data X, Y, Z to be stored in the mode changing memory 71 is designated such that the selection signal F1 selects an input signal "1" at the selectors 723 ~ 725. By using the LUT unit 731 to which the signals A, B, C are input and which outputs the signal Q, and the LUT unit 737 to which the signals D, E, F are input via the selector 723 ~ 725 and which outputs the signal W, the two 3-input 1-output LUTs as shown in Fig. 3B can be configured.

35 When, as shown in Fig. 3C, the 6-input 3-output LUT

is set to the mode of 6-input 1-output LUT, the selection signals F0 and F1 select an input "0" at each selector, and the selection signal F2 determines the value of the selector 726 from input signals D, E, F, and outputs the signal V. Thus, from 6 bit input of the signals A, B, C, and the signals D, E, F, 1 bit signal V is output.

As shown in Fig. 3D, when the 6-input 3-output LUT is set to the mode of 3-input 1-output LUT $\times$ 8 planes, the selection signals F0 and F1 select an input "0" at each selector, and the selection signal F2 determines the value of the selector 726 from the signals D, E, F, and outputs the signal V. In this case, the signals D, E, F, use plane switching signals.

As shown in Fig. 3E, when the 6-input 3-output LUT is set to the mode of 4-input 1-output LUT $\times$ 4 planes, the selection signals F0 and F1 select an input "0" at each selector, and the selection signal F2 determines the value of the selector 726 from the signals D, E, F, and outputs the signal V. In this case, the signal D is one of 4 bit input signals together with the signals A, B, C, and the signals E and F use plane switching signals.

As shown in Fig. 3F, when the 6-input 3-output LUT is set to the mode of 5-input 1-output LUT $\times$ 2 planes, the selection signals F0 and F1 select an input "0" at each selector, and the selection signal F2 determines the value of the selector 726 from the signals D, E, F, and outputs the signal V. In this case, the signal D and E are two of 5 bit input signals together with the signals A, B, C, and the signals F uses a plane switching signal.

As has been described above, according to the present embodiment, the 6-input 3-output LUT, for example, may be used in various modes of internal configuration by varying the values X, Y, Z of the mode changing memory.

Fig. 9 is a block diagram showing another example of internal configuration, which is different from the above

described internal configuration of 6-input 3-output LUT shown in Fig. 6.

As shown in Fig. 9, the 6-input 3-output LUT 8 (121) is comprised of a mode changing memory 81, selectors 821 ~ 826, and 3-input 2-output LUT units 831 ~ 834. The mode changing memory 81 stores 3 bit data X, Y, Z, designated by a user, so as to set the relation between 6 bit input A ~ F and 3 bit output Q, V, W in accordance with user's request.

Thus, in contrast to the above described 6-input 3-output LUT 7 shown in Fig. 6, which comprises eight 3-input 1-output LUT units 731 ~ 738, the present 6-input 3-output LUT 8 comprises four 3-input 2-output LUT units 831 ~ 834, and except for this, has substantially the same configuration.

3 bit data X, Y, Z, designated to the mode changing memory 81 of the LUT 8 shown in Fig. 9, selection signals F0 (X, Y, Z), F1 (X, Y, Z), and F2 (D, E, F, X, Y, Z), as well as the operation of selectors 821 ~ 826 (corresponding to the selectors 721 ~ 726) controlled by these selection signals F0, F1, F2, are the same as has been described with reference to Fig. 6 and Figs. 3A ~ 3F, and explanation thereof is therefore omitted.

Fig. 10 is a block diagram showing an example of 3-input 2-output LUT units in the 6-input 3-output LUT shown in Fig. 9. All of the 3-input 2-output LUT units 831 ~ 834 have the identical configuration.

The LUT unit 831 shown in Fig. 10 is comprised of an address decoder 8311, selectors 8312, 8313, and four sets of 4 bit memory unit group M41 ~ M44, M51 ~ M54, M61 ~ M64, M71 ~ M74. The address decoder 8311 decodes 2 bit input signal A, B to designate each one for the four sets of memory unit group M41 ~ M44, M51 ~ M54, M61 ~ M64, M71 ~ M74, and by the input signal C, selects and outputs the

data of one of the two sets of memory unit group M41 ~ M44 or M51 ~ M54 (output signal Q: the signal supplied to the input "0" of the selector 826), and data of one of the two sets of memory unit group M61 ~ M64 or M71 ~ M74 (the signal supplied to the input "1" of the selector 826).

Fig. 11 is a block diagram showing another example of 3-input 2-output LUT units in the 6-input 3-output LUT shown in Fig. 9.

The LUT unit 831 shown in Fig. 11 is comprised of an address decoder 8314, and two sets of 8 bit memory unit group M81 ~ M88 and M91 ~ M98. The address decoder 8314 decodes 3 bit input signal A, B, C to designate each one for the two sets of memory unit group M81 ~ M88 and M91 ~ M98, and outputs respective data (output signal Q: signal supplied to the input "0", and signal supplied to the input "1").

Fig. 12 is a block diagram showing still another example of 3-input 2-output LUT units in the 6-input 3-output LUT shown in Fig. 9.

The LUT unit 831 shown in Fig. 12 is comprised of an address decoder 8315, selectors 8316, 8317, and eight sets of 2 bit memory unit group M111, M121; M112, M122; ...; M118, M128. The address decoder 8315 decodes 1 bit input signal A to designate each one for the eight sets of memory unit group M111, M121 ~ M118, M128, and by 2 bit input signal B, C, selects and outputs the data of one set of the memory unit group M111, M121 ~ M114, M124 (output signal Q: the signal supplied to the input "0" of the selector 826), and the data of one set of the memory unit group M115, M125 ~ M118, M128 (signal supplied to the input "1" of the selector 826).

Fig. 13 is a block diagram showing an exemplary configuration of an ALU circuit (ALU 16) 90 of 8 operations. In Fig. 13, reference symbols G and H denote

16 bit data, I denotes command signal that determines the operation, and J denotes output signal.

As shown in Fig. 13, the ALU circuit 90 is comprised of eight operation circuits consisting of OR circuit 91, AND circuit 92, XOR circuit 93, not circuit 94, + (addition) circuit 95, NE (Not Equal) circuit 96, GT (Greater Than) circuit 97 and SHIFT circuit 98 having 16 bit data G and H input therein, respectively, and a selector 99 for selecting the output from the eight operation circuits 91 to 98 in accordance with the command signal I, and outputs the output signal J portion corresponding to the command signal I.

Cases where the ALU circuit (ALU 16) 90 shown in Fig. 13 is implemented with 3-input 1-output LUT to 7-input 1-output LUT as used in conventional FPGA (horizontal axis: 3 LUT ~ 7 LUT) is compared with cases where it is implemented with the 6-input 3-output LUT as shown in Fig. 6 (configuration comprising eight 3-input 1-output LUT 731 ~ 738, a mode changing memory 71 and selectors 721 ~ 726: 3 LUT * 8) and with the 6-input 3-output LUT as shown in Fig. 9 (configuration comprising four 3-input 2-output LUT 831 ~ 834, a mode changing memory 81 and selectors 821 ~ 826: 4 LUT * 4) as used in the FPGA according to the present invention, are compared in the following Figs. 14 and 15. The ALU 16 is equipped with, for example, a data selector for switching wire connection (a circuit which does not require LUT), a random logic (a circuit composed of LUT) and a flip-flop (a circuit for fixed portion of logic block). It is to be understood that the comparison in Figs. 14 and 15 is performed assuming that conditions other than the configuration of LUT are substantially the same.

Fig. 14 is a view showing the difference of the area ratio when the ALU 16 as shown in Fig. 13 is implemented with LUT used in conventional FPGA and in FPGA according

to the present invention (3 LUT ~ 7 LUT and 6-input 3-output LUT (3 LUT * 8 and 4 LUT * 4)). Fig. 15 is a view showing the difference of number of bits of configuration data when the ALU 16 as shown in Fig. 13 is implemented with LUT used in conventional FPGA and in FPGA according to the present invention. Vertical axis in Fig. 14 represents the area when the ALU 16 is configured using various LUTs, expressed as area ratio assuming the area of the case when configured with commonly used 4-input 1-output LUT (4 LUT) to be equal to 1. Vertical axis in Fig. 15 represents the number of bits of configuration data when the ALU 16 is configured using various LUTs.

As can be seen from Fig. 14, when the ALU 16 as shown in Fig. 13 is implemented with the 6-input 3-output LUT used in FPGA according to the present invention (3 LUT * 8 and 4 LUT * 4), for example, the area ratio is greatly reduced compared to the case where the same ALU 16 is implemented with LUT used in conventional FPGA (3 LUT ~ 7 LUT). More specifically, it can be seen that the case of 3 LUT * 8 where the 6-input 3-output LUT is implemented as 3-input 1-output LUT x 8 planes gives an area about 75% of that for the case where 4-input 1-output LUT (4 LUT) is used to implement the ALU 16 and gives the smallest area in conventional LUTs.

Further, as can be seen from Fig. 15, the number of bits of configuration data for the case where the ALU 16 is implemented with the 6-input 3-output LUT used in FPGA according to the present invention (3 LUT * 8 and 4 LUT * 4) is comparable to that for the case of 4 LUT that gives the smallest value among the conventional cases. Thus, although the 6-input 3-output LUT of the present invention requires 4 times as much configuration data as, for example, 4-input 1-output LUT, the number of bits of the configuration data can be made comparable. This is due to the fact that the conventional LUT constructs the selectors in output stage with LUTs while the present

invention achieves it by switching of routing wires so that number of LUTs used can be reduced.

In the above description, the 6-input 3-output LUT used in the FPGA according to the present invention is only an example, and the present invention can be equally applied to M-input N-output (e.g., 8-input 4-output) LUT. Further, it is to be understood that configuration of the 6-input 3-output LUT itself, for example, is not limited to the eight 3-input 1-output LUT units shown in Fig. 6, or to the four 3-input 2-output LUT units shown in Fig. 9, and various modification is possible within the scope of the invention.

As has been described above in detail, according to the present invention, the circuit area of a look up table (LUT) or a programmable logic circuit device can be reduced. Further, according to the present invention, the power consumption of a programmable logic circuit device can also be reduced.

Many different embodiments of the present invention may be constructed without departing from the spirit and scope of the present invention, and it should be understood that the present invention is not limited to the specific embodiments described in this specification, except as defined in the appended claims.

What is claimed is:

1. A look up table of M inputs and N outputs,
comprising:

5 a plurality of LUT units; and
an internal configuration control circuit
controlling an internal configuration of said plurality
of LUT units.

2. The look up table as claimed in claim 1,
wherein said internal configuration control circuit
10 comprises:

a plurality of selectors selecting I/O
signals of said plurality of LUT units; and
a selector control circuit controlling
said selectors and defining the internal configuration of
15 said plurality of LUT units.

3. The look up table as claimed in claim 2,
wherein said selector control circuit comprises a memory,
and controls said plurality of selectors in accordance
with data stored in said memory.

20 4. The look up table as claimed in claim 3,
wherein said plurality of selectors include:

an input signal selector provided at an
input of at least one of said LUT units to select an
input signal; and
25 an output signal selector provided at an
output of said LUT units selecting an output signal, said
input signal selector and said output signal selector
being controlled in accordance with the data stored in
said memory.

30 5. The look up table as claimed in claim 3,
wherein said plurality of selectors include:

an input signal selector provided at an
input of at least one of said LUT units to select an
input signal; and
35 an output signal selector provided at an
output of said LUT units selecting an output signal, said
input signal selector and said output signal selector

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being controlled in accordance with the input signal.

6. The look up table as claimed in claim 1, wherein said look up table of M inputs and N outputs is a 6-input 3-output look up table.

5 7. The look up table as claimed in claim 6, wherein said 6-input 3-output look up table comprises eight 3-input 1-output LUT units.

8. The look up table as claimed in claim 6, wherein said 6-input 3-output look up table comprises
10 four 3-input 2-output LUT units.

9. A programmable logic circuit device comprising:
a plurality of logic blocks;
a plurality of routing wires connected to
each of said logic blocks;
15 a plurality of switch circuits provided at an intersection of each of said routing wires;
a plurality of connection blocks provided between an I/O line of each of said logic blocks and each of said routing wires; and
20 an I/O block performing an input/output operation with external equipment, wherein each of said logic blocks has a look up table of M inputs and N outputs, comprising:
a plurality of LUT units; and
25 an internal configuration control circuit controlling an internal configuration of said plurality of LUT units.

10. The programmable logic circuit device as claimed in claim 9, wherein said internal configuration control circuit comprises:
30

a plurality of selectors selecting I/O signals of said plurality of LUT units; and
a selector control circuit controlling said selectors and defining the internal configuration of
35 said plurality of LUT units.

11. The programmable logic circuit device as claimed in claim 10, wherein said selector control

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circuit comprises a memory, and controls said plurality of selectors in accordance with data stored in said memory.

5 12. The programmable logic circuit device as claimed in claim 11, wherein said plurality of selectors include:

an input signal selector provided at an input of at least one of said LUT units to select an input signal; and

10 an output signal selector provided at an output of said LUT units selecting an output signal, said input signal selector and said output signal selector being controlled in accordance with the data stored in said memory.

15 13. The programmable logic circuit device as claimed in claim 11, wherein said plurality of selectors include:

an input signal selector provided at an input of at least one of said LUT units to select an input signal; and

20 an output signal selector provided at an output of said LUT units selecting an output signal, said input signal selector and said output signal selector being controlled in accordance with the input signal.

25 14. The programmable logic circuit device as claimed in claim 9, wherein said look up table of M inputs and N outputs is a 6-input 3-output look up table.

30 15. The programmable logic circuit device as claimed in claim 14, wherein said 6-input 3-output look up table comprises eight 3-input 1-output LUT units.

16. The programmable logic circuit device as claimed in claim 14, wherein said 6-input 3-output look up table comprises four 3-input 2-output LUT units.

35 17. A method of configuring a look up table of M inputs and N outputs, comprising the steps of:

providing a plurality of LUT units; and
selectively controlling I/O signals of

said plurality of LUT units to set a predetermined mode of an internal configuration.

18. The method of configuring a look up table as claimed in claim 17, wherein the I/O signals of said plurality of LUT units are selectively controlled in accordance with data stored in the corresponding look up table.

19. The method of configuring a look up table as claimed in claim 17, wherein an input signal input to at least one of said LUT units and an output signal output from said LUT unit are selectively controlled in accordance with data stored in the corresponding look up table.

20. The method of configuring a look up table as claimed in claim 17, wherein an input signal input to at least one of said LUT units and an output signal output from said LUT unit are selectively controlled in accordance with a predetermined function of the input signal.

PROGRAMMABLE LOGIC CIRCUIT DEVICE HAVING LOOK UP TABLE
ENABLING TO REDUCE IMPLEMENTATION AREA

5

ABSTRACT OF THE DISCLOSURE

10 A programmable logic circuit device has a plurality
of logic blocks, a plurality of routing wires, a
plurality of switch circuits, a plurality of connection
blocks, and an I/O block performing an input/output
operation with external equipment. The routing wires are
connected to each of the logic blocks, the switch
15 circuits are provided at an intersection of each of the
routing wires, and the connection blocks are provided
between an I/O line of each of the logic blocks and each
of the routing wires. Each of the logic blocks has a
look up table of M inputs and N outputs, which has a
20 plurality of LUT units; and an internal configuration
control circuit controlling an internal configuration of
the plurality of LUT units.

Fig.1

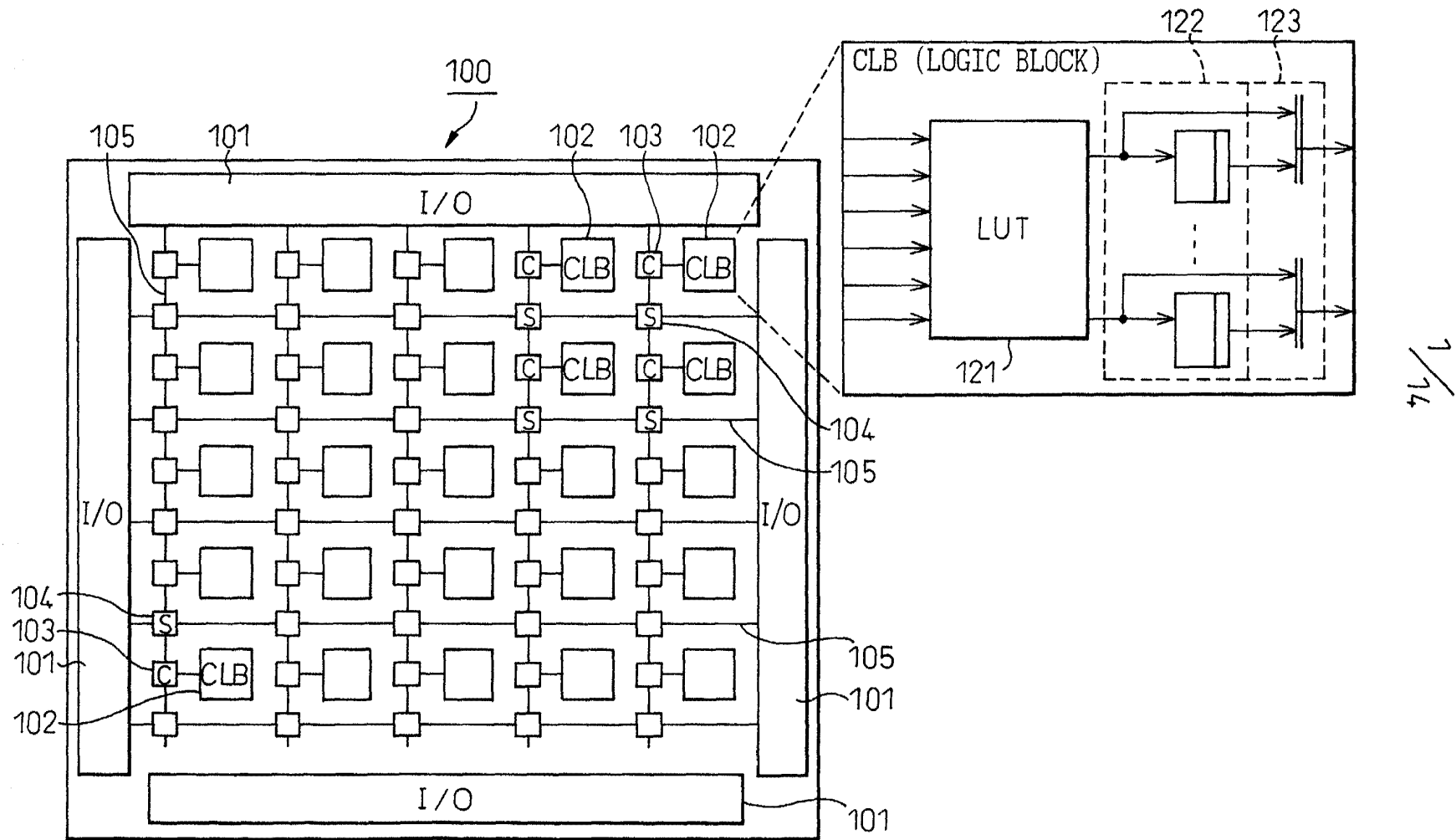


Fig.2

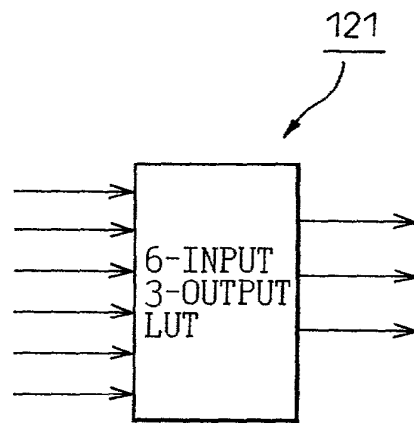


Fig.3A

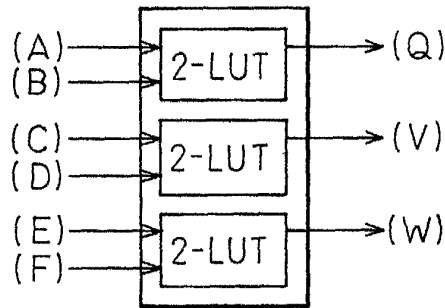


Fig.3B

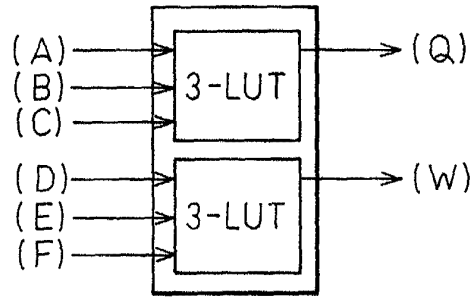


Fig.3C

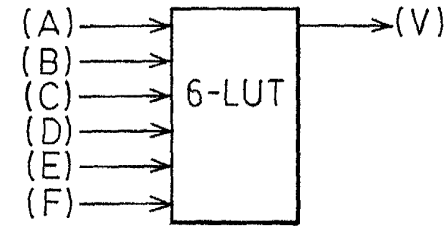


Fig.3D

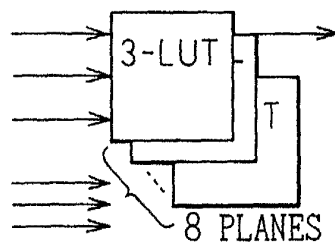


Fig.3E

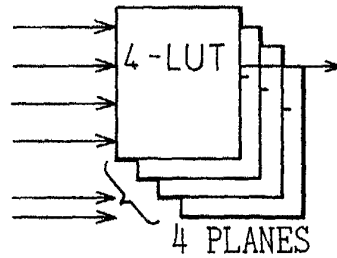


Fig.3F

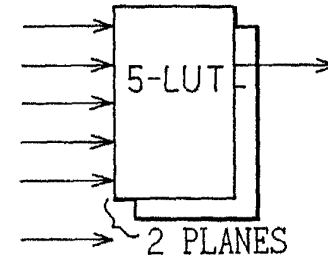
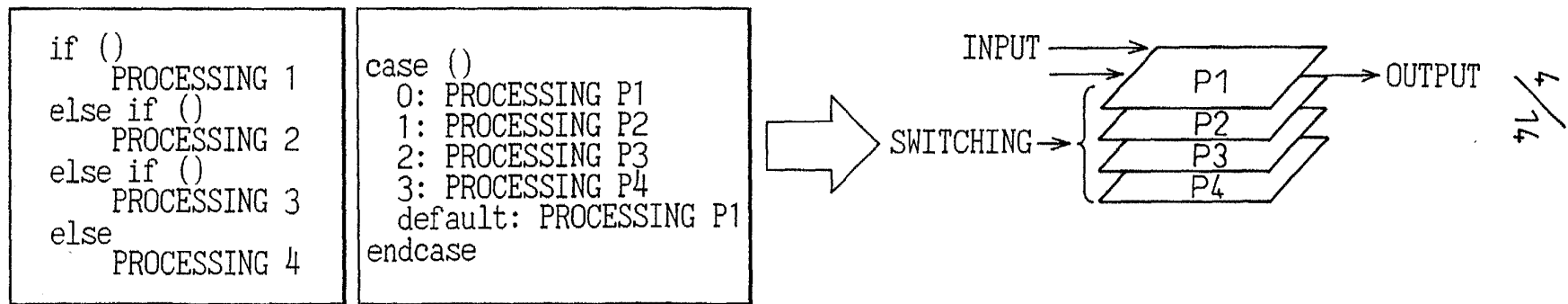


Fig.4



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Fig.5

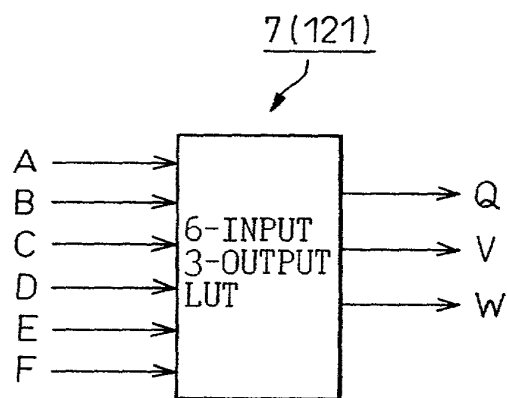


Fig.6

7 (121)

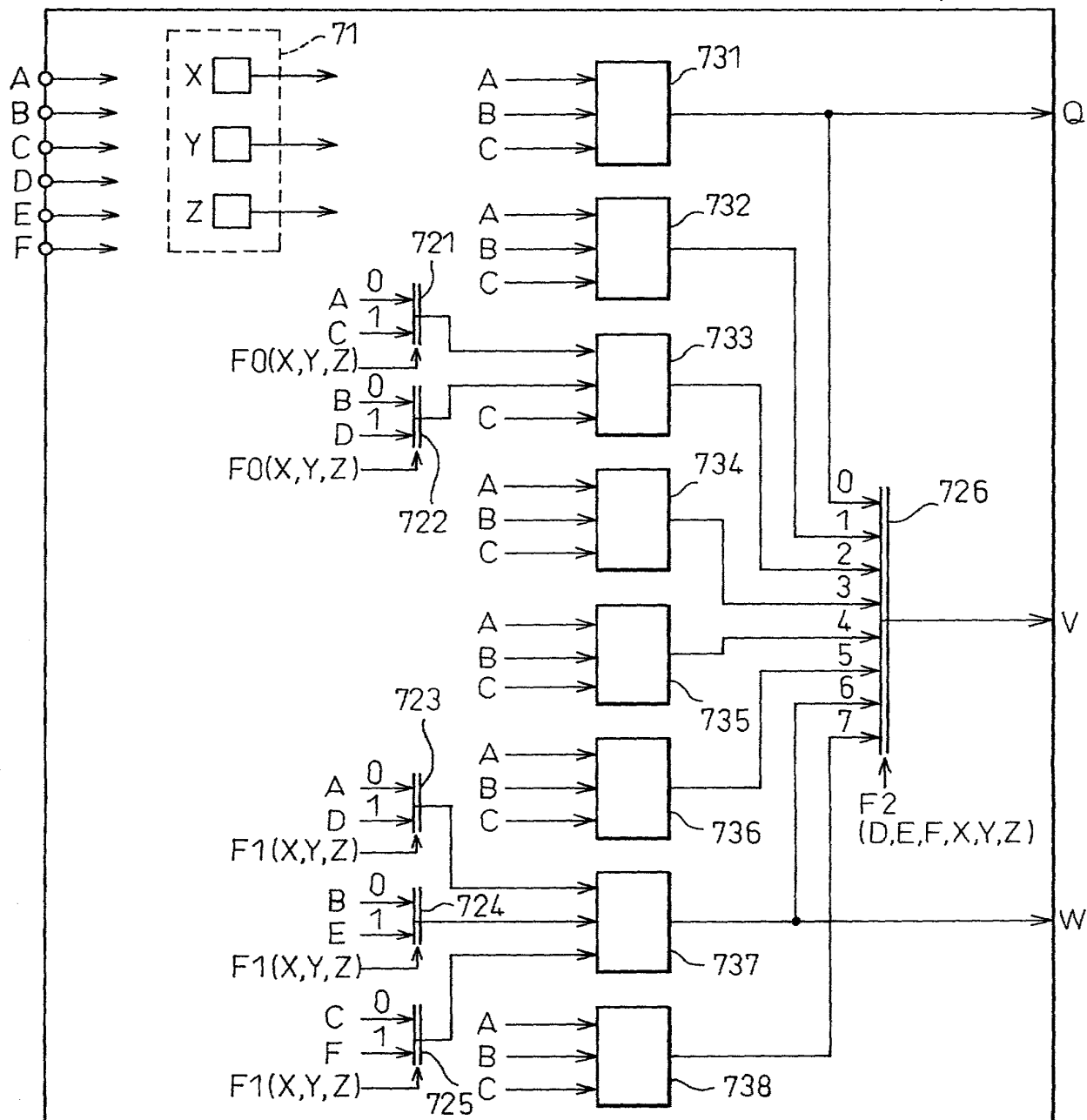


Fig.7

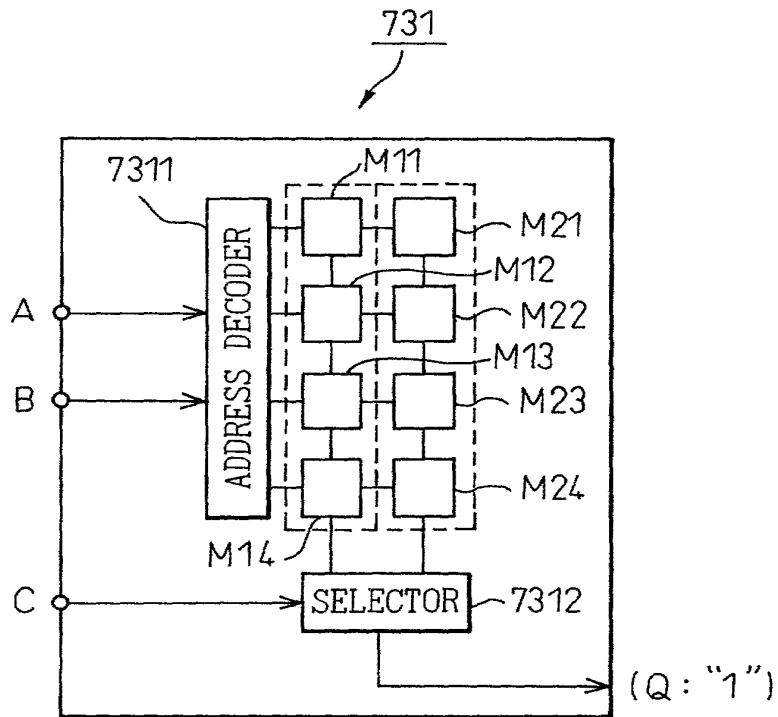


Fig. 8

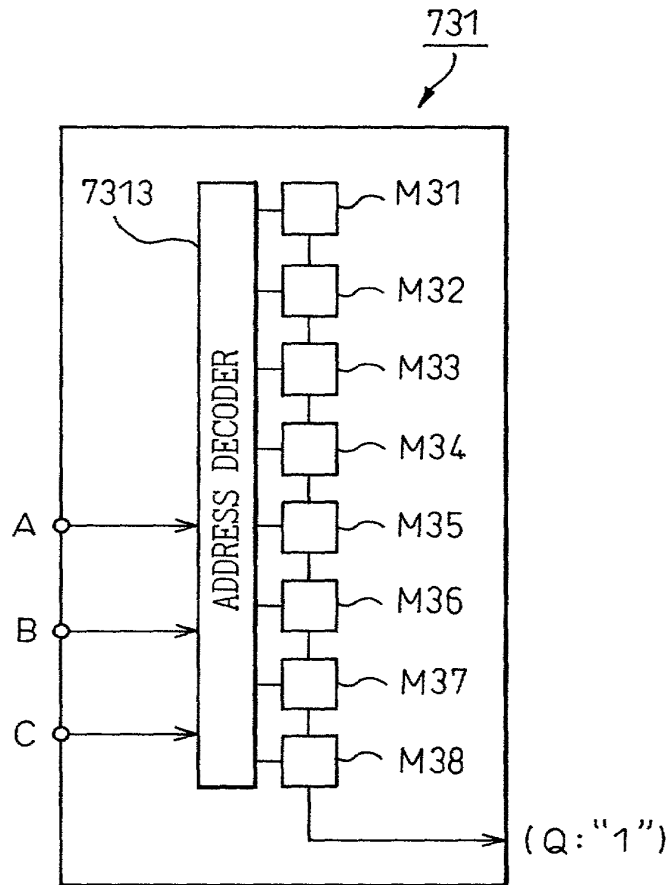


Fig.9

8(121)

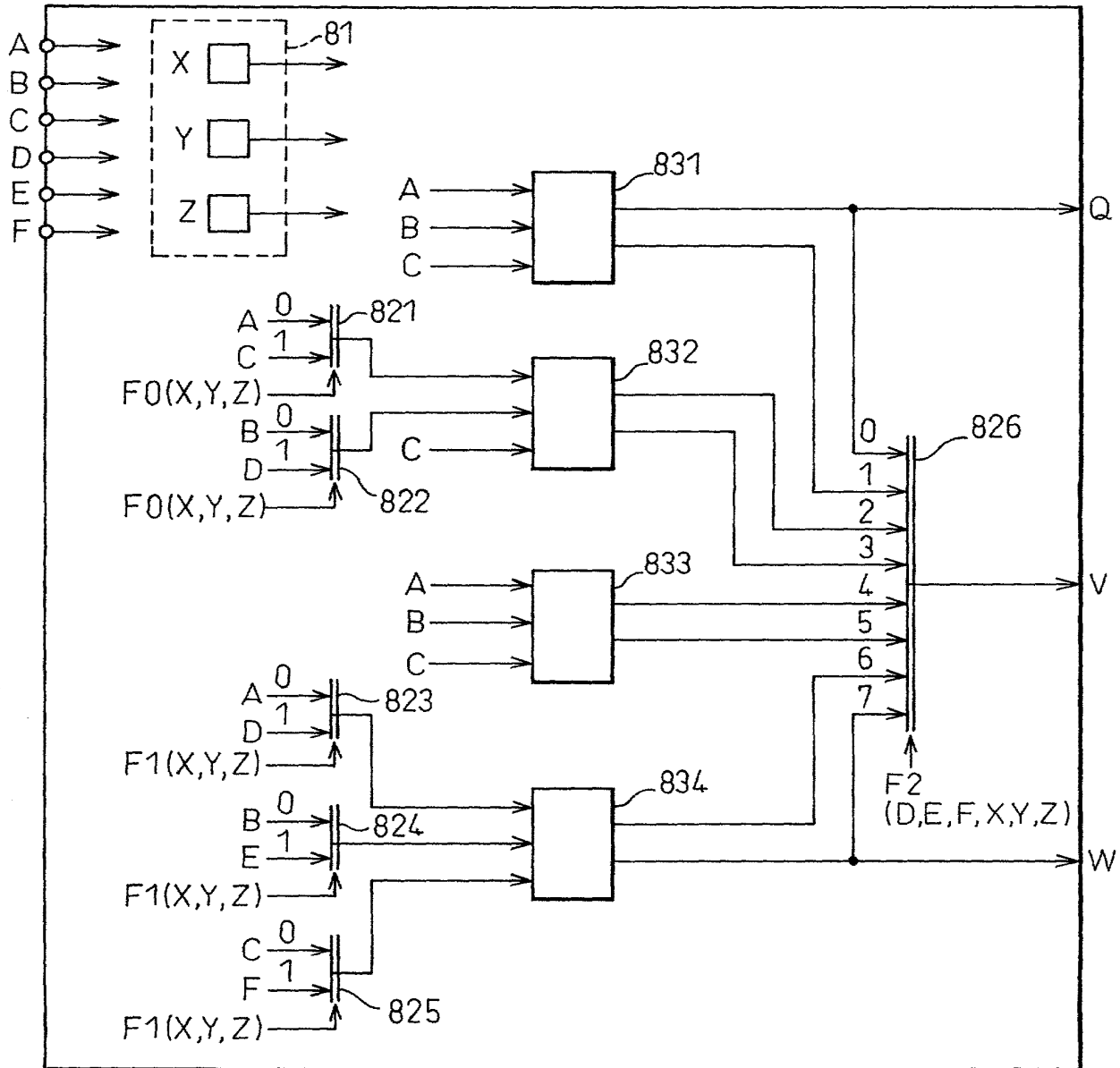


Fig.10

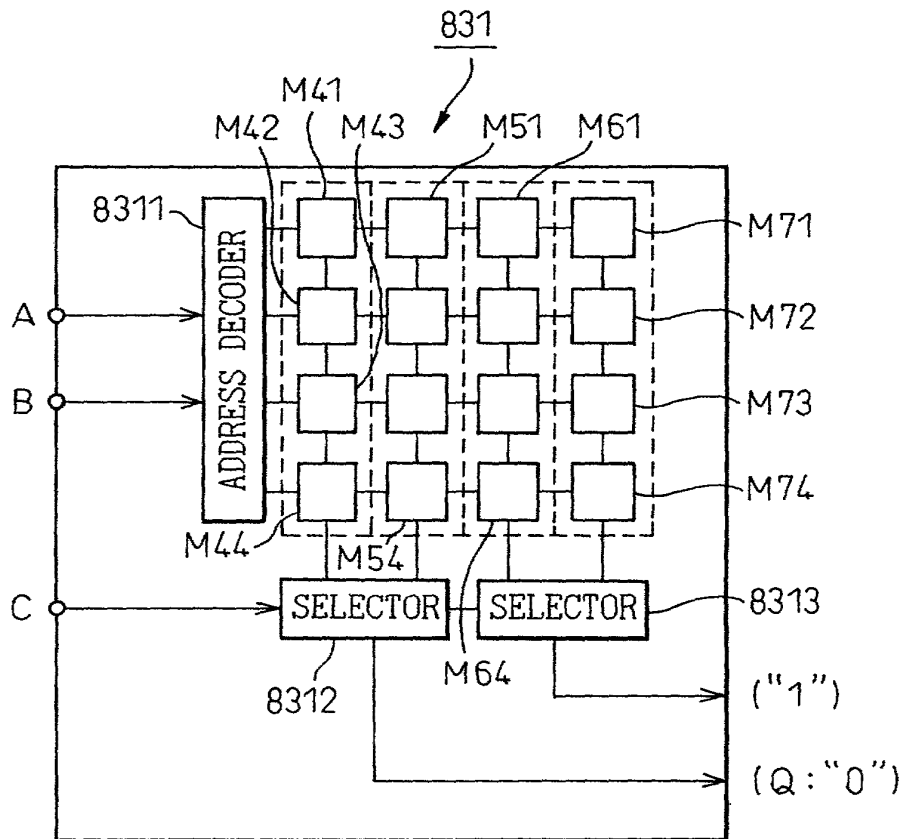


Fig.11

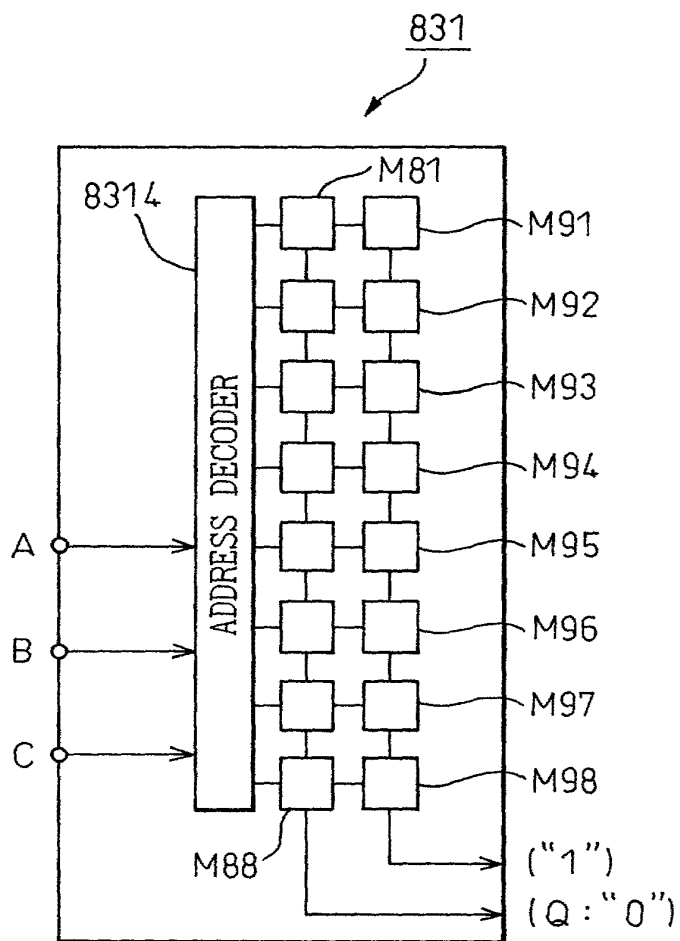


Fig.12

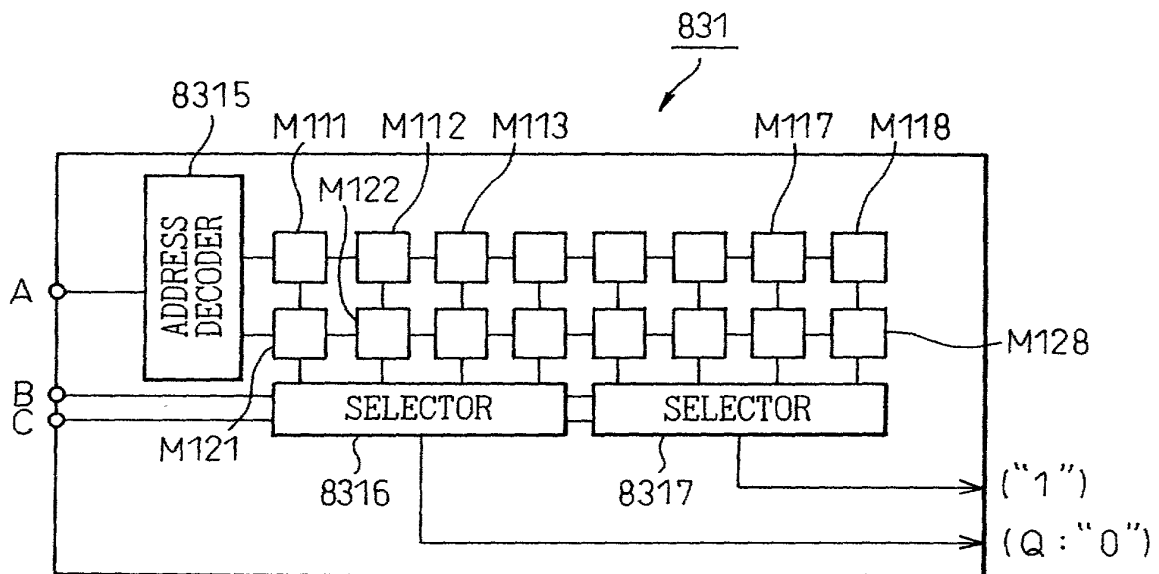
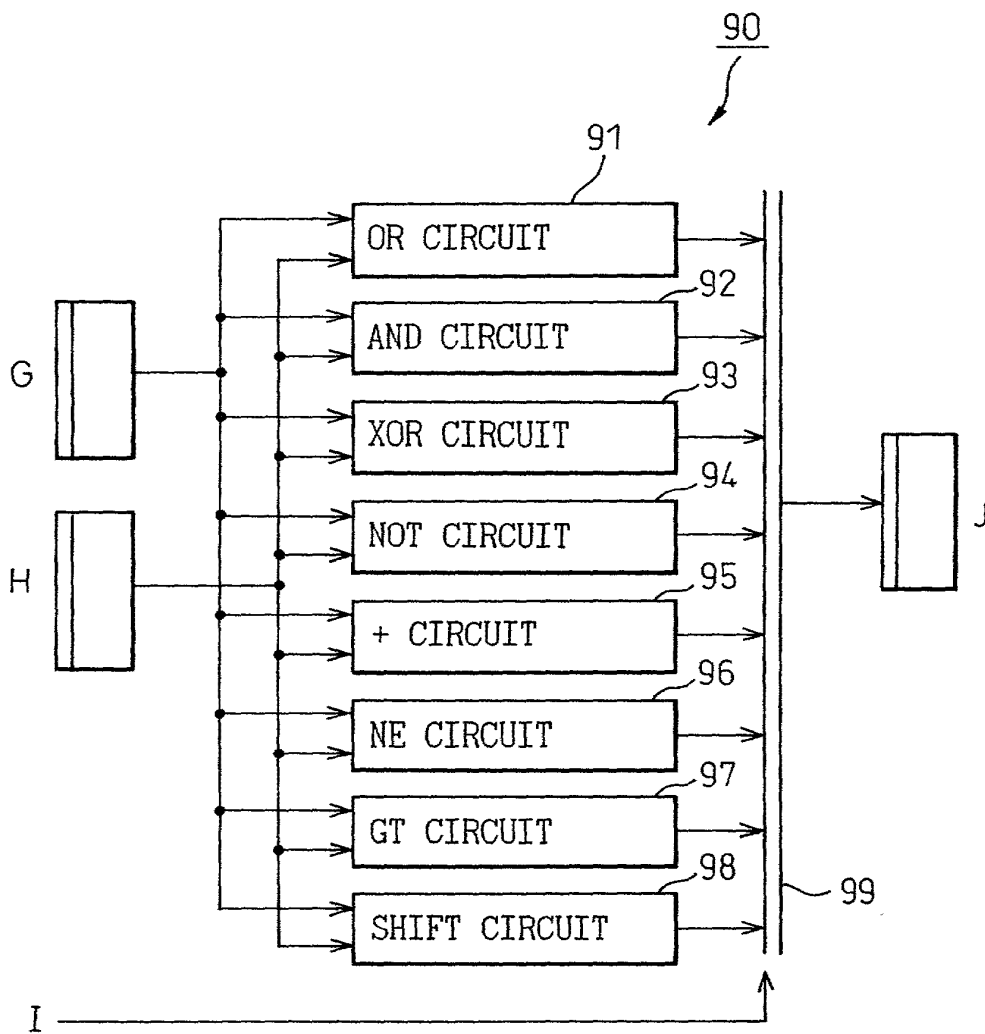


Fig.13



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Fig.14

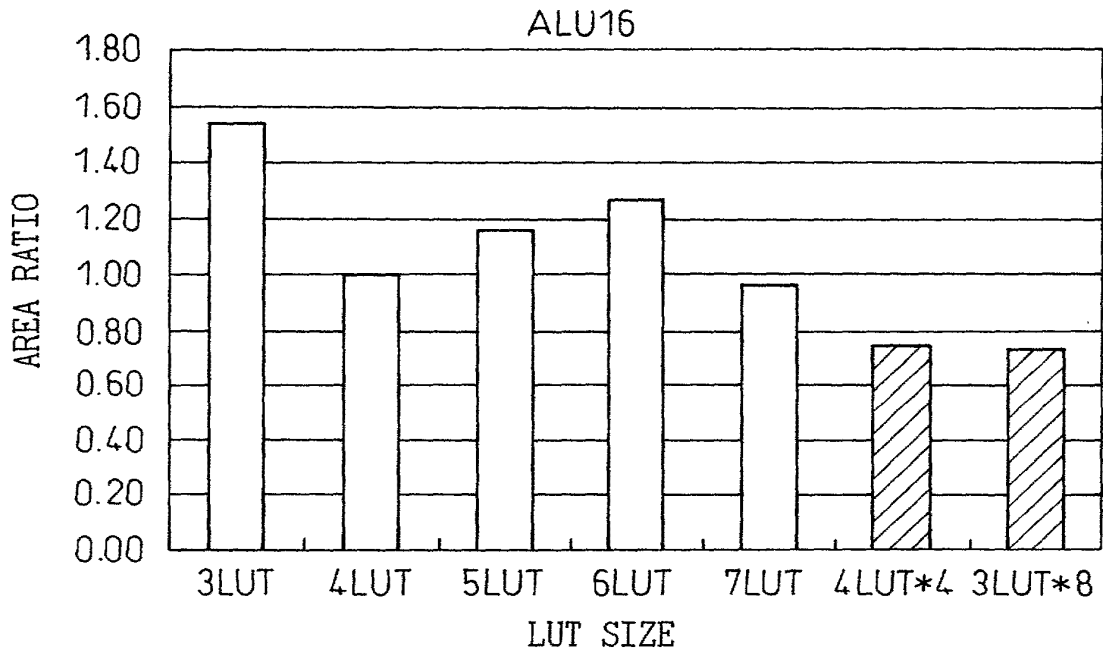
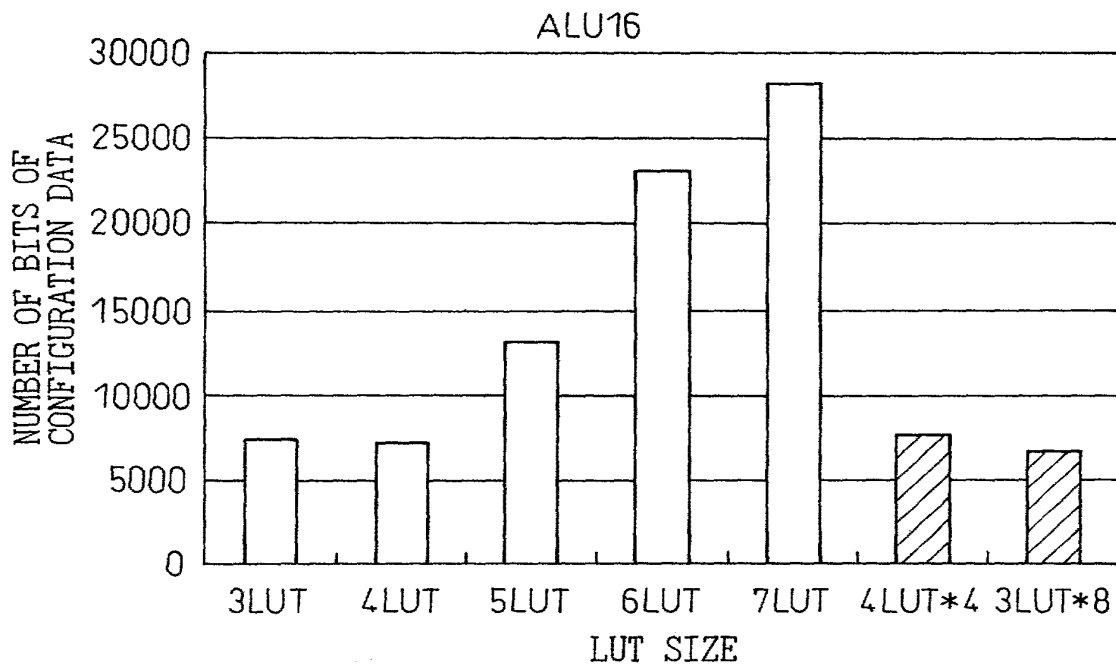


Fig.15



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特許出願宣言書及び委任状

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日本語宣言書

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My residence, post office address and citizenship are as stated next to my name.

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I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

PROGRAMMABLE LOGIC CIRCUIT DEVICE

HAVING LOOK UP TABLE ENABLING
TO REDUCE IMPLEMENTATION AREA

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☐ was filed on _____
as United States Application Number or
PCT International Application Number
_____ and was amended on
_____ (if applicable).

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I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

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Prior Foreign Application(s)

外国での先行出願 2001-199644 (Pat. Appln.)	Japan
(Number) (番号)	(Country) (国名)
(Number) (番号)	(Country) (国名)

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(Application No.) (出願番号)	(Filing Date) (出願日)
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(Application No.) (出願番号)	(Filing Date) (出願日)
(Application No.) (出願番号)	(Filing Date) (出願日)

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Priority Not Claimed
優先権主張なし

29/June/2001
(Day/Month/Year Filed)
(出願年月日)

(Day/Month/Year Filed)
(出願年月日)

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)
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(現況: 特許許可済、係属中、放棄済)

(Status: Patented, Pending, Abandoned)
(現況: 特許許可済、係属中、放棄済)

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Japanese Language Declaration (日本語宣言書)

委任状: 私は下記の発明者として、本出願に関する一切の
 手続を米特許商標局に対して遂行する弁理士または代理人
 として、下記の者を指名いたします。(弁理士、または代理
 人の氏名及び登録番号を明記のこと)

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 Stein, 37,240; Paul I. Kravetz, 35,230; Gerald P. Joyce, III, 37,648; Todd E. Marlette, 35,269; Harlan B. Williams, Jr., 34,756;
 George N. Stevens, 36,938; Michael C. Soldner, 41,455; Norman L. Ourada, 41,235; Kevin R. Spivak, P-43,148; and William M.
 Schertler, 35,348 (agent)

書類送付先

POWER OF ATTORNEY: As a named inventor, I hereby appoint
 the following attorney(s) and/or agent(s) to prosecute this
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 Office connected therewith (list name and registration number)

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 (202) 434-1500

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(第三以降の共同発明者についても同様に記載し、署名をす
 ること)

(Supply similar information and signature for third and subsequent
 joint inventors.)

11002-U.S. PTO

10/183590



PATENT NUMBER and
ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM 10183590	FILING DATE 06/28/2002	CLASS 326	SUBCLASS 41	GAU 2819	EXAMINER A. TRAN
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**APPLICANTS: Sueyoshi Toshinori; Iida Masahiro;

**CONTINUING DATA VERIFIED:

** FOREIGN APPLICATIONS VERIFIED:

JAPAN 2001-199644 06/29/2001

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Foreign priority claimed ☐ yes ☐ no		ATTORNEY DOCKET NO 1687.1001
35 USC 119 conditions met ☐ yes ☐ no		
Verified and Acknowledged Examiners's initials		
TITLE : Programmable logic circuit device having look up table enabling to reduce implementation area		

U.S. DEPT. OF COMM./PAT. & TM.: PTO-436L (Rev. 12-94)

NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED	
		Total Claims	Print Claim for O.G.
Assistant Examiner		DRAWING	
ISSUE FEE		Sheets Drwg.	Figs. Drwg.
Amount Due	Date Paid	Print Fig.	
☐ TERMINAL DISCLAIMER		Primary Examiner	
		Application Examiner	
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ISSUE SLIP STAPLE AREA (for additional cross-references)

ISSUING CLASSIFICATION

ORIGINAL					CROSS REFERENCE(S)									
CLASS		SUBCLASS			CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)								
INTERNATIONAL CLASSIFICATION														
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INDEX OF CLAIMS

✓		Rejected	- (Through numeral) ...	Canceled	N		Non-elected	A		Appeal
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Claim	Final	Original	Date
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If more than 150 claims or 9 actions staple additional sheet here

UTILITY PATENT APPLICATION

TRANSMITTAL

(Only for original applications)

APPLICATION ELEMENTS
See MPEP chapter 600 concerning utility patent application contents.

Attorney Docket No. 1687.1001

First Named Inventor or Application Identifier:
Toshinori SUEYOSHI, et al.

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Washington, DC 20231

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1. ☒ Fee Transmittal Form
2. ☒ Specification, Claims & Abstract[Total Pages: 22]
3. ☒ Drawing(s) (35 USC 113)[Total Sheets: 14] [FIGS. 1-15]
4. ☒ Oath or Declaration[Total Pages: 3]
 - a. ☒ Newly executed (original or copy)
 - b. ☐ Copy from a prior application (37 CFR 1.63(d))
 - i. ☐ **DELETION OF INVENTOR(S)**
Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
5. ☐ Verified Statement Claiming Small Entity Status
6. ☐ Application Data Sheet. See 37 C.F.R. 1.76
7. ☒ Applicant claims foreign priority benefit to: Japanese Application 2001-199644 filed June 29, 2001
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10. ☐ For publication of assignee information under 37 CFR 1.215(b), list the assignee as . The Assignment papers will be filed later.

**FEE VALUE
ACCOUNTABILITY**

DEPOSIT ACCOUNT NO. 193935

FEE CODE	VALUE FURNISHED

ACCOMPANYING APPLICATION PARTS

11. ☒ Assignment (cover sheet & document(s)) to SEMICONDUCTOR TECHNOLOGY ACADEMIC RESEARCH CENTER of Yokohama, Japan

☒ for publication of assignee information under 37 CFR 1.215(b)
12. ☐ 37 CFR 3.73(b) Statement (when there is an assignee) ☐ Power of Attorney
13. ☐ English Translation Document (if applicable)
14. ☒ Information Disclosure Statement (IDS)/PTO-1449 ☒ Copies of IDS Citations
15. ☐ Preliminary Amendment
16. ☒ Return Receipt Postcard (MPEP 503) (Should be specifically itemized)
17. ☒ Certified Copy of Priority Document(s) (if foreign priority is claimed)
18. ☐ Request and Certification for Nonpublication under 35 U.S.C. 122(b)(2)(B)(i). Applicant must attach form PTO/SB/35 or its equivalent
19. ☐ Other:

20. CORRESPONDENCE ADDRESS



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PATENT TRADEMARK OFFICE

NEW APPLICATION FEE TRANSMITTAL		Attorney Docket No.	1687.1001
		Application Number	
		Filing Date	June 28, 2002
AMOUNT ENCLOSED	\$ 780.00	First Named Inventor	Toshinori SUEYOSHI, et al.

FEE CALCULATION (fees effective 10/01/01)

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	TOTAL CLAIMS	20 - 20 =	0	X \$ 18.00 =	\$ 0.00
	INDEPENDENT CLAIMS	3 - 3 =	0	X \$ 84.00 =	0.00
	MULTIPLE DEPENDENT CLAIMS (any number; if applicable)			+ \$280.00 =	
				BASIC FILING FEE	740.00
				Total of above Calculations =	\$ 740.00
	Surcharge for late filing fee, Oath or Declaration (37 CFR 1.53(f)) (\$130.00)				
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				TOTAL FILING FEE =	\$ 740.00
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	Recordation of Assignment (\$40.00; 37 CFR 1.21(h))				
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SUBMITTED BY: STAAS & HALSEY LLP

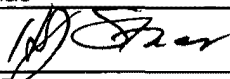
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Signature		Date	June 28, 2002

Fig. 1

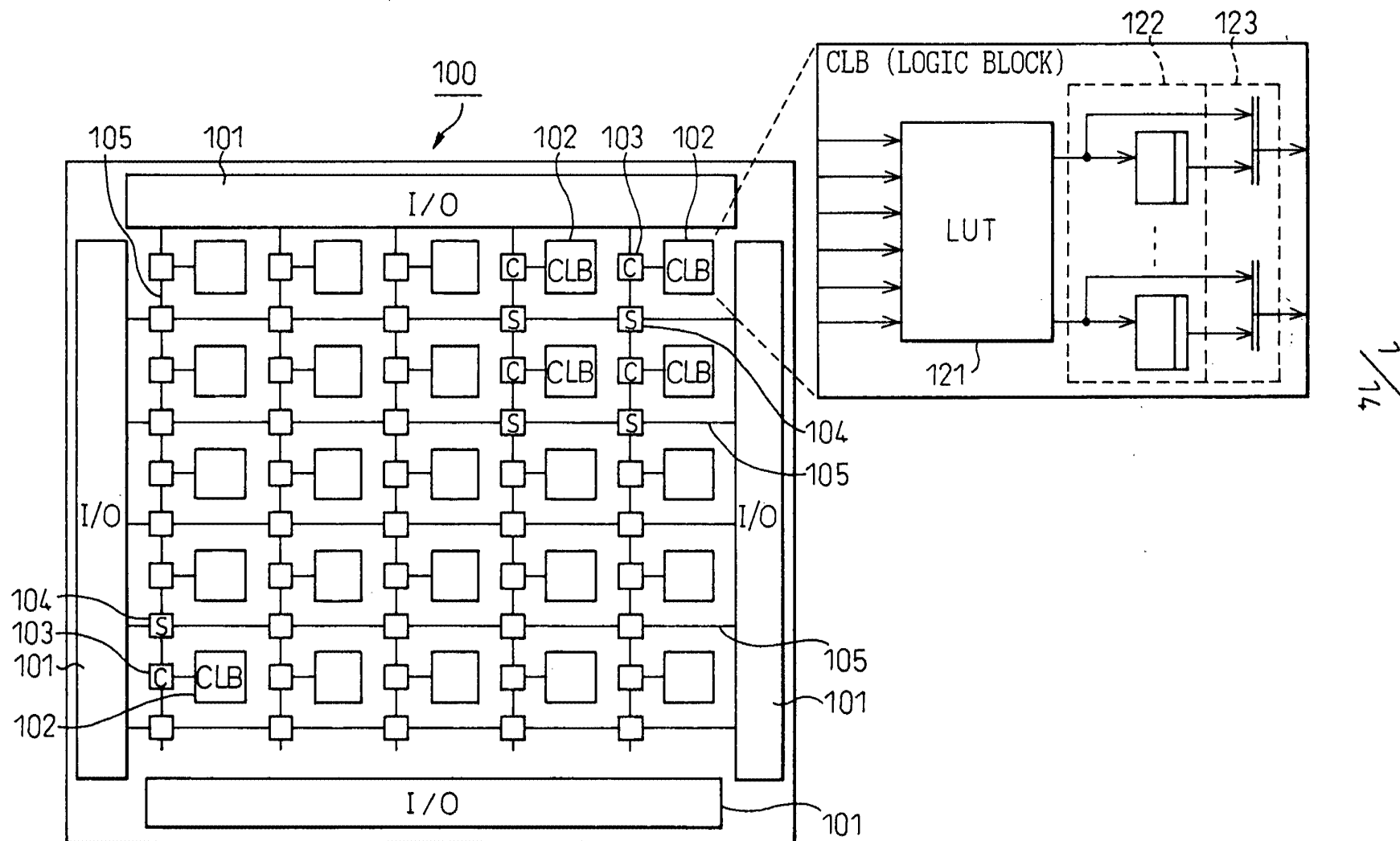
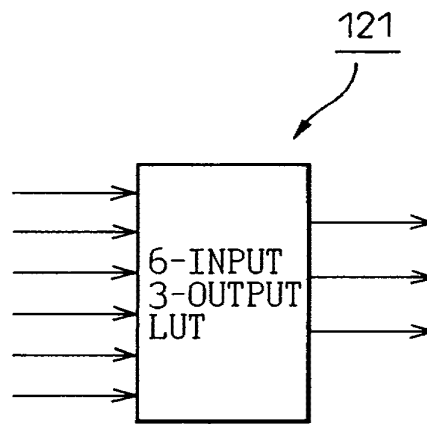


Fig.2



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Fig.3A

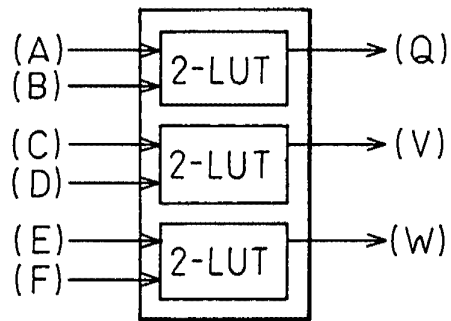


Fig.3B

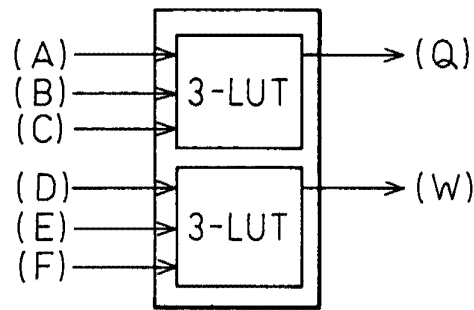


Fig.3C

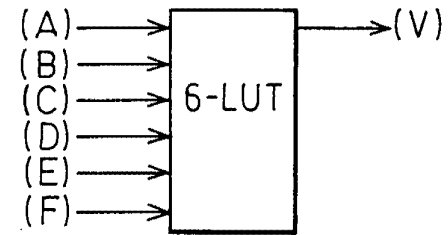


Fig.3D

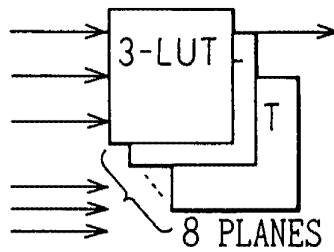


Fig.3E

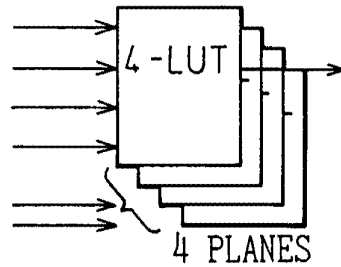


Fig.3F

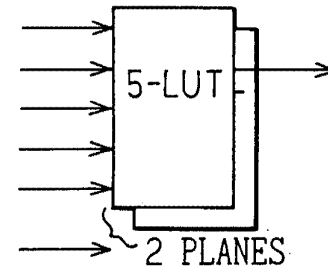


Fig.4

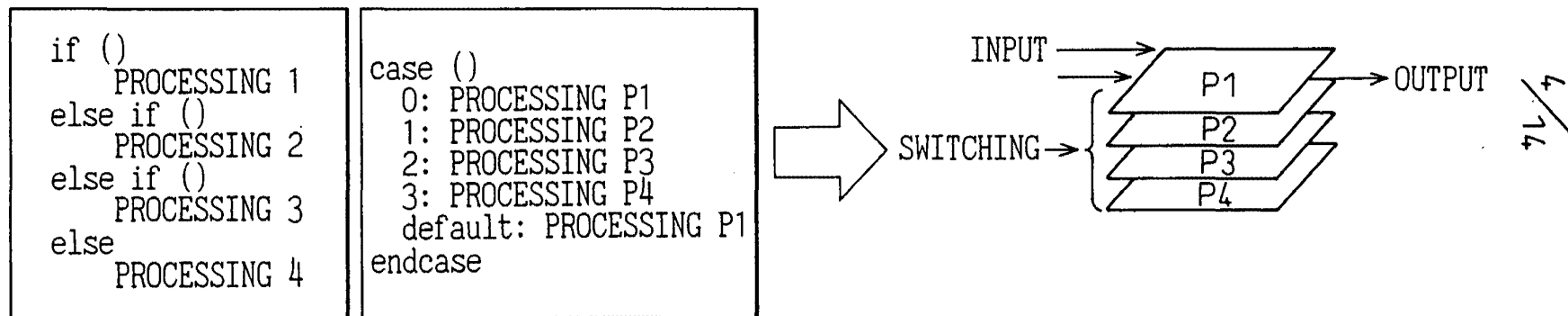


Fig. 5

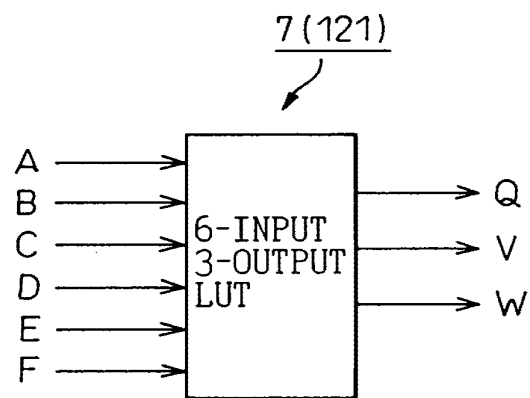


Fig. 6

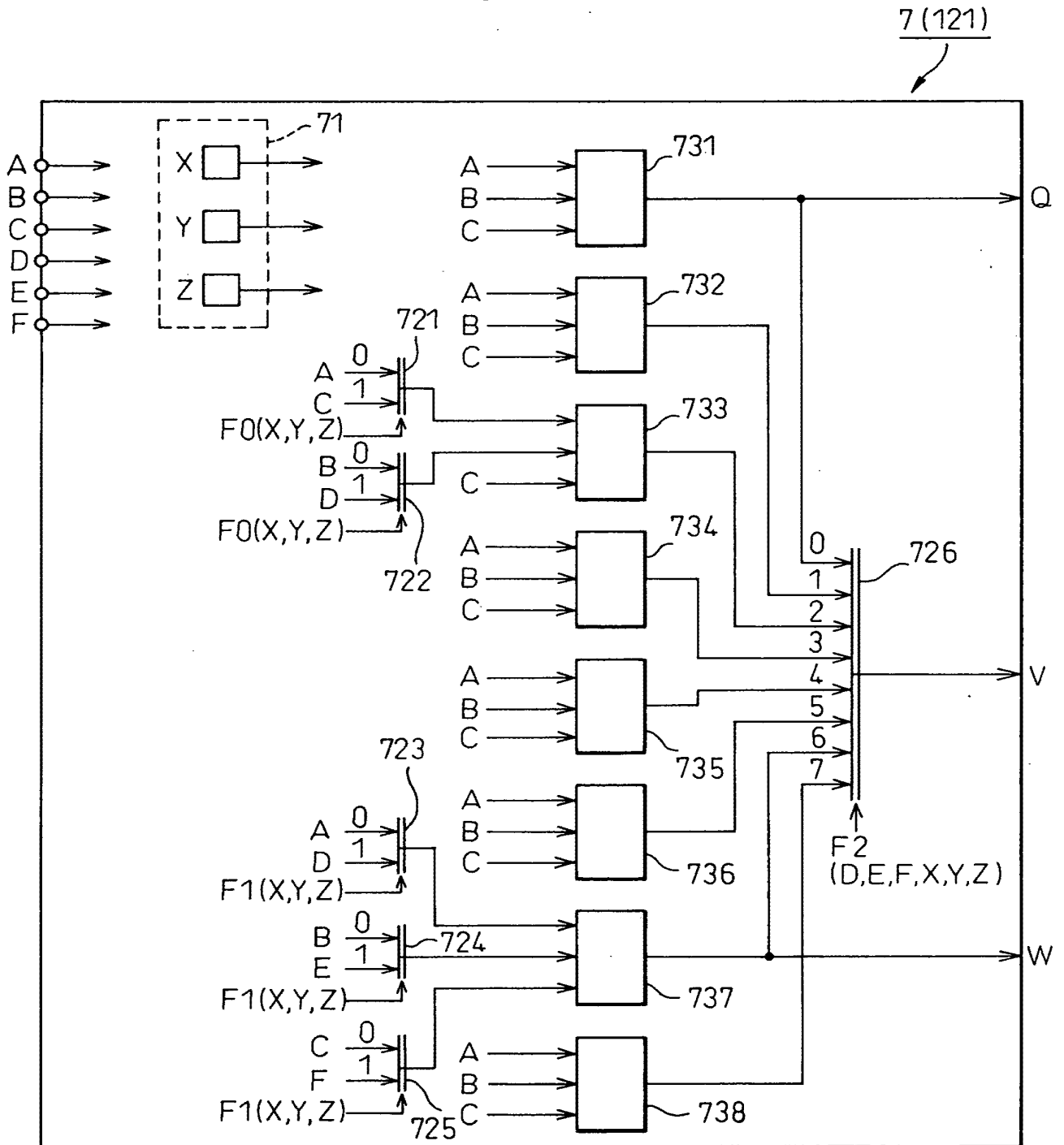


Fig.7

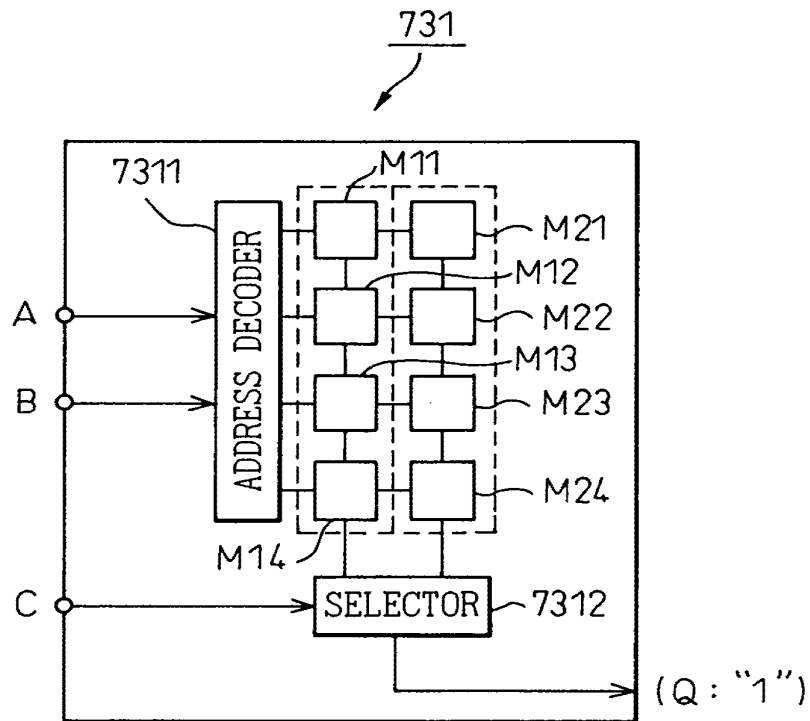


Fig. 8

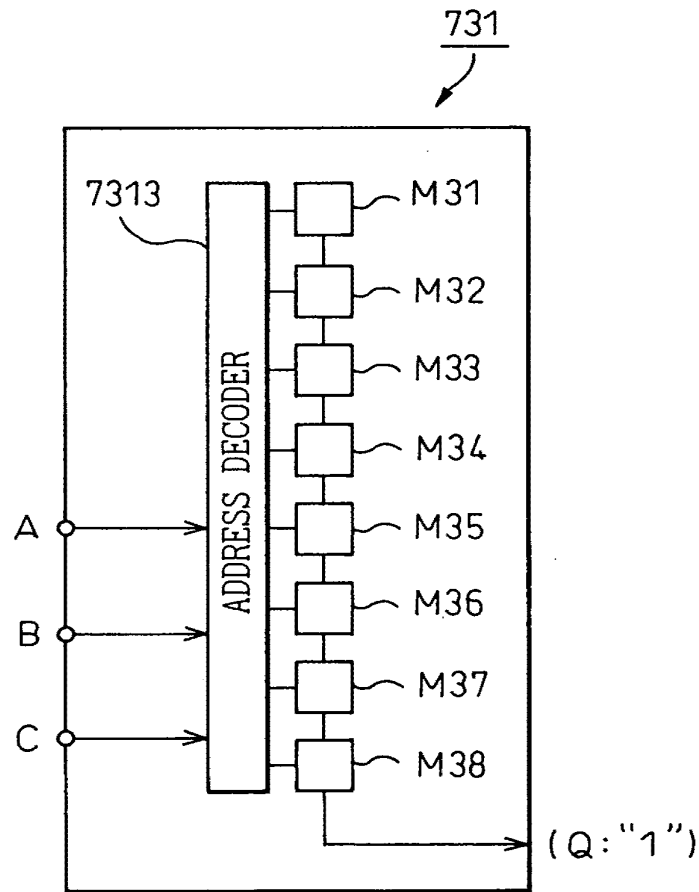


Fig.9

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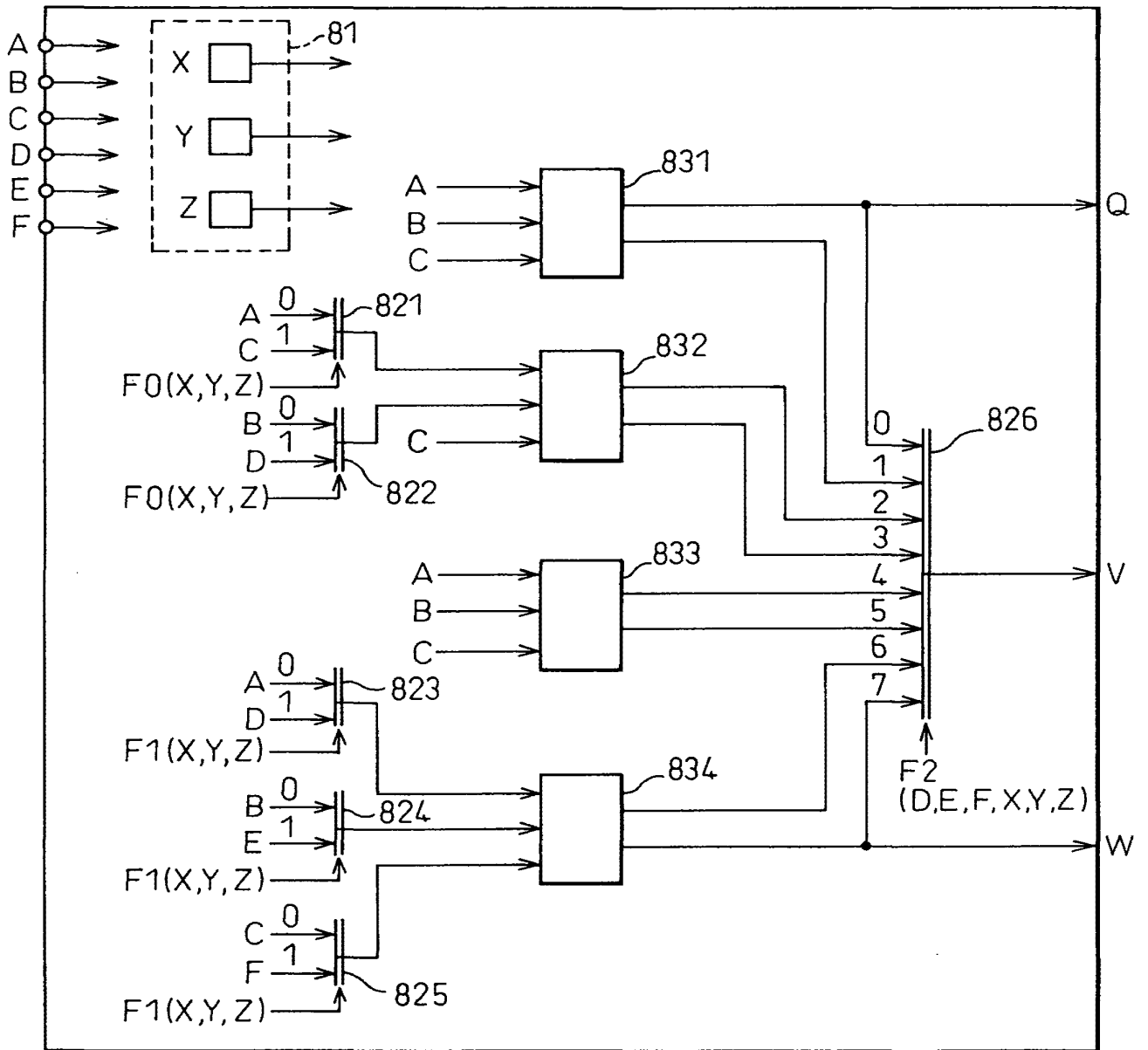


Fig.10

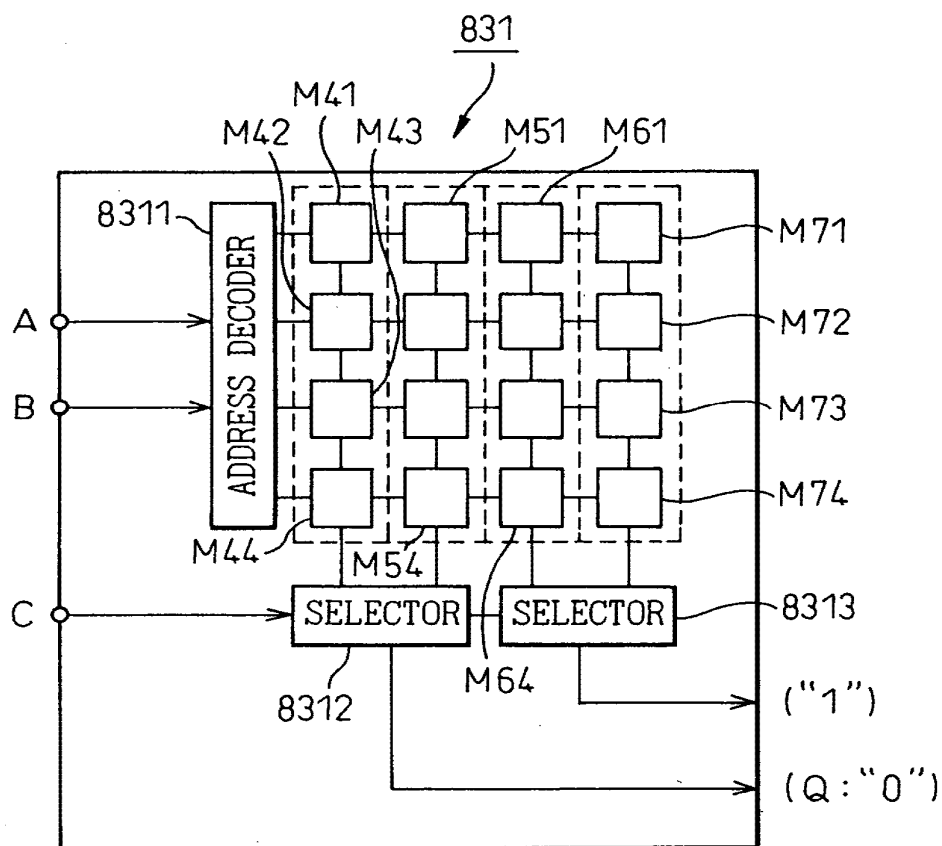


Fig.11

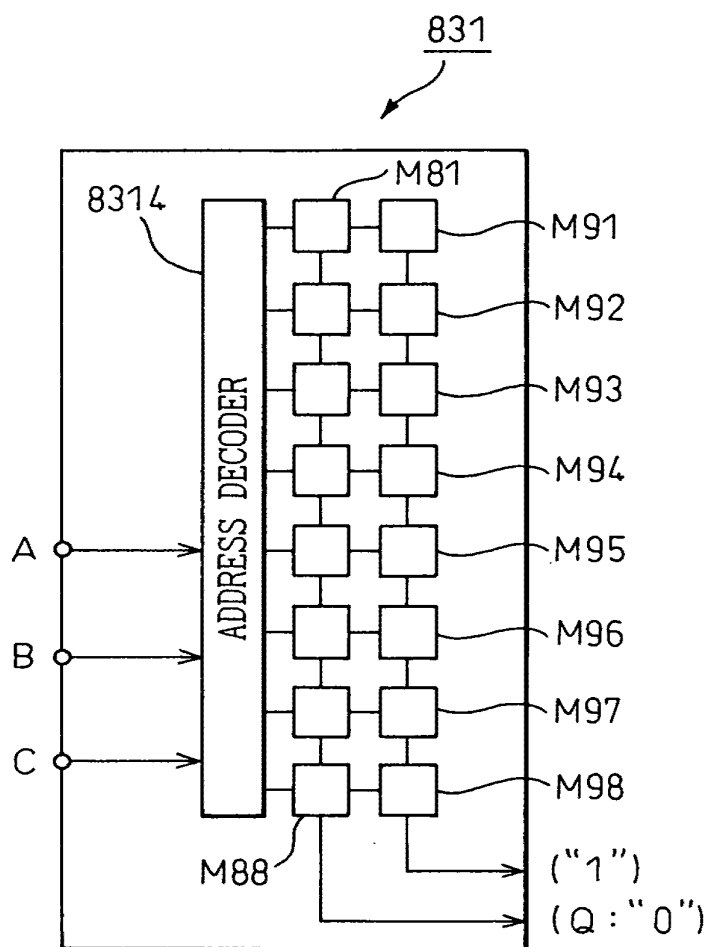


Fig.12

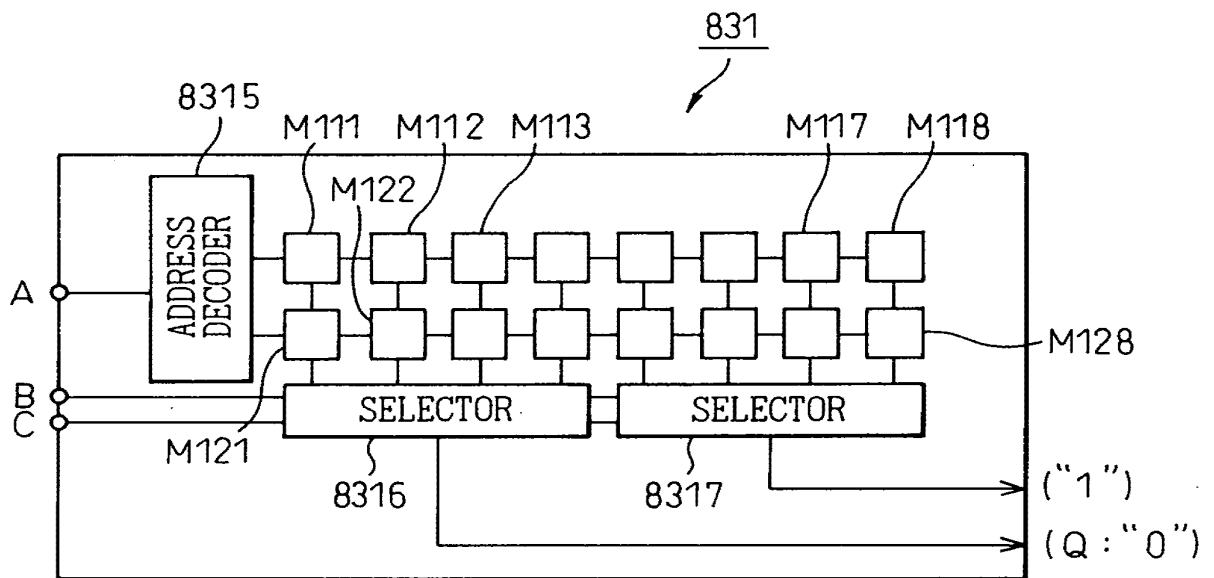
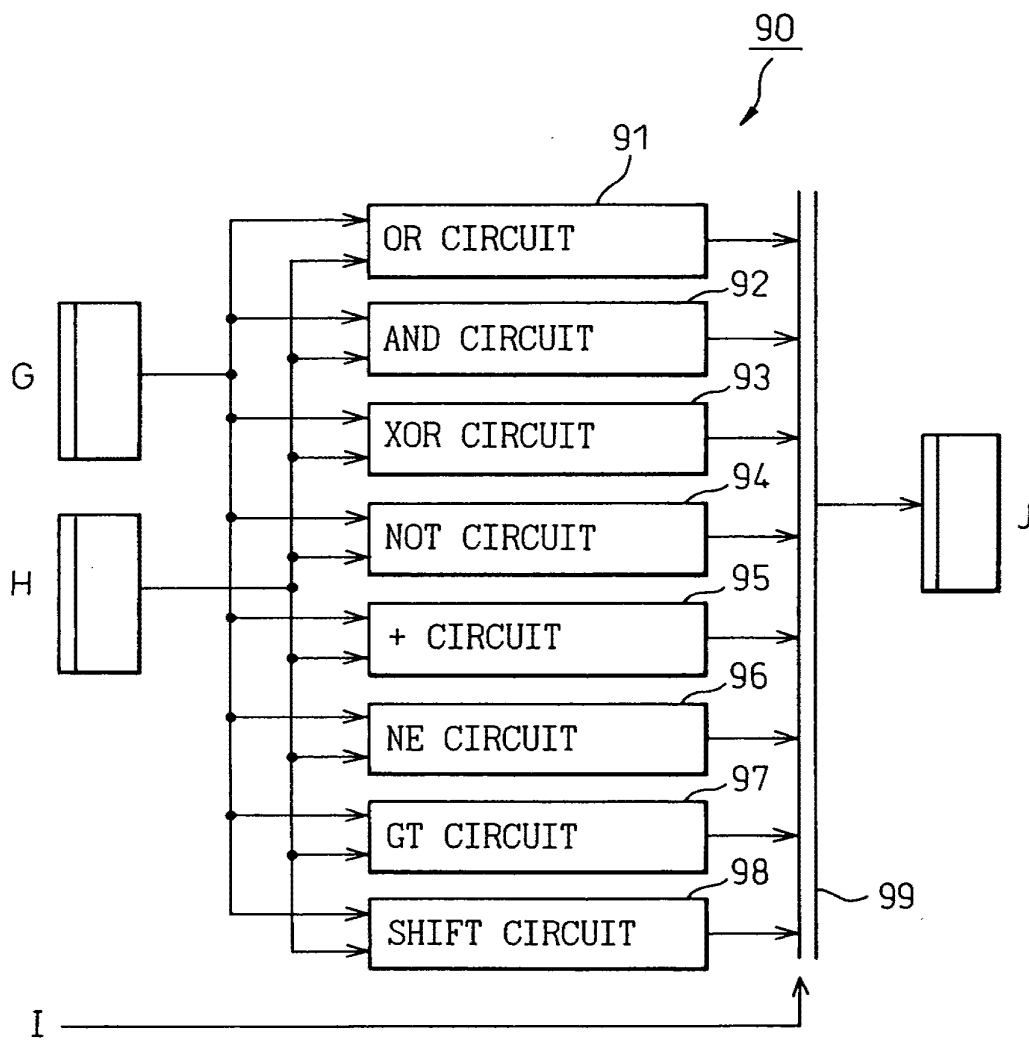


Fig.13



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Fig.14

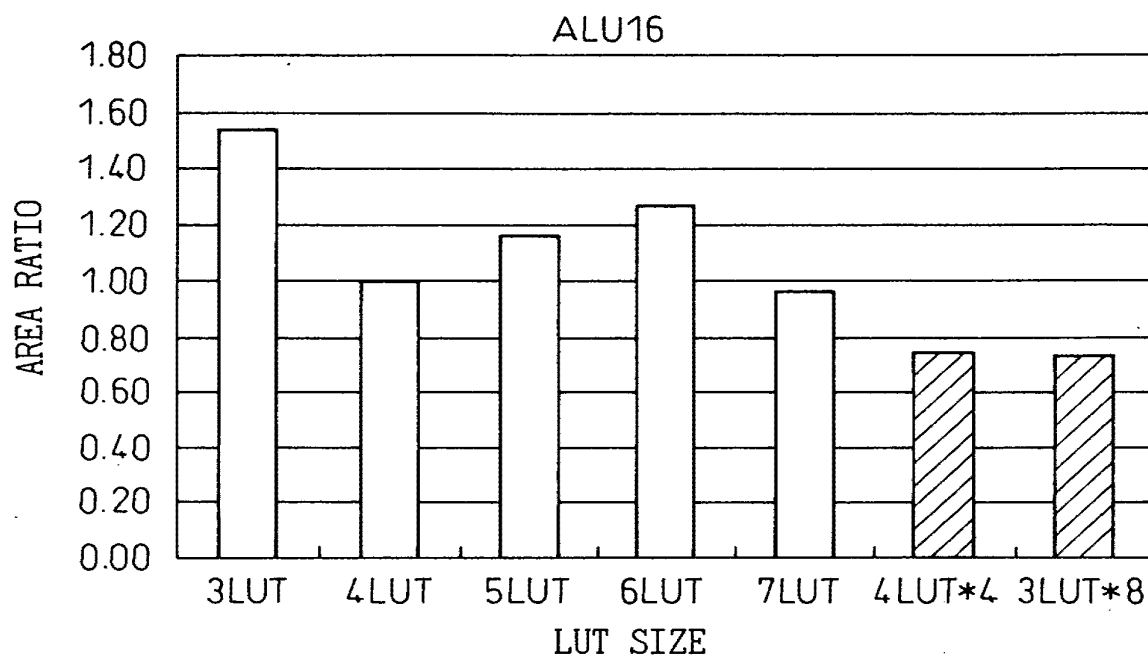
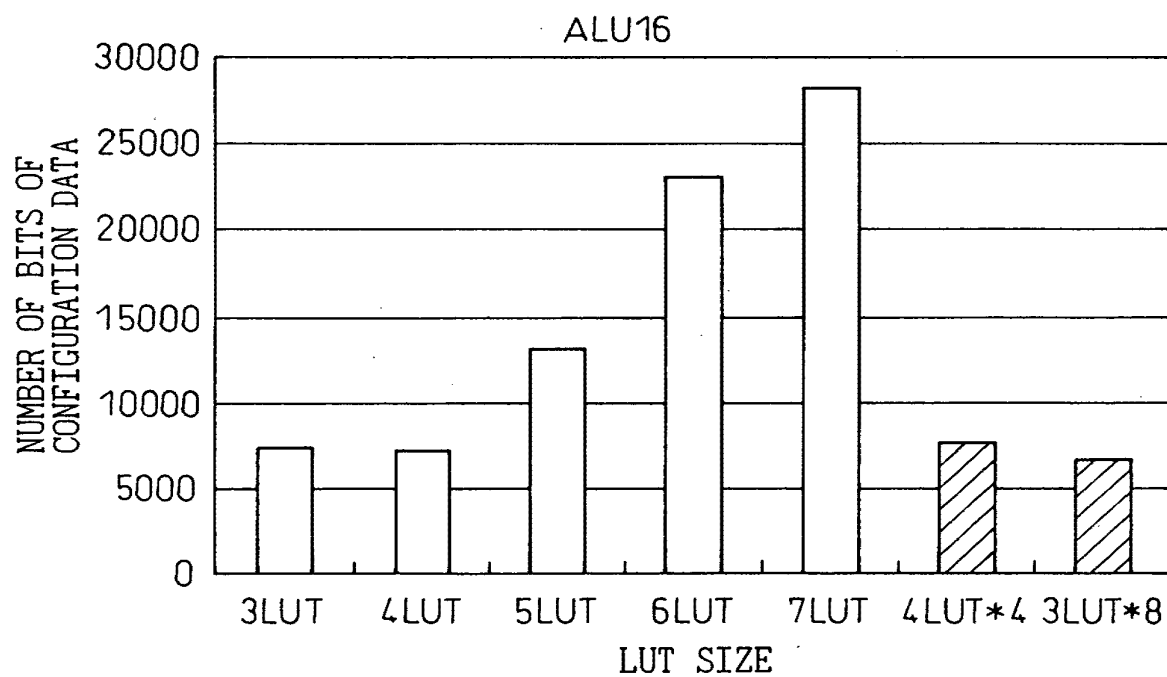


Fig.15



PROGRAMMABLE LOGIC CIRCUIT DEVICE HAVING LOOK UP TABLE
ENABLING TO REDUCE IMPLEMENTATION AREA

5 BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to an architectural technology for configuring a look up table that enables implementation area to be reduced.

10 2. Description of the Related Art

15 Recently, a programmable logic circuit device has attracted much attention as a device that can realize various logic circuits which meets diverse needs of users by programming internal circuits. Such a programmable logic circuit device is known as PLD (Programmable Logic Device) or FPGA (Field Programmable Gate Array), and recently is increasingly used not only for trial fabrication of hardwares, but also for constructing a large scale circuit (for example, a microprocessor) that has various functions in itself. These programmable logic circuits comprise look up tables (LUT: Look Up Table) as major components, and reduction of circuit area of such LUTs is strongly desired.

20 A look up table (LUT) as a major component of a programmable logic circuit device (PLD or FPGA) is composed of memories, and is capable of implementing an arbitrary logic circuit. Basic architecture of such a FPGA has been previously disclosed, for example, in U.S. Patent No. 4,706,216, and U.S. Patent No. 4,870,302.

25 Multi-context and cluster architecture of plural LUTs in FPGA has been disclosed, for example, in U.S. Patent No. 5,778,439 and U.S. Patent No. 5,905,385, etc. With regard to evaluation of LUT used in FPGA (for example, evaluation of functionality and area, as well as performance evaluation, and evaluation of cluster architecture), study results are found in, for example, J. Rose et al., "Architecture of Field Programmable Gate

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Arrays: The Effect of Logic Block Functionality on Area Efficiency", IEEE J. Solid State Circuits, vol. 25, no. 5, pp. 1217 - 1225, Oct. 1990, J. Rose et al., "The Effect of Logic Block Architecture on FPGA Performance", IEEE J. Solid State Circuits, vol. 27, no. 3, pp. 281-287, Mar. 1992, and E. Ahmed et al., "The Effect of LUT and Cluster Size on Deep Sub-micron FPGA Performance and Density", FPGA 2000, Monterey, CA USA, 2000.

In a programmable logic circuit device, the number of bits M of input signal for the logic circuit that can be implemented corresponds to the number of bits of the address of memory composing the LUT, and the number of bits N of output signal corresponds to the number of output bits of the memory. Thus, a logic circuit that can be implemented in one LUT is an arbitrary logic circuit of M inputs and N outputs. Such a LUT is denoted in the present specification as M-input N-output LUT.

Conventionally, in FPGA for example, the input number M and output number N are both fixed value. Any logic circuit is divided in circuit unit of M inputs and N outputs, and is implemented using plural LUTs.

Therefore, in a conventional FPGA, even if circuit division results in a circuit having input bit number less than M, one LUT needs to be assigned to this circuit, leading to unnecessary increase of implementation area (logic and routing circuitry area; circuit area).

SUMMARY OF THE INVENTION

An object of the present invention is to reduce the circuit area of a look up table (LUT) and hence of a programmable logic circuit device. Another object of the present invention is to reduce power consumption of a programmable logic circuit device.

According to the present invention, there is provided a look up table of M inputs and N outputs, comprising a plurality of LUT units; and an internal

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configuration control circuit controlling an internal configuration of the plurality of LUT units.

Further, according to the present invention, there is provided a programmable logic circuit device

5 comprising a plurality of logic blocks; a plurality of routing wires connected to each of the logic blocks; a plurality of switch circuits provided at an intersection of each of the routing wires; a plurality of connection blocks provided between an I/O line of each of the logic

10 blocks and each of the routing wires; and an I/O block performing an input/output operation with external equipment, wherein each of the logic blocks has a look up table of M inputs and N outputs, comprising a plurality of LUT units; and an internal configuration control

15 circuit controlling an internal configuration of the plurality of LUT units.

The internal configuration control circuit may comprise a plurality of selectors selecting I/O signals of the plurality of LUT units; and a selector control

20 circuit controlling the selectors and defining the internal configuration of the plurality of LUT units. The selector control circuit may comprise a memory, and control the plurality of selectors in accordance with data stored in the memory.

The plurality of selectors may include an input signal selector provided at an input of at least one of the LUT units to select an input signal; and an output signal selector provided at an output of the LUT units selecting an output signal, the input signal selector and the output signal selector being controlled in accordance

30 with the data stored in the memory. The plurality of selectors may include an input signal selector provided at an input of at least one of the LUT units to select an input signal; and an output signal selector provided at

35 an output of the LUT units selecting an output signal, the input signal selector and the output signal selector being controlled in accordance with the input signal.

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The look up table of M inputs and N outputs may be a 6-input 3-output look up table. The 6-input 3-output look up table may comprise eight 3-input 1-output LUT units. The 6-input 3-output look up table may comprise
5 four 3-input 2-output LUT units.

In addition, according to the present invention, there is also provided a method of configuring a look up table of M inputs and N outputs, comprising the steps of providing a plurality of LUT units; and selectively
10 controlling I/O signals of the plurality of LUT units to set a predetermined mode of an internal configuration.

The I/O signals of the plurality of LUT units may be selectively controlled in accordance with data stored in the corresponding look up table. An input signal input
15 to at least one of the LUT units and an output signal output from the LUT unit may be selectively controlled in accordance with data stored in the corresponding look up table. An input signal input to at least one of the LUT units and an output signal output from the LUT unit may
20 be selectively controlled in accordance with a predetermined function of the input signal.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be more clearly understood from the description of the preferred
25 embodiments as set forth below with reference to the accompanying drawings, wherein:

Fig. 1 is a block diagram showing an example of FPGA to which the present invention is applied;

Fig. 2 is a block diagram showing a 6-input 3-output LUT as an example of LUTs in the FPGA;
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Figs. 3A, 3B, 3C, 3D, 3E, and 3F are block diagrams showing the mode of internal configuration of the 6-input 3-output LUT shown in Fig. 2;

Fig. 4 is a view useful for explaining an example of
35 the method of mapping circuits in a look up table;

Fig. 5 is a block diagram showing a 6-input 3-output LUT as an example of a LUT in FPGA according to the

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present invention in conjunction with input/output signal;

Fig. 6 is a block diagram showing an example of the internal configuration of the 6-input 3-output LUT shown in Fig. 5;

Fig. 7 is a block diagram showing an example of 3-input 1-output LUT unit in the 6-input 3-output LUT of Fig. 6;

Fig. 8 is a block diagram showing another example of 3-input 1-output LUT unit in the 6-input 3-output LUT of Fig. 6;

Fig. 9 is a block diagram showing another example of the internal configuration of the 6-input 3-output LUT shown in Fig. 5;

Fig. 10 is a block diagram showing an example of 3-input 2-output LUT unit in the 6-input 3-output LUT of Fig. 9;

Fig. 11 is a block diagram showing another example of 3-input 2-output LUT unit in the 6-input 3-output LUT of Fig. 9;

Fig. 12 is a block diagram showing still another example of 3-input 2-output LUT unit in the 6-input 3-output LUT of Fig. 9;

Fig. 13 is a block diagram showing an example of configuration of a 8 operation ALU circuit (ALU 16);

Fig. 14 is a view showing difference of the area ratio for ALU 16 shown in Fig. 13 when implemented with LUT in conventional FPGA compared to LUT in FPGA according to the present invention; and

Fig. 15 is a view showing difference of the number of bits of configuration data for ALU 16 shown in Fig. 13 when implemented with LUT in conventional FPGA compared to LUT in FPGA according to the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Now, a look up table, a programmable logic circuit device comprising a look up table and a method for configuring a look up table according to the present

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invention will be described in detail below with reference to appended drawings.

Fig. 1 is a block diagram showing an example of FPGA to which the present invention is applied. In Fig. 1, reference numeral 100 denotes FPGA as an example of a programmable logic circuit device, 101 is an I/O block, 102 is a logic block (CLB: Configurable Logic Block), 103 is a connection block (C), 104 is a switch matrix (S), and 105 denotes routing wires.

As shown in Fig. 1, FPGA 100 is comprised of logic blocks (CLB) 102 arranged in the form of array, routing wire (channel area) 105 surrounding these CLB 102, and I/O blocks 101. At the intersection of the routing wire 105, switch matrices (S) 104 are disposed for connecting these components, and connection block (C) 103 is disposed between the I/O line of each CLB 102 and the routing wire 105. Each CLB 102 is comprised of a look up table (LUT) 121, latches 122, and selectors 123. The present invention relates mainly to the configuration of LUT 121.

Fig. 2 is a block diagram showing a 6-input 3-output LUT as an example of a LUT in a FPGA. This is an example of a LUT 121 in Fig. 1. Thus, the LUT shown in Fig. 2 corresponds to the configuration of a case of M-input N-output LUT in which $M = 6$, $N = 3$. The case of $M = 6$, $N = 3$ is only an example, and value of M and N is not limited to this case, but may include various other values, and may include the case $M = N$, or $M < N$.

Figs. 3A to 3F are block diagrams showing different modes of internal configuration of the 6-input 3-output LUT shown in Fig. 2, and showing that, as will be described in detail later, by varying the values (X, Y, Z) of mode changing memory (71), the 6-input 3-output LUT can be set to different internal configurations as shown in Figs. 3A to 3F.

Specifically, Fig. 3A shows a case where the 6-input 3-output LUT is set to a mode of three 2-input 1-output

LUT. In conventional FPGA (conventionally composed by using 4-input 1-output LUT as a unit), for example, three LUTs (4-input 1-output LUT) are required to assign three 2-input 1-output circuits to LUTs. In the configuration shown in Fig. 3A, only one 6-input 3-output LUT needs to be used for this purpose.

Area ratio of 4-input 1-output LUT to 6-input 3-output LUT including routing channel area is about 1 : 1.5. Therefore, as compared to the conventional configuration using three 4-input 1-output LUTs, the configuration shown in Fig. 3A can reduce the circuit area ratio to about $(1 \times 3) : 1.5$, that is, to about 1 : 0.5. Thus, reduction of circuit area of maximum 50% can be achieved.

Fig. 3B shows a case where the LUT is set to a mode of two 3 input 1 output LUTs. In this case, as compared to the conventional configuration where two 4-input 1-output LUTs are used, the circuit area ratio can be reduced to $(1 \times 2) : 1.5$, that is, 1 : 0.75. Thus, reduction of circuit area of maximum 25% can be achieved.

Further, Fig. 3C shows a case where the 6-input 3-output LUT is set to a mode of 6-input 1-output LUT.

Fig. 3D shows a case where the 6-input 3-output LUT is set to a mode of 3-input 1-output LUT $\times$ 8 planes.

Fig. 3E shows a case where the 6-input 3-output LUT is set to a mode of 4-input 1-output LUT $\times$ 4 planes, and Fig. 3F shows a case where the 6-input 3-output LUT is set to a mode of 5-input 1-output LUT $\times$ 2 planes.

Fig. 4 is a view useful for explaining the mapping method of circuits in the look up table, which shows the reason why mode setting of Figs. 3D to 3F above is possible.

As shown in Fig. 4, in the mapping method which utilizes, for example, the control structure of if ~, else, case, etc., in RTL (Register Transfer Level)

description of HDL (Hardware Description Language), since it is guaranteed that conditional branching is not explicitly simultaneous operation, processing within each condition is mapped to each context. Switching between contexts is performed, for example, by a signal from a control circuit implemented in other LUT (look up table).

In such a case, as shown in above described Figs. 3D to 3F, plural LUTs can be configured with one LUT. Specifically, in the case shown in Fig. 3D, eight 3-input 1-output LUTs can be configured with one LUT (in Fig. 3D, one 6-input 3-output LUT). In the case shown in Fig. 3E, four 4-input 1-output LUTs can be configured with one LUT, and in the case shown in Fig. 3F, two 5-input 1-output LUTs can be configured with one LUT.

Specifically, in the configuration shown in Fig. 3E, for example, as compared to conventional configuration using four 4-input 1-output LUTs, the circuit area ratio can be reduced to about $(1 \times 4) : 1.5$, that is, 1 : 0.375. Thus, reduction of implementation area (circuit area) of maximum about 62% can be achieved. In other words, the LUTs shown in Fig. 3E (LUTs configured with one 6-input 3-output LUT) can be configured in implementation area of about 32% of conventional LUTs (four 4-input 1-output LUTs), and can also substantially decrease the power consumption.

Also, if the case where an ALU circuit of 8 operations is implemented with conventional 4-input 1-output LUTs, is compared with the case where the 6-input 3-output LUT is used as 4-input 1-output LUT $\times$ 4 planes for implementing same ALU circuit, circuit area can be reduced to about 75%, and achieve considerable improvement in packaging efficiency.

Fig. 5 is a block diagram showing a 6-input 3-output LUT 7 as an example of LUT in FPGA according to the present invention in conjunction with the I/O signals. This corresponds to the 6-input 3-output LUT as shown in

Fig. 2 with six input signals A, B, C, D, E, F and three output signals Q, V, W added thereto.

Fig. 6 is a block diagram showing an example of internal configuration of the 6-input 3-output LUT shown in Fig. 5.

As shown in Fig. 6, the 6-input 3-output LUT 7 (121) is comprised of a mode changing memory 71, selectors 721 ~ 726, and 3-input 1-output LUT units (memory array) 731 ~ 738. The mode changing memory 71 stores 3 bits data X, Y, Z designated by a user so as to set the relation between 6 bit input A ~ F and 3 bit output Q, V, W in accordance with user's request.

A predetermined signal within 6 bit input signal is input to each selector (selector for selecting input signal) 721 ~ 725, so as to select input signal in accordance with data stored in the mode changing memory 71. That is, signals A, C are input to the selector 721, and signals B, D are input to selector 722, and one of the signals is selected by selection signal F0 (X, Y, Z) specified by data X, Y, Z, and is output, respectively. Similarly, signals A, D are input to the selector 723, and signals B, E are input to the selector 724, and signals C, F are input to the selector 725, and one of the signals is selected by selection signal F1 (X, Y, Z) specified by data X, Y, Z, and is output, respectively.

Each of 3-input 1-output LUT units 731 ~ 738 is comprised of an address decoder, a memory and a selector, as described later, and outputs 1 bit signal in response to 3 bit input signal, respectively. Thus, signals A, B, C are input to each of LUT units 731, 732, 734 ~ 736 and 738, and one of the signals A or C and one of the signals B or D selected by selection signal F0, and the signal C is input to the LUT unit 733, and one of the signals A or D, and one of the signals B or E, and one of the signals C or F, selected by the selection signal F1 is input to

the LUT unit 737. Output signals from the LUT units 731 ~ 738 are input to a selector (selector for selecting output signal) 726, and one of the signals is selected by selection signal F2 (D, E, F, X, Y, Z) specified by signals D, E, F and data X, Y, Z, and is output as signal V. The signal Q is the output signal from the LUT unit 731, and the signal W is the output signal from the LUT unit 737.

Fig. 7 is a block diagram showing an example of 3-input 1-output LUT unit 731 in the 6-input 3-output LUT 7 of Fig. 6. All of the 3-input 1-output LUT units 731 ~ 738 are of similar configuration.

The LUT unit 731 shown in Fig. 7 is comprised of an address decoder 7311, a selector 7312, and two sets of 4 bit memory unit groups M11 ~ M14, M21 ~ M24. The address decoder 7311 decodes 2 bit input signal A, B to designate each one of the memory unit groups M11 ~ M14 and M21 ~ M24, and further according to the input signal C, selects one of the sets M11 ~ M14 or M21 ~ M24 to output data.

Fig. 8 is a block diagram showing another example of 3-input 1-output LUT unit 731 in the 6-input 3-output LUT 7 of Fig. 6.

The LUT unit 731 shown in Fig. 8 is comprised of an address decoder 7313, and 8 bit memory unit groups M31 ~ M38. The address decoder 7313 decodes the 3 bit input signals A, B, C, to designate one of the memory unit groups M31 ~ M38, and output the data (Q).

The relation of the 3 bit data X, Y, Z, designated by the mode changing memory 71 in the 6-input 3-output LUT shown in Fig 6 as described above and the corresponding internal configurations (configuration modes) will be explained below with reference to Figs. 3A ~ 3F.

First, when, as shown in Fig. 3A, the 6-input 3-output LUT 7 (121) is set to the mode of three 2-input 1-

output LUTs, the selection signal F0 and F1 select an input "1" at each of the selectors 721, 722 and 723 ~ 725, and further, the selection signal F2 selects an input "2" at the selector 726.

5 That is, the user designates the 3 bit data X, Y, Z to be stored in the mode changing memory 71 such that the selection signal F0 (X, Y, Z) and F1 (X, Y, Z) selects an input "1" at each of the selectors 721, 722 and 723 ~ 725, and that the selection signal F2 (D, E, F, X, Y, Z) selects an input "2" at the selector 726.

10 Thus, by using the LUT unit 731 to which signals A, B, C are input and which outputs signal Q, the LUT unit 733 to which the signals C, D via the selectors 721, 722 and the direct signal C are input and which outputs the signal V via the selector 726, and the LUT unit 737 to which the signals D, E, F are input via the selectors 723 ~ 725 and which outputs the signal W, the three 2-input 1-output LUTs as shown in Fig. 3A can be configured. Although the input signal C in the LUT unit 731, one of the input signal C in the LUT unit 733, and the input signal D in the LUT unit 737 via the selector 723 are extra input signals in each of the LUT units, there is no problem about it.

25 Next, when, as shown in Fig. 3B, the 6-input 3-output LUT 7 is set to the mode of two 3-input 1-output LUTs, the 3 bit data X, Y, Z to be stored in the mode changing memory 71 is designated such that the selection signal F1 selects an input signal "1" at the selectors 723 ~ 725. By using the LUT unit 731 to which the signals A, B, C are input and which outputs the signal Q, and the LUT unit 737 to which the signals D, E, F are input via the selector 723 ~ 725 and which outputs the signal W, the two 3-input 1-output LUTs as shown in Fig. 3B can be configured.

35 When, as shown in Fig. 3C, the 6-input 3-output LUT

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is set to the mode of 6-input 1-output LUT, the selection signals F0 and F1 select an input "0" at each selector, and the selection signal F2 determines the value of the selector 726 from input signals D, E, F, and outputs the signal V. Thus, from 6 bit input of the signals A, B, C, and the signals D, E, F, 1 bit signal V is output.

As shown in Fig. 3D, when the 6-input 3-output LUT is set to the mode of 3-input 1-output LUT $\times$ 8 planes, the selection signals F0 and F1 select an input "0" at each selector, and the selection signal F2 determines the value of the selector 726 from the signals D, E, F, and outputs the signal V. In this case, the signals D, E, F, use plane switching signals.

As shown in Fig. 3E, when the 6-input 3-output LUT is set to the mode of 4-input 1-output LUT $\times$ 4 planes, the selection signals F0 and F1 select an input "0" at each selector, and the selection signal F2 determines the value of the selector 726 from the signals D, E, F, and outputs the signal V. In this case, the signal D is one of 4 bit input signals together with the signals A, B, C, and the signals E and F use plane switching signals.

As shown in Fig. 3F, when the 6-input 3-output LUT is set to the mode of 5-input 1-output LUT $\times$ 2 planes, the selection signals F0 and F1 select an input "0" at each selector, and the selection signal F2 determines the value of the selector 726 from the signals D, E, F, and outputs the signal V. In this case, the signal D and E are two of 5 bit input signals together with the signals A, B, C, and the signals F uses a plane switching signal.

As has been described above, according to the present embodiment, the 6-input 3-output LUT, for example, may be used in various modes of internal configuration by varying the values X, Y, Z of the mode changing memory.

Fig. 9 is a block diagram showing another example of internal configuration, which is different from the above

described internal configuration of 6-input 3-output LUT shown in Fig. 6.

As shown in Fig. 9, the 6-input 3-output LUT 8 (121) is comprised of a mode changing memory 81, selectors 821 ~ 826, and 3-input 2-output LUT units 831 ~ 834. The mode changing memory 81 stores 3 bit data X, Y, Z, designated by a user, so as to set the relation between 6 bit input A ~ F and 3 bit output Q, V, W in accordance with user's request.

Thus, in contrast to the above described 6-input 3-output LUT 7 shown in Fig. 6, which comprises eight 3-input 1-output LUT units 731 ~ 738, the present 6-input 3-output LUT 8 comprises four 3-input 2-output LUT units 831 ~ 834, and except for this, has substantially the same configuration.

3 bit data X, Y, Z, designated to the mode changing memory 81 of the LUT 8 shown in Fig. 9, selection signals F0 (X, Y, Z), F1 (X, Y, Z), and F2 (D, E, F, X, Y, Z), as well as the operation of selectors 821 ~ 826

(corresponding to the selectors 721 ~ 726) controlled by these selection signals F0, F1, F2, are the same as has been described with reference to Fig. 6 and Figs. 3A ~ 3F, and explanation thereof is therefore omitted.

Fig. 10 is a block diagram showing an example of 3-input 2-output LUT units in the 6-input 3-output LUT shown in Fig. 9. All of the 3-input 2-output LUT units 831 ~ 834 have the identical configuration.

The LUT unit 831 shown in Fig. 10 is comprised of an address decoder 8311, selectors 8312, 8313, and four sets of 4 bit memory unit group M41 ~ M44, M51 ~ M54, M61 ~ M64, M71 ~ M74. The address decoder 8311 decodes 2 bit input signal A, B to designate each one for the four sets of memory unit group M41 ~ M44, M51 ~ M54, M61 ~ M64, M71 ~ M74, and by the input signal C, selects and outputs the

data of one of the two sets of memory unit group M41 ~ M44 or M51 ~ M54 (output signal Q: the signal supplied to the input "0" of the selector 826), and data of one of the two sets of memory unit group M61 ~ M64 or M71 ~ M74 (the signal supplied to the input "1" of the selector 826).

Fig. 11 is a block diagram showing another example of 3-input 2-output LUT units in the 6-input 3-output LUT shown in Fig. 9.

The LUT unit 831 shown in Fig. 11 is comprised of an address decoder 8314, and two sets of 8 bit memory unit group M81 ~ M88 and M91 ~ M98. The address decoder 8314 decodes 3 bit input signal A, B, C to designate each one for the two sets of memory unit group M81 ~ M88 and M91 ~ M98, and outputs respective data (output signal Q: signal supplied to the input "0", and signal supplied to the input "1").

Fig. 12 is a block diagram showing still another example of 3-input 2-output LUT units in the 6-input 3-output LUT shown in Fig. 9.

The LUT unit 831 shown in Fig. 12 is comprised of an address decoder 8315, selectors 8316, 8317, and eight sets of 2 bit memory unit group M111, M121; M112, M122; ...; M118, M128. The address decoder 8315 decodes 1 bit input signal A to designate each one for the eight sets of memory unit group M111, M121 ~ M118, M128, and by 2 bit input signal B, C, selects and outputs the data of one set of the memory unit group M111, M121 ~ M114, M124 (output signal Q: the signal supplied to the input "0" of the selector 826), and the data of one set of the memory unit group M115, M125 ~ M118, M128 (signal supplied to the input "1" of the selector 826).

Fig. 13 is a block diagram showing an exemplary configuration of an ALU circuit (ALU 16) 90 of 8 operations. In Fig. 13, reference symbols G and H denote

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As shown in Fig. 13, the ALU circuit 90 is comprised of eight operation circuits consisting of OR circuit 91, AND circuit 92, XOR circuit 93, not circuit 94, + (addition) circuit 95, NE (Not Equal) circuit 96, GT (Greater Than) circuit 97 and SHIFT circuit 98 having 16 bit data G and H input therein, respectively, and a selector 99 for selecting the output from the eight operation circuits 91 to 98 in accordance with the command signal I, and outputs the output signal J portion corresponding to the command signal I.

Fig. 14 is a view showing the difference of the area ratio when the ALU 16 as shown in Fig. 13 is implemented with LUT used in conventional FPGA and in FPGA according

to the present invention (3 LUT ~ 7 LUT and 6-input 3-output LUT (3 LUT * 8 and 4 LUT * 4)). Fig. 15 is a view showing the difference of number of bits of configuration data when the ALU 16 as shown in Fig. 13 is implemented with LUT used in conventional FPGA and in FPGA according to the present invention. Vertical axis in Fig. 14 represents the area when the ALU 16 is configured using various LUTs, expressed as area ratio assuming the area of the case when configured with commonly used 4-input 1-output LUT (4 LUT) to be equal to 1. Vertical axis in Fig. 15 represents the number of bits of configuration data when the ALU 16 is configured using various LUTs.

As can be seen from Fig. 14, when the ALU 16 as shown in Fig. 13 is implemented with the 6-input 3-output LUT used in FPGA according to the present invention (3 LUT * 8 and 4 LUT * 4), for example, the area ratio is greatly reduced compared to the case where the same ALU 16 is implemented with LUT used in conventional FPGA (3 LUT ~ 7 LUT). More specifically, it can be seen that the case of 3 LUT * 8 where the 6-input 3-output LUT is implemented as 3-input 1-output LUT x 8 planes gives an area about 75% of that for the case where 4-input 1-output LUT (4 LUT) is used to implement the ALU 16 and gives the smallest area in conventional LUTs.

Further, as can be seen from Fig. 15, the number of bits of configuration data for the case where the ALU 16 is implemented with the 6-input 3-output LUT used in FPGA according to the present invention (3 LUT * 8 and 4 LUT * 4) is comparable to that for the case of 4 LUT that gives the smallest value among the conventional cases. Thus, although the 6-input 3-output LUT of the present invention requires 4 times as much configuration data as, for example, 4-input 1-output LUT, the number of bits of the configuration data can be made comparable. This is due to the fact that the conventional LUT constructs the selectors in output stage with LUTs while the present

In the above description, the 6-input 3-output LUT used in the FPGA according to the present invention is only an example, and the present invention can be equally applied to M-input N-output (e.g., 8-input 4-output) LUT. Further, it is to be understood that configuration of the 6-input 3-output LUT itself, for example, is not limited to the eight 3-input 1-output LUT units shown in Fig. 6, or to the four 3-input 2-output LUT units shown in Fig. 9, and various modification is possible within the scope of the invention.

Many different embodiments of the present invention may be constructed without departing from the spirit and scope of the present invention, and it should be understood that the present invention is not limited to the specific embodiments described in this specification, except as defined in the appended claims.

What is claimed is:

1. A look up table of M inputs and N outputs,
comprising:

5 a plurality of LUT units; and
an internal configuration control circuit
controlling an internal configuration of said plurality
of LUT units.

2. The look up table as claimed in claim 1,
wherein said internal configuration control circuit
10 comprises:

a plurality of selectors selecting I/O
signals of said plurality of LUT units; and
a selector control circuit controlling
said selectors and defining the internal configuration of
15 said plurality of LUT units.

3. The look up table as claimed in claim 2,
wherein said selector control circuit comprises a memory,
and controls said plurality of selectors in accordance
with data stored in said memory.

20 4. The look up table as claimed in claim 3,
wherein said plurality of selectors include:

an input signal selector provided at an
input of at least one of said LUT units to select an
input signal; and
25 an output signal selector provided at an
output of said LUT units selecting an output signal, said
input signal selector and said output signal selector
being controlled in accordance with the data stored in
said memory.

30 112 5. The look up table as claimed in claim 3,
wherein said plurality of selectors include:

an input signal selector provided at an
input of at least one of said LUT units to select an
input signal; and
35 an output signal selector provided at an
output of said LUT units selecting an output signal, said
input signal selector and said output signal selector

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being controlled in accordance with the input signal.

6. The look up table as claimed in claim 1, wherein said look up table of M inputs and N outputs is a 6-input 3-output look up table.

5 7. The look up table as claimed in claim 6, wherein said 6-input 3-output look up table comprises eight 3-input 1-output LUT units.

8. The look up table as claimed in claim 6, wherein said 6-input 3-output look up table comprises
10 four 3-input 2-output LUT units.

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9. A programmable logic circuit device comprising:
a plurality of logic blocks;
a plurality of routing wires connected to
each of said logic blocks;
15 a plurality of switch circuits provided at an intersection of each of said routing wires;
a plurality of connection blocks provided between an I/O line of each of said logic blocks and each of said routing wires; and
20 an I/O block performing an input/output operation with external equipment, wherein each of said logic blocks has a look up table of M inputs and N outputs, comprising:
a plurality of LUT units; and
25 an internal configuration control circuit controlling an internal configuration of said plurality of LUT units.

10. The programmable logic circuit device as claimed in claim 9, wherein said internal configuration control circuit comprises:
30 a plurality of selectors selecting I/O signals of said plurality of LUT units; and

a selector control circuit controlling said selectors and defining the internal configuration of
35 said plurality of LUT units.

11. The programmable logic circuit device as claimed in claim 10, wherein said selector control

↗ circuit comprises a memory, and controls said plurality of selectors in accordance with data stored in said memory.

12. The programmable logic circuit device as
5 claimed in claim 11, wherein said plurality of selectors include:

an input signal selector provided at an input of at least one of said LUT units to select an input signal; and

10 an output signal selector provided at an output of said LUT units selecting an output signal, said input signal selector and said output signal selector being controlled in accordance with the data stored in said memory.

15 ✓ 13. The programmable logic circuit device as claimed in claim 11, wherein said plurality of selectors include:

an input signal selector provided at an input of at least one of said LUT units to select an
20 input signal; and

an output signal selector provided at an output of said LUT units selecting an output signal, said input signal selector and said output signal selector being controlled in accordance with the input signal.

25 14. The programmable logic circuit device as claimed in claim 9, wherein said look up table of M inputs and N outputs is a 6-input 3-output look up table.

30 15. The programmable logic circuit device as claimed in claim 14, wherein said 6-input 3-output look up table comprises eight 3-input 1-output LUT units.

16. The programmable logic circuit device as claimed in claim 14, wherein said 6-input 3-output look up table comprises four 3-input 2-output LUT units.

35 17. A method of configuring a look up table of M inputs and N outputs, comprising the steps of:

providing a plurality of LUT units; and
selectively controlling I/O signals of

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said plurality of LUT units to set a predetermined mode of an internal configuration.

18. The method of configuring a look up table as claimed in claim 17, wherein the I/O signals of said plurality of LUT units are selectively controlled in accordance with data stored in the corresponding look up table.

19. The method of configuring a look up table as claimed in claim 17, wherein an input signal input to at least one of said LUT units and an output signal output from said LUT unit are selectively controlled in accordance with data stored in the corresponding look up table.

20. The method of configuring a look up table as claimed in claim 17, wherein an input signal input to at least one of said LUT units and an output signal output from said LUT unit are selectively controlled in accordance with a predetermined function of the input signal.

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PROGRAMMABLE LOGIC CIRCUIT DEVICE HAVING LOOK UP TABLE
ENABLING TO REDUCE IMPLEMENTATION AREA

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ABSTRACT OF THE DISCLOSURE

10 A programmable logic circuit device has a plurality
of logic blocks, a plurality of routing wires, a
plurality of switch circuits, a plurality of connection
blocks, and an I/O block performing an input/output
operation with external equipment. The routing wires are
connected to each of the logic blocks, the switch
15 circuits are provided at an intersection of each of the
routing wires, and the connection blocks are provided
between an I/O line of each of the logic blocks and each
of the routing wires. Each of the logic blocks has a
look up table of M inputs and N outputs, which has a
20 plurality of LUT units; and an internal configuration
control circuit controlling an internal configuration of
the plurality of LUT units.

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Declaration and Power of Attorney For Patent Application**特許出願宣言書及び委任状****Japanese Language Declaration****日本語宣言書**

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

PROGRAMMABLE LOGIC CIRCUIT DEVICE

HAVING LOOK UP TABLE ENABLING
TO REDUCE IMPLEMENTATION AREA

上記発明の明細書（下記の欄でxが印がついていない場合は、本書に添付）は、

the specification of which is attached hereto unless the following box is checked:

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国際出願番号を _____ とし、
(該当する場合) _____ に訂正されました。☐ was filed on _____
as United States Application Number or
PCT International Application Number
_____ and was amended on
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the above identified specification, including the claims, as
amended by any amendment referred to above.私は、連邦規則法典第37編第1条56項に定義されると
おり、特許資格の有無について重要な情報を開示する義務が
あることを認めます。I acknowledge the duty to disclose information which is material to
patentability as defined in Title 37, Code of Federal Regulations,
Section 1.56.

Japanes Language Declarati n (日本語宣言書)

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Prior Foreign Application(s)

外国での先行出願 2001-199644 (Pat. Appln.)	Japan
(Number) (番号)	(Country) (国名)
(Number) (番号)	(Country) (国名)

私は、第35編米国法典119条(e)項に基づいて下記の米国外特許出願規定に記載された権利をここに主張いたします。

(Application No.) (出願番号)	(Filing Date) (出願日)
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(Application No.) (出願番号)	(Filing Date) (出願日)
(Application No.) (出願番号)	(Filing Date) (出願日)

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I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Priority Not Claimed
優先権主張なし

29/June/2001
(Day/Month/Year Filed)
(出願年月日)

(Day/Month/Year Filed)
(出願年月日)

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)
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I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of application.

(Status: Patented, Pending, Abandoned)
(現況: 特許許可済、係属中、放棄済)

(Status: Patented, Pending, Abandoned)
(現況: 特許許可済、係属中、放棄済)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Japan se Language D clarification (日本語宣言書)

委任状: 私は下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁理士または代理人として、下記の者を指名いたします。(弁理士、または代理人の氏名及び登録番号を明記のこと)

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PATENT APPLICATION SERIAL NO. _____

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

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PATENT APPLICATION FEE DETERMINATION RECORD

Effective October 1, 2001

Application or Docket Number

101 83 590

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	20	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	20 minus 20 =	*
INDEPENDENT CLAIMS	3 minus 3 =	*
MULTIPLE DEPENDENT CLAIM PRESENT ☐		

* If the difference in column 1 is less than zero, enter "0" in column 2

CLAIMS AS AMENDED - PART II

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus	**
Independent	*	Minus	***
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐			

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus	**
Independent	*	Minus	***
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐			

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT C	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus	**
Independent	*	Minus	***
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐			

SMALL ENTITY TYPE ☐

OR OTHER THAN SMALL ENTITY

RATE	FEE
BASIC FEE	370.00
X\$ 9=	
X42=	
+140=	
TOTAL	

RATE	FEE
BASIC FEE	740.00
X\$18=	
X84=	
+280=	
TOTAL	790

SMALL ENTITY

OR OTHER THAN SMALL ENTITY

RATE	ADDITIONAL FEE
X\$ 9=	
X42=	
+140=	
TOTAL	

RATE	ADDITIONAL FEE
X\$18=	
X84=	
+280=	
TOTAL	

RATE	ADDITIONAL FEE
X\$ 9=	
X42=	
+140=	
TOTAL	

RATE	ADDITIONAL FEE
X\$18=	
X84=	
+280=	
TOTAL	

RATE	ADDITIONAL FEE
X\$ 9=	
X42=	
+140=	
TOTAL	

RATE	ADDITIONAL FEE
X\$18=	
X84=	
+280=	
TOTAL	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

Toshinori SUEYOSHI, et al.

Application No.:

Group Art Unit:

Filed: June 28, 2002

Examiner:

For: PROGRAMMABLE LOGIC CIRCUIT DEVICE HAVING LOOK UP TABLE ENABLING
TO REDUCE IMPLEMENTATION AREA



INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

In accordance with the duty of disclosure provisions of 37 CFR § 1.56, there is hereby provided certain information which the Examiner may consider material to the examination of the subject U.S. patent application. It is requested that the Examiner make this information of record if it is deemed material to the examination of the subject application.

1. Enclosures accompanying this Information Disclosure Statement are:

- 1a. ☒ Form PTO-1449.
- 1b. ☒ Copies of IDS citations.
- 1c. ☐ An English language copy of search report(s) from a counterpart foreign application or a PCT International Search Report.
- 1d. ☐ English language translation (complete or relevant portion(s)) attached to each non-English language publication.
- 1e. ☐ Explanations of Relevancy of References (ATTACHMENT 1(e), hereto) for providing a concise explanation of each non-English publication.

2. ☐ In accordance with 37 CFR § 1.98, a concise explanation of what is presently understood to be the relevance of each non-English language publication is

(Check appropriate Items 2a, 2b, 2c and/or 2d)

- 2a. ☐ satisfied because all non-English language publications were cited on the enclosed "English-language version of the search report or action which indicates the degree of relevance found by the foreign office". (See MPEP 609, Minimum Requirements for an Information Disclosure Statement, Part A(3): Concise Explanation of Relevance, pp. 600-100 to 600-101, Rev. 1, Feb. 2000.)
- 2b. ☐ set forth in the application.

- 2c. ☐ satisfied because an English language translation (complete or relevant portion(s)) is attached to each non-English language publication.
- 2d. ☐ enclosed as Attachment 1(e), hereto.
3. No admission is made that the information cited in this Statement is, or is considered to be, material to patentability nor a representation that a search has been made (other than search report(s) from a counterpart foreign application or a PCT International Search Report, if submitted herewith). 37 CFR §§ 1.97(g) and (h).

Respectfully submitted,

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By: 

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

Toshinori SUEYOSHI, et al.

Application No.:

Group Art Unit:

Filed: June 28, 2002

Examiner:

For: PROGRAMMABLE LOGIC CIRCUIT DEVICE HAVING LOOK UP TABLE ENABLING
TO REDUCE IMPLEMENTATION AREA

**SUBMISSION OF CERTIFIED COPY OF PRIOR FOREIGN
APPLICATION IN ACCORDANCE
WITH THE REQUIREMENTS OF 37 C.F.R. § 1.55**

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

In accordance with the provisions of 37 C.F.R. § 1.55, the applicant(s) submit(s)
herewith a certified copy of the following foreign application:

Japanese Patent Application No(s). 2001-199644

Filed: June 29, 2001

It is respectfully requested that the applicant(s) be given the benefit of the foreign filing
date(s) as evidenced by the certified papers attached hereto, in accordance with the
requirements of 35 U.S.C. § 119.

Respectfully submitted,

STAAS & HALSEY LLP

Date: June 28, 2002

By: 

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日 本 国 特 許 庁
JAPAN PATENT OFFICE

別紙添付の書類に記載されている事項は下記の出願書類に記載されている事項と同一であることを証明する。

This is to certify that the annexed is a true copy of the following application as filed with this Office

出 願 年 月 日

Date of Application:

2001年 6月29日

出 願 番 号

Application Number:

特願2001-199644

[ST.10/C]:

[JP2001-199644]

出 願 人

Applicant(s):

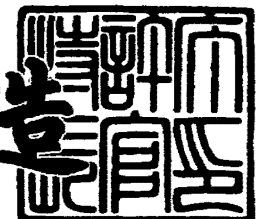
株式会社半導体理工学研究センター



2002年 1月11日

特許庁長官
Commissioner,
Japan Patent Office

及川耕造



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【発明の名称】 ルックアップテーブル、ルックアップテーブルを備える
プログラマブル論理回路装置、および、ルックアップテ
ーブルの構成方法

【請求項の数】 11

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【プルーフの要否】 要

【書類名】 明細書

【発明の名称】 ルックアップテーブル、ルックアップテーブルを備えるプログラマブル論理回路装置、および、ルックアップテーブルの構成方法

【特許請求の範囲】

【請求項1】 M入力N出力のルックアップテーブルであって、
複数のLUTユニットと、

該複数のLUTユニットによる内部構成を制御する内部構成制御手段とを備えることを特徴とするルックアップテーブル。

【請求項2】 請求項1に記載のルックアップテーブルにおいて、前記内部構成制御手段は、

前記複数のLUTユニットの入出力信号を選択する複数のセレクトと、

該各セレクトを制御して前記複数のLUTユニットによる構成を規定するセレクト制御手段とを備えることを特徴とするルックアップテーブル。

【請求項3】 請求項2に記載のルックアップテーブルにおいて、前記セレクト制御手段はメモリを備え、該メモリに格納するデータに応じて前記複数のセレクトを制御することを特徴とするルックアップテーブル。

【請求項4】 請求項3に記載のルックアップテーブルにおいて、前記セレクトは、

少なくとも1つの前記LUTユニットの入力に設けられて入力信号の選択を行う入力信号選択用セレクトと、

前記LUTユニットの出力に設けられて出力信号の選択を行う出力信号選択用セレクトとを備え、該入力信号選択用セレクトおよび該出力信号選択用セレクトは、前記メモリに格納するデータおよび／または前記入力信号に応じて制御されることを特徴とするルックアップテーブル。

【請求項5】 請求項1に記載のルックアップテーブルにおいて、前記M入力N出力のルックアップテーブルは、6入力3出力のルックアップテーブルであることを特徴とするルックアップテーブル。

【請求項6】 請求項5に記載のルックアップテーブルにおいて、前記6入力3出力のルックアップテーブルは、8つの3入力1出力LUTユニットを備え

ることを特徴とするルックアップテーブル。

【請求項 7】 請求項 5 に記載のルックアップテーブルにおいて、前記 6 入力 3 出力のルックアップテーブルは、4 つの 3 入力 2 出力 LUT ユニットの備えることを特徴とするルックアップテーブル。

【請求項 8】 複数の論理ブロックと、該各論理ブロックに接続される複数の配線と、該各配線の交差個所に設けられた複数のスイッチ手段と、該各論理ブロックの入出力線と前記各配線との間に設けられた接続ブロックと、外部との入出力を行う I/O ブロックとを備えるプログラマブル論理回路装置であって、

前記論理ブロックは、請求項 1 ～ 7 のいずれか 1 項に記載のルックアップテーブルを備えることを特徴とするプログラマブル論理回路装置。

【請求項 9】 M 入力 N 出力のルックアップテーブルを構成する方法であって、

複数の LUT ユニットの準備し、

該複数の LUT ユニットの入出力信号を選択制御して所定の内部構成モードを設定するようにしたことを特徴とするルックアップテーブルの構成方法。

【請求項 10】 請求項 9 に記載のルックアップテーブルの構成方法において、前記複数の LUT ユニットの入出力信号は、当該ルックアップテーブル内に格納されるデータに応じて選択制御されることを特徴とするルックアップテーブルの構成方法。

【請求項 11】 請求項 9 に記載のルックアップテーブルの構成方法において、少なくとも 1 つの前記 LUT ユニットに入力する信号、および、該 LUT ユニットが出力する信号は、それぞれ当該ルックアップテーブル内に格納されるデータおよび／または入力信号の所定の関数により選択制御されることを特徴とするルックアップテーブル。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】

本発明は実装面積の削減が可能なルックアップテーブルの構成技術に関する。

近年、プログラマブル論理回路装置は、内部回路を電氣的にプログラムするこ

とでユーザの様々な要求に応じた論理回路を実現することができるデバイスとして注目されている。このプログラマブル論理回路装置は、P L D (Programmable Logic Device) 或いはF P G A (Field Programmable Gate Array) として知られているが、最近では、ハードウェアの試作に対する利用を越えて、それ自体で様々な機能を有する大規模な回路（例えば、マイクロプロセッサ等）を構成するためにも使用されるようになって来ている。このようなプログラマブル論理回路装置は、ルックアップテーブル（L U T : Look Up Table）を主要な構成要素としているが、このL U Tの回路面積の削減が強く要望されている。

【0 0 0 2】

【従来の技術】

プログラマブル論理回路装置（P L DやF P G A）の主要な要素であるルックアップテーブル（L U T）はメモリから構成されており、任意の論理回路を実装することが可能である。このようなF P G Aの基本的な構成は、従来、例えば、米国特許第4 7 0 6 2 1 6号および第4 8 7 0 3 0 2号に提案されている。また、F P G Aにおけるマルチコンテキスト（multi-context）および複数のL U Tのクラスタ化に関しては、例えば、米国特許第5 7 7 8 4 3 9号および第5 9 0 5 3 8 5号等に提案されている。さらに、F P G A等に使用するL U Tに対する評価（例えば、機能性と面積に関する評価並びに性能評価、および、クラスタ化の評価等）に関しては、例えば、J. Rose et al., "Architecture of Field-Programmable Gate Arrays: The Effect of Logic Block Functionality on Area Efficiency", IEEE J. Solid-State Circuits, vol. 25, no. 5, pp. 1217-1225, Oct. 1990、J. Rose et al., "The Effect of Logic Block Architecture on FPGA Performance", IEEE J. Solid-State Circuits, vol. 27, no. 3, pp. 281-287, Mar. 1992、および、E. Ahmed et al., "The Effect of LUT and Cluster Size on Deep-Submicron FPGA Performance and Density", FPGA 2000, Monterey, CA USA, 2000に研究成果が示されている。

【0 0 0 3】

プログラマブル論理回路装置において、実装できる論理回路の入力信号のビット数MはL U Tを構成するメモリのアドレスのビット数に対応し、また、出力信

号のビット数Nはメモリの出力ビット数に対応している。したがって、1つのLUTに実装できる論理回路は、任意のM入力N出力の論理回路となる。本明細書では、このようなLUTをM入力N出力LUTと表す。

【0004】

【発明が解決しようとする課題】

従来、例えば、FPGAにおいて、LUTの入力数Mおよび出力数Nは共に固定値であり、任意の論理回路は、M入力N出力の回路単位に分割され、複数のLUTを用いて実装されるようになっている。

そのため、従来のFPGAでは、回路分割により入力数がMビット未満の回路が生じた場合、この入力数がMビット未満の回路に対しても1つのLUTを割り当てなければならず、実装面積の増加をもたらす原因になっている。

【0005】

本発明は、上述した従来のプログラマブル論理回路装置が有する課題に鑑み、ルックアップテーブル（LUT）すなわちプログラマブル論理回路装置の回路面積を削減することを主たる目的とする。さらに、本発明は、プログラマブル論理回路装置の消費電力の低減も目的とする。

【0006】

【課題を解決するための手段】

本発明の第1の形態によれば、M入力N出力のルックアップテーブルであって、複数のLUTユニットと、該複数のLUTユニットによる内部構成を制御する内部構成制御手段とを備えることを特徴とするルックアップテーブルが提供される。

【0007】

本発明の第2の形態によれば、複数の論理ブロックと、該各論理ブロックに接続される複数の配線と、該各配線の交差個所に設けられた複数のスイッチ手段と、該各論理ブロックの入出力線と前記各配線との間に設けられた接続ブロックと、外部との入出力を行うI/Oブロックとを備えるプログラマブル論理回路装置であって、前記論理ブロックは、M入力N出力のルックアップテーブルであって、複数のLUTユニットと、該複数のLUTユニットによる内部構成を制御する

内部構成制御手段とを有するルックアップテーブルを備えることを特徴とするプログラマブル論理回路装置が提供される。

【0008】

本発明の第3の形態によれば、M入力N出力のルックアップテーブルを構成する方法であって、複数のLUTユニットを準備し、該複数のLUTユニットの入出力信号を選択制御して所定の内部構成モードを設定するようにしたことを特徴とするルックアップテーブルの構成方法が提供される。

本発明によれば、LUT内にモード変更用のメモリを設けることにより、従来のFPGAで使用されるLUTと異なり、複数の入力数および出力数を有するLUTを実現することができる。これにより、分割された回路が必要とする入力信号数に適したLUTで構成することが可能となり、実装面積の増加を防ぐことができる。また、同時に動作しない回路を同一のLUT内に重ね合わせて実装し、これらを切り替えながら動作させることで、実装面積だけでなく消費電力も大幅に削減することができる。

【0009】

【発明の実施の形態】

以下、本発明に係るルックアップテーブル、ルックアップテーブルを備えるプログラマブル論理回路装置、および、ルックアップテーブルの構成方法を添付図面に従って詳述する。

図1は本発明が適用されるFPGAの一例を示すブロック図である。図1において、参照符号100はプログラマブル論理回路装置の一例としてのFPGA、101はI/Oブロック、102は論理ブロック（CLB：Configurable Logic Block）、103は接続ブロック（C）、104はスイッチマトリクス（S）、そして、105は配線を示している。

【0010】

図1に示されるように、FPGA100は、アレー状に配置された論理ブロック（CLB）102、これらCLB102を取り囲む配線（回線領域）105、および、外部との入出力を行うI/Oブロック101を備えて構成される。各配線105の交差個所には、それらを接続するためのスイッチマトリクス（S）1

04が配置され、さらに、各CLB102の入出力線と配線105との間にはそれぞれ接続ブロック(C)103が配置されている。各CLB102は、ルックアップテーブル(LUT)121、ラッチ122、および、セクタ123を備えて構成される。本発明は、主としてLUT121の構成に関するものである。

【0011】

図2はFPGAにおけるLUTの一例としての6入力3出力LUTを示すブロック図であり、図1におけるLUT121の一例を示すものである。すなわち、図2に示すLUTは、M入力N出力LUTにおいて、 $M=6$ 、 $N=3$ の場合の構成に対応するものである。なお、MおよびNの値に関して、 $M=6$ 、 $N=3$ は単なる一例であり、他の様々な値の場合もあり、さらに、 $M=N$ 、或いは、 $M<N$ となる場合もある。

【0012】

図3は図2に示す6入力3出力LUTの内部構成モードを示すブロック図であり、後に詳述するように、モード変更用メモリ(71)の値(X, Y, Z)を変えることで、6入力3出力LUTを図3(a)～図3(f)に示すような内部構成に設定することができるのを示している。

具体的に、図3(a)は、6入力3出力LUTを3個の2入力1出力LUTとしてモード設定した場合を示している。例えば、従来のFPGA(従来、4入力1出力LUTを単位として使用されている)において、3個の2入力1出力回路をLUTに割り当てるには3つのLUT(4入力1出力LUT)を必要とするが、図3(a)に示す構成では、1つの6入力3出力LUTだけで十分である。

【0013】

ところで、配線の領域を含む4入力1出力LUTと6入力3出力LUTの面積比は、1:1.5程度である。したがって、図3(a)に示す構成は、例えば、3つの4入力1出力LUTを使用する従来例に対して、回路の実装面積比を $(1 \times 3) : 1.5$ 、すなわち、1:0.5程度にすることができ、最大約50%の面積の削減が実現できる。

【0014】

また、図3(b)は、2個の3入力1出力LUTとしてモード設定した場合を

示す。この場合、例えば、2つの4入力1出力LUTを使用する従来例に対して、回路の実装面積比を $(1 \times 2) : 1.5$ 、すなわち、 $1 : 0.75$ 程度にすることができ、最大25%の面積の削減が実現できる。

さらに、図3(c)は、6入力3出力LUTを6入力1出力LUTとしてモードを設定した場合を示す。

【0015】

図3(d)は、3入力1出力LUT×8プレーンとしてモード設定した場合を示し、図3(e)は、4入力1出力LUT×4プレーンとしてモードを設定した場合を示し、そして、図3(f)は、5入力1出力LUT×2プレーンとしてモード設定した場合を示す。

図4はルックアップテーブルにおける回路のマッピング方法の一例を説明するための図であり、上記図3(d)～図3(f)のモード設定が可能な理由を示すものである。

【0016】

図4に示されるように、例えば、HDL (Hardware Description Language) におけるRTL (Register Transfer Level) 記述内のif～, else; case等の制御構造を利用したマッピング方法においては、条件分岐は明示的に同時動作でないことが保証されているため、各条件内の処理を各コンテキストにマッピングする。なお、各コンテキストの切り替えは、例えば、他のLUT (ルックアップテーブル) に実装された制御回路からの信号で行う。

【0017】

このような場合には、上述した図3(d)～図3(f)に示されるように、複数のLUTを1つのLUTで構成することができる。具体的に、図3(d)の場合には、8つの3入力1出力LUTを1つのLUT (図3(d)の場合には、1つの6入力3出力LUT) で構成することができる。また、図3(e)の場合には、4つの4入力1出力LUTを1つのLUTで構成することができ、さらに、図3(f)の場合には、2つの5入力1出力LUTを1つのLUTで構成することができる。

【0018】

具体的に、図 3 (e) に示す構成は、例えば、4 つの 4 入力 1 出力 LUT を使用する従来例に対して、回路の実装面積比を $(1 \times 4) : 1.5$ 、すなわち、 $1 : 0.375$ 程度にすることができ、最大約 62 % の面積の削減が実現できる。換言すると、図 3 (e) に示す実施例の LUT (1 個の 6 入力 3 出力 LUT で構成した LUT) は、従来の LUT (4 個の 4 入力 1 出力 LUT で構成した LUT) の約 32 % の実装面積で構成することができ、さらに、消費電力も大幅に低減することができる。

【0019】

また、例えば、8 オペレーションの ALU 回路を、従来の 4 入力 1 出力 LUT に実装した場合と、図 3 (e) に示すような 6 入力 3 出力 LUT を 4 入力 1 出力 LUT $\times 4$ プレーンとして使用し、これに実装した場合とを比較すると、回路実装面積を約 75 % にして実装効率の向上を実現することができる。

図 5 は本発明に係る FPGA における LUT の一例としての 6 入力 3 出力 LUT 7 を入出力信号と共に示すブロック図であり、図 2 に示す 6 入力 3 出力 LUT 121 に対して 6 つの入力信号 A, B, C, D, E, F と 3 つの出力信号 Q, V, W を追加したものに相当する。

【0020】

図 6 は図 5 に示す 6 入力 3 出力 LUT の内部構成の一例を示すブロック図である。

図 6 に示されるように、6 入力 3 出力 LUT 7 (121) は、モード変更用メモリ 71、セクタ 721 ~ 726、および、3 入力 1 出力 LUT ユニット (メモリアレイ) 731 ~ 738 を備えている。モード変更用メモリ 71 は、ユーザにより指定された 3 ビットのデータ X, Y, Z を格納するようになっており、6 ビットの入力 A ~ F と 3 ビットの出力 Q, V, W との関係をユーザの要求に応じて設定するようになっている。

【0021】

各セクタ (入力信号選択用セクタ) 721 ~ 725 には、6 ビットの入力信号内の所定の信号が入力され、それぞれモード変更用メモリ 71 に格納されたデータ X, Y, Z に応じて入力信号の選択を行うようになっている。すなわち、

セレクタ 7 2 1 には信号 A, C が入力され、また、セレクタ 7 2 2 には信号 B, D が入力され、それぞれデータ X, Y, Z により規定される選択信号 F 0 (X, Y, Z) により一方の信号が選択されて出力される。同様に、セレクタ 7 2 3 には信号 A, D が入力され、また、セレクタ 7 2 4 には信号 B, E が入力され、さらに、セレクタ 7 2 5 には信号 C, F が入力され、それぞれデータ X, Y, Z により規定される選択信号 F 1 (X, Y, Z) により一方の信号が選択されて出力される。

【 0 0 2 2 】

各 3 入力 1 出力 LUT ユニット 7 3 1 ~ 7 3 8 は、後述するように、アドレスデコーダ、メモリ、および、セレクタを備え、それぞれ 3 ビットの入力信号に応じて 1 ビットの信号を出力する。すなわち、各 LUT ユニット 7 3 1, 7 3 2, 7 3 4 ~ 7 3 6 および 7 3 8 には、それぞれ信号 A, B, C が入力され、また、LUT ユニット 7 3 3 には、選択信号 F 0 により選択された信号 A または C の一方と信号 B または D の一方、および、信号 C が入力される。さらに、LUT ユニット 7 3 7 には、選択信号 F 1 により選択された信号 A または D の一方、信号 B または E の一方、および、信号 C または F の一方が入力される。そして、LUT ユニット 7 3 1 ~ 7 3 8 の出力信号はセレクタ（出力信号選択用セレクタ）7 2 6 に入力され、信号 D, E, F およびデータ X, Y, Z により規定される選択信号 F 2 (D, E, F, X, Y, Z) により 1 つの信号が選択され、信号 V として出力される。なお、信号 Q は、LUT ユニット 7 3 1 の出力とされ、また、信号 W は、LUT ユニット 7 3 7 の出力とされている。

【 0 0 2 3 】

図 7 は図 6 の 6 入力 3 出力 LUT 7 における 3 入力 1 出力 LUT ユニット 7 3 1 の一例を示すブロック図である。なお、各 3 入力 1 出力 LUT ユニット 7 3 1 ~ 7 3 8 は全て同様の構成とされている。

図 7 に示す LUT ユニット 7 3 1 は、アドレスデコーダ 7 3 1 1、セレクタ 7 3 1 2、および、2 組の 4 ビットで構成されたメモリユニット群 M 1 1 ~ M 1 4, M 2 1 ~ M 2 4 を備えている。アドレスデコーダ 7 3 1 1 は、2 ビットの入力信号 A, B をデコードしてメモリユニット群 M 1 1 ~ M 1 4 および M 2 1 ~ M 2

4の各1つを指定し、さらに、入力信号Cによって、メモリユニット群M11～M14またはM21～M24の一方の組を選択してデータを出力する。

【0024】

図8は図6の6入力3出力LUT7における3入力1出力LUTユニット731の他の例を示すブロック図である。

図8に示すLUTユニット731は、アドレスデコーダ7313、および、8ビットのメモリユニット群M31～M38を備えている。アドレスデコーダ7313は、3ビットの入力信号A、B、Cをデコードしてメモリユニット群M31～M38の1つを指定してそのデータ(Q)を出力する。

【0025】

上述した図6に示す6入力3出力LUTにおけるモード変更用メモリ71に指定された3ビットデータX、Y、Zと、それに対応した内部構成(設定モード)との関係を図3(a)～図3(f)に対応させて説明する。

まず、図3(a)に示すように、6入力3出力LUT7(121)を3個の2入力1出力LUTとしてモード設定する場合、選択信号F0およびF1は各セクタ721、722および723～725において入力『1』を選択し、さらに、選択信号F2はセクタ726において入力『2』を選択する。

【0026】

すなわち、ユーザは、選択信号F0(X、Y、Z)およびF1(X、Y、Z)が各セクタ721、722および723～725における入力『1』を選択するように、且つ、選択信号F2(D、E、F、X、Y、Z)がセクタ726における入力『2』を選択するように、モード変更用メモリ71に格納する3ビットデータX、Y、Zを指定する。

【0027】

そして、信号A、B、Cが入力されて信号Qを出力するLUTユニット731、セクタ721、722を介した信号C、Dおよび直接の信号Cが入力されてセクタ726を介して信号Vを出力するLUTユニット733、および、セクタ723～725を介した信号D、E、Fが入力されて信号Wを出力するLUTユニット737を使用することで、図3(a)に示す3個の2入力1出力LUT

Tとして構成することができる。なお、LUTユニット731における入力信号C、LUTユニット733における一方の入力信号C、および、LUTユニット737におけるセクタ723を介した入力信号Dは、各LUTユニットにおいて余分な入力信号となっているが、問題となることはない。

【0028】

次に、図3（b）に示すように、6入力3出力LUT7を2個の3入力1出力LUTとしてモード設定する場合、選択信号F1はセクタ723～725における入力『1』を選択するようにモード変更用メモリ71に格納する3ビットデータX、Y、Zを指定する。そして、信号A、B、Cが入力されて信号Qを出力するLUTユニット731、および、セクタ723～725を介した信号D、E、Fが入力されて信号Wを出力するLUTユニット737を使用することで、図3（b）に示す2個の3入力1出力LUTとして構成することができる。

【0029】

図3（c）に示すように、6入力3出力LUTを6入力1出力LUTとしてモード設定する場合には、選択信号F0およびF1は各セクタにおける入力『0』を選択し、選択信号F2は入力信号D、E、Fによってセクタ726の値を決定し、信号Vを出力する。すなわち、信号A、B、Cと信号D、E、Fの6ビット入力により、1ビットの信号Vを出力する。

【0030】

図3（d）に示すように、6入力3出力LUTを3入力1出力LUT×8プレーンとしてモード設定する場合には、選択信号F0およびF1は各セクタにおける入力『0』を選択し、選択信号F2は信号D、E、Fによってセクタ726の値を決定し、信号Vを出力する。この場合、信号D、E、Fはプレーン切り替え信号が使用される。

【0031】

図3（e）に示すように、6入力3出力LUTを4入力1出力LUT×4プレーンとしてモード設定する場合にも、選択信号F0およびF1は各セクタにおける入力『0』を選択し、選択信号F2は信号D、E、Fによってセクタ726の値を決定し、信号Vを出力する。この場合、信号Dは、信号A、B、Cと共

に4ビットの入力信号の1つであり、また、信号EおよびFはプレーン切り替え信号が使用されることになる。

【0032】

図3(f)に示すように、6入力3出力LUTを5入力1出力LUT×2プレーンとしてモード設定する場合には、選択信号F0およびF1は各セクタにおける入力『0』を選択し、選択信号F2は信号D、E、Fによってセクタ726の値を決定し、信号Vを出力する。この場合、信号DおよびEは、信号A、B、Cと共に5ビットの入力信号の2つであり、また、信号Fはプレーン切り替え信号が使用されることになる。

【0033】

上述したように、本実施例によれば、例えば、6入力3出力LUTを、モード変更用メモリ71の値X、Y、Zを変えることにより様々な内部構成モードとして使用することができる。

図9は図5に示す6入力3出力LUTの内部構成の他の例を示すブロック図であり、前述した図6とは異なる6入力3出力LUTの内部構成の例を示すものである。

【0034】

図9に示されるように、6入力3出力LUT8(121)は、モード変更用メモリ81、セクタ821～826、および、3入力2出力LUTユニット831～834を備えている。モード変更用メモリ81は、ユーザにより指定された3ビットのデータX、Y、Zを格納するようになっており、6ビットの入力A～Fと3ビットの出力Q、V、Wとの関係をユーザの要求に応じて設定するようになっている。

【0035】

すなわち、上述した図6に示す6入力3出力LUT7が8つの3入力1出力LUTユニット731～738を備えていたのに対して、図9に示す本6入力3出力LUT8は、4つの3入力2出力LUTユニット831～834を備えている点を除き、他は実質的に同様の構成とされている。

なお、図9に示すLUT8におけるモード変更用メモリ81に指定する3ビッ

トのデータX, Y, Zと、それにしたがった選択信号F0 (X, Y, Z), F1 (X, Y, Z) およびF2 (D, E, F, X, Y, Z)、並びに、これら選択信号F0, F1, F2により制御される各セクタ821~826 (セクタ721~726に対応)の動作は、図6および図3(a)~図3(f)を参照して説明したのと同様であり、ここではその説明を省略する。

【0036】

図10は図9の6入力3出力LUTにおける3入力2出力LUTユニットの一例を示すブロック図である。なお、各3入力2出力LUTユニット831~834は全て同様の構成とされている。

図10に示すLUTユニット831は、アドレスデコーダ8311、セクタ8312, 8313、および、4組の4ビットで構成されたメモリユニット群M41~M44, M51~M54, M61~M64, M71~M74を備えている。アドレスデコーダ8311は、2ビットの入力信号A, Bをデコードして4組のメモリユニット群M41~M44, M51~M54, M61~M64およびM71~M74の各1つを指定し、さらに、入力信号Cによって、メモリユニット群M41~M44またはM51~M54の一方の組のデータ(出力信号Q:セクタ826の入力『0』に供給される信号)と、メモリユニット群M61~M64またはM71~M74の一方の組のデータ(セクタ826の入力『1』に供給される信号)とを選択して出力する。

【0037】

図11は図9の6入力3出力LUTにおける3入力2出力LUTユニットの他の例を示すブロック図である。

図11に示すLUTユニット831は、アドレスデコーダ8314、および、2組の8ビットのメモリユニット群M81~M888およびM91およびM98を備えている。アドレスデコーダ8314は、3ビットの入力信号A, B, Cをデコードして2組のメモリユニット群M81~M888およびM91およびM98の各1つを指定し、それぞれデータ(出力信号Q:セクタ826の入力『0』に供給される信号と、セクタ826の入力『1』に供給される信号)を出力する。

【0038】

図12は図9の6入力3出力LUTにおける3入力2出力LUTユニットのさらに他の例を示すブロック図である。

図11に示すLUTユニット831は、アドレスデコーダ8315、セクタ8416、8317、および、8組の2ビットのメモリユニット群M111, M121; M112, M122; …; M118, M128を備えている。アドレスデコーダ8315は、1ビットの入力信号Aをデコードして8組のメモリユニット群M111, M121~M118, M128の各1つを指定し、さらに、2ビットの入力信号B, Cによって、メモリユニット群M111, M121~M114, M124の内の一組のデータ（出力信号Q:セクタ826の入力『0』に供給される信号）と、メモリユニット群M115, M125~M118, M128の内の一組のデータ（セクタ826の入力『1』に供給される信号）とを選択して出力する。

【0039】

図13は8オペレーションのALU回路（ALU16）90の一構成例を示すブロック図である。図13において、参照符号GおよびHは16ビットのデータ、Iはオペレーションを決めるコマンド信号、そしてJは出力信号を示している。

図13に示されるように、ALU回路90は、それぞれ16ビットのデータGおよびHが入力されたOR回路91、AND回路92、XOR回路93、not回路94、+（加算）回路95、NE（Not Equal）回路96、GT（Greater Than）回路97およびSHIFT（シフト）回路98の8つの演算回路と、これら8つの演算回路91~98の出力をコマンド信号Iにより選択するセクタ99とを備え、コマンド信号Iに対応した出力信号J部を出力するようになっている。

【0040】

この図13に示すALU回路（ALU16）90に対して、従来のFPGAで使用されている3入力1出力LUTから7入力1出力LUT（横軸：3LUT~7LUT）に実装した場合と、本発明に係るFPGAで使用される図6に示すよ

うな6入力3出力LUT（8つの3入力1出力LUT 731～738、モード変更メモリ71およびセクタ721～726を備える構成：3LUT*8）および図9に示すような6入力3出力LUT（4つの3入力2出力LUT 831～834、モード変更メモリ81およびセクタ821～826を備える構成：4LUT*4）に実装した場合とを比較して、次の図14および図15に示す。なお、LUT16は、例えば、配線の切り替えを行うデータセクタ（LUTを使用する必要がない回路）、ランダムロジック（LUTで構成される回路）、および、フリップフロップ（論理ブロックの固定部分の回路）を備えている。また、図14および図15の比較は、LUTの構成以外の条件が実質的に同一として行われているのはいうまでもない。

【0041】

図14は図13に示すALU16を従来および本発明に係るFPGAで使用されるLUT（3LUT～7LUTおよび6入力3出力LUT（3LUT*8並びに4LUT*4））に実装したときの面積比の相違を示す図であり、また、図15は図13に示すALU16に対して従来および本発明に係るFPGAで使用されるLUTに実装したときの構成データビット数の相違を示す図である。図14における縦軸は、一般に使用されている4入力1出力LUT（4LUT）を用いて構成した場合の面積を1とし、それに対する様々なLUTを使用して構成した場合の面積比を示し、また、図15における縦軸は、様々なLUTを使用して構成した場合の構成データのビット数を示している。

【0042】

図14から明らかなように、例えば、図13に示すようなALU16を本発明に係るFPGAで使用されている6入力3出力LUT（3LUT*8および4LUT*4）に実装した場合の面積比は、同じのALU16を従来のFPGAで使用されているLUT（3LUT～7LUT）に実装した場合に比べて大幅に小さくなる事が分かる。具体的に、例えば、6入力3出力LUTを3入力1出力*8プレーンとして実装した3LUT*8は、従来のLUT中で最小面積を示す4入力1出力LUT（4LUT）を用いて実装した場合の約75%の面積とすることが分かる。

【 0 0 4 3 】

さらに、図 1 5 から明らかなように、ALU 1 6 を本発明に係る F P G A で使用されている 6 入力 3 出力 L U T (3 L U T * 8 および 4 L U T * 4) に実装した場合の構成データビット数は、従来の L U T 中で最小の 4 L U T の場合と同等であることが判る。すなわち、本発明 6 入力 3 出力 L U T は、例えば、4 入力 1 出力に対して 4 倍の構成データを必要とするにも関わらず、構成データビット数を同等とすることができるのは、従来の L U T が出力段のセレクタを L U T により構成しているのに対して、本発明では配線の切り替えによって行われるので L U T の使用数を削減することができるからである。

【 0 0 4 4 】

以上の説明において、本発明に係る F P G A で使用される 6 入力 3 出力 L U T は、単なる一例であり、M 入力 N 出力 (例えば、8 入力 4 出力) の L U T に適用することができる。さらに、例えば、6 入力 3 出力 L U T 自体の構成に関しても、図 6 に示す 8 つの 3 入力 1 出力 L U T ユニットおよび図 9 に示す 4 つの 3 入力 2 出力 L U T ユニットに限定されるものではなく、様々な変更が可能なものというまでもない。

【 0 0 4 5 】

【発明の効果】

以上、詳述したように、本発明によれば、ルックアップテーブル (L U T) すなわちプログラマブル論理回路装置の回路面積を削減することができる。さらに、本発明によれば、プログラマブル論理回路装置の消費電力を低減することもできる。

【図面の簡単な説明】

【図 1】

本発明が適用される F P G A の一例を示すブロック図である。

【図 2】

F P G A における L U T の一例としての 6 入力 3 出力 L U T を示すブロック図である。

【図 3】

図 2 に示す 6 入力 3 出力 L U T の内部構成モードを示すブロック図である。

【図 4】

ルックアップテーブルにおける回路のマッピング方法の一例を説明するための図である。

【図 5】

本発明に係る F P G A における L U T の一例としての 6 入力 3 出力 L U T を入出力信号と共に示すブロック図である。

【図 6】

図 5 に示す 6 入力 3 出力 L U T の内部構成の一例を示すブロック図である。

【図 7】

図 6 の 6 入力 3 出力 L U T における 3 入力 1 出力 L U T ユニットの一例を示すブロック図である。

【図 8】

図 6 の 6 入力 3 出力 L U T における 3 入力 1 出力 L U T ユニットの他の例を示すブロック図である。

【図 9】

図 5 に示す 6 入力 3 出力 L U T の内部構成の他の例を示すブロック図である。

【図 1 0】

図 9 の 6 入力 3 出力 L U T における 3 入力 2 出力 L U T ユニットの一例を示すブロック図である。

【図 1 1】

図 9 の 6 入力 3 出力 L U T における 3 入力 2 出力 L U T ユニットの他の例を示すブロック図である。

【図 1 2】

図 9 の 6 入力 3 出力 L U T における 3 入力 2 出力 L U T ユニットのさらに他の例を示すブロック図である。

【図 1 3】

8 オペレーションの A L U 回路 (A L U 1 6) の一構成例を示すブロック図である。

【図 1 4】

図 1 3 に示す A L U 1 6 に対して従来および本発明に係る F P G A で使用される L U T に実装したときの面積比の相違を示す図である。

【図 1 5】

図 1 3 に示す A L U 1 6 に対して従来および本発明に係る F P G A で使用される L U T に実装したときの構成データビット数の相違を示す図である。

【符号の説明】

7, 8, 1 2 1 … ルックアップテーブル (L U T : 6 入力 3 出力 L U T)

7 1, 8 1 … モード変更用メモリ

1 0 0 … プログラマブル論理回路装置 (F P G A)

1 0 1 … I / O ブロック

1 0 2 … 論理ブロック (C L B)

1 0 3 … 接続ブロック (C)

1 0 4 … スイッチマトリクス (S)

1 0 5 … 配線

1 2 2 … ラッチ

1 2 3 … セレクタ

7 2 1 ~ 7 2 6, 8 2 1 ~ 8 2 6 … セレクタ

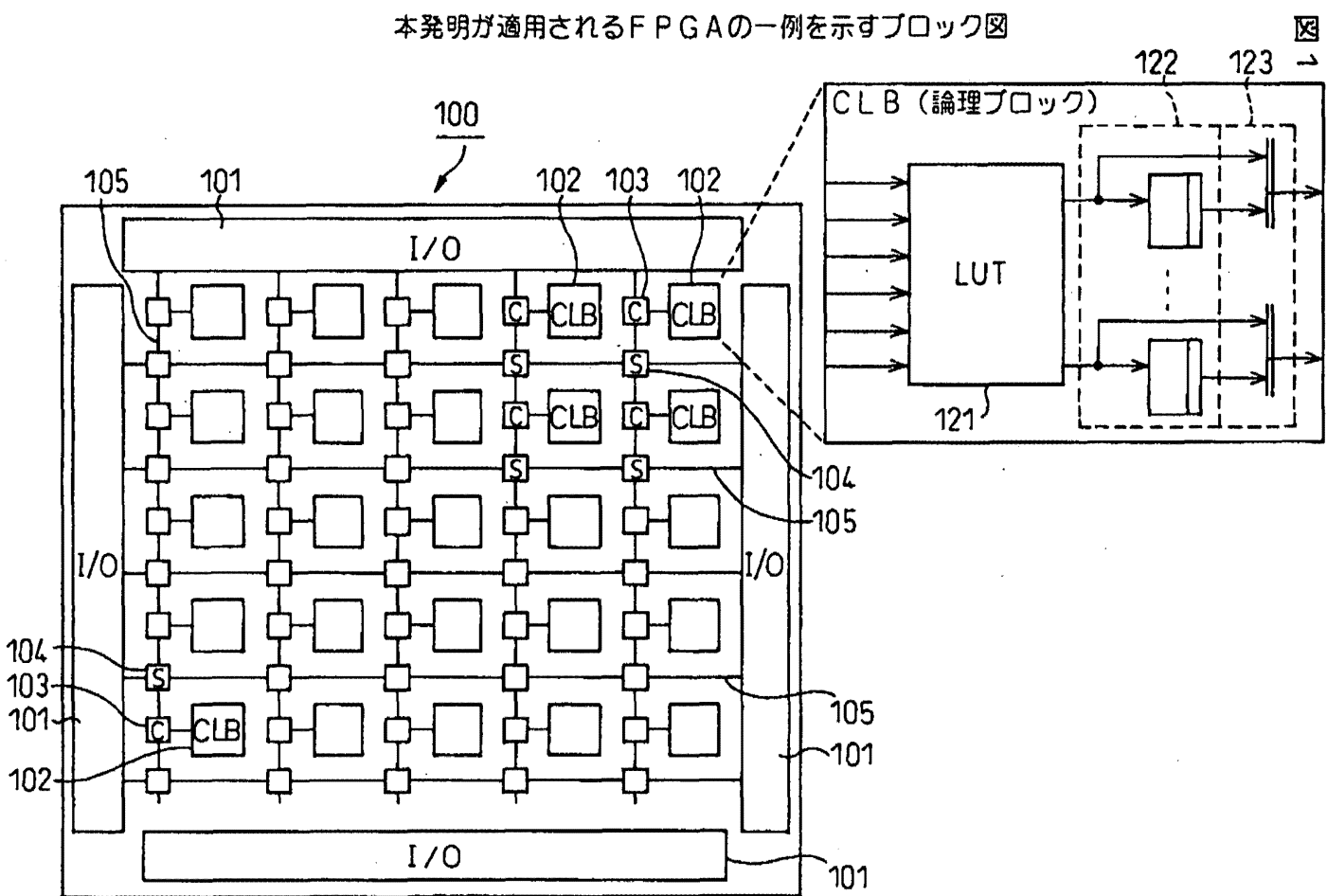
7 3 1 ~ 7 3 8 … 3 入力 1 出力 L U T ユニット

8 3 1 ~ 8 3 4 … 3 入力 2 出力 L U T ユニット

【書類名】

図面

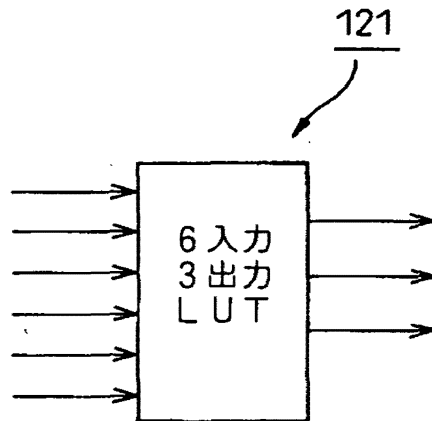
【図 1】



【図 2】

図 2

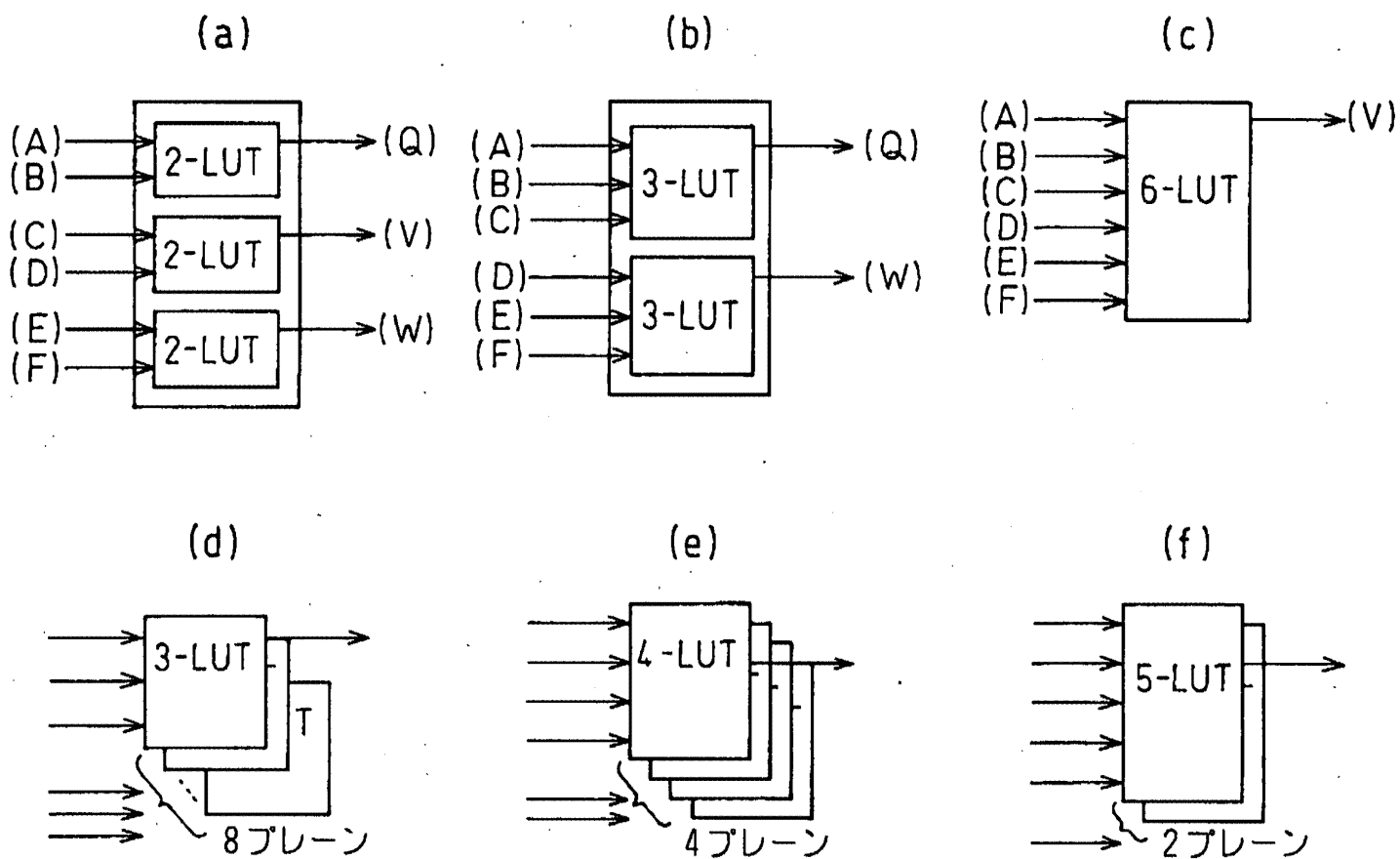
FPGAにおけるLUTの一例としての6入力3出力LUT
を示すブロック図



【図3】

図 3

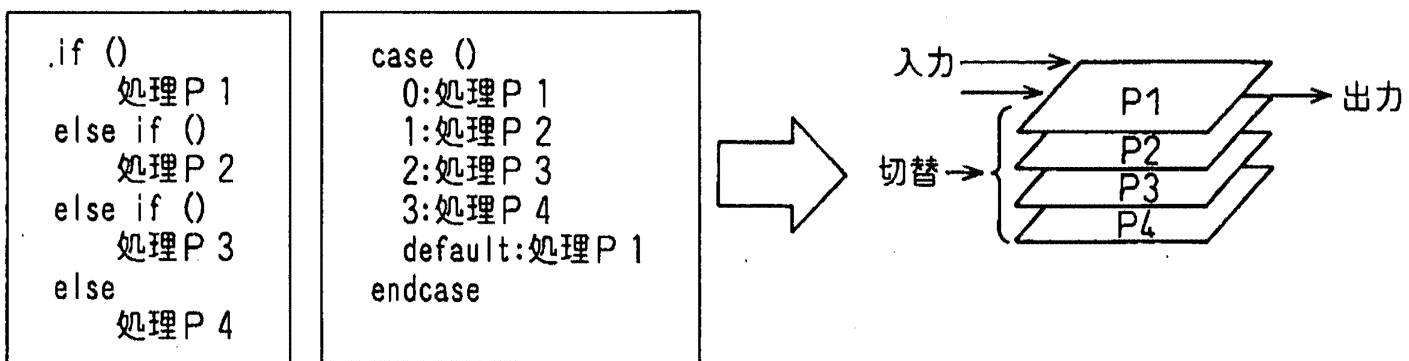
図2に示す6入力3出力LUTの内部構成モードを示すブロック図



【図4】

図 4

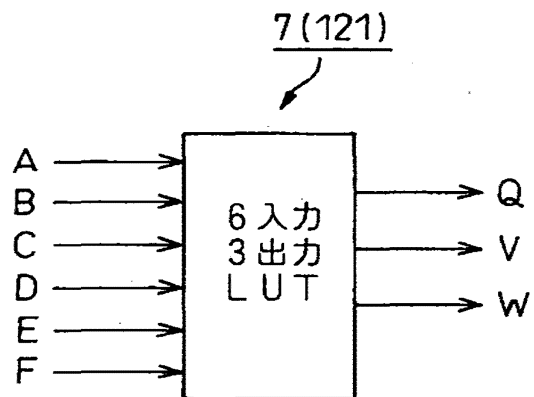
ルックアップテーブルにおける回路のマッピング方法の一例を説明するための図



【図 5】

図 5

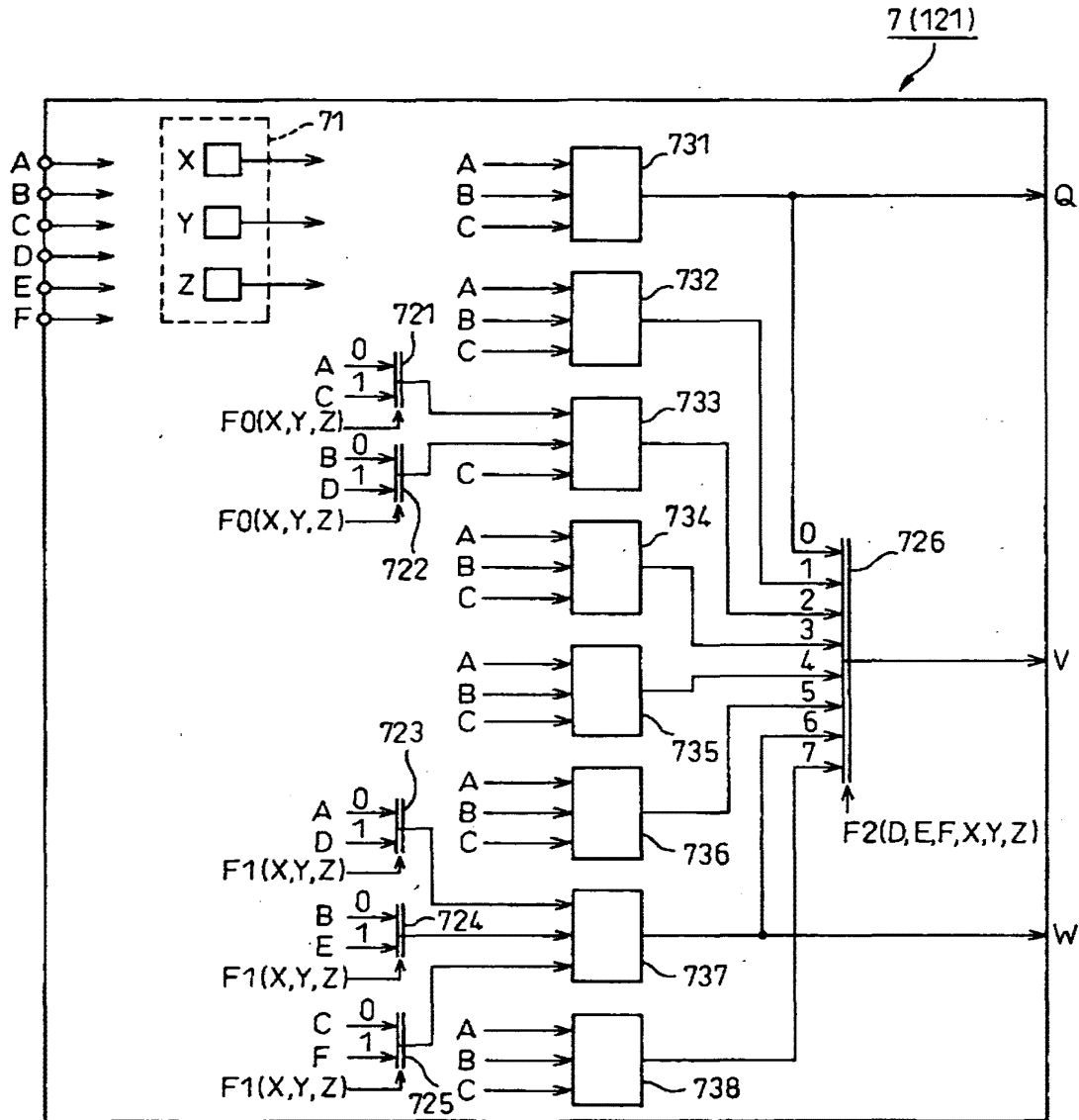
本発明に係る F P G A における L U T の一例としての
6 入力 3 出力 L U T を入出力信号と共に示すブロック図



【図 6】

図 6

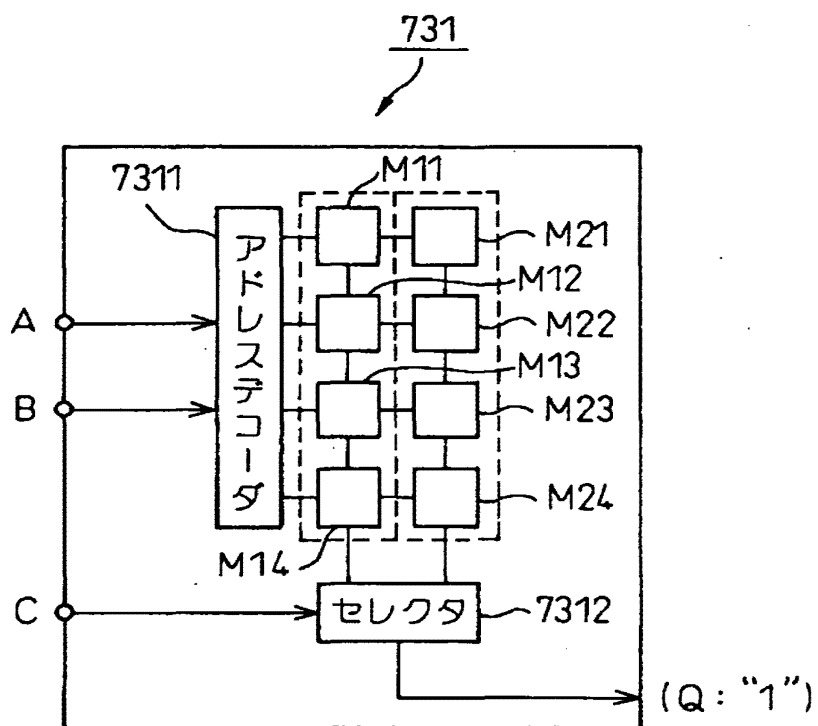
図 5 に示す 6 入力 3 出力 LUT の内部構成の一例を示すブロック図



【図 7】

図 7

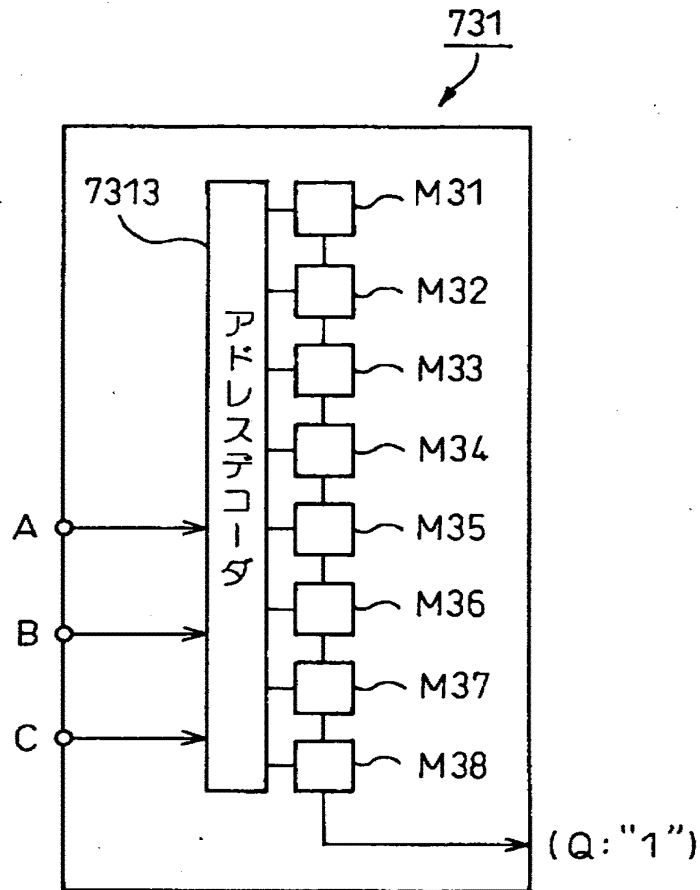
図 6 の 6 入力 3 出力 LUT における 3 入力 1 出力 LUT ユニットの一例を示すブロック図



【図 8】

図 8

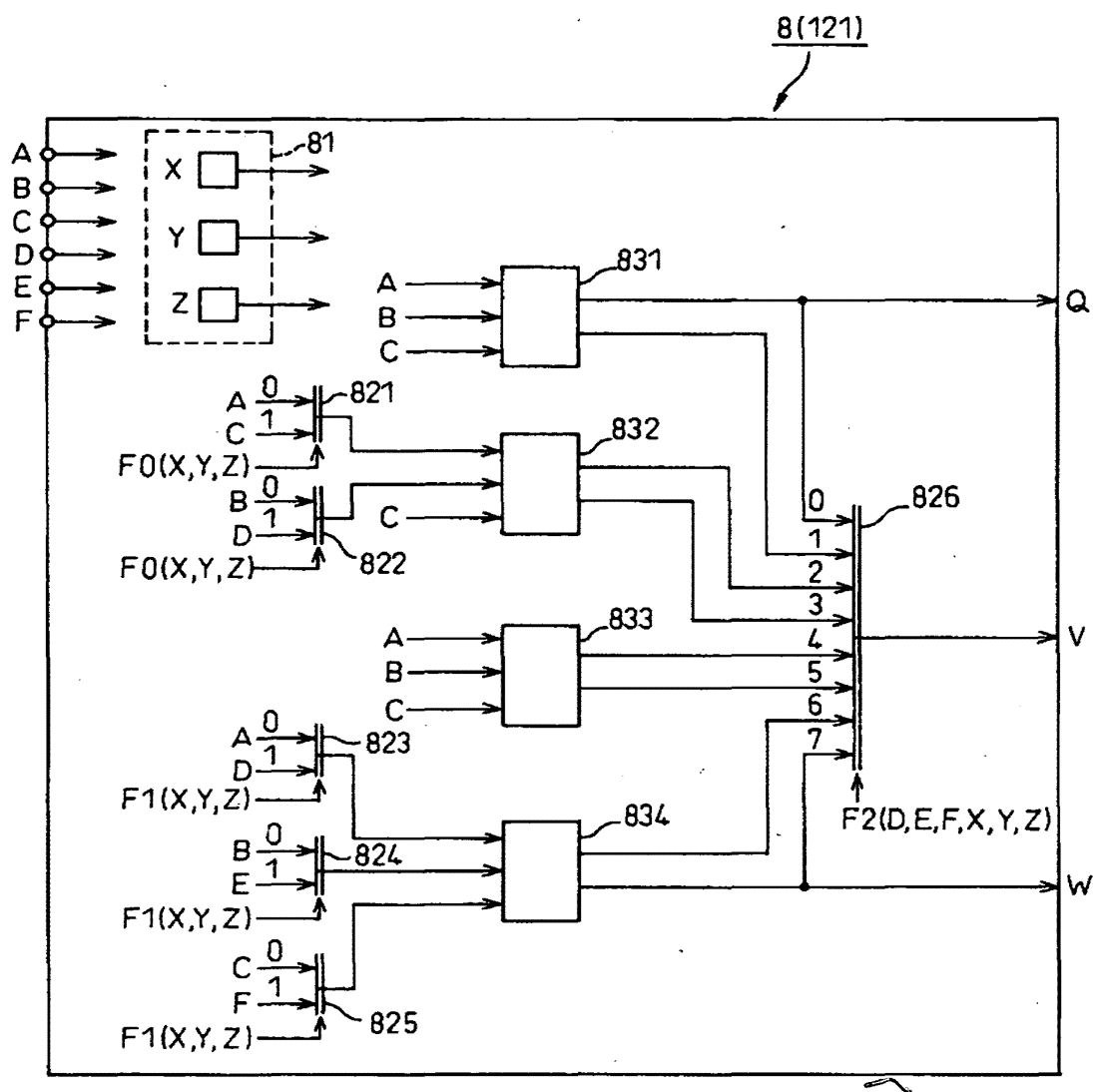
図 6 の 6 入 3 出 L U T における 3 入 1 出 L U T ユニットの他の例を示すブロック図



【图9】

图 9

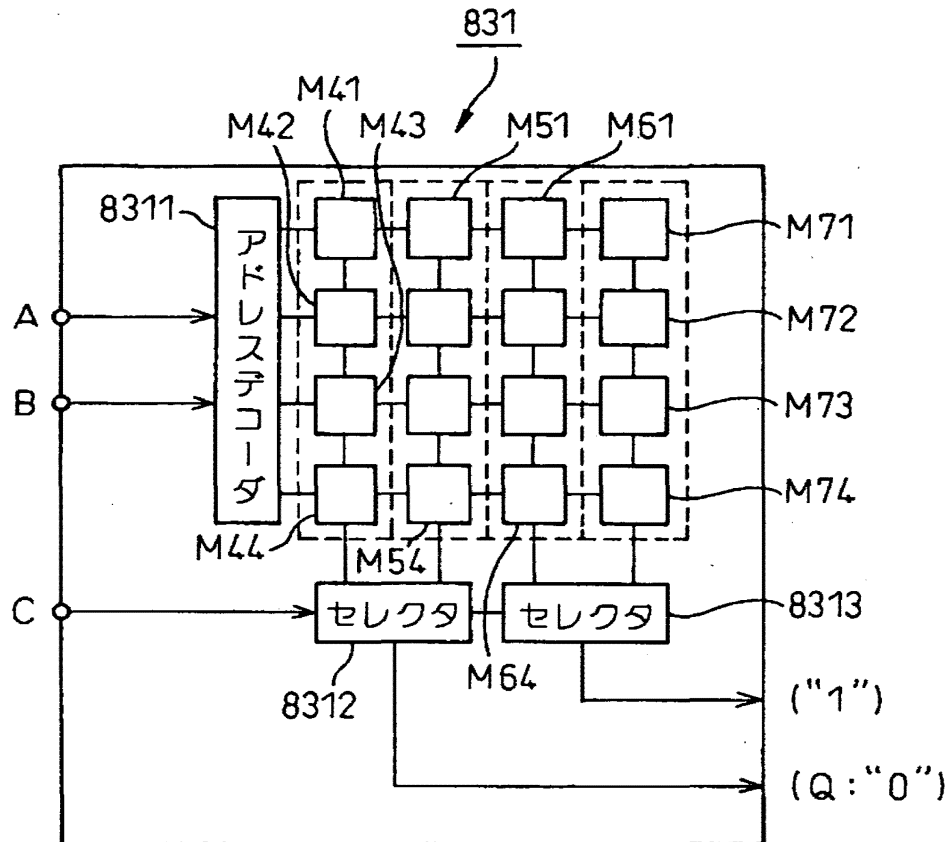
図5に示す6入力3出力LUTの内部構成の他の例を示すブロック図



【図10】

図10

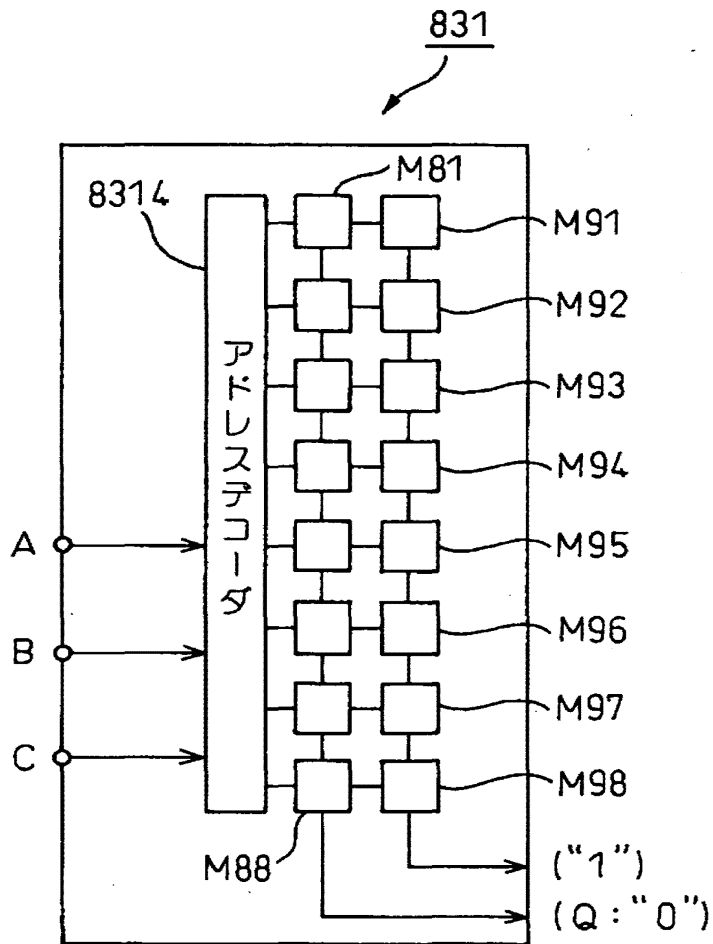
図9の6入力3出力UTにおける3入力2出力UTユニットの一例を示すブロック図



【図 11】

図 11

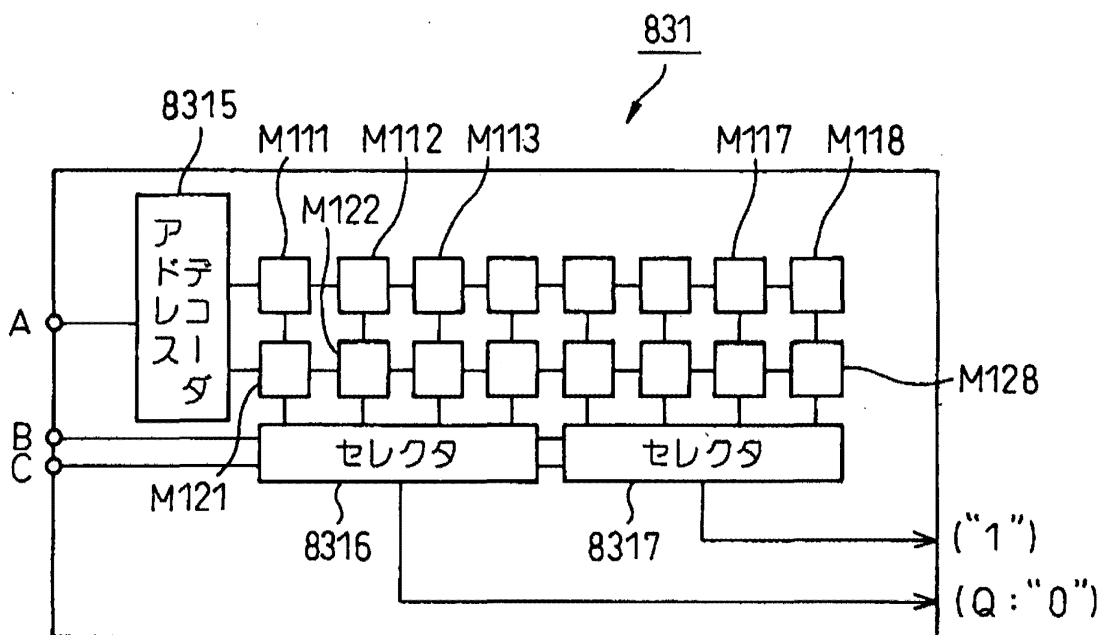
図 9 の 6 入 3 出 LUT における 3 入 2 出 LUT ユニットの他の例を示すブロック図



【図12】

図 12

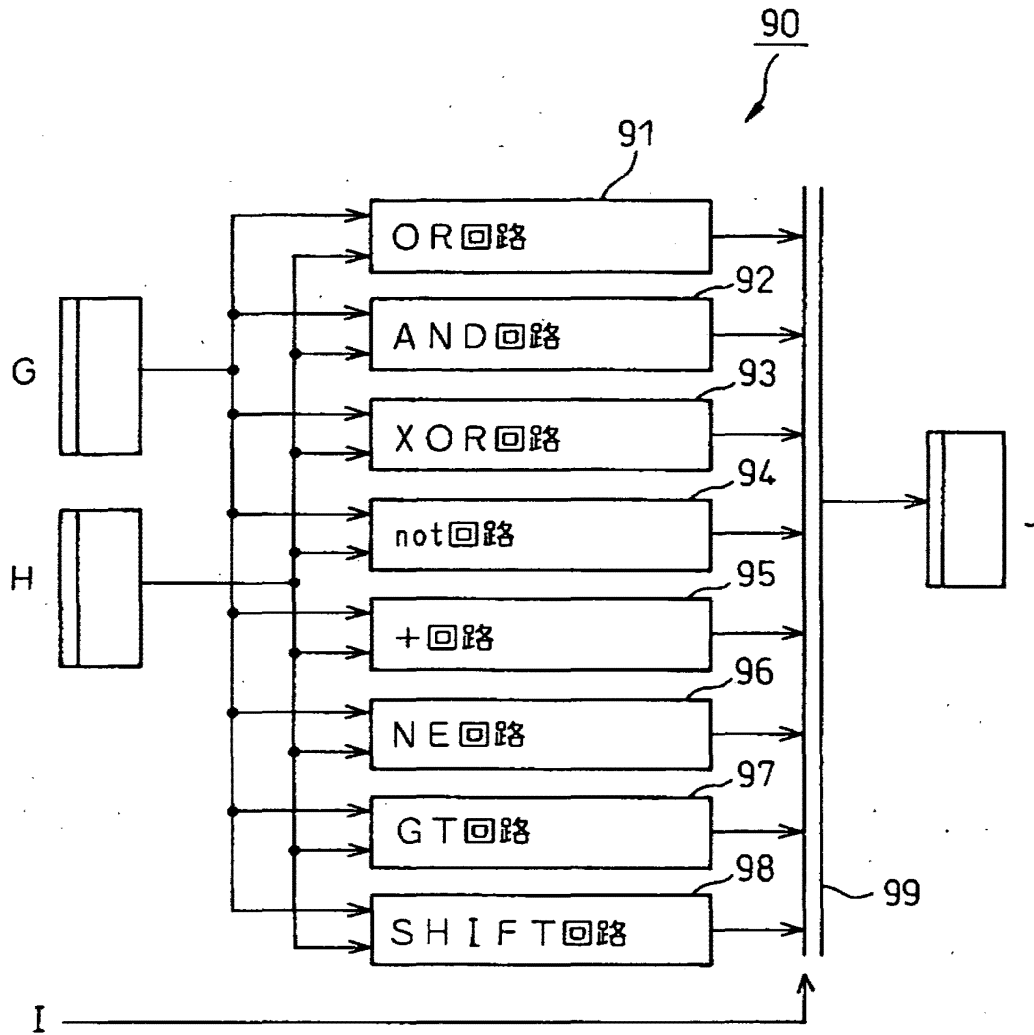
図9の6入力3出力LUTにおける3入力2出力LUTユニットのさらに他の例を示すブロック図



【図13】

図13

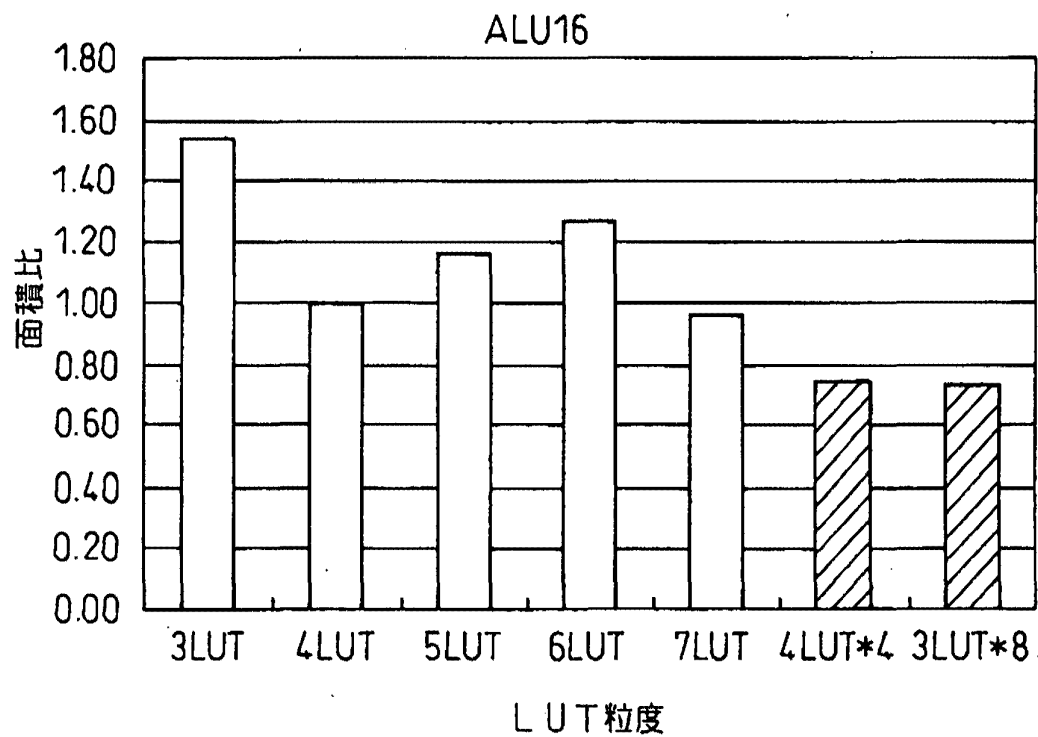
8オペレーションのALU回路（ALU16）の一構成例
を示すブロック図



【図14】

図 14

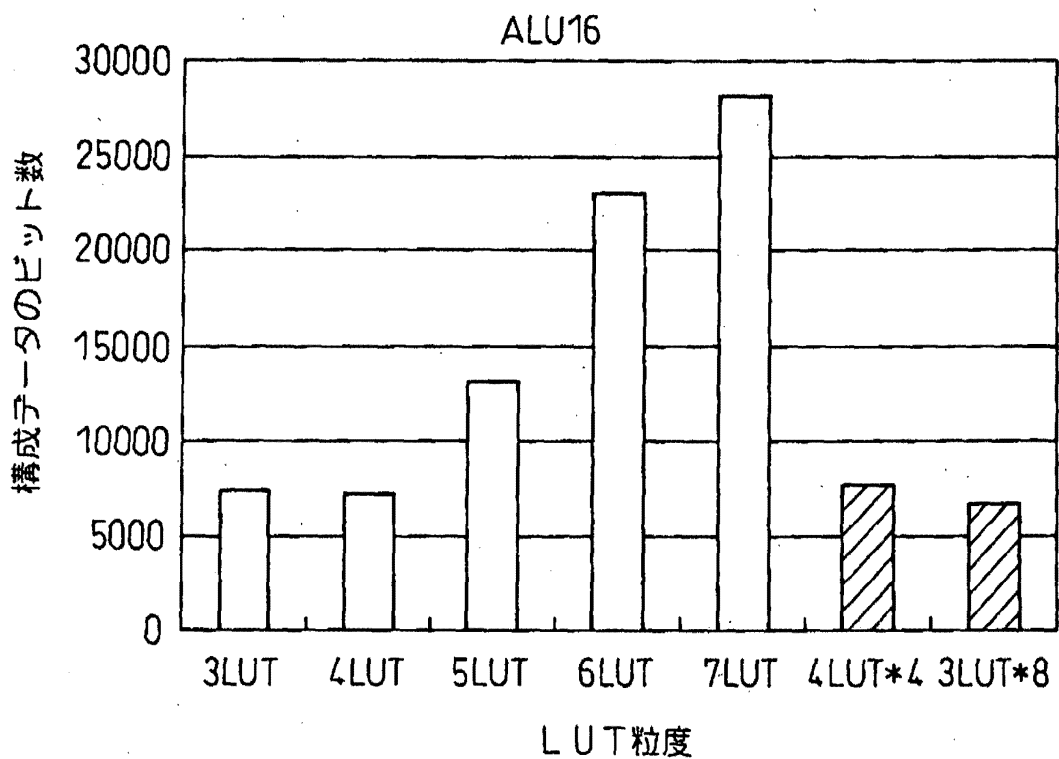
図13に示すALU16に対して従来および本発明に係るFPGAで使用されるLUTに実装したときの面積比の相違を示す図



【図15】

図15

図13に示すALU16に対して従来および本発明に係るFPGAで使用されるLUTに実装したときの構成データビット数の相違を示す図



【書類名】 要約書

【要約】

【課題】 従来、例えば、FPGAにおいて、LUTの入力数および出力数は共に固定値であり、実装面積の増加をもたらすことになっていた。

【解決手段】 M入力N出力のルックアップテーブル7であって、複数のLUTユニット731～738と、該複数のLUTユニットによる内部構成を制御する内部構成制御手段71，721～726とを備えるように構成する。

【選択図】 図6

出 願 人 履 歴 情 報

識別番号 [396023993]

1. 変更年月日 2001年 3月23日

[変更理由] 住所変更

住 所 神奈川県横浜市港北区新横浜3丁目17番地2 友泉新横浜ビル6階

氏 名 株式会社半導体理工学研究センター



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/183,590	06/28/2002	Toshinori Sueyoshi	1687.1001	9469

21171 7590 08/25/2003

STAAS & HALSEY LLP
SUITE 700
1201 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER

TRAN, ANH Q

ART UNIT	PAPER NUMBER
----------	--------------

2819

DATE MAILED: 08/25/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application N .

10/183,590

Applicant(s)

SUEYOSHI ET AL.

Examiner

Anh Q. Tran

Art Unit

2819

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 June 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 June 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- | | |
|--|---|
| 1) ☒ Notice of References Cited (PTO-892) | 4) ☐ Interview Summary (PTO-413) Paper No(s). _____ |
| 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) ☐ Notice of Informal Patent Application (PTO-152) |
| 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) <u>3</u> . | 6) ☐ Other: |

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. Claims 5, 13, & 20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. These limitations does not further limiting the controlling of the selectors of claims 3, 11, instead replace it.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims are rejected under 35 U.S.C. 102(e) as being anticipated by Lien et al (6,476,636).

Regarding claim 1, Lien shows a look up table (Fig. 7 and 50, Fig. 10) of M inputs (A, B, C of 50-56 detail shown in Fig. 10) and N outputs (JO, Y, JPO of 50-56 detail shown in Fig. 10), comprising:

A plurality of LUT units (82, 84 of 50-56), and an internal configuration control circuit (86-96, 98, 102, & 104 of 50-56) controlling an internal configuration of the plurality of LUT units.

Regarding claim 2, Lien shows the internal configuration control circuit comprises:

A plurality of selectors (86-96, 98, 102, & 104 are multiplexers); and

A selector control circuit (CM, col. 1 lines, 59 to col. 2, line 26) controlling the selectors and defining the internal configuration of the plurality of LUT units.

Regarding claims 3-4, Lien shows an input signal selector (86-96) provided at an input of at least one of the LUT units to select an input signal (A, B, or C); and

An output signal selector (102-104) provided at an output of the LUT units selecting an output signal, the input signal selector and the output signal selector being controlled in accordance with the data stored in the memory (CM, col. 1 lines, 59 to col. 2, line 26).

Regarding claim 6, Lien shows the look up table of M inputs and N outputs is a 6-input 3-output look up table.

Regarding claim 7, Lien shows the 6-input 3-output look up table comprise eight 3-input and 1-output LUT units (50-56, each including two LUTs shown in Fig. 10 together make-up eight LUTs).

Regarding claim 8, Lien shows the 6-input 3-output look up table comprise four 3-input and 2-output LUT units (50-56, each including 3-input and 2-output and shown in Fig. 10).

Regarding claim 9, Lien shows a programmable logic circuit device (Fig. 4, 7, 10, 12, 13, & 14) comprising:

A plurality of logic blocks (40, Fig. 13A);

A plurality of routing wires (Fig. 14) connected to each of the logic blocks;

A plurality of switch circuits (130, Fig. 14) provided at an intersection of each of the routing wires;

A plurality of connection blocks (134, 132, Fig. 14) provided between an I/O line of each of the logic blocks and each of the routing wires; and

An I/O block (42, Fig. 12) performing an input/output operation with external equipment, wherein each of the logic blocks has a look up table of M inputs and N outputs (rest of the limitations are described above), comprising:

A plurality of LUT units; and

An internal configuration control circuit controlling an internal configuration of the plurality of LUT units.

The limitations of claims 10-12, 14-16 are rejected as described above.

The apparatus described above are applicable to the method claims 17-19.

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Lane et al (6,323,677) discloses a logic module having a plurality of look-up table and input/output selectors.

Art Unit: 2819

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh Q. Tran whose telephone number is 703-306-4507. The examiner can normally be reached on M-TH (7:00-5:30) Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 703-305-3493. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Anh Tran
8/14/03

A handwritten signature in black ink, appearing to be 'Anh Tran', written in a cursive style.

Notice of References Cited	Application/Control No. 10/183,590	Applicant(s)/Patent Under Reexamination SUEYOSHI ET AL.	
	Examiner Anh Q. Tran	Art Unit 2819	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6323677	11-2001	Lane et al	326/37
	B	US-6476636	11-2002	Lien et al	326/41
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
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	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE LIST OF REFERENCES CITED BY APPLICANT <i>(Use several sheets if necessary)</i>	ATTORNEY DOCKET NO. 1687.1001	APPLICATION NO. 10/183590
	FIRST NAMED INVENTOR Toshinori SUEYOSHI, et al.	
	FILING DATE June 28, 2002	GROUP ART 10/183590

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NO.	DATE	NAME	CLASS	SUB- CLASS	FILING DATE
AT	AA	4,706,216	11/1987	Carter	✓	—	
	AB	4,870,302	09/1989	Freeman	✓	1	
	AC	5,778,439	07/1998	Trimberger et al.	✓	1	
	AD	5,905,385	05/1999	Sharpe-Geisler	✓	—	
	AE						
	AF						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB- CLASS	TRANSLATION YES NO	
	AG							
	AH							
	AI							
	AJ							
	AK							
	AL							

OTHER REFERENCES (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)

AT	AM	Rose, Jonathoan, et al., "Architecture of Field-Programmable Gate Arrays: The Effect of Logic Block Functionality on Area Efficiency", IEEE J. Solid-State Ciruits, Vol. 25, No. 5, pages 1217-1225, October 1990.
	AN	Rose, Jonathan et al., "The Effect of Logic Block Architecture on FPGA Performance", IEEE J. Solid-State Circuits, Vol. 27, No. 3., pages 281-287, March 1992.
	AO	Ahmed, Elias et al., "The Effect of LUT and Cluster Size on Deep-Submicron FPGA Performance and Density", FPGA 2000, Monterey, CA USA, 2000.

EXAMINER <i>[Signature]</i>	DATE CONSIDERED <i>8/14/03</i>
EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

REPLY/AMENDMENT FEE TRANSMITTAL

DEC 12 2003

Attorney Docket No. 1687.1001
Application Number 10/183,590
Filing Date June 28, 2002
First Named Inventor Toshinori SUEYOSHI, et al.
Group Art Unit 2819

AMOUNT ENCLOSED 110.00 Examiner Name Anh Q. Tran

FEE CALCULATION (fees effective 10/01/03)

CLAIMS AS AMENDED	Claims Remaining After Amendment	Highest Number Previously Paid For	Number Extra	Rate	Calculations
TOTAL CLAIMS	20	- 20 =	0	X \$ 18.00 =	\$ 0.00
INDEPENDENT CLAIMS	3	- 3 =	0	X \$ 86.00 =	0.00

Since an Official Action set an original due date of November 25, 2003, petition is hereby made for an extension to cover the date this reply is filed for which the requisite fee is enclosed (1 month (\$110); 2 months (\$420); 3 months (\$950); 4 months

If Notice of Appeal is enclosed, add (\$320.00)

If Statutory Disclaimer under Rule 20(d) is enclosed, add fee (\$110.00)

Information Disclosure Statement (Rule 1.17(p)) (\$180.00)

Total of above Calculations =

\$ 110.00

Reduction by 50% for filing by small entity (37 CFR 1.9, 1.27 & 1.28)

TOTAL FEES DUE =

\$ 110.00

(1) If entry (1) is less than entry (2), entry (3) is "0".

(2) If entry (2) is less than 20, change entry (2) to "20".

(4) If entry (4) is less than entry (5), entry (6) is "0".

(5) If entry (5) is less than 3, change entry (5) to "3".

METHOD OF PAYMENT

- ☒ Check enclosed as payment.
- ☐ Charge "TOTAL FEES DUE" to the Deposit Account No. below.
- ☐ No payment is enclosed and no charges to the Deposit Account are authorized at this time (unless specifically required to obtain a filing date).

GENERAL AUTHORIZATION

- ☒ If the above-noted "AMOUNT ENCLOSED" is not correct, the Commissioner is hereby authorized to credit any overpayment or charge any additional fees necessary to:

Deposit Account No.

19-3935

Deposit Account Name

STAAS & HALSEY LLP

- ☒ The Commissioner is also authorized to credit any overpayments or charge any additional fees required under 37 CFR 1.16 (filing fees) or 37 CFR 1.17 (processing fees) during the prosecution of this application, including any related application(s) claiming benefit hereof pursuant to 35 USC § 120 (e.g., continuations/divisionals/CIPs under 37 CFR 1.53(b) and/or continuations/divisionals/CPAs under 37 CFR 1.53(d)) to maintain pendency hereof or of any such related application.

SUBMITTED BY: STAAS & HALSEY LLP

Typed Name Alicia M. Choi Reg. No. 46,621

Signature

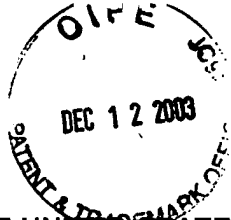
Alicia M. Choi

Date

12/12/2003

2819 #

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DEC 24 2003
TECHNOLOGY CENTER 2808



Docket No.: 1687.1001

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Toshinori SUEYOSHI, et al.

Serial No. 10/183,590

Group Art Unit: 2819

Confirmation No. 9469

Filed: June 28, 2002

Examiner: Anh Q. Tran

For: PROGRAMMABLE LOGIC CIRCUIT DEVICE HAVING LOOK UP TABLE ENABLING
TO REDUCE IMPLEMENTATION AREA

AMENDMENT

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

This is in response to the Office Action mailed August 25, 2003, and having a period for response set to expire on November 25, 2003. A Petition for a one-month extension of time, together with the requisite fee for same, is submitted herewith, thereby extending the period for response to December 25, 2003.

The following amendments and remarks are respectfully submitted. Reconsideration of the claims is respectfully requested.

12/16/2003 BABRAHA1 00000042 10183590

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IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please CANCEL claims 2-3 and 10-11 without prejudice or disclaimer and AMEND claims 1, 4, 5, 9, 12, 13, and 17 in accordance with the following:

1. (ORIGINAL) A look up table of M inputs and N outputs, comprising:
a plurality of LUT units; and
an internal configuration control circuit controlling an internal configuration of said plurality of LUT units, wherein said internal configuration control circuit comprises
a plurality of selectors selecting I/O signals of said plurality of LUT units, and
a selector control circuit having a memory, controlling said plurality of selectors in
accordance with data stored in said memory, and defining the internal configuration of said
plurality of LUT units.

2 –3 CANCELLED

4. (CURRENTLY AMENDED) The look up table as claimed in claim ~~3~~1, wherein said plurality of selectors include:
an input signal selector provided at an input of at least one of said LUT units to select an input signal; and
an output signal selector provided at an output of said LUT units selecting an output signal, said input signal selector and said output signal selector being controlled in accordance with the data stored in said memory.

5. (CURRENTLY AMENDED) The look up table as claimed in claim ~~3~~1, wherein said plurality of selectors include:
an input signal selector provided at an input of at least one of said LUT units to select an input signal; and
an output signal selector provided at an output of said LUT units selecting an output signal, said input signal selector and said output signal selector being controlled in accordance

with the input signal.

6. (ORIGINAL) The look up table as claimed in claim 1, wherein said look up table of M inputs and N outputs is a 6-input 3-output look up table.

7. (ORIGINAL) The look up table as claimed in claim 6, wherein said 6-input 3-output look up table comprises eight 3-input 1-output LUT units.

8. (ORIGINAL) The look up table as claimed in claim 6, wherein said 6-input 3-output look up table comprises four 3-input 2-output LUT units.

9. (CURRENTLY AMENDED) A programmable logic circuit device comprising: a plurality of logic blocks;
a plurality of routing wires connected to each of said logic blocks;
a plurality of switch circuits provided at an intersection of each of said routing wires;
a plurality of connection blocks provided between an I/O line of each of said logic blocks and each of said routing wires; and
an I/O block performing an input/output operation with external equipment, wherein each of said logic blocks has a look up table of M inputs and N outputs, comprising:
a plurality of LUT units; and
an internal configuration control circuit controlling an internal configuration of said plurality of LUT units, wherein said internal configuration control circuit comprises
a plurality of selectors selecting I/O signals of said plurality of LUT units, and
a selector control circuit having a memory, controlling said plurality of selectors in accordance with data stored in said memory, and defining the internal configuration of said plurality of LUT units.

10 – 11 CANCELLED

12. (CURRENTLY AMENDED) The programmable logic circuit device as claimed in claim 11, wherein said plurality of selectors include:
an input signal selector provided at an input of at least one of said LUT units to select an input signal; and
an output signal selector provided at an output of said LUT units selecting an output

signal, said input signal selector and said output signal selector
being controlled in accordance with the data stored in said memory.

13. (CURRENTLY AMENDED) The programmable logic circuit device as claimed in claim 449, wherein said plurality of selectors include:

an input signal selector provided at an input of at least one of said LUT units to select an input signal; and

an output signal selector provided at an output of said LUT units selecting an output signal, said input signal selector and said output signal selector being controlled in accordance with the input signal.

14. (ORIGINAL) The programmable logic circuit device as claimed in claim 9, wherein said look up table of M inputs and N outputs is a 6-input 3-output look up table.

15. (ORIGINAL) The programmable logic circuit device as claimed in claim 14, wherein said 6-input 3-output look up table comprises eight 3-input 1-output LUT units.

16. (ORIGINAL) The programmable logic circuit device as claimed in claim 14, wherein said 6-input 3-output look up table comprises four 3-input 2-output LUT units.

17. (CURRENTLY AMENDED) A method of configuring a look up table of M inputs and N outputs, comprising ~~the steps of~~:

providing a plurality of LUT units; and

selectively controlling I/O signals of said plurality of LUT units to set a predetermined mode of an internal configuration.

18. (ORIGINAL) The method of configuring a look up table as claimed in claim 17, wherein the I/O signals of said plurality of LUT units are selectively controlled in accordance with data stored in the corresponding look up table.

19. (ORIGINAL) The method of configuring a look up table as claimed in claim 17, wherein an input signal input to at least one of said LUT units and an output signal output from said LUT unit are selectively controlled in accordance with data stored in the corresponding look up table.

20. (ORIGINAL) The method of configuring a look up table as claimed in claim 17, wherein an input signal input to at least one of said LUT units and an output signal output from said LUT unit are selectively controlled in accordance with a predetermined function of the input signal.

REMARKS

In accordance with the foregoing, claims 1, 4, 5, 9, 12, 13, and 17 have been amended. Claims 2-3 and 10-11 have been cancelled without prejudice or disclaimer.

Claims 1, 4-9, and 12-20 are pending and under consideration.

REJECTION UNDER 35 U.S.C. § 112:

In the Office Action, at page 2, claims 5, 13, and 20 were rejected under 35 U.S.C. § 112, second paragraph, for the reasons set forth therein. This rejection is traversed and reconsideration is requested.

Dependent claim 5, for instance, further recites features of the selectors. According to dependent claim 2, "a selector control circuit" controls "said selectors." Further, dependent claim 5 provides that the selectors include an input signal selector and an output signal selector, where the input signal selector and the output signal selector "**being controlled** in accordance with the input signal," emphasis added. Thus, because the selector control circuit does the control of the selectors, which include the input and output signal selectors, the selector control circuit controls the selectors in accordance with the input signal selected. Accordingly, dependent claim 5 is definite.

Dependent claim 13 recites, "an input signal selector provided at an input of at least one of said LUT units to select an input signal; and an output signal selector provided at an output of said LUT units selecting an output signal, said input signal selector and said output signal selector being controlled in accordance with the input signal," and dependent claim 20 recites, "wherein an input signal input to at least one of said LUT units and an output signal output from said LUT unit are selectively controlled in accordance with a predetermined function of the input signal."

Similar arguments are incorporated herein as those presented supporting the definiteness of dependent claim 5 to support the definiteness of dependent claims 13 and 20. It is respectfully requested that the rejection to the claims be withdrawn.

REJECTION UNDER 35 U.S.C. § 102:

In the Office Action, at page 2, claims 1-20 were rejected under 35 U.S.C. § 102 in view of U.S. Patent No. 6,476,636 to Lien et al. ("Lien"). This rejection is traversed and reconsideration is requested.

Lien generally describes a tileable field programmable gate array (FPGA) architecture

suitable for both integrated circuits (ICs) requiring large FPGAs and small FPGAs, where the FPGA is to be manufactured as its own IC or to be manufactured into a large IC (for example, SoC). Specifically, as shown in FIGS. 2, 3A, 35 and 4 of Lien, the FPGA has a plurality of functional groups (FGs), a regular routing structure, and a plurality of interface groups (IGs). As shown in FIGS. 2, 3A, 38 and 4 of Lien, the FPGA has FPGA tiles; and as shown in FIG. 5 of Lien the FPGA tile has a plurality of FGs and ICs. Further, as shown in FIG. 7, four LUs 50, 52, 54, and 56 are connected in a bus-connection manner, which is different from a switching-connection manner in a general FPGA. Further, as shown in FIG. 10 of Lien, the LU 50 has a plurality of LUTs 82, 84, a flip-flop (FF) 106, and a plurality of selectors 86, 88, ..., 104. In Lien, column 8, lines 25 through 27, describes that "one purpose of including two LUTE 82, 84 in the LU 50 is so that they can be used together to provide a four-input LUT."

However, Lien does not teach or suggest "a selector control circuit having a memory, controlling said plurality of selectors in accordance with data stored in said memory," as recited in independent claims 1 and 9. Specifically, as recited in independent claims 1 and 9, the look up table of M inputs and N outputs comprise "a plurality of LUT units; and an internal configuration control circuit controlling an internal configuration of said plurality of LUT units, wherein said internal configuration control circuit comprises a plurality of selectors selecting I/O signals of said plurality of LUT units, and a selector control circuit having a memory." Further, the selector control circuit of independent claims 1 and 9, controls "said plurality of selectors in accordance with data stored in said memory," and defines "the internal configuration of said plurality of LUT units." These claimed features of the present invention (claims 1 and 9) is not taught or suggested in Lien. Accordingly, it is respectfully requested that independent claims 1 and 9 and related dependent claims be allowed.

CONCLUSION:

In accordance with the foregoing, it is respectfully submitted that all outstanding objections and rejections have been overcome and/or rendered moot, and further, that all pending claims patentably distinguish over the prior art. Thus, there being no further outstanding objections or rejections, the application is submitted as being in condition for allowance, which action is earnestly solicited.

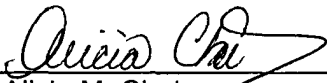
If the Examiner has any remaining issues to be addressed, it is believed that prosecution can be expedited by the Examiner contacting the undersigned attorney for a telephone interview to discuss resolution of such issues.

If there are any underpayments or overpayments of fees associated with the filing of this Amendment, please charge and/or credit the same to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

Date: 12/12/03

By: 
Alicia M. Choi
Registration No: 46,621

1201 New York Avenue, NW, Suite 700
Washington, D.C. 20005
Telephone: (202) 434-1500
Facsimile: (202) 434-1501



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/183,590	06/28/2002	Toshinori Sueyoshi	1687.1001	9469
21171	7590	03/03/2004	EXAMINER	
STAAS & HALSEY LLP SUITE 700 1201 NEW YORK AVENUE, N.W. WASHINGTON, DC 20005			TRAN, ANH Q	
			ART UNIT	PAPER NUMBER
			2819	

DATE MAILED: 03/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/183,590

Applicant(s)

SUEYOSHI ET AL.

Examiner

Anh Q. Tran

Art Unit

2819

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 December 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,4-9 and 12-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,4-6,9 and 12-20 is/are rejected.
- 7) ☒ Claim(s) 7,8,15 and 16 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) ☒ Notice of References Cited (PTO-892) | 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) ☐ Notice of Informal Patent Application (PTO-152) |
| 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) ☐ Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims are rejected under 35 U.S.C. 102(e) as being anticipated by Lane et al (6,323,677).

Regarding claim 1, Lane shows a look up table (100b, Fig. 5) of M inputs (A, B, C, D, Q, DCIN, CIN) and N outputs (DCOUT, COUT, output from 150), comprising:

A plurality of LUT units (110a-110c), and

an internal configuration control circuit (102, 240, 250, 120a, 120b, 124, R)

controlling an internal configuration of the plurality of LUT units, where the internal configuration control circuit comprises

A plurality of selectors (102, 240, 250, 120a) selecting I/O signals of the plurality of LUT units, and

A selector control circuit (R which is FCE, col. 12, 34-38) having a memory, controlling the plurality of selectors in accordance with data stored in the memory, and defining the internal configuration of the plurality of LUT units.

Regarding claim 4, Lane shows an input signal selector (250) provided at an input of at least one of the LUT units to select an input signal (A, B, or D); and

An output signal selector (120a) provided at an output of the LUT units selecting an output signal, the input signal selector and the output signal selector being controlled in accordance with the data stored in the memory (RDCNMULT).

Regarding claim 5, Lane shows an input signal selector (250) provided at an input of at least one of the LUT units to select an input signal (A, B, or D); and

An output signal selector (120a) provided at an output of the LUT units selecting an output signal, the input signal selector and the output signal selector being controlled in accordance with the input signal (D).

Regarding claim 6, Lane shows the look up table of M inputs and N outputs is a 6-input 3-output look up table (6-input: A, B, C, D, Q, DCIN, CIN; 3-output: DCOUT, 150, COUT).

Regarding claim 7, Lane shows the 6-input 3-output look up table comprise eight 3-input and 1-output LUT units (50-56, each including two LUTs shown in Fig. 10 together make-up eight LUTs).

Regarding claim 8, Lane shows the 6-input 3-output look up table comprise four 3-input and 2-output LUT units (50-56, each including 3-input and 2-output and shown in Fig. 10).

Regarding claim 9, Lane shows a programmable logic circuit device (Fig. 4, 7, 10, 12, 13, & 14) comprising:

A plurality of logic blocks (module, col. 1, lines 20-29);

Art Unit: 2819

A plurality of routing wires (interconnection conductor) connected to each of the logic blocks;

A plurality of switch circuits (other circuit element) provided at an intersection of each of the routing wires;

A plurality of connection blocks (see U.S. pat. No. 5,909,126 or 5,999,015) provided between an I/O line of each of the logic blocks and each of the routing wires; and

An I/O block (inherent limitation) performing an input/output operation with external equipment, wherein each of the logic blocks has a look up table of M inputs and N outputs and the rest of the limitations are described above in claim 1.

The limitations of claims 12-14 are rejected as described above.

The apparatus described above are applicable to the method claims 17-20.

Allowable Subject Matter

3. Claims 7-8, and 15-16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh Q. Tran whose telephone number is 571-272-1813. The examiner can normally be reached on M-TH (7:00-5:30) Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANH Q. TRAN
PRIMARY EXAMINER


2/19/04

Notice of References Cited	Application/Control No. 10/183,590	Applicant(s)/Patent Under Reexamination SUEYOSHI ET AL.	
	Examiner Anh Q. Tran	Art Unit 2819	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,323,677	11-2001	Lane et al.	326/37
	B	US-5,909,126	06-1999	Cliff et al.	326/41
	C	US-5,999,015	12-1999	Cliff et al.	326/39
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims



Application No.

10/183,590

Examiner

Anh Q. Tran

Applicant(s)

SUEYOSHI ET AL.

Art Unit

2819

✓	Rejected
=	Allowed

—	(Through numeral) Cancelled
÷	Restricted

N	Non-Elected
I	Interference

A	Appeal
O	Objected

Claim		Date									
Final	Original										
	2										
	19										
	24										
	✓										
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Search Notes

Application No.

10/183,590

Examiner

Anh Q. Tran

Applicant(s)

SUEYOSHI ET AL.

Art Unit

2819

SEARCHED

Class	Subclass	Date	Examiner
326	38 1 41	2/19/04	AT

INTERFERENCE SEARCHED

Class	Subclass	Date	Examiner

**SEARCH NOTES
(INCLUDING SEARCH STRATEGY)**

	DATE	EXMR



AF 2819/8
#FW
(1)
Attorney Docket No. 1687.1001

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application of:

Toshinori SUEYOSHI, et al.

Application No.: 10/183,590

Group Art Unit: 2819

Filed: June 28, 2002

Examiner: Anh Q. Tran

Confirmation No.: 9469

For: PROGRAMMABLE LOGIC CIRCUIT DEVICE HAVING LOOK UP TABLE ENABLING
TO REDUCE IMPLEMENTATION AREA

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure provisions of 37 CFR § 1.56, there is hereby provided certain information which the Examiner may consider material to the examination of the subject U.S. patent application. It is requested that the Examiner make this information of record if it is deemed material to the examination of the subject application.

1. Enclosures accompanying this Information Disclosure Statement are:

- 1a. ☒ Form PTO-1449.
- 1b. ☒ Copies of IDS citations.
- 1c. ☒ A Japanese language Office Action from a counterpart foreign application.
- 1d. ☒ English language translation (abstracts only) attached to each non-English language publication.
- 1e. ☐ Explanations of Relevancy of References (ATTACHMENT 1(e), hereto) for providing a concise explanation of each non-English publication.
- 1f. ☐ List of Copending Applications (ATTACHMENT 1(f), hereto).
- 1g. ☐ List of Additional Submitted Documents (ATTACHMENT 1(g), hereto).

2. ☐ This Information Disclosure Statement is filed under 37 CFR §1.97(b):

(Check either Item 2a or 2b or 2c or 2d)

- 2a. ☐ Within three months of the filing date of a national application other than a Continued Prosecution Application under § 1.53(d);
- 2b. ☐ Within three months of the date of entry of the national stage as set forth in § 1.491 in an international application.
- 2c. ☐ Before the mailing of a first Office Action on the merits; or
- 2d. ☐ Before the mailing of a first Office Action after the filing of a Request for Continued Examination under § 1.114.

3. ☐ This Information Disclosure Statement is filed under 37 CFR § 1.97(c) after the period specified in paragraph 2 above but before the mailing date of any of a Final Office Action under § 1.113, a Notice of Allowance under § 1.311 or an action that otherwise closes prosecution in the application, AND

(Check either Item 3a or 3b; Item 3b to be checked if any reference known for more than 3 months)

- 3a. ☐ The §1.97(e) Statement in Item 5 below is applicable; OR
 3b. ☐ The \$180.00 fee set forth in 37 C.F.R. §1.17(p) is:
☐ enclosed.
☐ to be charged to Deposit Account No. 19-3935.

4. ☒ This Information Disclosure Statement is filed under 37 CFR §1.97(d) after the period specified in paragraph 3 above, but on or before payment of the Issue Fee, AND

- 4a. ☒ The § 1.97(e) Statement in Item 5 below is applicable; AND
 4b. ☒ The \$180.00 fee set forth in 37 C.F.R. §1.17(p) is:
☒ enclosed.
☐ to be charged to Deposit Account No. 19-3935.

5. ☒ Statement under § 1.97(e) (*applicable if Item 3a or Item 4a is checked*)
(Check either Item 5a or 5b)

- 5a. ☒ In accordance with 37 CFR § 1.97(e)(1), it is stated that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement.
 5b. ☐ In accordance with 37 CFR § 1.97(e)(2), it is stated that no item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in this Information Disclosure Statement was known by any individual designated in §1.56(c) more than three months prior to the filing of this Information Disclosure Statement.

6. ☐ This is a continuation/divisional/continuation-in-part application under 37 CFR § 1.53(b).

(Check appropriate Items 6a and/or 6b)

- 6a. ☐ Copies of the publications listed on the attached Form PTO-1449 which were previously cited in prior application Serial No. ___, filed on ___, and which is relied on for an earlier effective filing date for the subject application under 35 U.S.C. § 120, have been omitted pursuant to 37 CFR § 1.98(d).
 6b. ☐ Copies of the publications listed on the attached Form PTO-1449 which were not previously cited in prior application Serial No. ___, filed on ___, and which is relied on for an earlier effective filing date for the subject application under 35 U.S.C. § 120, are provided herewith.

7. ☐ This is a continuation/divisional application under 37 CFR § 1.53(d) or a Request for Continued Examination under 37 CFR 1.114.

(Check either Item 7a or 7b)

- 7a. ☐ The Issue Fee has not been paid.
7b. ☐ A Petition to Withdraw from issue under 37 CFR § 1.313(c) is filed concurrently herewith or has been granted. A continuation/divisional application under 37 CFR § 1.53(d) or a Request for Continued Examination under 37 CFR 1.114, after payment of the Issue Fee, is proper in accordance with 37 CFR § 1.53(d)(1)(ii) or 37 CFR 1.114(a), respectively.

8. ☐ This is a Supplemental Information Disclosure Statement.

(Check either Item 8a or 8b)

- 8a. ☐ This Supplemental Information Disclosure Statement under 37 CFR § 1.97(f) supplements the Information Disclosure Statement filed on _____. A bona fide attempt was made to comply with 37 CFR § 1.98, but inadvertent omissions were made. These omissions have been corrected herein. Accordingly, additional time is requested so that this Supplemental IDS can be considered as if properly filed on _____.
8b. ☐ This Supplemental Information Disclosure Statement is timely filed within one (1) month of the Notice under 37 CFR § 1.97 and 1.98, mailed _____.

9. ☒ In accordance with 37 CFR § 1.98, a concise explanation of what is presently understood to be the relevance of each non-English language publication is:

(Check appropriate Items 9a, 9b, 9c and/or 9d)

- 9a. ☐ satisfied because all non-English language publications were cited on the enclosed "English language version of the search report or action which indicates the degree of relevance found by the foreign office". (See MPEP § 609, Minimum Requirements for an Information Disclosure Statement, Part A(3): Concise Explanation of Relevance, 8th Ed.)
9b. ☐ set forth in the application.
9c. ☒ satisfied because an English language translation (abstracts only) is attached to each non-English language publication.
9d. ☐ enclosed as Attachment 1(e), hereto.

10. No admission is made that the information cited in this Statement is, or is considered to be, material to patentability nor a representation that a search has been made (other than search report(s) from a counterpart foreign application or a PCT International Search Report, if submitted herewith). 37 CFR §§ 1.97(g) and (h).

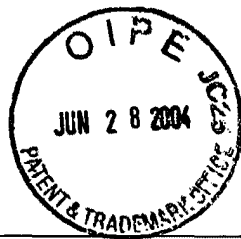
11. The Commissioner is authorized to credit any overpayment or charge any additional fee required under 37 CFR § 1.17 for this Information Disclosure Statement to Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

Dated: 6/28/2007
1201 New York Ave., N.W., Suite 700
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By: Alicia Choi
Alicia M. Choi
Registration No. 46,621



Sheet 1 of 1

FORM PTO-1449

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

ATTORNEY DOCKET NO.

1687.1001

APPLICATION NO.

10/183,590

FIRST NAMED INVENTOR

Toshinori SUEYOSHI, et al.

FILING DATE

June 28, 2002

GROUP ART UNIT

2819

LIST OF REFERENCES CITED BY APPLICANT

(Use several sheets if necessary)

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NO.	DATE	NAME	CLASS	SUB- CLASS	FILING DATE
	AA	5,442,306	08/15/95	Woo			
	AB						
	AC						
	AD						
	AE						
	AF						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB- CLASS	TRANSLATION YES NO	
	AG	03-063846	03/19/91	Japan			abstract	
	AH	08-237109	09/13/96	Japan			abstract	
	AI							
	AJ							
	AK							
	AL							

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

TRANSLATION
YES NO

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EXAMINER

DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

PATENT ABSTRACTS OF JAPAN

(11)Publication number : **03-063846**

(43)Date of publication of application : 19.03.1991

(51)Int.Cl.

G06F 12/00

G06F 1/02

G06F 15/66

(21)Application number : 01-200701

(71)Applicant : FUJI PHOTO FILM CO LTD

(22)Date of filing : 02.08.1989

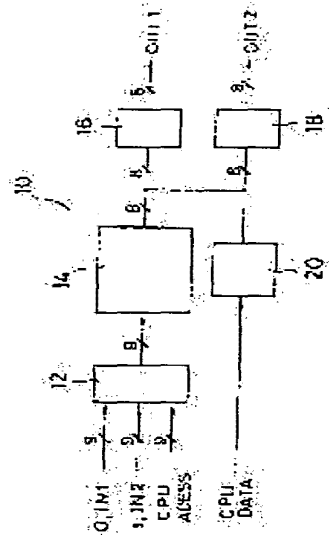
(72)Inventor : KIMURA HIDEAKI

(54) LOOK-UP TABLE DEVICE

(57)Abstract:

PURPOSE: To reduce the number of signal lines to make access a look-up table(LUT) by storing at least two LUTs in one memory, and making access those plural LUTs in time division.

CONSTITUTION: The device is equipped with a data selector 12, a memory 14 to store first and second LUTs, a latch circuit 16 to latch the output of the first LUT, and a latch circuit 18 to latch the output of the second LUT. Also, it is equipped with a bidirectional buffer 20 to transmit data to be transmitted to a central processing unit (CPU) and data to be written on the memory 14 from the CPU. And an input signal to one of the plural LUTs is selected sequentially with the data selector 12, and the data is read out from a selected LUT, and after it is held with the latch circuit transiently, it is outputted sequentially at need to the next processing circuit, and access to the plural LUTs are performed sequentially in time division. In such a way, it is possible to reduce the number of signal lines to make access the plural LUTs.



LEGAL STATUS

[Date of request for examination]

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[Patent number]

[Date of registration]

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PARTIAL TRANSLATION

(on page 3 from right over column line 17 through left under column line 16)

Figure 1 is a block diagram showing an embodiment of a look-up table device according to the present invention.

The look-up table device 10 shown in Fig. 1 has a data selector 12, a memory 14 to store a first look-up table (below, described as LUT) and a second LUT, a latch circuit 16 to latch an output signal of the first LUT, a latch circuit 18 to latch an output signal of the second LUT, and a bidirectional buffer 20 to transmit data to be transmitted to a central processing unit (CPU: not shown) and data to be written on the memory 14 from the CPU.

The data selector 12, which may be constituted by a multiplexer (MUX), and the like, sequentially selects one from three input signals of an input signal IN1 to be inputted to the first LUT, an input signal IN2 to be inputted to the second LUT, and CPU address signal CPU ADDRESS in accordance with an instruction from the CPU (not shown) or a predetermined order, so as to transmit to the memory 14.

⑨ 日本国特許庁(JP)

⑩ 特許出願公開

⑫ 公開特許公報(A) 平3-63846

⑤ Int.Cl.⁵

G 06 F 12/00
1/02
15/66

識別記号

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庁内整理番号

8841-5B
7459-5B
8419-5B

④ 公開 平成3年(1991)3月19日

審査請求 未請求 請求項の数 1 (全9頁)

⑭ 発明の名称 ルックアップテーブル装置

⑯ 特 願 平1-200701

⑰ 出 願 平1(1989)8月2日

⑱ 発 明 者 木 村 秀 明 神奈川県足柄上郡開成町宮台798番地 富士写真フイルム株式会社内

⑲ 出 願 人 富士写真フイルム株式会社 神奈川県南足柄市中沼210番地

⑳ 代 理 人 弁理士 渡辺 望 稔

明 細 書

3. 発明の詳細な説明

1. 発明の名称

ルックアップテーブル装置

2. 特許請求の範囲

(1) 複数のルックアップテーブルを格納する1つのメモリと、この複数のルックアップテーブルの1つへの入力信号を選択するデータセレクタと、前記複数のルックアップテーブルのそれぞれに対応して設けられ、それぞれのルックアップテーブルの出力をラッチするラッチ回路とを有することを特徴とするルックアップテーブル装置。

<産業上の利用分野>

本発明は、ルックアップテーブル装置に関し、より詳細には、画像処理回路を構成する要素として用いられる複数のルックアップテーブルを1つのメモリに有するルックアップテーブル装置に関する。

<従来の技術>

画像読取装置や画像読取記録装置などにおいては、光電子増倍管(フォトマルチプライヤ)、撮像管およびCCDなどの固体撮像素子等を用いて、原稿画像を読み取った後に、読み取られた画像信号を画像処理装置において種々の画像処理を行った後に適当な画像記録装置によって感光材料や感光体等の記録材料に記録している。

例えば、写真やフイルムなどの連続階調画像の原稿をCCDで読み取って電気信号に変換し

た後、網点階調画像を有する印刷用フィルムなどを作製するスキャナなどの画像読取記録装置においては、CCDで読み取った画像信号を画像処理装置において、ゲイン補正などのアナログ補正後、A/D変換し、シェーディング補正や暗時補正などのCCD補正をし、次いで、対数変換、階調変換、倍率変換、平滑化、鮮鋭化などの各処理後、網掛処理して、網点画像信号とし、この網点画像信号を画像記録装置において、光源の発光信号に変調してフィルム上に網点画像を再生している。

このような画像処理装置や画像記録装置の変調処理装置（以下、総称して画像処理装置という）においては、ある入力信号に対応して予め定められたデータを迅速かつ簡便に読み出すために、多数のルックアップテーブル（LUT）が用いられている。従来、これらのルックアップテーブル（LUT）は、それぞれ1つずつ個々のメモリに格納されていた。

また、このような画像処理装置においては、

数の処理回路をゲートアレイ等によりIC化しようとする、ICと外付けメモリとを接続するデータラインやアドレスラインの信号線などがそれぞれのメモリに対して必要となり、接続するためのピン数が不足し、IC化できる回路規模が制限されてしまうという問題がある。

例えば、1つのLUTにアクセスするための信号線がN本必要な場合には、2個のLUTの場合は2N本、M個のLUTを用いる場合にはM・N本の信号線が必要となり、IC化する際にICのピン数が不足してしまう。

また、最近、LUTを格納するためのメモリの容量が大きくなってきており、非常に小さなLUTに個々にメモリチップを配置するのは、コストダウンの妨げとなっている。

本発明の目的は、上記従来技術の問題点を解消し、1つのメモリに少なくとも2つのLUTを格納し、時分割でこれら複数のLUTにアクセスするように構成することにより、LUTへアクセスするための信号線を減らすことがで

複数の画像処理を行う回路をゲートアレイ方式等でIC化して複数の異なる画像処理を行うことのできる高集積化画像処理回路が用いられている。

<発明が解決しようとする課題>

ところで、1つのLUTに対し1つのメモリを用いると、多数のLUTを用いる場合、メモリの周辺回路、例えば中央処理装置（CPU）からデータを書いたりするための周辺回路などが数多くなり、回路構成が大変になる。

例えば、前記画像処理回路をゲートアレイ等でIC化しようとする際に、LUTを格納したメモリも一緒にIC化しようすると、ICが高いものになり、回路構成全体のコストが高くなってしまう。

このため、従来は、LUTを格納するメモリは、ICの外部に配置されていた。ところで、多数のLUTを用いる画像処理装置において、1つのLUTを1つのメモリに格納し、複

数、装置構成をコンパクトで安価なものとすることができるばかりか、LUTを格納するメモリを外部に配置する場合にも、複数の処理回路をゲートアレイ等によりIC化する場合にもIC化できる回路規模を大きくでき、必要なメモリの個数を減らすことができ、1つのICの有する処理機能を増大させることができ、装置構成全体として、例えば画像処理装置全体としてのコストを低減させることのできるルックアップテーブル装置を提供するにある。

<課題を解決するための手段>

上記目的を達成するために、本発明は、複数のルックアップテーブルを格納する1つのメモリと、この複数のルックアップテーブルの1つへの入力信号を選択するデータセクタと、前記複数のルックアップテーブルのそれぞれに対応して設けられ、それぞれのルックアップテーブルの出力をラッチするラッチ回路とを有することを特徴とするルックアップテーブル装置を

提供するものである。

前記メモリは、2つのルックアップテーブルを格納するのが好ましい。

< 発明の作用 >

本発明に係るルックアップテーブル装置は、1つのメモリに2つ以上のLUTを格納し、前記メモリに接続されたデータセクタにより複数のLUTのうちの1つへの入力信号を順次選択し、この入力信号により選択されたLUTからデータを読み取り、このLUTからの出力データを一時的に対応するラッチ回路で保持した後に必要に応じて順次、次の処理回路に出力することにより、あるいは、LUTからの出力データをCPUに入力したり、CPUからLUTにデータを書き込んだりすることにより、複数のLUTに時分割で順次アクセスすることができる。

従って、本発明のルックアップテーブル装置は、複数のLUTにアクセスするための信号線

の数を減らすことができ、また必要なメモリの個数を減らすことができ、装置の回路構成をコンパクトで安価なものとすることができる。

このため本発明のルックアップテーブル装置を用いる処理装置、例えば画像処理装置の回路構成において、少ないメモリを外部に置いてゲートアレイ等によりIC化する際に回路規模を大きくすることができ、1つのICの有する機能を増大させることができるので、前記処理装置、画像処理装置の装置全体の回路構成をコンパクトで安価なものとすることができる。

< 実施態様 >

本発明に係るルックアップテーブル装置を添付の図面に示す好適実施例に基づいて詳細に説明する。

第1図は、本発明のルックアップテーブル装置の一実施例を示すブロック図である。

同図に示すルックアップテーブル装置10は、データセクタ12と、第1のルックアップ

テーブル（以下、LUTとする）と第2のLUTとの2つのLUTを格納するメモリ14と、第1のLUTの出力をラッチするラッチ回路16と、第2のLUTの出力をラッチするラッチ回路18と、図示しないCPUへ伝送するデータおよび前記CPUからメモリ14に書き込むデータを伝送する双方向バッファ20とを有する。

データセクタ12は、第1のLUTへの入力信号IN1と、第2のLUTへの入力信号IN2と、CPUアドレス信号CPU ADDRESSとの3つの入力信号の中から図示しないCPUなどの指令もしくは予め定められた順序で順次1つの入力信号を選択し、メモリ14に伝送するためのもので、マルチプレクサ（MUX）などのデータセクタを用いることができる。

データセクタ12とメモリ14とは1組の信号線、すなわちアドレスラインで接続され、データセクタ12により選択された1つの入力信号がメモリ14に伝送される。

メモリ14は、第1のLUTと第2のLUTを格納するメモリであり、CPUなどによりその内容が書き込まれたり、書き換えられることがない場合はROMでもよいが、CPUからの書き込みを考慮する必要がある場合はRAMで構成するのがよい。1つのメモリに2つのLUTすなわち第1のルックアップテーブルであるLUT1と第2のルックアップテーブルLUT2の内容を割り付ける方法としては、どのような方法でもよいが、例えば、以下の表1に示すようにLUT1およびLUT2の内容が8bitデータである時、アドレスデータを9bitとしてメモリアドレスが000000000～011111111まではLUT1に割り付け、メモリアドレス100000000～111111111まではLUT2に割り付ける方法などを用いることができる。

表 1 メモリの割付

メモリアドレス	メモリ内容
000000000 000000001 011111111	L U T 1
100000000 100000001 111111111	L U T 2

ここでは、L U T 1 および L U T 2 の内容を読み出すためのアドレスデータを 9 b i t データとし、先頭の 1 b i t を L U T 1 と L U T 2 のいずれの L U T を選択するかを判別データ、例えば 0 であれば L U T 1 を、1 であれば L U T 2 のルックアップテーブルの内容を読み出すように構成される。こうして読み出されるデータは前述したように 8 b i t データである。

このように構成することにより、8 b i t の

大きさおよび内容に応じて適宜定めればよいが、1つのメモリに格納する L U T の数が多くなれば、メモリの中からある特定の L U T のデータを読み出すのに必要な時間が長くなる。

従って、本発明のルックアップテーブル装置 10 を低速で動作させることが可能な場合には 1つのメモリに多数の L U T を格納させることができる。

画像処理装置のように大量の画素データを処理する場合などのように、データ処理にある程度の速度が要求される場合には、2つの L U T を 1つのメモリに格納するのが好ましい。

一般に 1つの L U T へアクセスするための信号線の本数を N 本とすると、2つの L U T を用いる場合、従来の装置のように、1つの L U T を 1つのメモリに格納して用いると 2 N 本の信号線が必要であるが、本発明のルックアップテーブル装置のように 2つの L U T を 1つのメモリに格納して用いると N + 1 本の信号線に減らすことができる。さらに、2 M 個または

メモリデータからなる 2つの L U T を格納したメモリ 14 へのアドレスラインは、9 b i t のアドレスデータを伝送する 9 本の信号線であればよい。一方、8 b i t のメモリデータからなる 2つの L U T を別々のメモリへ格納した場合、各メモリへのアドレスデータは 8 b i t であり、各メモリへアクセスするため信号線はそれぞれ 8 本が必要で、合計 16 本の信号線が必要となる。第 1 図に示す本発明のルックアップテーブル装置 10 のように 2つの L U T を格納した 1つのメモリ 14 においては、アクセスするための信号線を 9 本とすることができる。

上記の例では、L U T 1 と L U T 2 のメモリ量を等しくしたけれども、本発明はこれに限定されるわけではなく、一方を多く、他方を少なくしてもよい。

また、メモリ 14 に格納される L U T の数は、2つに限定されるわけではなく、3つ以上であってもよく、メモリ 14 の容量、L U T の

2 M - 1 個の L U T を用いる場合に従来装置で必要な 2 M · N 本または (2 M - 1) · N 本の信号線を N + M 本の信号線に減らすことができる。

メモリ 14 から延長されるデータラインはラッチ回路 16、18 および双方向バッファ 20 に接続される。

ラッチ回路 16 および 18 は、それぞれメモリ 14 から順次出力される第 1 の L U T (L U T 1) および第 2 の L U T (L U T 2) のデータを一時的に蓄えておく回路であって、ラッチ回路 16 は、I N 1 による L U T 1 の 8 b i t のデータを O U T 1 として出力し、ラッチ回路 18 は、I N 2 による L U T 2 の 8 b i t のデータを O U T 2 として出力する。

双方向バッファ 20 は、C P U にメモリ 14 からのデータを伝送するとともに、C P U からメモリ 14 に書き込むためのデータを伝送することのできる伝送方向切換器である。

ここで、本発明のルックアップテーブル装置

10においては、2つのLUTを格納するメモリ14を除いて、すなわち、データセクタ12、2つのラッチ回路16、18および双方向バッファ20は、図示しないCPUと一緒にゲートアレイ等によりIC化することができる。

この時、メモリ14とICとの間には、ICのデータセクタ(MUX)12に接続される、例えば9本の信号線からなるデータラインと2つのラッチ回路16および18に接続される、例えば8本の信号線からなるデータラインが接続される。この他、図示しないがメモリ14とCPUとの間には、メモリ14からCPUへの読み出し、またはCPUからメモリ14への書き込みを制御するための制御ラインが接続されている。また、図示しないがIC内において、データセクタ(MUX)12を制御するための制御ライン、ラッチ回路16および18を制御するための制御ラインなどがタイミング制御回路との間に接続される。このよう

に保持した後、OUT2に出力する。

こうして、データセクタ(MUX)12はIN1およびIN2をタイミング制御回路の所定の信号、例えばクロック信号に応じて交互に時分割で入力信号を選択し、メモリ14へ出力する。また、ラッチ回路16と18では、タイミング制御回路の所定の信号、例えば、クロック信号に対応した信号に従って、交互にデータの一時保持と出力とを時分割でくり返す。

なお、データセクタ(MUX)12でCPU ADDRESSが選択される場合には、この信号でアドレスが指定され、CPUは、そのアドレスのメモリに対して双方向バッファ20を介してデータの読み出しまたは書き込みを行う。

第2図に、第1図に示す本発明のルックアップテーブル装置10の具体的な回路構成の一実施例を示す。さらに第3図および第4図に、第2図に示すルックアップテーブル装置10のそれぞれ異なる動作状態の一例のタイムチャー

にCPUおよび制御回路の構成は、従来公知の回路構成を用いることができる。

本発明のルックアップテーブル装置10は、基本的に以上のように構成されるが、以下にその作用について述べる。

まず、データセクタ(MUX)12はタイミング制御回路からの所定の信号に基づいてIN1を選択し、IN1から入力された先頭が0である9bitのアドレスデータをメモリ14に出力する。メモリ14ではLUT1からアドレスデータに応じた8bitのメモリデータを読み出し、ラッチ回路16へ出力し、ラッチ回路16で一時的に保持した後、OUT1に出力する。一方、タイミング制御回路からの信号が切り換ると、データセクタ(MUX)12はIN2を選択し、IN2から入力された先頭が1である9bitアドレスデータをメモリ14に出力し、メモリ14ではLUT2から8bitのメモリデータを読み出し、ラッチ回路18へ出力し、ラッチ回路18で一時的

トを示す。なお、第2図に示すルックアップテーブル装置10の構成要素は、タイミング制御回路22を除き、第1図に示すルックアップテーブル装置10と全く同一であるので、その詳細な説明は省略する。

第2図において、データセクタ(MUX)12のA、BおよびCは、それぞれIN1、IN2およびADR(第1図ではCPU ADDRESSとして示す)の入力側端子を示し、Yは出力側端子を示す。また、S1、S2は入力先A、B、Cの選択信号(入力端子)である。

メモリ14におけるAはメモリアドレスデータ(入力側端子)、Dはメモリデータ(出力側端子)を示す。またWE、OEは、それぞれメモリ14からの読み出しおよび書き込みのタイミング信号入力端子である。

ラッチ回路16および18におけるDはメモリデータ(入力側端子)、Qは出力データ(出力側端子)である。

双方向バッファ20のDATAは、図示しないCPUとメモリ14との間のデータ（例えば画像データ）の伝送を行うためのCPUとの間の入出力ラインである。

タイミング制御回路22は、MUX12、メモリ14、ラッチ回路16および18、双方向バッファ20の信号選択および入出力のタイミングを制御するための制御回路である。ここで入力側において、CLKはクロック信号（入力側端子）、MODEはCPUアクセス動作（MODE=0）、リアルタイム動作（MODE=1）とを選択するモード選択信号（入力側端子）、RDおよびWRはそれぞれCPUからのメモリ読み出し信号およびメモリ書き込み信号（入力端子）を示す。また、出力側において、G1およびG2は、それぞれ双方向バッファ20のCPUによるメモリ14の読み出しおよび書き込みのデータの伝送方向制御信号（出力端子）であり、S1、S2は前述したよ

うにMUX12のセレクト信号（出力端子）、WEおよびOEは、前述したように、メモリ14の書き込みおよび読み出しタイミング信号、C1およびC2は、それぞれラッチ回路16および18の入出力のタイミング制御信号である。

ここでデータセクタであるMUX12の動作は、制御回路22からのS1およびS2の信号により入力先をA、B、Cのうちから選択し、Y出力としてメモリ14に出力する。選択方法の一例を表2に示す。

表 2

S 1	S 2	Y 出 力
0	0	A 入力 (IN 1)
1	0	B 入力 (IN 2)
0	1	C 入力 (ADR)

まず、CPUによるメモリ14のLUT1またはLUT2の読み出しおよび書き込みを行うCPUアクセス動作をさせる場合には、タイミ

ング制御回路22へモード選択信号MODE=0が入力され、タイミング制御回路22からMUX12へMUXセレクト信号S1=0、S2=1が入力されている。

この時、第3図に示すように、タイミング制御回路22のメモリ読み出し信号RD、メモリ書き込み信号WEが変化すると、RDの変化に応じG1が変化して双方向バッファ20をメモリ14からCPUへデータが伝送される方向にデータ伝送方向を切換えるとともにOEが変化してメモリ14を読み出し可能な状態として、WRの変化に応じ、G2により双方向バッファ20のデータ伝送方向をCPUからメモリ14に向う方向に切り換えるとともに、WEによりメモリ14を書き込み可能な状態にする。

一方、メモリ14に収納されたLUT1とLUT2を順次読み出すリアルタイム動作を行わせる場合には、タイミング制御回路22へモー

ド選択信号MODE=1が入力され、タイミング制御回路22からMUX12へ常にMUXセレクト信号S2=0が入力されている。またこの時には、タイミング制御回路22からメモリ14へメモリ書き込み信号WE=1、メモリ読み出し信号OE=0が常に入力されており、メモリ14への書き込みは禁止され、メモリ14からの読み出しは常時可能な状態にされる。

ここで、第4図に示すように、タイミング制御回路22へ図示のようなクロック信号CLKが入力されると、これに応じ、MUXセレクト信号S1が変化し、表2に示すように入力先をA(0、IN1)とB(1、IN2)に切り換え、これに対応してタイミング制御信号C1およびC2が変化して、それぞれラッチ回路16および18の入出力を制御する。すなわち、第4図に示すように、MUXセレクト信号S1の0と1との変化に従ってメモリ14の入力側

メモリAの内容が0、IN1のメモリアドレスデータと1、IN2のメモリアドレスデータとに切り換わり、メモリ14の出力側およびラッチ回路16と18の入力側のメモリDの内容がこれらのアドレスデータに応じて読み出された表1に示すメモリ内容すなわちLUT1とLUT2のデータとに切り換わる。また、第4図に示すように、ラッチ回路16のOUT1およびラッチ回路18のOUT2がそれぞれ信号C1およびC2の立ち上りで切り換わる。

こうして、第2図に示すルックアップテーブル装置10において、表1に示すLUT1とLUT2の2つのルックアップテーブルの内容が1つのメモリ14から順次読み出される。

本発明のルックアップテーブル装置は、複数のLUTを必要とする回路、特に画像処理装置の各種処理回路、例えば、諧調変換処理回路、平滑化処理回路および鮮鋭化処理回路などに好適に用いることができる。

以上、本発明について好適実施例を挙げて説

明したが、本発明は、これに限定されるものではなく、本発明の要旨を逸脱しない範囲において種々の改良並びに設計の変更が可能なことは勿論である。

従って、本発明によれば、使用するメモリの数を減らすことができ、IC化した際にもコンパクト化できるので、装置構成をコンパクトかつ安価にすることができる。よって、本発明のルックアップテーブル装置は、多数の処理を行う画像処理装置の各種処理回路に好適に用いることができる。

4. 図面の簡単な説明

第1図は、本発明に係るルックアップテーブル装置の一実施例の構成を示すブロック図である。

第2図は、第1図に示すルックアップテーブル装置の具体的な回路構成の一実施例のブロック図である。

第3図および第4図は、第2図に示すルックアップテーブル装置のそれぞれ異なる動作状態の一例を示すタイムチャートである。

明したが、本発明は、これに限定されるものではなく、本発明の要旨を逸脱しない範囲において種々の改良並びに設計の変更が可能なことは勿論である。

<発明の効果>

以上、詳述したように、本発明によれば、1つのメモリに複数のルックアップテーブルを格納するので、1つのルックアップテーブルを個々に1つのメモリに格納する場合に比べて、ルックアップテーブルにアクセスするための信号線を減らすことができる。

このため、本発明によれば、複数の処理回路をゲートアレイ等によりIC化する際に複数のルックアップテーブルを1つの外付けメモリに格納することにより、個々の外付けメモリに格納する場合に比べて、信号線の数を減らすことができるので、IC化に際してピン数の不足を招くことがなく、IC化の規模が制限されない。

符号の説明

- 10…ルックアップテーブル装置、
- 12…マルチプレクサ(MUX)、
- 14…メモリ、
- 16、18…ラッチ回路、
- 20…双方向バッファ、
- 22…タイミング制御回路

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FIG. 1

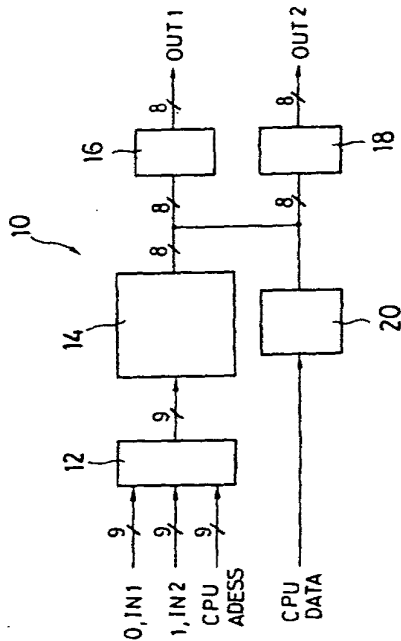


FIG. 2

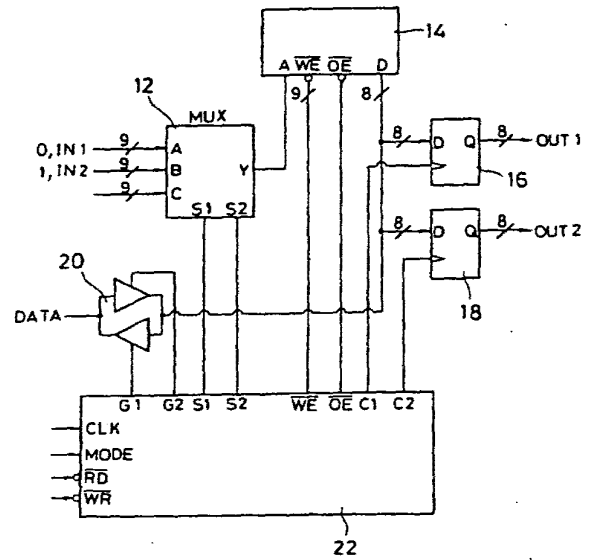


FIG. 3 MODE=0 (CPU アクセス動作) S1=0, S2=1

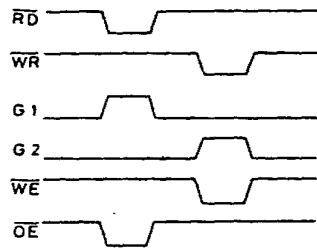
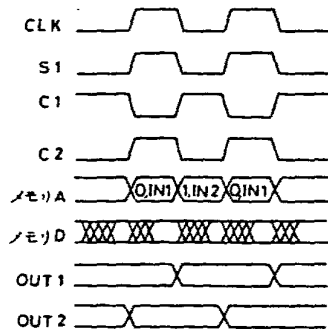


FIG. 4 MODE=1 (リアルタイム動作) S2=0, WE=1, OE=0



手続補正書 (自発)

平成02年03月28日

特許庁長官 吉田 文 毅 殿

1. 事件の表示

平成01年特許願第200701号

2. 発明の名称

ルックアップテーブル装置

3. 補正をする者

事件との関係 特許出願人

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氏 名 (8015) 弁理士 旗 辺 望 祐

5. 補正の対象

明細書の「発明の詳細な説明」の欄

および図面 (第2図および第4図)



方 式 審 査 関

6. 補正の内容

(1) 明細書第13頁第20行～第14頁第1行目の「 2^M または 2^M-1 個」を「 $(2^{M-1}+1)$ 個ないし 2^M 個」に訂正する。

(2) 同第14頁第2行目の「 $2^M \cdot N$ 本または $(2^M-1) \cdot M$ 本」を「 $(2^{M-1}+1) \cdot N$ 本または $2^M \cdot N$ 本」に訂正する。

(3) 同第18頁第14行目の「端子...」を「端子」を示す。また $\overline{OE}$ および $\overline{WE}$ に訂正する。

(4) 同第20頁第5行目の「入出力のタイミング制御」を「サンプリングクロック」に訂正する。

(5) 同第22頁第15行目の「タイミング制御」を「サンプリングクロック」に訂正する。

(6) 同第23頁第17行目の「諧調」「階調」に訂正する。

(7) 図面第2図および第4図を別紙の通り訂正する。

FIG. 2

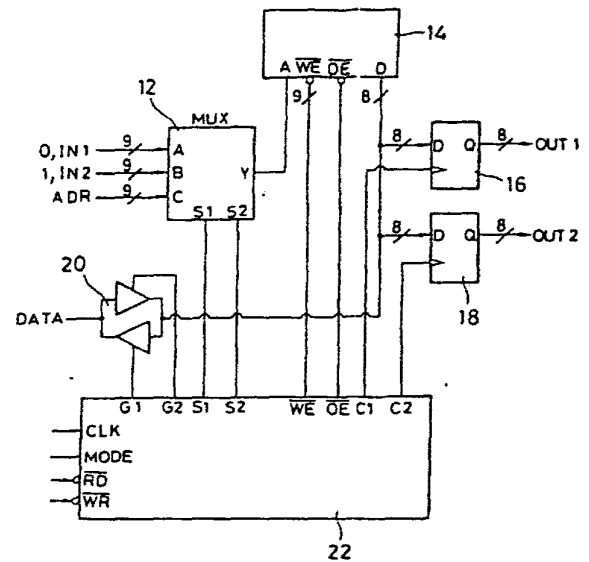
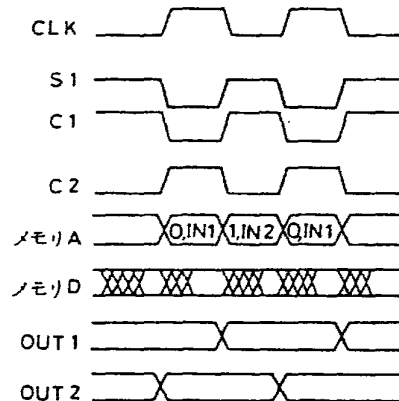


FIG. 4

MODE=1 (リアルタイム動作) S2=0, $\overline{WE}=1$, $\overline{OE}=0$ 

PATENT ABSTRACTS OF JAPAN

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(51)Int.Cl.

H03K 19/177
G11C 11/413
H01L 21/82

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(71)Applicant : AT & T CORP
(72)Inventor : WOO NAM-SUNG

(30)Priority

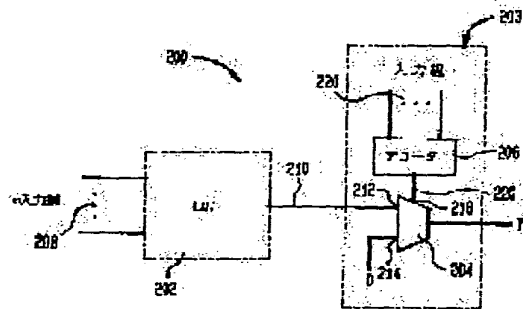
Priority number : 94 304013 Priority date : 09.09.1994 Priority country : US

(54) FIELD PROGRAMMABLE GATE ARRAY

(57)Abstract:

PROBLEM TO BE SOLVED: To increase the number of inputs of each programmable logic cell(PLC) by providing a decoder circuit arrangement A which performs operation to increase the number of inputs of the PLC and connecting the arrangement A to a lookup table of each PLC.

SOLUTION: Each PLC 200 consists of a decoder circuit arrangement 203 provided with multiplexer MUX 204 and a decoder circuit 206 and a lookup table(KUT) 202. The LUT 202 executes a Boolean network having m input lines 208, and an output line 210 is connected to one input terminal 212 out of a pair of input terminals of the MUX 204, and an input terminal 214 is connected to default value 0. A circuit 206 to which an address selector terminal 218 of the MUX 204 is connected outputs H or L to an output line 220 by the combinational value of L input lines 220. Thus, the number of inputs of each PLC is increased by the corresponding number of inputs of the circuit 206 to enhance the capability.



LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

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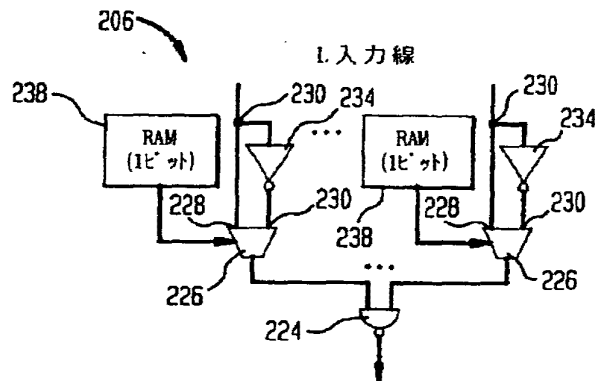
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(54)【発明の名称】 フィールドプログラマブルゲートアレイ

(57)【要約】

【目的】 複数のPLCを有し、各PLCがそれへの入力数を増加させるよう動作可能なデコーダ回路配置を提供する。

【構成】 各プログラマブルロジックセルの入力数を増加させるデコーダ回路配置を備えたフィールドプログラマブルゲートアレイのプログラマブルロジックセル。デコーダ回路配置は、各プログラマブルロジックセルのルックアップテーブルに接続する。



【特許請求の範囲】

【請求項1】 フィールドプログラマブルゲートアレイからなる集積回路であって、

(a) 複数の入力端子と1つの出力端子を有する少なくとも1つのルックアップテーブルと、

(b) 前記少なくとも1つのルックアップテーブルの出力端子に接続されたデコーダ回路配置とからなり、前記デコーダ回路配置は、(i) アドレスセクタ端子と、前記少なくとも1つのルックアップテーブルの出力端子に接続された少なくとも1つの入力端子とを有する多重化回路と、(ii) 複数の入力端子を有し、前記多重化回路のアドレスセクタに接続されたデコーダ回路を含むことを特徴とする集積回路。

【請求項2】 請求項1記載の集積回路において、前記多重化回路は、前記少なくとも1つのルックアップテーブルの出力端子に接続された第1の入力端子と、不履行値に接続された第2の入力端子とを有する2対1マルチプレクサを含み、前記2対1マルチプレクサは、前記デコーダ回路を、前記マルチプレクサの前記第1及び第2の入力端子間に前記マルチプレクサの出力端子を選択的に接続可能にさせる、前記デコーダ回路に接続された前記アドレスセクタを有する集積回路。

【請求項3】 請求項2記載の集積回路において、前記デコーダ回路配置は、さらに、前記第2の入力端子に接続され、前記不履行バルブを提供するように動作可能な1ビットスタティックRAMを含む集積回路。

【請求項4】 請求項1記載の集積回路において、前記デコーダ回路は、複数の入力端子と、前記多重化回路のアドレスセクタに接続された出力端子とを有するNANDロジックゲートを含む集積回路。

【請求項5】 請求項4記載の集積回路において、前記NANDゲートの各入力端子は2対1マルチプレクサに接続されている集積回路。

【請求項6】 請求項5記載の集積回路において、各々の前記2対1マルチプレクサは、その各アドレスセクタに接続された1ビットスタティックRAMを含む集積回路。

【請求項7】 多数のプログラマブルロジックセルを有するフィールドプログラマブルゲートアレイ集積回路であって、各プログラマブルロジックセルは、

(a) 各々が複数の入力端子と1つの出力端子を有する複数のルックアップテーブルと、

(b) 前記各ルックアップテーブルの各出力端子に接続された入力端子を有する第1のマルチプレクサ回路と、

(c) 前記第1の多重化手段の出力端子に接続されたデコーダ回路配置とからなり、前記デコーダ回路配置は、

(i) 前記第1の多重化手段の出力に接続された入力を有する第2のマルチプレクサ回路と、(ii) 複数の入力を有し、前記第2の多重化手段のアドレスセクタに接続されたデコーダ回路とを含むことを特徴とするフィ

ールドプログラマブルゲートアレイ集積回路。

【請求項8】 請求項7記載のフィールドプログラマブルゲートアレイにおいて、前記第1の多重化手段は、前記第1及び第2のルックアップテーブルに接続された各入力端子を有する2対1マルチプレクサであるフィールドプログラマブルゲートアレイ。

【請求項9】 請求項8記載のフィールドプログラマブルゲートアレイにおいて、前記第2の多重化手段は、前記第1の2対1マルチプレクサの出力に接続された第1の入力と、前記デコーダ回路に接続されたアドレスセクタとを有する第2の2対1マルチプレクサを含むフィールドプログラマブルゲートアレイ。

【請求項10】 請求項9記載のフィールドプログラマブルゲートアレイにおいて、1ビットスタティックRAMは前記第2の2対1マルチプレクサの第2の入力に接続されているフィールドプログラマブルゲートアレイ。

【請求項11】 請求項10記載のフィールドプログラマブルゲートアレイにおいて、前記デコーダ回路は、複数の入力端子と、前記第2の2対1マルチプレクサのアドレスセクタに接続された1つの出力端子を有するNANDロジックゲートを含むフィールドプログラマブルゲートアレイ。

【請求項12】 請求項11記載のフィールドプログラマブルゲートアレイにおいて、前記NANDゲートの各入力端子は2対1マルチプレクサに接続されているフィールドプログラマブルゲートアレイ。

【請求項13】 多数のプログラマブルロジックセルを有するフィールドプログラマブルゲートアレイ集積回路であって、各プログラマブルロジックセルは、

(a) 各々が複数の入力端子と1つの出力端子を有する複数のルックアップテーブルと、

(b) 各々が前記ルックアップテーブルの出力端子に接続された入力端子を有する複数のマルチプレクサ回路と、

(c) 各々が前記マルチプレクサ回路アドレスセクタに接続された複数のデコーダ回路配置と、

(d) 各々が前記各マルチプレクサ回路の出力端子に接続された複数の入力端子と、1つの出力端子とを有するロジック制御回路とからなることを特徴とするフィールドプログラマブルゲートアレイ集積回路。

【請求項14】 請求項13記載のフィールドプログラマブルゲートアレイにおいて、前記ロジック制御回路はNANDゲートであるフィールドプログラマブルゲートアレイ。

【請求項15】 請求項14記載のフィールドプログラマブルゲートアレイにおいて、前記各マルチプレクサ回路は2対1マルチプレクサであるフィールドプログラマブルゲートアレイ。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】本発明は、集積回路半導体チップに形成されたプログラマブルロジック装置に関し、特に、フィールドプログラマブルゲートアレイチップの一部であるロジックセルに関する。

【0002】

【従来の技術及び発明が解決しようとする課題】集積回路（IC）は、伝統的に、1つの機能、またはソフトウェアプログラミングで定義された複数の機能を実行した。しかしながら、いずれの場合にも、機能を実行したロジック構成はICの設計の間に決定された。もっと最近には、ロジック構成を製造後に変更できる集積回路が開発されている。例えば、ロジック機能をユーザーが確立することができるフィールドプログラマブルゲートアレイ（FPGA）が開発されている。典型的には、このロジック機能はプログラマブルファンクションユニット（PFU）で実行される。このPFUは、一般的に、望ましいロジック及びメモリ機能を実行するために望ましい配置に接続することができる種々のロジック回路素子（例えば、ANDゲート、ORゲート、NANDゲート、NORゲート、フリップフロップ、ルックアップテーブルメモリ、マルチプレクサ、レジスタ、ラッチ、3状態バッファ）を含んでいる。例えば、典型的なロジック機能は、組合せロジック、アダー、カウンタ及び他のデータパス機能を含んでいる。組合せロジックは典型的にルックアップテーブル（LUT）を用いて実行されるのに対して、逐次ロジックは典型的にフリップフロップやラッチのような記憶素子（レジスタ）を用いて実行される。

【0003】上述のように、各ロジックセル（すなわちPLC：プログラマブルロジックセル）は、ルックアップテーブル（LUT）を用いて組合せロジック機能を実行する。典型的には、LUTは、スタティックランダムアクセスメモリ（RAM）を用いて、各PLCの組合せロジック機能に従ってブールの機能を実行する。

“K”は、ブールのネットワークに接続してFPGAの個々のPLCで実行することができる最大入力数を示すことになるのを注意されたい。典型的には、Kの値が増加するにつれて、アプリケーション回路（FPGAチップで実行される回路）を実行するのに必要とされる（PLCと同様な）LUTのレベル（例えば深さ）の数は減少し、これは時間遅延をほとんどなくする（回路速度を高める）。したがって、大きなK値を持つPLCを備えることが望ましいことがある。

【0004】例えば、図1は先行技術のPLC150のLUT152のブロック図を示す。詳細には、LUT152は、PLC150に4入力（例えばK=4）までのブール機能を実行させることができる16ビットRAMである。図2は、先行技術のPLC160のF及びGLUT162及び164のブロック図を示す。F及びGLUT162及び164は両方とも16ビットRA

Mであり、PLC160に、PLC160の回路構成に対応して5入力A1、A2、A3、A4及びA5（K=5）までのブール機能を実行させることができる（入力A2、A3及びA4はF及びGLUTの両方に共通になっている）。図3は、PLC170にその回路構成に関連して9入力（A1乃至A9）（K=9）までのいくつかのブール機能を実行させることができる、8ビット

H LUT172に接続された上述のF及びGLUT162及び164の各出力を有するFPGA PLC170のブロック図を示す。

【0005】したがって、PLCにおけるLUTの特定のサイズ（RAM）とそれらの回路構成は、特定のPLCのK値を決定する。例えば、上述のPLC150（図2）には、5のK値を提供する32ビットの結合サイズの16ビットRAM F及びGLUT162及び164が備えられている。対照的に、上述のPLC170（図3）は、（F及びGLUTの入力（A1乃至A4及びA6乃至A9）は互いに独立している）8のK値を提供する32ビットの結合サイズの同等の16ビットRAM F及びGLUTを備えている。さらに、K値を上げるためにF及びGLUT162及び164の出力端子に追加のLUTを加えることができる。例えば、PLC170（図3）に追加されたH-LUT172はK値を1だけ増加させるように機能した。しかしながら、追加のLUTをPLCに追加すると、信号伝搬時間が増加し（例えば、回路速度が減少し）、たいていの回路アプリケーションにとって不利になる。さらに、FPGAにおけるPLCレベルの数が増加すると、それに応じて、FPGAのサイズとコストが共に増加する。

【0006】

【課題を解決するための手段】本発明は、複数のPLCを有し、各PLCが、各PLCへの入力数（K）を増加させるように動作可能なデコーダ回路配置を含む、フィールドプログラマブルゲートアレイに向けられたものである。このデコーダ回路配置は、工程には、各PLCの各LUTに接続され、それにより、PLCの入力数は、上述のデコーダ回路配置の対応する入力数だけ増加する。

【0007】各デコーダ回路配置は、好適には、PLCのLUTに接続されたマルチプレクサ回路を含む。さらに、複数の入力端子と、マルチプレクサ回路のアドレスセクタに接続された出力端子とを有するデコーダ回路が備えられる。好適な実施例では、マルチプレクサ回路は、LUTの出力端子に接続された第1の入力端子と、不履行値に接続された第2の入力端子とを有する2対1MUXを含む。2対1MUXのアドレスセクタは上述のデコーダ回路に接続されて制御される。したがって、本発明のデコーダ回路配置は、回路網FPGAにLUTの追加層を追加する必要性を要することなく、FPGAと関連するブール網の最大入力数（K）を増加させるこ

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とによって、各PLCの能力を増加させる。本発明の上記の特徴は、添付図面と共に行なわれる以下の本発明による装置の一実施例の詳細な説明の参照により、容易に明らかになり理解できるだろう。

【0008】

【発明の実施の形態】次に図面を参照すると、同じ参照数字は同じすなわち同等の構成要素を識別する。図4は、本発明のデコーダ回路配置203に接続されたルックアップテーブル(LUT)202を含むプログラマブルロジックセル(PLC)200の一部を示す。最も簡単な実施例におけるデコーダ回路配置203はマルチプレクサ(MUX)204と従来のデコーダ回路206を含む。市販のFPGA、例えばAT&Tから市販されているORCA FPGA、の集積回路内でPLC200を提供することができるのが当業者にはわかる。一般に、PLC200へのデコーダ回路配置203の提供は、LUT回路網の追加層の追加と関連して上述した欠点を持つことなく、PLC200の入力数(K)を増加させる機能がある。

【0009】図4を参照すると、例として、LUT202は、2^mビット級のものであり、そのため、m入力208(例えばK=m)を有するブール網を実行することができる。例えば、LUT202は、16ビット級(2^m=16, m=4)のものならば、4入力(K=4)までを有するブール網を実行するのに適応している。LUT202の出力線210は、好適には2対1のMUX204の第1の入力端子212に接続されている。MUX204の第2の入力端子214はデフォルト値(0)に接続されている。MUX204のアドレスセクタ端子218はデコーダ回路206に接続されている。周知のとおり、このようなデコーダ回路206は、入力信号の組合せを、入力組合せ信号に相当する1つの出力信号に変換する装置である。例として、デコーダ回路206はL入力線220を有するように適応されている。したがって、このデコーダ回路206は、L入力220の組合せ値に依存してその出力端子(線220)にロジックハイ(1)またはロジックロー(0)出力のどちらかを持つように動作する。デコーダ回路206の変換方式は、デコーダ回路206の特定の入力組合せ値に依存してロジックハイ(1)またはロジックロー(0)出力値を持つように容易に構成することができるのが当業者にはわかる。

【0010】また、従来のように、MUX204のアドレスセクタ218に入力される値(例えば0乃至1)は、どの入力端子(212または214)が出力端子Yに接続されるべきかを選択する決定力がある。好適には、MUX204はアクティブロー(0)になるように適応され、そのため、デコーダ回路206の出力(線220)がロジックロー(0)の場合、MUX204の第1の入力端子212はその出力Yに接続される。例え

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ば、デコーダ回路206の出力がロジックロー(0)ならば、MUX204のY出力値は、出力線210を介してLUT202の出力値と等しくなる。デコーダ回路206の出力がロジックハイ(1)ならば、MUX204のY出力値は、第2の入力端子214の不履行値(0)に等しくなる。

【0011】したがって、図4に関して上記に説明したように、PLC200は、m+L入力(K=m+L)が提供され、それにより、その中に最大m+L入力を有するブール機能を実行する能力が与えられる。例えば、LUT202が8ビットLUT(m=3)であり、かつデコーダ回路206が5入力(L=5)を持つように構成されている場合は、PLC200は、最大8入力(K=8=3+5)を有するブール機能を実行する能力が与えられる。したがって、デコーダ回路配置203は、PLC200の入力数(K)を(L)の係数だけ増加させるように動作する。

【0012】次に図5a乃至5cを参照すると、図4のデコーダ回路206の他の好適な実施例が示されている。図5aは、L入力端子を持つ従来のNANDゲート222の形態を有するデコーダ回路206を示している。図5bは、L入力端子を持ち、各入力端子が2対1MUX226に接続されているNANDゲート224の形態のデコーダ回路206を示している。各2対1マルチプレクサ226は、共通ノード232、ここでは中間ノード232と関連する各入力端子228、230を有し、入力端子230は従来のインバータ234である。MUX226のアドレスセクタ236は、1ビットスタティックランダムアクセスメモリ(RAM)238に接続されて制御される。図5cは、第1及び第2のトランジスタ240及び242から構成される図5bのMUX226を示し、各トランジスタ240、242のベースは1ビットスタティックRAM238に接続され、それにより作動または不動作にされる。図4のデコーダ回路206は、多数の回路方式で構成することができ(例えば、NANDゲート224をANDゲートに代えても良い)、図5に示されたものに制限されるべきでないことがわかる。

【0013】図6は、本発明によるPL250におけるデコーダ回路配置245のさらに他の好適な実施例を示す。デコーダ回路配置245は、MUX204の第2の入力端子214が1ビットスタティックRAM252に接続されているほかは、図4のデコーダ回路配置203と実質的に同じである。RAM252の提供は、ユーザーに、MUX204を0または1のどちらかの不履行値を持つように適応させる能力を与える。

【0014】図7は、既存のFPGAへの本発明のデコーダ回路配置の提供の一例を示す。図7には、上述のAT&T ORCA FPGAのPLC300への図6のデコーダ回路配置245の提供が示されている。便宜

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上、ORCA FPGAの上部の2つのLUT302, 304のみが示されていることを理解すべきである。LUT302及び304は16ビットLUTであり、各LUT302, 304には4入力($m=4$)が備えられている。各LUT302, 304の3つの入力は互いに接続されており(A1, A2及びA3)、そのため、LUT302及び304の合計入力数は5になっている($m=5$, A0, A1, A2, A3及びA4)。各LUT302及び304の出力は、それぞれ線308及び310を介して2対1マルチプレクサ306に接続されている。MUX306の出力は線312を介して上述のMUX204の第1の入力端子212に接続されている。したがって、上述のデコーダ回路配置245は、ORCA FPGAのPLC300と協動的に機能する能力が与えられ、上述のように、PLC300の入力数をL(デコーダ回路206の入力数)だけ増加させるように動作する。例えば、デコーダ回路206が3入力($L=3$)を持つように適応されている場合は、PLC300の合計入力数(K)は8になる($K=8=5+3=m+L$)。

【0015】次に図8を参照すると、本発明のデコーダ回路351を提供した上述のORCA FPGAのPLC350の他の好適な実施例が示されている。PLC350は、図7のPLC300の2つの2対1MUX306, 204と対照的に4対1MUX360が提供されていることを除いて、図7のPLC300と実質的に同じである。PLC350は上述の16ビットLUT302, 304を含み、LUT302, 304の各出力(線303及び305)は、それぞれ、線352, 354を介してMUX360の第1及び第2の入力端子362, 364に入力されている。L入力デコーダ回路206はMUX360の第1のアドレスセクタ端子372に接続され、MUX360の入力端子366及び368は、0または1のどちらかのデフォルト値を提供するように動作する1ビットスタティックRAM373に接続されている。

【0016】動作時、デコーダ回路206の出力がアクティブロー(0)ならば、MUX360の出力(Y)は、第2のアドレスセクタ端子374に入力される値に依存して、入力端子362, 364を介して、LUT302またはLUT304の出力値のどちらかから選択される。したがって、MUX360の出力(Y)はLUT302またはLUT304のどちらかの値を有する。デコーダ回路206の出力が非能動(1)ならば、MUX360の出力(Y)は入力端子366, 368を介してRAM373の出力と等しくなる。

【0017】上述のデコーダ回路配置351は、FPGAのLUTのどれにでも接続することができ、FPGAの上部の2つのLUTに制限されるべきでないことがわかる。したがって、上述のように、特定のPLCに用いられる各デコーダ回路配置は、その特定のPLCの入力

8

数(K)を相応じて増加させるのに有効である。

【0018】本発明をさらに例示するため、一例として、8入力組合せロジック機能が表Aに示されている。この機能は、典型的に、もくろまれたアプリケーションには多過ぎる変数を有し、したがって、もっと少ない機能群に“分解”しなければならないことが当業者にはわかる。表Bは、市販のソフトウェア、例えばユー・シー・パークレイ(U.C.Berkley)からのSIS 1.1、で発生する3つのより少ない組合せ機能を示す。表Bに示された3機能の組合せは、論理的に、以下に示されるような表Aに示された機能と同等である。

【0018】

【表1】

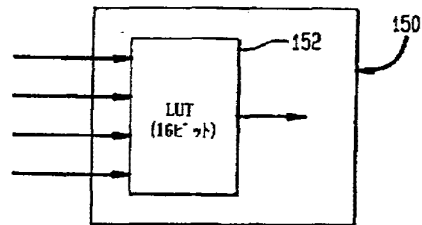


表 A

【表2】

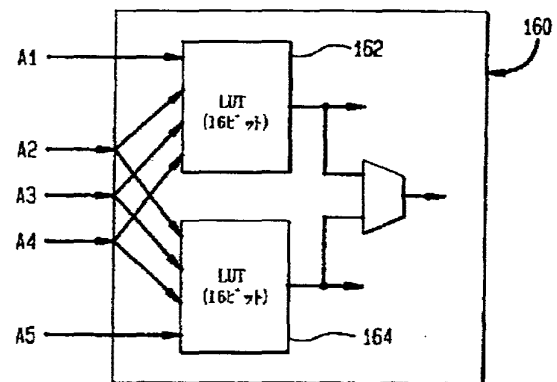


表 B

【0019】表A及びBに示された上述のロジック機能は、図9に示されるような2つのPLC(PLC400及びPLC420)を提供する上述の先行技術のAT&T ORCA FPGAにおいて実行することができる。

PLC400において、LUT T3及びT4(402)は“tmp1”カバー出力を供給し、LUT T1及びT0(404)は“tmp2”カバー出力を供給し、LUT T3及びT2(402)とLUT T1及びT0(404)には、それぞれ4入力(a1, a3, a5, a6, a7)が提供されている。tmp1及びtmp2カバー出力は、それぞれ、PLC420のLUT T3及びT2(406)に入力され、LUT T3及びT2(406)には追加の入力(a2, a4, a8)が提供されている。PLC420のLUT T3及びT2(406)は“y”カバー出力(線422)を供給す

る。上述した図9のFPGA回路配置は、8入力を有する'y'カバーを提供するためにPLC400、420の2つのレベルを必要としたことが注目される。したがって、上述の入力信号(a1乃至a8)は、'y'カバー出力信号が発生する前に、PLC400、420の2つのレベルによって処理する必要があった。ゆえに、上述のように、追加のPLC420レベルは、FPGAの信号伝搬時間とコストの増加ばかりでなく、PLC420を適応させるのに要するFPGAの全体サイズの増加をもたらす。

【0020】図9の先行技術のFPGAと対照的に、図10は、本発明のデコード回路配置を提供する上述のAT&T ORCA FPGAのPLC450を示す。PLC450は、各々がそれぞれ上述の5入力(m=5) a1, a3, a5, a6及びa7を有するLUT T3及びT2(452)とLUT T1及びT0(454)を含んでいる。LUT T3及びT2(452)からの'tmp1'出力は2対1MUX456に接続され、LUT T1及びT0(454)からの'tmp2'出力は2対1MUX458に接続されている。MUX456はデコード回路460に接続されたアドレスセクタ457を備え、MUX458はデコード回路462に接続されたアドレスセクタ459を備えている。各MUX458、460の出力(線470及び472)は、それぞれ、その出力が'y'カバーを提供するNANDゲート464に接続されている。デコード回路460及び462には、それぞれ、上述の3入力(L=3) a2, a4及びa8が提供されている。特に、デコード回路460は、入力a2, a4及びa8がそれぞれ010の時にアクティブロー(0)になるように適応され、デコード回路462は、入力a2, a4及びa8がそれぞれ101の時にアクティブロー(0)になるように適応されている。

【0021】したがって、本発明による図10のFPGA回路配置は、図9の先行技術のFPGA回路配置と比較して、同じ8入力(K=8, a1乃至a8)を用いて同等の'y'出力を提供する。しかしながら、図10のFPGA回路配置は、上述の図9の先行技術のFPGA回路配置が2つのPLC400、420を必要としたのと対照的に、1つだけのPLC450を用いることにより前記の同等の結果を達成している。したがって、本発明のFPGA回路配置(図10)は、全体サイズが小さくなり、遅延時間が減少し(入力信号は1つのPLC4

50で処理することを要するだけである)、PLC400及び420の2つのレベルを要する先行技術のFPGA回路配置と比較して回路のコストが減少するという利点がある。

【0022】ここで開示されたものは単に本発明の原理の応用例に過ぎない。他の配置及び方法は、本発明の精神と範囲を逸脱することなく当業者により提供され得る。

【図面の簡単な説明】

10 【図1】先行技術の回路構成のプログラマブルロジックセルのブロック図を示す。

【図2】先行技術の他の回路構成のプログラマブルロジックセルのブロック図を示す。

【図3】先行技術の他の回路構成のプログラマブルロジックセルのブロック図を示す。

【図4】本発明を具体化したデコード回路配置を実行するプログラマブルロジックセルを示す。

【図5A】図4のデコード回路配置の他の回路構成の1を示す。

20 【図5B】図4のデコード回路配置の他の回路構成の2を示す。

【図5C】図4のデコード回路配置の他の回路構成の3を示す。

【図6】デコード回路配置のマルチプレクサの入力不履行値を決定するように動作可能な1ビットスタティックRAMを備えた、図4のデコード回路配置を示す。

【図7】第1及び第2のルックアップテーブルを有するプログラマブルロジックセルに用いられた図6のデコード回路配置を示す。

30 【図8】4対1マルチプレクサを含む図7のデコード回路配置を示す。

【図9】互いに縦続接続された2つのプログラマブルロジックセルを有する、先行技術のFPGAを示す。

【図10】本発明を具体化したデコード回路配置を含む1つのプログラマブルロジックセルを有するFPGAを示す。

【符号の説明】

202 LUT

204 MUX

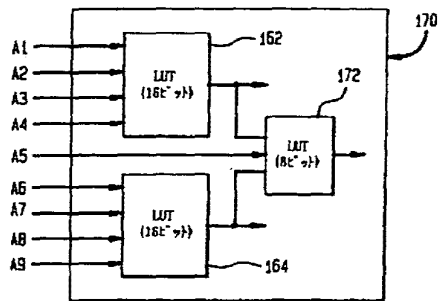
40 206 デコード回路

208 m入力

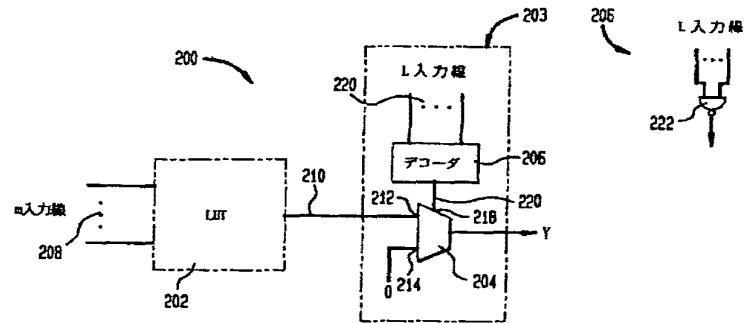
210 出力線

214 入力端子

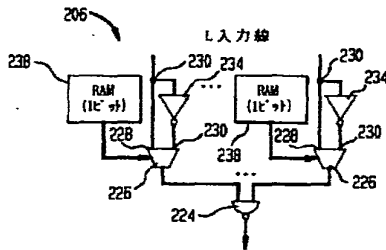
【図1】



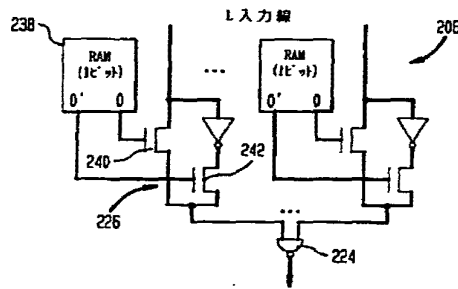
【図2】



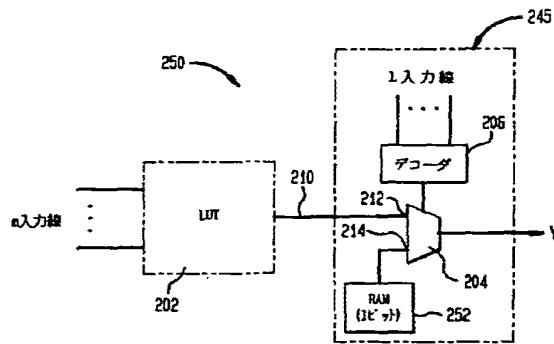
【図4】



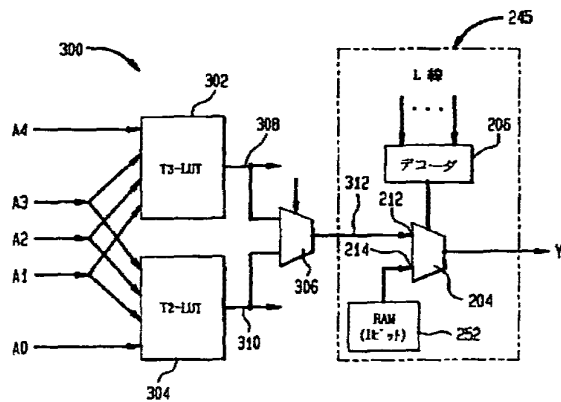
【図5】



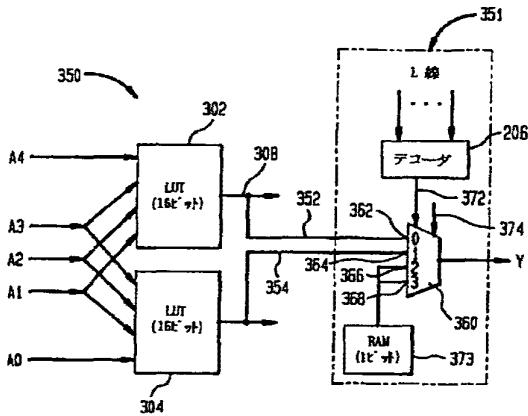
【図6】



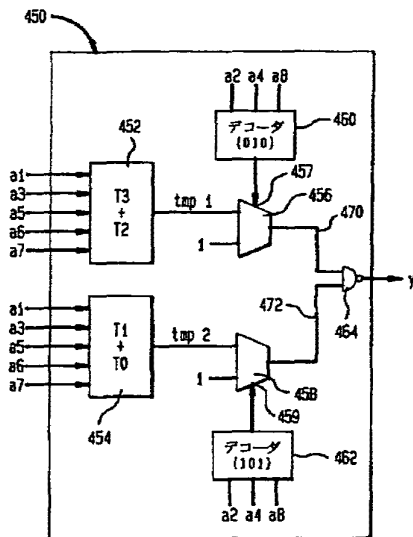
【図7】



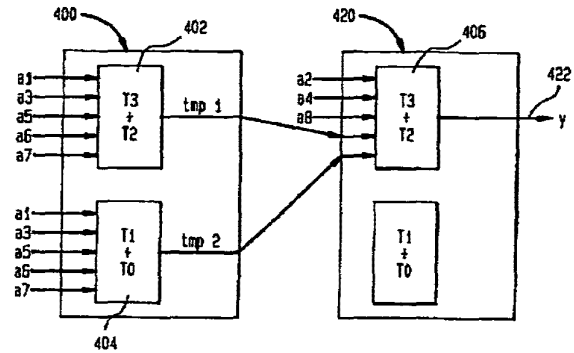
【図8】



【図10】



【図9】



【手続補正書】

【提出日】平成8年1月8日

【手続補正1】

【補正対象書類名】明細書

【補正対象項目名】図面の簡単な説明

【補正方法】変更

【補正内容】

【図面の簡単な説明】

【図1】 先行技術の回路構成のプログラマブルロジックセルのブロック図を示す。

【図2】 先行技術の他の回路構成のプログラマブルロジックセルのブロック図を示す。

【図3】 先行技術の他の回路構成のプログラマブルロジックセルのブロック図を示す。

ックセルのブロック図を示す。

【図4】 本発明を具体化したデコーダ回路配置を実行するプログラマブルロジックセルを示す。

【図5】 図4のデコーダ回路配置の他の回路構成を示す。

【図6】 デコーダ回路配置のマルチプレクサの入力不履行値を決定するように動作可能な1ビットスタティックRAMを備えた、図4のデコーダ回路配置を示す。

【図7】 第1及び第2のルックアップテーブルを有するプログラマブルロジックセルに用いられた図6のデコーダ回路配置を示す。

【図8】 4対1マルチプレクサを含む図7のデコーダ回

路配置を示す。

【図9】互いに縦続接続された2つのプログラマブルロジックセルを有する、先行技術のFPGAを示す。

【図10】本発明を具体化したデコード回路配置を含む1つのプログラマブルロジックセルを有するFPGAを示す。

【符号の説明】

202	LUT
204	MUX
206	デコード回路
208	m入力
210	出力線
214	入力端子



Corres. and Mail
BOX AF

RESPONSE UNDER 37 CFR 1.116
EXPEDITED PROCEDURE
EXAMINING GROUP 2819
Docket No.: 1687.1001

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Toshinori SUEYOSHI, et al.

Serial No. 10/183,590

Group Art Unit: 2819

Confirmation No. 9469

Filed: June 28, 2002

Examiner: Anh Q. Tran

For: PROGRAMMABLE LOGIC CIRCUIT DEVICE HAVING LOOK UP TABLE ENABLING
TO REDUCE IMPLEMENTATION AREA

AMENDMENT AFTER FINAL REJECTION

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Attention: **BOX AF**

Sir:

This is in response to the Office Action mailed March 3, 2004, and having a period for response set to expire on June 3, 2004. A petition and fee for a one-month Extension of Time is enclosed, thereby extending the response period to July 3, 2004.

Reconsideration of the claims is respectfully requested. The following remarks are respectfully submitted.

07/02/2004 YPOLITE1 00000110 10183590

01 FC:1251

110.00 0P

IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

1. (PREVIOUSLY PRESENTED) A look up table of M inputs and N outputs, comprising:

- a plurality of LUT units; and
- an internal configuration control circuit controlling an internal configuration of said plurality of LUT units, wherein said internal configuration control circuit comprises
 - a plurality of selectors selecting I/O signals of said plurality of LUT units, and
 - a selector control circuit having a memory, controlling said plurality of selectors in accordance with data stored in said memory, and defining the internal configuration of said plurality of LUT units.

2 –3 CANCELLED

4. (PREVIOUSLY PRESENTED) The look up table as claimed in claim 1, wherein said plurality of selectors include:

- an input signal selector provided at an input of at least one of said LUT units to select an input signal; and

- an output signal selector provided at an output of said LUT units selecting an output signal, said input signal selector and said output signal selector being controlled in accordance with the data stored in said memory.

5. (PREVIOUSLY PRESENTED) The look up table as claimed in claim 1, wherein said plurality of selectors include:

- an input signal selector provided at an input of at least one of said LUT units to select an input signal; and

- an output signal selector provided at an output of said LUT units selecting an output signal, said input signal selector and said output signal selector being controlled in accordance

with the input signal.

6. (ORIGINAL) The look up table as claimed in claim 1, wherein said look up table of M inputs and N outputs is a 6-input 3-output look up table.

7. (ORIGINAL) The look up table as claimed in claim 6, wherein said 6-input 3-output look up table comprises eight 3-input 1-output LUT units.

8. (ORIGINAL) The look up table as claimed in claim 6, wherein said 6-input 3-output look up table comprises four 3-input 2-output LUT units.

9. (PREVIOUSLY PRESENTED) A programmable logic circuit device comprising: a plurality of logic blocks;

a plurality of routing wires connected to each of said logic blocks;

a plurality of switch circuits provided at an intersection of each of said routing wires;

a plurality of connection blocks provided between an I/O line of each of said logic blocks and each of said routing wires; and

an I/O block performing an input/output operation with external equipment, wherein each of said logic blocks has a look up table of M inputs and N outputs, comprising:

a plurality of LUT units; and

an internal configuration control circuit controlling an internal configuration of said plurality of LUT units, wherein said internal configuration control circuit comprises

a plurality of selectors selecting I/O signals of said plurality of LUT units, and

a selector control circuit having a memory, controlling said plurality of selectors in accordance with data stored in said memory, and defining the internal configuration of said plurality of LUT units.

10 – 11 CANCELLED

12. (PREVIOUSLY PRESENTED) The programmable logic circuit device as claimed in claim 9, wherein said plurality of selectors include:

an input signal selector provided at an input of at least one of said LUT units to select an input signal; and

an output signal selector provided at an output of said LUT units selecting an output signal, said input signal selector and said output signal selector being controlled in accordance with the data stored in said memory.

13. (PREVIOUSLY PRESENTED) The programmable logic circuit device as claimed in claim 9, wherein said plurality of selectors include:

an input signal selector provided at an input of at least one of said LUT units to select an input signal; and

an output signal selector provided at an output of said LUT units selecting an output signal, said input signal selector and said output signal selector being controlled in accordance with the input signal.

14. (ORIGINAL) The programmable logic circuit device as claimed in claim 9, wherein said look up table of M inputs and N outputs is a 6-input 3-output look up table.

15. (ORIGINAL) The programmable logic circuit device as claimed in claim 14, wherein said 6-input 3-output look up table comprises eight 3-input 1-output LUT units.

16. (ORIGINAL) The programmable logic circuit device as claimed in claim 14, wherein said 6-input 3-output look up table comprises four 3-input 2-output LUT units.

17. (PREVIOUSLY PRESENTED) A method of configuring a look up table of M inputs and N outputs, comprising:

providing a plurality of LUT units; and

selectively controlling I/O signals of said plurality of LUT units to set a predetermined mode of an internal configuration.

18. (ORIGINAL) The method of configuring a look up table as claimed in claim 17, wherein the I/O signals of said plurality of LUT units are selectively controlled in accordance with data stored in the corresponding look up table.

19. (ORIGINAL) The method of configuring a look up table as claimed in claim 17, wherein an input signal input to at least one of said LUT units and an output signal output from

said LUT unit are selectively controlled in accordance with data stored in the corresponding look up table.

20. (ORIGINAL) The method of configuring a look up table as claimed in claim 17, wherein an input signal input to at least one of said LUT units and an output signal output from said LUT unit are selectively controlled in accordance with a predetermined function of the input signal.

REMARKS

It is respectfully noted that on the Office Action Summary, claims 1, 4-6, 9, and 12-20, which is inclusive of claims 15-16, are rejected. Furthermore, on page 3 of the Office Action, claims 7 and 8 are rejected in view of FIG. 10 of U.S. Patent No. 6,323,677 to Lane et al. However, on page 4 of the Office Action, it is indicated that claims 7-8 and 15-16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form.

It is respectfully requested that it be noted in subsequent actions that claims 7, 8, 15, and 16 are not rejected but objected to.

In accordance with the foregoing, claims 1, 4-6, 9, 12-14, and 17-20 stand rejected and claims 7, 8, 15, and 16 stand objected to.

Claims 1, 4-9, and 12-20 are pending and under consideration.

REJECTION UNDER 35 U.S.C. § 102:

In the Office Action, at page 2, claims 1-20 were rejected under 35 U.S.C. § 102 in view of U.S. Patent No. 6,323,677 to Lane et al. ("Lane"). This rejection is traversed and reconsideration is requested.

Lane generally describes a programmable logic device circuitry for improving multiplier speed and/or efficiency. Contrary to the assertions made in the Office Action, Lane fails to teach or suggest, "an internal configuration control circuit controlling an internal configuration of said plurality of LUT units," as recited in independent claims 1 and 9. Rather, Lane provides a PLC 102, which is programmable by function control element 104, to output either input C or an inverted carry in signal. See column 4, lines 40-53. An output signal of PLC 102 is a third input to look-up table (LUT) 110a and also to the control input terminal of PLC 120b. For instance, logic module 100a is used as a four-input look-up table, FCE and RSELC is programmed logic 1 to cause PLC 102 to select the C input (rather than CIN) for application to one input of look-up table 110a and to the control input of PLC 120b. See column 6, line 27-31. Nothing in Lane teaches or suggests that the inputs to the LUT 110a are used to control the internal configuration

thereof.

Further, look-up tables 110 in Lane are programmed so that logic module 100b combines Q, A, and CIN in a sense indicated by input B in order to provide an up or down counter. See column 8, lines 14-26. In other words, the direction of counting is indicated by input B, and counting is enabled by input A. Thus, rather than controlling the internal configuration of the look-up tables in Lane, the input signals to these tables are used to trigger counting.

In addition, although Lane generally provides that components of PLCs can be controlled by various, programmable, function control elements ("FCEs"), that alone does not teach or suggest that FCEs are also controlling the internal configuration of the LUTs. Rather, based on the description of the system in Lane, and, for instance, the specific sections previously discussed of Lane, the FCEs merely cause PLCs to select an input signal for application to one of the LUTs and allow the LUTs to process the input signal and generate an output signal as pre-programmed. There is no actual control of the internal configuration of the LUTs.

Further, Lane fails to teach or suggest, "selectively controlling I/O signals of said plurality of LUT units **to set a predetermined mode of an internal configuration,**" emphasis added, as recited in independent claim 17. Rather, a PLC in Lane selects an input for application to an LUT and to the control input of a PLC. The PLC may be programmed to select an output signal of one of the LUTs. There is no setting of a predetermined mode of an internal configuration of the LUTs in Lane.

Thus, Lane fails to teach or suggest all the recitations of independent claims 1, 9, and 17. Accordingly, it is respectfully requested that independent claims 1, 9, and 17 and related dependent claims be allowed.

CONCLUSION:

In accordance with the foregoing, it is respectfully submitted that all outstanding objections and rejections have been overcome and/or rendered moot and further, that all pending claims patentably distinguish over the prior art. There being no further outstanding objections or rejections, the application is submitted as being in condition for allowance, which action is earnestly solicited. At a minimum, this Amendment should be entered at least for purposes of Appeal, since it either clarifies and/or narrows the issues for consideration by the Board.

If the Examiner has any remaining issues to be addressed, it is believed that prosecution

can be expedited and possibly concluded by the Examiner's contacting the undersigned attorney for a telephone interview to discuss any such remaining issues.

If there are any underpayments or overpayments of fees associated with the filing of this Amendment, please charge and/or credit the same to our Deposit Account No. 19-3935.

Respectfully submitted,

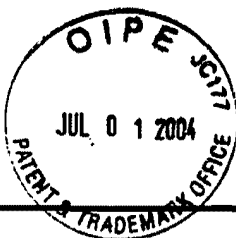
STAAS & HALSEY LLP

Date: July 1, 2004

By:


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IPW AF/2819
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S&H Form: (10/03)



**REPLY/AMENDMENT
FEE TRANSMITTAL**

Attorney Docket No.	1687.1001
Application Number	10/183,590
Filing Date	June 28, 2002
First Named Inventor	Toshinori SUEYOSHI, et al.
Group Art Unit	2819
Examiner Name	Anh Q. Tran

AMOUNT ENCLOSED 110.00

FEE CALCULATION (fees effective 10/01/03)

CLAIMS AS AMENDED	Claims Remaining After Amendment	Highest Number Previously Paid For	Number Extra	Rate	Calculations
TOTAL CLAIMS	20	- 20 =	0	X \$ 18.00 =	\$ 0.00
INDEPENDENT CLAIMS	3	- 3 =	0	X \$ 86.00 =	0.00
Since an Official Action set an <u>original</u> due date of <u>June 3, 2004</u> , petition is hereby made for an extension to cover the date this reply is filed for which the requisite fee is enclosed (1 month (\$110); 2 months (\$420); 3 months (\$950); 4 months (\$1,480); 5					\$110.00
If Notice of Appeal is enclosed, add (\$330.00)					
If Statutory Disclaimer under Rule 20(d) is enclosed, add fee (\$110.00)					
Information Disclosure Statement (Rule 1.17(p)) (\$180.00)					
Total of above Calculations =					\$ 110.00
Reduction by 50% for filing by small entity (37 CFR 1.9, 1.27 & 1.28)					
TOTAL FEES DUE =					\$ 110.00

- (1) If entry (1) is less than entry (2), entry (3) is "0".
(2) If entry (2) is less than 20, change entry (2) to "20".
(4) If entry (4) is less than entry (5), entry (6) is "0".
(5) If entry (5) is less than 3, change entry (5) to "3".

METHOD OF PAYMENT

- ☐ Check enclosed as payment.
- ☐ Charge "TOTAL FEES DUE" to the Deposit Account No. below.
- ☐ No payment is enclosed and no charges to the Deposit Account are authorized at this time (unless specifically required to obtain a filing date).

GENERAL AUTHORIZATION

- ☒ If the above-noted "AMOUNT ENCLOSED" is not correct, the Commissioner is hereby authorized to credit any overpayment or charge any additional fees necessary to:
- Deposit Account No. 19-3935
- Deposit Account Name STAAS & HALSEY LLP
- ☒ The Commissioner is also authorized to credit any overpayments or charge any additional fees required under 37 CFR 1.16 (filing fees) or 37 CFR 1.17 (processing fees) during the prosecution of this application, including any related application(s) claiming benefit hereof pursuant to 35 USC § 120 (e.g., continuations/divisionals/CIPs under 37 CFR 1.53(b) and/or continuations/divisionals/CPAs under 37 CFR 1.53(d)) to maintain pendency hereof or of any such related application.

SUBMITTED BY: STAAS & HALSEY LLP

Typed Name	Alicia M. Choi	Reg. No.	46,621
Signature		Date	July 1, 2004

PATENT APPLICATION FEE DETERMINATION RECORD Effective October 1, 2001				Application or Docket Number <u>101 83 590</u>	
CLAIMS AS FILED - PART I					
		(Column 1)	(Column 2)		
TOTAL CLAIMS		20			
FOR		NUMBER FILED	NUMBER EXTRA		
TOTAL CHARGEABLE CLAIMS		20 minus 20 =			
INDEPENDENT CLAIMS		3 minus 3 =			
MULTIPLE DEPENDENT CLAIM PRESENT		☐			
* If the difference in column 1 is less than zero, enter "0" in column 2					
CLAIMS AS AMENDED - PART II					
		(Column 1)	(Column 2)	(Column 3)	
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR		PAYMENT EXTRA
	Total	20	Minus	20	=
	Independent	2	Minus	3	=
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐				
71-01					
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR		PAYMENT EXTRA
	Total	10	Minus	20	=
	Independent	3	Minus	3	=
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐				
AMENDMENT C	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR		PAYMENT EXTRA
	Total		Minus		=
	Independent		Minus		=
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐				
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. * If the "Highest Number Previously Paid For" in THIS SPACE is less than 20, enter "20." * If the "Highest Number Previously Paid For" in THIS SPACE is less than 3, enter "3." The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.					

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	FEE		RATE	FEE
BASIC FEE	370.00	OR	BASIC FEE	740.00
X\$ 8=		OR	X\$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL		OR	TOTAL	740

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X\$ 8=		OR	X\$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X\$ 9=		OR	X\$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

SMALL ENTITY TYPE ☐		OR	OTHER THAN SMALL ENTITY	
RATE	ADDITIONAL FEE		RATE	ADDITIONAL FEE
X\$ 9=		OR	X\$18=	
X42=		OR	X84=	
+140=		OR	+280=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

Index of Claims



Application No.

10/183,590

Examiner

Anh Q. Tran

Applicant(s)

SUEYOSHI ET AL.

Art Unit

2819

✓	Rejected
=	Allowed

-	(Through numeral) Cancelled
+	Restricted

N	Non-Elected
I	Interference

A	Appeal
O	Objected

Claim	Date
Final	Original
1	2
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Claim	Date
Final	Original
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Claim	Date
Final	Original
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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

21171 7590 08/02/2004
STAAS & HALSEY LLP
SUITE 700
1201 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER

TRAN, ANH Q

ART UNIT

PAPER NUMBER

2819

DATE MAILED: 08/02/2004

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/183,590	06/28/2002	Toshinori Sueyoshi	1687.1001	9469

TITLE OF INVENTION: PROGRAMMABLE LOGIC CIRCUIT DEVICE HAVING LOOK UP TABLE ENABLING TO REDUCE IMPLEMENTATION AREA

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1330	\$300	\$1630	11/02/2004

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE REFLECTS A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE APPLIED IN THIS APPLICATION. THE PTOL-85B (OR AN EQUIVALENT) MUST BE RETURNED WITHIN THIS PERIOD EVEN IF NO FEE IS DUE OR THE APPLICATION WILL BE REGARDED AS ABANDONED.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL should be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). Even if the fee(s) have already been paid, Part B - Fee(s) Transmittal should be completed and returned. If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail**

**Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (703) 746-4000**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

21171 7590 08/02/2004

**STAAS & HALSEY LLP
SUITE 700
1201 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005**

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (703) 746-4000, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/183,590	06/28/2002	Toshinori Sueyoshi	1687.1001	9469

TITLE OF INVENTION: PROGRAMMABLE LOGIC CIRCUIT DEVICE HAVING LOOK UP TABLE ENABLING TO REDUCE IMPLEMENTATION AREA

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1330	\$300	\$1630	11/02/2004

EXAMINER	ART UNIT	CLASS-SUBCLASS
TRAN, ANH Q	2819	326-038000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
 (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
 (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent); ☐ individual ☐ corporation or other private group entity ☐ government

4a. The following fee(s) are enclosed:

- ☐ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s):

- ☐ A check in the amount of the fee(s) is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☐ The Director is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is not claiming SMALL ENTITY status. See, e.g., 37 CFR 1.27(g)(2).

The Director of the USPTO is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above.

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

(Authorized Signature)

(Date)

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TRANSMIT THIS FORM WITH FEE(S)



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/183,590	06/28/2002	Toshinori Sueyoshi	1687.1001	9469
21171	7590	08/02/2004	EXAMINER	
STAAS & HALSEY LLP SUITE 700 1201 NEW YORK AVENUE, N.W. WASHINGTON, DC 20005			TRAN, ANH Q	
			ART UNIT	PAPER NUMBER
			2819	

DATE MAILED: 08/02/2004

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (703) 305-1383. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (703) 305-8283.

me

Notice of Allowability	Application No.	Applicant(s)	
	10/183,590	SUEYOSHI ET AL.	
	Examiner	Art Unit	
	Anh Q. Tran	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 7/01/04.
2. ☒ The allowed claim(s) is/are 1,4-9 and 12-20.
3. ☒ The drawings filed on 28 June 2002 are accepted by the Examiner.
4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☒ All b) ☐ Some* c) ☐ None of the:
 1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
 6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
 - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|---|--|
| <ol style="list-style-type: none"> 1. ☐ Notice of References Cited (PTO-892) 2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08),
Paper No./Mail Date <u>6/28/04</u> 4. ☐ Examiner's Comment Regarding Requirement for Deposit
of Biological Material | <ol style="list-style-type: none"> 5. ☐ Notice of Informal Patent Application (PTO-152) 6. ☐ Interview Summary (PTO-413),
Paper No./Mail Date _____. 7. ☐ Examiner's Amendment/Comment 8. ☒ Examiner's Statement of Reasons for Allowance 9. ☐ Other _____. |
|---|--|

Anh Q. Tran
Examiner
Art Unit: 2819

DETAILED ACTION

Allowable Subject Matter

1. Claims 1, 4-9, 12-20 are allowed.
2. The following is an examiner's statement of reasons for allowance:
3. although the prior art of record discloses control circuit having a memory for controlling a plurality of selectors for selecting LUTs' input signals, but no teaching of controlling and defining an internal configuration of the LUT; with respect to claims 1, 9, and 17, in addition to other limitations in the claims, the prior art of record fails to teach or disclose the applicant's invention as claimed, particularly the feature describing an internal configuration control circuit controlling and defining an internal configuration of the plurality of LUT units.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

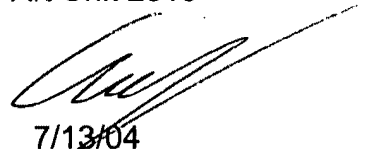
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh Q. Tran whose telephone number is 571-272-1813. The examiner can normally be reached on M-TH (7:00-5:30) Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2819

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Anh Q. Tran
Examiner
Art Unit 2819



7/13/04



Sheet 1 of 1

FORM PTO-1449	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTORNEY DOCKET NO. 1687.1001	APPLICATION NO. 10/183,590
LIST OF REFERENCES CITED BY APPLICANT (Use several sheets if necessary)		FIRST NAMED INVENTOR Toshinori SUEYOSHI, et al.	
		FILING DATE June 28, 2002	GROUP ART UNIT 2819

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NO.	DATE	NAME	CLASS	SUB- CLASS	FILING DATE
AT	AA	5,442,306	08/15/95	Woo			
	AB						
	AC						
	AD						
	AE						
	AF						

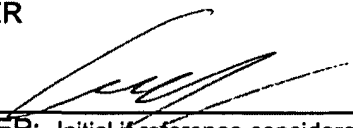
FOREIGN PATENT DOCUMENTS

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB- CLASS	TRANSLATION YES NO	
AT	AG	03-063846	03/19/91	Japan			abstract	
AT	AH	08-237109	09/13/96	Japan			abstract	
	AI							
	AJ							
	AK							
	AL							

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

TRANSLATION
YES NO

	AM			
--	----	--	--	--

EXAMINER 	DATE CONSIDERED 7/12/04
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	



Corres. and Mail
BOX AF

RESPONSE UNDER 37 CFR 1.116
EXPEDITED PROCEDURE
EXAMINING GROUP 2819
Docket No.: 1687.1001

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Toshinori SUEYOSHI, et al.

Serial No. 10/183,590

Group Art Unit: 2819

Confirmation No. 9469

Filed: June 28, 2002

Examiner: Anh Q. Tran

For: PROGRAMMABLE LOGIC CIRCUIT DEVICE HAVING LOOK UP TABLE ENABLING
TO REDUCE IMPLEMENTATION AREA

AMENDMENT AFTER FINAL REJECTION

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Attention: **BOX AF**

Sir:

This is in response to the Office Action mailed March 3, 2004, and having a period for response set to expire on June 3, 2004. A petition and fee for a one-month Extension of Time is enclosed, thereby extending the response period to July 3, 2004.

Reconsideration of the claims is respectfully requested. The following remarks are respectfully submitted.

07/02/2004 YPOLITE1 00000110 10183590

.01 FC:1251

110.00 OP

OK to Enter.

**ANH Q. TRAN
PRIMARY EXAMINER**

7/29/04

PATENT APPLICATION FEE DETERMINATION RECORD
Effective October 1, 2003

Application or Docket Number

10183590

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS		
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	minus 20=	*
INDEPENDENT CLAIMS	minus 3 =	*
MULTIPLE DEPENDENT CLAIM PRESENT ☐		

* If the difference in column 1 is less than zero, enter "0" in column 2

CLAIMS AS AMENDED - PART II

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	* 16	Minus ** 20	=
Independent	* 3	Minus *** 3	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐			

SMALL ENTITY TYPE ☐

OR OTHER THAN SMALL ENTITY

RATE	FEE		RATE	FEE
BASIC FEE	385.00	OR	BASIC FEE	770.00
X\$ 9=		OR	X\$18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL		OR	TOTAL	

SMALL ENTITY OR

OTHER THAN SMALL ENTITY

RATE	ADDI-TIONAL FEE		RATE	ADDI-TIONAL FEE
X\$ 9=		OR	X\$18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL		OR	TOTAL	
ADDIT. FEE		OR	ADDIT. FEE	

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus **	=
Independent	*	Minus ***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐			

RATE	ADDI-TIONAL FEE		RATE	ADDI-TIONAL FEE
X\$ 9=		OR	X\$18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL		OR	TOTAL	
ADDIT. FEE		OR	ADDIT. FEE	

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT C	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus **	=
Independent	*	Minus ***	=
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐			

RATE	ADDI-TIONAL FEE		RATE	ADDI-TIONAL FEE
X\$ 9=		OR	X\$18=	
X43=		OR	X86=	
+145=		OR	+290=	
TOTAL		OR	TOTAL	
ADDIT. FEE		OR	ADDIT. FEE	

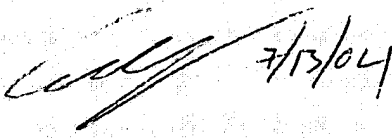
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Issue Classification 	Application No.	Applicant(s)	
	10/183,590	SUEYOSHI ET AL.	
	Examiner	Art Unit	
	Anh Q. Tran	2819	

ISSUE CLASSIFICATION									
ORIGINAL		CLASS	CROSS REFERENCE(S)						
CLASS	SUBCLASS		SUBCLASS (ONE SUBCLASS PER BLOCK)						
326	38	326	39	40					
INTERNATIONAL CLASSIFICATION									
A03K	19173								
	/								
	/								
	/								
	/								
(Assistant Examiner) (Date)		 (Primary Examiner) (Date)			Total Claims Allowed: 46				
 (Legal Instruments Examiner) (Date)					O.G. Print Claim(s)		O.G. Print Fig.		
					1		9		

☐ Claims renumbered in the same order as presented by applicant		☐ CPA		☐ T.D.		☐ R.1.47	
Final	Original	Final	Original	Final	Original	Final	Original
1	1		31		61		121
	2		32		62		122
	3		33		63		123
2	4		34		64		124
3	5		35		65		125
4	6		36		66		126
5	7		37		67		127
6	8		38		68		128
7	9		39		69		129
	10		40		70		130
	11		41		71		131
8	12		42		72		132
9	13		43		73		133
10	14		44		74		134
11	15		45		75		135
12	16		46		76		136
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Index of Claims



Application No.

10/183,590

Examiner

Anh Q. Tran

Applicant(s)

SUEYOSHI ET AL.

Art Unit

2819

✓	Rejected
=	Allowed

—	(Through numeral) Cancelled
+	Restricted

N	Non-Elected
I	Interference

A	Appeal
O	Objected

Claim		Date									
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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
 United States Patent and Trademark Office
 Address: COMMISSIONER FOR PATENTS
 P.O. Box 1450
 Alexandria, Virginia 22313-1450
 www.uspto.gov

BIBDATASHEET

CONFIRMATION NO. 9469

Bib Data Sheet

SERIAL NUMBER 10/183,590	FILING DATE 06/28/2002 RULE	CLASS 326	GROUP ART UNIT 2819	ATTORNEY DOCKET NO. 1687.1001
-----------------------------	---------------------------------------	--------------	------------------------	-------------------------------------

APPLICANTS

Toshinori Sueyoshi, Kumamoto-shi, JAPAN;
 Masahiro Iida, Fujisawa-shi, JAPAN;

** CONTINUING DATA *****

** FOREIGN APPLICATIONS *****
 JAPAN 2001-199644 06/29/2001 *AT*

IF REQUIRED, FOREIGN FILING LICENSE GRANTED
 ** 08/06/2002

Foreign Priority claimed 35 USC 119 (a-d) conditions met	☒ yes ☐ no ☒ yes ☐ no ☐ Met after Allowance	STATE OR COUNTRY JAPAN	SHEETS DRAWING 14	TOTAL CLAIMS 20	INDEPENDENT CLAIMS 3
---	---	------------------------------	-------------------------	-----------------------	----------------------------

Verified and Acknowledged
 Examiner's Signature *[Signature]* Initials *AT*

ADDRESS
 21171
 STAAS & HALSEY LLP
 SUITE 700
 1201 NEW YORK AVENUE, N.W.
 WASHINGTON, DC
 20005

TITLE
 Programmable logic circuit device having look up table enabling to reduce implementation area

FILING FEE	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time)
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Search Notes

Application No.

10/183,590

Examiner

Anh Q. Tran

Applicant(s)

SUEYOSHI ET AL.

Art Unit

2819

SEARCHED

Class	Subclass	Date	Examiner
326	37 1 47	7/12/04	AT

INTERFERENCE SEARCHED

Class	Subclass	Date	Examiner
as	above	7/12/04	AT

**SEARCH NOTES
(INCLUDING SEARCH STRATEGY)**

	DATE	EXMR

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail**

Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (703) 746-4000

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

21171 7590 08/02/2004

STAAS & HALSEY LLP
 SUITE 700
 1201 NEW YORK AVENUE, N.W.
 WASHINGTON, DC 20005



Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (703) 746-4000, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

09/27/2004 MBIZUNE2 00000194 10183590

01 FC:1501 1330.00 OP
 02 FC:1504 300.00 OP

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/183,590	06/28/2002	Toshinori Sueyoshi	1687.1001	9469

TITLE OF INVENTION: PROGRAMMABLE LOGIC CIRCUIT DEVICE HAVING LOOK UP TABLE ENABLING TO REDUCE IMPLEMENTATION AREA

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1330	\$300	\$1630	11/02/2004

EXAMINER	ART UNIT	CLASS-SUBCLASS
TRAN, ANH Q	2819	326-038000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address - PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
 (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 STAAS & HALSEY LLP

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Semiconductor Technology Academic
 Research Center

Kanagawa, Japan

Please check the appropriate assignee category or categories (will not be printed on the patent); ☐ individual ☒ corporation or other private group entity ☐ government

4a. The following fee(s) are enclosed:

- ☒ Issue Fee
☒ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s):

- ☒ A check in the amount of the fee(s) is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☒ The Director is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number 19-3935 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is not claiming SMALL ENTITY status. See, e.g., 37 CFR 1.27(g)(2).

The Director of the USPTO is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above.

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

(Authorized Signature)

(Date)

Alicia Chai, Reg #46,621

9/23/2004

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TRANSMIT THIS FORM WITH FEE(S)



Attorney Docket No. 1687.1001

Copy

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

Toshinori SUEYOSHI, et al.

Application No.: 10/183,590

ATTENTION

Confirmation No.: 9469

CERTIFICATE OF CORRECTION

Filed: June 28, 2002

BRANCH

U.S. Patent No.: 6,812,737

Issued: November 2, 2004

For: PROGRAMMABLE LOGIC CIRCUIT DEVICE HAVING LOOK UP TABLE ENABLING TO REDUCE IMPLEMENTATION AREA

REQUEST FOR CERTIFICATE OF CORRECTION

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Certificate
MAR 10 2005
of Correction

Sir:

Patentee(s) respectfully request(s) that a Certificate of Correction be issued in the subject patent, pursuant to 35 USC § 254 and 37 CFR § 1.322, to correct the error(s) shown on the attached Form PTO-1050. A check in the amount of \$100 to cover the cost of the Certificate is attached.

One or more of the errors shown on the attached Form PTO-1050 is or are within the responsibility of the undersigned; each thereof is of a clerical or typographical nature or of minor character and occurred in good faith, and the correction thereof is consistent with the prosecution record.

03/07/2005 AWONDAF2 00000068 6812737

01 FC:1811

100.00 0P

Respectfully submitted,

STAAS & HALSEY LLP

Date: Feb. 28, 2005

By: *H. J. Staas*
H. J. Staas
Registration No. 22,010

1201 New York Ave, N.W., Suite 700
Washington, D.C. 20005
Telephone: (202) 434-1500
Facsimile: (202) 434-1501

MAR 11 2005

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.
(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO : 6,812,737

DATED : November 2, 2004

INVENTOR(S) : Toshinori SUEYOSHI, et al.

Column 12, line 6, change "unit" to --units--

Column 12, line 11, change "unit" to --units--

MAILING ADDRESS OF SENDER:

STAAS & HALSEY LLP
1201 New York Ave., N.W.
Suite 700
Washington, DC 20005

PATENT NO. 6,812,737

No. of add'l copies
@ 50¢ per page

⇒

MAR 11 2005

MAR 11 2005

101 183,590

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,812,737 B2
DATED : November 2, 2004
INVENTOR(S) : Toshinori Sueyoshi et al.

Page 1 of 1

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 12,
Lines 6 and 11, change "unit" to -- units --

Signed and Sealed this

Twenty-sixth Day of April, 2005

A handwritten signature in black ink, appearing to read "Jon W. Dudas". The signature is stylized with a large, looped initial "J" and a cursive "Dudas".

JON W. DUDAS
Director of the United States Patent and Trademark Office

PETITION TO ACCEPT UNINTENTIONALLY DELAYED PAYMENT OF MAINTENANCE FEE IN AN EXPIRED PATENT (37 CFR 1.378(b))

Patent Number	Issue Date (YYYY-MM-DD)	Application Number	Filing Date (YYYY-MM-DD)	Docket Number (if applicable)
6,812,737	2004-11-02	10/183,590	2002-06-28	Y16YL039

CAUTION: Maintenance fee payment must correctly identify: (1) the patent number and (2) the application number of the actual U.S. application leading to issuance of that patent to ensure the fee(s) is/are associated with the correct patent. 37 CFR 1.366(c) and (d).

SMALL ENTITY

☐ Patentee claims, or has previously claimed, small entity status. See 37 CFR 1.27.

LOSS OF ENTITLEMENT TO SMALL ENTITY STATUS

☐ Patentee is no longer entitled to small entity status. See 37 CFR 1.27(g)

NOT Small Entity

	Fee	Code
☐	3 ½ year	(1551)
☐	7 ½ year	(1552)
☒	11 ½ year	(1553)

Small Entity

	Fee	Code
☐	3 ½ year	(2551)
☐	7 ½ year	(2552)
☐	11 ½ year	(2553)

PETITION FEE

The petition fee required by 37 CFR 1.17(m) (Fee Code 1558 /2558) must be paid as a condition of accepting unintentionally delayed payment of the maintenance fee.

MAINTENANCE FEE (37 CFR 1.20(e)-(g))

The appropriate maintenance fee must be submitted with this petition.

STATEMENT

THE UNDERSIGNED CERTIFIES THAT THE DELAY IN PAYMENT OF THE MAINTENANCE FEE TO THIS PATENT WAS UNINTENTIONAL

PETITIONER(S) REQUEST THAT THE DELAYED PAYMENT OF THE MAINTENANCE FEE BE ACCEPTED AND THE PATENT REINSTATED

THIS PORTION MUST BE COMPLETED BY THE SIGNATORY OR SIGNATORIES

37 CFR 1.378(c) states: "Any petition under this section must be signed in compliance with 37 CFR 1.33(b)."

I certify, in accordance with 37 CFR 1.4(d)(4) that I am

- ☒ An attorney or agent registered to practice before the Patent and Trademark Office
- ☐ A sole patentee
- ☐ A joint patentee; I certify that I am authorized to sign this submission on behalf of all the other patentees as evidenced by the power of attorney in the application
- ☐ A joint patentee; all of whom are signing this e-petition
- ☐ The assignee of record of the entire interest that qualifies as an authorized party under 37 CFR 1.33(b)

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays valid OMB control number.

Patent Practitioner			
A signature of the applicant or representative is required in accordance with 37 CFR 1.33 and 10.18. Please see 37 CFR 1.4(d) for the form of the signature			
Signature	/Konomi Takeshita/	Date (YYYY-MM-DD)	2016-12-07
Name	Konomi Takeshita	Registration Number	38333
This collection of information is required by 37 CFR 1.378(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. This form can only be used when in conjunction with EFS-Web. If this form is mailed to the USPTO, it may cause delays in reinstating the patent.			

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner: Masahiro IIDA

Application No./Patent No.: 10/183,590 / 6,812,737 Filed/Issue Date: 2002-06/28 / 2004-11-02

Titled: **PROGRAMMABLE LOGIC CIRCUIT DEVICE HAVING LOOK UP TABLE ENABLING TO REDUCE IMPLEMENTATION AREA**

Masahiro IIDA, a Individual
(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that it is:

1. ☒ the assignee of the entire right, title, and interest in;
2. ☐ an assignee of less than the entire right, title, and interest in
(The extent (by percentage) of its ownership interest is _____ %); or
3. ☐ the assignee of an undivided interest in the entirety of (a complete assignment from one of the joint inventors was made)

the patent application/patent identified above, by virtue of either:

A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy therefore is attached.

OR

B. ☒ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: Toshinori SUEYOSHI and Masahiro IIDA To: Semiconductor Tech. Academic Research Ctr.

The document was recorded in the United States Patent and Trademark Office at
Reel 013050, Frame 0486, or for which a copy thereof is attached.

2. From: Semiconductor Tech. Academic Research Ctr. To: Masahiro IIDA

The document was recorded in the United States Patent and Trademark Office at
Reel 033904, Frame 0739, or for which a copy thereof is attached.

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☒ As required by 37 CFR 3.73(b)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Konomi Takeshita/
Signature

December 7, 2016
Date

Konomi Takeshita
Printed or Typed Name

38333
Title

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	10183590			
Filing Date:	28-Jun-2002			
Title of Invention:	PROGRAMMABLE LOGIC CIRCUIT DEVICE HAVING LOOK UP TABLE ENABLING TO REDUCE IMPLEMENTATION AREA			
First Named Inventor/Applicant Name:	Toshinori Sueyoshi			
Filer:	Konomi Takeshita			
Attorney Docket Number:	1687.1001			
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
PET. REVIVE ABANDON APP, DELAY PYMT-RESP	1453	1	1700	1700
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1700

Electronic Acknowledgement Receipt

EFS ID:	27719189
Application Number:	10183590
International Application Number:	
Confirmation Number:	9469
Title of Invention:	PROGRAMMABLE LOGIC CIRCUIT DEVICE HAVING LOOK UP TABLE ENABLING TO REDUCE IMPLEMENTATION AREA
First Named Inventor/Applicant Name:	Toshinori Sueyoshi
Customer Number:	21171
Filer:	Konomi Takeshita
Filer Authorized By:	
Attorney Docket Number:	1687.1001
Receipt Date:	07-DEC-2016
Filing Date:	28-JUN-2002
Time Stamp:	17:50:25
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	\$ 1700
RAM confirmation Number	120816INTEFSW00006414502270
Deposit Account	502270
Authorized User	Konomi Takeshita

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

37 CFR 1.16 (National application filing, search, and examination fees)

37 CFR 1.17 (Patent application and reexamination processing fees)

37 CFR 1.19 (Document supply fees)
37 CFR 1.20 (Post Issuance fees)
37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	ExecutedPOAsb81aY16YL039.pdf	253253	no	1
			366f788598ee1443e23be341ecc873b0f39a0097		
Warnings:					
Information:					
2	Change of Address	FeeAddressIndicationFormSB47Y16YL039.pdf	204024	no	2
			53e8cc94b60f72e62b508fd8f74dedae0881e111		
Warnings:					
Information:					
3	Petition for review by the Office of Petitions	PetitionToMaintenanceFeeExpi redsb66Y16YL039.pdf	1999004	no	3
			0ae84c39b82c8812985cfc1b16209bdc681d41f4		
Warnings:					
Information:					
4	Assignee showing of ownership per 37 CFR 3.73	StatementUnder37CFRsb96Y16YL039.pdf	436721	no	2
			819be48eaf9b78ae78ca83e2e1c586ad1002b535		
Warnings:					
Information:					
5	Fee Worksheet (SB06)	fee-info.pdf	30621	no	2
			64e2611985467e1e4b9b598390df08e6faa5d1e0		
Warnings:					
Information:					
Total Files Size (in bytes):			2923623		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT - POWER OF ATTORNEY OR REVOCATION OF POWER OF ATTORNEY WITH A NEW POWER OF ATTORNEY AND CHANGE OF CORRESPONDENCE ADDRESS	Patent Number	6,812,737
	Issue Date	2004-11-02
	First Named Inventor	Toshinori SUEYOSHI
	Title	PROGRAMMABLE LOGIC CIRCUIT DEVICE HAVING LOOK UP TABLE ENABLING TO SERVICE
	Attorney Docket Number	Y16YL039

I hereby revoke all previous powers of attorney given in the above-identified patent.

☐ A Power of Attorney is submitted herewith.

OR

☒ I hereby appoint Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s) with respect to the patent identified above, and to transact all business in the United States Patent and Trademark Office connected therewith: 87046

OR

☐ I hereby appoint Practitioner(s) named below as my/our attorney(s) or agent(s) with respect to the patent identified above, and to transact all business in the United States Patent and Trademark Office connected therewith:

Practitioner(s) Name	Registration Number

Please recognize or change the correspondence address for the above-identified patent to:

☒ The address associated with the above-mentioned Customer Number.

OR

☐ The address associated with Customer Number:

OR

☐ Firm or Individual Name			
Address			
City	State	Zip	
Country			
Telephone	Email		

I am the:

☐ Inventor, having ownership of the patent.

OR

☒ Patent owner.
Statement under 37 CFR 3.73(b) (Form PTO/SB/96) submitted herewith or filed on _____

SIGNATURE of Inventor or Patent Owner

Signature	<i>Masahiro Iida</i>	Date	December 6, 2016
Name	Masahiro IIDA	Telephone	
Title and Company	Professor, Kumamoto University		

NOTE: Signatures of all the inventors or patent owners of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☒ *Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

"FEE ADDRESS" INDICATION FORM

Address to:
Mail Stop M Correspondence
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Fax to:
571-273-6500

- OR -

INSTRUCTIONS: The issue fee must have been paid for application(s) listed on this form. In addition, only an address represented by a Customer Number can be established as the fee address for maintenance fee purposes (hereafter, fee address). A fee address should be established when correspondence related to maintenance fees should be mailed to a different address than the correspondence address for the application. **When to check the first box below:** If you have a Customer Number to represent the fee address. **When to check the second box below:** If you have no Customer Number representing the desired fee address, in which case a completed Request for Customer Number (PTO/SB/125) must be attached to this form. For more information on Customer Numbers, see the Manual of Patent Examining Procedure (MPEP) § 403.

For the following listed application(s), please recognize as the "Fee Address" under the provisions of 37 CFR 1.363 the address associated with:



Customer Number:

87046**OR**

The attached Request for Customer Number (PTO/SB/125) form.

PATENT NUMBER (if known)	APPLICATION NUMBER
6,812,737	10/183,590

Completed by (check one):



Applicant/Inventor

/Konomi Takeshita/

Signature



Attorney or Agent of record 38333
 (Reg. No.)

Konomi Takeshita

Typed or printed name



Assignee of record of the entire interest. See 37 CFR 3.71.
 Statement under 37 CFR 3.73(b) is enclosed.
 (Form PTO/SB/96)

215-701-6349

Requester's telephone number



Assignee recorded at Reel _____ Frame _____

December 7, 2016

Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

* Total of 2 forms are submitted.

This collection of information is required by 37 CFR 1.363. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 5 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. **DO NOT SEND COMPLETE D FORMS TO THIS ADDRESS.**
SEND TO: Mail Stop M Correspondence, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
10/183,590	06/28/2002	Toshinori Sueyoshi	1687.1001

21171
STAAS & HALSEY LLP
SUITE 700
1201 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

CONFIRMATION NO. 9469
POWER OF ATTORNEY NOTICE



OC000000087937731

Date Mailed: 12/15/2016

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 12/07/2016.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/dtvernon/



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
10/183,590	06/28/2002	Toshinori Sueyoshi	Y16YL039

CONFIRMATION NO. 9469

POA ACCEPTANCE LETTER

87046
Konomi Takeshita
Eight Penn Center, Suite 1300,
1628 John F. Kennedy Blvd.
Philadelphia, PA 19103



Date Mailed: 12/15/2016

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 12/07/2016.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/dtvernon/

JAN/05/2017/THU 07:30 AM

FAX No.

P. 001

JAPAN AND INTERNATIONAL
PATENT, TRADEMARK AND
COPYRIGHT MATTERS

Omori & Yaguchi

EIGHT PENN CENTER, SUITE 1300
1628 JOHN F. KENNEDY BLVD
PHILADELPHIA, PA 19103

TOKYO
PHILADELPHIA

TEL: (215)701-6349
FAX: (215)751-0192

FACSIMILE TRANSMISSION

TO: USPTO / Facsimile Transmitted to
Maintenance Fee

FAX No.: 571-273-6500

FROM: Konomi Takeshita

DATE: January 5, 2017

Patent No.: 6,812,737

Application No. 10/183,590

Our Ref.: Y16YL039

MESSAGE:

Attached please find a signed **Maintenance Fee Transmittal Form (PTO/SB/45)** to pay the 11.5 year Maintenance Fee plus a Surcharge. Those Fees are to accompany the **Petition to Accept Unintentionally Delayed Payment of Maintenance Fee In an Expired Patent (PTO/SB/66)** previously submitted via **EFS-Web on December 7, 2016**. The required Petition Fee (\$1700) was already paid via EFS-Web on December 7, 2016.

Please process the attached Maintenance Fee Payment, to permit granting of the Petition (PTO/SB/66) and reinstatement of this patent.

If you have any questions or need further information in this matter, please give me a call at (215) 701-6349 (office). Thank you.

Best regards,



Konomi Takeshita - Reg. No. 38,333

*** The information contained in this facsimile message is privileged and confidential information intended only for the use of the recipient named above. If the reader of this message is not the intended recipient, or the employee or agent responsible to deliver it to the intended recipient, any distribution or copying of this immediately by telephone and return the original message to us at the above address by mail. ***

We have 2 pages to send, including this sheet. If any pages need to be retransmitted, please call **215-701-6349**

PTO/SB/45 (03-13)

Approved for use through 05/31/2015. OMB 0651-0016

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

MAINTENANCE FEE TRANSMITTAL FORM

(Do not submit this form electronically via EFS-Web)

Address to:
Director of the United States
Patent and Trademark Office
Attn: Maintenance Fee
2051 Jamieson Avenue, Suite 300
Alexandria, VA 22314

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Director of the United States Patent and Trademark Office, Attn: Maintenance Fee, 2051 Jamieson Avenue, Suite 300, Alexandria, VA 22314"

Signature 01/06/2017 DALLIN 00000001 502270

- OR -

Typed or printed name 01 FC:1599 7400.00 DA

Fax to: 571-273-6500

Enclosed herewith is the payment of the maintenance fee(s) for the listed patent(s).

1. ☐ A check for the amount of \$ _____ for the full payment of the maintenance fee(s) and any necessary surcharge is enclosed.
2. ☐ Payment by credit card. Form PTO-2038 is enclosed.
3. ☒ The Director is hereby authorized to charge \$ 7,560.00 to cover the payment of the fee(s) indicated below to
 Deposit Account No. 502270
4. ☒ The Director is hereby authorized to charge any deficiency in the payment of the required fee(s) or credit any overpayment to
 Deposit Account No. 502270

Item	Patent Number*	U.S. Application Number* (e.g., 08/555,555)	Maintenance Fee Amount (37 CFR 1.20(e)-(g))	Surcharge Amount (37 CFR 1.20(h))	Payment Year (select one below) Column 5		
					3.5 yrs	7.5 yrs	11.5 yrs
1	6,812,737	10/183,590	\$7,400.00	\$160.00			X
2							
3							
4							
5							

Subtotals: Columns 3 & 4

\$7,400.00

\$160.00

Total Payment

\$7,560.00

☐ additional sheets attached for listing additional patents.

* Information required by 37 CFR 1.366(c) (columns 1 & 2). Information requested under 37 CFR 1.366(d) (columns 3, 4, & 5).

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on Form PTO-2038.

Respectfully submitted,**

Customer's Signature Konori Takeshita

Customer's Name Konori Takeshita

Registration Number, if applicable: 38333

Telephone: 201-701-6349

Fax: 201-751-0192

Note: All correspondence will be forwarded to the "Fee Address" or to the "Correspondence Address" if no "Fee Address" has been provided. See 37 CFR 1.363.

Payment of small entity fee is appropriate if small entity status still exists, see 37 CFR 1.27(g). To establish small entity status or to notify of a loss of entitlement to small entity status, a written assertion is required. See 37 CFR 1.27 and 1.33(b). Payment of micro entity fee is appropriate if patent owner certifies micro entity status. Form PTO/SB/15A or B or equivalent must either be enclosed or have been submitted previously. To notify of a loss of entitlement to micro entity status, a written assertion is required. See 37 CFR 1.29 and 1.33(b).

**** WHERE MAINTENANCE FEE PAYMENTS ARE TO BE MADE BY AUTHORIZATION TO CHARGE A DEPOSIT ACCOUNT, BOTH THE NAME AND SIGNATURE OF AN AUTHORIZED USER ARE REQUIRED.**

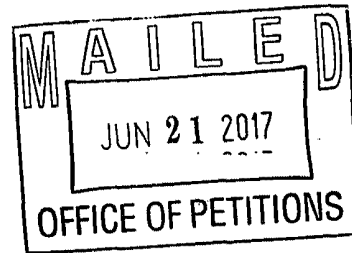
This collection of information is required by 37 CFR 1.366. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 5 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Director of the United States Patent and Trademark Office, Attn: Maintenance Fee, 2051 Jamieson Avenue, Suite 300, Alexandria, VA 22314.

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P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov



KONOMI TAKESHITA
EIGHT PENN CENTER, SUITE 1300,
1628 JOHN F. KENNEDY BLVD.
PHILADELPHIA PA 19103

In re Patent No. 6,812,737	:	
Issue Date: November 02, 2004	:	
Application No. 10/183,590	:	DECISION ON PETITION
Filed: June 28, 2002	:	
Attorney Docket No. Y16YL039	:	

This is a decision on the petition under 37 CFR 1.378(b), filed December 07, 2016, to accept the unintentionally delayed payment of a maintenance fee for the above-identified patent.

The petition is **GRANTED**.

This patent expired on November 02, 2016 for failure to pay the eleven and one-half year maintenance fee.

The maintenance fee is hereby accepted and the above-identified patent is reinstated as of the mail date of this decision.

Telephone inquiries concerning this decision should be directed to the undersigned at (571) 272-4231.

/Michelle R. Eason/
Michelle R. Eason
Paralegal Specialist
Office of Petitions



ELECTRONIC PAYMENT RECEIPT

APPLICATION #
10/183,590

RECEIPT DATE / TIME
04/22/2021 03:15:26 PM ET

ATTORNEY DOCKET #
Y16YL039

Title of Invention

PROGRAMMABLE LOGIC CIRCUIT DEVICE HAVING LOOK UP TABLE ENABLING TO REDUCE IMPLEMENTATION AREA

Application Information

APPLICATION TYPE Utility - Nonprovisional Application
under 35 USC 111(a)

PATENT # 6812737

CONFIRMATION # 9469

FILED BY Joshua Slavitt

PATENT CENTER # 60181328

AUTHORIZED BY -

CUSTOMER # 87046

FILING DATE 06/28/2002

CORRESPONDENCE ADDRESS -

FIRST NAMED INVENTOR Toshinori Sueyoshi

Payment Information

PAYMENT METHOD
CARD / 1007

PAYMENT TRANSACTION ID
E20214LF15560409

PAYMENT AUTHORIZED BY
Joshua Slavitt

FEE CODE	DESCRIPTION	ITEM PRICE(\$)	QUANTITY	ITEM TOTAL(\$)
1811	CERTIFICATE OF CORRECTION	160.00	1	160.00
TOTAL AMOUNT:				\$160.00

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

**UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION**Page 1 of 1

PATENT NO. : 6,812,737

APPLICATION NO.: 10/183,590

ISSUE DATE : November 2, 2004

INVENTOR(S) : Toshinori Sueyoshi and Masahiro Iida

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the title page, item (75) Inventors: "Toshinori Sueyoshi, Kumamoto (JP); Masahiro Iida, Fujisawa (JP)" should be deleted and replaced with --Masahiro Iida, Fujisawa (JP)--.

MAILING ADDRESS OF SENDER (Please do not use Customer Number below):

Joshua R. Slavitt (Reg. No. 40,816)
535 Hamilton Road
Merion Station, PA 19066

This collection of information is required by 37 CFR 1.322, 1.323, and 1.324. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Attention Certificate of Corrections Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

UNITED STATES PATENT AND TRADEMARK OFFICE

U.S. Patent No.: 6,812,737
Application No.: 10/183,590
Issue Date: November 4, 2004
Inventors: Toshinori Sueyoshi and Masahiro Iida

STATEMENT SUBMITTED WITH CERTIFICATE OF CORRECTION

I, Masahiro Iida, hereby state as follows:

1. Toshinori Sueyoshi was erroneously listed as a co-inventor for the above-referenced patent.
2. I agree that inventorship should be changed to delete Toshinori Sueyoshi as a co-inventor so that I am listed as the sole inventor.
3. As the sole assignee of the above-referenced patent, as evidenced by the assignments recorded with the U.S. Patent and Trademark Office at Reel 13050, Frames 486-487, and at Reel 33904, Frames 739-740, I agree to the foregoing change of inventorship in the above-referenced patent.

Masahiro Iida
Masahiro Iida

Dated: Apr. 20 / 2021

UNITED STATES PATENT AND TRADEMARK OFFICE

U.S. Patent No.: 6,812,737
Application No.: 10/183,590
Issue Date: November 4, 2004
Inventors: Toshinori Sueyoshi and Masahiro Iida

STATEMENT SUBMITTED WITH CERTIFICATE OF CORRECTION

I, Toshinori Sueyoshi, hereby state as follows:

1. I was erroneously listed as a co-inventor for the above-referenced patent.
2. I agree that inventorship should be changed to delete my name as a co-inventor so

that Masahiro Iida is listed as the sole inventor.

Toshinori Sueyoshi
Toshinori Sueyoshi

Dated: Apr 14, 2021



ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #
10/183,590

RECEIPT DATE / TIME
04/22/2021 03:15:26 PM ET

ATTORNEY DOCKET #
Y16YL039

Title of Invention

PROGRAMMABLE LOGIC CIRCUIT DEVICE HAVING LOOK UP TABLE ENABLING TO REDUCE IMPLEMENTATION AREA

Application Information

APPLICATION TYPE Utility - Nonprovisional Application
under 35 USC 111(a)

PATENT # 6812737

CONFIRMATION # 9469

FILED BY Joshua Slavitt

PATENT CENTER # 60181328

FILING DATE 06/28/2002

CUSTOMER # 87046

FIRST NAMED INVENTOR Toshinori Sueyoshi

CORRESPONDENCE ADDRESS -

AUTHORIZED BY -

Documents

TOTAL DOCUMENTS: 4

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
InventorCorrectionPetition.pdf	2	Request for Certificate of Correction	99 KB
sb44.pdf	1	Request for Certificate of Correction	120 KB
StatementsforCorrectionofInventorship.pdf	2	Oath or Declaration filed	1363 KB
TransmittalLetter.pdf	2	Miscellaneous Incoming Letter	105 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
InventorCorrectionPetition.pdf	08D1315AED2E81AE0B77D9950A7B24678BFAC157D8F646D52 7574DDA7872528DE5ED3BC018976C8BB534B2A28ADBA5FB9 920559A9DE2D8CD8F0739E72E479AEF
sb44.pdf	B7F45CF754DAF129837EA39ED960DCA4AA784F320343BA8F5 4DB698A4E038E7C39A72CFD6BB3EEBEBF0A8804AEBCA47C A7244C3BD79B031B10A131C207E2E41C
StatementsforCorrectionofInven torship.pdf	49CC254CCADB2010E1FB7E884395400EB7F4316202AD9018D 0FD7B01F3D5542E7C3C06A5A5B64319C3BEE3C752D50002DF 20E8927911FC93BDC08A0A5DCECEDF
TransmittalLetter.pdf	391EAC289191594237EB7F3CB12152121995B36D49D40F2364 5E481145E7EFB12DF8BD5C632EB028AD0D6C1EA4771CB5DF 18FB1DDBEBAF645D8195D4CDE91986

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of: Sueyoshi, et al.	§
	§
Patent No.: 6,812,737	§
	§
Application No.: 10/183,590	§
	§
Issued: November 2, 2004	§
	§
For: PROGRAMMABLE LOGIC CIRCUIT	§
DEVICE HAVING LOOK UP TABLE	§
ENABLING TO REDUCE	§
IMPLEMENTATION AREA	§

PETITION TO CORRECT INVENTORSHIP (37 C.F.R. §1.324(a))

Commissioner for Patents
Office of Data Management Attention: Certificates of Correction Branch
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Pursuant to 37 C.F.R. §1.324(a), the named co-inventors and the current assignee respectfully request that U.S. Patent No. 6,812,737 be corrected as follows:

On the title page, item (75) Inventors: “Toshinori Sueyoshi, Kumamoto (JP); Masahiro Iida, Fujisawa (JP)” should be deleted and replaced with --Masahiro Iida, Kumamoto (JP)--.

REMARKS

This Request to Correct Inventorship is filed in order to correct the inventorship of the U.S. Patent No. 6,812,737 pursuant to the provisions of 37 C.F.R. § 1.324(a) and MPEP § 1481.02.

U.S. Patent No. 6,812,737 erroneously sets forth inventorship. The correct inventorship of this patent should be Masahiro Iida as the sole inventor. Accordingly, Toshinori Sueyoshi should be deleted as an inventor.

As indicated in the accompanying statements, both listed co-inventors agree to the foregoing change.

Further, Masahiro Iida is presently the sole assignee of the patent, as evidenced by the assignments recorded with the U.S. Patent and Trademark Office at Reel 13050, Frames 486-487, and at Reel 33904, Frames 739-740, and his statement constitutes consent of the assignee to the change in inventorship.

The processing fee set forth in 37 C.F.R. § 1.20(b) is submitted herewith.

Accordingly, issuance of a Certificate of Correction in U.S. Letters Patent No. 6,812,737 to reflect the correct inventorship is respectfully requested.

Respectfully submitted,

Slavitt IP Law, LLC

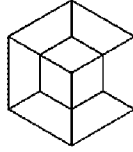
Date: April 22, 2021

/Joshua R. Slavitt/

Joshua R. Slavitt

Reg. No. 40816

Slavitt IP Law, LLC
535 Hamilton Road
Merion Station, PA 19066
Telephone: (215) 880-2569



Joshua R. Slavitt
josh@slavittiplaw.com

SLAVITT IP LAW

INTELLECTUAL PROPERTY LAW

**535 HAMILTON ROAD
MERION STATION, PA 19066
(215) 880-2569
WWW.SLAVITTIPLAW.COM**

April 22, 2021

Commissioner for Patents
Office of Data Management Attention: Certificates of Correction Branch
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Pursuant to 37 C.F.R. §1.324(a), the named co-inventors and the current assignee respectfully request that U.S. Patent No. 6,812,737 be corrected as follows:

On the title page, item (75) Inventors: “Toshinori Sueyoshi, Kumamoto (JP); Masahiro Iida, Fujisawa (JP)” should be deleted and replaced with --Masahiro Iida, Kumamoto (JP)--.

U.S. Patent No. 6,812,737 erroneously sets forth inventorship. The correct inventorship of this patent should be Masahiro Iida as the sole inventor. Accordingly, Toshinori Sueyoshi should be deleted as an inventor. As indicated in the accompanying statements, both listed co-inventors agree to the foregoing change. Further, Masahiro Iida is presently the sole assignee of the patent, as evidenced by the assignments recorded with the U.S. Patent and Trademark Office

at Reel 13050, Frames 486-487, and at Reel 33904, Frames 739-740, and his statement constitutes consent of the assignee to the change in inventorship.

The processing fee set forth in 37 C.F.R. § 1.20(b) is submitted herewith.

Accordingly, issuance of a Certificate of Correction in U.S. Letters Patent No. 6,812,737 to reflect the correct inventorship is respectfully requested.

Respectfully submitted,

Slavitt IP Law, LLC

Date: April 22, 2021

/Joshua R. Slavitt/

Joshua R. Slavitt

Reg. No. 40816



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/183,590	06/28/2002	Toshinori Sueyoshi	Y16YL039	9469

87046 7590 05/19/2022
Keisen Associates
Eight Penn Center, Suite 1100
1628 John F. Kennedy Blvd.
Philadelphia, PA 19103

EXAMINER

TRAN, ANH Q

ART UNIT	PAPER NUMBER
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2819

MAIL DATE	DELIVERY MODE
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05/19/2022

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.



UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

Patent No.: 6812737
Issue Date: 11/02/2004
Appl. No.: 10/183,590
Filed: 06/28/2002

PART (A) RESPONSE FOR CERTIFICATES OF CORRECTION

This is a decision on the Certificate of Correction request filed 22 April 2022.

The request for issuance of Certificate of Correction for the above-identified correction(s) under the provisions of 37 CFR 1.322 and/or 1.323 is hereby:

(Check one)

☒ Approved ☐ Approved in Part ☐ Denied

Comments: _____

PART (B) PETITION UNDER 37 CFR 1.324 OR 37 CFR 1.48

☐ This is a decision on the petition filed _____ to correct inventorship under 37 CFR 1.324.

☐ This is a decision on the request under 37 CFR 1.48, petition filed _____. In view of the fact that the patent has already issued, the request under 37 CFR 1.48 has been treated as a petition to correct inventorship under 37 CFR 1.324.

The petition is hereby: ☐ Granted ☐ Dismissed

Comment: _____

The patented filed is being forwarded to Certificate of Corrections Branch for issuance of a certificate naming only the actual inventor or inventors.

/ALEXANDER H TANINGCO/
Supervisory Patent Examiner, Art Unit 2844
Technology Center 2800
Phone: (571)272-8048

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,812,737 B2
APPLICATION NO. : 10/183590
DATED : November 2, 2004
INVENTOR(S) : Masahiro Iida

Page 1 of 1

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the Title Page

Item (12) delete "Sueyoshi, et al." and insert --Masahiro Iida--.

Item (75) Inventors: "Toshinori Sueyoshi, Kumamoto (JP); Masahiro Iida, Fujisawa (JP)"
should be deleted and replaced with --Masahiro Iida, Fujisawa (JP)--.

Signed and Sealed this
Fourteenth Day of June, 2022

Katherine Kelly Vidal
Director of the United States Patent and Trademark Office