

**IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION**

PROFESSOR MASAHIRO IIDA,

Plaintiff,

V.

INTEL CORPORATION,

Defendant.

Case No. 6:22-cv-00662-ADA

JURY TRIAL DEMANDED

PROFESSOR MASAHIRO IIDA'S RESPONSIVE CLAIM CONSTRUCTION BRIEF

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I. INTRODUCTION

Intel has identified two terms used in the claims of U.S. Patent No. 6,812,737 (the '737 patent) as requiring construction. Each of those terms can be construed according to their plain and ordinary meanings by one of ordinary skill in the art when those terms are read in view of the specification. Therefore, no construction of either term is necessary.

First, the parties dispute whether the phrase “look up table of M inputs and N outputs” requires construction. Intel asserts that Professor Iida defined this term in the '737 patent, and that his supposed definition displaces its otherwise plain and ordinary meaning. Contrary to Intel's contention, however, Professor Iida did *not* act as his own lexicographer, and where a patentee does not unequivocally impart his own *novel* meaning to claim terms, the plain and ordinary meaning should prevail. *See, e.g., Uniloc Luxembourg S.A. v. Corel Inc.*, 2014 U.S. Dist. LEXIS 172979, at *29 (E.D. Tex. December 15, 2014). The language of the '737 patent comes nowhere close to meeting the exacting standard for lexicography—clearly setting forth a definition of the disputed claim term and clearly expressing an intent to define that term. *See GE Lighting Solutions, LLC v. AgiLight, Inc.*, 750 F.3d 1304, 1309 (Fed. Cir. 2014). Moreover, even if the cited passages of the '737 patent describing—not defining—a look up table of M inputs and N outputs constitute lexicography, Intel itself readily concedes that such language is “consistent with the plain and ordinary meaning of that phrase.” Dkt. No. 51 at 12. Applying the plain and ordinary meaning would neither ignore any asserted lexicography nor would it invite juror confusion as to the scope of the claims.

Second, the parties dispute whether the phrase “LUT units” renders the asserted claims indefinite or requires construction. According to Intel, the claimed “LUT units” are “smaller look up tables (i.e., LUTs) that, when taken together, comprise the larger ‘look up table of M inputs

and N outputs.’” Dkt. 51 at 1. Yet Intel’s description fails to capture the essence of our common, everyday understanding of what it means to be a “unit”—a basic, unitary, individual element. Just as two adjacent apartment units are not considered to be a single “unit,” particular rooms within a single apartment unit are also not regarded as separate “units.” The same is true for look up tables.

Intel obfuscates the plain and ordinary meaning of “unit” by engaging in arbitrary box drawing on a simplified block diagram of a look up table. Whether a given look up table of M inputs and N outputs comprises a plurality of LUT units is not a matter of how a simplified block diagram *may be viewed*, but rather how the look up table itself is actually *implemented*. One of ordinary skill in the art well understands what a LUT unit is according to its plain and ordinary meaning, particularly upon reading the written description of the ’737 patent and reviewing its figures. In this case, as Intel’s Adaptive Logic Modules are designed and implemented using a plurality of LUT units, infringement as to these claim elements is evident. As a result, the term “LUT unit” is neither indefinite nor does it require construction.

II. THE RELEVANT TECHNOLOGY

A. Field Programmable Gate Arrays

Field Programmable Gate Arrays (FPGAs) are programmable logic devices that typically comprise three major components: a grid of programmable logic elements, input/output (I/O) elements, and interconnect elements. *See* Declaration of Dr. Marwan Hassoun (“Hassoun Decl.”) at ¶ 18. The programmable logic elements (also called logic blocks) are capable of expressing Boolean (logic) functions, the programmable I/O elements provide an external interface, and the routing elements (e.g., wires) connect the different parts. *Id.*

When considering logic block architecture, there are several trade-offs between area efficiency and delay. *Id.* at ¶ 19. The area efficiency indicates how efficiently logic blocks are used when a circuit is implemented on an FPGA. *Id.* The area efficiency is higher when logic blocks are used with a low number of unused (i.e. wasted) elements (i.e. functionality). *Id.*

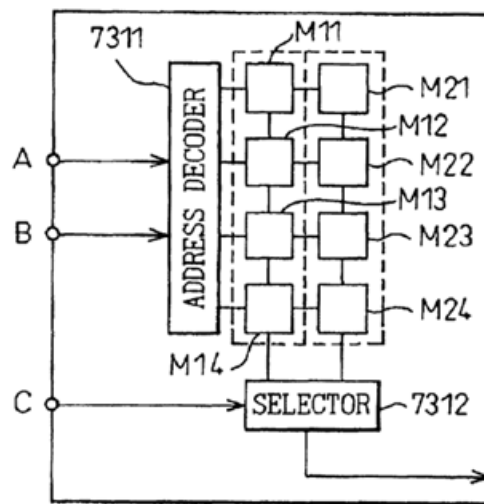
Regarding area efficiency, there are the following trade-offs in logic blocks:

- As functions per logic block increase, the total number of logic blocks required to implement the desired circuit *decreases*.
- On the other hand, since the area of the logic block itself and the number of inputs and outputs increase, the overall area per logic block *increases*.

Id. at ¶ 20.

B. Look Up Tables

Programmable logic blocks used in FPGAs implement logic functions using look up tables, which are often referred to by the acronym “LUT.” *Id.* at ¶ 21. A look up table is a “digital memory” that can implement a logic function by storing the values for that function’s truth table in its memory cells. *Id.* As noted by Intel, one example of a look up table is depicted as a block diagram in Fig. 7 of the ’737 patent:



Id. at ¶ 22. As shown in this figure, the memory comprises a four-by-two array of eight bits (M11–M14 and M21–M24) and a selector (7312) that selects between the two columns of memory cells that are collectively addressed using three binary values (A, B, and C)—which are the inputs. *Id.*

The number of LUT inputs is one of the most important factors when determining the structure and number of logic blocks. *Id.* at ¶ 23. As the number of inputs of the LUT increases, the total number of logic blocks required to implement a given logic function decreases. On the other hand, because a LUT having k inputs requires 2^k memory bits, the overall area of each logic block increases. *Id.* Furthermore, as the number of input/output pins of the logic block increases, the area of the routing part also increases. *Id.* As a result, the overall area per logic block increases as well. *Id.* Since the area of an FPGA is a function of the total number of logic blocks $\times$ the area per logic block, there is clearly an area trade-off. *Id.*

Another consideration is processing speed. *Id.* at ¶ 24. Generally, a larger input LUT results in a reduction in the number of circuit components (commonly known as logic stages) the signals have to traverse (commonly known as logic depth) in order to produce the desired output (i.e. implement the logic function). *Id.* On the other hand, other parameters being equal, to implement the same function using a smaller input LUT would require more logic stages and thus a larger logic depth resulting in slower operating speed (more delay). *Id.*

To summarize, if the number of inputs of a LUT is large, the number of logic stages to implement a large function is reduced, generally resulting in higher operational speed. *Id.* at ¶ 25. However, when implementing a smaller logic function that, for example, does not utilize all of the LUT inputs, the area efficiency is reduced due to unused circuitry within the logic block. *Id.* On the other hand, if the number of inputs of the LUT is small, the number of logic stages to

implement the same function increases and the operational speed is degraded; but, area efficiency is improved. *Id.* In this fashion, the input size of the LUT is closely related to the area efficiency and delay of the FPGA. *Id.*

Many of the leading researchers in the field of programmable computing—Professor Jonathan Rose, his colleagues at the University of Toronto, as well as other individuals in Toronto and San Jose working for Altera Corporation (Intel’s predecessor infringer)—spent the 1990s and several of the first years of the 21st century grappling with how to optimize the foregoing tradeoffs. *See, e.g.*, Dkt. Nos. 51-5 and 51-13. These efforts were mostly focused on determining the optimal input size for the LUTs used in logic blocks. *See id.*

III. THE ’737 PATENT

On June 29, 2001, Professor Iida (then, a doctoral candidate) filed a patent application directed to a revolutionary breakthrough in FPGA chip architecture. At that time, the leading researchers in the field were still focused on optimizing LUT size for area efficiency and delay. Importantly, their focus was predicated on the long-held assumption that LUT size—i.e., the number of inputs for a given look up table—was *fixed*. In rejecting that conventional assumption, Professor Iida invented an FPGA architecture that allowed a large look up table, such as a 6-LUT, to be configured in such a manner that, in one configuration, it operates as a single, 6-input look up table and, in a variety of other configurations, it operates as two or more smaller look up tables of varying size. *See, e.g.*, ’737 patent at Figs. 3A-3F, 6, and 9 attached as Exhibit A. This invention was a literal breakthrough insofar as it broke through the entire optimization problem with which many others in the field, including those at Altera, had been endeavoring for years to solve—without success. With Professor Iida’s novel architecture, one no longer needed to be

concerned with the “optimal LUT size” when look up tables could now be configured, at will, to *vary in size*.

The revolutionary nature of Professor Iida’s invention was further confirmed when, on February 10, 2003, about nineteen months *after* Professor Iida’s filing date, Altera filed its own patent application on the very same invention—what it termed Adaptive Logic Modules (ALMs)—and, in 2004, when Altera introduced the Stratix II line of FPGA chips trumpeting to the world a 15% performance increase with 12% area decrease realized specifically by the use of ALMs.

IV. LEGAL STANDARDS

The construction of terms found in patent claims is a question of law to be determined by the Court. *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 979 (Fed. Cir. 1995) (en banc), *aff’d*, 517 U.S. 370 (1996). “[T]he interpretation to be given a term can only be determined and confirmed with a full understanding of what the inventors actually invented and intended to envelop with the claim.” *Phillips v. AWH Corp.*, 415 F.3d 1303, 1316 (Fed. Cir. 2005) (quoting *Renishaw PLC v. Marposs Societa’ per Azioni*, 158 F.3d 1243, 1250 (Fed. Cir. 1998)). Consequently, courts construe claims in the manner that “most naturally aligns with the patent’s description of the invention.” *Id.*

“It is a ‘bedrock principle’ of patent law that ‘the claims of a patent define the invention to which the patentee is entitled the right to exclude.’” *Phillips*, 415 F.3d at 1312 (quoting *Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1115 (Fed. Cir. 2004)). Thus, the first step in claim construction is to look to the language of the claims themselves. *Renishaw*, 158 F.3d at 1248 (“The claim construction inquiry . . . begins and ends in all cases with the actual words of the claim.”). To determine the meaning of the claims, courts

begin by considering the intrinsic evidence. *Phillips*, 415 F.3d at 1313; *C.R. Bard, Inc. v. U.S. Surgical Corp.*, 388 F.3d 858, 861 (Fed. Cir. 2004). The intrinsic evidence includes the claims themselves, the specification, and the prosecution history. *Phillips*, 415 F.3d at 1314; *C.R. Bard, Inc.*, 388 F.3d at 861. Where “commonly understood words” are used, the “ordinary meaning of claim language as understood by a person of skill in the art may be readily apparent,” and “claim construction in such cases involves little more than the application of the widely accepted meaning of commonly understood words.” *Phillips*, 415 F.3d at 1314.

V. DISPUTED CLAIM CONSTRUCTIONS

A. “Look up table of M inputs and N outputs” (claims 1, 2, 7, and 13-15)

Professor Iida’s Proposed Construction	Intel’s Proposed Construction
Plain and ordinary meaning.	“Component of a programmable logic circuit device that is composed of memories and is capable of implementing an arbitrary logic circuit of M inputs on at least one of N outputs.”

The term “look up table of M inputs and N outputs” is recited in the preamble of independent claims 1, 7, and 13 of the ’737 patent. For example, claim 1 of the ’737 patent recites:

1. A **look up table of M inputs and N outputs**, comprising:

a plurality of LUT units; and

an internal configuration control circuit controlling an internal configuration of said plurality of LUT units, wherein said internal configuration control circuit comprises

a plurality of selectors selecting I/O signals of said plurality of LUT units, and

a selector control circuit having a memory, controlling said plurality of selectors in accordance with data stored in said memory, and defining the internal configuration of said plurality of LUT units.

Look up tables are well-understood logic components that are commonly described with reference to their specific numbers of inputs and outputs. Hassoun Decl. at ¶ 36. One example of such nomenclature would be a (6,2)-LUT, describing a look up table having six inputs and two outputs (in addition to internal memory cells, selectors, and wiring). *Id.* This is the nomenclature that was used by Altera in, among other things, the patent it acquired on the infringing technology. *See* U.S. Pat. No. 6,943,580 at column 3, lines 30-40, attached as Exhibit B¹. When a look up table has only a single output, it can sometimes be identified just by the number of inputs—e.g., a 4-LUT—in which there are four inputs and a single output is assumed. Hassoun Decl. at ¶ 36. This nomenclature was also used by Altera in the patent it acquired on the infringing technology. *See* Exhibit B at column 3, lines 40-47.

If a look up table is described generically, that is, without reference to the specific numbers of inputs and outputs, variables in the form of letters are used in place of numbers. Hassoun Decl. at ¶ 37. For look up tables with only a single output, one descriptor used in the art is K-LUT (or k-LUT), where the “K” (or “k”) stands for the number of inputs. *Id.* As in the prior examples, this nomenclature was also used by Altera in the patent it acquired on the infringing technology. *See* Exhibit B at column 1, lines 49-58. In corresponding fashion, where both the inputs and outputs are described generically, two variables are used—the first representing the number of inputs, and the second representing the number of outputs. Hassoun Decl. at ¶ 37.

In the ’737 patent, Professor Iida describes look up tables with reference to both inputs and outputs. When referring to look up tables having specific numbers of inputs and outputs, the

¹ Notably, even though Professor Iida’s U.S. patent application was published on January 2, 2003, it was never considered during the prosecution of the ’580 patent. Had it been considered, Professor Iida believes the ’580 patent would never have issued.

'737 patent refers to them in an even more explicit fashion than Altera did. For example, as evident from the brief descriptions of Figures 5-6, the look up table depicted therein is described as “a 6-input 3-output LUT.” See Exhibit A at column 3, lines 10-16. In the background section of the '737 patent, Professor Iida describes LUT nomenclature generally as follows:

In a programmable logic circuit device, the number of bits M of input signal for the logic circuit that can be implemented corresponds to the number of bits of the address of memory composing the LUT, and the number of bits N of output signal corresponds to the number of output bits of the memory. Thus, a logic circuit that can be implemented in one LUT is an arbitrary logic circuit of M inputs and N outputs. Such a LUT is denoted in the present specification as M-input N-output LUT.

Exhibit A at column 1, lines 46-54.

In its opening claim construction brief, Intel advocates for the following construction for the term “look up table of M inputs and N outputs”:

Component of a programmable logic circuit device that is composed of memories and is capable of implementing an arbitrary logic circuit of M inputs on at least one of N outputs.

Dkt. No. 51 at 10. Intel asserts that its proposed construction “clarifies that the claimed ‘look up table of M inputs and N outputs’ must be capable of implementing any arbitrary function of its M inputs and at least one of N outputs.” Dkt. No. 51 at 10. This “clarification,” however, is unnecessary.

Contrary to Intel’s assertions, the plain and ordinary meaning of a look up table need not require: (1) an expression of its relationship to a programmable logic circuit device in which it *may* be used; nor (2) an expression of its capabilities. Rather, one of ordinary skill in the art would readily understand the plain and ordinary meaning of the term “look up table of M inputs and N outputs” upon review of the '737 patent without further description as a component of a programmable logic device or without further description of the extent of its capabilities to

implement logic functions. Hassoun Decl. at ¶¶ 38-39. Unnecessary language may inject ambiguity in the Court’s construction or invite the trier of fact to interpret the Court’s construction, thus defeating the whole purpose of claim construction. *See Markman*, 517 U.S. at 388 (“[J]udges, not juries, are the better suited to find the acquired meaning of patent terms.”).

A disputed claim term should be construed in light of its “ordinary and customary meaning,” which is “the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application.” *Phillips*, 415 F.3d at 1312. Moreover, courts indulge a heavy presumption that claim terms carry their full ordinary and customary meaning “unless the patentee unequivocally imparted a *novel* meaning to those terms or expressly relinquished claim scope during prosecution.” *Omega Eng’g, Inc. v. Raytek Corp.*, 334 F.3d 1314, 1323 (Fed. Cir. 2003) (internal citation omitted, emphasis supplied); *see also Teleflex, Inc. v. Ficosa N. Am. Corp.*, 299 F.3d 1313, 1325-26 (Fed. Cir. 2002) (“In the absence of an express intent to impart a novel meaning to claim terms, an inventor’s claim terms take on their ordinary meaning”). Indeed, even where a patentee acts as his own lexicographer by providing explicit definitions of claim terms, where the patentee does not unequivocally impart a *novel* meaning to claim terms the plain and ordinary meaning should still prevail. *See, e.g., Uniloc Luxembourg S.A.*, 2014 U.S. Dist. LEXIS 172979 at *29; *see also Phillips*, 415 F.3d at 1316 (when the specification “reveal[s] a *special* definition given to a claim term by the patentee *that differs from the meaning it would otherwise possess*[.] . . . the patentee’s lexicography governs.”) (emphasis supplied).

It bears repeating that the standard for finding lexicography is “exacting.” *GE Lighting Solutions*, 750 F.3d at 1309. To act as his own lexicographer, a patentee must “clearly set forth a definition of the disputed claim term,” and “clearly express an intent to define the term.” *Id.*

(quoting *Thorner v. Sony Computer Entm't Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012); *see also Renishaw*, 158 F.3d at 1249. The patentee's lexicography must appear "with reasonable clarity, deliberateness, and precision." *Renishaw*, 158 F.3d at 1249.

While Intel claims that Professor Iida acted as his own lexicographer (despite failing to satisfy the exacting standard for doing so), Intel readily concedes that the language of the '737 patent that Intel asserts constitutes lexicography "is consistent with the plain and ordinary meaning of that phrase." Dkt. No. 51 at 12. As noted above, where a patentee does not unequivocally impart a *novel* meaning to claim terms, the plain and ordinary meaning should prevail. *See, e.g., Uniloc Luxembourg S.A.*, 2014 U.S. Dist. LEXIS 172979 at *29.

Under these circumstances, there is no need to construe the claim term "look up table of M inputs and N outputs." *See O2 Micro Int'l Ltd. v. Beyond Innovation Tech. Co.*, 521 F.3d 1351, 1362 (Fed. Cir. 2008) ("district courts are not (and should not be) required to construe every limitation present in a patent's asserted claims."). As a result, the Court should apply the plain and ordinary meaning to the disputed term.

B. "LUT Units" (all asserted claims)

Professor Iida's Proposed Construction	Intel's Proposed Construction
Plain and ordinary meaning.	Indefinite. Otherwise, if not indefinite, each "LUT unit" is a "component of a programmable logic circuit device that is composed of memories and is capable of implementing an arbitrary logic circuit of its inputs with at least one output."

The term "LUT units" is recited in all of the asserted claims, which are claims 1, 2, 7, 8, and 13-15 of the '737 patent. For example, claim 1 of the '737 patent recites:

1. A look up table of M inputs and N outputs, comprising:

a plurality of **LUT units**; and

an internal configuration control circuit controlling an internal configuration of said plurality of **LUT units**, wherein said internal configuration control circuit comprises

a plurality of selectors selecting I/O signals of said plurality of **LUT units**, and

a selector control circuit having a memory, controlling said plurality of selectors in accordance with data stored in said memory, and defining the internal configuration of said plurality of **LUT units**.

In its opening brief, Intel asserts that the phrase “LUT units” renders the asserted claims indefinite or requires construction. According to Intel, the claimed LUT units are simply “smaller look up tables (i.e., LUTs) that, when taken together, comprise the larger ‘look up table of M inputs and N outputs.’” Dkt. 51 at 1. Yet, as noted above, Intel’s description fails to capture the essence of our common, everyday understanding of what it means for something to be a “unit”—that is, a basic, unitary, individual element. Hassoun Decl. at ¶ 42. A critical analysis of Intel’s simplified block diagram of an exemplary look up table (shown at pages 7 and 16 of its opening brief) demonstrates how Intel obfuscates what a LUT unit is by engaging in arbitrary box drawing divorced from the reality of how look up tables are actually implemented.

Where “commonly understood words” are used, the “ordinary meaning of claim language as understood by a person of skill in the art may be readily apparent,” and “claim construction in such cases involves little more than the application of the widely accepted meaning of commonly understood words.” *Phillips*, 415 F.3d at 1314. Claim terms need not be construed where they are “neither unfamiliar to the jury, confusing to the jury, nor affected by the specification or prosecution history.” *Bd. of Trustees of Leland Stanford Junior Univ. v. Roche Molecular Sys., Inc.*, 528 F. Supp. 2d 967, 976 (N.D. Cal. 2007); *United States Well Servs. v. Halliburton Co.*, 2022 U.S. Dist. LEXIS 50347 (W.D. Tex. January 17, 2022); *see also United States Surgical Corp. v. Ethicon, Inc.*, 103 F.3d 1554, 1568 (Fed. Cir. 1997) (“Claim construction is a matter of

resolution of disputed meanings and technical scope, to clarify and when necessary to explain what the patentee covered by the claims, for use in the determination of infringement. It is not an obligatory exercise in redundancy.”). Thus, while a court’s role is to construe claim terms as matter of law, “part of this role is to determine the extent of which to construe the claims or whether construction is even necessary.” *800 Adept, Inc. v. AT&T Mobility, LLC*, 2008 U.S. Dist. LEXIS 93179, at *35 (E.D. Tex. July 23, 2008). Further, where additional language “may be unduly limiting, confusing, or redundant, it is in the court’s power to determine that no construction is necessary.” *Id.*

One of ordinary skill in the art well understands what a LUT unit is according to its plain and ordinary meaning, particularly upon reading the written description of the ’737 patent and reviewing its figures. Hassoun Decl. at ¶ 43. The ’737 patent provides numerous of examples of LUT units that would assist a person of ordinary skill in the art in understanding the meaning of the term. *Id.* at ¶ 44. For example, as shown in Figure 6 of the ’737 patent, and described at column 5, lines 26-29, “the 6-input 3-output LUT 7 (121) is comprised of a mode changing memory 71, selectors 721-726, **and 3-input 1-output LUT units (memory array) 731-738.**”

As further described in the ’737 patent:

Each of 3-input 1-output LUT units 731-738 is comprised of an address decoder, a memory and a selector, as described later, and outputs 1 bit signal in response to 3 bit input signal, respectively. Thus, signals A, B, C are input to each of LUT units 731, 732, 734-736 and 738, and one of the signals A or C and one of the signals B or D selected by selection signal F0, and the signal C is input to the LUT unit 733, and one of the signals A or D, and one of the signals B or E, and one of the signals C or F, selected by the selection signal F1 is input to the LUT unit 737. Output signals from the LUT units 731-738 are input to a selector (selector for selecting output signal) 726, and one of the signals is selected by selection signal F2 (D, E, F, X, Y, Z) specified by signals D, E, F and data X, Y, Z, and is output as signal V. The signal Q is the output signal from the LUT unit 731, and the signal W is the output signal from the LUT unit 737.

Exhibit A at column 5, lines 46-61.

Figures 7 and 8 of the '737 patent each show block diagrams of exemplary 3-input 1-output LUT units that can be used in the 6-input 3-output look up table depicted in Fig. 6. The LUT unit shown in Figure 7 is comprised of an address decoder, a selector, and two sets of 4-bit memory unit groups M11-M14, M21-M24. The address decoder decodes 2-bit input signal A, B to designate each one of the memory unit groups M1-M14 and M21-M24, and further according to the input signal C, selects one of the sets M11-M14 or M21-M24 to output data. *See* Exhibit A at column 5, line 66 to column 6, line 6. The LUT unit shown in Figure 8 “is comprised of an address decoder 7313, and 8 bit memory unit groups M31-M38. The address decoder 7313 decodes the 3 bit input signals A, B, C, to designate one of the memory unit groups M31-M38, and output the data (Q).” Exhibit A at column 6, lines 10-14.

Figure 9 of the '737 patent is a block diagram showing another exemplary 6-input 3-output look up table having an internal configuration that is different from the 6-input 3-output look up table shown in Fig. 6. Figures 10 and 11 of the '737 patent each show block diagrams of exemplary 3-input 2-output LUT units that can be used in the 6-input 3-output look up table depicted in Fig. 9.

Importantly, whether a given look up table of M inputs and N outputs comprises a plurality of LUT units is not a matter of how simplified block diagrams of look up tables are *viewed*, but rather how look up tables are actually *implemented*, that determines whether or not a look up table comprises a plurality of LUT units. Hassoun Decl. at ¶ 53. A single, unitary structure that is a LUT is exactly that, an irreducible LUT unit. *Id.* at ¶ 55. A person of ordinary skill in the art would understand that, by design, a LUT unit cannot be fractured or divided into smaller LUT units. *Id.* This understanding would be confirmed by reference to the '737 patent, and specifically to Figs. 6-11. *Id.*

A person of ordinary skill in the art would understand the meaning of the term “LUT units” as that term is used in the ’737 patent. *Id.* at ¶ 56. A person of ordinary skill in the art would understand that a constructed “look up table of M inputs and N outputs” as taught by the ’737 patent is not ***divided*** into LUT units, but rather ***implemented*** with a plurality of LUT units. *Id.* As a result, a person of ordinary skill in the art would well understand the scope of structures that satisfy the claims. *Id.*

Intel presents an example of a simplified block diagram of a 3-input, 2-output look up table. *See* Dkt. 51 at 7 and 16. The three inputs are designated as A, B, and C, and the two outputs are designated as Q and R. *Id.* According to Intel, this diagram “*may be viewed* as being comprised of four smaller look up tables with the components shown inside the yellow boxes, each having two inputs (A and B), with the outputs from the two yellow look up tables on the left proceeding to output selector 1 (i.e., an output selector outside the look up table), and the outputs from the two yellow look up tables on the right proceeding to output selector 2 (also outside the look up table).” *Id.* at 7 (emphasis supplied). Alternatively, according to Intel, this diagram “*may be viewed* as having two (rather than four) smaller look up tables with the components shown in the green boxes, each having three inputs (A, B, and C), with no selectors connected to outputs Q and R from the look up tables.” *Id.* (emphasis supplied).

Intel’s analysis is plainly incorrect. It is not a matter of how simplified diagrams ***may be viewed***, but rather how physical look up tables are actually ***designed and implemented***, that determines whether or not they comprise a plurality of LUT units or not. Hassoun Decl. at ¶ 60. As a result, Intel’s description of its exemplary diagram is misleading by classifying it both a “single device” and “having four LUT units.” *Id.* A person of ordinary skill in the art, and Intel’s engineers, would clearly understand the distinction. *Id.*

Intel also invokes the analogy to apartment units in its discussion of the term “unit.” This is actually an apt analogy. Just as one does not regard separate but adjacent apartment units as a single unit, one also does not consider individual rooms (or suites of rooms) within a single apartment to be separate apartment units either. Analogous to Intel’s yellow boxes, if two people were to exit adjacent bedrooms within an apartment into an adjoining interior hallway, neither person would be regarded as having exited the unit—that only happens when one exits the front doorway of the apartment into an exterior hallway. Similarly, and analogous to Intel’s green boxes, if the layout of a two-bedroom apartment with one bathroom and a kitchen were “viewed” as one apartment “unit” having one bedroom and the kitchen and another apartment “unit” having the other bedroom and the bathroom, one would not suddenly have two separate apartment units as each requires a kitchen *and* a bathroom. Importantly, if one is going to determine apartment units based only on a floor plan, the floor plan must contain sufficient detail.

A person of ordinary skill in the art would understand that the ’737 patent is about the implementation, architecture, configuration, and construction (i.e. build) of circuits—not how such circuits *may be* viewed. *Id.* at ¶ 61; *see also* pin citations to the ’737 patent referenced therein. Intel’s simplified diagram alone does not actually provide enough detail to a person of ordinary skill in the art to determine whether or not its green or yellow boxes represent individual LUT units, but the details of how a given look up table is actually *implemented* would resolve any ambiguity. *Id.* at ¶ 62. A person of ordinary skill in the art would easily identify a LUT unit given sufficient information about the design of a given look up table. *Id.* at ¶ 63.

In the present case, it is Intel which is engaging in arbitrary box drawing on a simplified block diagram without regard to how these circuitry components are actually constructed. Intel

obfuscates the issue by its focus on how *diagrams may be viewed* rather than on how *look up tables are actually designed and implemented*. The '737 patent is abundantly clear to a person of ordinary skill in the art—a LUT unit is described as a “memory array” and illustrated clearly in a variety of embodiments (*e.g.*, Figures 6-11). Regardless of how one might conceptually divide a block diagram in one’s mind, the question of Intel’s infringement is clear and determinable: Are the look up tables used in Intel’s FPGA chips built using a plurality of LUT units? There is no confusion nor is there indefiniteness to one of ordinary skill in the art. They are. Moreover, in view of the common, everyday understanding of what it means for something to be a “unit,” the term “LUT unit” does not require construction. Under these circumstances, there is simply no need to construe “LUT unit.” *See O2 Micro*, 521 F.3d at 1362 (“district courts are not (and should not be) required to construe every limitation present in a patent’s asserted claims.”). As a result, the Court should apply the plain and ordinary meaning to the term “LUT unit.”

VI. CONCLUSION

For the foregoing reasons, Professor Iida respectfully requests that the Court refrain from construing the disputed claim terms as they need only be accorded their plain and ordinary meaning.

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Respectfully submitted,

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CERTIFICATE OF SERVICE

I hereby certify that on February 9, 2023, a true and correct copy of the foregoing was served on all counsel of record who have appeared in this case via the Court's CM/ECF system per Local Rule CV-5.

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