

**IN THE UNITED STATES DISTRICT COURT  
FOR THE WESTERN DISTRICT OF TEXAS  
WACO DIVISION**

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PROFESSOR MASAHIRO IIDA,

Plaintiff,

v.

INTEL CORPORATION,

Defendant.

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Case No. 6:22-cv-00662-ADA

**JURY TRIAL DEMANDED**

**PROFESSOR MASAHIRO IIDA'S SURREPLY CLAIM CONSTRUCTION BRIEF**

**TABLE OF CONTENTS**

I. INTRODUCTION ..... 1

II. ARGUMENT ..... 2

    A. “Look up table of M inputs and N outputs” ..... 2

    B. “LUT units” ..... 2

III. CONCLUSION ..... 5

**TABLE OF AUTHORITIES**

| <b>Cases</b>                                                                                  | <b>Page</b> |
|-----------------------------------------------------------------------------------------------|-------------|
| <i>Funai Elec. Co. v. Daewoo Elecs. Corp.</i> ,<br>616 F.3d 1357 (Fed. Cir. 2010) .....       | 2           |
| <i>GE Lighting Solutions, LLC v. AgiLight, Inc.</i> ,<br>750 F.3d 1304 (Fed. Cir. 2014) ..... | 1           |

## I. INTRODUCTION

Intel’s reply brief mischaracterizes Professor Iida’s position regarding claim construction.

*First*, Intel reiterates its false and unsupported claim that Professor Iida has acted as his own lexicographer with regard to the claim term “look up table of M inputs and N outputs.” The language of U.S. Patent No. 6,812,737 (“the ’737 patent”) comes nowhere close to meeting the exacting standard for lexicography—clearly setting forth a definition of the disputed claim term and clearly expressing an intent to define that term. *See GE Lighting Solutions, LLC v. AgiLight, Inc.*, 750 F.3d 1304, 1309 (Fed. Cir. 2014). The passages of the ’737 patent that Intel cites *describe*—not define—a look up table of M inputs and N outputs, and Intel readily concedes that such language is “consistent with the plain and ordinary meaning of that phrase.” Dkt. No. 51 at 12. Applying the plain and ordinary meaning would neither ignore any asserted lexicography nor would it invite juror confusion as to the scope of the claims. As a result, no construction is required.

*Second*, Intel’s rebuttal regarding the term “LUT unit” continues its avoidance of our common, everyday understanding of what it means to be a “unit”—a basic, unitary, individual element. Intel also reiterates its obfuscation of the plain and ordinary meaning of “unit” by repeating its arbitrary box drawing on a simplified representation of an exemplary look up table. Whether a given look up table of M inputs and N outputs comprises a plurality of LUT units is not a matter of how an abstract representation (e.g. a figure) *may be viewed*, but rather how a look up table itself is *implemented*. Here, as Intel’s Adaptive Logic Modules are designed and implemented using a plurality of LUT units, infringement as to this claim element is evident. As a result, the term “LUT unit” is neither indefinite nor does it require construction.

## II. ARGUMENT

### A. “Look up table of M inputs and N outputs”

As described in the ’737 patent, a “look up table ... is composed of memories, and is capable of implementing an arbitrary logic circuit.” ’737 patent at column 1, lines 25-28. The ’737 patent goes on to explain:

In a programmable logic circuit device, the number of bits M of input signal for the logic circuit that can be implemented corresponds to the number of bits of the address of memory composing the LUT, and the number of bits N of output signal corresponds to the number of output bits of the memory. Thus, a logic circuit that can be implemented in one LUT is an arbitrary logic circuit of M inputs and N outputs. Such a LUT is denoted in the present specification as M-input N-output LUT.

*Id.* at column 1, lines 46-54.

Intel quotes the Federal Circuit for the proposition that “construction of a claim term is proper if ‘the explanation aids the court and the jury in understanding the term as it is used in the claimed invention.’” Dkt. No. 57 at 2 (quoting *Funai Elec. Co. v. Daewoo Elecs. Corp.*, 616 F.3d 1357, 1366 (Fed. Cir. 2010)). Intel then speculates that “without a construction, the jury might incorrectly assume that a ‘look up table of M inputs and N outputs’ must be able to perform an arbitrary function of M inputs on *each* of its N outputs or need not be able to perform any arbitrary function of its inputs *at all*.” *Id.* (emphasis in original). Intel’s speculation, however, is just that—speculation. Moreover, Intel undermines its own position by stating—in the very next sentence—that “neither party appears to advocate for this position.” *Id.* Intel’s concern regarding potential jury confusion is entirely fictive and unwarranted.

### B. “LUT units”

Intel continues to engage in arbitrary box drawing on diagrams of look up tables which fail to provide sufficient detail as to their implementation, or which refute Intel’s position. By

staying in the conceptual realm, Intel attempts to inject unwarranted confusion where none exists in practice.

To begin with, Intel continues to ignore the common, everyday understanding of the word “unit”—a basic, unitary, individual element. Contrary to its assertion, Intel’s exemplary figure at page 5 of its reply brief is neither an “implementation” nor a “physical device.” Rather, it is merely a conceptual diagram that, on its own, does not provide sufficient implementation detail to allow a person of ordinary skill in the art to determine whether it depicts one or more individual LUT units.

A person of ordinary skill in the art would understand the meaning of the term “LUT units” and that meaning is consistent with its use in the ’737 patent. *See* Declaration of Marwan Hassoun (“Hassoun Decl.”) at ¶ 56. A person of ordinary skill in the art would understand that a constructed “look up table of M inputs and N outputs” as taught by the ’737 patent is not *divided* into LUT units, but rather *implemented* with a plurality of LUT units. *Id.* As a result, a person of ordinary skill in the art would well understand the scope of structures that satisfy the claims. *Id.* It is Intel that is being vague, not the claim language.

Intel asserts that “nothing in the claims explains how to identify the LUT units in a particular device.” Dkt. No. 57 at 5. This is simply not true. The claims are abundantly clear as the term “LUT unit” would be understood by a person of ordinary skill as an individual LUT that cannot be fractured or divided *into smaller LUT units*. The plain meaning of “LUT units” supports this position. Circuit components are not abstractions—they are hardware that exist in the real world. By contrast, *representations* of circuit components *are* abstractions that may or may not provide sufficient detail to determine how such circuit components have actually been constructed. Intel blurs the distinction between the two.

Intel asserts that “everything in a circuit is ‘reducible’ down to a sea of transistors deposited on silicon.” *Id.* at 7. This is an entirely fallacious argument that mischaracterizes Professor Iida’s position. It is not a question of whether a LUT unit is reducible “down to a sea of transistors” but, rather, whether a LUT unit is reducible *to other LUTs*. Analogously, an individual water molecule may be “reduced” to two hydrogen atoms and one oxygen atom, but no one would confuse these individual atoms with water.

Intel’s example of metric measurements of length further demonstrates its misdirection. Again, Intel chooses to mix different units (a meter vs. a centimeter) and reduces one type of unit to another type of unit. In Intel’s oversimplified analogy, Intel asserts that a meter is a unit of length that can be “logically reduced” to 100 centimeters. *Id.* at 8. In other words, the *concept* of a meter can be viewed as equivalent to 100 centimeters. But in the physical world, implementation is critical. If one were presented with a single meter-long rod, it would be regarded as a single meter-length unit. If, however, one were presented with a chain having an overall length of one meter that was composed of 100 individual centimeter-length links, then the chain would comprise 100 centimeter-length units. Again, implementation details matter.

In another example, Intel asserts that a two-bedroom apartment that has two bathrooms and two kitchens could be “reduced” into two “apartment units.” *Id.* But it is not merely a matter of how one *views* this imagined apartment that makes it one or two units in one’s mind. Rather, it is and remains a single apartment unit unless and until one physically converts it into two separate units by constructing a dividing wall to separate groups of rooms and installing a second entrance so that the two resulting apartment units each have their own entry. Once again, implementation details matter.

Most tellingly, Intel introduces a figure from an Altera<sup>1</sup> White Paper on FPGA architecture that illustrates this point perfectly. As explained in the White Paper:

Figure 2 *shows a 4-LUT*, which consists of 16 bits of SRAM and a 16:1 multiplexer implemented as a tree of 2:1 multiplexers. The 4-LUT can implement any function of 4 inputs (A, B, C, D) by setting the appropriate value in the LUT-mask. To simplify the 4-LUT in Figure 2, *it can also be built from two 3-LUTs* connected by a 2:1 multiplexer.

Dkt. No. 57-2 at 3 (emphasis supplied). As is evident from the plain language of the White Paper itself, while both figures represent the same conceptual/functional diagram, these two figures actually show *two different and distinct implementations*. As explained in the White Paper, the figure on the left shows a *single* LUT unit (comprising one 4-LUT), while the figure on the right shows a 4-LUT “built from” *two* LUT units, that is, two 3-LUTs. *Id.* Intel’s colorful additions to the figure on the right are further examples of its arbitrary box drawing that are utterly divorced from the realities of implementation. The White Paper makes crystal clear that these figures represent two, and only two, distinct implementations. One of ordinary skill would readily understand (as explained by the figure and the description of how it was designed/built) the figure on the left as built as a single LUT unit, and the figure on the right as built from two, *and only two*, LUT units. Intel’s fanciful imaginings of four 2-LUTs or eight 1-LUTs are negated by the actual language of the White Paper. There is no ambiguity nor is there any confusion.

### III. CONCLUSION

For the foregoing reasons, Professor Iida respectfully requests that the Court refrain from construing the disputed claim terms as they need only be accorded their plain and ordinary meaning.

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<sup>1</sup> Altera, the original infringer, was acquired by Intel in 2015, and the referenced Altera White Paper remains available on Intel’s website at: <https://www.intel.com/content/dam/support/us/en/programmable/support-resources/bulk-container/pdfs/literature/wp/wp-01003.pdf>.

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Respectfully submitted,

/s/ Joshua R. Slavitt

Joshua R. Slavitt\*  
Pennsylvania State Bar No. 63139  
SLAVITT IP LAW, LLC  
535 Hamilton Road  
Merion Station, PA 19066  
Phone: (215) 880-2569  
Email: [josh@slavittiplaw.com](mailto:josh@slavittiplaw.com)

Travis C. Barton  
Texas State Bar No. 00790276  
Richard D. Milvenan  
Texas State Bar No. 14171800  
McGINNIS & LOCHRIDGE LLP  
1111 W. 6th Street, Bldg. B, Suite 400  
Austin, TX 78703  
Phone: (512) 495-6005  
Facsimile: (512) 505-6305  
Email: [tcbarton@mcginnislaw.com](mailto:tcbarton@mcginnislaw.com)  
Email: [rmilvenan@mcginnislaw.com](mailto:rmilvenan@mcginnislaw.com)

Jacob C. Cohn\*  
Pennsylvania State Bar No. 54139  
GORDON REES SCULLY MANSUKHANI LLP  
1717 Arch Street, Suite 610  
Philadelphia, PA 19103  
Phone: (215) 561-2300  
Email: [jcohn@grsm.com](mailto:jcohn@grsm.com)

*\*Admitted pro hac vice*

*Attorneys for Plaintiff,  
Professor Masahiro Iida*

**CERTIFICATE OF SERVICE**

I hereby certify that on March 8, 2023, a true and correct copy of the foregoing was served on all counsel of record who have appeared in this case via the Court's CM/ECF system per Local Rule CV-5.

/s/ Joshua R. Slavitt

Joshua R. Slavitt