

**IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION**

PROFESSOR MASAHIRO IIDA,

Plaintiff,

v.

INTEL CORPORATION,

Defendant.

Case No. 6:22-cv-00662-ADA

Jury Trial Demanded

**INTEL CORPORATION'S FIRST AMENDED
PRELIMINARY INVALIDITY CONTENTIONS**

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Pursuant to the Court’s Standing Order Governing Proceedings 4.2—Patent Cases § II.4 and the Scheduling Order in the above-captioned matter (Docket No. 41), Defendant Intel Corporation (“Intel”) provides these first amended preliminary invalidity contentions (“Invalidity Contentions”) for the claims asserted by Plaintiff Masahiro Iida (“Plaintiff” or “Iida”) from U.S. Patent No. 6,812,737 (the “’737 patent” or “Asserted Patent”) in Plaintiff’s Preliminary Infringement Contentions served September 20, 2022 (“Infringement Contentions”), namely claims 1, 2, 7, 8, and 13–15 of the ’737 patent (collectively, the “Asserted Claims”).

These Invalidity Contentions address the invalidity of the Asserted Claims, identify additional reservations and explanations, and describe the accompanying document production. Intel reserves the right to amend these contentions as provided by Federal Rule of Civil Procedure 26(e), the Court’s Standing Order Governing Proceedings 4.2—Patent Cases, and any other applicable law, rule, or precedent. Intel also reserves the right to amend and/or supplement these Invalidity Contentions based on information subsequently identified and/or should Iida be permitted to correct, clarify, amend, and/or supplement its Infringement Contentions.

I. INTRODUCTION

A. Iida’s Infringement Contentions

In his Infringement Contentions, Iida identified June 29, 2001, as his alleged priority date for the ’737 patent. Without admitting the validity of any priority date, Intel uses June 29, 2001, as the priority date of the ’737 patent for the purposes of these Invalidity Contentions.

Iida’s Infringement Contentions are deficient in that they fail to properly and completely disclose how the Accused Products allegedly infringe the Asserted Claims. For example, Iida fails to explain how the alleged “selector control circuit” controls “said plurality of selectors in accordance with data stored in said memory[.]” In particular, Iida identifies a group of multiplexers as the alleged “selectors,” and he does not explain how those selectors are

controlled in accordance with data stored in memory. To the extent Iida contends that components downstream from the alleged “output signal selectors,” such as flip-flops, are part of the alleged “look up table” of the accused product(s), Iida also fails to explain how those components could be considered part of the look up table. Intel reserves the right to amend and/or supplement these invalidity contentions should the court permit Iida to correct, clarify, amend, and/or supplement its Infringement Contentions.

B. Overview of Invalidity Grounds

The Asserted Claims are invalid under 35 U.S.C. §§ 102 and 103¹ because they are anticipated by, or would have been obvious to a skilled artisan in view of, the prior art. *See* Section II.A, *infra*. The Asserted Claims are also invalid under § 102(f) because the ’737 patent fails to name all joint inventors, including Toshinori Sueyoshi. Furthermore, the Asserted Claims are invalid under 35 U.S.C. § 112 for lack of written description, lack of enablement, indefiniteness, and/or because they do not set forth what the patentee regarded as the invention. *See* Section II.B, *infra*. The Asserted Claims are also unenforceable due to inequitable conduct. *See* Section II.C, *infra*.

These disclosures are made based on prior art presently known to Intel. Merits discovery in this case has not yet commenced. The Court has not construed the terms of the Asserted Claims, and the Court has not determined the level of education or experience of one of ordinary skill in the art. Intel reserves the right to modify, amend, and/or supplement these Invalidity Contentions in view of, without limitation, information provided by Iida concerning its infringement allegations; additional discovery concerning the alleged priority, conception, and

¹ Citations in these contentions to 35 U.S.C. §§ 102 and 103 are to the pre-AIA version of those statutes that are applicable to the Asserted Patent.

reduction to practice of any of the Asserted Claims; additional prior art obtained through discovery or further investigation, including without limitation discovery from Iida or third parties; claim constructions by the Court; positions taken by Iida in this action or any other proceeding; the parties' expert reports; and/or as other circumstances warrant.

II. INVALIDITY CONTENTIONS

Intel's Invalidity Contentions are based on information currently available to Intel and its current understanding of the Asserted Claims as stated in Iida's deficient Infringement Contentions, without the benefit of a claim construction order, fact discovery, or expert testimony. Intel objects to any attempt to infer claim construction positions from any identification of prior art or invalidity contention contained herein. Certain positions put forth in these Invalidity Contentions are predicated (to the extent that Iida's positions can be ascertained) on Iida's incorrect interpretation of the Asserted Claims as evidenced by his Infringement Contentions provided to Intel and his claim construction positions. Intel's Invalidity Contentions are not, and should not be construed as, admissions or adoptions of a particular claim scope or construction, or as an admission that any particular element of an asserted claim is found in any accused product. Intel reserves the right to adopt claim construction positions that differ from positions put forth in this document. Intel disagrees with Iida's application of the Asserted Claims to the accused product(s) (to the extent that Iida's positions can be ascertained), and Intel expressly denies infringement.

A. Invalidity Under 35 U.S.C. §§ 102 and 103

Intel contends that all the Asserted Claims are invalid as anticipated under 35 U.S.C. § 102 and/or obvious under 35 U.S.C. § 103. Intel relies on and incorporates all prior art references cited on the cover of the Asserted Patent and in its prosecution history, as well as all prior art cited on the cover of the counterpart Japanese Patent No. 3580785B2, including for

supporting Intel's arguments regarding the obviousness of the Asserted Claims. Intel further relies on and incorporates by reference, as if originally set forth herein, all invalidity positions, and all associated prior art and claim charts, disclosed to Iida by potential or actual licensees to any of the Asserted Claims. Intel hereby discloses and identifies as if originally set forth herein, all prior art references listed and/or asserted in the above as invalidating prior art against each of the Asserted Claims. In addition, Intel identifies prior art patents, publications, products, and systems that disclose the elements of the Asserted Claims explicitly, inherently, or as part of an obvious combination, and may also be relied on to show the state of the art in the relevant timeframes and/or reasons or motivations to combine prior art references.

In those instances in which Intel asserts that an Asserted Claim is invalid under 35 U.S.C. § 112, Intel has applied the prior art in accordance with its assumption that Iida contends such Asserted Claim (1) has sufficient supporting written description, (2) is enabled, (3) is not indefinite, and (4) sets forth what the inventor(s) regarded as the invention. Intel's Invalidity Contentions should not be construed as an admission that any Asserted Claim meets the requirements of § 112.

1. Prior Art for the '737 Patent

Subject to its reservation of rights, Intel identifies below (in Tables 1, 2, and 3) each item of prior art that anticipates or renders obvious one or more of the Asserted Claims. Table 1 provides the identity of each prior art patent publication by its number, filing date, and date of issuance or publication. Table 2 provides the identity of each non-patent prior art publication including, where possible, its title, date of publication, author, and publisher. Table 3 provides the identity of each system or product that was known or used in the United States before the purported date of invention, *see* 35 U.S.C. § 102(a), and/or that was the subject of public use or sale in the United States more than one year prior to the date of application for the '737 patent,

see 35 U.S.C. § 102(b), including (where possible): the name of the item; the identity of the person or entity that made the sale, offer for sale, or use or that made the information known; and date the sale, offer for sale, or use took place or the information became known. Prior art patents and patent publications filed in or designating the United States additionally qualify as prior art under 35 U.S.C. § 102(e). Tables 1–3 further include references that may be relied upon to show the state of the art at the time and/or inherency regardless of whether the references themselves qualify as prior art.

Discovery is ongoing, and Intel expects relevant discovery to be obtained from Plaintiff and third parties. Intel’s prior art investigation, therefore, is not yet complete. As a result, Intel reserves the right to present additional items of prior art under 35 U.S.C. § 102 or § 103 located through discovery. Intel specifically reserves the right to supplement these Invalidity Contentions with information obtained through discovery of Plaintiff and third parties.

(a) *Table 1: Prior Art Patents / Patent Publications*

Patent / Application	Filing Date / Priority Date²	Published / Issue Date	Short Name	Starting Bates Number
U.S. Patent No. 5,587,921	11/20/1995	12/24/1996	Agrawal I	97300DOC000177958
U.S. Patent No. 5,982,193	12/22/1997	11/9/1999	Agrawal II	97300DOC000178036
U.S. Patent No. 6,380,759	7/26/2000	4/30/2002	Agrawal III	97300DOC000178118
U.S. Patent No. 5,889,413	11/22/1996	3/30/1999	Bauer I	97300DOC000178210
U.S. Patent No. 6,323,682	5/19/2000	11/27/2001	Bauer II	97300DOC000178223
U.S. Patent No. 6,288,568	5/19/2000	9/11/2001	Bauer III	97300DOC000178259

² Some of the patents or patent applications claim priority to earlier dates, as disclosed on the face of those patent or patent applications.

Patent / Application	Filing Date / Priority Date²	Published / Issue Date	Short Name	Starting Bates Number
U.S. Patent No. 6,297,665	5/19/2000	10/2/2001	Bauer IV	97300DOC000178297
U.S. Patent No. 4,706,216	2/27/1985	11/10/1987	Carter I	97300DOC000178333
U.S. Patent No. 4,758,985	3/28/1986	7/19/1988	Carter II	97300DOC000178355
U.S. Patent No. 5,224,056	10/30/1991	6/29/1993	Chene	97300DOC000178382
U.S. Patent No. 5,815,726	6/7/1995	9/29/1998	Cliff I	97300DOC000178415
U.S. Patent No. 5,909,126	6/28/1996	6/1/1999	Cliff II	97300DOC000178439
U.S. Patent No. 5,926,036	8/19/1998	6/20/1999	Cliff III	97300DOC000178457
U.S. Patent No. 5,999,015	7/29/1997	12/7/1999	Cliff IV	97300DOC000178508
U.S. Patent No. 6,122,720	8/7/1998	9/19/2000	Cliff V	97300DOC000178523
U.S. Patent No. 5,258,668	5/8/1992	11/2/1993	Cliff VI	97300DOC000193018
U.S. Patent No. 5,260,611	5/8/1992	11/9/1993	Cliff VII	97300DOC000193027
U.S. Patent No. 5,274,581	5/8/1992	12/28/1993	Cliff VIII	97300DOC000193047
U.S. Patent No. 4,870,302	2/19/1988	9/26/1989	Freeman I	97300DOC000178546
U.S. Patent No. 5,343,406	7/28/1989	8/30/1994	Freeman II	97300DOC000178572
U.S. Patent No. 5,488,316	4/26/1995	1/30/1996	Freeman III	97300DOC000178591
U.S. Patent No. 5,414,377	10/18/1994	5/9/1995	Freidin I	97300DOC000178610
U.S. Patent No. 5,566,123	2/10/1995	10/15/1996	Freidin II	97300DOC000178617

Patent / Application	Filing Date / Priority Date²	Published / Issue Date	Short Name	Starting Bates Number
Japanese Patent Application Publication No. H09-121153A	10/25/1995	5/6/1997	Fujii	97300DOC000178631 97300DOC000178646 97300DOC000178677
U.S. Patent No. 6,026,227	9/24/1997	2/15/2000	Furtek	97300DOC000178727
Japanese Patent Application Publication No. H04-335453A	5/10/1991	11/24/1992	Giichi	97300DOC000178758
U.S. Patent No. 6,351,143	6/15/2001	2/26/2002	Guccione	97300DOC000178761
Japanese Patent Application Publication No. S64-072197A	9/3/1987	3/17/1989	Hersh	97300DOC000178776
Japanese Patent Application Publication No. S64-86280A	9/28/1987	3/30/1989	Hirosawa	97300DOC000192939
U.S. Patent No. 4,750,155	9/19/1985	6/7/1988	Hsieh I	97300DOC000178783
U.S. Patent No. 5,295,090	5/24/1993	3/15/1994	Hsieh II	97300DOC000178792
U.S. Patent Application Pub. No. 2002/0079921 A1	11/9/2001	6/27/2002	Kaviani I	97300DOC000178816
U.S. Patent No. 6,978,427	5/18/2004	12/20/2005	Kaviani II	97300DOC000178863
U.S. Patent No. 5,801,547	10/23/1996	9/1/1998	Kean	97300DOC000178884
Japanese Patent Application Publication No. H03-063846A	8/2/1989	3/19/1991	Kimura	97300DOC000178908 97300DOC000178899

Patent / Application	Filing Date / Priority Date²	Published / Issue Date	Short Name	Starting Bates Number
Japanese Utility Model Application Publication No. S62-195861U	5/29/1986	12/12/1987	Kondo	97300DOC000192950
U.S. Patent No. 6,323,677	4/4/2000	11/27/2001	Lane	97300DOC000178927
U.S. Patent No. 6,476,636	9/2/2000	11/5/2002	Lien	97300DOC000178946
U.S. Patent No. 6,678,646	12/14/1999	1/13/2004	McConnell	97300DOC000178976
U.S. Patent No. 6,157,209	12/18/1998	12/5/2000	McGettigan	97300DOC000178988
U.S. Patent No. 5,991,788	3/14/1997	11/23/1999	Mintzer	97300DOC000178997
Japanese Patent Application Publication No. H01-183685A	1/18/1988	7/21/1989	Mizoguchi	97300DOC000192970
U.S. Patent No. 6,255,849	2/4/2000	7/3/2001	Mohan I	97300DOC000179007
U.S. Patent No. 6,336,208	2/4/1999	1/1/2002	Mohan II	97300DOC000179027
U.S. Patent No. 5,715,376	1/30/1995	2/3/1998	Nakayama	97300DOC000179045
U.S. Patent No. 5,481,206	9/20/1994	1/2/1996	New I	97300DOC000179182
U.S. Patent No. 6,292,019	2/16/2000	9/18/2001	New II	97300DOC000179218
U.S. Patent No. 5,546,018	8/9/1995	8/13/1996	New III	97300DOC000179228
U.S. Patent No. 6,288,570	10/3/2000	9/11/2001	New IV	97300DOC000179261
U.S. Patent No. 6,396,302 B2	5/18/2001	5/28/2002	New V	97300DOC000179293

Patent / Application	Filing Date / Priority Date²	Published / Issue Date	Short Name	Starting Bates Number
U.S. Patent No. 7,248,073 B2	10/24/2006	7/24/2007	New VI	97300DOC000179344
U.S. Patent No. 6,407,576	3/2/2000	6/18/2002	Ngai	97300DOC000179396
U.S. Patent No. 5,426,378	4/20/1994	6/20/1995	Ong	97300DOC000179426
PCT Application WO 00/54411	3/10/2000	9/14/2000	Or-Bach I	97300DOC000179450
U.S. Patent No. 6,236,229	5/13/1999	5/22/2001	Or-Bach II	97300DOC000179612
U.S. Patent No. 6,331,790	9/11/2000	12/18/2001	Or-Bach III	97300DOC000179623
U.S. Patent No. 6,576,811 B2	3/12/2001	6/29/2004	Or-Bach IV	97300DOC000179718
U.S. Patent No. 6,819,136 B2	6/3/2003	10/16/2004	Or-Bach V	97300DOC000179826
U.S. Patent No. 6,323,680	3/2/2000	10/27/2001	Pederson	97300DOC000179934
U.S. Patent No. 5,898,602	1/25/1996	4/27/1999	Rothman	97300DOC000180124
U.S. Patent No. 6,198,304	2/22/2001	3/6/2001	Sasaki	97300DOC000180138
Japanese Patent Application Publication No. H10-78861A	9/3/1996	3/24/1998	Sato	97300DOC000180163 97300DOC000180168
U.S. Patent No. 5,905,385	4/1/1997	5/18/1999	Sharpe	97300DOC000180179
Japanese Patent Application Publication No. H01-106623A	10/20/1987	4/24/1989	Shibata I	97300DOC000180189 97300DOC000193056
Japanese Examined Patent Application Publication No. H06-44708B2	10/20/1987	6/8/1994	Shibata II	97300DOC000180197 97300DOC000193073

Patent / Application	Filing Date / Priority Date²	Published / Issue Date	Short Name	Starting Bates Number
U.S. Patent No. 6,353,331	7/10/2000	3/5/2002	Shimanek	97300DOC000180208
U.S. Patent No. 6,201,408	5/30/1998	3/13/2001	Skahill	97300DOC000180217
Japanese Patent Application Publication S62-288891A	6/9/1986	12/15/1987	Tanaka	97300DOC000192975
U.S. Patent No. 5,682,107	3/19/1996	10/28/1997	Tavana	97300DOC000192978
U.S. Patent No. 5,581,198	2/24/1995	12/3/1996	Trimberger I	97300DOC000180232
U.S. Patent No. 5,610,829	5/15/1996	3/11/1997	Trimberger II	97300DOC000180242
U.S. Patent No. 5,646,545	8/18/1995	7/8/1997	Trimberger III	97300DOC000180268
U.S. Patent No. 5,778,439	8/18/1995	7/7/1998	Trimberger IV	97300DOC000180357
Japanese Patent Application Publication No. H09-181598A	12/18/1995	7/11/1997	Uu	97300DOC000180442 97300DOC000180450
U.S. Patent No. 6,388,466	4/27/2001	5/14/2002	Wittig I	97300DOC000180464
U.S. Patent No. 6,150,838	2/25/1999	10/21/2000	Wittig II	97300DOC000180485
U.S. Patent No. 6,184,712	2/25/1999	2/6/2001	Wittig III	97300DOC000180527
U.S. Patent No. 6,118,300	10/24/1998	9/12/2000	Wittig IV	97300DOC000180567
U.S. Patent No. 6,400,180	5/18/2001	6/14/2002	Wittig V	97300DOC000180592
U.S. Patent No. 6,501,296	7/24/2001	12/31/2002	Wittig VI	97300DOC000180644
U.S. Patent No. 5,442,306	9/9/1994	8/15/1995	Woo I	97300DOC000180684

Patent / Application	Filing Date / Priority Date²	Published / Issue Date	Short Name	Starting Bates Number
Japanese Patent Application Publication No. H08-237109A	9/8/1995	9/13/1996	Woo II	97300DOC000180694 97300DOC000180703
Japanese Patent Application Publication No. H05-252024A	3/2/1992	9/28/1993	Yamada I	97300DOC000180722 97300DOC000180730
Japanese Patent No. 2882617B2	3/2/1992	2/5/1999	Yamada II	97300DOC000180747
U.S. Patent No. 5,920,202	4/4/1997	7/6/1999	Young I	97300DOC000180759
U.S. Patent No. 5,963,050	3/24/1997	10/5/1999	Young II	97300DOC000180771
U.S. Patent No. 6,051,992	4/1/1999	4/18/2000	Young III	97300DOC000180803
U.S. Patent No. 6,097,212	5/1/2000	10/9/1997	Agrawal IV	97300DOC000194340

(b) Table 2: Non-Patent Prior Art Publications

Description	Publication Date	Short Name	Starting Bates Number
Xilinx Inc., <i>XCELL: The Quarterly Journal For Xilinx Programmable Logic Users</i> , Issue 1 (1988)	1988	XCell No. 1	97300DOC000180815
Xilinx Inc., <i>The Programmable Gate Array Data Book</i> , Norcomp Inc. (1989)	1989	1989 Xilinx Data Book	97300DOC000180839

Description	Publication Date	Short Name	Starting Bates Number
Xilinx Inc., <i>XC3020s Break World Speed Record</i> , XCELL: The Newsletter for Programmable Gate Array Users, Issue 3 (Second/Third Quarter 1989)	1989	XCell No. 3	97300DOC000180823
Jonathan Rose et al., <i>Architecture of Field-Programmable Gate Arrays: The Effect of Logic Block Functionality on Area Efficiency</i> , IEEE Journal of Solid-State Circuits, vol. 25, no. 5, 1217-25 (Oct. 1990)	1990	Rose	97300DOC000181219
Xilinx Inc., <i>The Programmable Gate Array Data Book</i> (1991)	1991	1991 Xilinx Data Book	97300DOC000181228
Dwight Hill et al., <i>ORCA: A New Architecture for High-Performance FPGA's</i> , Field-Programmable Gate Arrays: Architectures and Tools for Rapid Prototyping: Second Int'l Workshop on Field-Programmable Logic and Applications, Vienna, Austria, Aug. 31 – Sept. 2, 1992: Selected Papers, 52-60 (1993)	1992	ORCA: A New Architecture	97300DOC000181991

Description	Publication Date	Short Name	Starting Bates Number
Jack L. Kouloheris & Abbas El Gama, PLA-Based FPGA Area Versus Cell Granularity, IEEE 1992 Custom Integrated Circuits Conference, 4.3.1 (1992)	1992	Kouloheris	97300DOC000181987
Narasimha B. Bhat & Dwight Hill, <i>Routable Technology Mapping for LUT FPGAs</i> , Proceedings 1992 IEEE International Conference on Computer Design: VLSI in Computers & Processors, 95-98 (Jan. 1992)	1992	Bhat & Hill	97300DOC000181648
Robert J. Francis, <i>A Tutorial on Logic Synthesis for Lookup-Table Based FPGA</i> , IEEE Int'l Conference Aided Design, Institute of Electrical Engineers Inc., 40-40 (Nov. 1992)	1992	Francis	97300DOC000187647
Satwant Singh et al., <i>The Effect of Logic Block Architecture on FPGA Performance</i> , IEEE Journal of Solid-State Circuits, vol. 27, no. 3, 281-87 (Mar. 1992)	1992	Singh - Effect	97300DOC000194072
Stephen D. Brown et al., <i>Field-Programmable Gate Arrays</i> (1992)	1992	Brown - FPGAs	97300DOC000181652

Description	Publication Date	Short Name	Starting Bates Number
Stephen Dean Brown, Ph.D. Thesis, <i>Routing Algorithms and Architectures for Field-Programmable Gate Arrays</i> , Department of Electrical Engineering, University of Toronto (Jan. 1992)	1992	Brown Ph.D. Thesis	97300DOC000181869
Texas Instruments Inc., <i>TICPAL22V10Z-25C, TIPCAL22V10Z-30I, EPIC CMOS Programmable Array Logic Circuits Data Sheet</i> , SRPS07C-D3323, September 1989 – Revised February 1992 (Feb. 1992)	1992	Texas Instruments Data Sheet	97300DOC000182014
Xilinx Inc., XCELL: The Newsletter for Xilinx Programmable Logic Users, Issue 7 (Second Quarter 1992)	1992	XCell No. 7	97300DOC000182036
Dwight Hill & Nam-Sung Woo, <i>The Benefits of Flexibility in Lookup Table-based FPGA's</i> , IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 12, no. 2, 349-53 (Feb. 1993)	1993	Hill & Woo	97300DOC000182431
FLEX 81188A New Product Plan, Revision 0.0 (Nov. 22, 1993)	1993	FLEX 81188A NPP	97300DOC000176226

Description	Publication Date	Short Name	Starting Bates Number
Gordan V. Hyland & Stephen D. Brown, Programmable Devices Architecture Overview Tutorial (1993)	1993	Hyland & Brown Tutorial	97300DOC000177527
Jianshe He & Jonathan Rose, <i>Advantages of Heterogeneous Logic Block Architectures for FPGAs</i> in Proceedings of IEEE Custom Integrated Circuits Conference - CICC '93 (1993)	1993	He - Advantages	97300DOC000194050
Jianshe He, Masters Thesis, <i>Technology Mapping and Architecture of Heterogeneous Field-Programmable Gate Arrays</i> , University of Toronto (1992)	1993	He Master's Thesis	97300DOC000182334
Narasimha B. Bhat et al., Performance-Oriented Fully Routable Dynamic Architecture for a Field Programmable Logic Device, Technical Report no. UCB/ERL M93/42, Electronic Research Laboratory, University of California, Berkeley (June 1993), at http://www2.eecs.berkeley.edu/Pubs/TechRpts/1993/ERL-93-42.pdf	1993	Bhat - Performance-Oriented	97300DOC000182291

Description	Publication Date	Short Name	Starting Bates Number
Narasimha B. Bhat, Novel Techniques for High Performance Field Programmable Logic Devices, Technical Report no. UCB/ERL M93/80, Electronic Research Laboratory, University of California, Berkeley (Nov. 1993), at http://www2.eecs.berkeley.edu/Pubs/TechRpts/1993/ERL-93-80.pdf	1993	Bhat - Novel Techniques	97300DOC000182060
Robert H. Krambeck et al., <i>ORCA: A High Speed, High Density FPGA Architecture</i> , Digest of Papers, Compcon Spring, IEEE, 367-72 (1993)	1993	Krambeck	97300DOC000182436
Xilinx Inc., <i>The Programmable Gate Array Data Book</i> (1993)	1993	1993 Xilinx Data Book	97300DOC000182442
Donald W. Cherepacha, Master's Thesis, <i>A Field-Programmable Gate Array Architecture Optimized for Datapaths</i> , Department of Electrical and Computer Engineering, University of Toronto (1994)	1994	Cherepacha Master's Thesis	97300DOC000183052
Stephen M. Trimberger et al., <i>Field-Programmable Gate Array Technology</i> (1994)	1994	Trimberger - FPGA Technology	97300DOC000183159

Description	Publication Date	Short Name	Starting Bates Number
Tsutomu Sasao & Jon T. Butler, <i>A Design Method for Look-up Table Type FPGA by Pseudo-Kronecker Expansion</i> , Proceedings of 24 th Int'l Symposium on Multiple-Valued Logic (ISMVL '94), IEEE, 97-106 (1994)	1994	Sasao	97300DOC000183149
Xilinx Inc., <i>The Programmable Gate Array Data Book</i> (1994)	1994	1994 Xilinx Data Book	97300DOC000183470
Xilinx Inc., <i>XCELL: The Quarterly Journal For Xilinx Programmable Logic Users</i> , Issue 15, (Fourth Quarter 1994)	1994	XCell No. 15	97300DOC000183430
Altera FLEX 10K EPF102880 New Product Plan (Jan. 18, 1995)	1995	FLEX 10K EPF102880 NPP	97300DOC000175109
Altera FLEX 10K EPF102880 New Product Plan (Jan. 18, 1995)	1995	FLEX 10K EPF102880 NPP	97300DOC000176539
Amit Chowdhary & John P. Hayes, <i>Technology Mapping for Field-Programmable Gate Arrays Using Integer Programming</i> , Proceedings of IEEE Int'l Conference on Computer-Aided Design, IEEE, 346-52 (Nov. 1995)	1995	Chowdhary & Hayes	97300DOC000184162

Description	Publication Date	Short Name	Starting Bates Number
Anthony Stansfield & Ian Page, <i>The Design of a New FPGA Architecture</i> , Int'l Workshop on Field Programmable Logic and Applications, [Springer, Berlin, Heidelberg] 1-14 (Aug. 1995)	1995	Stansfield	97300DOC000184286
AT&T Microelectronics, <i>ORCA 1C Series Field-Programmable Gate Arrays (ATTIC03, ATTIC05, ATTIC07, and ATTIC09) Data Sheet</i> (May 1995)	1995	ORCA 1C Data Sheet	97300DOC000184178
Edward Tau et al., <i>A First Generation DPGA Implementation</i> , Proceedings of the Third Canadian Workshop on Field-Programmable Devices, 138-143 (1995)	1995	Tau	97300DOC000184301
Electronic Design Automation, EDN.com, https://www.edn.com/edn-11-09-95-electronic-design-automation/ (Nov. 9, 1995)	1995	EDN - Electronic Design Automation	97300DOC000184169
Xilinx, Inc., 17 XCell 15 (1995)	1995	XCell No. 17	97300DOC000184375
Xilinx, Inc., 18 XCell 18 (1995)	1995	XCell No. 18	97300DOC000184407
Xilinx, Inc., XC4000E Field Programmable Gate Arrays: Preliminary Product Specifications (Sept. 14, 1995)	1995	XC4000E Preliminary Product Specification	97300DOC000184307

Description	Publication Date	Short Name	Starting Bates Number
Actel Corporation, <i>ACT 1 Series FPGAs</i> (datasheet), 1-283 - 1-306 (Apr. 1996)	1996	1996 ACT 1 Series FPGAs	97300DOC000184447
Alireza Kaviani & Stephen Brown, "Hybrid FPGA Architecture," Fourth Int'l ACM Symposium on Field-Programmable Gate Arrays (1996)	1996	Kaviani	97300DOC000184539
Altera Announces Faster Speed Grades for All FLEX 10K Family Devices, EETimes, https://www.eetimes.com/altera-announces-faster-speed-grades-for-all-flex-10k-family-devices/ (Sept. 16, 1996)	1996	EETimes - Altera Announces Faster Speed	97300DOC000184528
Botticelli New Product Plan Z1179A, Revision 1.0 (Oct. 11, 1996)	1996	Botticelli NPP	97300DOC000177407
Don Cherepacha & David Lewis, <i>DP-FPGA: An FPGA Architecture Optimized for Datapaths</i> , VLSI Design, vol. 4, no. 4, 329-43 (1996)	1996	Cherepacha & Lewis	97300DOC000184512
Field-Programmable Gate Arrays - Data Book, Lucent Technologies Microelectronics Group (Oct. 1996)	1996	Lucent FPGA Data Book	97300DOC000184546

Description	Publication Date	Short Name	Starting Bates Number
Fujii Koji & Urano Masami, <i>A Study on Logic Block with Variable Number of Inputs in FPGA</i> , Proceedings of the 1996 IEICE General, IEICE Corp. (Mar. 1996)	1996	Fujii - Study on Logic Block (JP)	97300DOC000184532 97300DOC000184537
Gate Array vs. Programmable Logic Cost Analysis, Altera White Paper v2.0 (Oct. 1996)	1996	Altera White Paper on Cost Analysis	97300DOC000177948
MicroSim Teams Up with FPGA Pioneer Xilinx, EETimes, https://www.eetimes.com/microsim-teams-up-with-fpga-pioneer-xilinx/ (Dec. 24, 1996)	1996	EETimes - MicroSim Teams Up with Xilinx	97300DOC000184530
Srinivas Reddy et al., <i>A High Density Embedded Array Programmable Logic Architecture</i> , Proceedings of Custom Integrated Circuits Conference, IEEE, 251-54 (May 1996)	1996	Reddy	97300DOC000185298
Stephen Brown & Jonathan Rose, <i>FPGA and CPLD Architectures: A Tutorial</i> , IEEE Design and Test of Computers, vol. 13, no. 2, 42-57 (Dec. 1996)	1996	Brown & Rose	97300DOC000194034

Description	Publication Date	Short Name	Starting Bates Number
Takayuki Suyama et al., <i>LUT-based FPGA Technology Mapping using Permissible Functions</i> , Proceedings of 9 th Int'l Conference on VLSI Design, IEEE, 215-18 (Jan. 1996)	1996	Suyama	97300DOC000185302
Xilinx Inc., <i>The Programmable Gate Array Data Book</i> (1996)	1996	1996 Xilinx Data Book	97300DOC000185316
Xilinx, Inc., Using Dedicated Carry Logic in XC4000E (July 4, 1996)	1996	XC4000E Dedicated Carry Logic	97300DOC000185306
Akihisa Ohta et al., <i>Full Custom Design for Bit Serial FPGA</i> , Information Processing Society of Japan, Research Report System LSI Design Technology, 121-28 (1997-SLDM-085) (Oct. 1997)	1997	Ohta	97300DOC000186502
Amit Chowdhary & John P. Hayes, <i>General Modeling and Technology-Mapping Technique for LUT-based FPGAs</i> , Proceedings of the 1997 ACM 5 th Int'l Symposium on Field-Programmable Gate Arrays, 43-49 (Feb. 1997)	1997	Chowdhary - General Modeling	97300DOC000186309
Amit Chowdhary, Ph.D. Thesis, Technology Mapping for Field-Programmable Gate Arrays, University of Michigan (1997)	1997	Chowdhary Ph.D. Thesis	97300DOC000186319

Description	Publication Date	Short Name	Starting Bates Number
da Vinci (APEX 20K400) Design Review 1 (Dec. 17, 1998)	1997	APEX 20K400 Design Review	97300DOC000177852
da Vinci (APEX 20K400) New Product Plan Z1200A, Revision 0.0 (Dec. 9, 1997)	1997	1997 APEX 20K400 NPP	97300DOC000177698
Exemplar Announces Support for Xilinx XC4000EX Family, EETimes (Apr. 2, 1997)	1997	EETimes - Exemplar Support for Xilinx	97300DOC000186480
Julio Faura et al., A Novel Mixed Signal Programmable Device with On-Chip Microprocessor, Proceedings of CICC 97 - Custom Integrated Circuits Conference, 103-106 (1997), at https://ieeexplore.ieee.org/document/606594	1997	Faura - Novel Mixed Signal	97300DOC000186488
Julio Faura et al., Reconfiguration and Real-Time Probing on a Novel Mixed Signal Programmable Device with On-Chip Microprocessor, Field-Programmable Logic and Applications (W. Luk et al. eds.), 1-10 (1997) at https://link.springer.com/chapter/10.1007/3-540-63465-7_205	1997	Faura - Reconfiguration	97300DOC000186492
Lucent Technologies, <i>ATT3000 Series Field-Programmable Gate Arrays Data Sheet</i> (Feb. 1997)	1997	ATT3000 Data Sheet	97300DOC000186225

Description	Publication Date	Short Name	Starting Bates Number
Lucent Technologies, <i>ORCA OR3Cxxx/OR3Txxx Series Field-Programmable Gate Arrays Preliminary Product Brief</i> (Nov. 1997)	1997	ORCA 3 Preliminary Product Brief	97300DOC000186510
Vaughn Betz & Jonathan Rose, <i>Cluster-Based Logic Blocks for FPGAs: Area Efficiency vs. Input Sharing and Size</i> , Proceedings of CICC 97 - Custom Integrated Circuits Conference, IEEE, 551-54 (May 1997)	1997	Betz - Cluster-Based Logic Blocks	97300DOC000186305
Wayback Machine capture of "About Altera Devices," http://www.altera.com/html/products/products.html#flex (June 5, 1997)	1997	Wayback About Altera Devices	97300DOC000186524
Wayback Machine capture of "About Microelectronics," Lucent Technologies, http://www.lucent.com/micro/fpga/info.html (June 16, 1997)	1997	Wayback Lucent About Microelectronics	97300DOC000186527
Wayback Machine capture of "FPGA Product Literature," http://www.xilinx.com/products/fpgaspec.htm (June 16, 1997)	1997	1997 Wayback Xilinx FPGA Product Literature	97300DOC000186532

Description	Publication Date	Short Name	Starting Bates Number
Wayback Machine capture of "Microelectronics Field-Programmable Gate Arrays - Documentation & Application Notes," http://www.lucent.com/micro/fpga/docs.html#prodbrief (June 15, 1997)	1997	Wayback Lucent Microelectronics FPGAs	97300DOC000186530
Xilinx FPGA Roadmap Points to Die Size Parity with Gate Arrays by End of Year, EETimes, https://www.eetimes.com/xilinx-fpga-roadmap-points-to-die-size-parity-with-gate-arrays-by-end-of-year/ (June 23, 1997)	1997	EETimes - Xilinx FPGA Roadmap	97300DOC000186482
Xilinx Introduces Fully Programmable Alternative to System-Level ASIC Design, EETimes, https://www.eetimes.com/xilinx-introduces-fully-programmable-alternative-to-system-level-asic-design/ (Nov. 25, 1997)	1997	EETimes - Xilinx Introduces Virtex	97300DOC000186484
Xilinx Lowers the Cost of XC3000 Performance, EETimes, https://www.eetimes.com/xilinx-lowers-the-cost-of-xc3000-performance/ (Mar. 3, 1997)	1997	EETimes - Xilinx Lowers Cost of XC3000	97300DOC000186486
Xilinx, Inc., Block Adaptive Filter (Jan. 9, 1997)	1997	XC4000E/X Block Adaptive Filter	97300DOC000186534

Description	Publication Date	Short Name	Starting Bates Number
Yuichiro Shibata, et al., HOSMII: a Virtual Hardware System Based on an FPGA Embedded with DRAM (1997)	1997	Shibata - HOSMII	97300DOC000186518
Ali Sheikholeslami et al., <i>Look-Up Tables (LUTs) for Multiple-Valued, Combinational Logic</i> , Proceedings, 1998 28 th IEEE Int'l Symposium on Multiple-Valued Logic (Cat. No. 98CB36138) IEEE, 264-69 (May 1998)	1998	Sheikholeslami	97300DOC000186734
Altera Data Book (Jan. 1998)	1998	Altera Data Book	97300DOC000175312
da Vinci (APEX 20K400) New Product Plan Z1200A, Revision 1.0 (June 25, 1998)	1998	1998 APEX 20K400 NPP	97300DOC000176943
Earnings RoundUp: New Product Intros Boost Sales for Xilinx, EETimes, https://www.eetimes.com/earnings-roundupnew-product-intros-boost-sales-for-xilinx/ (Oct. 21, 1998)	1998	EETimes - Xilinx Earnings RoundUp	97300DOC000186563
FLEX 10K Data Sheet v3.11 (May 1998)	1998	1998 FLEX 10K Data Sheet	97300DOC000186565
FLEX 10K50E (Z1221A) New Product Plan, Revision 1.0 (June 1998)	1998	FLEX 10K50E NPP	97300DOC000176343

Description	Publication Date	Short Name	Starting Bates Number
Lucent Technologies Combines FPGA, Standard-Cell Logic on Single Silicon Chip for High Performance, Flexibility, EDN.com, https://www.edn.com/lucent-technologies-combines-fpga-standard-cell-logic-on-single-silicon-chip-for-high-performance-flexibility/ (May 13, 1998)	1998	EDN - Lucent Combines FPGA, Standard-Cell Logic	97300DOC000186556
Masahiro Iida et al., <i>On Chip Multi-Processor with Hardwired Thread Controller</i> , Information Processing Society of Japan, vol. 39, no. 6, 1613-621 (June 1998)	1998	Iida - On Chip	97300DOC000186715
Michel Renovell et al., <i>SRAM-Based FPGA's: Testing the LUT/RAM Modules</i> , Proceedings Int'l Test Conference 1998 (IEEE Cat. No. 98CH36270) 1102-11 (Oct. 1998)	1998	Renovell	97300DOC000186724
Scott Hauk, <i>The Roles of FPGAs in Reprogrammable Systems</i> , Proceedings of the IEEE, vol. 86, no. 4, 615-38, (Apr. 1998)	1998	Hauk	97300DOC000186679

Description	Publication Date	Short Name	Starting Bates Number
Steve Trimberger, <i>Scheduling Designs into a Time-Multiplexed FPGA</i> , Proceedings of the 1998 ACM/SIGDA 6 th Int'l Symposium on Field Programmable Gate Arrays, 153-60 (Mar. 1998)	1998	Trimberger - Scheduling Designs	97300DOC000186740
Vaughn Betz & Jonathan Rose, <i>How Much Logic Should Go in an FPGA Logic Block</i> , Design & Test of Computers, IEEE, vol. 15, no. 1, 10-15 (Jan. 1998)	1998	Betz & Rose	97300DOC000186544
Wayback Machine capture of "FPGA Product Literature," http://www.xilinx.com:80/products/fpgaspec.htm (Feb. 10, 1998)	1998	1998 Wayback Xilinx FPGA Product Literature	97300DOC000186750
Wayback Machine capture of "Lucent Technologies' New 0.25-micron FPGA's Deliver the Speed Needed for Advanced Applications," Lucent Technologies News Release, http://www.lucent.com/micro/NEWS/012698a.html (Jan. 26, 1998)	1998	Wayback Lucent News Release	97300DOC000186748
Xilinx Inc., <i>The Programmable Logic Data Book</i> (Apr. 1998)	1998	1998 Xilinx Data Book	97300DOC000186752

Description	Publication Date	Short Name	Starting Bates Number
Xilinx Inc., XCELL: The Quarterly Journal For Xilinx Programmable Logic Users, Issue 27 (First Quarter 1998)	1998	XCell No. 27	97300DOC000187504
Xilinx, Inc., Xilinx FPGAs: A Technical Overview for the First-Time User (Dec. 12, 1998)	1998	1998 Xilinx Technical Overview	97300DOC000187502
Altera APEX 20K400E New Product Plan Z1236A, Revision 1.0 (Sept. 15, 1999)	1999	1999 APEX 20K400E NPP	97300DOC000177117
Altera Introduction v6 (May 1999)	1999	Altera Introduction	97300DOC000187546
Altera Ships Apex 20K, EDN.com (Apr. 20, 1999), https://www.edn.com/altera-ships-apex-20k/	1999	EDN - Altera Ships Apex 20K	97300DOC000187638
Altera Ships Apex 20K, EETimes (Apr. 20, 1999)	1999	EETimes - Altera Ships Apex 20K	97300DOC000187645
APEX 20K Programmable Logic Device Family, Data Sheet v2.01 (Aug. 1999)	1999	1999 APEX 20K Data Sheet	97300DOC000187566
APEX 20K400 New Product Plan Z1200A, Revision 2.0 (Jan. 18, 1999)	1999	1999 APEX 20K400 NPP	97300DOC000176753
APEX 20K400 New Product Plan Z1200A Revision 2.0 (Jan. 18, 1999)	1999	1999 APEX 20K400 NPP	97300DOC000192421

Description	Publication Date	Short Name	Starting Bates Number
Jason P. Clifford & Steven J.E. Wilton, <i>Architecture of Cluster-based FPGAs with Memory</i> , Proceedings of the IEEE 2000 Custom Integrated Circuits Conference (Cat. no. 00CH37044), IEEE, 131-34 (May 1999)	1999	Clifford	97300DOC000187634
Katsuto Nakajima et al., <i>Overview of FPGA-based Parallel Machine RASH</i> , Proceedings of the Information Processing Society of Japan, 58th National Convention, 141-42 (1999)	1999	Nakajima	97300DOC000191051
Lucent Technologies, <i>ORCA Series 2 Field-Programmable Gate Arrays Data Sheet</i> (June 1999)	1999	ORCA 2 Data Sheet	97300DOC000187655
Lucent Technologies, <i>ORCA Series 2 Field-Programmable Gate Arrays Product Brief</i> (Apr. 1999)	1999	ORCA 2 Product Brief	97300DOC000187847
Lucent Technologies, <i>ORCA Series 3C and 3T Field-Programmable Gate Arrays Data Sheet</i> (June 1999)	1999	ORCA 3 Data Sheet	97300DOC000187853
Lucent Technologies, <i>ORCA Series 3C and 3T Field-Programmable Gate Arrays Product Brief</i> (Apr. 1999)	1999	ORCA 3 Product Brief	97300DOC000188063

Description	Publication Date	Short Name	Starting Bates Number
Om Agrawal et al., <i>An Innovative, Segmented High Performance FPGA Family with Variable-Grain-Architecture and Wide-gating Functions</i> , Proceedings of the 1999 ACM/SIGDA 7 th Int'l Symposium on Field Programmable Gate Arrays, 17-26 (Feb. 1999)	1999	Agrawal - Innovative	97300DOC000187536
Toshinori Sueyoshi & Masahiro Iida, <i>Reconfigurable Computing</i> , IPSJ Magazine, vol. 40, no. 8, 777-82 (Aug. 1999)	1999	1999 Sueyoshi & Iida	97300DOC000188083
Xilinx Inc., <i>Libraries Guide</i> (1999)	1999	1999 Xilinx Libraries Guide	97300DOC000189279
Xilinx Inc., <i>The Programmable Logic Data Book</i> (1999)	1999	1999 Xilinx Data Book	97300DOC000188238
Xilinx, Inc., <i>Designing Flexible, Fast CAMs with Virtex Family FPGAs</i> (1999)	1999	Virtex Designing CAMs	97300DOC000188089
Xilinx, Inc., <i>XC4000E and XC4000X Series Field Programmable Gate Arrays: Product Specification</i> (May 14, 1999)	1999	XC4000E/X Product Specification	97300DOC000188106
Xilinx, <i>XCELL: The Quarterly Journal for Programmable Logic Users</i> , no. 31 (First Quarter 1999)	1999	XCell No. 31	97300DOC000188174

Description	Publication Date	Short Name	Starting Bates Number
Yuichiro Shibata, et al, A Data Driven Virtual Hardware Using an FPGA Integrated with DRAM	1999	Shibata - Data Driven	97300DOC000188071
Amit Singh et al., <i>A Novel High Throughput Reconfigurable FPGA Architecture</i> , Proceedings of the 2000 ACM/SIGDA 8 th Int'l Symposium on Field Programmable Gate Arrays, 22-29 (2000)	2000	Singh - Novel	97300DOC000191053
APEX 20K400F (APEX II) New Product Plan Z1313A rev0.0 Table of Contents (Aug. 4, 2000)	2000	APEX II NPP TOC	97300DOC000192923
APEX 20K400F (APEX II) New Product Plan Ch. 1	2000	APEX II NPP Ch. 1	97300DOC000192616
APEX 20K400F (APEX II) New Product Plan Ch. 2	2000	APEX II NPP Ch. 2	97300DOC000192703
APEX 20K400F (APEX II) New Product Plan Ch. 3	2000	APEX II NPP Ch. 3	97300DOC000192704
APEX 20K400F (APEX II) New Product Plan Ch. 4	2000	APEX II NPP Ch. 4	97300DOC000192755
APEX 20K400F (APEX II) New Product Plan Ch. 5	2000	APEX II NPP Ch. 5	97300DOC000192809
APEX 20K400F (APEX II) New Product Plan Ch. 6	2000	APEX II NPP Ch. 6	97300DOC000192820
APEX 20K400F (APEX II) New Product Plan Ch. 7	2000	APEX II NPP Ch. 7	97300DOC000192827
APEX 20K400F (APEX II) New Product Plan Ch. 8	2000	APEX II NPP Ch. 8	97300DOC000192858
APEX 20K400F (APEX II) New Product Plan Ch. 9	2000	APEX II NPP Ch. 9	97300DOC000192872

Description	Publication Date	Short Name	Starting Bates Number
APEX 20K400F (APEX II) New Product Plan Ch. 10	2000	APEX II NPP Ch. 10	97300DOC000192618
APEX 20K400F (APEX II) New Product Plan Ch. 11	2000	APEX II NPP Ch. 11	97300DOC000192661
APEX 20K400F (APEX II) New Product Plan Ch. 12	2000	APEX II NPP Ch. 12	97300DOC000192678
APEX 20K400F (APEX II) New Product Plan Ch. 13	2000	APEX II NPP Ch. 13	97300DOC000192701
APEX 20K400F (APEX II) New Product Plan Appendix A	2000	APEX II NPP App'x A	97300DOC000192609
APEX 20K400F (APEX II) New Product Plan Update	2000	APEX II NPP Update	97300DOC000192920
Elias Ahmed & Jonathan Rose, <i>The Effect of LUT and Cluster Size on Deep-Submicron FPGA Performance and Density</i> , Proceedings of the 2000 ACM/SIGDA 8 th Int'l Symposium on Field Programmable Gate Arrays, 3-12 (Feb. 2000)	2000	Ahmed	97300DOC000190113

Description	Publication Date	Short Name	Starting Bates Number
<i>Field Programmable Logic and Applications: The Roadmap to Reconfigurable Computing</i> , 10th Int'l Conference, FPL 2000, Villach, Austria, August 2000 Proceedings (R.W. Hartenstein & H. Grunbacher eds., 2000)	2000	Hartenstein	97300DOC000190163
Hiroai Asami et al., <i>Improvement of DES Circuit on FPGA-Based Parallel Machine RASH</i> , IECE Technical Report, 117-24 (Jan. 2000)	2000	Asami - DES Circuit	97300DOC000190123
Hiroai Asami et al., <i>Improvement of DES Key Search of FPGA-based Parallel Machine RASH</i> , <i>Information Processing Society of Japan: High Performance Computing</i> , vol. 41, no. SIG 5(HPS 1), 50-57 (Aug. 2000)	2000	Asami - DES Key Search	97300DOC000190131
Jason Cong & Kenneth Yen, <i>Synthesis for FPGAs with Embedded Memory Blocks</i> , Proceedings of the 2000 ACM/SIGDA 8 th Int'l Symposium on Field Programmable Gate Arrays, 75-82 (Feb. 2000)	2000	Cong - Synthesis	97300DOC000190139

Description	Publication Date	Short Name	Starting Bates Number
Jason Cong et al., <i>Technology Mapping For k/m-Macrocell Based FPGAs</i> , Proceedings of the 2000 ACM/SIGDA 8th Int'l Symposium on Field Programmable Gate Arrays, 51-59 (Feb. 2000)	2000	Cong - Technology Mapping	97300DOC000190147
Katsumi Takahashi et al., <i>Time-Memory Trade-Off Cryptanalysis on FPGA-based Parallel Machine RASH</i> , Proceedings 4 th Int'l Conference/Exhibition on High Performance Computing in the Asia-Pacific Region, IEEE, vol. 1, 366-69 (May 2000)	2000	Takahashi	97300DOC000191061
Lucent Technologies, EDN.com, https://www.edn.com/lucen-t-technologies/ (Aug. 17, 2000)	2000	EDN - Lucent	97300DOC000190156
Masahiro Iida & Toshinori Sueyoshi, <i>LUT Granularity Evaluation for Reconfigurable Logic</i> , The Institute of Electronics, Information and Communication Engineers, 77-82 (2000)	2000	Iida - LUT Granularity	97300DOC000191045
Wayback Machine capture of "APEX Device Family," www.altera.com/html/products/apex.html (Mar. 3, 2000)	2000	Wayback APEX Device Family	97300DOC000191189

Description	Publication Date	Short Name	Starting Bates Number
Wayback Machine capture of “On-Line Literature: APEX 20K Devices,” www.altera.com:80/html/literature/la20k.html (Feb. 29, 2000)	2000	Wayback Altera On-Line Literature	97300DOC000191187
Xilinx Inc., <i>The Programmable Logic Data Book</i> (2000)	2000	2000 Xilinx Data Book	97300DOC000191383
Xilinx Virtex 2.5V Field Programmable Gate Arrays, Final Product Specification v2.2 (May 23, 2000)	2000	Virtex Product Specification	97300DOC000191115
Xilinx, Inc., Linear Feedback Shift Registers in Virtex Devices (2000)	2000	Virtex LSFR	97300DOC000191110
Xilinx, Inc., Virtex Series Configuration Architecture User Guide (2000)	2000	Virtex Configuration Architecture	97300DOC000191065
Xilinx, XCELL: The Quarterly Journal for Programmable Logic Users, no. 35 (2000)	2000	XCell No. 35	97300DOC000191193
Xilinx, XCELL: The Quarterly Journal for Programmable Logic Users, no. 36 (2000)	2000	XCell No. 36	97300DOC000191256
Xilinx, XCELL: The Quarterly Journal for Programmable Logic Users, no. 37 (Fall 2000)	2000	XCell No. 37	97300DOC000191319
Altera APEX 20KC Programmable Logic Device, Data Sheet v1.1 (Apr. 2001)	2001	2001 APEX 20KC Data Sheet	97300DOC000191837

Description	Publication Date	Short Name	Starting Bates Number
Altera Introduces APEX II Family, EETimes (Apr. 23, 2001), https://www.eetimes.com/altera-introduces-apex-ii-family/	2001	EETimes - Altera Introduces APEX II	97300DOC000191947
Altera Revenue Falls 25%, But Earnings Beat Expectations, EDN.com (July 23, 2001), https://www.edn.com/altera-revenue-falls-25-but-earnings-beat-expectations/	2001	EDN - Altera Revenue Falls	97300DOC000191941
APEX Devices Brochure (Jan. 2001)	2001	APEX Devices Brochure	97300DOC000191927
Hiroai Asami et al., <i>The Applicability of Synthetic Aperture Radar Processing on a FPGA-based Parallel Machine RASH</i> , Information Processing Society of Japan, 19-24 (2001)	2001	Asami - Applicability	97300DOC000191935
Hue-Sung Kim, Ph.D. Thesis, <i>Towards Adaptive Balanced Computing (ABCs) Using Reconfigurable Functional Caches (RFCs)</i> , Iowa State University (2001)	2001	Kim Ph.D. Thesis	97300DOC000191956
Masahiro Iida & Toshinori Sueyoshi, <i>Proposal of a Logic Block Architecture for Reconfigurable Logic</i> , Information Processing Society of Japan, 141-46 (Nov. 2001)	2001	2001 Iida - Logic Block Architecture	97300DOC000191950

Description	Publication Date	Short Name	Starting Bates Number
Wayback Machine capture of “APEX II Devices: The Next-Generation APEX SOPC,” http://www.altera.com/products/devices/apex2/ap2-index.html (May 1, 2001)	2001	2001 Wayback APEX II Devices	97300DOC000192088
Wayback Machine capture of APEX II: The Complete I/O Solution, http://www.altera.com/literature/br/br_ap2.pdf (June 13, 2001)	2001	2001 Wayback APEX II: The Complete IO Solution	97300DOC000192090
Xilinx Inc., <i>XCELL: The Authoritative Journal for Programmable Logic Users, Special Edition - Virtex - II Platform FPGA</i> , Issue 40 (2001)	2001	XCell No. 40	97300DOC000192098
Amit Chowdhary & John P. Hayes, <i>General Technology Mapping for Field-Programmable Gate Arrays Based on Lookup Tables</i> , ACM Transactions on Design Automation of Electronic Systems, vol. 7, no. 1, 1-32 (Jan. 2002) at, https://www.researchgate.net/publication/220305957	2002	Chowdhary & Hayes - General Technology Mapping	97300DOC000192198

Description	Publication Date	Short Name	Starting Bates Number
Masahiro Iida & Toshinori Sueyoshi, <i>A Proposal of Programmable Logic Architecture for Reconfigurable Computing</i> , Proceedings of the IEEK Conference, The Institute of Electronics and Information Engineers, 1457-1550 (Jul. 2002)	2002	2002 Iida & Sueyoshi	97300DOC000192241
Masahiro Iida & Toshinori Sueyoshi, <i>Proposal and Evaluation of a Logic Block Architecture for Reconfigurable Logic</i> , Information Processing Society of Japan, vol. 43, no. 5, 1181-90 (May 2002)	2002	2002 Iida - Logic Block Architecture	97300DOC000192231
Masahiro Iida, Ph.D. Thesis, <i>Research on Reconfigurable Computing</i> , Kumamoto University Graduate School of Science and Technology (Mar. 2002)	2002	Iida Ph.D. Thesis	97300DOC000192245
Toshinori Sueyoshi & Masahiro Iida, <i>Configurable and Reconfigurable Computing for Digital Signal Processing</i> , IEICE Transactions on Fundamentals, vol. E85-A, No.3, 591-99 (Mar. 2002)	2002	2002 Sueyoshi - Configurable	97300DOC000192372
Nov. 7, 2022 eBay Order of Devices (PII Redacted)	N/A	eBay Order 2022-11-07	97300DOC000192381
Nov. 11, 2022 eBay Order of Device (PII Redacted)	N/A	eBay Order 2022-11-10	97300DOC000192383

Description	Publication Date	Short Name	Starting Bates Number
Altera EP20K100EFC324-2N eBay Listing	N/A	eBay Altera EP20K100EFC324-2N	97300DOC000192392
Altera EPF10K50VBC356-2 eBay Listing	N/A	eBay Altera EPF10K50VBC356-2	97300DOC000192395
Altera EPF8282ATC100-2 eBay Listing	N/A	eBay Altera EPF8282ATC100-2	97300DOC000192398
AT&T ATT3030-70M68 eBay Listing	N/A	eBay AT&T ATT3030-70M68	97300DOC000192384
AT&T OR3T80-6BA352 eBay Listing	N/A	eBay AT&T OR3T80-6BA352	97300DOC000192401
Xilinx XC2018-70PC84C eBay Listing	N/A	eBay Xilinx XC2018-70PC84C	97300DOC000192406
Xilinx XC3090A-PC84BKJ eBay Listing	N/A	eBay Xilinx XC3090A-PC84BKJ	97300DOC000192409
Xilinx XC4005E-4PQ160C eBay Listing	N/A	eBay Xilinx XC4005E-4PQ160C	97300DOC000192412
Xilinx XC5210P-Q208AKM eBay Listing	N/A	eBay Xilinx XC5210P-Q208AKM	97300DOC000192415
Xilinx XCV50-6FG256 eBay Listing	N/A	eBay Xilinx XCV50-6FG256	97300DOC000192418
Ashok K. Sharma, Programmable Logic Handbook: PLDs, CPLDs, and FPGAs (1998 McGraw-Hill)	1998	Sharma	97300DOC000193584
Vaughn Betz et al., Architecture and CAD for Deep-Submicron FPGAs (1999 Kluwer Academic Publishers)	1999	Betz	97300DOC000194079

Description	Publication Date	Short Name	Starting Bates Number
Jonathan Rose et al., <i>Architecture of Field-Programmable Gate Arrays</i> , Proceedings of the IEEE, vol. 81, no. 7 (July 1993)	1993	Rose - Architecture	97300DOC000194055

(c) Table 3: Prior Art Products and Systems³

Name	Developer, Provider, or Manufacturer⁴	Short Name	Use, Knowledge, Sold, or Offered Date⁵
FLEX 8000 Family of Programmable Logic Devices	Altera Corporation	FLEX 8000	1997
FLEX 10K Family of Programmable Logic Devices	Altera Corporation	FLEX 10K	1998
APEX 20K Family of Programmable Logic Devices	Altera Corporation	APEX 20K	1999
ATT3000 Series Product	AT&T Microelectronics / Lucent Technologies	ATT3000	1996
Microelectronics Optimized Reconfigurable Cell Array (ORCA) Series Product	AT&T Microelectronics / Lucent Technologies	ORCA	1995
Virtex Family of Programmable Logic Devices	Xilinx, Inc.	Virtex	1999
XC2000 Family of Programmable Logic Devices	Xilinx, Inc.	XC2000	1988

³ Documents and things relied on as evidence of the prior art products and systems are cited in the corresponding claim charts.

⁴ Including all relevant affiliates and/or successors in interest.

⁵ These products were used, known, sold, or offered for sale at least as of this date. Intel reserves the right to revise these dates in light of additional discovery from the parties or third parties.

Name	Developer, Provider, or Manufacturer ⁴	Short Name	Use, Knowledge, Sold, or Offered Date ⁵
Xilinx, Inc. XC3000 Family of Programmable Logic Devices	Xilinx, Inc.	XC3000	1988
Xilinx, Inc. XC4000 Family of Programmable Logic Devices	Xilinx, Inc.	XC4000	1992
Xilinx, Inc. XC5200 Family of Programmable Logic Devices	Xilinx, Inc.	XC5200	1995

2. Admitted Prior Art

The Asserted Patent, in its specification, contains statements admitting that certain claim limitations were already known in the art at the time of the purported invention. Such admissions “are binding on the patentee for purposes of a later inquiry into obviousness.” *PharmaStem Therapeutics, Inc. v. ViaCell, Inc.*, 491 F.3d 1342, 1362 (Fed. Cir. 2007); *see also Constant v. Advanced Micro-Devices, Inc.*, 848 F.2d 1560, 1570 (Fed. Cir. 1988) (same as to anticipation). The following list of examples of admitted prior art for the Asserted Patent is illustrative and not exhaustive. References cited as admitted prior art in the Asserted Patent are incorporated herein by reference.

- Look up table of M inputs and N outputs
 - “Recently, a programmable logic circuit device has attracted much attention as a device that can realize various logic circuits which meets diverse needs of users by programming internal circuits. Such a programmable logic circuit device is known as PLD (Programmable Logic Device) or FPGA (Field Programmable Gate Array), and recently is increasingly used not only for trial fabrication of hardwares, but also for constructing a large scale circuit (for example, a microprocessor) that has various functions in itself. These programmable logic

circuits comprise look up tables (LUT: Look Up Table) as major components, and reduction of circuit area of such LUTs is strongly desired.” ’737 patent at 1:13–24.

- “A look up table (LUT) as a major component of a programmable logic circuit device (PLD or FPGA) is composed of memories, and is capable of implementing an arbitrary logic circuit.” ’737 patent at 1:25–28.
- “In a programmable logic circuit device, the number of bits M of input signal for the logic circuit that can be implemented corresponds to the number of bits of the address of memory composing the LUT, and the number of bits N of output signal corresponds to the number of output bits of the memory. Thus, a logic circuit that can be implemented in one LUT is an arbitrary logic circuit of M inputs and N outputs. Such a LUT is denoted in the present specification as M -input N -output LUT.” ’737 patent at 1:46–54.
- “Conventionally, in FPGA for example, the input number M and output number N are both fixed value. Any logic circuit is divided in circuit unit of M inputs and N outputs, and is implemented using plural LUTs.” ’737 patent at 1:55–58.
- LUT units
 - “Multi-context and cluster architecture of plural LUTs in FPGA has been disclosed, for example, in U.S. Pat. Nos. 5,778,439 and 5,905,385, etc.” ’737 patent at 1:30–32.
 - “Conventionally, in FPGA for example, the input number M and output number N are both fixed value. Any logic circuit is divided in circuit unit of M inputs and N outputs, and is implemented using plural LUTs.” ’737 patent at 1:55–58.

- Programmable logic circuit device, comprising: a plurality of logic blocks; a plurality of routing wires connected to each of said logic blocks; a plurality of switch circuits provided at an intersection of each of said routing wires; a plurality of connection blocks provided between an I/O line of each of said logic blocks and each of said routing wires; and an I/O block performing an input/output operation with external equipment
 - “Recently, a programmable logic circuit device has attracted much attention as a device that can realize various logic circuits which meets diverse needs of users by programming internal circuits. Such a programmable logic circuit device is known as PLD (Programmable Logic Device) or FPGA (Field Programmable Gate Array), and recently is increasingly used not only for trial fabrication of hardwares, but also for constructing a large scale circuit (for example, a microprocessor) that has various functions in itself. These programmable logic circuits comprise look up tables (LUT: Look Up Table) as major components, and reduction of circuit area of such LUTs is strongly desired.” ’737 patent at 1:13–24.
 - “Basic architecture of such a FPGA has been previously disclosed, for example, in U.S. Pat. Nos. 4,706,216, and 4,870,302.” ’737 patent at 1:28–30.
 - “FIG. 1 is a block diagram showing an example of FPGA to which the present invention is applied. In FIG. 1, reference numeral 100 denotes FPGA as an example of a programmable logic circuit device, 101 is an I/O block, 102 is a logic block (CLB: Configurable Logic Block), 103 is a connection block (C), 104 is a switch matrix (S), and 105 denotes routing wires.” ’737 patent at 3:54–60.

- “As shown in FIG. 1, FPGA 100 is comprised of logic blocks (CLB) 102 arranged in the form of array, routing wire (channel area) 105 surrounding these CLB 102, and I/O blocks 101. At the intersection of the routing wire 105, switch matrices (S) 104 are disposed for connecting these components, and connection block (C) 103 is disposed between the I/O line of each CLB 102 and the routing wire 105. Each CLB 102 is comprised of a look up table (LUT) 121, latches 122, and selectors 123. The present invention relates mainly to the configuration of LUT 121.” ’737 patent at 3:61–4:3.
- Logic blocks each having a look up table
 - “Recently, a programmable logic circuit device has attracted much attention as a device that can realize various logic circuits which meets diverse needs of users by programming internal circuits. Such a programmable logic circuit device is known as PLD (Programmable Logic Device) or FPGA (Field Programmable Gate Array), and recently is increasingly used not only for trial fabrication of hardwares, but also for constructing a large scale circuit (for example, a microprocessor) that has various functions in itself. These programmable logic circuits comprise look up tables (LUT: Look Up Table) as major components, and reduction of circuit area of such LUTs is strongly desired.” ’737 patent at 1:13–24.
 - “A look up table (LUT) as a major component of a programmable logic circuit device (PLD or FPGA) is composed of memories, and is capable of implementing an arbitrary logic circuit.” ’737 patent at 1:25–28.

- “Basic architecture of such a FPGA has been previously disclosed, for example, in U.S. Pat. Nos. 4,706,216, and 4,870,302.” ’737 patent at 1:28–30.
- “Multi-context and cluster architecture of plural LUTs in FPGA has been disclosed, for example, in U.S. Pat. Nos. 5,778,439 and 5,905,385, etc.” ’737 patent at 1:30–32.
- “As shown in FIG. 1, FPGA 100 is comprised of logic blocks (CLB) 102 arranged in the form of array, routing wire (channel area) 105 surrounding these CLB 102, and I/O blocks 101. At the intersection of the routing wire 105, switch matrices (S) 104 are disposed for connecting these components, and connection block (C) 103 is disposed between the I/O line of each CLB 102 and the routing wire 105. Each CLB 102 is comprised of a look up table (LUT) 121, latches 122, and selectors 123. The present invention relates mainly to the configuration of LUT 121.” ’737 patent at 3:61–4:3.

3. Obviousness

In *KSR*, the Supreme Court emphasized that an idea that is the result of ordinary innovation, ordinary skill, or common sense should not be patentable. *See KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398 (2007). The Supreme Court held that a person of ordinary skill in the art is “a person of ordinary creativity, not an automaton” and “in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle.” *Id.* at 420–21. Although a patent challenger is not required to show that one of ordinary skill in the art would have had a specific motivation to combine prior art references, such a showing may be helpful to the obviousness analysis. *Id.* at 418; *see also id.* at 402.

One of skill in the art would have had reason to or been motivated to combine the references identified herein because, for example, the combinations fall into one or more of the following categories:

- A combination of elements known in the prior art according to known methods to yield a predictable result;
- A combination that is a simple substitution of one or more known elements for another to obtain a predictable result;
- A combination that involves using a known technique to improve a similar device or method in the same way;
- A combination that involves applying a known technique to a known device or method ready for improvement to yield a predictable result;
- A combination that results from a finite number of identified, predictable solutions with a reasonable expectation of success, such that the solution was one which was “obvious to try”;
- A combination that results from known work in one field of endeavor prompting variations of it for use either in the same field or a different field based on design incentives or other market forces in which the variations were predictable to one of ordinary skill in the art; and
- A teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill in the art to modify the prior art reference or to combine the teachings of various prior art references to arrive at the claimed invention.

Further, the Federal Circuit has held that a motivation to combine references may be implicit for patents based on improvements:

[A]n implicit motivation to combine exists not only when a suggestion may be gleaned from the prior art as a whole, but when the “improvement” is technology-independent and the combination of references results in a product or process that is more desirable, for example because it is stronger, cheaper, cleaner, faster, lighter, smaller, more durable, or more efficient. Because the desire to enhance commercial opportunities by improving a product or process is universal—and even common-sensical—we have held that there exists in these situations a motivation to combine prior art references even absent any hint of suggestion in the references themselves. In such situations, the proper question is whether the

ordinary artisan possesses knowledge and skills rendering him *capable* of combining the prior art references.

DyStar Textilfarben GmbH & Co. Deutschland KG v. C.H. Patrick Co., 464 F.3d 1356, 1368 (Fed. Cir. 2006).

The prior art references identified in these contentions explicitly or implicitly refer to other prior art references, share common authors or inventors, were published in the same journals, presented at the same conferences, and/or were developed at common companies, schools, or organizations, all of which would motivate one of skill in the art to combine them. These references are also within the field(s) of the Asserted Patent and are directed to similar subject matter or problems within the field(s). Additionally, any products, devices, or processes described in the references existed and/or were invented before or during the period in which the claimed inventions were developed, providing further motivation to combine them.

Intel may rely on cited or uncited portions of the prior art, other documents, and/or percipient and expert testimony to establish that a person of ordinary skill in the art would have had a reason to or been motivated to modify or combine the prior art so as to render the claims invalid as obvious.

4. Exhibits to Intel's Invalidity Contentions

Exhibit A-1 to these Invalidity Contentions set forth Intel's prior art arguments in more detail.

Section A of Exhibit A-1 identifies Claim Chart Exhibits (Exhibits A-2 through A-26) of exemplary prior art references that render the Asserted Claims anticipated and/or obvious under the proper construction of those claims and/or under Iida's apparent interpretation of the claims as set forth in its Complaint and Preliminary Infringement Contentions. All of the Asserted Claims of the Asserted Patent are invalid as anticipated under 35 U.S.C. § 102 in view of each of

the prior art references identified herein as specified in the Claim Chart Exhibits, which identify specific examples of where each limitation of the Asserted Claims is found in the prior art reference, and/or obvious under 35 U.S.C. § 103 in view of the state of the prior art alone, the admitted prior art described in the Invalidity Contentions, and/or in combination with the references and disclosures detailed in Tables 1–3 of the Invalidity Contentions as well as the prior art references identified herein as specified in the Claim Chart Exhibits. As such, Intel’s inclusion of exemplary prior art references and combinations does not preclude Intel from identifying other invalidating combinations as appropriate.

Section B of Exhibit A-1 sets forth exemplary combinations of the charted prior art references that render obvious the Asserted Claims of the ’737 patent in light of the express and/or inherent disclosures of the references, as well as in view of the knowledge of a person of ordinary skill in the art. Intel reserves the right to rely on any combinations of the references as reflected in the corresponding claim charts to demonstrate the obviousness of the Asserted Claims of the ’737 patent. For at least the reasons described above, in Exhibit A-1, and in the Claim Chart Exhibits, it would have been obvious to one of ordinary skill in the art to combine any of a number of prior art references, including any combination of those identified in the Claim Chart Exhibits, to meet the limitations of the asserted claims. As such, Intel’s inclusion of exemplary combinations does not preclude Intel from identifying other invalidating combinations as appropriate.

Section C of Exhibit A-1 sets forth Intel’s contention that there is no evidence of any indicia of non-obviousness of the Asserted Claims. Intel reserves the right to respond to and address any evidence purporting to support indicia of non-obviousness if Plaintiff were to come forward with such evidence, and based on the results of further investigation and analysis.

Section D of Exhibit A-1 sets forth Intel's contention that a person of ordinary skill in the art at the time of the claimed inventions had reason to modify each reference listed and charted in Intel's Claim Chart Exhibits or combine that reference with one or more of the other references and disclosures detailed in Tables 1–3 of these Invalidity Contentions in light of the knowledge of a person of ordinary skill at the time and information in the prior art references cited herein. The prior art references identified above that have not been charted show the state of the art at the times of or prior to the purported inventions of the Asserted Patent, and/or show reasons or motivations to combine prior art references, as set forth in Section D of Exhibit A-1, described in more detail below.

The Claim Chart Exhibits may cite and incorporate by reference prior art references, other relevant material, and/or sections of other charts. These citations are intended to incorporate the referenced information in its entirety. The identification of any patent or patent publication shall be deemed to include any counterpart patent or application filed, published, or issued anywhere in the world. The citations to any specifications, guidelines, or reports published by standard-setting organizations shall be deemed to include any product that implements such specifications, guidelines, or reports and that would qualify as prior art under 35 U.S.C. § 102, *e.g.*, under §§ 102(a), 102(b), or 102(g)(2).

The references discussed in the Claim Chart Exhibits may disclose the elements of the asserted claims explicitly or inherently, or they may be relied upon to show the state of the art in the relevant time frame. In addition, statements in the Claim Chart Exhibits that it would be obvious to modify the teachings of a reference are not meant to exclude arguments that it would also be obvious to combine the reference with other prior art.

The Claim Chart Exhibits cite exemplary portions of identified references. The identified references may contain additional disclosures for a particular claim limitation, and Intel reserves all rights to rely on other portions of the identified references to support its contentions. Persons of ordinary skill in the art generally read a prior art reference as a whole and in the context of other publications and literature. Intel may rely on uncited portions of the prior art references, other prior art references incorporated into such references, other publications, and percipient and/or expert testimony to provide context and as aids to understanding and interpreting the portions of the cited prior art references. Disclosures relating to initial elements of dependent claims are disclosed in connection with the independent claims from which they depend, even though they are not repeated for each dependent claim.

Intel may also rely on uncited portions of the prior art references, other publications, and expert testimony to establish that a person of ordinary skill in the art would have been motivated to modify or combine certain cited references and/or would have applied his or her general knowledge and common sense so as to render the claims obvious. Where Intel cites to a particular figure in a prior art reference, the citation should be understood to encompass the caption and description of the figure, any text relating to the figure, and the figure itself. Similarly, where a portion of text refers to a figure, the citation should be understood to include the figure as well.

The U.S. and foreign patents, publications, products and systems disclosed in the Claim Chart Exhibits qualify as prior art under various provisions of the Patent Act (prior to its amendment by the America Invents Act), including pre-AIA 35 U.S.C. § 102(a), (b), (e) and/or (g). Intel may also rely on persons identified as inventors of the patents and authors of the publications cited in the Claim Chart Exhibits, as well as individuals identified in any of the

parties' initial disclosures and discovery responses, and others as they become identified through further discovery, as prior inventors, as persons of ordinary skill in the art, or as persons having knowledge of, or having previously used, publicly disclosed, published, offered for sale, or sold, the alleged inventions claimed in the Asserted Patent. Discovery is ongoing, and Intel continues to investigate and analyze the prior art. Intel reserves the right to supplement and/or amend these contentions based on the results of such investigation and analysis. Intel further reserves the right to rely on the system described in any prior art publication(s) cited herein in addition to, or in place of, relying on the publications themselves.

All items of prior art contained in the Claim Chart Exhibits, either alone or in combination, render one or more of the Asserted Claims obvious. Intel's contention in the Claim Chart Exhibits that a reference discloses a limitation also means that Intel contends that the reference renders that limitation obvious alone, in combination with the knowledge of a person of ordinary skill in the art, and in combination with other references.

Some of the disclosures cited in certain of the Claim Chart Exhibits are based on Intel's understanding of how Iida is interpreting the Asserted Claims for the purpose of his Infringement Contentions (to the extent Iida's contentions can be understood). Intel does not intend to and does not adopt Iida's claim interpretations or concede that Iida's claim interpretations are correct. Nothing stated herein or in any Claim Chart Exhibit should be treated as an admission or suggestion that Intel agrees with Iida regarding either the scope of any of the Asserted Claims, or any express or implied claim constructions advanced by Iida in its Infringement Contentions or anywhere else, or that any of Intel's accused products meet any limitation of the Asserted Claims. Nothing stated herein or in any Claim Chart Exhibit should be construed as an admission or waiver of any particular construction of any claim term. Nothing stated herein or in any Claim

Chart Exhibit should be construed as a waiver of any argument available under 35 U.S.C. § 112. Intel reserves all rights to challenge any of the Asserted Claims under 35 U.S.C. § 112, including by arguing that they are not supported by the written description, not enabled, indefinite, and/or do not set forth what the inventors regarded as the invention, notwithstanding the disclosure in any Claim Chart Exhibit corresponding to that claim. *See* Section II.B, *infra*. Nothing stated herein or in any Claim Chart Exhibit should be construed as an admission or waiver with respect to the effective filing date of any of the Asserted Claims.

5. Inventorship

Intel contends that the Asserted Claims of the '737 patent are invalid pursuant to 35 U.S.C. § 102(f). For example, Toshinori Sueyoshi may be a joint inventor of the '737 patent, and therefore, his non-joinder would invalidate that patent under § 102(f). *See generally* P-00001–P-00135 (describing Sueyoshi's role in the conception and reduction to practice of the claimed invention(s) of the '737 patent). Sueyoshi is a named inventor of the Japanese patent to which the '737 patent claims priority, JP3580785B2. He was also a named inventor of the '737 patent itself until just before this suit was filed. Thus, Sueyoshi appears to have played a role in the '737 patent's alleged invention, and that role may have “(1) contribute[d] in some significant manner to the conception or reduction to practice of the invention, (2) ma[de] a contribution to the claimed invention that is not insignificant in quality, when that contribution is measured against the dimension of the full invention, and (3) do[ne] more than merely explain to the real inventors well-known concepts and/or the current state of the art.” *In re VerHoef*, 888 F.3d 1362, 1366 (Fed. Cir. 2018), as amended (May 7, 2018) (quoting *Pannu v. Iolab Corp.*, 155 F.3d 1344, 1351 (Fed. Cir. 1998)). Accordingly, the failure to name Sueyoshi as an inventor on the '737 patent may be invalidating. 35 U.S.C. § 102(f).

Intel therefore reserves the right to assert that the '737 patent is invalid pursuant to § 102(f) and/or § 102(g)(2) on additional grounds, and/or that the '737 patent is invalid pursuant to those sections, if it obtains further evidence during discovery that the named inventor of the '737 patent did not invent, or did not first invent, the subject matter claimed in the patents. For example, there may be other joint inventors who are not named in the '737 patent.

B. Invalidity Under 35 U.S.C. § 112

As detailed below, certain of the Asserted Claims lack written description or enablement, are indefinite, and/or fail to claim what the inventors regard as the invention under provisions of 35 U.S.C. § 112. The § 112 invalidity contentions set forth below are subject to revision and amendment pursuant to Federal Rule of Civil Procedure 26(e) and the Orders of record in this matter to the extent appropriate in light of, without limitation, information provided by Iida concerning its infringement allegations, further investigation and discovery, the Court's constructions of the claims at issue, positions taken by Iida in this action or any other proceeding, review and analysis of expert witnesses, and/or as other circumstances warrant.

1. Lack of Enablement/Written Description Under 35 U.S.C. § 112, ¶ 1

Paragraph 1 of 35 U.S.C. § 112 requires that the specification contain a written description of the invention. “[T]he hallmark of written description is disclosure.” *Boston Scientific Corp. v. Johnson & Johnson*, 647 F.3d 1353, 1361–62 (Fed. Cir. 2011) (citation omitted). The test for whether a specification adequately describes an invention is “whether the disclosure of the application relied upon reasonably conveys to those skilled in the art that the inventor had possession of the claimed subject matter as of the filing date [T]he test requires an objective inquiry into the four corners of the specification from the perspective of a person of ordinary skill in the art . . . [I]t is a question of fact.” *Ariad Pharms., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010) (en banc); *Boston Scientific*, 647 F.3d at 1362. “Adequate

written description means that the applicant, in the specification, must convey with reasonable clarity to those skilled in the art that, as of the filing date sought, he or she was in possession of the [claimed] invention.” *Agilent Techs., Inc. v. Affymetrix, Inc.*, 567 F.3d 1366, 1379 (Fed. Cir. 2009). It is well settled that “one cannot disclose a forest in the original application, and then later pick a tree out of the forest and say here is my invention.” *Purdue Pharma L.P. v. Faulding Inc.*, 230 F.3d 1320, 1326 (Fed. Cir. 2000). Rather, the specification must provide some guides or “blaze marks” that disclose the claimed invention “specifically, as something appellants actually invented.” *Ariad*, 598 F.3d at 1348.

The enablement requirement of § 112 requires that the patent specification teach a skilled artisan how to “make and use” the claimed invention, which the Federal Circuit has held requires teaching “those skilled in the art how to make and use the full scope of the claimed invention without ‘undue experimentation.’” *Genentech, Inc. v. Novo Nordisk A/S*, 108 F.3d 1361, 1365 (Fed. Cir. 1997) (quoting *In re Wright*, 999 F.2d 1557, 1561 (Fed. Cir. 1993)). “[T]he scope of the claims must be less than or equal to the scope of the enablement.” *Nat’l Recovery Tech., Inc. v. Magnetic Separation Sys., Inc.*, 166 F.3d 1190, 1196 (Fed. Cir. 1999).

The claims of the ’737 patent fail to reasonably convey to one of ordinary skill that the inventor(s) had possession of the subject matter of the invention and fail to enable a person of ordinary skill to make and use the invention as claimed for at least the following reasons:

- To the extent that the term “internal configuration control circuit controlling an internal configuration of said plurality of LUT units” in claims 1 and 7 of the ’737 patent, and any claims dependent therefrom, is interpreted to require the ability to alter the effective number of inputs and/or outputs of “LUT units” themselves, those claims are invalid for failure to satisfy the requirements of 35 U.S.C. § 112, ¶ 1. The specification as filed does

not contain an adequate written description and/or enabling disclosure of controlling any internal aspect of LUT units themselves, let alone the number of inputs and/or outputs of each of them. Rather, the “LUT units” described in the embodiments each have a fixed number of inputs and outputs, such as 3 inputs and 1 output in Figure 6 of the ’737 patent, or 3 inputs and 2 outputs in Figure 9 of the ’737 patent. *See, e.g.,* ’737 patent at 5:26–30, 5:46–49, 7:26–28, Figs. 6, 9.

- To the extent that the term “selector control circuit having a memory, . . . defining the internal configuration of said plurality of LUT units” in claims 1 and 7 of the ’737 patent, and any claims dependent therefrom, is interpreted to require the ability for a “selector control circuit having a memory” to change or determine the effective number of inputs and/or outputs of “LUT units” themselves, those claims are invalid for failure to satisfy the requirements of 35 U.S.C. § 112, ¶ 1. The specification as filed does not contain an adequate written description and/or enabling disclosure of changing or determining any internal aspect of LUT units themselves, let alone the number of inputs and/or outputs of each of them. Rather, the “LUT units” described in the embodiments each have a fixed number of inputs and outputs, such as 3 inputs and 1 output in Figure 6 of the ’737 patent, or 3 inputs and 2 outputs in Figure 9 of the ’737 patent. *See, e.g.,* ’737 patent at 5:26–30, 5:46–49, 7:26–28, Figs. 6, 9.
- To the extent that the term “selectively controlling I/O signals of said plurality of LUT units to set a predetermined mode of an internal configuration” in claim 13 of the ’737 patent, and any claims dependent therefrom, is interpreted to require the ability for a “selective[] control[] [of] I/O signal of said plurality of LUT units” to change or determine the effective number of inputs and/or outputs of “LUT units” themselves, those

claims are invalid for failure to satisfy the requirements of 35 U.S.C. § 112, ¶ 1. The specification as filed does not contain an adequate written description and/or enabling disclosure of changing or determining any internal aspect of LUT units themselves, let alone the number of inputs and/or outputs of each of them. Rather, the “LUT units” described in the embodiments each have a fixed number of inputs and outputs, such as 3 inputs and 1 output in Figure 6 of the ’737 patent, or 3 inputs and 2 outputs in Figure 9 of the ’737 patent. *See, e.g.*, ’737 patent at 5:26–30, 5:46–49, 7:26–28, Figs. 6, 9.

- To the extent the claim terms “the I/O signals of said plurality of LUT units are selectively controlled in accordance with data stored in the corresponding look up table” and “an input signal input to at least one of said LUT units and an output signal output from said LUT unit are selectively controlled in accordance with data stored in the corresponding look up table” in claims 14 and 15 (respectively) of the ’737 patent are interpreted to refer to a separate “look up table” from the one that is being configured, those claims are invalid for failure to satisfy the requirements of 35 U.S.C. § 112, ¶ 1. The specification as filed does not contain an adequate written description and/or enabling disclosure of selectively controlling any I/O signals of LUT units in accordance with data stored in a “look up table” that is outside of or separate from the “look up table” that is being configured.

* * *

Therefore, the Asserted Claims of the ’737 patent are invalid for lacking sufficient written description and/or an enabling disclosure.

2. Invalidity Under 35 U.S.C. § 112, ¶ 2 and/or ¶ 6

Claims are indefinite under 35 U.S.C. § 112, ¶ 2 when they “fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention.” *Nautilus, Inc. v.*

Biosig Instruments, Inc., 572 U.S. 898, 901 (2014). To the extent an asserted apparatus claim includes both apparatus and method limitations, that claim is invalid for indefiniteness under § 112, ¶ 2 because it fails to identify or notify the public of what constitutes direct infringement. *See IPXL Holdings, L.L.C. v. Amazon.com, Inc.*, 430 F.3d 1377 (Fed. Cir. 2005).

Paragraph 2 of 35 U.S.C. § 112 also requires that the claimed subject matter be what “the inventor or a joint inventor regards as the invention.” “Where it would be apparent to one of skill in the art, based on the specification, that the invention set forth in a claim is not what the patentee regarded as his invention, we must hold that claim invalid under § 112, paragraph 2.” *Allen Eng’g Corp. v. Bartell Indus., Inc.*, 299 F.3d 1336, 1349 (Fed. Cir. 2002).

Intel also identifies each claim element governed by 35 U.S.C. § 112, ¶ 6. The presence of the word “means” in a claim element creates a rebuttable presumption that § 112, ¶ 6 applies. *Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1348 (Fed. Cir. 2015). In addition, “[g]eneric terms such as ‘mechanism,’ ‘element,’ ‘device,’ and other nonce words that reflect nothing more than verbal constructs may be used in a claim in a manner that is tantamount to using the word ‘means’ because they ‘typically do not connote sufficiently definite structure’ and therefore may invoke § 112, para. 6.” *Id.* at 1350 (holding that “module” was simply a generic description for software or hardware that performs a specific function, and applying § 112, ¶ 6). The essential inquiry under § 112, ¶ 6 is whether the words of the claim are understood by persons of ordinary skill in the art to have a sufficiently definite meaning as the name for structure. *Id.* at 1348. A means-plus-function element is “construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof.” 35 U.S.C. § 112, ¶ 6. However, claims governed by § 112, ¶ 6 are indefinite if “the claim term fails to recite sufficiently definite

structure or else recites function without reciting sufficient structure for performing that function.” *Williamson*, 792 F.3d at 1348 (internal quotation marks and citation omitted).

Means-plus-function claims directed to software require the specification to disclose an algorithm corresponding to the claimed function. *See EON Corp. IP Holdings LLC v. AT&T Mobility LLC*, 785 F.3d 616, 621 (Fed. Cir. 2015); *Aristocrat Techs. Austl. Pty Ltd. v. Int’l Game Tech.*, 521 F.3d 1328, 1333 (Fed. Cir. 2008); *WMS Gaming, Inc. v. Int’l Game Tech.*, 184 F.3d 1339, 1348–49 (Fed. Cir. 1999). The specification must disclose some algorithm in “understandable terms” that “provide[] sufficient structure”; it cannot merely restate the function recited in the claim. *Finisar Corp. v. DirecTV Grp.*, 523 F.3d 1323, 1340 (Fed. Cir. 2008); *see also Blackboard, Inc. v. Desire2Learn, Inc.*, 574 F.3d 1371, 1383 (Fed. Cir. 2009) (“The ACM is essentially a black box that performs a recited function. But how it does so is left undisclosed.”); *ePlus, Inc. v. Lawson Software, Inc.*, 700 F.3d 509, 518 (Fed. Cir. 2012) (holding that “black box” labeled “Purchase Orders” was insufficient structure to perform the “generate purchase orders” function); *Noah Sys., Inc. v. Intuit Inc.*, 675 F.3d 1302, 1317 (Fed. Cir. 2012) (“[T]he disclosure must identify the method for performing the function, whether or not a skilled artisan might otherwise be able to glean such a method from other sources or from his own understanding.”).

Intel hereby incorporates by reference the enablement and written description contentions above regarding the same claim limitations. In addition to Intel’s reservation of rights stated above, Intel notes that the Court’s Scheduling Order (Docket No. 41) contemplates that all indefiniteness issues be brought to the Court’s attention through the *Markman* briefing process, Intel’s detailed arguments as to indefiniteness will be presented at that time, through the *Markman* meet and confer and briefing processes.

(a) Section 112, ¶ 2 and/or ¶ 6 Contentions for the '737 Patent

Intel reserves the right to argue that the limitations of the '737 patent listed below, when read in light of the specification and prosecution history, fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention. The written description does not use phrases that appear in these limitations, the claim language lacks antecedent basis, and/or the claim language, as phrased and read in context of other claim limitations, is insolubly ambiguous. As one of ordinary skill would not understand the metes and bounds of the claims in which these limitations appear, each of the identified claims is invalid as indefinite pursuant to 35 U.S.C. § 112, ¶ 2.

- “LUT units” (claims 1, 7, and 13, and any claims dependent therefrom)
- “internal configuration control circuit controlling an internal configuration of said plurality of LUT units” (claims 1 and 7, and any claims dependent therefrom)
- “selector control circuit having a memory, controlling said plurality of selectors in accordance with data stored in said memory, and defining the internal configuration of said plurality of LUT units” (claims 1 and 7, and any claims dependent therefrom)
- “said input signal selector and said output signal selector being controlled in accordance with the data stored in said memory” (claims 2 and 8)
- “selectively controlling I/O signals of said plurality of LUT units to set a predetermined mode of an internal configuration” (claim 13, and any claims dependent therefrom)
- “predetermined mode of an internal configuration” (claim 13, and any claims dependent therefrom)
- “the I/O signals of said plurality of LUT units are selectively controlled in accordance with data stored in the corresponding look up table” (claim 14)

- “an input signal input to at least one of said LUT units and an output signal output from said LUT unit are selectively controlled in accordance with data stored in the corresponding look up table” (claim 15)

Additionally, the Asserted Claims are invalid under § 112, ¶ 2 for failure to claim what “the inventor or a joint inventor regards as the invention.” For example, during prosecution, the inventor(s) overcame an examiner’s rejection by arguing that a prior art reference identified by the Examiner, Lane, did not disclose an internal configuration control circuit that controls an internal configuration of the *look up table*. See, e.g., P-000192 (purporting to distinguish Lane). Yet the Asserted Claims recite controlling an internal configuration of the “LUT units” (claims 1 and 7, and claims dependent therefrom) or selectively controlling I/O signals of “LUT units” to set a predetermined mode of an internal configuration (claim 13, and claims dependent therefrom). To the extent the claims recite controlling or setting the “internal configuration” of the claimed LUT units (as opposed to the claimed look up table), that is not, based on the specification, what the inventor(s) apparently regarded as the invention. As another example, claims 14 and 15 of the ’737 patent recited selectively controlling I/O signals of LUT units “in accordance with data stored in the corresponding look up table.” To the extent this recited data refers to something besides the type of data stored in element 71 of Figure 6 or element 81 of Figure 9, that is also not, based on the specification, what the inventor(s) apparently regarded as the invention.

In addition, claim 13 of the ’737 patent and any claims dependent therefrom recite both a system/device and method for using that system/device, which “does not apprise a person of ordinary skill in the art of [their] scope” and renders them invalid under § 112, ¶ 2. *IPXL Holdings*, 430 F.3d at 1384.

The limitations of the '737 patent listed below are governed by § 112, ¶ 6 because the claim language is not understood by persons of ordinary skill in the art to have a sufficiently definite meaning as the name for structure. Each of the claims in which these limitation(s) appear is indefinite because the specification fails to disclose, or clearly link or associate, the structure, material, or acts corresponding to the listed limitation in the claim.

- “internal configuration control circuit” (claims 1 and 7, and any claims dependent therefrom)
- “selector control circuit” (claims 1 and 7, and any claims dependent therefrom)
- “selector(s)” (claims 1 and 7, and any claims dependent therefrom)
- “input signal selector” (claims 2, 3, 8, and 9)
- “output signal selector” (claims 2, 3, 8, and 9)

* * *

Therefore, all of the Asserted Claims of the '737 patent are invalid under § 112, ¶ 2 and/or ¶ 6 for indefiniteness and/or failing to particularly point out and distinctly claim the subject matter which the applicant regarded as the inventions.

C. Unenforceability

The claims of the '737 patent are unenforceable due to inequitable conduct before the United States Patent and Trademark Office (“PTO”). Intel hereby incorporates by reference its affirmative defense and counterclaim of inequitable conduct, and the allegations therein, from its Second Amended Answer to the Complaint and Amended Counterclaims, including ¶ 101 and ¶¶ 117–179.

In particular, the Semiconductor Technology Academic Research Center (“STARC”) (the original assignee of the '737 patent), Toshinori Sueyoshi, Plaintiff, and others associated with the

prosecution of the '737 patent ("the Applicants"), as well as their prosecuting attorneys or agents, withheld all or substantially all portions of material Japanese prior art references from the PTO, including the Sato and Yamada I prior art references cited in Table 1 above. The Applicants were aware of and understood the materiality of those references to the U.S. patent application because of a June 2001 prior art survey conducted by the Fujitsu Patent Division on behalf of STARC, before the Japanese parent application to the '737 patent was filed, and a March 15, 2004 Japanese Patent Office ("JPO") Office Action (the "Japanese Office Action") rejecting all the pending claims in the Japanese parent application, where those claims were nearly identical in scope to the claims pending in the U.S. application. The Applicants also withheld from the PTO the Japanese Office Action and their response, including narrowing amendments to the claims pending before the JPO. Moreover, while the Applicants disclosed two Japanese prior art references (Woo II and Kimura) on June 28, 2004, after narrowing the claims in the Japanese application in response to the Japanese Office Action, they did so in a misleading way by omitting the relevant context of the Japanese prosecution and submitting only translations of the abstracts for those references.

The single most reasonable inference for the behavior of the Applicants during prosecution of the '737 patent is an intent to deceive the PTO. As alleged in the First Amended Answer to the Complaint and Amended Counterclaims, the Applicants demonstrated a pattern of breaches of their duty of candor to the PTO in their prosecution of the application that issued as the '737 patent, and this was done with the intention to deceive the PTO. Moreover, the information withheld as a result of Applicants' omissions and misrepresentations was not cumulative of other references or information before the PTO. But for the Applicants' and

prosecuting attorneys/agents' failure to comply with the duty of candor to the PTO, the '737 patent would not have issued.

III. DOCUMENT PRODUCTION

Pursuant to the Court's Standing Order Governing Proceedings 4.2—Patent Cases § II.4 and the Scheduling Order in the above-captioned matter (Docket No. 41), Intel is producing with these Invalidity Contentions prior art referenced in the Invalidity Contentions and technical documents, including software where applicable, sufficient to show the operation of the accused product(s). These documents are contained in the Bates ranges 97300DOC000000002 to 97300DOC000193096 and 97300DOC000193331 to 97300DOC000194440. Intel will further supplement this production should it later find additional, responsive documents.

Dated: March 9, 2023

/s/ Zachary M. Briers

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CERTIFICATE OF SERVICE

I certify that on March 9, 2023, I caused a copy of **Intel Corporation's First Amended Preliminary Invalidity Contentions** and accompanying Exhibits A-1 and A-26 to be served electronically on counsel of record for Plaintiff Masahiro Iida.

/s/ J. Kain Day
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