UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,
Petitioner

v.

PROFESSOR MASAHIRO IIDA,
Patent Owner

Case IPR2023-00864
U.S. Patent No. 6,812,737

PATENT OWNER'S PRELIMINARY RESPONSE TO PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 6,812,737

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PATENT OWNER'S EXHIBIT LIST

Exhibit No.	Description of Document
2001	S. Singh, J. Rose, P. Chow and D. Lewis, *The effect of logic block architecture on FPGA performance,* IEEE Journal of Solid-State Circuits, vol. 27, no. 3 (March 1992)
2002	J. Rose, R. J. Francis, D. Lewis and P. Chow, *Architecture of field-programmable gate arrays: the effect of logic block functionality on area efficiency*, IEEE Journal of Solid-State Circuits, vol. 25, no. 5 (Oct. 1990)
2003	E. Ahmed and J. Rose, *The effect of LUT and cluster size on deep-submicron FPGA performance and density*, Proceedings of the 2000 ACM/SIGDA eighth international symposium on Field programmable gate arrays (2000)
2004	M. Hutton, et al., *Fracturable FPGA Logic Elements*, Altera Corporation (2006)
2005	Claim Construction Order in *Iida v. Intel Corp.*, No. 1:23-cv-00899-ADA (W.D. Tex.)
2006	Order Granting Defendant's Motion to Transfer in *Iida v. Intel Corp.*, No. 1:23-cv-00899-ADA (W.D. Tex.)
2007	First Amended Scheduling Order in *Iida v. Intel Corp.*, No. 1:23-cv-00899-ADA (W.D. Tex.)
2008	Intel's Amended Preliminary Invalidity Contentions in *Iida v. Intel Corp.*, No. 6:22-cv-00662-ADA (W.D. Tex.)

I. INTRODUCTION

Pursuant to 37 C.F.R. § 42.107(a), Professor Masahiro Iida ("Patent Owner"), submits the following Preliminary Response to the Petition for *Inter Partes* Review (the "Petition") of claims 1-16 of U.S. Patent No. 6,812,737 ("'737 patent") submitted by Intel Corporation ("Petitioner"), in the above-captioned matter.

The Board should deny the Petition (1) as a sound exercise of its discretion under 35 U.S.C. § 314(a) upon consideration of the factors set forth in *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (PTAB Mar. 20, 2020), and (2) because the Petition fails to present a compelling challenge to the patentability of the claims of the '737 patent. In this case, all six of the *Fintiv* factors militate against institution. Parallel District Court litigation between the Patent Owner and the Petitioner resumed at the end of July and is now scheduled to proceed to trial in September 2024, months before a final written decision would be due. As a result, *inter partes* review in this case would not serve as an effective and efficient *alternative* to district court litigation. Rather, it would simply be a duplication and waste of both the Board's and the parties' resources.

Moreover, the Petition clearly fails to establish that each and every limitation of the challenged claims of the '737 patent are taught in or suggested by the cited references. Critically, the Petition fails to show that the combination of Fujii with

Betz, or the combination of Fujii with Betz and Chow, disclose a look up table comprising: (1) a plurality of LUT units; and (2) a configuration control circuit controlling an internal configuration of the plurality of LUT units wherein the configuration control circuit comprises (a) a plurality of selectors selecting I/O signals of said plurality of LUT units, and (b) a selector control circuit having a memory, controlling said plurality of selectors in accordance with data stored in said memory, and defining the internal configuration of said plurality of LUT units.

Section 314(a) "invests the Director with discretion on the question whether to institute review." *SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1348, 1356 (2018). "[T]he agency's decision to deny a petition is a matter committed to the Patent Office's discretion." *Cuozzo Speed Techs., LLC v. Lee*, 579 U.S. 261, 273 (2016). "[T]he PTO is permitted, but never compelled, to institute an IPR proceeding." *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1367 (Fed. Cir. 2016). For the reasons discussed below, the Board should exercise its discretion by refraining from instituting *inter partes* review in the present case because: (1) all of the discretionary factors militate against institution; and (2) Petitioner has failed to present sufficient evidence that the challenged claims are obvious as the cited art fails to teach or suggest the claimed invention.

II. THE RELEVANT TECHNOLOGY

A. Field Programmable Gate Arrays

Field Programmable Gate Arrays (FPGAs) are programmable logic devices that typically comprise three major components: a grid of programmable logic elements, input/output (I/O) elements, and interconnect elements. *See* Declaration of Dr. Marwan Hassoun in support of Patent Owner's Responsive Claim Construction Brief in *Iida v. Intel Corp.*, No. 6:22-cv-00662-ADA (W.D. Tex.) attached to the Petition as Exhibit 1033 at ¶ 18. The programmable logic elements (also called logic blocks) are capable of expressing Boolean (logic) functions, the programmable I/O elements provide an external interface, and the routing elements (e.g., wires) connect the different parts. *Id.*

When considering logic block architecture, there are several trade-offs between area efficiency and delay. *Id.* at ¶ 19. The area efficiency indicates how efficiently logic blocks are used when a circuit is implemented on an FPGA. *Id.* The area efficiency is higher when logic blocks are used with a low number of unused (*i.e.*, wasted) elements (*i.e.*, functionality). *Id.* Regarding area efficiency, there are the following trade-offs in logic blocks:

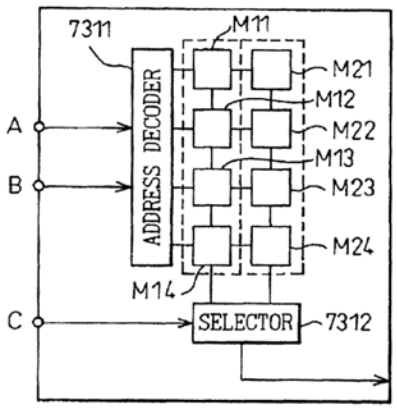
- As functions per logic block increase, the total number of logic blocks required to implement the desired circuit decreases.

• On the other hand, since the area of the logic block itself and the number of inputs and outputs increase, the overall area per logic block increases.

Id. at ¶ 20.

B. Look Up Tables

Programmable logic blocks used in FPGAs implement logic functions using look up tables, which are often referred to by the acronym "LUT." *Id.* at ¶ 21. A look up table is a "digital memory" that can implement a logic function by storing the values for that function's truth table[1] in its memory cells. *Id.* One example of a look up table is depicted as a block diagram in Fig. 7 of the '737 patent:



Id. at ¶ 22. As shown in this figure, the memory comprises a four-by-two array of eight bits (M11–M14 and M21–M24) and a selector (7312) that selects between

[1] A truth table is a tabular representation of all the combinations of values for inputs and their corresponding outputs.

the two columns of memory cells that are collectively addressed using three binary values (A, B, and C)—which are the inputs. *Id.*

The number of LUT inputs is one of the most important factors when determining the structure and number of logic blocks. *Id.* at ¶ 23. As the number of inputs of the LUT increases, the total number of logic blocks required to implement a given logic function decreases. *Id.* On the other hand, because a LUT having k inputs requires 2^k memory bits, the overall area of each logic block increases. *Id.* Furthermore, as the number of input/output pins of the logic block increases, the area of the routing part also increases. *Id.* As a result, the overall area per logic block increases as well. *Id.* Since the area of an FPGA is a function of the total number of logic blocks × the area per logic block, there is clearly an area trade-off. *Id.*

Another consideration is processing speed. *Id.* at ¶ 24. Generally, a larger input LUT results in a reduction in the number of circuit components (commonly known as logic stages) the signals have to traverse (commonly known as logic depth) in order to produce the desired output (i.e., implement the logic function). *Id.* On the other hand, other parameters being equal, to implement the same function using a smaller input LUT would require more logic stages and thus a larger logic depth resulting in slower operating speed (more delay). *Id.*

To summarize, if the number of inputs of a LUT is large, the number of logic stages to implement a large function is reduced, generally resulting in higher operational speed. *Id.* at ¶ 25. However, when implementing a smaller logic function that, for example, does not utilize all of the LUT inputs, the area efficiency is reduced due to unused circuitry within the logic block. *Id.* On the other hand, if the number of inputs of the LUT is small, the number of logic stages to implement the same function increases and the operational speed is degraded; but, area efficiency is improved. *Id.* In this fashion, the input size of the LUT is closely related to the area efficiency and delay of the FPGA. *Id.*

Many of the leading researchers in the field of programmable computing—Professor Jonathan Rose, his colleagues at the University of Toronto, as well as other individuals in Toronto and San Jose working for Altera Corporation (Petitioner's predecessor infringer)—spent the 1990s and several of the first years of the 21st century grappling with how to optimize the aforementioned tradeoffs. *See*, *e.g.*, Exhibits 2001-2003. These efforts were mostly focused on determining the optimal input size for the LUTs used in logic blocks. *See id.*

III. U.S. PATENT NO. 6,812,737 AND THE CHALLENGED CLAIMS

A. The ’737 Patent

On June 29, 2001, Professor Iida (then, a doctoral candidate) filed a patent application directed to a revolutionary breakthrough in FPGA chip architecture.[2] At that time, the leading researchers in the field were still focused on optimizing LUT size for area efficiency and delay. *See* Exhibit 2003. Importantly, their research was predicated on the long-held assumption that LUT size—i.e., the number of inputs for a given look up table—was fixed. In rejecting that conventional assumption, Professor Iida invented an FPGA architecture that allowed a large look up table, such as a 6-LUT, to be configured in such a manner that, in one configuration, it operates as a single, 6-input look up table and, in a variety of other configurations, it operates as two or more smaller look up tables of varying size. *See*, *e.g.*, ’737 patent attached to the Petition as Exhibit 1001 at Figs. 3A-3F, 6, and 9. This invention was a literal breakthrough insofar as it broke through the entire optimization problem with which many others, including the leading researchers in

[2] The application filed on June 29, 2001, was a Japanese patent application. The U.S. application (which issued as the ’737 patent) was filed on June 28, 2002—within one year of the original filing date—and claimed priority to the Japanese application.

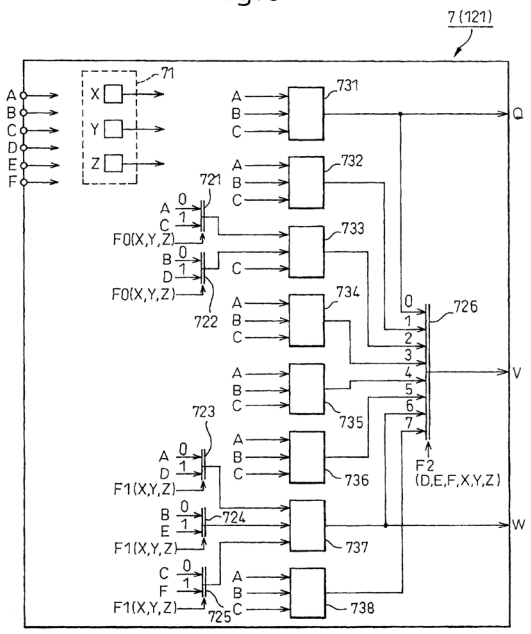
the field, had been endeavoring for years to solve—without success. With Professor Iida's novel architecture, one no longer needed to be concerned with the "optimal LUT size" when look up tables could now be configured, at will, to vary in size.

The revolutionary nature of Professor Iida's invention was further confirmed when, on February 10, 2003, about nineteen months after Professor Iida's first filing date, Altera (the original infringer acquired by Petitioner in 2015) filed its own patent application[3] on what it termed Adaptive Logic Modules (ALMs) and, shortly thereafter, when Altera introduced the Stratix II line of FPGA chips trumpeting to the world a 15% performance improvement with a 12% area improvement realized specifically by the use of ALMs. *See* Exhibit 2004.

The '737 patent generally relates to a novel architecture for configuring look up tables that enables a reduction in implementation area. Figure 6 the '737 patent provides an overview of one embodiment:

[3] Altera's patent application issued as U.S. Patent No. 6,943,580 on September 13, 2005. Professor Iida's prior filed U.S. patent application was not considered in the prosecution of Altera's patent application.

Fig.6



As shown in Figure 6, and described at column 5, lines 26-29 of the ’737 patent, “the 6-input 3-output LUT 7 (121) is comprised of a mode changing memory 71, selectors 721-726, and 3-input 1-output LUT units (memory array) 731-738.” Exhibit 1001.

As further described in the ’737 patent:

> Each of 3-input 1-output LUT units 731-738 is comprised of an address decoder, a memory and a selector, as described later, and outputs 1 bit signal in response to 3 bit input signal, respectively. Thus, signals A, B, C are input to each of LUT units 731, 732, 734-736 and 738, and one of the signals A or C and one of the signals B or D selected by selection signal F0, and the signal C is input to the LUT unit 733, and one of the signals A or D, and one of the signals B or E, and one of the signals C or F, selected by the selection signal F1 is

input to the LUT unit 737. Output signals from the LUT units 731-738 are input to a selector (selector for selecting output signal) 726, and one of the signals is selected by selection signal F2 (D, E, F, X, Y, Z) specified by signals D, E, F and data X, Y, Z, and is output as signal V. The signal Q is the output signal from the LUT unit 731, and the signal W is the output signal from the LUT unit 737.

Exhibit 1001 at col. 5, lines 46-61.

Figures 7 and 8 of the ’737 patent each show block diagrams of exemplary 3-input 1- output LUT units that can be used in the 6-input 3-output look up table depicted in Figure 6:

Fig.7

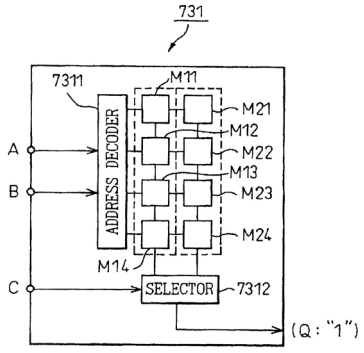
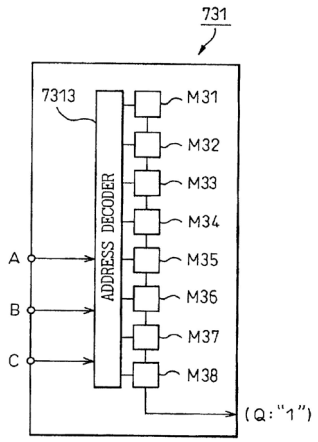


Fig.8

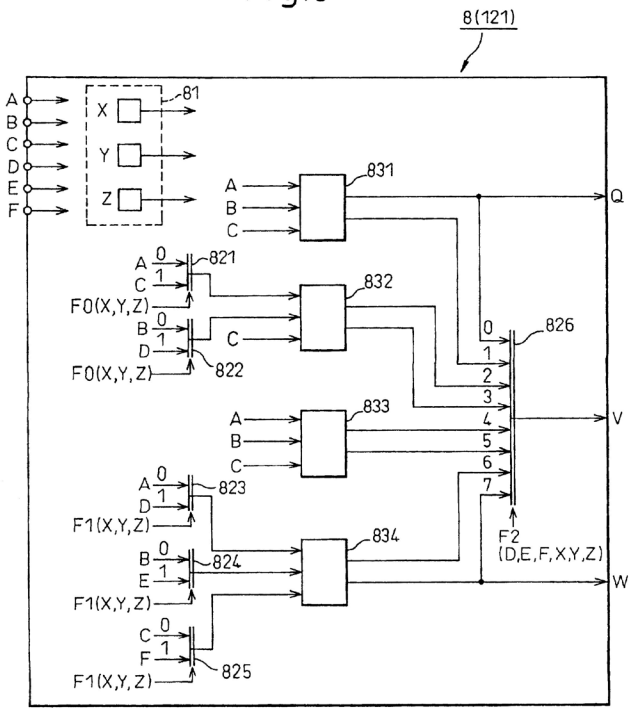


The LUT unit 731 shown in Figure 7 is comprised of an address decoder 7311, a selector 7312, and two sets of 4-bit memory unit groups M11-M14, M21-M24. The address decoder decodes 2-bit input signal A, B to designate each one of the memory unit groups M1-M14 and M21-M24, and further according to the input

signal C, selects one of the sets M11-M14 or M21-M24 to output data. *See* Exhibit 1001 at col. 5, line 66, to col. 6, line 6. The LUT unit 731 shown in Figure 8 "is comprised of an address decoder 7313, and 8 bit memory unit groups M31-M38. The address decoder 7313 decodes the 3 bit input signals A, B, C, to designate one of the memory unit groups M31-M38, and output the data (Q)." Exhibit 1001 at col. 6 lines 10-14.

Figure 9 of the '737 patent is a block diagram showing another exemplary 6-input 3-output look up table having an internal configuration that is different from the 6-input 3-output look up table shown in Figure 6:

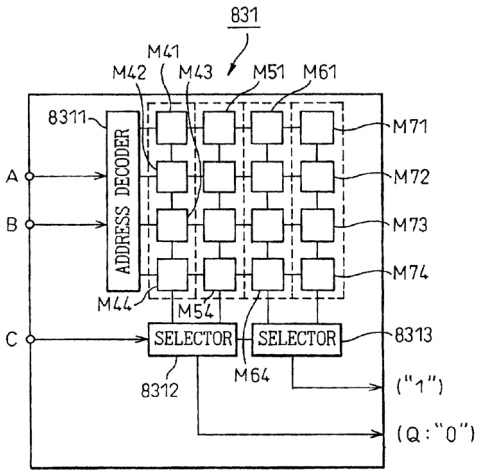
Fig.9



As described in the ’737 patent, the look up table 8(121) shown in Figure 9 “is comprised of a mode changing memory 81, selectors 821-826, and 3-input 2-output LUT units 831-834.” Exhibit 1001 at col. 7, lines 26-28.

Figure 10 of the ’737 patent is a block diagram showing an exemplary 3-input 2-output LUT unit in the 6-input 3-output look up table as depicted in Figure 9:

Fig.10

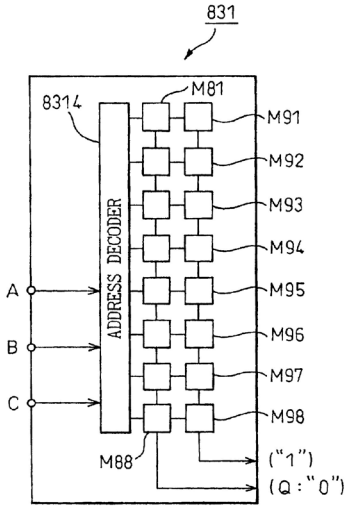


The LUT unit 831 shown in Figure 10 is comprised of an address decoder 8311, selectors 8312 and 8313, and four sets of 4-bit memory unit group M41-M44, M51-M54, M61-M64, M71-M74. The address decoder decodes 2-bit input signal A, B to designate each one for the four sets of memory unit group M41-M44, M51-M54, M61-M64, M71-M74, and by the input signal C, selects and outputs the data of one of the two sets of memory unit group M41-M44 or M51-M54 (output signal

Q: the signal supplied to the input "0" of the selector 826), and data of one of the two sets of memory unit group M61-M64 or M71-M74 (the signal supplied to the input "1" of the selector 826). Exhibit 1001 at col. 7, lines 50-61.

Figure 11 of the '737 patent is a block diagram that shows another example of a 3-input 2-output LUT unit in the 6-input 3-output look up table depicted in Figure 9:

Fig.11



As described in the '737 patent, the LUT unit 831 shown in Figure 11 "is comprised of an address decoder 8314, and two sets of 8 bit memory unit group M81-M88 and M91-M98. The address decoder 8314 decodes 3 bit input signal A, B, C to designate each one for the two sets of memory unit group M81-M88 and M91-M98, and outputs respective data. Exhibit 1001 at col. 7, line 65 to col. 8, line 5.

The foregoing examples of LUT units elucidate quite clearly and robustly how one of ordinary skill in the art would practice the claimed invention—by selecting pluralities of LUT units and other components to build a look up table of M inputs and N outputs capable of various configurations shown, by way of example, in Figures 3A-3F, 6, and 9 of the '737 patent. *See* Exhibit 1001. Importantly, it is not a matter of how simplified *block diagrams* of look up tables may be *viewed*, but rather how look up tables are actually *implemented*, that determines whether or not a look up table comprises a plurality of LUT units. A person of ordinary skill in the art would understand that, by design, a LUT unit is a look up table that cannot be fractured or divided into smaller look up tables. Exhibit 1033 at ¶ 55. This understanding would be confirmed by reference to the '737 patent, and specifically to Figures 6-11. *Id.*

The '737 patent contains three independent claims. Claim 1 is directed to a novel look up table of M inputs and N outputs that comprises a plurality of LUT units and an internal configuration control circuit controlling the internal configuration of the plurality of LUT units. The internal configuration control circuit comprises a plurality of selectors selecting I/O signals of the plurality of LUT units, and a selector control circuit having a memory, controlling said plurality of selectors in accordance with data stored in said memory, and defining the internal configuration of said plurality of LUT units. Claim 7 is directed to a

programmable logic circuit device that comprises a plurality of logic blocks each of which comprises the novel look up table as recited in claim 1. And claim 13 is directed to a method for configuring a look up table that comprises a plurality of LUT units, and selectively controlling I/O signals of said plurality of LUT units to set a predetermined mode of an internal configuration.

Claims 2-6 depend, directly or indirectly, from claim 1 and each recites additional details regarding either the plurality of LUT units or the internal configuration control circuit. Claims 8-12 depend, directly or indirectly, from claim 7 and mirror the details recited in claims 2-6. Claims 14-16 depend from claim 13, and recite details regarding how input and output signals are controlled.

B. Summary of Challenged Claims

Petitioner challenges Claims 1-16 of the ’737 patent on the following four grounds:

Claims Challenged	Basis	References
1-5, 7-11, and 13-16	§ 103(a)	Fujii in view of Betz
6 and 12	§ 103(a)	Fujii in view of Betz and general knowledge of a POSITA
1-5, 7-11, and 13-16	§ 103(a)	Fujii in view of Betz and Chow
6 and 12	§ 103(a)	Fujii in view of Betz, Chow, and general knowledge of a POSITA

C. Claim Construction

Claim construction in an *inter partes* review is only necessary when the definition of the terms is in controversy, and then only to the extent necessary to

resolve said controversy. *Realtime Data LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019); *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)). In an *inter partes* review, claims are "construed using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. § 282(b)." 37 C.F.R. § 42.100(b). All claim terms must be construed "in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent." Under this standard, claim terms are generally given their plain and ordinary meaning as would have been understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc).

In the present case, on August 21, 2023, the District Court in the parallel proceeding entered a claim construction order as to two disputed claim terms: "Look up table of M inputs and N outputs" and "LUT unit." Both terms were accorded their plain and ordinary meanings. *See* Exhibit 2005.

IV. APPLICABLE LEGAL STANDARDS

The Board may only grant an IPR petition where "the information presented in the petition ... shows that there is a reasonable likelihood that the petitioner

would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a); 37 C.F.R. § 42.108(c). Accordingly, the IPR petitioner bears the burden of showing this statutory threshold has been met. *See Office Patent Trial Practice Guide*, 77 Fed. Reg. 48,756 (Aug. 14, 2012) ("The Board ... may institute a trial where the petitioner establishes that the standards for instituting the requested trial are met ….").

On June 21, 2022, the Director issued USPTO Memorandum, Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation (the "Guidance Memo"). According to this Guidance Memo, if the evidence of unpatentability is merely sufficient to meet the statutory institution threshold—a "reasonable likelihood" of prevailing for IPR, or "more likely than not" unpatentable for post-grant review—then the Board will conduct a *Fintiv* analysis. Only if the evidence of unpatentability is compelling does the guidance preclude discretionary denial under *Fintiv*. Moreover, institution remains discretionary even where a petitioner is reasonably likely to prevail on one challenged claim. *See Salem Fabrication Techs. Grp., Inc., v. Uniglass Eng'g Oy*, IPR2022-01517, Paper 9 at 23-24 (PTAB Mar. 22, 2023) (citing *SAS Inst.*, 138 S. Ct. at 1356 and *Harmonic*, 815 F.3d at 1367).

V. A PERSON OF ORDINARY SKILL IN THE ART

Petitioner contends that a person of ordinary skill in the art ("POSITA") as of the effective filing date of the '737 Patent "would have had a bachelor's degree in electrical engineering, computer engineering, or an equivalent degree, and one year of professional experience relating to PLDs or FPGAs. More education could substitute for experience, and vice versa." Petition at 8. For purposes of this preliminary response only, the Patent Owner applies Petitioner's definition.

VI. INSTITUTION SHOULD BE DENIED UNDER *FINTIV* FACTORS

Institution of *inter partes* review is discretionary. *See* 35 U.S.C. § 314(a); *SAS Inst.*, 138 S. Ct. at 1356 (explaining that section "314(a) invests the Director with discretion on the question whether to institute review") (emphasis omitted). Section 314(a) provides the Board discretion to deny institution based on parallel proceedings involving the same patent and efficiency considerations. *See NHK Spring Co. v. Intri-Plex Techs., Inc.*, IPR2018-000752, Paper 8 (PTAB Sept. 12, 2018) (precedential).

In deciding whether to exercise discretion under 35 U.S.C. § 314(a), the Board may consider "events in other proceedings related to the same patent, either at the Office, in district courts, or the ITC." *Patent Trial and Appeal Board Consolidated Trial Practice Guide*, at 58 (Nov. 2019), https://www.uspto.gov/TrialPracticeGuideConsolidated. The precedential order in

Fintiv identifies six factors to consider when a patent owner raises an argument for discretionary denial under § 314(a). These factors are as follows:

1. Whether the court has granted a stay or evidence exists that one may be granted if a proceeding is instituted;
2. Proximity of the court's trial date to the Board's projected statutory deadline for a final written decision;
3. Investment in the parallel proceeding by the court and the parties;
4. Overlap between issues raised in the petition and in the parallel proceeding;
5. Whether the petitioner and the defendant in the parallel proceeding are the same party; and
6. Other circumstances that impact the Board's exercise of discretion, including the merits.

Fintiv, Paper 11 at 6. In evaluating these factors, the Board "takes a holistic view of whether efficiency and integrity of the system are best served by denying or instituting review." *Id.* at 6.

A. *Fintiv* Factor 1 Weighs Against Institution Because There Is No Evidence that a Stay Would Be Granted if this IPR Proceeding Were Instituted

As noted above, the first *Fintiv* factor is "whether the Court granted a stay or evidence exists that one may be granted if a proceeding is instituted." *Fintiv*, Paper 11 at 6. The parallel District Court litigation pending in the Western District of Texas, Waco Division, was stayed on March 14, 2023. *See* Exhibit 1042. This stay, however, was issued only because Petitioner had filed a motion for intra-district

transfer and the Markman hearing date was rapidly approaching. On July 27, 2023, the Court granted Petitioner's motion and lifted the stay. *See* Exhibit 2006. Notably, the Court retained the case on Judge Albright's docket. *Id.* A *Markman* hearing was held on August 15, 2023, and discovery opened on August 16, 2023. *See* Exhibit 2007.

Petitioner has indicated that it intends to move for a new stay in the parallel District Court litigation in light of its IPR petition. *See* Petition at 84. Courts in the Western District of Texas, and Judge Albright in particular, disfavor and routinely deny such motions. *See Continental Intermodal Grp. v. Sand Revolution LLC*, No. 7:18-cv-00147 (W.D. Tex. July 22, 2020) (Judge Albright) (Text Order denying motion to stay pending IPR proceeding noting that the "Court strongly believes [in] the Seventh Amendment."); *Multimedia Content Mgmt. LLC v. Dish Network*, No. 6:18-CV-00207-ADA, 2019 U.S. Dist. LEXIS (W.D. Tex. May 30, 2018) (Judge Albright) (denying stay).

In view of Judge Albright's expressed reluctance to stay trials pending IPR proceedings, it is unlikely that a stay motion would be granted pending an IPR. Moreover, the Board should not speculate as to the likelihood of a stay. "In the absence of specific evidence, [the Board] will not attempt to predict how the district court in the related district court litigation will proceed" regarding a request

for a stay. *Sand Revolution II, LLC v. Continental Intermodal Grp. – Trucking LLC*, IPR2019-01393, Paper 24 at 7 (PTAB June 16, 2020).

The first *Fintiv* factor weighs against institution.

B. *Fintiv* Factor 2 Weighs Against Institution Because a Parallel District Court Proceeding Is Scheduled for Trial Prior to the Projected Statutory Deadline for the Board's Final Written Decision.

The second *Fintiv* factor looks to whether trial will occur before the Board's deadline to issue a Final Written Decision. According to *Fintiv*, "[i]f the court's trial date is earlier than the projected statutory deadline, the Board generally has weighed this fact in favor of exercising authority to deny institution." *Fintiv*, Paper 11 at 9. The Board has routinely found this factor to weigh in favor of denial when the anticipated trial date precedes the final written decision, even if only briefly. *See e.g.*, *Stanley Black & Decker, Inc., et al. v. Zircon Corp.*, IPR2020-01572, Paper 10 at 12 (PTAB April 19, 2021) (three months); *Next Caller, Inc. v. TrustID, Inc.*, IPR2019-00961, Paper 10 at 14-15 (PTAB Oct. 16, 2019) (three months); *Eclinicalworks, LLC et al. v. Decapolis LLC*, IPR2022-00229, Paper 10 at 9 (PTAB Apr. 13, 2022) (one to two months); *E-One, Inc. v. Oshkosh Corp.*, IPR2019-00161, Paper 16 at 6 (PTAB May 15, 2019) (one month).

Petitioner has asserted that the second *Fintiv* factor weighs against discretionary denial. *See* Petition at 83. Petitioner's assertion, however, was made

at a time when the parallel District Court proceeding had been stayed and the original case schedule had been suspended. As noted above, however, the District Court has recently lifted the stay. *See* Exhibit 2006. Moreover, the District Court has entered a First Amended Case Schedule in which trial is now scheduled to begin on September 30, 2024. *See* Exhibit 2007.

If the Board were to institute a trial, the deadline to issue a final written decision would not occur until November 29, 2024, two months ***after*** the scheduled trial date in the parallel District Court litigation. According to *Fintiv*, "[i]f the court's trial date is earlier than the projected statutory deadline, the Board generally has weighed this fact in favor of exercising authority to deny institution." *Fintiv*, Paper 11 at 9

The second *Fintiv* factor weighs against institution.

C. Fintiv Factor 3 Weighs Against Institution Because the Parties Will Have Invested Significant Efforts in the Parallel Proceeding by the Time the Board's Institution Decision Is Due.

Factor 3 relates to investment in parallel proceedings by the court and the parties. *Fintiv*, Paper 11 at 9. The present parallel District Court proceeding was commenced in June 2022 and is pending in a fast-moving district that employs expedited case schedules. *See*, *e.g.*, Exhibit 2007. The parties have exchanged infringement and invalidity contentions, and fully briefed issues relating to claim construction. A claim construction hearing was held on August 15, 2023, and a

claim construction ruling was issued on August 21, 2023. Moreover, discovery opened on August 16, 2023, and the parties have already begun serving and responding to discovery requests. By the end of November 2023, when an institution decision would be due, the parties will have already exchanged and responded to initial sets of written discovery requests and produced and reviewed substantial numbers of documents. With almost 18 months behind them and only 10 months remaining until trial, the parties will have already invested a significant amounts of resources in the parallel District Court proceeding by the time an institution decision will be due.

The third *Fintiv* Factor weighs against institution.

D. *Fintiv* Factor 4 Weighs Against Institution Because There Is Substantial Overlap Between the Parallel Proceeding and Any Potential *Inter Partes* Review Proceeding.

"[I]f the petition includes the same or substantially the same claims, grounds, arguments, and evidence as presented in the parallel proceeding, this fact has favored denial." *Fintiv*, Paper 11, at 12. This factor weighs against institution because there is substantial overlap between the claims, prior art, and invalidity/patentability theories at issue in the parallel District Court proceedings and any potential *inter partes* review proceeding that would be instituted.

As demonstrated by Petitioner's Amended Preliminary Invalidity Contentions, Petitioner's invalidity position in the parallel District Court

proceeding relies upon the same references common to all grounds stated in the Petition. *See* Exhibit 2008 at pp. 8 (Fujii) and 40 (Betz). Because of this substantial overlap, there are particularly strong "concerns of inefficiency and the possibility of conflicting decision" if the IPR is instituted. *Fintiv*, Paper 11 at 12.

In the present case, the Western District of Texas will have adjudicated the validity of the claims of the '737 patent, based on the very same references relied upon in the Petition, before a final written decision would be due.[4] *See Eclinicalworks*, Paper 10 at 13 (finding factor 4 weighs strongly in favor of denial where the ground in the petition was included in the preliminary invalidity contentions in parallel case); *Fintiv*, Paper 15 at 15.

Moreover, the Petitioner has not stipulated not to pursue a determination of invalidity in the parallel District Court proceeding on the same grounds as in the Petition.[5] Thus, if the Board were to institute *inter partes* review in this case, the

[4] Insofar as all of the grounds stated in the Petition are based on obviousness—a question of law for the Court to decide—the adjudication of the validity of the '737 patent with respect to the references cited in the Petition may actually occur in advance of trial.

[5] Petitioner has declined to employ a *Sotera* stipulation not to pursue in the District Court proceeding those grounds it has raised in the Petition or that it could have

Board would be deciding *exactly* the same issues that have been raised in the parallel District Court proceeding. Moreover, as noted above in connection with the second *Fintiv* factor, those issues will have *already been addressed* in the parallel District Court proceeding before a final written decision would issue. This is the epitome of inefficiency and potentially conflicting decisions that were cautioned against in *Fintiv* and the Guidance Memo. *Fintiv*, Paper 11 at 12; Guidance Memo at 7. Instituting an IPR proceeding in this case would be an inefficient use of the Board's limited resources because the parallel District Court litigation, in which Petitioner has asserted precisely the same prior art and arguments, will reach trial well before an IPR proceeding would conclude. A discretionary denial on this basis is entirely consistent with Congressional intent which created IPRs "to provide an effective and efficient *alternative* to district

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reasonably raised in the Petition. *See Sotera Wireless, Inc. v. Masimo Corp.*, IPR2020-01019, Paper 12 (PTAB Dec. 1, 2020). Had it done so, Petitioner would have ensured that an *inter partes* review would be a "true alternative" to the district court proceeding. *Id.* at 19. Rather, by pursuing the same arguments in parallel proceedings, Petitioner has chosen to promote a duplication of efforts and the attendant waste of limited judicial and administrative resources resulting therefrom. This choice should not be endorsed or rewarded by the Board.

court litigation." *NHK Spring*, Paper 10 at 20 (emphasis supplied, internal citation omitted).

The fourth *Fintiv* factor weighs against institution.

E. *Fintiv* Factor 5 Weighs Against Institution Because the Petitioner Is the Defendant in the Parallel District Court Proceedings.

Petitioner in this proceeding is the defendant in the parallel District Court litigation. The Board determined in *Sand Revolution* that "[a]lthough it is far from an unusual circumstance that a petitioner in *inter partes* review and a defendant in a parallel district court proceeding are the same, or where a district court is scheduled to go to trial before the Board's final decision would be due in a related *inter partes* review, this factor weighs in favor of discretionary denial." *Sand Revolution*, Paper 24, at 12-13 (citing *Fintiv* at 13-14). In denying institution in the *Fintiv* proceeding, the Board determined that "[b]ecause the petitioner and the defendant in the parallel proceeding are the same party, this factor weighs in favor of discretionary denial." *Fintiv*, Paper 15, at 15.

As noted above, Petitioner is the defendant in the parallel District Court proceeding presently pending in the Western District of Texas in which the Patent Owner is asserting that Petitioner has infringed the '737 Patent, and Petitioner is challenging the validity of the '737 Patent using the same arguments and prior art references identified in the Petition. *See Cisco Sys., Inc. v. Ramot at Tel Aviv Univ.*

Ltd., IPR2020-00123, Paper 14 at 10 (PTAB May 15, 2020) (denying institution because "the parallel proceedings would duplicate effort. This is an inefficient use of Board, party, and judicial resources and raises the possibility of conflicting decisions").

The fifth *Fintiv* factor weighs against institution.

F. Fintiv Factor 6 Weighs Against Institution Because There Are No Other Circumstances that Favor Institution, and the Merits of Petitioner's Challenges are Weak.

When the first five *Fintiv* factors favor denial, the sixth *Fintiv* factor looks to whether Petitioner has put forth a compelling challenge. *See CommScope Techs. LLC v. Dali Wireless, Inc.*, IPR2022-01242, Paper 23 at 5 (PTAB Feb. 27, 2023) (precedential). When determining whether there is a compelling unpatentability challenge, "the Board evaluates whether the Petition presents challenges 'in which the evidence, if unrebutted in trial, would plainly lead to a conclusion that one or more claims are unpatentable by a preponderance of the evidence.'" *Id.* at 3 (quoting Guidance Memo at 4).

As explained more fully below, Petitioner's challenges to the validity of the '737 patent based on Fujii combined with Betz, or Fujii combined with Betz and Chow, lack merit as the cited references fail to teach or suggest a look up table of M inputs and N outputs comprising a plurality of LUT units and an internal configuration control circuit controlling an internal configuration of said plurality

of LUT units. Therefore, "[t]he merits, taken as a whole, do not tip the balance in favor of Petitioner and instead also weigh in favor [of] discretionary denial in a balanced assessment of all the circumstances." *Fintiv*, Paper 15 at 17.

The sixth *Fintiv* factor weighs against institution.

G. Summary of *Fintiv* factors.

As outlined above, each one of the six *Fintiv* factors weighs against institution of *inter partes* review. Taken together, the collective and coincident direction of all of the *Fintiv* factors make a compelling case against institution. Therefore, under § 314(a) and in consideration of the totality of the *Fintiv* factors, the Board should exercise its discretion and deny institution of *inter partes* review.

VII. RESPONSE TO PETITION GROUNDS

Because denial of the Petition is warranted under § 314(a), the Board need not reach the substantive merits of the Petition. A substantive analysis is nevertheless provided below, if only to underscore the weakness of the Petition (which, as explained above, is a consideration under *Fintiv* factor six).

A. Summary of Petition Grounds.

Petitioner raises four separate but closely related grounds as the basis for the Petition. According to Ground 1, Petitioner asserts that Japanese Unexamined Patent Application Publication No. H09-121153A ("Fujii") in combination with Vaughn Betz et al., *Architecture and CAD for Deep-Submicron FPGAs* (Kluwer

Academic Publishers 1999) ("Betz") renders obvious claims 1-5, 7-11, and 13-16 of the '737 patent. According to Ground 3, Petitioner asserts that Fujii in combination with Betz and Paul Chow et al., *The Design of a SRAM-Based Field-Programmable Gate Array—Part II: Circuit Design and layout*, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 7, no. 3, pp. 321-330, Sept. 1999 ("Chow") also renders obvious claims 1-5, 7-11, and 13-16 of the '737 patent.

According to Ground 2, Petitioner asserts that Fujii in combination with Betz and the general knowledge of a person of ordinary skill in the art renders obvious claims 6 and 12 of the '737 patent. And according to Ground 4, Petitioner asserts that Fujii in combination with Betz, Chow, and the general knowledge of a person of ordinary skill in the art also renders obvious claims 6 and 12 of the '737 patent.

B. Overview of Fujii.

Fujii is directed to a programmable logic element. This programmable logic element is characterized as "a unit for implementing logic functions in a programmable LSI[6] whose logic functions can be programmed by a user." Exhibit

[6] Although Fujii doesn't explain the term, "LSI" is a well-known acronym in the semiconductor industry that stands for "large-scale integration" and refers to the

1005 at (0001). As explained in the abstract of Fujii, "[t]he objective is to provide a programmable logic element capable of efficiently realizing a desired logic function using fewer logic elements and less memory according to the logic function to be realized." *Id.* at Abstract. According to Fujii, this objective is achieved by a logic element in which "a plurality of selection circuits in a logic element are connected to different memory circuits, and are divided into a plurality of selection circuits each having a smaller number of inputs than the number of inputs of the logic element, and a plurality of logic functions having inputs less than the number of inputs of the logic elements are simultaneously assigned to one logic element." *Id.* at (0010).

Fujii's approach of using selection circuits and logic functions to build a unitary programmable logic element is made plain in the section entitled "Embodiments and Examples of the Invention." Fujii includes figures depicting three slightly different embodiments: Figure 1 depicts programmable logic element PL1, Figure 8 depicts programmable logic element PL2, and Figure 15 depicts

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process of integrating or embedding thousands of transistors on a single silicon semiconductor microchip. In the context of its use in Fujii, the term "programmable LSI" can be understood as referring generally to a programmable semiconductor chip.

programmable logic element PL3. Notably, *all* of these embodiments disclose programmable logic elements comprised of individual circuitry components (e.g., control circuits, selectors, and transmission gates), *not* LUT units.

Fujii elaborates on the individual components that are required to build programmable logic element PL1 in paragraph (0015) in which it describes a collection of the following individual components: "Specifically, the programmable logic element PL1 includes memory circuits cell 00 to cell 15, selectors x00 to x14, selectors x16 to x20, x31, x32, CMOS transfer gates x22, x23, control circuits x15, x21, and inverters x24 to x30." *Id.* at (0015). Notably absent from this recitation is any mention of LUT units. Fujii discloses "memory circuit groups" but these groups do not comprise *structural* elements. Rather, they are *functional* groupings based on use modes of the total number of memory circuit groups provided in the programmable logic element.

Figure 6 of Fujii is "a diagram showing the correspondence between input and output signals in the programmable logic element PL1 and output signals of the memory circuit." *Id.* at (0037). It is important to note that this "diagram" is, in fact, simply a series of tables and *not* a circuit diagram showing a plurality of LUT units used to implement a larger look up table of M inputs and N outputs. These tables are simply logical *representations* (rather than any particular physical *implementation*) of the various memory circuit groups and an explanation of what

functionality the memory elements (*i.e.*, cells in PL1) would produce if grouped in a particular way.

Fujii provides a lengthy description of the operation of programmable logic element PL1. *See id.* at (0036)-(0052). Notably, nowhere in this description, or indeed anywhere else, does Fujii either teach or suggest any implementation for its programmable logic elements that utilizes a plurality of individual LUT units. Absent such a teaching or suggestion, Fujii also fails to teach or suggest a configuration control circuit for controlling an internal configuration of a plurality of LUT units. Rather, the scope of its disclosure is limited to teaching the use of individual logic components that collectively are used to build programmable circuits PL1, PL2, and PL3. *See id.* at (0015), (0059), (0082). Moreover, Fujii switches between operations using "control signals," including Figure 6 where Fujii shows different functionality of the logic element PL1 based on "control signals for determining the ***use mode*** of the programmable logic circuit PL1." *See id.* at (0038) (emphasis added). Fujii proceeds to explain in detail how to control the components of the element PL1 including selectors, control circuits, and transfer gates in order to produce the various functional modes in Figures 6(1), 6(2) and 6(3). *See id.* at (0038)-(0052).

C. Overview of Betz.

While Petitioner accords more to Fujii than it actually teaches, Petitioner concedes that Fujii fails to teach or suggest the use of a selector control circuit that has a memory, controlling the plurality of selectors in accordance with data stored in said memory, and defining the internal configuration of said plurality of LUT units. As a result, Petitioner proposes the combination of Fujii with Betz.

Betz is an FPGA textbook from the late 1990s that Petitioner cites for its general teachings regarding the use of certain types of switches that can be controlled in accordance with data stored in memory. *See* Exhibit 1006 at Fig. 2.2. According to Petitioner, Betz teaches that it was known to implement SRAM-based switches to control selection of inputs and outputs of look-up tables within a logic block. *Id.* at 214, Fig.B.8.

D. Overview of Chow.

Chow is a paper from 1999 that discusses various circuit-level design considerations for a particular test FPGA chip the authors call Logic that's Erasable and Greatly Optimized (LEGO). *See* Exhibit 1023 at 322. Chow states that "[t]hree techniques for programming the configuration bits were identified." *Id.* at 325. Petitioner makes much of the statement in Chow that "[t]he simplest is to connect all of the bits into a long shift register." *Id.* Indeed, Petitioner repeatedly quotes this passage in the Petition as if that were the preferred technique Chow selected for its

LEGO chip. Yet Petitioner fails to point out that this technique was actually disadvantageous and *not* chosen in Chow. *Id.* Indeed, it was found to be the slowest of all methods identified. *Id.*

E. Ground 1: Fujii in Combination with Betz Fails to Teach/Suggest Every Feature Recited in the Challenged Claims (Claims: 1-5, 7-11, and 13-16).

As noted above, Fujii is directed to a programmable logic element. The solution that Fujii proposes is a singular "programmable logic element capable of efficiently realizing a desired logic function by using fewer logic elements and less memory according to the logic function to be realized." Exhibit 1005 at (0009). There is no teaching or suggestion in Fujii of constructing a programmable logic element from a plurality of individual LUT units. Absent such a teaching or suggestion, there is also no teaching or suggestion in Fujii of constructing a programmable logic element with a configuration control circuit controlling an internal configuration of a plurality of LUT units.

Petitioner has asserted that Fujii discloses a plurality of LUT units "by teaching that PL1 has 'plural memory circuit groups.'" Petition at 18. Neither the memory circuits nor the memory circuit groups of Fujii are LUT units. Fujii is directed towards an implementation in the form of a single programmable logic element comprising a certain number of memory circuits which can be functionally grouped using control circuits, selectors, and transfer gates. Fujii's specific

teaching of how to implement a more efficient single unit describes such a single unit not in terms of a plurality of individual LUT units—as taught in the ’737 patent—but rather as a collection of the individual components that are required to build this single unit (i.e., control circuits, selectors, and transfer gates). *See* Exhibit 1005 at (0015), (0038)-(0052), (0059)-(0069), and (0079)-(0082). Fujii fails to teach or suggest a look up table comprising a plurality of LUT units.

A “look up table of M inputs and N outputs,” as taught by the ’737 patent, is not *divided* into LUT units, but rather *implemented* with a plurality of LUT units. According to Petitioner, for the embodiment of Fujii called PL1, “the 16 storage elements are divided into 4+4+8 (divided into 2^2+2^2+2^2), and the sequence $\{2^{[X]i}\}$ in this case is $\{2^2, 2^2, 2^3\}$.” Exhibit 1005 at (0051). Based on these groupings, Petitioner then concludes that PL1 has a top “2-LUT” with four memory circuits, a middle “2-LUT” with four memory circuits, and a bottom “3-LUT” with eight memory circuits. *See* Exhibit 1005 at FIG.6(2). As noted above, however, the tables of Figure 6 of Fujii are simply logical *representations* (rather than any particular physical *implementation*) of the various memory circuit groups and an explanation of what functionality the memory elements (*i.e.*, cells in PL1) would produce if grouped in a particular way.

Petitioner is engaging in box drawing on PL1 that explains the functionality in ***one*** particular use mode of operation (*i.e.*, the mode shown in Figure 6(2))

without regard to how these circuitry components are *actually constructed. See* Petition at 21. Petitioner obfuscates the issue by its focus on how *diagrams may be viewed* rather than on how *look up tables are actually designed and implemented*. Critically, Petitioner does not address Figures 6(1) and 6(3) of Fujii that would have, under Petitioner's flawed logic, different LUT units for the very same logic element PL1. In short, Petitioner confuses the *use modes* of Fujii with *implementation*. Regardless of the use mode, Fujii discloses a particular implementation for its programmable logic element, and that disclosure neither teaches nor suggests the use of a plurality of LUT units in constructing a look up table of M inputs and N outputs.

Petitioner also asserts that Fujii discloses "an internal configuration control circuit controlling an internal configuration of said plurality of LUT units" because it discloses a circuit that allows PL1 to "switch[] between three operations" or "use mode[s]." Petition at 25. According to Petitioner, this mode-switching is not materially different from the "controlling an internal configuration of said plurality of LUT units" described in the '737 patent. *Id.* at 33. But it is. The programmable logic element of Fujii uses a "plurality of selection circuits" that are "divided into a plurality of selection circuits," not a plurality of LUT units, in its logic element. Moreover, Fujii controls these selection circuits simply with control signals and not "an internal configuration control circuit." Lacking any teaching or suggestion of a

plurality of LUT units, Fujii is similarly lacking in any teaching or suggestion of a configuration control circuit controlling an internal configuration of a plurality of LUT units.

Petitioner combines Fujii with the teachings of Betz in order to assert that it was known that certain types of switches can be controlled in accordance with data stored in memory. *See* Exhibit 1006 at Fig. 2.2. From this, Petitioner asserts that the teachings of Fujii combined with Betz teach "a selector control circuit having a memory, controlling said plurality of selectors in accordance with data stored in said memory, and defining the internal configuration of said plurality of LUT units." Petition at 37. The addition of Betz fails to address the lack of any teaching or suggestion in Fujii of a plurality of LUT units or a configuration control circuit controlling an internal configuration of the plurality of LUT units. Thus, even if the memory-controlled selectors of Betz could be applied to the programmable logic elements of Fujii, the combination would still fail to teach or suggest a look up table of M inputs and N outputs comprising a plurality of LUT units and a configuration control circuit controlling an internal configuration of the plurality of LUT units.

F. Ground 3: Fujii in Combination with Betz and Chow Fails to Teach/Suggest Every Feature Recited in the Challenged Claims (Claims: 1-5, 7-11, and 13-16).

Petitioner asserts that, to the extent the phrase "a memory" in the challenged claims requires a *single* memory, Fujii in combination with Betz and Chow render the claims obvious. As noted above, the combination of Fujii and Betz fails to teach or suggest the claimed invention for reasons other than whether the memory recited in the claims must constitute a single memory. As a result, regardless of whether Chow provides sufficient disclosure of the use of a single memory, the shortcomings of the combination of Fujii with Betz remain.

As noted above, Chow states that "[t]hree techniques for programming the configuration bits were identified," and Petitioner makes much of the statement in Chow that "[t]he simplest is to connect all of the bits into a long shift register." Exhibit 1023 at 325. It bears repeating that this technique was found to be disadvantageous and *not* chosen in Chow. *Id.* Indeed, it was the slowest of all methods identified. *Id.* As a result of its perceived disadvantages, a person of ordinary skill in the art would *not* be motivated to modify the combination of Fujii with Betz with a technique known to be disadvantageous.

Fujii in combination with Betz and Chow fail to teach or suggest a look up table of M inputs and N outputs comprising a plurality of LUT units and a

configuration control circuit controlling an internal configuration of the plurality of LUT units.

G. Grounds 2 and 4: Fujii in Combination with Betz and General Knowledge of a POSITA (and optionally Chow) Fails to Teach/Suggest Every Feature Recited in the Challenged Claims (Claims: 6 and 12).

Grounds 2 and 4 pertain only to dependent claims 6 and 12, which depend from claims 1 and 7, respectively. Neither Grounds 2 or 4 cure any of the deficiencies identified above with respect to Grounds 1 and 3 as neither of them teach or suggest a look up table comprising a plurality of LUT units and a configuration control circuit controlling an internal configuration of the plurality of LUT units. As a result, both Grounds 2 and 4 suffer from the same fatal flaws as Grounds 1 and 3.

VIII. CONCLUSION

For the reasons stated above, the Board should deny institution of *inter partes* review. Pursuant to 35 U.S.C. § 314 and *Fintiv*, all of the relevant factors weigh against institution as doing so would cause the Board and the parties to incur significant expense and wasted efforts based on the overlap of parties and issues with District Court litigation that is scheduled for trial in advance of a final written decision. Further, Petitioner has not established a reasonable likelihood that it will

prevail on any ground presented in the Petition as the cited references fail to teach or suggest all of the limitations of the claims of the ’737 Patent.

Dated: August 28, 2023

Respectfully submitted,

/s/ *Joshua R. Slavitt*
Joshua R. Slavitt
Reg. No. 40,816
SLAVITT IP LAW, LLC
535 Hamilton Road
Merion Station, PA 19066
Phone: (215) 880-2569
Email: josh@slavittiplaw.com

Attorney for Patent Owner
Professor Masahiro Iida

CERTIFICATE OF COMPLIANCE WITH WORD COUNT

Pursuant to 37 C.F.R. § 42.24(d), I certify that this Preliminary Response complies with the type-volume limits of 37 C.F.R. § 42.24(b)(1) because it contains 8,503 words, excluding the parts of this Patent Owner's Preliminary Response that are exempted by 37 C.F.R. § 42.24(a), according to the word processing system used to prepare this Patent Owner's Preliminary Response.

Respectfully submitted,

Dated: August 28, 2023

By: /Joshua R. Slavitt/
Joshua R. Slavitt
Registration No. 40,816

Counsel for Patent Owner
Professor Masahiro Iida

CERTIFICATE OF SERVICE

The undersigned certifies that, pursuant to 37 C.F.R. § 42.6(e), a copy of the foregoing PATENT OWNER'S PRELIMINARY RESPONSE was served via email (as consented to by counsel) on August 28, 2023, to lead and backup counsel of record for Petitioner as follows:

Heather E. Takahashi (Reg. No. 78,418)
heather.takahashi@mto.com

Vincent Y. Ling (Reg. No. 67,145)
vincent.ling@mto.com

intel-iida-ipr@mto.com
Munger, Tolles & Olson LLP
350 S. Grand Ave. 50th Fl.
Los Angeles, CA 90071

Dated: August 28, 2023

By: /Joshua R. Slavitt/
Joshua R. Slavitt
Registration No. 40,816

Counsel for Patent Owner
Professor Masahiro Iida