

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,
Petitioner,

v.

MASAHIRO IIDA,
Patent Owner.

Case No. IPR2023-00864
U.S. Patent No. 6,812,737

**PETITIONER'S AUTHORIZED REPLY
TO PATENT OWNER'S PRELIMINARY RESPONSE**

TABLE OF EXHIBITS

Exhibit No.	Description
1001	U.S. Patent No. 6,812,737
1002	Prosecution History of U.S. Patent No. 6,812,737
1003	Declaration of Stephen W. Melvin, Ph.D.
1004	Curriculum Vitae of Stephen W. Melvin, Ph.D.
1005	Japanese Unexamined Patent Application Publication No. H09-121153A (“Fujii”), certified translation, and declaration of translator
1006	Vaughn Betz et al., <i>Architecture and CAD for Deep-Submicron FPGAs</i> (Kluwer Academic Publishers 1999) (“Betz”)
1007	U.S. Patent No. 6,097,212 (“Agrawal”)
1008	U.S. Patent No. 5,926,036 (“Cliff”)
1009	Declaration of Agnes O. Villero Regarding Betz, Brown-FPGA, Trimberger, and Bhat
1010	Prosecution History of Japanese Patent Application No. 2001-199644 (which issued as Japanese Patent No. 3580785B2), certified translation, and declaration of translator
1011	Stephen D. Brown et al., <i>Field-Programmable Gate Arrays</i> (Kluwer Academic Publishers 1992) (“Brown-FPGA”)
1012	Stephen M. Trimberger et al., <i>Field-Programmable Gate Array Technology</i> (Springer Science+Business Media New York 1994) (“Trimberger”)
1013	Stephen Brown & Jonathan Rose, “FPGA and CPLD Architectures: A Tutorial,” <i>IEEE Design and Test of Computers</i> , vol. 13, no. 2, 42-57 (Dec. 1996) (“Brown-Rose”) (from pages 4-19 of Declaration of Gordon MacPherson at Ex.1014)
1014	Declaration of Gordon MacPherson regarding Stephen Brown & Jonathan Rose, “FPGA and CPLD Architectures: A Tutorial,” <i>IEEE Design and Test of Computers</i> , vol. 13, no. 2, 42-57 (Dec. 1996)
1015	Jianshe He & Jonathan Rose, “Advantages of Heterogeneous Logic Block Architectures for FPGAs,” <i>Proceedings of IEEE Custom</i>

Exhibit No.	Description
	<i>Integrated Circuits Conference - CICC '93</i> (1993) (“He”) (from pages 4-8 of Declaration of Gordon MacPherson at Ex.1016)
1016	Declaration of Gordon MacPherson regarding Jianshe He & Jonathan Rose, “Advantages of Heterogeneous Logic Block Architectures for FPGAs,” <i>Proceedings of IEEE Custom Integrated Circuits Conference - CICC '93</i> (1993) (from pages 4-8 of Declaration of Gordon MacPherson)
1017	Jonathan Rose et al., “Architecture of Field-Programmable Gate Arrays,” <i>Proceedings of the IEEE</i> , vol. 81, no. 7, 1013-29 (July 1993) (“Rose”) (from pages 4-20 of Declaration of Gordon MacPherson at Ex.1018)
1018	Declaration of Gordon MacPherson regarding Jonathan Rose et al., “Architecture of Field-Programmable Gate Arrays,” <i>Proceedings of the IEEE</i> , vol. 81, no. 7, 1013-29 (July 1993)
1019	Satwant Singh et al., <i>The Effect of Logic Block Architecture on FPGA Performance</i> , IEEE Journal of Solid-State Circuits, vol. 27, no. 3, 281-87 (Mar. 1992) (“Singh”) (from pages 4-10 of Declaration of Gordon MacPherson at Ex.1020)
1020	Declaration of Gordon MacPherson regarding Satwant Singh et al., <i>The Effect of Logic Block Architecture on FPGA Performance</i> , IEEE Journal of Solid-State Circuits, vol. 27, no. 3, 281-87 (Mar. 1992)
1021	Narasimha B. Bhat, “Novel Techniques for High Performance Field Programmable Logic Devices,” Technical Report no. UCB/ERL M93/80, Electronic Research Laboratory, University of California, Berkeley (Nov. 1993) (“Bhat”)
1022	Donald W. Cherepacha, Master’s Thesis, <i>A Field-Programmable Gate Array Architecture Optimized for Datapaths</i> , Department of Electrical and Computer Engineering, University of Toronto (1994) (“Cherepacha”)
1023	Paul Chow et al., “The Design of a SRAM-Based Field-Programmable Gate Array—Part II: Circuit Design and layout,” in <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , vol. 7, no. 3, pp. 321-330, Sept. 1999 (“Chow”) (from pages 4-13 of Declaration of Gordon MacPherson at Ex.1024)

Exhibit No.	Description
1024	Declaration of Gordon MacPherson regarding Paul Chow et al., “The Design of a SRAM-Based Field-Programmable Gate Array—Part II: Circuit Design and layout,” in <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , vol. 7, no. 3, pp. 321-330, Sept. 1999
1025	U.S. Patent No. 5,905,385 (“Sharpe-Geisler”)
1026	Excerpt of Tom M. Apostol, <i>Calculus, Volume I</i> (Wiley 1967) (“Apostol”)
1027	<i>Principles and Structures of FPGAs</i> (Hideharu Amano, ed., Springer 2018) (“Amano”)
1028	Jason Cong et al., “Technology Mapping For k/m -Macrocell Based FPGAs,” in <i>Proceedings of the 2000 ACM/SIGDA 8th Int’l Symposium on Field Programmable Gate Arrays</i> , 51-59 (Feb. 2000) (“Cong”)
1029	Plaintiff’s Preliminary Infringement Contentions in <i>Iida v. Intel Corp.</i> , No. 6:22-cv-00662-ADA (W.D. Tex.)
1030	Complaint in <i>Masahiro Iida v. Intel Corporation and Intel K.K.</i> , filed July 4, 2022, in the Department of Intellectual Property Rights, Tokyo District Court, certified translation, and declaration of translator
1031	Intel’s Opening Claim Construction Brief in <i>Iida v. Intel Corp.</i> , No. 6:22-cv-00662-ADA (W.D. Tex.)
1032	Iida’s Responsive Claim Construction Brief in <i>Iida v. Intel Corp.</i> , No. 6:22-cv-00662-ADA (W.D. Tex.)
1033	Declaration of Dr. Marwan Hassoun in support of Professor Masahiro Iida’s Responsive Claim Construction Brief in <i>Iida v. Intel Corp.</i> , No. 6:22-cv-00662-ADA (W.D. Tex.)
1034	Intel’s Reply Claim Construction Brief in <i>Iida v. Intel Corp.</i> , No. 6:22-cv-00662-ADA (W.D. Tex.)
1035	Iida’s Sur-Reply Claim Construction Brief in <i>Iida v. Intel Corp.</i> , No. 6:22-cv-00662-ADA (W.D. Tex.)
1036	Joint Claim Construction Statement in <i>Iida v. Intel Corp.</i> , No. 6:22-cv-00662-ADA (W.D. Tex.)
1037	USPTO Memorandum, Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation (June

Exhibit No.	Description
	21, 2022), available at https://www.uspto.gov/sites/default/files/documents/interim_proc_discretionary_denials_aia_parallel_district_court_litigation_memo_20220621_.pdf (“Guidance Memo”)
1038	U.S. District Courts – National Judicial Caseload Profile (Dec. 2022), obtained at https://www.uscourts.gov/statistics-reports/analysis-reports/federal-court-management-statistics , per Guidance Memo at n.4
1039	Scheduling Order dated Oct. 14, 2022, in <i>Iida v. Intel Corp.</i> , No. 6:22-cv-00662-ADA (W.D. Tex.)
1040	Japanese Patent No. 3580785B2, certified translation, and declaration of translator
1041	Iida’s Brief filed March 20, 2023, in <i>Masahiro Iida v. Intel Corporation and Intel K.K.</i> , filed July 4, 2022, in the Department of Intellectual Property Rights, Tokyo District Court, certified translation, and declaration of translator, certified translation, and declaration of translator
1042	Order to Stay Case dated March 14, 2023, in <i>Iida v. Intel Corp.</i> , No. 6:22-cv-00662-ADA (W.D. Tex.)
1043	Andrew S. Tanenbaum, <i>Structured Computer Organization</i> (2d ed. 1984) (“Tanenbaum”)
1044	Neil H.E. Weste & Kamran Eshraghian, <i>Principles of CMOS VLSI Design: A Systems Perspective</i> (1985) (“Weste”)
1045	<i>Sotera</i> Stipulation
1046	U.S. District Courts – National Judicial Caseload Profile (June 2023), obtained at https://www.uscourts.gov/statistics-reports/analysis-reports/federal-court-management-statistics , per Guidance Memo at n.4

Petitioner submits this Reply to Patent Owner’s Preliminary Response (“POPR”) (Paper 7). As explained in the Petition (Paper 2, 84-86), and further below, the *Fintiv* factors favor institution.

In particular, given new developments in the district court litigation—namely, that the stay in the district court litigation in effect at the time the Petition was filed was lifted on July 27, 2023, and a new trial date was set—Petitioner provided Patent Owner with a *Sotera* stipulation after the POPR was filed. Ex.1045. In Patent Owner’s own words, that stipulation “ensure[s] that an *inter partes* review would be a ‘true alternative’ to the district court proceeding.” POPR, 25 n.5. Pursuant to the Director’s June 21, 2022 Memorandum (“Guidance Memo”), this alone prevents discretionary denial under *Fintiv*. See Ex.1037, 7-8.

Factor 1 (Stay): Based on two cherry-picked decisions, Patent Owner claims “there is no evidence” a stay would be granted if review were instituted. POPR, 19-20. But the judge in the pending district court litigation, the Honorable Alan Albright, has stayed litigation pending instituted IPRs in instances where, as here, the instituted claims would cover every claim asserted in the district court. See, e.g., *Sonrai Memory Ltd. v. W. Digital Techs., Inc.*, No. 6:21-CV-01168-ADA, 2022 WL 3108818, at *5 (W.D. Tex. Aug. 4, 2022); *Lone Star SCM Sys. v. Zebra Techs. Corp.*, No. 6:21-cv-842-ADA, 2023 WL 4923962, at *5 (W.D. Tex. July 31, 2023).

Factor 2 (Trial Proximity): Patent Owner cites several years-old decisions (all of which predate the Guidance Memo), arguing this factor weighs in favor of denial because the *current* district court schedule places trial before the statutory deadline. POPR, 21-22. Not so. The Board’s analysis on this factor turns on median time-to-trial statistics. *See* Guidance Memo, 8-9. Here, the “median time-to-trial is around the same time” as the statutory deadline (November 28, 2024), so this factor weighs against discretionary denial. *Id.*, 9; *see* Petition, 84-85 (citing Ex.1038, which identifies the median time to trial in the Western District of Texas as 29.5 months, placing trial in December 2024).¹ Additionally, Petitioner filed its Petition on April 20, 2024, within its statutory deadline of June 24, 2024.

Factors 3 (Investment in Parallel Proceedings), 4 (Overlap), and 5 (Same Parties): These factors are tailored to “avoid duplicative efforts between the” Board and district court. *See* POPR, 6 (discussing factors 3 and 5), 7-8 (discussing factor 4). Because Petitioner agreed to a *Sotera* stipulation, Ex.1045, there will be no overlap between the district court and Board proceedings. *See id.*, 7-8. What is more, Petitioner challenges all 16 claims of the ’737 patent, while Patent Owner has

¹ Although the most recent statistics identify a median time to trial of 26.4 months, the resulting trial date would still be “around the same time” as the final written decision deadline—falling in September 2024. *See* Ex.1046.

asserted only seven claims in the district court litigation (claims 1, 2, 7, 8, 13, 14, and 15). *See* Ex.1029 at 2. Moreover, when the Board issues its institution decision, investment in the district court case will have been minimal, as the parties will not yet have completed fact discovery, prepared expert reports, or filed summary judgment motions. Thus, these factors collectively weigh against discretionary denial.

Factor 6 (Compelling Merits): Patent Owner's argument on this factor is nothing more than a nod at his assertions on the merits. POPR, 27-28. Those assertions fail to undermine the extensive, detailed analysis presented in the Petition and the supporting expert declaration (Ex.1003).

In sum, even if Petitioner's *Sotera* stipulation were not outcome-determinative, the *Fintiv* factors collectively weigh against discretionary denial.

Dated: September 12, 2023

Respectfully submitted,

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CERTIFICATE OF SERVICE UNDER 37 C.F.R. §42.6(e)(4)

I hereby certify that on September 12, 2023, I will cause a copy of the foregoing document, including any exhibits filed therewith, to be served via electronic mail, as previously consented to by Patent Owner, upon the following:

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