

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,
Petitioner,

v.

MASAHIRO IIDA,
Patent Owner.

IPR2023-00864
Patent 6,812,737 B2

Before JEAN R. HOMERE, DANIEL J. GALLIGAN, and
STEPHEN E. BELISLE, *Administrative Patent Judges*.

HOMERE, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. Background

Intel Corporation (“Petitioner”) filed a Petition for *inter partes* review of claims 1–16 of U.S. Patent No. 6,812,737 B2 (Ex. 1001, “the ’737 patent”). Paper 2 (“Pet.”), 1. Masahiro Iida (“Patent Owner”) filed a Preliminary Response. Paper 7 (“PO Prelim. Resp.”). Pursuant to the Board’s email authorization on September 5, 2023, Petitioner filed a Preliminary Reply (Paper 8, “Pet. Prelim. Reply”) and Patent Owner filed a Preliminary Sur-reply (Paper 9, “PO Prelim. Sur-reply”).

Institution of an *inter partes* review is authorized by statute only when “the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a) (2018). We have authority, acting on the designation of the Director, to determine whether to institute an *inter partes* review under 37 C.F.R. § 42.4(a).

Based on the current record, and for the reasons explained below, we determine that Petitioner has established a reasonable likelihood that it would prevail with respect to at least one challenged claim. Accordingly, we institute *inter partes* review.

B. Real Parties in Interest

Petitioner and Patent Owner identify themselves as the real parties in interest. Pet. 1; Paper 4, 1.

C. Related Matters

The parties indicate that the '737 patent is the subject of the following district court proceeding:

Masahiro Iida v. Intel Corp., Case No. 6:22-cv-00662-ADA
(W.D. Tex.) (“the Texas litigation”).

Pet. 1; Paper 4, 1.

Petitioner also notes that the '737 patent claims priority to a Japanese application that issued as Japanese Patent No. 3,580,785 (“JP '785 patent”), and Patent Owner has asserted the JP '785 patent against Petitioner in the Tokyo District Court, Intellectual Property Division, in *Iida v. Intel Corp. and Intel K.K.*, Case No. 19129 (Wa) of 2022. Pet. 1–2.

D. The Challenged '737 Patent

The '737 patent is titled “Programmable Logic Circuit Device Having Look Up Table Enabling to Reduce Implementation Area,” and relates to “an architectural technology for configuring a look up table that enables implementation area to be reduced.” Ex. 1001, code (54), 1:8–11. Figure 1 of the '737 patent, reproduced below, shows field programmable gate array (FPGA) 100 as an example of a programmable logic circuit device (PLD) including a look up table (LUT). *Id.* at 3:1–2.

Fig.1

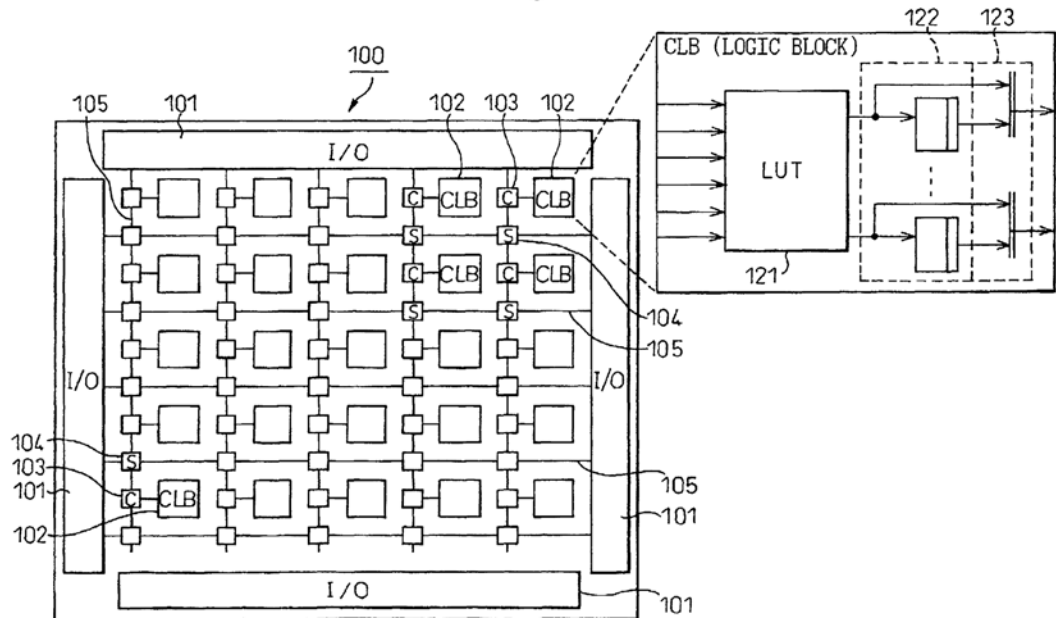
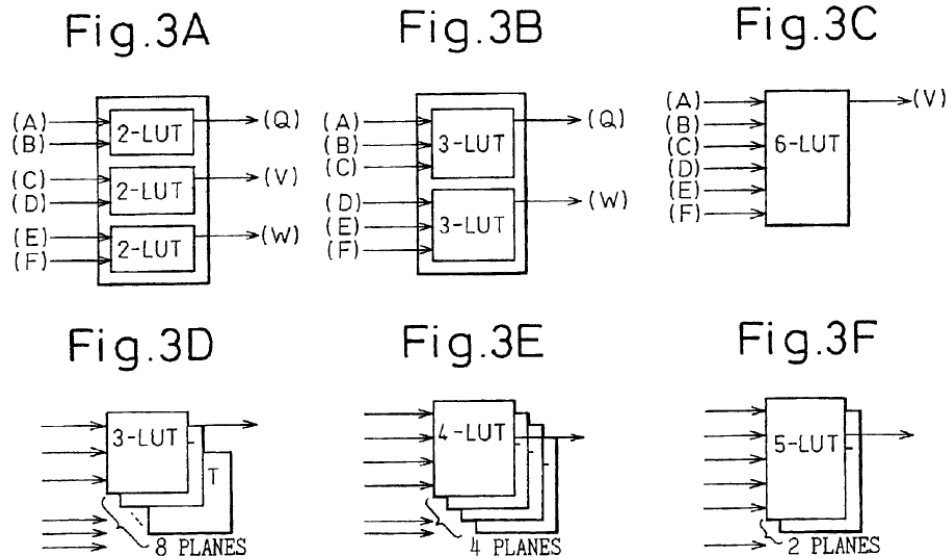


Figure 1 above depicts FPGA 100 including configurable logic blocks (CLB) 102, input/output (I/O) blocks 101, switch circuits (S) 104, and connection blocks 103 connected together via routing wires 105, enabling input/output (I/O) blocks 101 to perform an I/O operation with an external equipment. *Id.* at 3:61–4:1. Each CLB 102 includes LUT 121 with M inputs and N outputs, latches 122, selector 123, as well as a control circuit for controlling an internal configuration of LUT 121. *Id.* at 4:1–3.

Figures 3A–3F of the '737 patent, reproduced below, illustrate different modes of internal configuration of an exemplary LUT (6-input 3-output LUT), showing that by varying values (X, Y, Z) of mode changing memory (71, shown in Figure 6, *infra*), the LUT can be set to different internal configurations. *Id.* at 4:12–17.



Figures 3A–3F illustrate different modes of internal configuration of an exemplary LUT (a 6-input 3-output LUT). *Id.* at 3:5–8, 4:12–17.

Figure 3A above illustrates a case where the 6-input 3-output LUT is set to a mode where it is configured as three 2-input 1-output LUTs. *Id.* at 4:18–19. The '737 patent explains that in a conventional FPGA (composed of 4-input 1-output LUTs), three LUTs (4-input 1-output LUTs) are required to assign three 2-input 1-output circuits. *Id.* at 20–23. In the configuration shown in Figure 3A, only one 6-input 3-output LUT needs to be used for this purpose. *Id.* at 4:23–25. The chip area ratio of a 4-input 1-output LUT to a 6-input 3-output LUT, including the routing channel area, is about 1:1.5. *Id.* at 4:26–27. Therefore (in accordance with the '737 patent), as compared to the conventional configuration using three 4-input 1-output LUTs, the configuration shown in Figure 3A can reduce the circuit area ratio to about $(1 \times 3):1.5$ or by about 50%. *Id.* at 4:26–33.

Figure 3B above illustrates a case where the LUT is set to a mode where it is configured as two 3 input 1-output LUTs such that, when compared to the conventional configuration where two 4-input 1-output

LUTs are used, the circuit area ratio (in accordance with Figure 3B) can be reduced to $(1 \times 2):1.5$ or by about 25%. *Id.* at 4:33–39. Figure 3C above shows a further case where the 6-input 3-output LUT is set to a mode where it is configured as a single 6-input 1-output LUT; Figure 3D above shows a case where the 6-input 3-output LUT is set to a mode of 3-input 1-output LUT $\times 8$ planes; Figure 3E shows a case where the 6-input 3-output LUT is set to a mode of 4-input 1-output LUT $\times 4$ planes, and Figure 3F shows a case where the 6-input 3-output LUT is set to a mode of 5-input 1-output LUT $\times 2$ planes. *Id.* at 4:39–48.

Figure 6 of the '737 patent, reproduced below, is a block diagram illustrating an example of an internal configuration of the exemplary 6-input 3-output LUT described above. *Id.* at 3:14–16, 5:24–26.

Fig.6

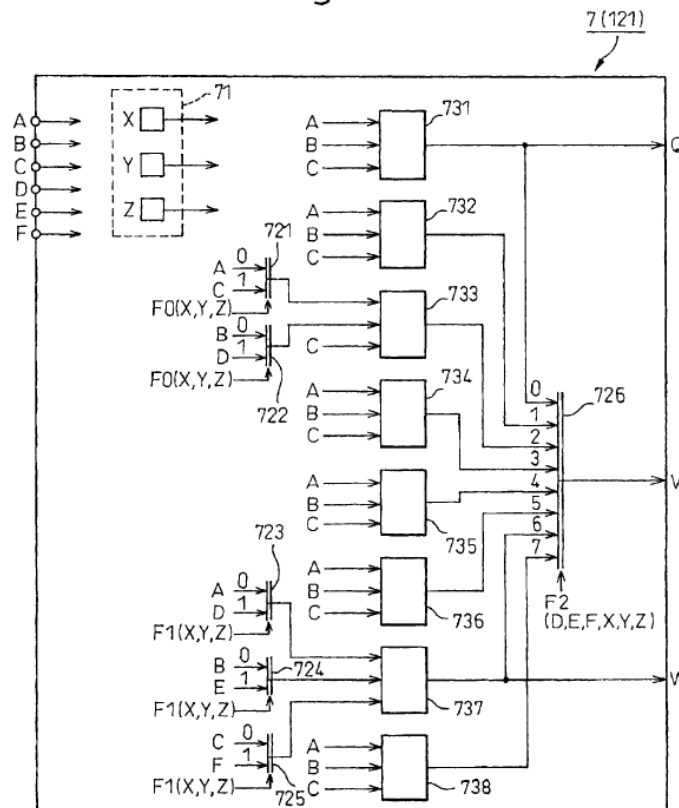


Figure 6 depicts a block diagram illustrating an example of an internal configuration of exemplary 6-input 3-output LUT 121 including mode changing memory 71, selectors 721–725, and 3-input 1-output LUT units (memory array) 731~738. *Id.* at 3:14–16, 5:24–33.

As shown in Figure 6, mode changing memory 71 stores 3 bits of data X, Y, Z provided by a user to set the relationship between a 6-bit input A~F and a 3 bit output Q, V, W, in accordance with the user's request. *Id.* at 5:24–33. A predetermined signal (i.e., subset of bits) within the 6-bit input signal is input to each selector (a selector for selecting the input signal) 721~725, so as to select the input signal in accordance with data stored in mode changing memory 71. *Id.* at 5:34–45. That is, signals A and C are input to selector 721 and signals B and D are input to selector 722, and one of each pair of signals is selected by selection signal F0 (X, Y, Z) specified by the data X, Y, Z, and is output to a respective input of 3-input 1-output LUT 733. *Id.* Similarly, signals A and D are input to selector 723, signals B and E are input to selector 724, and signals C and F are input to selector 725, and one of each pair of signals is selected by selection signal F1 (X, Y, Z) specified by the data X, Y, Z, and is output to a respective input of 3-input 1-output LUT 737. *Id.*

Each of the 3-input 1-output LUTs 731~738 includes an address decoder, a memory, and a selector, and outputs a 1-bit signal in response to a 3 bit input signal, respectively. *Id.* at 5:46–49. Input signals A, B, and C are input to each of LUTs 731, 732, 734~736, and 738; one of the signals A and C and one of the signals B and D, selected by selection signal F0 as discussed above, and signal C are input to LUT 733; one of the signals A and D, one of the signals B and E, and one of the signals C and F, selected by selection signal F1 as discussed above, are input to LUT 737. *Id.* at

5:46–55. Output signals from LUTs 731–738 are input to a selector 726, and one of the signals is selected by selection signal F2 (D, E, F, X, Y, Z) specified by input signals D, E, F and by data X, Y, Z, and is output as signal V. *Id.* at 5:55–60. Signal Q is the output signal from LUT 731, and signal W is the output signal from LUT 737. *Id.* at 5:60–61. “[B]y varying the values (X, Y, Z) of mode changing memory (71),” which control selectors 721–726, “the 6-input 3-output LUT can be set to different internal configurations as shown in Figures 3A to 3F,” above. *Id.* at 4:12–17.

E. The Challenged Claims

Petitioner challenges claims 1–16 of the ’737 patent. Pet. 1. Claims 1, 7, and 13 are independent. Claim 1 is illustrative of the challenged claims and is reproduced below.

1. [1PRE] A look up table of M inputs and N outputs, comprising:
[1A] a plurality of LUT units; and
[1B] an internal configuration control circuit controlling an internal configuration of said plurality of LUT units, [1C] wherein said internal configuration control circuit comprises
a plurality of selectors selecting I/O signals of said plurality of LUT units, and
[1D] a selector control circuit having a memory, controlling said plurality of selectors in accordance with data stored in said memory, and defining the internal configuration of said plurality of LUT units.

Ex. 1001, 9:51–63 (bracketed designations added by Petitioner (*see* Pet. 88)).

F. Prior Art and Asserted Grounds of Unpatentability

The Petition relies on the following prior art references:

Name	Reference	Exhibit
Fujii	Japanese Unexamined Patent Application Publication No. H9-121153A, published May 6, 1997	1005
Betz	Vaughn Betz et al., <i>Architecture and CAD for Deep-Submicron FPGAs</i> (Kluwer Academic Publishers 1999)	1006
Chow	Paul Chow et al., <i>The Design of a SRAM-Based Field-Programmable Gate Array—Part II: Circuit Design and Layout</i> , IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 7, No. 3, 321–330 (Sept. 1999)	1023

Petitioner asserts claims 1–16 are unpatentable based on the following grounds (Pet. 1):

Claim(s) Challenged	35 U.S.C. §	Reference(s)
1–16	103(a) ¹	Fujii, Betz ²

¹ The application resulting in the '737 patent was filed on June 28, 2002—a date prior to the date when the Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112–29, 125 Stat. 284 (2011), took effect. Thus, we refer to the pre-AIA version of section 103.

² Petitioner lists separate obviousness grounds for claims 6 and 12 based on combinations of prior art references with “the general knowledge of a [person of ordinary skill in the art].” Pet. 4. Because “the inquiry into whether any ‘differences’ between the invention and the prior art would have rendered the invention obvious to a skilled artisan necessarily depends on such artisan’s knowledge,” *Koninklijke Philips N.V. v. Google LLC*, 948 F.3d 1330, 1337 (Fed. Cir. 2020), we do not list those grounds separately.

Claim(s) Challenged	35 U.S.C. §	Reference(s)
1–16	103(a)	Fujii, Betz, Chow

Pet. 4. Petitioner submits a declaration of Stephen W. Melvin, Ph.D. (Ex. 1003, “Melvin Declaration”) in support of its contentions.

II. DISCRETIONARY DENIAL OF INSTITUTION

Patent Owner contends that we should exercise our discretion to deny institution under 35 U.S.C. § 314(a) in light of the Texas litigation. Prelim. Resp. 18–28. Patent Owner contends that the factors identified in *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (PTAB Mar. 20, 2020) (precedential) (“*Fintiv*”), weigh against institution. *Id.*

On June 21, 2022, the Director of the U.S. Patent and Trademark Office (“USPTO”) issued a Memorandum titled “Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings With Parallel District Court Litigation” (“Memorandum”),³ which states, among other things, that “the PTAB will not discretionarily deny institution in view of parallel district court litigation where a petitioner presents a stipulation not to pursue in a parallel proceeding the same grounds or any grounds that could have reasonably been raised before the PTAB.” Memorandum 3 (citing *Sotera Wireless, Inc. v. Masimo Corp.*, IPR2020-01019, Paper 12 (PTAB Dec. 1, 2020) (precedential as to § II.A)).

On September 1, 2023, Petitioner submitted the following stipulation in a letter to Patent Owner:

³ The Memorandum is available at https://www.uspto.gov/sites/default/files/documents/interim_proc_discretionary_denials_aia_parallel_district_court_litigation_memo_20220621_.pdf.

I write to inform you that Petitioner Intel Corporation hereby stipulates that, if the Patent Trial and Appeal Board institutes an inter partes review (“IPR”) proceeding for U.S. Patent No. 6,812,737 on the grounds presented in Intel’s Petition in IPR2023-00864, Intel will not pursue an invalidity defense in the above-referenced district court litigation that the patent claims subject to the instituted IPR are invalid based on grounds that were raised or reasonably could have been raised during the IPR.

Ex. 1045 (emphasis omitted).

Petitioner replies that, pursuant to the Director’s memorandum, this submission is a *Sotera* stipulation, which prevents discretionary denial under *Fintiv*. Pet. Prelim. Reply 1. Patent Owner responds that “Petitioner’s counsel’s letter (Exhibit 1045) falls short as an enforceable *Sotera* stipulation as Petitioner ha[d] not filed it as part of the record in the parallel proceeding pending in the Western District of Texas.” PO Prelim.

Sur-reply 1. According to Patent Owner,

While the language in this letter is consistent with that of *Sotera*, the critical difference is that the petitioner in *Sotera* actually offered the Board an enforceable stipulation insofar as it had been filed as part of the record in the District Court. *See Sotera Wireless, Inc. v. Masimo Corporation*, IPR2020-01019, Paper 12 at 13. Filing is what elevated a proposed undertaking to an enforceable stipulation. No such comparably enforceable stipulation has been offered by Petitioner in the present case. Simply put, Exhibit 1045 does not constitute an enforceable *Sotera* stipulation. It is “without effect.”

Id. at 2–3.

Further, on September 20, 2023, Petitioner submitted in the Texas litigation “**Intel’s *Sotera* Stipulation Regarding Invalidity Contentions**,” which states the following:

Intel stipulates that, if the Patent Trial and Appeal Board institutes an IPR proceeding for U.S. Patent No. 6,812,737 on the grounds presented in Intel’s Petition in IPR2023-00864, Intel will not pursue an invalidity defense in the above-captioned district court litigation that the patent claims subject to the instituted IPR are invalid based on grounds that were raised or reasonably could have been raised during the IPR.”

Ex. 1047, 1.

Patent Owner’s arguments are moot in light of Petitioner’s filing of the stipulation with the District Court. Ex. 1047. Therefore, we decline to exercise our discretion to deny institution in this proceeding under *Fintiv* in accordance with the Memorandum.

III. PATENTABILITY ANALYSIS

A. Principles of Law

1. Inter Partes Review

“In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)). Petitioner bears the burden of persuasion to prove unpatentability of each challenged claim by a preponderance of the evidence. 35 U.S.C. § 316(e). This burden never shifts to Patent Owner. *Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015). The Board may authorize an *inter partes* review if we determine that the information presented in the Petition

and Patent Owner's Preliminary Response shows that there is a reasonable likelihood that Petitioner will prevail with respect to at least one of the claims challenged in the petition. 35 U.S.C. § 314(a).

2. Obviousness

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art, (2) any differences between the claimed subject matter and the prior art, (3) the level of skill in the art, and (4) when in evidence, any objective evidence of nonobviousness.⁴ *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

A patent claim “is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art.” *KSR*, 550 U.S. at 418. An obviousness determination requires finding “both ‘that a skilled artisan would have been motivated to combine the teachings of the prior art references to achieve the claimed invention, and that the skilled artisan would have had a reasonable expectation of success in doing so.’” *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359,

⁴ At this stage of the proceeding, the parties have not directed us to any such objective evidence.

1367–68 (Fed. Cir. 2016) (citation omitted); *see KSR*, 550 U.S. at 418. Further, an assertion of obviousness “cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.” *KSR*, 550 U.S. at 418; *In re NuVasive, Inc.*, 842 F.3d 1376, 1383 (Fed. Cir. 2016) (a finding of a motivation to combine “must be supported by a ‘reasoned explanation’” (citation omitted)).

At this preliminary stage, we determine whether the information presented in the Petition shows there is a reasonable likelihood that Petitioner would prevail in establishing that at least one of the challenged claims would have been obvious over at least one of the proposed combinations of prior art.

B. Level of Ordinary Skill in the Art

The level of ordinary skill in the art is “a prism or lens” through which we view the prior art and the claimed invention. *Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001). The person of ordinary skill in the art is a hypothetical person presumed to have known the relevant art at the time of the invention. *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995). In determining the level of ordinary skill in the art, we may consider certain factors, including: “(1) the educational level of the inventor; (2) type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the technology; and (6) educational level of active workers in the field.” *Best Med. Int’l, Inc. v. Elekta Inc.*, 46 F.4th 1346, 1353 (Fed. Cir. 2022) (citations omitted). “The patent’s purpose can also be informative.” *Id.*

Petitioner contends that a person having ordinary skill in the art at the time of the invention

would have had a bachelor's degree in electrical engineering, computer engineering, or an equivalent degree, and one year of professional experience relating to PLDs or FPGAs. More education could substitute for experience, and vice versa. This person would have been capable of understanding and applying the '737 patent's teachings and would have had a working knowledge of PLDs, including prior art describing look-up table designs.

Pet. 8 (citing Ex. 1003 ¶¶ 29–34; Ex. 1033 ¶ 32).

Patent Owner does not contest Petitioner's proffered definition of the level of ordinary skill in the art or offer a definition of its own. *See* PO Prelim. Resp. 18 (“For purposes of this preliminary response only, the Patent Owner applies Petitioner's definition.”).

We find Petitioner's proposal is consistent with the problems and solutions disclosed in the '737 patent and prior art of record, and adopt it as our own for purposes of this Decision. *See, e.g., In re GPAC Inc.*, 57 F.3d at 1579 (approving the determination of the level of ordinary skill in the art by appeal to the references of record).

C. Claim Construction

We apply the same claim construction standard used in district court actions under 35 U.S.C. § 282(b), namely that articulated in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). *See* 37 C.F.R. § 42.100(b). In applying that standard, claim terms generally are given their ordinary and customary meaning as would have been understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire

patent disclosure. *Phillips*, 415 F.3d at 1312–13. “In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence.” *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17).

Petitioner presents the parties’ claim construction positions from the Texas litigation for the claim terms “look up table of M inputs and N outputs” and “LUT units.” Pet. 8–9. Petitioner submits that the parties agree that a “look up table of M inputs and N outputs” is a “component that is composed of memories and is capable of implementing an arbitrary logic circuit of M inputs on at least one of N outputs.” Pet. 9–11 (citing Ex. 1003 ¶¶ 71–73; Ex. 1032, 3–4, 7–11; Ex. 1035, 1–2; Ex. 1033, ¶¶ 21, 23). With respect to the claim term “LUT units,” Petitioner explains that in the Texas litigation, Petitioner has argued that “*LUT units*” are smaller look-up tables into which a larger “*look up table*” may be divided, while Patent Owner contends that the plain-and-ordinary meaning of “LUT unit” is “an individual LUT that cannot be fractured or divided *into smaller LUT units*.” Pet. 11 (citing Ex. 1003 ¶ 74; Ex. 1035, 3). Petitioner then submits that “the Board need not resolve this dispute because the challenged claims are unpatentable under either construction.” *Id.*

Patent Owner responds that on August 21, 2023, the District Court in the Texas litigation entered a claim construction order according both of these claim terms their plain and ordinary meanings. PO Prelim. Resp. 16 (citing Ex. 2005).

Our reviewing court states, “the ‘ordinary meaning’ of a claim term is its meaning to the ordinary artisan after reading the entire patent.” *Phillips*, 415 F.3d at 1321. In this case, the ’737 patent recites in relevant parts the following:

In a programmable logic circuit device, the number of bits M of input signal for the logic circuit that can be implemented corresponds to the number of bits of the address of memory composing the LUT, and the number of bits N of output signal corresponds to the number of output bits of the memory. Thus, a logic circuit that can be implemented in one LUT is an arbitrary logic circuit of M inputs and N outputs. Such a LUT is denoted in the present specification as M-input N-output LUT.

Ex. 1001, 1:46–54.

As shown in FIG. 6, the 6-input 3-output LUT 7 (121) is comprised of a mode changing memory 71, selectors 721-726, and [eight] 3-input 1-output LUT units (memory array) 731-738. The mode changing memory 71 stores 3 bits [of] data X, Y, Z designated by a user so as to set the relation between 6 bit input A-F and 3 bit output Q, V, W in accordance with [a] user’s request.

Ex. 1001, 5:26–33.

For purposes of this Decision, consistent with the ’737 patent, we determine that the plain and ordinary meaning of “look up table of M inputs and N outputs” refers to “a memory having 2^M entries (addressable locations), each of which stores an N-bit word, wherein the memory is capable of implementing an arbitrary logic circuit of M inputs and N outputs.” We likewise determine that the plain and ordinary meaning of “LUT unit” refers to a “unit of an LUT, wherein the unit constitutes a memory.” *Id.*

We note that this determination does not preclude the parties from arguing their proposed constructions of the claims during trial. Indeed, the parties are hereby given notice that claim construction, in general, is an issue to be addressed at trial. The parties are therefore encouraged to further develop these arguments during trial. A final determination as to claim construction will be made at the close of the proceeding, after any hearing, based on all the evidence of record.

For purposes of this Decision, we determine that no other terms need express construction. *See Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (“The Board is required to construe ‘only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

D. Overview of the Asserted Prior Art

1. Fujii (Ex. 1005)

Fujii relates to “a programmable logic element, which is a unit for implementing logic functions in a programmable LSI whose logic functions can be programmed by a user.” Ex. 1005 ¶ 1.

Fujii provides an example of a conventional FPGA, which is a conventional RAM-type programmable LSI and includes logic elements arranged in an array, with “a circuit element characterized by the number of inputs K called a LUT (Look Up Table) [being] mainly used” for the logic element. *Id.* ¶¶ 2–5; Fig. 22. The K-input, 1-output LUT is a 2^K -word, 1-bit memory, and by rewriting the contents of the internal SRAM, it is possible to implement an arbitrary logic function with K inputs and 1 output. *Id.* ¶ 5.

On the FPGA, a plurality of LUTs having the same number of inputs are arrayed, with the number of inputs of the LUT often being 3–5. *Id.* Fujii describes a problem with these conventional FPGAs in which K-input LUTs are used as programmable logic elements and a plurality of these LUTs are arranged in the array. *Id.* ¶ 6. Each K-input LUT is not necessarily assigned a logic function with K inputs—that is, if a logic function whose actual number of inputs i is less than K, is assigned to a K-input 1-bit output LUT, only 2^i bits of memory are used to store the program that implements the logic function, and therefore, $(2^K - 2^i)$ bits of memory remain in the LUT as memory not used for the program (invalid memory). *Id.* The logic elements PL11 having such invalid memories cause a problem of lowering the degree of integration in the FPGA. *Id.* ¶¶ 7–8.

Fujii addresses this problem by providing a programmable logic element

in which a plurality of selection circuits in a logic element are connected to different memory circuits, and are divided into a plurality of selection circuits each having a smaller number of inputs than the number of inputs of the logic element, and a plurality of logic functions having inputs less than the number of inputs of the logic elements are simultaneously assigned to one logic element.

Id. ¶¶ 9–10. Fujii’s Figure 1, reproduced below, illustrates such a programmable logic element PL1. *Id.* ¶ 11.

(FIG. 1)

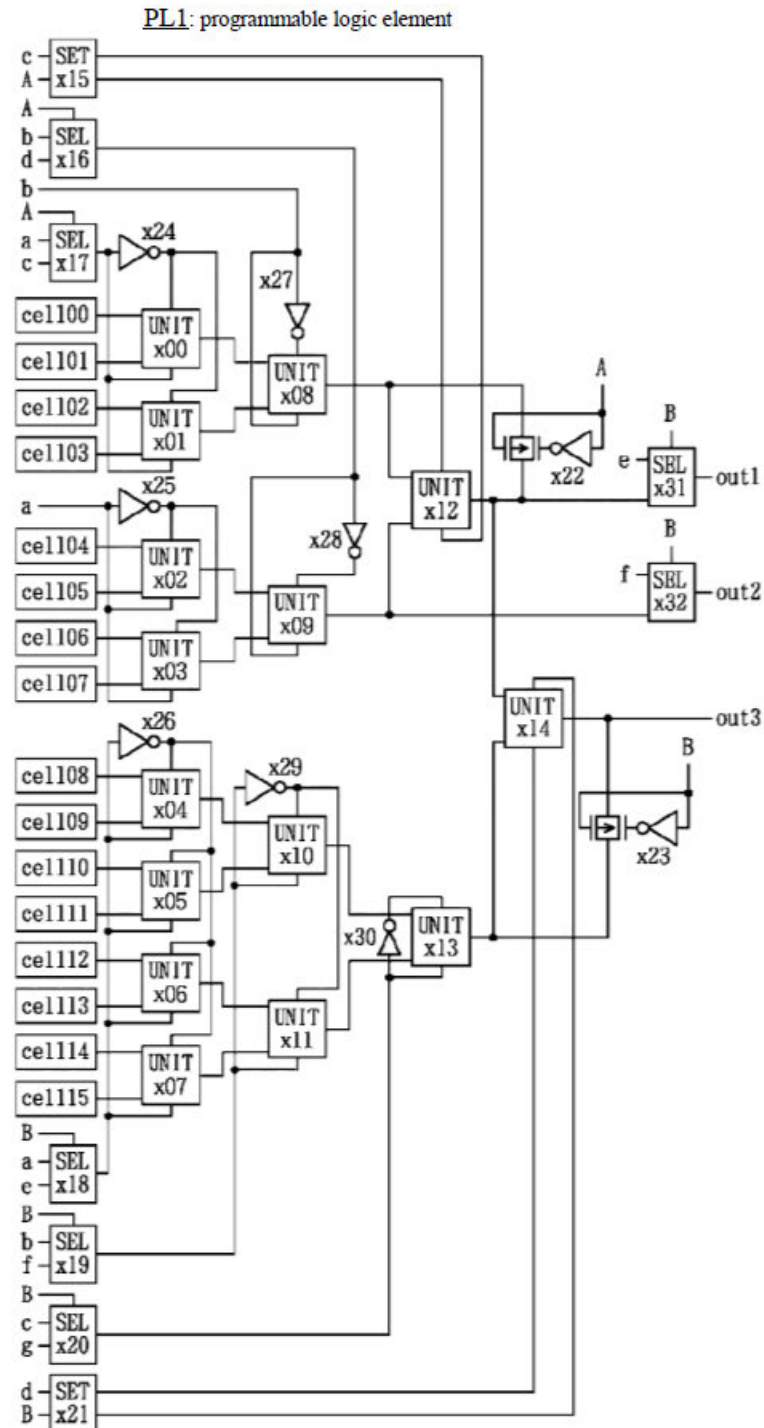


Figure 1 illustrates a programmable logic element PL1 in which a plurality of selection circuits in a logic element are connected to different memory

circuits, and are divided into a plurality of selection circuits each having a smaller number of inputs than the number of inputs of the logic element.
Id. ¶¶ 9–11.

Programmable logic element PL1 switches between the following operations based on multiple control signals. *Id.* ¶¶ 11–12. One operation is “an operation of selecting one output signal from the output signals of the 16 memory circuits and outputting the selected output signal as the output signal of the programmable logic element PL1.” *Id.* ¶ 12.

A second operation is

an operation of outputting the selected output signal of the memory circuit as the output signal of the programmable logic element PL1 ($n=2$, $X_1=3$, $X_2=3$), where this one memory circuit is selected from each memory circuit after dividing the 16 memory circuits into two memory circuit groups each composed of 8 memory circuits, selecting 3 input signals and 3 input signals that do not overlap each other from 7 input signals, and as the selection signal for selecting a predetermined memory circuit from each memory circuit group, applying the selected three input signals to each memory circuit group.

Id.

A third operation is

an operation of outputting the output signal of the selected memory circuit as the output signal of the programmable logic element PL1 ($n=3$, $X_1=3$, $X_2=2$), where this one memory circuit is selected from each memory circuit after dividing the 16 memory circuits into three memory circuit groups [respectively] composed of 8, 4, and 4 memory circuits, selecting 3 input signals, 2 input signals, and 2 input signals that do not overlap each other from 7 input signals, and as the selection signal for selecting a predetermined memory circuit from each memory circuit group, applying the selected three, two, two input signals to each memory circuit group.

Id.

Programmable logic element PL1 uses up to seven input terminals and up to three output terminals, and (i) changes the number of input terminals and output terminals used by switching between the above three operations, (ii) selects, in each operation, the input terminals from the seven available input terminals and the output terminals from the three available output terminals, and (iii) prevents an increase in the number of terminals by sharing input/output terminals between patterns that do not operate simultaneously. *Id.* ¶ 13.

Fujii's Figures 6(1)–6(3), reproduced below, illustrate a correspondence between input and output signals in programmable logic element PL1 and output signals of the memory circuit. *Id.* ¶ 37.

(FIG. 6)

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Figures 6(1)–6(3) illustrate a correspondence between input and output signals in programmable logic element PL1 and output signals of the memory circuit. *Id.* ¶ 37.

In Figures 6(1)–6(3), A and B are control signals for determining the mode of programmable logic circuit PL1; “a,” “b,” “c,” “d,” “e,” “f,” and “g” are input signals; out1, out2, and out3 are output signals, and cell00 to cell15 are selectable memory circuits. *Id.* ¶ 38. First, as shown in Figures 1 and 6(1), when control signals (A, B) are (1, 1), signal “a” is selected as a selection signal for selectors x00, x01, x02, x03, x04, x05, x06, and x07, signal “b” is selected as a selection signal for selectors x08, x09, x10, and x11, signal “c” is selected as a selection signal for selectors x12 and x13, and signal “d” is selected as a selection signal for selector x14. *Id.* ¶ 39. Thus, as shown in Figure 6(1), when control signals (A,B) are (1,1), input signals a, b, c, and d select one of cell00–cell15 for out3, and the circuit of Figure 1 is configured as a 4 x 1 LUT.

Further, as shown in Figures 1 and 6(2), when control signals (A, B) are (0, 0), signal “a” is selected as a selection signal for selectors x02 and x03, signal “b” is selected as a selection signal for selector x08, signal “c” is selected as a selection signal for selectors x00 and x01, signal “d” is selected as a selection signal for selector x09, signal “e” is selected as a selection signal for selectors x04, x05, x06 and x07, signal “f” is and selected as a selection signal for selectors x10 and X11, and signal “g” is selected as a selection signal for selector x13. *Id.* ¶¶ 45, 46. Thus, as shown in Figure 6(2), when control signals (A,B) are (0,0), input signals b and c select one of cell00–cell03 for out1, input signals a and d select one of cell04–cell07 as out2, input signals e, f, g select one of cell08–cell15 as out3, and the circuit of Figure 1 is configured as two 2 x 1 LUTs and one 3 x 1 LUT.

Next, as shown in Figures 1 and 6(3), if control signals (A, B) are (1, 0), signal “a” is selected as a selection signal for selectors x00, x01, x02, and x03, signal “b” is selected as a selection signal for selectors x08 and x09, signal “c” is selected as a selection signal for selector x12, signal “e” is selected as the selection signal for selectors x04, x05, x06, and x07, signal “f” is selected as the selection signal for selectors x10 and x11, and signal “g” is selected as the selection signal for selector x13. *Id.* ¶42. Thus, as shown in Figures 1 and 6(3), when control signals (A,B) are (1,0), input signals a, b and c select one of cell00–cell07 for out1, input signals c, d, and e select one of cell08–cell15 as out3, and the circuit of Figure 1 is configured as two 3 x 1 LUTs.

2. Betz (Ex. 1006)

Betz is a book titled “Architecture and CAD for Deep-Submicron FPGAs,” describing, *inter alia*, FPGA architecture, circuitry, and process modeling. *See* Ex. 1006, Title, Table of Contents (Chapter 2, Appendix B). Betz explains that “[a]ll FPGAs are composed of three fundamental components: logic blocks, I/O blocks and programmable routing.” *Id.* at 11. Betz further explains that a circuit is implemented in an FPGA by programming each of the logic blocks to implement a small portion of the logic required by the circuit, and each of the I/O blocks to act as an input pad or an output pad, as required by the circuit, with programmable routing configured to make all the necessary connections between the logic blocks, and from logic blocks to I/O blocks. *Id.* SRAM-based switches (cells) may be used to control pass transistors, multiplexers, and tri-state buffers, in order to configure the FPGA’s

programmable routing and logic blocks as required. *Id.* at 11–12, Fig. 2.2. Multiplexers are used to implement connection blocks from a set of routing tracks to logic block input pins. *Id.* at 212. Multiplexers may be implemented as a binary tree of pass transistors (as shown in Figure B.7 of Betz, reproduced below), with buffers added on the inputs and output of the multiplexer. *Id.* at 213–214.

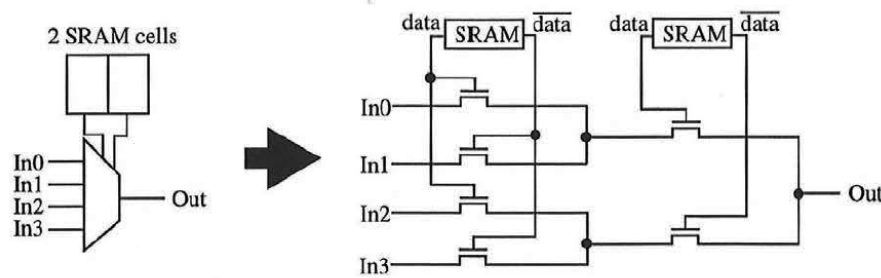


FIGURE B.7 Schematic of a 4-input SRAM-controlled multiplexer.

Figure B.7 illustrates multiplexers implemented as a binary tree of pass transistors, with SRAM cells controlling which multiplexer input is selected (for input pin connection blocks). *Id.* at 213–214.

Figure B.8 of Betz, reproduced below, illustrates a logic block of an FPGA. *Id.* at 214.

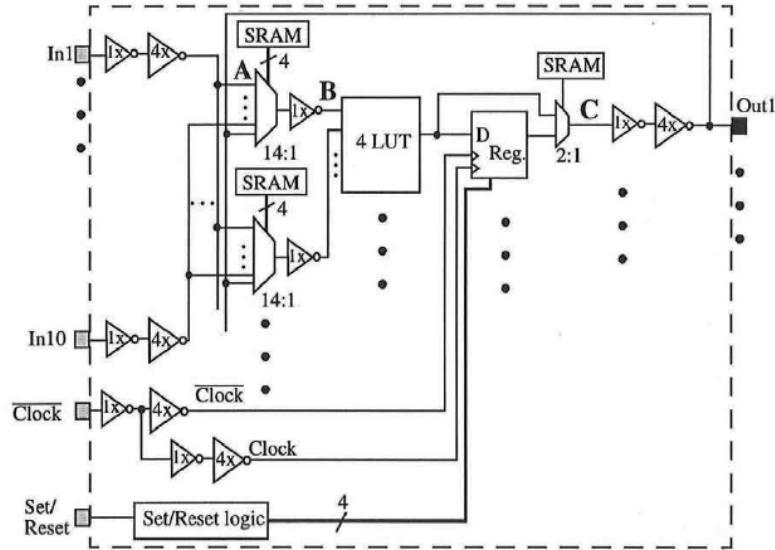


FIGURE B.8 Schematic of a logic cluster of size 4 with 10 logic inputs, 1 clock and a set/reset input.

Figure B.8 of Betz, reproduced above, illustrates a logic block of an FPGA. Betz notes that, to keep Figure B.8 understandable, the figure does not show all the repeated structures in a logic cluster of size 4. Specifically, the figure shows only two of the ten input pin buffers, two of the sixteen 14:1 multiplexers, and one each of the four 4-LUTs, registers, and BLE (basic logic element) output buffers contained in a size 4 logic cluster. *Id.* at 214.

The logic block illustrated in Figure B.8 is a logic cluster of size 4 with 10 logic inputs and one clock. *Id.* at 214. One set/reset signal of programmable polarity may be shared by all four registers in the logic block. *Id.* The four times minimum strength buffer driving the output pin is strong enough to drive the local routing, but not, in general, the routing tracks. *Id.* at 215.

3. Chow (Ex. 1023)

Chow is a paper titled “The Design of a SRAM-Based Field-Programmable Gate Array—Part II: Circuit Design and Layout,” and describes the high-level architectural design of a static random-access

memory programmable FPGA, including design of logic block circuits and connections between the logic and the routing structure. Ex. 1023, 321, Title. Chow also proposes a design style with a minitile that contains a portion of all the components in the logic tile, resulting in less full-custom hand layout effort, and permitting easy changing of the hard-wired connections in the logic block architecture. *Id.* at 321 (Abstr.).

Chow describes the circuit-level design of one FPGA architecture including (i) a lookup table (LUT), (ii) an output stage (following the LUT) that contains a multiplexer to select the latched or unlatched version of the output before the signal is driven through a connection block (C block) onto the routing tracks, (iii) one switch block (S block), or a number of S blocks, and (iv) and another C block where the signal reaches the input of the next logic block. *Id.* at 321. The C block is used to connect signals in the routing tracks to the input pins of the logic blocks, and may be implemented using multiplexers or point-to-point switches, and static random-access memory (SRAM) used as the programming bits. *Id.* at 322. Chow explains that there are multiple techniques for programming the bits, the simplest technique being to connect all of the bits into a long shift register. *Id.* at 325. Another technique is to organize the programming bits into rows and columns, as in a regular memory. *Id.* at 325–326.

E. Asserted Obviousness Based on Fujii and Betz

Petitioner argues that claims 1–16 would have been obvious in view of Fujii and Betz. Pet. 4, 13–82. In support of its showing, Petitioner relies upon the Melvin Declaration. *Id.* (citing Ex. 1003).

We have reviewed Petitioner’s assertions and supporting evidence. For the reasons discussed below, and based on the record before us, we are persuaded that Petitioner demonstrates a reasonable likelihood of prevailing in showing that at least one challenged claim would have been obvious over the combination of Fujii and Betz.

Claim 1: [IPRE] A look up table of M inputs and N outputs, comprising: [1A] a plurality of LUT units

Independent claim 1 recites “[a] look up table of M inputs and N outputs, comprising: a plurality of LUT units.” Ex. 1001, 9:51–53.

Petitioner argues that Fujii teaches these limitations. Pet. 13–24 (citing Fujii ¶¶ 5, 6, 11, 12, 14, 24–27, 30–38, 40–44, 47, 48, 54, 55, 71–80, 94–97; Ex. 1003 ¶¶ 83–99) (asserting that “[Fujii’s programmable logic element] PL1 is a look-up table of 4 inputs” and “three ‘*outputs*’, out1, out2, and out3, that output the values of selected memory bits according to the use modes shown in FIG.6,” and “PL1 . . . [also] comprises ‘three memory circuit groups each composed of 8, 4, and 4 memory circuits, selecting 3 input signals, 2 input signals, and 2 input signals’ . . . which are ‘*a plurality of LUT units*’”).

Patent Owner argues Petitioner has failed to meet its burden for claim 1 because: (i) Fujii is directed to a programmable logic element and “[t]here is no teaching or suggestion in Fujii of constructing [the] programmable logic element from a plurality of individual LUT units”; (ii) “[n]either the memory circuits nor the memory circuit groups of Fujii are LUT units” and (iii) Fujii does not teach or suggest “the use of a plurality of LUT units in constructing a look up table of M inputs and N outputs.” *See*

PO Prelim. Resp. 34–37. According to Patent Owner, Fujii is directed towards implementing a single programmable logic element including memory circuits, which can be functionally grouped using control circuits, selectors, and transfer gates. *Id.* at 34. However, Patent Owner contends that Fujii’s specific teaching describes how to implement a single unit, not a plurality of individual LUT units. *Id.* at 34–35. In particular, Patent Owner argues that “the tables of Figure 6 of Fujii are simply logical *representations* (rather than any particular physical *implementation*) of the various memory circuit groups and an explanation of what functionality the memory elements (*i.e.*, cells in PL1) would produce if grouped in a particular way.” *Id.* at 35. Patent Owner alleges that Petitioner is engaging in box drawing on PL1 to explain the functionality in one particular use mode of operation without regard to how these circuitry components are actually constructed. *Id.* at 35–36. Patent Owner further alleges that Petitioner therefore obfuscates the issue by focusing on how diagrams may be viewed as opposed to how look up tables are actually designed and implemented. *Id.* at 36. Consequently, Patent Owner submits that, regardless of the use mode, Fujii’s disclosure of a particular implementation for its programmable logic element neither teaches nor suggests the use of a plurality of LUT units in constructing a look up table of M inputs and N outputs. *Id.*

We disagree with Patent Owner’s arguments. As set forth in our claim construction section above, an “LUT unit” refers to a unit (e.g., memory) in an LUT of M inputs and N outputs. Accordingly, the disputed claim limitation “a look up table of M inputs and N outputs, comprising: a plurality of LUT units” requires, *inter alia*, an arbitrary logic circuit including a memory array (a plurality of LUT units) of M inputs and N

outputs. We thus agree with Petitioner that Fujii's disclosure of PL 1 including three memory circuit groups each composed of 8, 4, and 4 memory circuits having respectively 3 input signals, 2 input signals, and 2 input signals, and sharing three outputs constitute an arbitrary logic circuit with M inputs and N outputs including memory arrays, and thereby teaches a lookup table with M inputs and N outputs including *a plurality of LUT units*.

Further, Patent Owner argues that the addition of Betz "fails to address the lack of any teaching or suggestion in Fujii of a plurality of LUT units" and "even if the memory-controlled selectors of Betz could be applied to the programmable logic elements of Fujii, the combination would still fail to teach or suggest a look up table of M inputs and N outputs comprising a plurality of LUT units." PO Prelim. Resp. 37.

We do not agree with Patent Owner. As noted above, Fujii's disclosure teaches the look up table of M inputs and N outputs including the plurality of LUT units.

Accordingly, for the foregoing reasons and on this preliminary record, we determine that Petitioner has sufficiently shown that the proposed combination of Fujii and Betz teaches preamble and limitation [1A].⁵

⁵ Neither party argues whether the preamble limits claim 1. Although we find that the evidence supports that the prior art teaches the preamble, we do not determine at this stage of the proceeding whether the preamble of claim 1 is limiting.

*Claim 1: [1B] an internal configuration control circuit
controlling an internal configuration of said plurality of LUT units*

Independent claim 1 further recites that the look up table of M inputs and N outputs comprises “an internal configuration control circuit controlling an internal configuration of said plurality of LUT units.”

Ex. 1001, 9:54–55.

Petitioner argues that Fujii teaches these limitations. Pet. 25–34 (citing Fujii ¶¶ 2, 14, 24–28, 36–47, 51, 54, 55, 71–80, 94–97; Ex. 1003 ¶¶ 100–107) (asserting that “Fujii discloses control signals, selectors, control circuits, CMOS transfer gates, and the wires connecting those components to each other and/or other components within PL1” which constitute “*an internal configuration control*” circuit for ‘*controlling an internal configuration of said plurality of LUT units*’” as this “circuit . . . allows PL1 to ‘switch[] between three operations’ or ‘use mode[s],’ as shown in FIG.6,” with “Fujii’s three [use] modes [being] internal configurations of the ‘*LUT units*’ that are switched by varying values of control signals”).

Patent Owner argues Petitioner has failed to meet its burden for claim 1 because: (i) there is no teaching or suggestion in Fujii of constructing its programmable logic element with “a configuration control circuit controlling an internal configuration of a plurality of LUT units”; (ii) Fujii’s implementation of use modes is materially different from the “controlling an internal configuration of said plurality of LUT units” described in the ’737 patent, as Fujii’s “programmable logic element . . . uses a ‘plurality of selection circuits’ that are ‘divided into a plurality of selection circuits,’ not a plurality of LUT units, in its logic element,” and Fujii controls these selection circuits simply with control signals, not with

“an internal configuration control circuit”; and (iii) the addition of Betz “fails to address the lack of any teaching or suggestion in Fujii of a plurality of LUT units or a configuration control circuit controlling an internal configuration of the plurality of LUT units” and even if the memory-controlled selectors of Betz could be applied to the programmable logic elements of Fujii, “the combination would still fail to teach or suggest a look up table of M inputs and N outputs comprising a plurality of LUT units and a configuration control circuit controlling an internal configuration of the plurality of LUT units.” *See* PO Prelim. Resp. 34–37.

We do not agree with Patent Owner’s arguments. Claim limitation 1[B] requires an internal configuration control circuit for controlling an internal configuration of the plurality of LUT units. Consistent with the ’737 patent, the internal configuration circuit includes a plurality of selectors for selecting I/O signals of the LUT units, and a selector control circuit with a memory for controlling the selectors according to instructions stored in the memory. Ex. 1001, 9:56–63. Because Fujii’s disclosure of a 3-mode-switching operation likewise involves using selectors for selecting I/O signals to the memory arrays (LUT units) to operate them in a desired mode according to selection signals received from the selectors, we agree with Petitioner that Fujii teaches or suggests the internal configuration circuit for controlling the internal configuration of the LUT units. Ex. 1005 ¶¶ 11–13; Pet. 25, 33.

Accordingly, for the foregoing reasons and on this preliminary record, we determine that Petitioner has sufficiently shown that the proposed combination Fujii and Betz teaches limitations [1B].

Claim 1: [1C] wherein said internal configuration control circuit comprises a plurality of selectors selecting I/O signals of said plurality of LUT units, and

Independent claim 1 further recites that “said internal configuration control circuit comprises a plurality of selectors selecting I/O signals of said plurality of LUT units.” Ex. 1001, 9:56–59.

Petitioner argues that Fujii teaches these limitations. Pet. 34–37 (asserting that “Fujii discloses this limitation because it discloses selectors x16-x20 that select input signals of the ‘*plurality of LUT units*’ in PL1 and selectors x12, x14, x31, and x32 that select output signals of the ‘*plurality of LUT units*’ in PL1” such that “Fujii’s ‘*internal configuration control circuit comprises a plurality of selectors [selectors x12, x14, x16-x20, x31, x32] selecting I/O signals [e.g., selector x16 selects between inputs b and d and selector x12 selects between outputs of the top and middle 2-LUTs] of said plurality of LUT units*’”) (bracketed material added by Petitioner)).

Patent Owner does not specifically respond to these arguments. *See* Prelim. Resp. Nonetheless, the burden remains on Petitioner to demonstrate unpatentability. *See Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015).

Based on our review and consideration of the current record, we determine that Petitioner has sufficiently shown that Fujii (combined with Betz) teaches limitations [1C].

Claim 1: [1D] [wherein said internal configuration control circuit comprises] a selector control circuit having a memory, controlling said plurality of selectors in accordance with data stored in said memory, and defining the internal configuration of said plurality of LUT units

Independent claim 1 further recites that the internal configuration control circuit comprises “a selector control circuit having a memory, controlling said plurality of selectors in accordance with data stored in said memory, and defining the internal configuration of said plurality of LUT units.” Ex. 1001, 9:60–63.

Petitioner asserts that the combination of Fujii and Betz teaches this limitation. Pet. 37–45.

Patent Owner does not specifically respond to these arguments. *See* Prelim. Resp.

Based on our review and consideration of the current record, we determine that Petitioner has sufficiently shown that the combination of Fujii and Betz teaches limitations [1D].

Conclusion Regarding Independent Claim 1

For the foregoing reasons, we determine that Petitioner has established a reasonable likelihood of prevailing on its assertion that independent claim 1 would have been obvious in view of the combination of Fujii and Betz.

Independent Claims 7 and 13

For essentially the same reasons as independent claim 1, Petitioner contends that independent claims 7 and 13 would have been obvious over the combined teachings of Fujii and Betz. Pet. 4, 58–71 (claim 7), 73–74 (claim 13). Patent Owner does not separately argue independent claims 7 and 13. *See* Prelim. Resp.

Accordingly, for the same reasons as set forth above for independent claim 1, we determine that Petitioner has adequately shown that the combination of Fujii and Betz teaches the limitations in claims 7 and 13, and has provided sufficient rationale for combining the references for purposes of institution. We determine, on the current record and for purposes of this Decision, that the information presented in the Petition demonstrates a reasonable likelihood that Petitioner would prevail in its obviousness contentions regarding claims 7 and 13.

Dependent Claims 2–6, 8–12, and 14–16

Petitioner also contends that claims 2–6, 8–12, and 14–16, which depend directly or indirectly from independent claims 1, 7, and 13, would have been obvious over Fujii and Betz. Pet. 4, 45–58, 71–82.

We have reviewed Petitioner’s initial showing as to the dependent claims, and find that Petitioner has sufficiently shown that the combination of Fujii and Betz teaches each of the limitations of these claims at this stage of the proceeding. *Id.* We further note that Patent Owner does not separately address the patentability of these claims beyond its arguments as to independent claim 1, addressed above. *See* Prelim. Resp. We determine, on the current record and for purposes of this Decision, that the information

presented in the Petition demonstrates a reasonable likelihood that Petitioner would prevail in its obviousness contentions regarding claims 2–6, 8–12, and 14–16.

As we preliminarily conclude that Petitioner demonstrates a reasonable likelihood of prevailing with respect to its obviousness challenge to independent claim 1 as rendered obvious by Fujii and Betz, we institute review on all challenged claims on all grounds set forth in the Petition, including Petitioner’s challenge to claims 1–16 as rendered obvious by Fujii and Betz. *See SAS Inst. Inc. v. Iancu*, 138 S. Ct. 1348, 1354 (2018); *PGS Geophysical AS v. Iancu*, 891 F.3d 1354, 1360 (Fed. Cir. 2018).

F. Asserted Obviousness Based on Fujii, Betz, and Chow

Petitioner argues that claims 1–16 would have been obvious in view of Fujii, Betz, and Chow. Pet. 4, 82–84.

Patent Owner argues Petitioner has failed to meet its burden with respect to limitations pertaining to *a look up table of M inputs and N outputs, a plurality of LUT units, and an internal configuration control circuit controlling an internal configuration of said plurality of LUT units*. PO Prelim. Resp. 38–39. In particular, Patent Owner argues that “the combination of Fujii and Betz fails to teach or suggest the claimed invention for reasons other than whether the memory recited in the claims must constitute a single memory” (Petitioner’s reason for bringing in Chow), referencing the reasons discussed with respect to the ground based on Fujii and Betz. *Id.* at 38. Patent Owner also submits that “a person of ordinary skill in the art would *not* be motivated to modify the combination of Fujii with Betz with a technique known to be disadvantageous [in Chow].” *Id.*

Based on our review and consideration of the current record, and for the same reasons as set forth above for ground 1, we determine that Petitioner has adequately shown that the combination of Fujii, Betz, and Chow teaches the limitations in claims 1, 7, and 13, and has provided sufficient rationale for combining the references for purposes of institution.

Although Chow notes that the use of a single shift register is the slowest option, it also states that it is the simplest option. Ex. 1023, 325; *see* Prelim. Resp. 33–34 (discussing this disclosure). On this record, we find persuasive Petitioner’s contentions that using a single shift register, as taught in Chow, “would have merely amounted to use of a known technique (programming a shift register with configuration bits) to improve a similar device (Fujii-Betz PL1) in the same way (implementing the simplest technique to program the configuration bits).” Pet. 83 (citing Ex. 1003 ¶ 197); *see also Intel Corp. v. Qualcomm Inc.*, 21 F.4th 784, 800 (Fed. Cir. 2021) (“It’s not necessary to show that a combination is ‘the *best* option, only that it be a *suitable* option.”) (quoting *PAR Pharm., Inc. v. TWI Pharms., Inc.*, 773 F.3d 1186, 1197–98 (Fed. Cir. 2014))).

We determine, on the current record and for purposes of this Decision, that the information presented in the Petition demonstrates a reasonable likelihood that claims 1, 7, and 13 are unpatentable under 35 U.S.C. § 103(a) over the combination of Fujii, Betz, and Chow.

Because we preliminarily conclude that Petitioner demonstrates a reasonable likelihood of prevailing with respect to its challenge to independent claims 1, 7, and 13 in view of Fujii, Betz, and Chow, we also institute review on Petitioner’s challenge to dependent claims 2–6, 8–12, and

14–16 for obviousness based on Fujii, Betz, and Chow. *See SAS*, 138 S. Ct. at 1354; *PGS Geophysical*, 891 F.3d at 1360.

IV. CONCLUSION

For the foregoing reasons, we determine that the information presented establishes a reasonable likelihood that Petitioner would prevail in showing that at least one challenged claim of the '737 patent is unpatentable. At this preliminary stage, we have not made a final determination with respect to the patentability of the challenged claims or any underlying factual and legal issues. *See TriVascular, Inc. v. Samuels*, 812 F.3d 1056, 1068 (Fed. Cir. 2016) (noting that “there is a significant difference between a petitioner’s burden to establish a ‘reasonable likelihood of success’ at institution, and actually proving invalidity by a preponderance of the evidence at trial”).

Accordingly, *inter partes* review is instituted as to all challenged, non-disclaimed claims and all proposed grounds of unpatentability. *See* 37 C.F.R. § 42.108(a).

V. ORDER

Accordingly, it is:

ORDERED that pursuant to 35 U.S.C. § 314(a), an *inter partes* review of claims 1–16 of the '737 patent is instituted with respect to the grounds set forth in the Petition; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial, which commences on the entry date of this Decision.

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