

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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SAMSUNG ELECTRONICS CO., LTD.  
Petitioner

v.

DAEDALUS PRIME LLC  
Patent Owner

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Patent No. 9,202,699

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**DECLARATION OF DR. STANLEY SHANFIELD IN SUPPORT OF  
PETITION FOR *INTER PARTES* REVIEW  
OF U.S. PATENT NO. 9,202,699**

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I, Stanley Shanfield, declare as follows:

## **I. INTRODUCTION**

1. I have been retained by Samsung Electronics Co., Ltd. (“Petitioner”) as an independent expert consultant in this proceeding before the United States Patent and Trademark Office (“PTO”) regarding U.S. Patent No. 9,202,699 (“the ’699 patent”) (Ex. 1001). I have been asked to consider whether certain references disclose or suggest the features recited in claims 1, 2, and 4-11 of the ’699 patent. My opinions are set forth below.

2. I am being compensated at a rate of \$385/hour for my work in this proceeding. My compensation is in no way contingent on the nature of my findings, the presentation of my findings in testimony, or the outcome of this or any other proceeding. I have no other interest in this proceeding.

## **II. BACKGROUND AND QUALIFICATIONS**

3. I am an independent consultant. All of my opinions stated in this declaration are based on my own personal knowledge and professional judgment. In forming my opinions, I have relied on my knowledge and experience in designing, developing, and fabricating integrated circuits, including interconnect structures used in such integrated circuits.

4. I am over 18 years of age and, if I am called upon to do so, I would be competent to testify as to the matters set forth herein. A copy of my current

curriculum vitae, which details my education and professional and academic experience, is attached as an addendum with this declaration. The following provides an overview of some of my experience that is relevant to the matters set forth in this declaration.

5. I received a B.S. in Physics from the University of California, Irvine in 1977. I received the University of California Regents Award for Outstanding Research Project for my experimental and theoretical work on rotating relativistic electron beams. Under full ERDA (DOE) scholarship, I received a Ph.D. in Physics from the Massachusetts Institute of Technology in 1981.

6. After receiving my doctorate degree, I worked at Spire Corporation in Bedford, Massachusetts from 1981-1984, where I served as a Staff Scientist, and later, a Senior Staff Scientist. At Spire, I developed new methods for low temperature deposition of plasma-assisted CVD epitaxial silicon. In addition, I built, operated, and characterized an ion-assisted deposition system for making coating for semiconductor and machine tool industries.

7. From 1985-1999, I worked at Raytheon Corporation. As staff and later as section manager, I developed reactive ion etching (RIE) processes for patterning dielectrics (silicon dioxide, silicon nitride, silicon oxynitride, etc.), conductive layers (aluminum-copper, copper-silicon, W-silicide, TaN, doped polysilicon, etc.) and organic layers (photoresist, polyimide, etc.). For example, I developed a low

damage, high selectivity process as part of the FET gate formation step. I was responsible for purchasing equipment and developing processes for several plasma systems typical of those used in the semiconductor industry, including load-locked RIE, microwave ECR RIE, barrel etchers, single-wafer elevated temperature RIE systems, etc.

8. In 1996, I became the Manager of Semiconductor Operations at Raytheon. As Manager, I built and led a 300 employee, \$60 million revenue-generating semiconductor development, commercial system design, and electronic module manufacturing operation. I worked directly with engineers in the selection, installation and optimization of several chemo-mechanical polishing systems (CMP), including analysis of operational maintenance and performance monitoring. The manufacturing facility eventually used multiple production CMP systems, and I directly participated in establishing the required metrology (optical thickness monitoring) for maintaining polishing uniformity standards.

9. From 1999-2001, I worked at AXSUN Technologies as part of the founding team, first as the Director of Manufacturing & Wafer Fab Technology, and later, as the Vice President of Operations. As Director of Manufacturing & Wafer Fab Technology, I led device and module manufacturing, creating a wafer fab and circuit board assembly infrastructure; my responsibilities included hiring over 70 individuals and leading production design efforts. In my role as Vice President of

Operations, I designed, fabricated, and productized AXSUN's microelectromechanical (MEM) Fabry-Perot optical filter, and I managed a new generation of electronics module design. In addition, I established a process and fabrication facility in Belfast, Northern Ireland for producing thick oxide silicon-on-insulator devices. As a result of my work at AXSUN, I was awarded patents on semiconductor processing and control electronics.

10. I have served since 2003 at the Charles Stark Draper Laboratory ("Draper Laboratory") in Cambridge, Massachusetts, ultimately becoming a Distinguished Member of Technical Staff and Technical Director in Advanced Hardware Development. I led the Advanced Hardware Development Division (approximately 80 staff) in their work on the laboratory's multi-chip integrated circuit module facility. The laboratory has acquired several semiconductor-grade CMP systems for the purpose of fabricating multi-chip modules and for planarization operations in MEMS devices, and I have been involved in their operation and optimization.

11. I have authored more than 25 journal and conference papers. My publications include numerous papers on topics relating to semiconductor processing, advanced semiconductor devices, electronic circuit design and packaging. I have been invited to give professional talks at various conferences. I am also a co-inventor of several U.S. Patents.

12. I am not an attorney and offer no legal opinions, but in the course of my work, I have had experience studying and analyzing patents and patent claims from the perspective of a person skilled in the art.

### III. MATERIALS REVIEWED

13. The opinions in this Declaration are based on the documents I reviewed, my knowledge and experience, and professional judgment. In forming my opinions expressed in this Declaration, I have reviewed the following materials: U.S. Patent No. 9,202,699 (Ex. 1001); the prosecution history of U.S. Patent No. 9,202,699 (Ex. 1004); U.S. Patent Publication No. 2011/0147842 to Cappellani *et al.* (“Cappellani”) (Ex. 1005); U.S. Patent Publication No. 2011/0298061 to Siddiqui *et al.* (“Siddiqui”) (Ex. 1006); U.S. Patent Publication No. 2011/0108930 to Cheng *et al.* (“Cheng”) (Ex. 1007); U.S. Patent Publication No. 2005/0148137 to Brask *et al.* (“Brask”) (Ex. 1008); Hisamoto *et al.*, FinFET—A Self-Aligned Double-Gate MOSFET Scalable to 20 nm, IEEE Transactions on Electron Devices, Vol. 47, No. 12, Dec. 2000 (“Hisamoto”) (Ex. 1009); U.S. Patent No. 8,951,853 to Park *et al.* (“Park”) (Ex. 1010); U.S. Patent No. 7,858,421 to Chen *et al.* (“Chen”) (Ex. 1011); U.S. Patent No. 8,558,336 to Su *et al.* (“Su”) (Ex. 1012); U.S. Patent No. to Kikuchi *et al.* (“Kikuchi”) (Ex. 1013); U.S. Patent Publication No. 2010/0173479 to Joo (“Joo”) (Ex. 1014); U.S. Patent 6,802,944 to Ahmad *et al.* (“Ahmad”) (Ex. 1015); U.S. Patent 6,500,771 to Vassiliev *et al.* (“Vassiliev”) (Ex. 1016); Plummer *et al.*, Silicon

VLSI Technology, Fundamentals, Practice and Modeling, 2000 (“Plummer”) (Ex. 1017); Leobandung *et al.*, Wire-Channel and Wrap-Around-Gate Metal-Oxide-Semiconductor Field-Effect Transistors with a Significant Reduction of Short Chanel Effects, J. Vac. Sci. Technol. B 15(6), Nov/Dec 1997 (“Leobandung”) (Ex. 1018); Tang *et al.*, FinFET – A Quasi-Planar Double-Gate MOSFET, 2001 IEEE International Solid-State Circuits Conference, 2001 (“Tang”) (Ex. 1019); U.S. Patent Publication No. 2010/0038715 to Babich *et al.* (“Babich”) (Ex. 1020); U.S. Patent Publication No. 2009/0065877 to Tshchiaki (“Tshchiaki-877”) (Ex. 1021); U.S. Patent Publication No. 2004/0256645 to Tshchiaki *et al.* (“Tshchiaki-645”) (Ex. 1022); U.S. Patent Publication No. 2009/0057730 to Furukawa *et al.* (“Furukawa”) (Ex. 1023); U.S. Patent Publication No. 2008/0203440 to Tshchiaki (“Tshchiaki-440”) (Ex. 1024); Wolf, Silicon Processing for the VLSI Era, Vol. 3: The Submicron MOSFET, 1995 (“Wolf”) (Ex. 1025); Neaman, Semiconductor Physics and Devices (Third Edition), 2003 (“Neaman”) (Ex. 1026); and any other materials I refer to in this declaration in support of my opinions.

14. All of the opinions contained in this declaration are based on the documents I reviewed and my knowledge and professional judgment. My opinions have also been guided by my appreciation of how a person of ordinary skill in the art would have understood the claims and the specification of the '699 patent at the time of the alleged invention, which I have been asked to initially consider as the

early 2010s (including September 30, 2011, the filing date of International Application PCT/US2011/054464 (“the ’464 PCT application”) to which the ’699 patent claims priority, which I understand is the earliest possible priority date for the ’699 patent). My opinions reflect how one of ordinary skill in the art would have understood the ’699 patent, the prior art to the patent, and the state of the art at the time of the alleged invention.

15. Based on my experience and expertise, it is my opinion that certain prior art references disclose or suggest all the features recited in claims 1, 2, and 4-11 of the ’699 patent, as I discuss in detail below.

#### **IV. LEVEL OF ORDINARY SKILL IN THE ART**

16. I am familiar with the level of ordinary skill in the art with respect to the alleged inventions of the ’699 patent as of what I understand is the earliest possible priority date of September 30, 2011, which is the filing date of the ’464 PCT application to which the ’699 patent claims priority. Specifically, based on my review of the ’699 patent, the technology, the educational level and experience of active workers in the field, the types of problems faced by workers in the field, the solutions found to those problems, the sophistication of the technology in the field, and drawing on my own experience, I believe a person of ordinary skill in the art would have had a bachelor’s degree in a field relating to the semiconductor manufacturing process like materials science, physics, electrical engineering, or

other related subjects, and at least two to three years of experience with fabrication of integrated circuits. More education can supplement practical experience and vice versa. Depending on the engineering background and level of education of a person, it would have taken a few years for the person to become familiar with the problems encountered in the art and to become familiar with the prior and current solutions to those problems.

17. All of my opinions in this declaration are from the perspective of one of ordinary skill in the art, as I have defined it here, during the relevant timeframe (early 2010s timeframe).

## **V. TECHNICAL BACKGROUND**

18. In this section, I present a brief overview of certain aspects of transistors used in integrated circuits and the manufacture of such transistors at the time of the alleged invention that will assist in better understanding the '699 patent and the prior art that I discuss in this declaration.

### **A. Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs)**

19. Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) have long been used as building blocks for integrated circuits (ICs).

The MOSFET, in conjunction with other circuit elements, is capable of voltage gain and signal-power gain. The MOSFET is also used extensively in digital circuit applications where, because of its relatively small

size, thousands of devices can be fabricated in a single integrated circuit. The MOSFET is, without doubt, the core of integrated circuit design at the present time.

(Ex. 1026, 449.)

20. A typical MOSFET includes four terminals, i.e., the gate terminal (G), the source terminal (S), the drain terminal (D), and the body terminal (B), as shown in the figure and corresponding symbol below. (*Id.*, 484.)

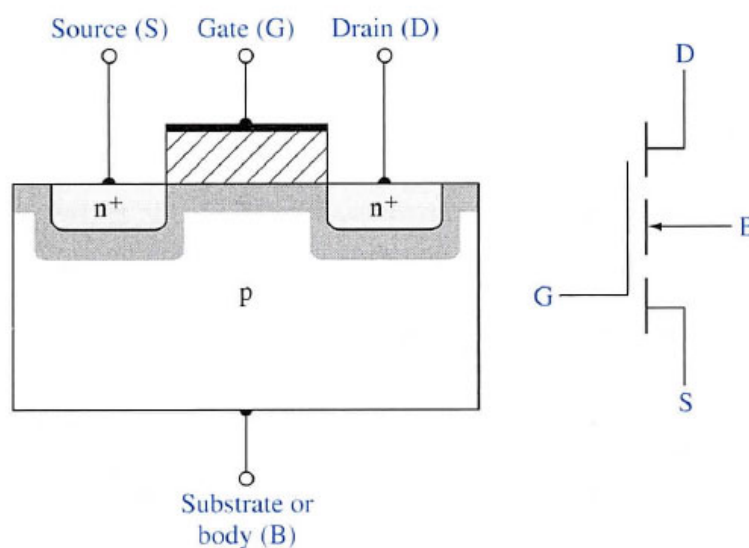
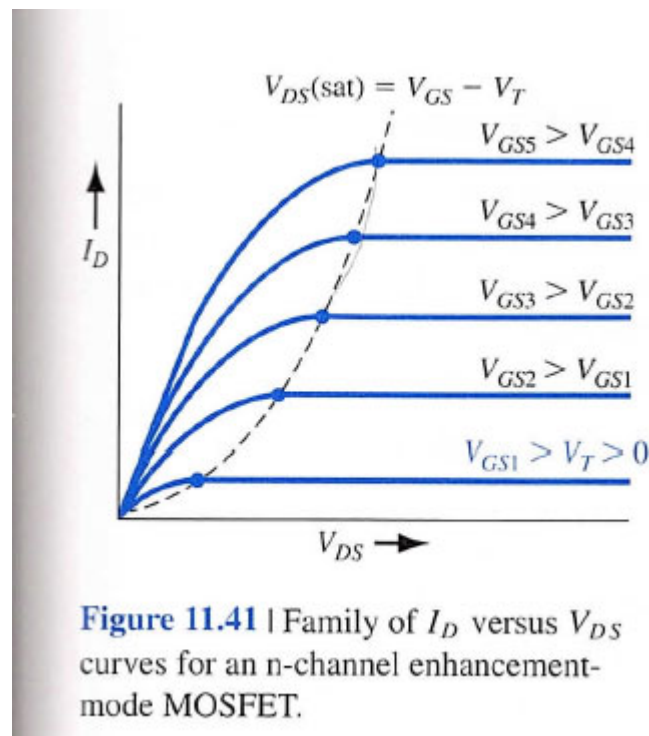


**Figure 11.35** | Cross section and circuit symbol for an n-channel enhancement-mode MOSFET.

(*Id.*, FIG. 11.35.)

21. In many cases, a MOSFET functions like a switch. Using an n-channel MOSFET as an example, when a sufficiently large positive gate voltage is applied, an electron inversion layer is formed, which establishes a channel that connects the source and drain terminals, allowing the charge carriers to flow from the source

terminal through the channel to the drain terminal. (*Id.*, 484; *see also id.*, 484-485 (disclosing that, in addition to n-channel MOSFETs, other known MOSFET types are p-channel MOSFETs).) In particular, by applying a certain drain bias ( $V_{DS}$ ) and a gate bias ( $V_{GS}$ ) that is sufficiently large, i.e., larger than the threshold voltage ( $V_T$ ) of the MOSFET, a current may flow through the MOSFET (i.e., from the source terminal, through the channel, and then to the drain terminal). (*Id.*, 484-490.) Under this scenario, the MOSFET is turned “on.”



(*Id.*, FIG. 11.41.) When the gate bias is less than the threshold voltage, no current (other than some leakage current) flows between the source and drain terminals. (*Id.*, 487 (“When  $V_{GS} < V_T$ , the drain current is zero.”).) Under this scenario, the

MOSFET is turned “off.” In other words, a MOSFET may be turned on or off based on the voltage applied to the gate terminal.

22. In MOSFETs, the conductivity of semiconductor material may be modified by adding impurity atoms, which are known as dopant atoms or simply as dopants. (*Id.*, 103.) Depending on the type of dopants added, the dominant electrical charge carriers may either be electrons (negative charge carriers) or holes (positive charge carriers). (*Id.*; *see also id.*, 115 (“the real power of semiconductors is realized by adding small, controlled amounts of specific dopant, or impurity, atoms.... [Such] doping process can greatly alter the electrical characteristics of the semiconductor.”).) An n-type semiconductor refers to a semiconductor material that has electrons as the majority carrier, and a p-type semiconductor refers to a semiconductor material that has holes as the majority carrier. (*Id.*, 116-119 (discussion regarding typical dopants used for silicon, which is a semiconductor material, to form either an n-type or p-type semiconductor material).)

23. As the size of MOSFETs is downscaled in order to fit more transistors in a single device, the feature size (i.e., the physical dimensions of the device), including the channel length, is reduced. The reduction in feature size is reflected in Figure 1-2 of Plummer below.

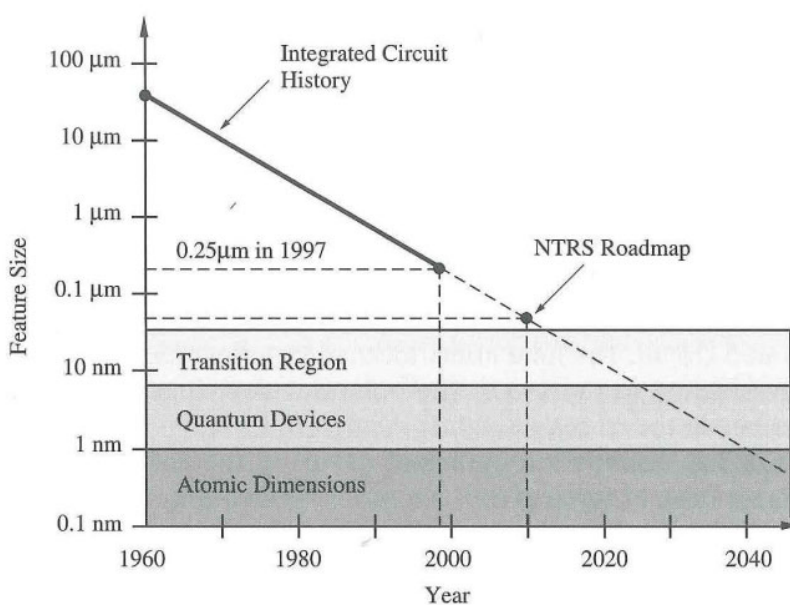


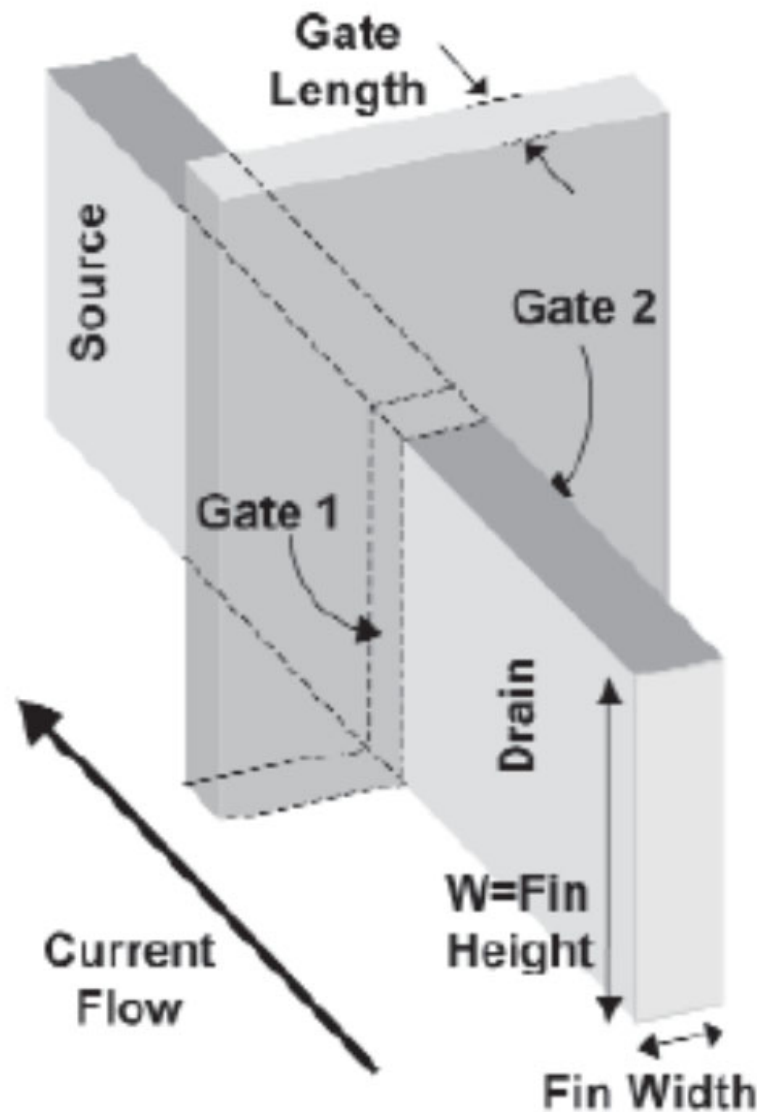
**Figure 1-2** Historical trends and future projections for the minimum feature size used in integrated circuits in manufacturing.

(Ex. 1017, 3 (FIG. 1-2).) The reduced channel length leads to several non-ideal effects, including “short-channel effects” that negatively impact the performance of MOSFETs. For example, short-channel effects can lead to an increased leakage current, making it difficult to turn the transistor completely off. In other words, the gate terminal loses control of the channel’s conductivity as the channel remains conductive (i.e., conducting increased leakage current) even when the applied gate voltage should have the channel in the non-conductive (“off”) state. (Ex. 1018, 1 (“When the size of conventional metal-oxide-semiconductor field-effect transistors (MOSFETs) is reduced to the deep submicron regime, the transistors usually suffer severe short channel effects (SCEs). One of the effects is a large subthreshold slope, which leads to a large leakage current.”).) Increased leakage current can result in

inefficient transistor operation and excess power consumption, thereby making it difficult to achieve low power operations as desired for many portable devices.

**B. Fin Field Effect Transistors (FinFETs)**

24. FinFETs are a non-planar form of MOSFET that provides better control of channel's conductivity by effectively having multiple gates, which can help combat short-channel effects. A FinFET has a slab of semiconductor material that is vertically oriented like a "fin" and extends from the surface of the substrate, where the gate generally wraps around the top and sides of the fin. The schematic below shows features of such a fin field-effect transistor (FinFET).



(Ex. 1019, 2 (FIG. 7.4.1).)

25. Such a FinFET is similar to the planar MOSFETs that I discuss above in Section V.A, as both include source/drain regions, a channel region, and a gate electrode. In a FinFET, however, the channel, source, and drain are located in the “fin,” and a FinFET has multiple gates, e.g., on the vertical sidewalls of the fin for two-gate FinFETs, where three-gate FinFETs also have a gate on the top side of the

fin. A FinFET transistor is desirable because it can provide greater gate-to-channel overlap without significantly increasing the lateral dimensions of the transistor. The greater gate-to-channel overlap results in improved gate control, which can reduce short channel effects and unwanted leakage current. (Ex. 1019, 1 (“Scaling conventional CMOS transistors much below 50nm is difficult. Control of leakage currents requires gate dielectrics so thin and bodies doped so heavily that a process window sufficiently large for manufacturing might not be found. Double-gate MOSFET [e.g., FinFET] structures can overcome these and other limitations to transistor scaling. By placing a second gate on the opposite side of the device, the gate capacitance to the channel is doubled and the channel potential is better controlled by the gate electrode, thus limiting the leakage current.”).)

26. FinFETs may be fabricated using conventional MOSFET process technologies. (Ex. 1009, 1 (“The quasiplanar nature of this new variant of the vertical double-gate MOSFETs can be fabricated relatively easily using the conventional planar MOSFET process technologies.”), 5 (“In spite of its double-gate structure, FinFET is close to its root, the conventional MOSFET in terms of layout and fabrication. The result is a quasiplanar device.”).)

### **C. Self-Aligned (Borderless) Contacts**

27. As transistors sizes shrink and the critical dimensions are further reduced, forming electrical contacts to the terminals (e.g., source/drain regions) of

the transistor becomes more challenging. (Ex. 1020, ¶[0002] (“The formation of electrical contacts to electronic and memory devices is a considerable challenge as the integration density of these devices is increased as a consequence of technology scaling.”); Ex. 1007, ¶[0009] (“As the CDs of CMOS devices are being aggressively scaled, forming contacts on those small devices is becoming more and more difficult [due] to the tight overlay tolerance.”).) “In order to fit the contact between adjacent gates, contacts must be made at dimensions approaching the gate length of the device unlike previous technologies where the contacts were many times larger than the gate.” (Ex. 1020, ¶[0003].) Smaller transistor dimensions make proper alignment of the source/drain contacts with respect to the gate more difficult, where misalignment can result in unwanted short circuits and device inoperability:

Definition of this contact is a lithographic challenge.

Alignment of the contact to the source, drain, and gate of the device is critical. In particular, misalignment of the source and drain contacts with respect to the gate can cause electrical shorts, rendering the device inoperable.

(*Id.*)

28. Borderless self-aligned contacts provide connections to source/drain regions in a manner that overcomes the above-noted challenges associated with the reduction in transistor size. (*Id.*, ¶[0008] (“Embodiments of the present invention provide...field-effect transistors with borderless self-aligned electrical contacts.

Contacts that are self-aligned to the source and drain are highly desirable to overcome the misalignment problem discussed above.”); Ex. 1007, ¶[0009] (“Borderless contacts and techniques relating thereto help reduce the amount of space required for contacts, and enable production of smaller devices having a tighter pitch.”).)

29. An example of formation of self-aligned contacts is illustrated in figures 1-6 of Siddiqui. (Ex. 1006, FIGs. 1-6.) As shown in annotated figure 4 below, silicon nitride spacers 18 are formed on the sidewalls and a silicon nitride protective cap structure 60 is formed on the top of the gate, wherein the spacers and cap protect the gate during the etching operation that forms the hole for the contact. (Ex. 1006, ¶¶[0034], [0062]-[0064].)

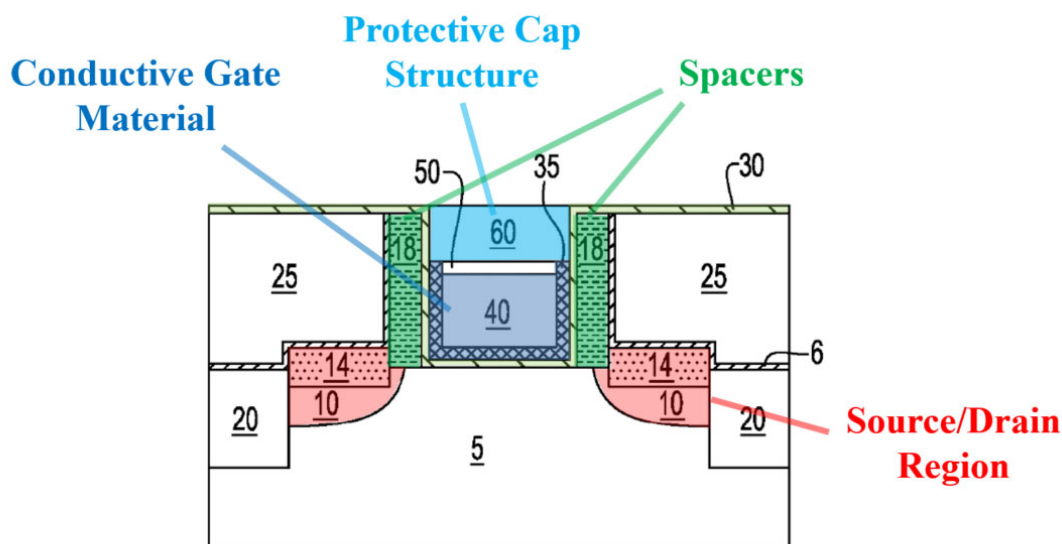


FIG. 4

(*Id.*, FIG. 4 (annotated).)

30. Annotated figure 6 below shows the contact 90 formed in a via hole that has been etched through the dielectric layers 85 and 25, where the hole exposes the source/drain region and allows the contact to make an electrical connection with the source/drain region. (Ex. 1006, ¶¶[0065], [0070].) The etching to form the via hole is a selective etch that removes the material of the dielectric layers 25 and 85 faster than the silicon nitride of the protective cap 60 and spacer 18, where the etching slows or stops at those silicon nitride layers. (Ex. 1006, ¶¶[0065], [0069].)

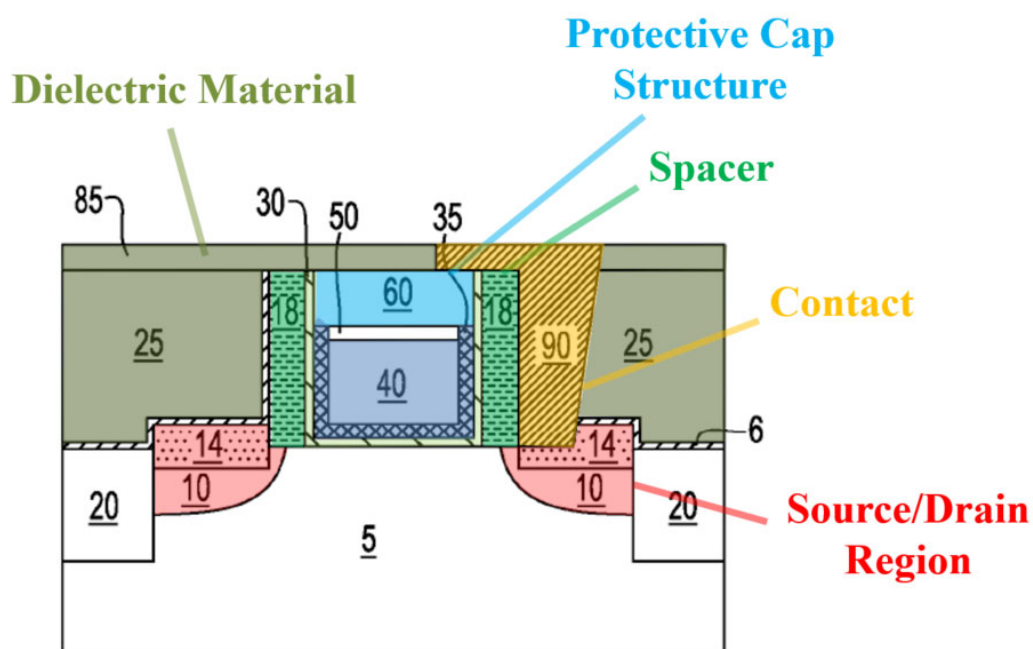


FIG. 6

(*Id.*, FIG. 6 (annotated).)

31. As described by Tsuchiaki-645, such a self-aligned contact formation process makes it possible to form contact holes with increased alignment tolerance because the gate stack and other parts of the transistor are protected by a silicon nitride layer (e.g., like the cap and spacers of Siddiqui discussed above), thereby simplifying manufacturing and reducing cost:

The silicon nitride layer 28 will serve as a barrier layer or an etch-stop layer, i.e., a liner layer, during the contact hole formation through an interlayer dielectric layer (not shown in the drawings) at a later stage. Thanks to this liner layer, it is possible to form a contact hole without accurately aligning the contact holes to the positions of the NiSi regions 26 on the source and drain regions (i.e., borderless contact) because the contact etching (i.e., dielectric etching which could also etch the dielectric material in the STI regions) stops at this liner layer without encroaching the STI region even when the hole opening overlaps the STI region by slight misalignment. Accordingly, it is possible to simplify the device manufacturing process, thereby decreasing the manufacturing costs.

(Ex. 1022, ¶[0081]; *see also* Ex. 1024, ¶[0091] (“The above contact hole fabrication with a large process margin in its position alignment is commonly called as ‘borderless contact formation’. Obviously, thus-attained simplification of device fabrication contributes greatly to reducing the manufacturing cost.”), Ex. 1021,

¶[0119] (“Resulting process tolerance for less accurate alignment of contact-hole patterns to the NiSi layers [on source and drain regions] enables easy contact formation (i.e., ‘borderless contact formation’) and improves manufacturability of the devices. Accordingly the production costs can be reduced”); Ex. 1007, ¶[0008], ¶[0009] (“Borderless contacts and techniques relating thereto help reduce the amount of space required for contacts, and enable production of smaller devices having a tighter pitch.”).)

## **VI. OVERVIEW OF THE '699 PATENT**

32. The '699 patent is entitled “Capping Dielectric Structure for Transistor Gates.” (Ex. 1001, Title.) The '699 patent discloses that “[i]n the fabrication of non-planar transistors, such as tri-gate transistors and FinFETs, non-planar semiconductor bodies may be used to form transistors capable of full depletion with very small gate lengths (e.g., less than about 30nm).” (*Id.*, 3:21-24.) Annotated figure 1 of the '699 patent below shows a non-planar transistor 100 that includes a non-planar transistor fin 112, where a transistor gate 122, which includes gate dielectric layer 124 and gate electrode 126, is formed over the fin 112. (*Id.*, 3:52-4:11.)

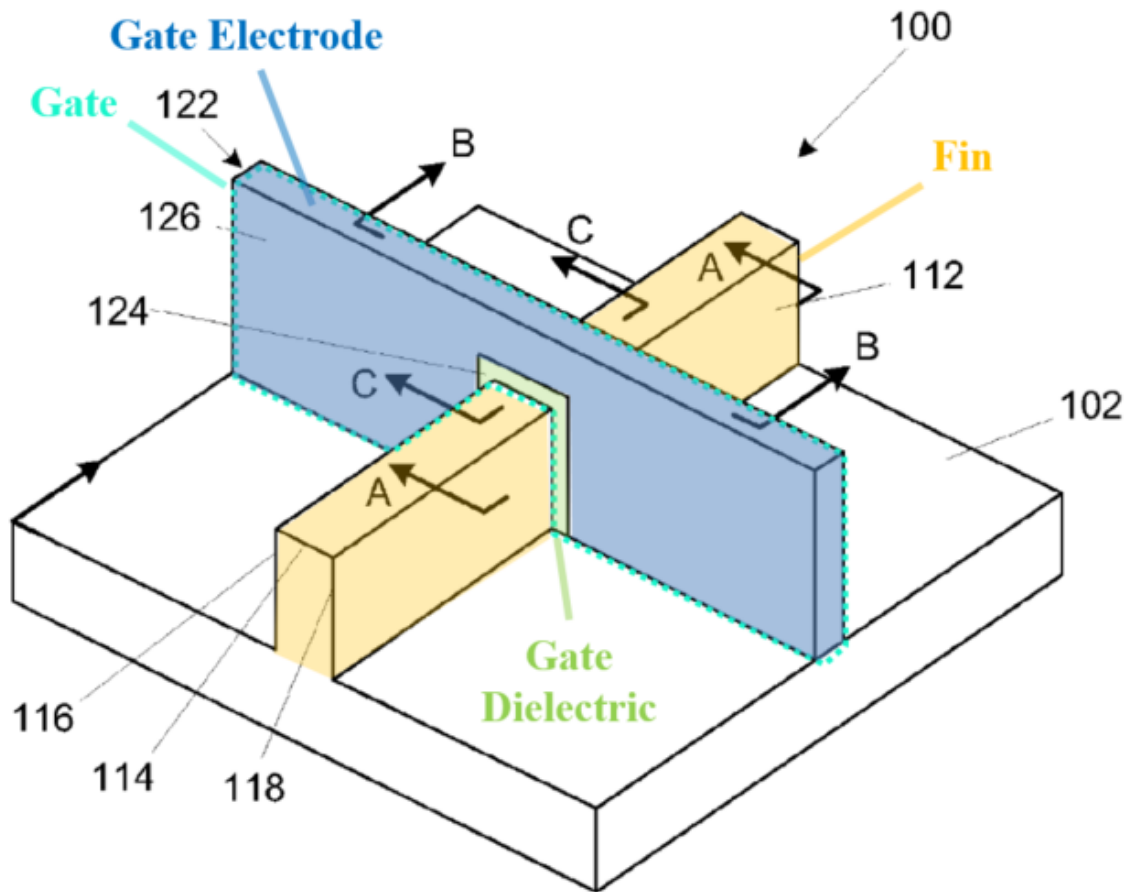


FIG. 1

(*Id.*, FIG. 1 (annotated).)

33. Source and drain regions, which are not shown in figure 1 above, are formed in the fin on opposite sides of the gate electrode. (*Id.*, 4:41-43.) The '699 patent discloses that “[i]n one embodiment, the source and drain regions may be formed by doping the non-planar transistor fins 112,” whereas “[i]n another embodiment, the source and drain regions may be formed by removing [portions] of

the non-planar transistor fins 112 and replacing these portions with appropriate material(s) to form the source and drain regions.” (*Id.*, 4:43-50.) The ’699 patent further discloses that the gate structure for the non-planar transistor can be formed by first forming a sacrificial gate structure that is later removed and replaced with a functional gate structure. Figure 6 below is a cross-sectional view of the non-planar transistor shown in figure 1 along arrows A-A of figure 1, and shows sacrificial gate 136. (*Id.*, 4:51-54, 5:8-11.)

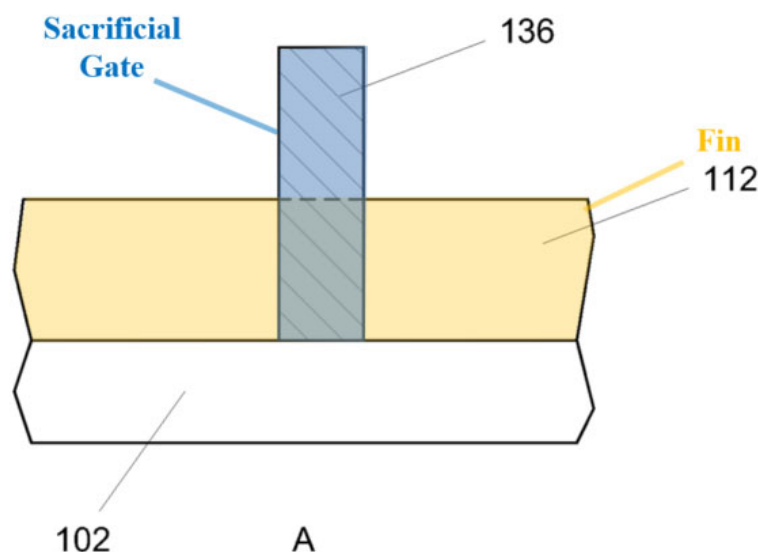


**FIG. 6**

(*Id.*, FIG. 6 (annotated).)

34. As shown in annotated figures 7 and 8 below, gate spacers 144 on sidewalls 146 of the sacrificial gate 136 are formed by first depositing a conformal dielectric layer over the sacrificial gate 136 and substrate 102 and then etching,

where fin spacers can also be formed during formation of the gate spacers. (*Id.*, 5:11-27.)

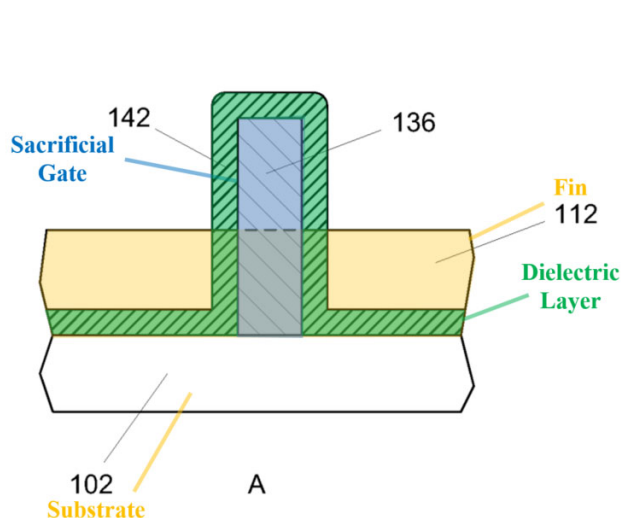


FIG. 7

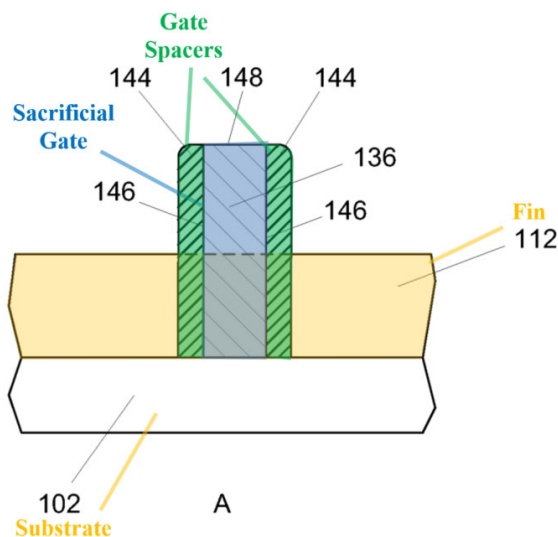


FIG. 8

(*Id.*, FIGs. 7, 8 (annotated).)

35. After forming the gate spacers, source/drain regions are formed (*id.*, 5:28-44, FIG. 9), and then the sacrificial gate 136 is removed to form a gate trench 154 (*id.* 5:54-55, FIG. 11). Gate dielectric material 124 is formed in the gate trench, and then conductive gate material 154 is deposited in the gate trench and excess gate material is removed. (*Id.*, 5:57-6:3.) As shown in annotated figure 16 below, a portion of the gate electrode 126 is removed to form a recess 158. (*Id.*, 6:4-8.)

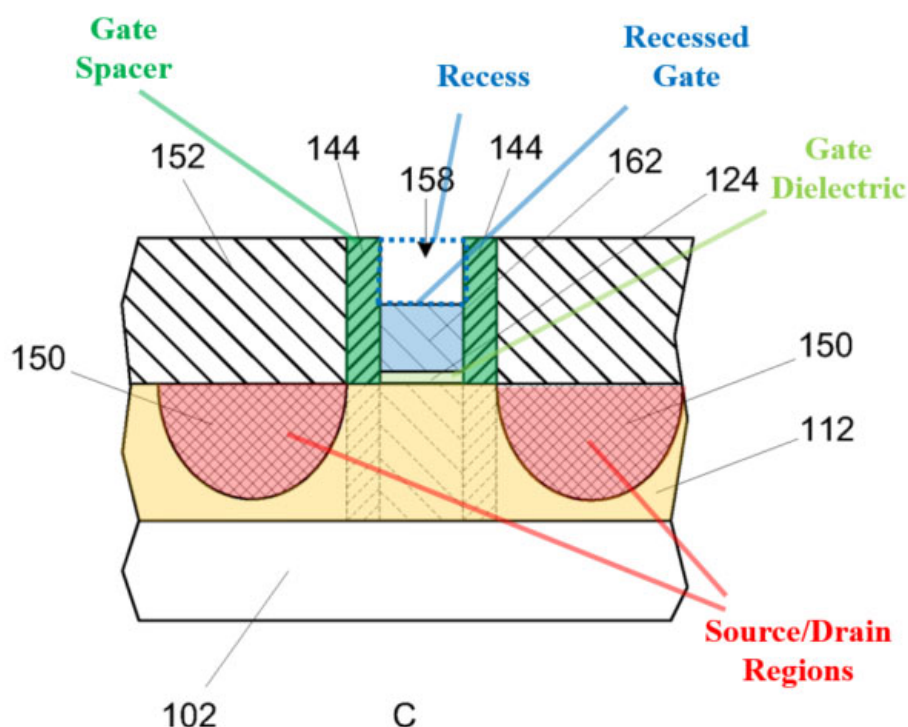


FIG. 16

(*Id.*, FIG. 16 (annotated).)

36. After recessing the gate, a capping layer is formed in the recess, where the capping material may be formed using high density plasma (HPD) dielectric deposition. (*Id.*, 6:9-29.) “After deposition, the capping dielectric material 164 may be planarized to remove excess capping dielectric material 164 (e.g. capping dielectric material 164 not within the recess of FIG. 16) to form a capping dielectric structure 166 on the recessed non-planar transistor gate 162 and between a gate spacers 144, as shown in FIG. 19.” (*Id.*, 7:21-26.)

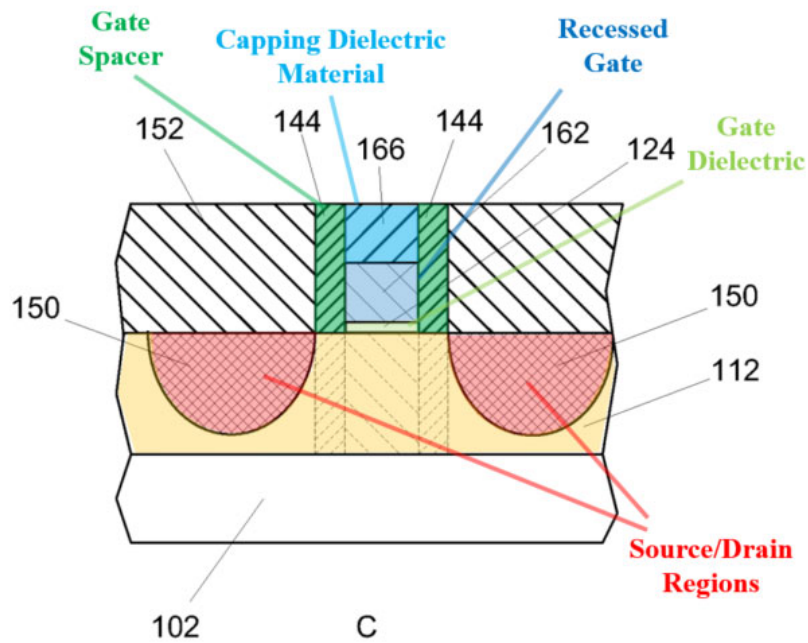


FIG. 19

(*Id.*, FIG. 19 (annotated).)

37. As shown in annotated figure 20 below, a dielectric material layer 168 is deposited overlying the transistor structure, and an etch mask 172 is patterned to include an opening 174. (*Id.*, 7:30-39.)

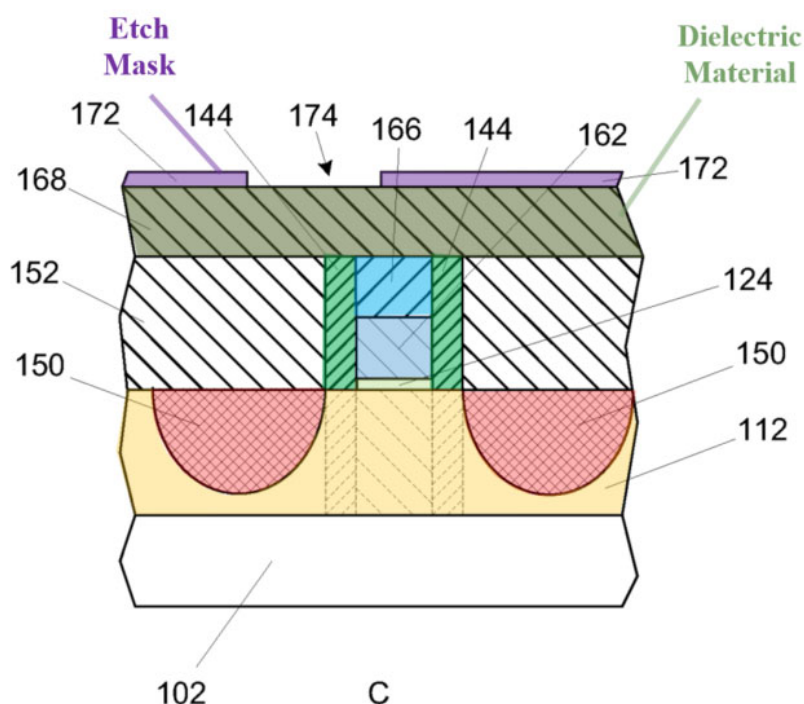


FIG. 21

(*Id.*, FIG. 21 (annotated).)

38. As shown in annotated figure 22 below, a contact opening 182 is formed to expose a portion of the source drain region 150, where the contact opening 182 can be formed by selective etching that removes the dielectric material layers 152 and 168 faster than gate spacers 144 and the capping dielectric structure 166. (*Id.*, 7:39-51.) As the '699 patent recognizes, using such a selective etch to form such a contact opening was known in the art. (*Id.*, 7:52 (“This is known in the art as self-aligning.”).)

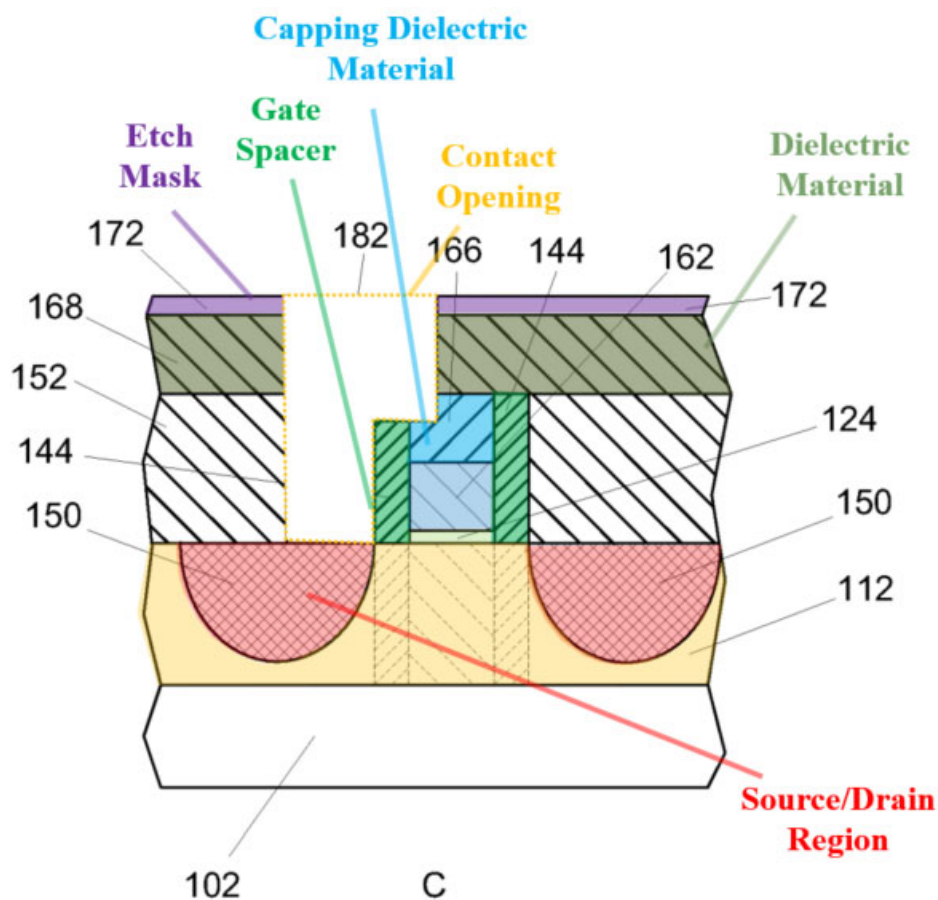


FIG. 22

(*Id.*, FIG. 22 (annotated).)

39. As shown in figure 25 below, conductive contact material 188 is deposited in the contact opening 182 to form the self-aligned source/drain contact 190. (*Id.*, 7:53-54, 7:65-8:1.)

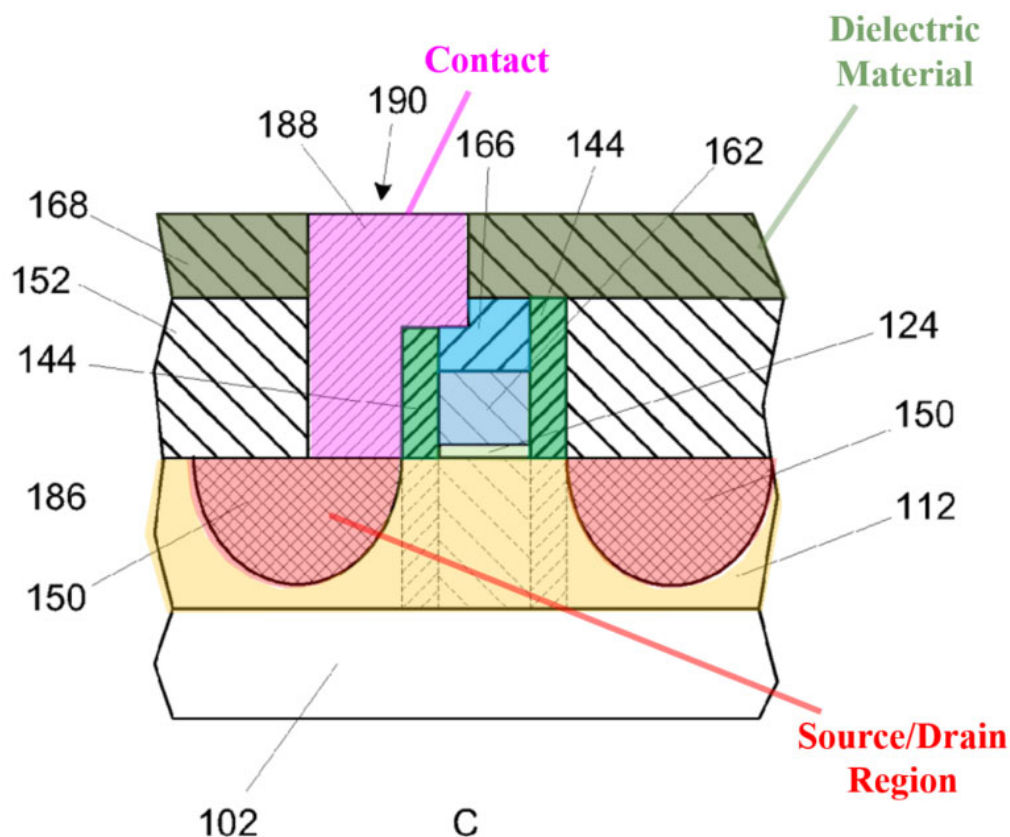


FIG. 25

(*Id.*, FIG. 25 (annotated).)

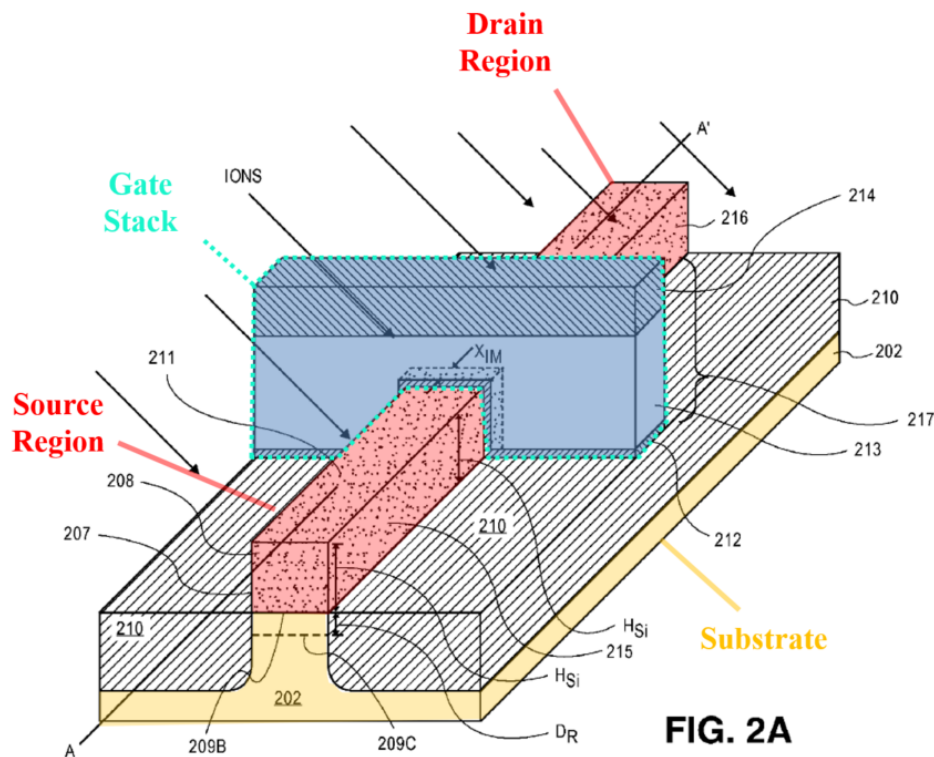
## VII. CLAIM CONSTRUCTION

40. I understand that claim terms are typically given their ordinary and customary meaning, as would have been understood by a person of ordinary skill in the art, at the time of the alleged invention, which I understand is the early 2010s (including September 30, 2011). In considering the meaning of the claims, however, I understand that one must consider the language of the claims, the specification, and the prosecution history of record.

## VIII. OVERVIEW OF THE PRIOR ART

### A. Cappellani

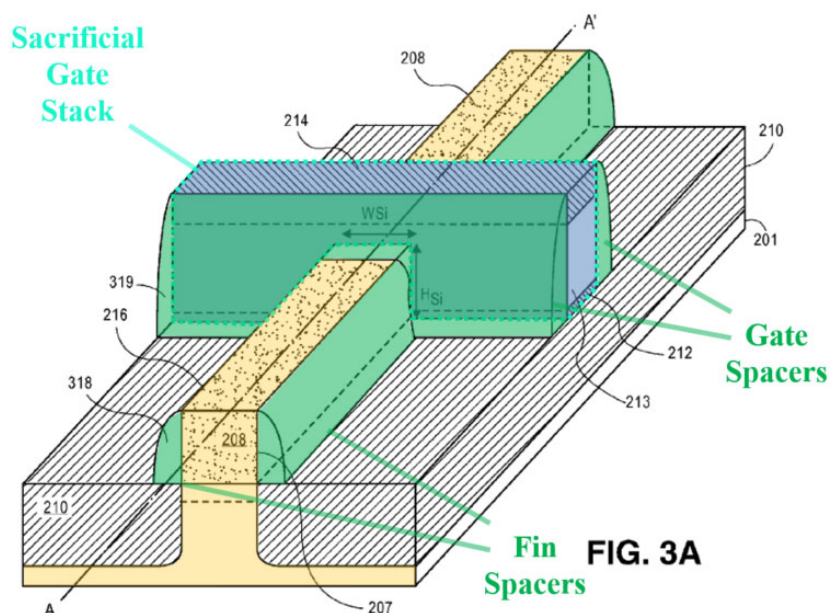
41. Cappellani discloses a FinFET that is formed using a replacement gate process. (Ex. 1005, ¶ [0007], ¶ [0026] (“In the exemplary embodiment, the gate stack 217 is sacrificial and subsequently removed for replacement gate process.”).) As shown in figure 2A below, gate stack 217, which includes a gate dielectric 212, a gate electrode 213, and a gate cap 214, is a sacrificial gate for the FinFET. (Ex. 1005, ¶ [0026], [0028].)



(*Id.*, FIG. 2A (annotated).)

42. As shown in annotated figures 3A and 3B below, Cappellani discloses forming gate stack spacers 319 adjacent to the sacrificial gate and fin spacers 318

adjacent to the fin, where the gate and fin spacers are formed of a dielectric material such as silicon nitride. (*Id.*, ¶[0032].)



(*Id.*, FIG. 3A annotated.)

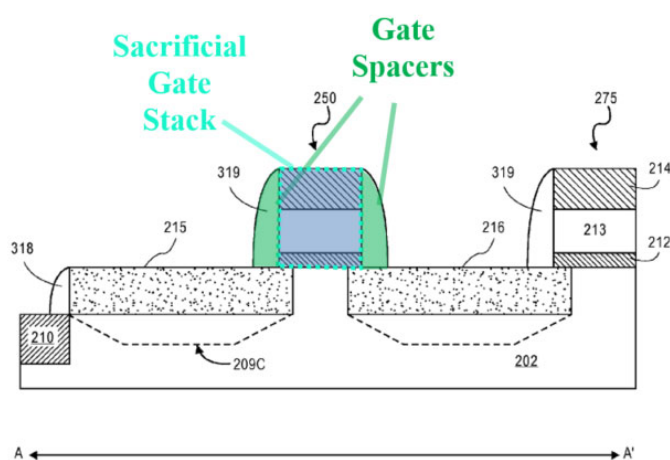
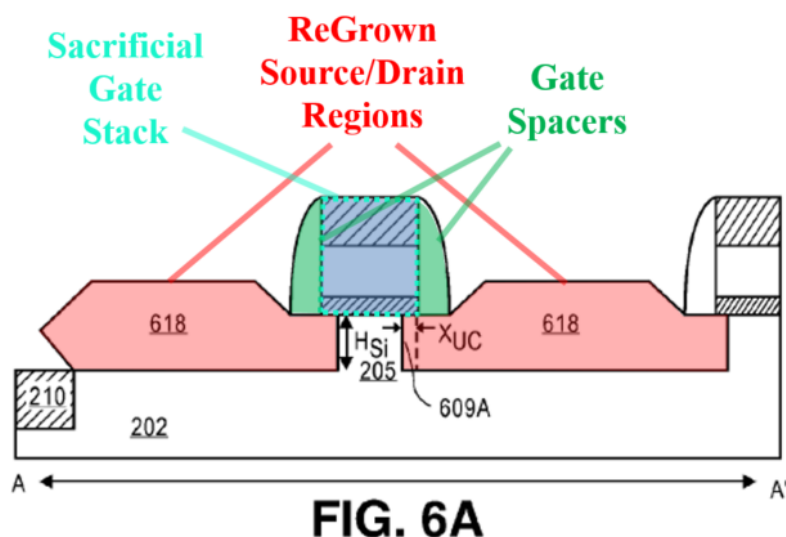


**FIG. 3B**

(*Id.*, FIG. 3B annotated.)

43. As shown in annotated figure 6A below, after formation of the spacers, source/drain regions are regrown using epitaxial deposition. (Ex. 1005, ¶[0040] (“Returning to FIG. 1, at operation 114, the source/drain cavity 420, including the source/drain extension cavity 421, is filled with a material using a selective epitaxial deposition process to form regrown source/drain fin.”), ¶[0041] (“The epitaxial deposition operation 114 therefore regrows source/drain regions and source/drain extensions in one process.”).)

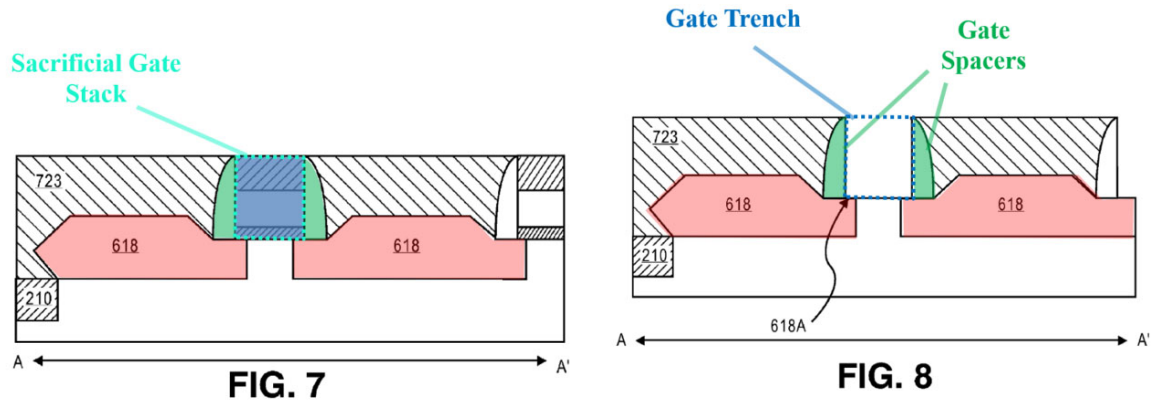


(*Id.*, FIG. 6A (annotated).)

44. After regrowing the source/drain regions, Cappellani discloses removing the sacrificial gate structure shown in figure 7 to form a trench opening between the gate spacers shown in figure 8. (Ex. 1005, ¶[0047] (“Next, for embodiments of the invention in which a replacement metal gate process is used, the gate stack 217 is removed using an etching process at operation 118 to expose the

regrown drain/source extension 618A which filled in the extension cavity 421. ...

FIG. 8 illustrates the trench opening that is formed when the gate stack is etched away.”.)



(*Id.*, FIGs. 7, 8 (annotated).)

45. As shown in annotated figure 9 below, Cappellani discloses forming a functional gate in the gate trench, where the functional gate includes gate dielectric layer 924 and a metal gate electrode layer 926. (Ex. 1005, ¶¶[0048]-[0049].)

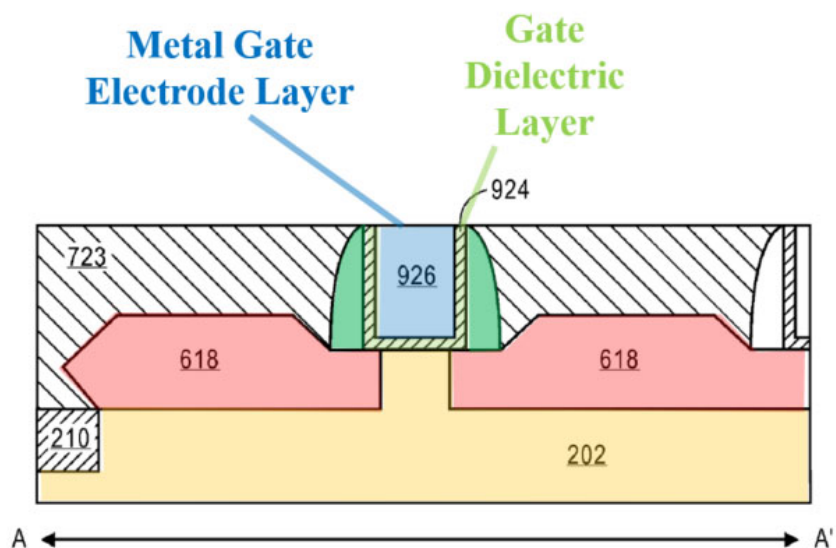
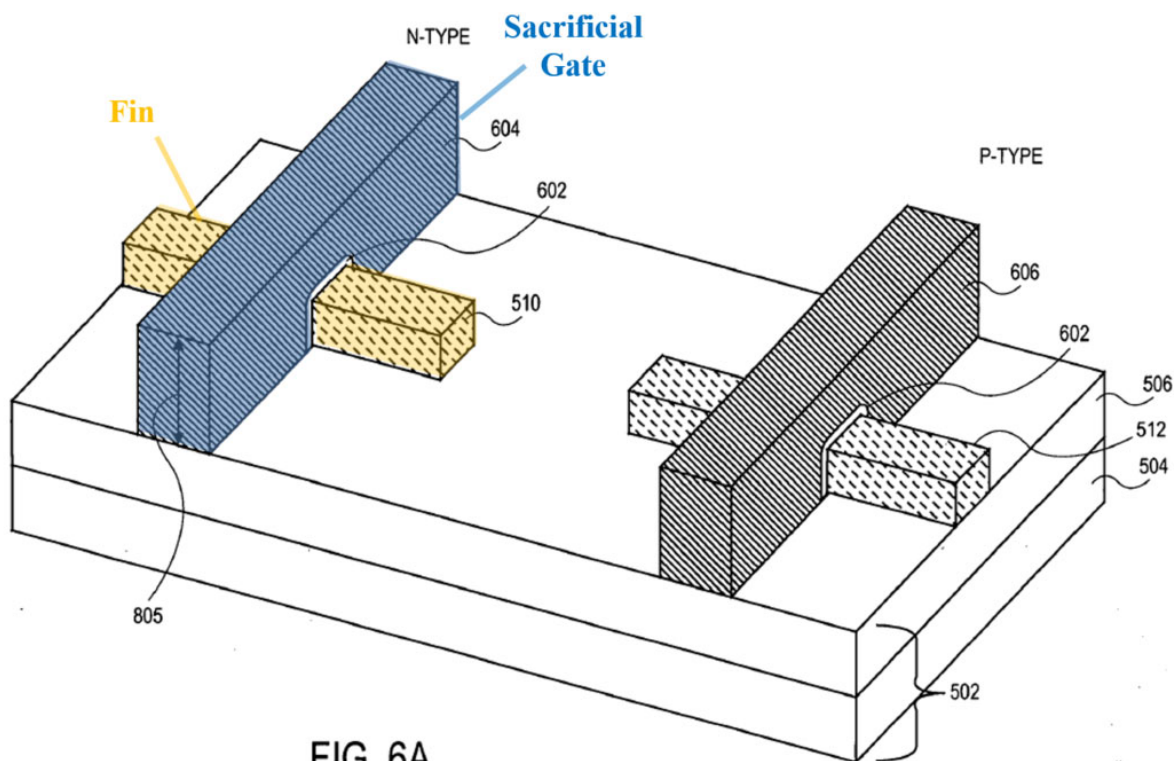


**FIG. 9**

(*Id.*, FIG. 9 (annotated).)

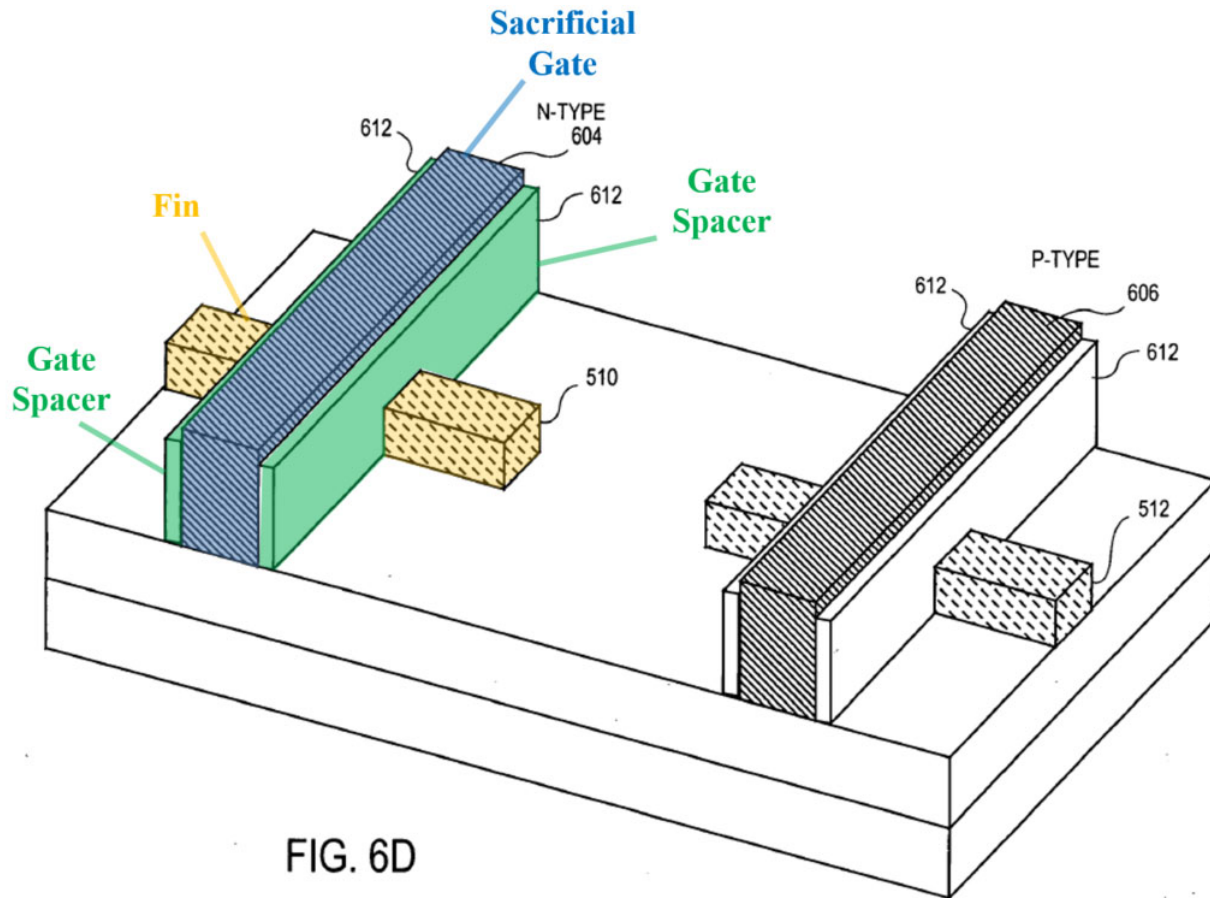
**B. Brask**

46. Like Cappellani, Brask also discloses a FinFET that is formed using a replacement gate process. As shown in annotated figure 6A below, Brask discloses forming a sacrificial gate dielectric layer 602 and a sacrificial gate electrode layer 604 over a semiconductor body or “fin” 510. (Ex. 1008, ¶¶[0046], [0059].)



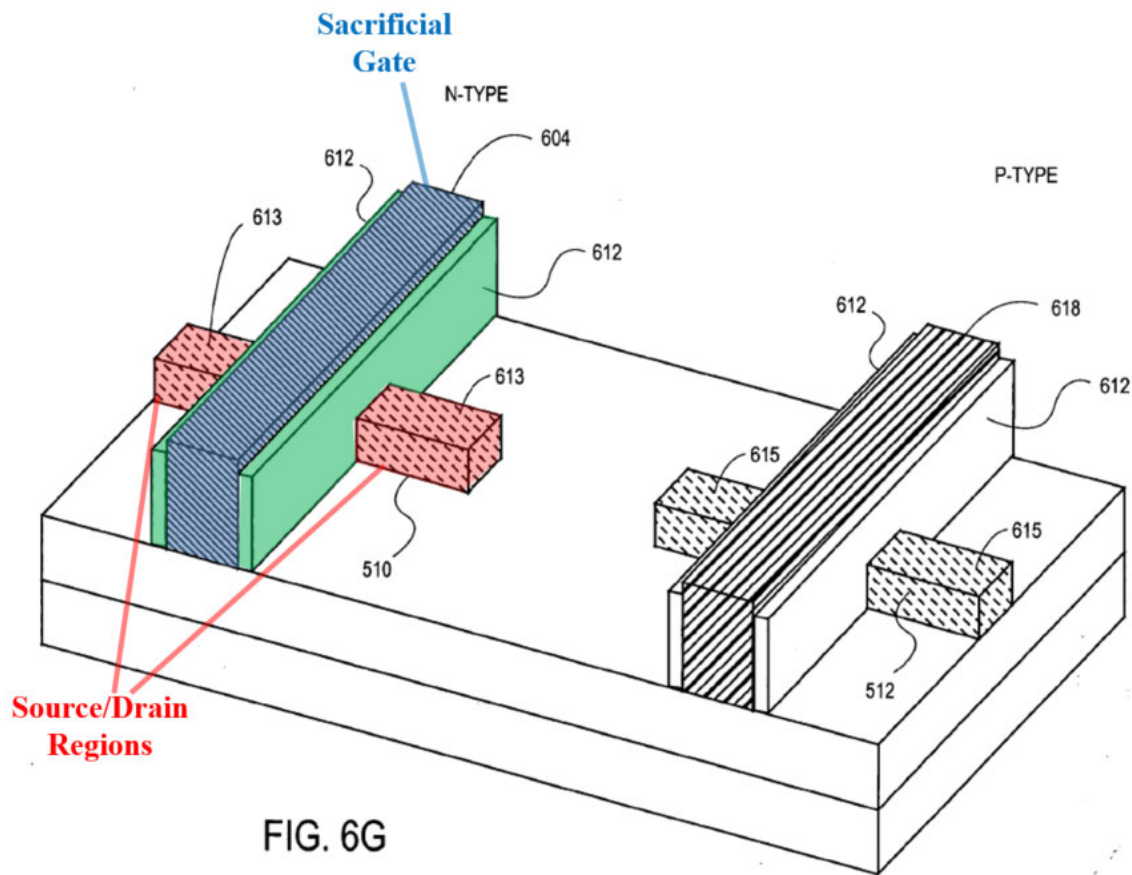
(*Id.*, FIG. 6A (annotated).)

47. As shown in annotated figure 6D below, Brask discloses forming dielectric sidewall spacers 612 adjacent to the sacrificial gate 604. (Ex. 1008, ¶[0065].) Brask discloses that the gate spacers are formed by blanket depositing a dielectric layer and then etching to remove the dielectric material from the areas other than the sidewalls of the gate electrode. (*Id.*)



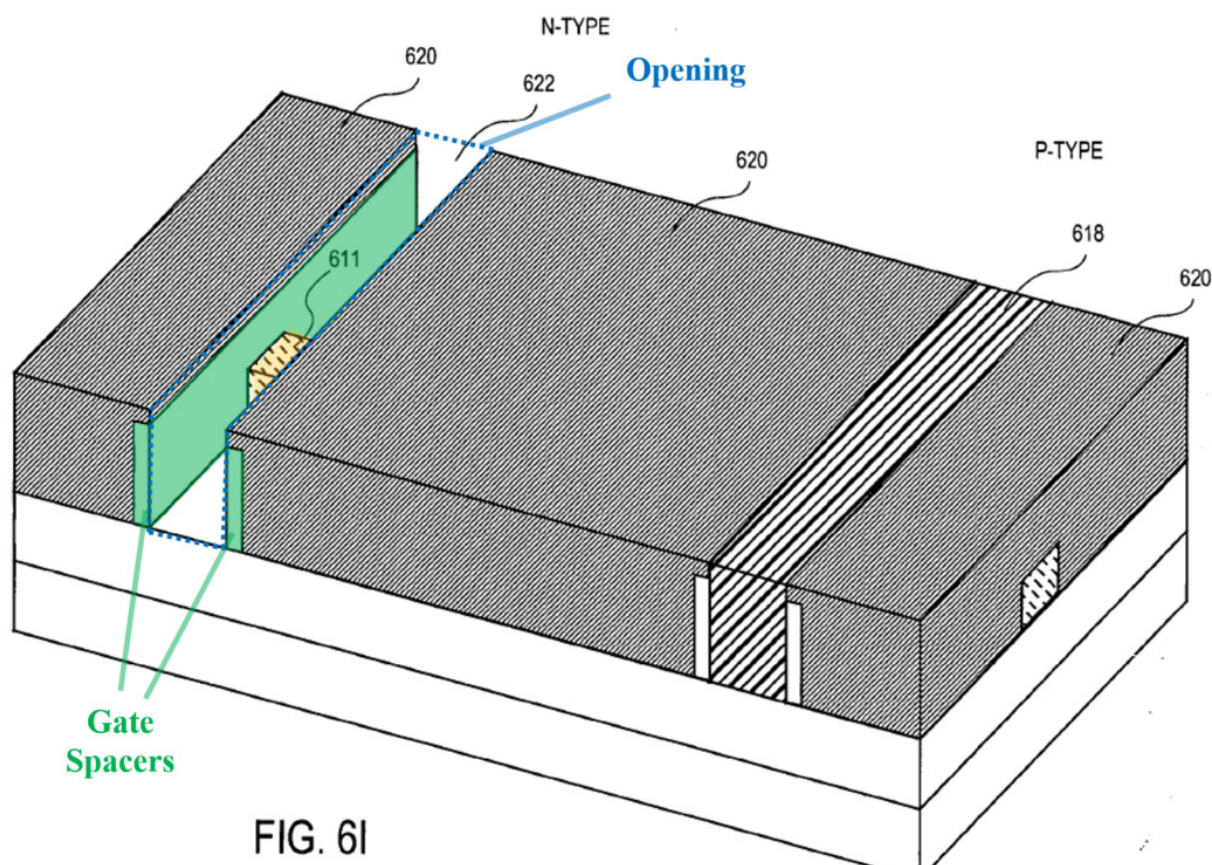
(*Id.*, FIG. 6D annotated.)

48. As shown in annotated figure 6G below, after formation of the spacers, source/drain regions are formed. (*Id.*, ¶¶[0067]-[0069].)



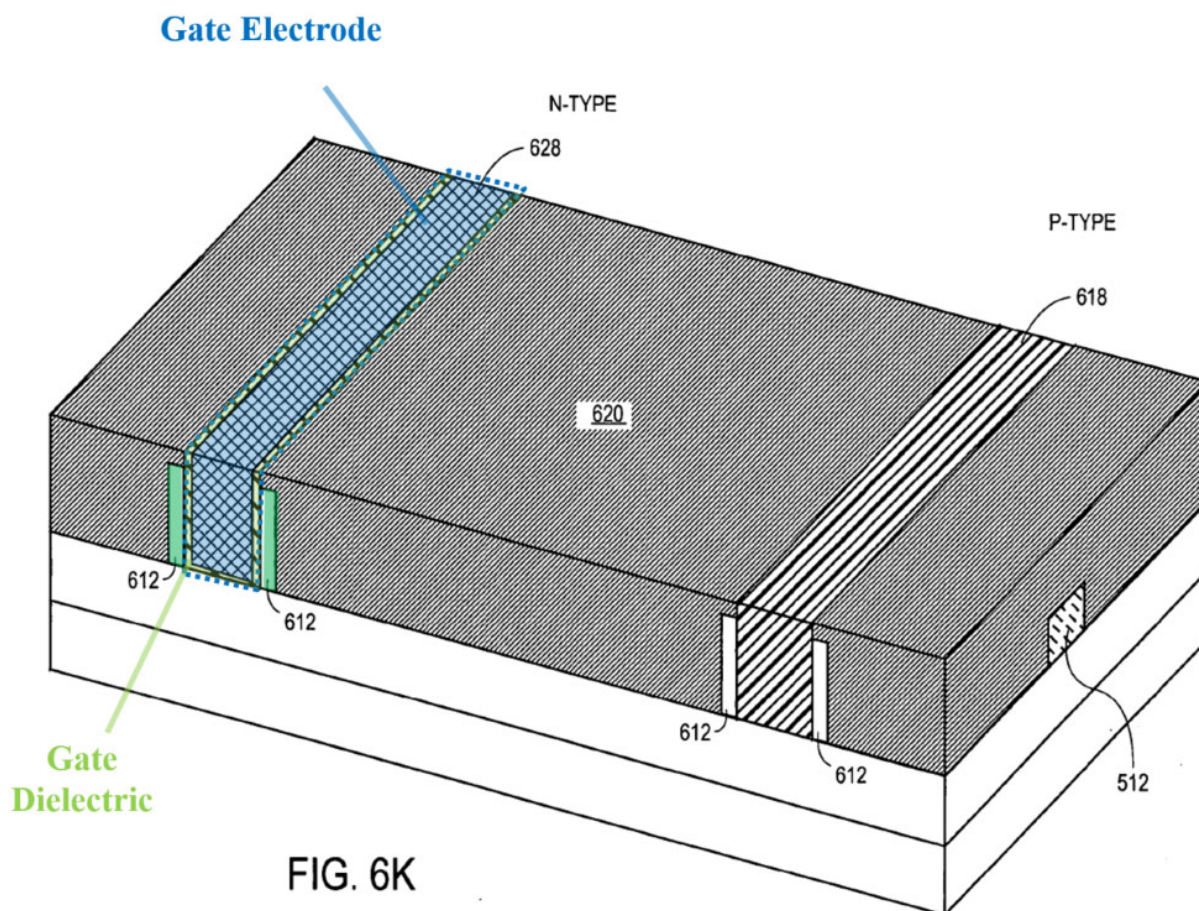
(*Id.*, FIG. 6G (annotated).)

49. As illustrated in annotated figure 6I below, Brask discloses removing the sacrificial gate structure, which includes the gate electrode 604 and gate dielectric layer 602 for the n-type transistor, to form opening 622 between the spacers. (*Id.*, ¶¶[0072]-[0073].)



(*Id.*, FIG. 6I (annotated).)

50. As illustrated in annotated figure 6K below, Brask discloses forming a replacement gate structure in the opening 622, where the replacement gate structure includes gate dielectric film 624 and gate electrode material 626. (*Id.*, ¶[0074].)



(*Id.*, FIG. 6K (annotated).)

### C. Siddiqui

51. Like Cappellani and Brask, Siddiqui also relates to a transistor that is formed using a replacement gate structure, where Siddiqui further discloses forming a self-aligned contact for the transistor. (Ex. 1006, Title (“Structure and Method for Replacement Gate MOSFET with Self-Aligned Contact Using Sacrificial Mandrel Dielectric”; ¶¶[0003], [0017].) As shown in annotated figure 1 of Siddiqui below, protective dielectric layers 18 (i.e., spacers) are formed on the sides of the replacement gate structure 4 of the transistor. (Ex. 1006, ¶[0018] (“protective

dielectric layers 18 that are present on sidewalls of the replacement gate structure 4.”), ¶[0032] (“FIG. 1 further depicts forming a protective dielectric layer 18 on the sidewall of the replacement gate structure. ... In one embodiment, the protective dielectric layer 18 is provided by at least one spacer.”).) Siddiqui further discloses that the spacers can be formed of silicon nitride using a deposition and etch process. (*Id.*, ¶[0032]-[0034].)

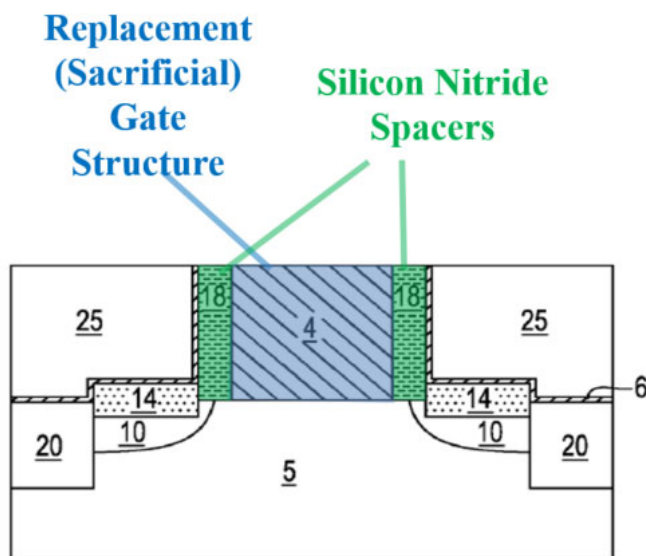


FIG. 1

(*Id.*, FIG. 1 (annotated).)

52. Siddiqui discloses that after removing a sacrificial gate layer, a functional gate structure is formed, which includes a gate dielectric layer 30, work function metal layer 35, and metal fill material 40. (*Id.*, ¶[0040], [0043], [0056], [0057] (“The metal fill material 40, work function metal layer 35 and the gate dielectric layer 30 provide a functional gate structure”).) After formation of the

functional gate structure to complete the transistor, Siddiqui teaches forming a self-aligned contact to the source/drain region of the transistor. (*Id.*, ¶[0004] (“[T]he contacts to at least one of the source and drain region are self aligned, i.e., are not shorted to the gate structure.”).)

53. As a part of forming the self-aligned contact, Siddiqui discloses recessing the functional gate and forming a protective cap structure that, along with the silicon nitride sidewalls, protects the functional gate from damage during the etch process that forms the via hole for the self-aligned contact. (*Id.*, ¶[0058] (“the metal film material 40 may be recessed”), ¶[0062] (“FIG. 4 depicts forming a protective cap structure 60 of the functional gate structure. ... The protective cap structure 60 may be comprised of any dielectric material that can protect the functional gate from being damaged during the etch process that provides the openings to the source regions 10 and the drain regions 15.”), ¶[0070].)

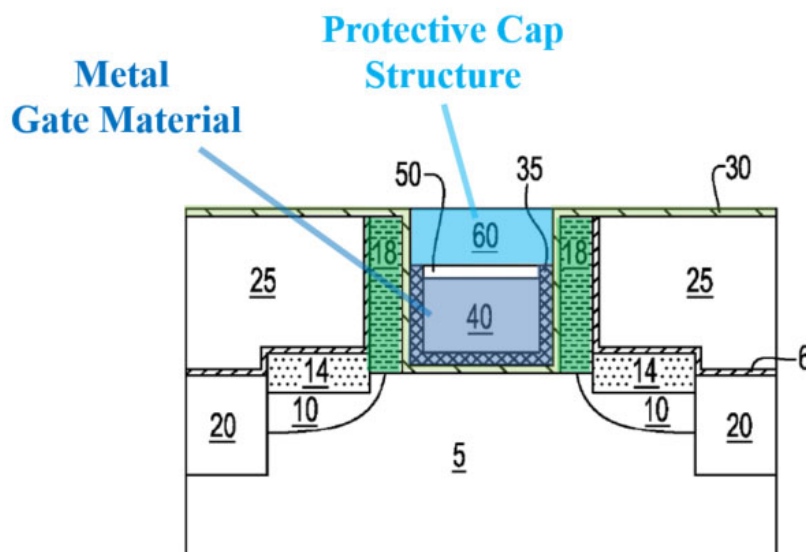


FIG. 4

(*Id.*, FIG. 4.)

54. Siddiqui discloses forming the contact by first etching to form a via 75 through the interlevel dielectric layer 85 and the mandrel dielectric layer 25 to expose the underlying source/drain region. (*Id.*, ¶[0068] (“The interlevel dielectric layer 85 and the mandrel dielectric layer 25 are then patterned and etched to form vias 75 to the source regions 10 and the drain regions 15 using patterning and selective etch process.”).) Annotated figure 6 of Siddiqui shows the via 75 after conductive metal has been deposited in the contact opening to form the contact 90. (*Id.*, ¶[0070].)

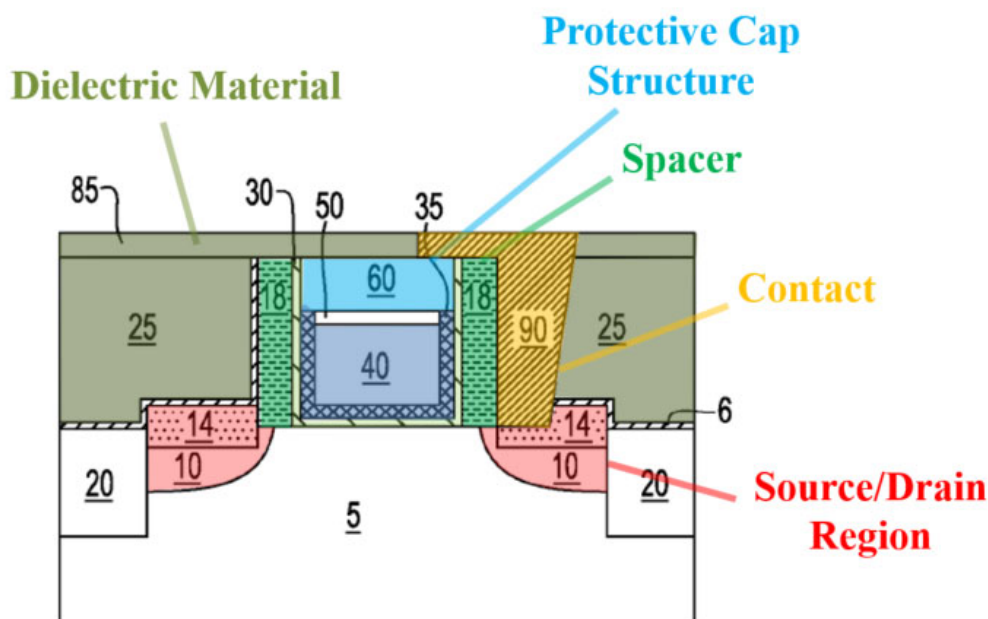


FIG. 6

(*Id.*, FIG. 6 (annotated).)

### D. Cheng

55. Cheng discloses that FinFETs have allowed the size of FET transistors to be reduced, which in turn has reduced the critical dimensions (CDs) of those transistors, thereby making the formation of contacts more difficult. (Ex. 1007, ¶¶[0008]-[0009].) In this context, Cheng discloses that “[b]orderless contacts and techniques relating thereto help reduce the amount of space required for contacts, and enable production of smaller devices having a tighter pitch.” (*Id.*, ¶[0009], ¶[0031].)

56. Cheng’s third embodiment is related to field effect transistors (FETs) that utilize sacrificial gate structures. (Ex. 1007, ¶[0052] (“[T]he third exemplary

embodiment utilizes a gate-last technique, the initial gates are dummy gates (e.g., placeholders) that will be replaced at a later time.”.) Cheng’s transistor formation includes removal of dummy gates (e.g. sacrificial gates) between gate spacers and then formation of a replacement gate structure in the resulting opening between the spacers, where the gate is formed by first depositing a dielectric layer and then depositing conductive gate material in the form of a metal gate. (Ex. 1007, ¶¶[0051], [0053].)

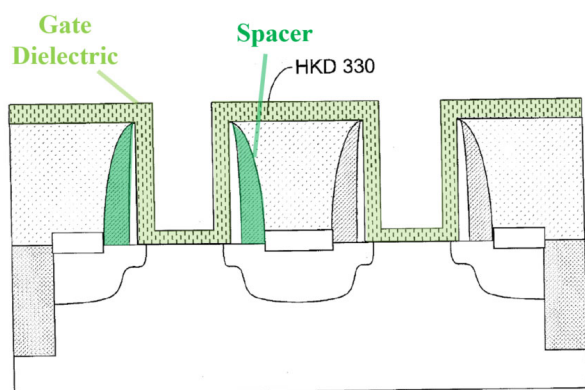


FIG. 22

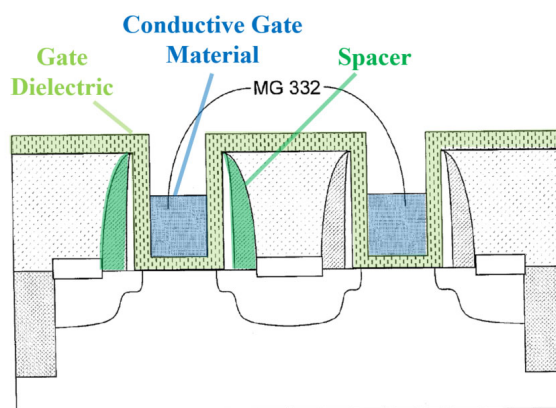
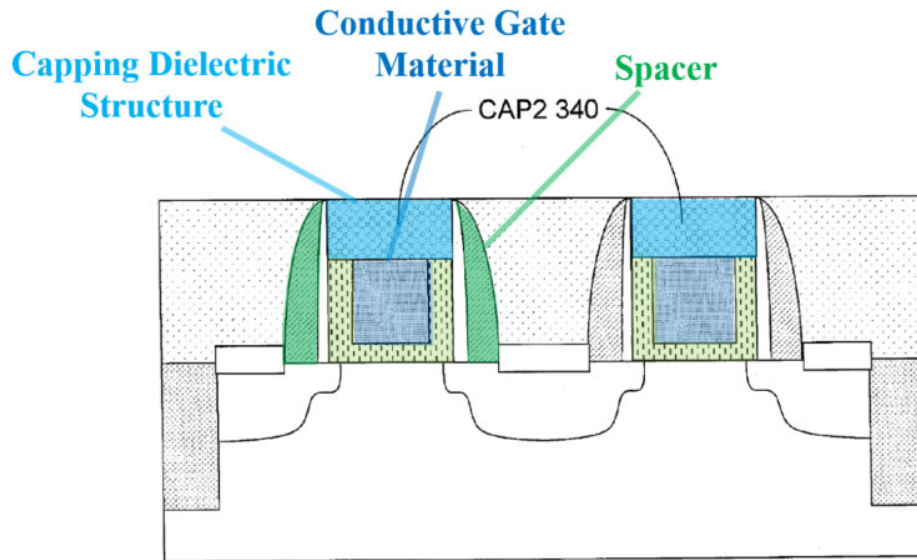


FIG. 23

(*Id.*, FIGs. 22, 23 (annotated).)

57. Cheng further discloses that after depositing the material for the metal gate, the gate material is recessed in order to allow for formation of a cap that, along with gate spacers, isolates the gate from a subsequently formed borderless contact. (*Id.*, ¶[0055] (“The borderless contact is isolated from the gate by a spacer(s) and insulating cap layer (CAP2 340).”))



(*Id.*, FIG. 25.)

58. Cheng further discloses that, after depositing an interlevel dielectric layer, etching is used to form the space for contact area (CA) 326 to expose the underlying source/drain region. (Ex. 1007, ¶[0054] (“A contact mask and a contact RIE are used to remove the ILD material from between the gates, thus forming the space for the borderless contact.”).) Conductive material is deposited in the contact area space to form the contact, which is shown in annotated figure 26 below. (*Id.*, ¶[0054] (“The mask is removed and the contact area (CA) 326 is formed, as illustrated in FIG. 26, by filling the contact with conductive material, such as a metal, a metal containing material or a material comprising a metal, as non-limiting examples.”).)

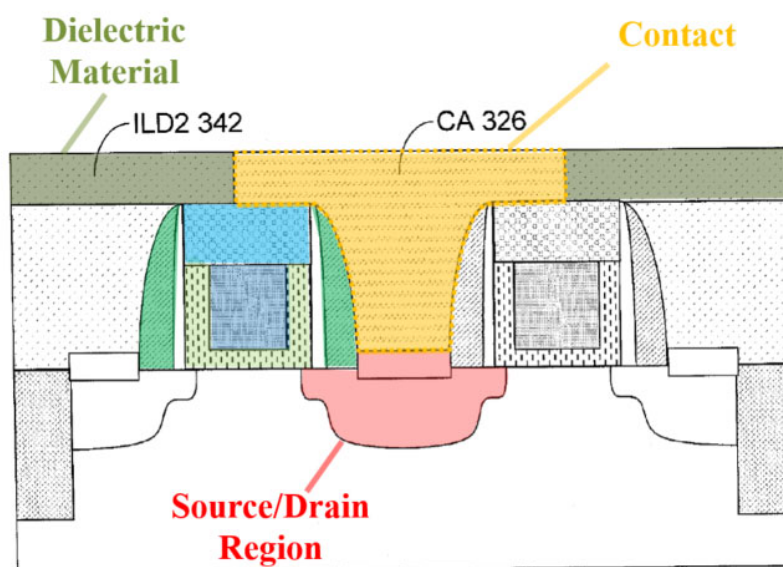


FIG. 26

(*Id.*, FIG. 26 (annotated).)

**E. Park**

59. Park is directed to forming transistors with improved performance, where Park discloses a nitride capping layer overlying the transistor structure. (Ex. 1010, Abstract (“forming a first capping nitride layer covering the gate electrode and the source/drain regions, the first capping nitride layer including a Si—H rich SiN layer”), 1:14-17.) Park further discloses that the nitride capping layer can be formed using high density plasma chemical vapor deposition (HDPCVD). (Ex. 1010, 6:32-37 (“The capping nitride layer 37 may be formed at a temperature of about 350° C. to about 500° C. using, e.g., low pressure chemical vapor deposition (LPCVD), plasma enhanced chemical vapor deposition (PECVD), high density plasma chemical vapor deposition (HDPCVD), or a combination thereof.”).)

**IX. THE PRIOR ART DISCLOSES ALL OF THE FEATURES OF THE CHALLENGED CLAIMS**

**A. Cappellani in Combination with Siddiqui Discloses or Suggests the Features of Claims 1, 2, and 5-11**

60. In my opinion, Cappellani in combination with Siddiqui discloses or suggests all of the features of claims 1, 2, and 5-11 of the '699 patent.

**1. Claim 1**

**a) “A method comprising:”**

61. I understand that “[a] method, comprising” is the preamble to claim 1 of the '699 patent. I have been asked to assume that the preamble is a claim limitation. Under that assumption, in my opinion, Cappellani discloses a method. For example, Cappellani is entitled “Multi-Gate Semiconductor Device with Self-Aligned Epitaxial Source and Drain” (Ex. 1005, Title) and discloses a method for “forming epitaxial source and drain extensions in a multi-gate MOS device (e.g., ‘finfet’),” where a sacrificial gate stack is removed before forming a replacement metal gate. (*Id.*, ¶[0022] (“Described herein are systems and methods of forming epitaxial source and drain extensions in a multi-gate MOS device (e.g., ‘finfet’).”), ¶[0026] (“In the exemplary embodiment, the gate stack 217 is sacrificial and subsequently removed for a replacement metal gate process.”).) Such a method is further discussed below for claim elements 1[b]-1[l]. (*See* my discussion below in





gate for the non-planar transistor. (Ex. 1005, ¶[0026] (“In the exemplary embodiment, the gate stack 217 is sacrificial and subsequently removed for replacement gate process.”), ¶[0028].)

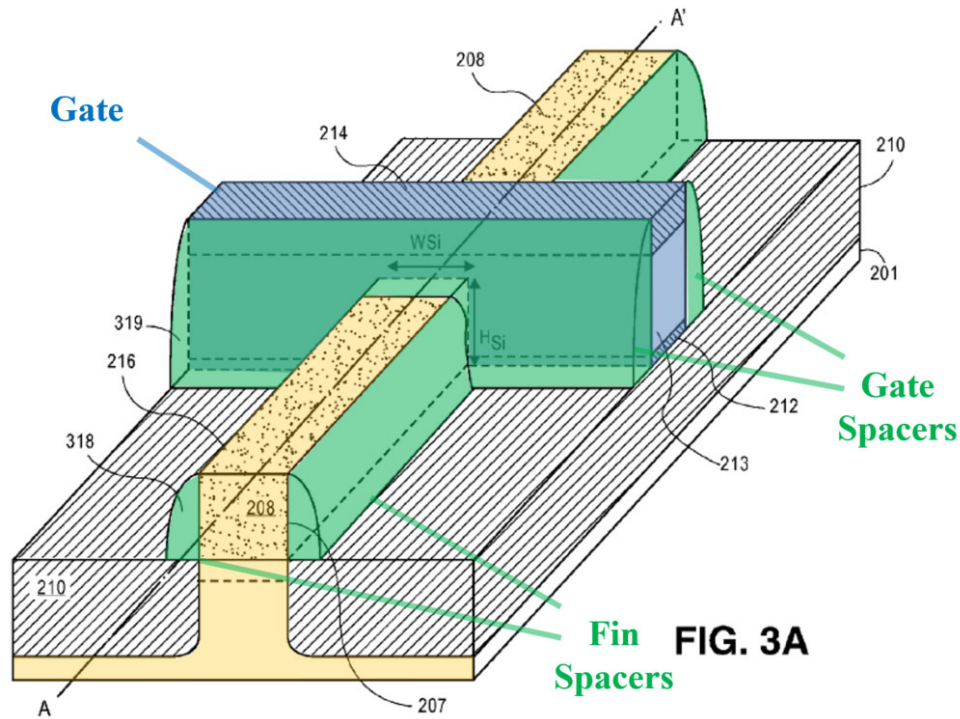
- c) **“depositing a dielectric material layer over the sacrificial non-planar transistor gate and the non-planar transistor fin;”**
- d) **“forming non-planar transistor gate spacers from a portion of the dielectric material layer adjacent the sacrificial non-planar transistor gate;”**

64. In my opinion, Cappellani in view of Siddiqui discloses or suggests these limitations. For example, as shown in annotated figures 3A and 3B below, Cappellani discloses forming gate stack spacers 319 (“non-planar transistor gate spacers”) adjacent to the sacrificial gate, where the gate spacers are formed of dielectric material:

Returning to FIG. 1, at operation 108, **spacers are formed on either side of the gate stack** and the semiconductor fin. The **spacers may be formed using conventional dielectric materials, including but not limited to silicon oxide or silicon nitride.** The width of the spacers may be chosen based on design requirements for the multi-gate transistor being formed. FIGS. 3A and 3B illustrate **a gate stack spacer 319 formed on sidewalls of the gate stack 217. Formation of the gate stack spacer 319 also forms a fin spacer 318 on the sidewalls of the semiconductor**

**fin**, in particular adjacent to the doped fin region 208, and disposed on the isolation region 210.

(Ex. 1005, ¶[0032] (emphasis added).)



(*Id.*, FIG. 3A (annotated).)

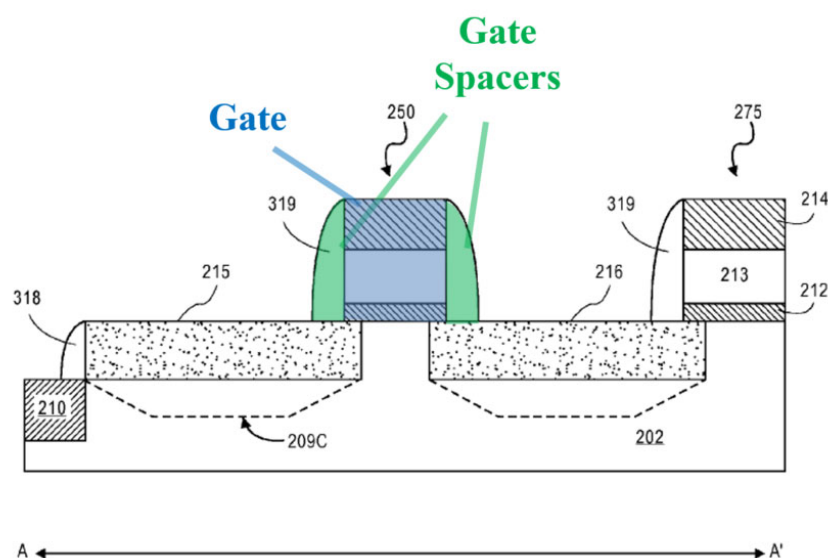


**FIG. 3B**

(*Id.*, FIG. 3B (annotated).)

65. Cappellani does not explicitly disclose forming the gate spacers by first depositing the dielectric material for the spacers over the sacrificial gate and fin and then forming the spacers from that dielectric material that is deposited over the gate and fin. However, formation of gate spacers using blanket deposition of the dielectric material for the gate spacers followed by etching was a well-known and widely-used technique for gate spacer formation, and a person of ordinary skill in the art would have been motivated to form Cappellani's gate spacers in such a

manner. (Ex. 1008<sup>1</sup>, ¶[0065] (“dielectric sidewall spacers 612 can be formed along opposite sidewalls of the sacrificial gate electrodes 604 and 606 ... by any **well known techniques**, such as by blanket depositing the conformal sidewall spacer dielectric over the substrate including the top surface and sidewalls of the sacrificial gate electrodes 604 and 606 as well as on the top surface and sidewalls of semiconductor bodies 510 and 512 as well as onto the exposed surface of the insulating substrate. ... The dielectric spacer material is then anisotropically etched back to remove the dielectric spacer material from a horizontal surface (e.g., top surface) of the sacrificial gate electrodes 604 and 606 and the top surface of the semiconductor bodies 510 and 512 and insulating substrate 602, while leaving spacer material on the vertical surfaces (e.g., sidewalls) of sacrificial gate electrodes 604 and 606 to form sidewall spacers”) (emphasis added), ¶[0053] (“Spacers 540 can be formed by blanket **depositing** a conformal dielectric film, such as but not limited to silicon nitride, silicon oxide, silicon oxynitride or combination thereof over the substrate include the gate electrodes 526 and 528 and semiconductor bodies 510 and 512. ... Next, the dielectric film is anisotropically **etched** by, for example, plasma

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<sup>1</sup> I refer to Brask, Furukawa, Cheng, Tschiki-877, Tschiki-440, Tschiki-645, Chen, and Kikuchi to demonstrate the knowledge of a person of ordinary skill in the art at the time of the alleged invention.

etching or reactive ion etching to form the sidewall spacers 540.”); Ex. 1023, ¶[0016] (“Nitride spacers 122 are formed by depositing conformal silicon nitride layer followed by directional RIE of nitride to etch off the nitride on the horizontal surface leaving the nitride spacer on the vertical surfaces of gate stack.”); Ex. 1007, ¶[0039] (“formation of oxide and/or nitride spacers around the gate stacks (e.g., via **deposition and etching** or oxide growth)”) (emphasis added); Ex. 1022, ¶[0075] (“[A] silicon nitride layer having a thickness of 20 nm is deposited by using the CVD method. Thereafter, an anisotropy etching such as the RIE process is performed so as to the silicon nitride layer being selectively remained at the vertical side portions of the gate electrode 16, thereby forming gate sidewalls 20.”); Ex. 1021, ¶[0106] (“A silicon nitride (SiN) film of e.g., 10 nm in film thickness is then deposited on the entire surface by CVD. ... Anisotropic etching such as RIE is then performed to form SiN gate sidewalls ... on both sides of the gate electrode”); Ex. 1024 ¶[0072], (“Then, by conformally depositing a stack of silicon nitride (SiN) film ... and successively RIE-etching the stacked films, double-layered gate sidewalls ... are formed”); Ex. 1011, 4:28-34 (“Two material layers (not shown in the figures) are formed by chemical vapor deposition (CVD) processes to cover the gates 112 and the semiconductor substrate 110. An anisotropic etching process is subsequently performed on the material layers to turn the two material layers into liners 130 and spacers 132. Each of the liners 130 is positioned around the sidewall of each gate

112, and each of the spacers 132 is positioned on the sidewall of the corresponding liner 130.”); Ex. 1013, 5:40-43 (“Thereafter, an insulating film is formed on the entire upper surface of the silicon substrate. The insulating film is then etched back to be left as insulating spacers 38 beside the gate electrodes 35.”).)

66. Indeed, forming gate spacers using conformal deposition followed by anisotropic etching was well-known long before the alleged invention date. (Ex. 1025, 595-596 (“A conformal deposition process produces a thicker film at the edge of the gate-to-active area step than on flat areas. Thus, an anisotropic dry-etch process will clear the oxide in the flat areas while leaving spacers at the sidewalls of the poly gate.”), FIG. 9-31.)

67. Indeed, blanket depositing the dielectric material over both the gate and the fin and then etching to form the spacers is consistent with Cappellani’s disclosure that the gate spacers and source/drain spacers are formed simultaneously. (Ex. 1005, ¶[0032] (“Formation of the gate stack spacer 319 also forms a fin spacer 318 on the sidewalls of the semiconductor fin, in particular adjacent to the doped fin region 208, and disposed on the isolation region 210.”).) As a person of ordinary skill in the art would have appreciated, performing a blanket deposition over the entirety of the transistor structure and then using the same etching operation to produce the gate and fin spacers would have been an efficient way to form both sets of spacers using a minimal number of steps. Therefore, a person of ordinary skill in the art would

have been motivated to use such a well-known technique for forming the gate spacers. As a person of ordinary skill in the art would have appreciated, using a blanket deposition and etching process for forming the spacers in Cappellani's transistor would have been nothing more than the application of a known technique (forming spacers by blanket deposition and etching) to a similar structure (the transistor structure including the sacrificial gate stack and fin) to achieve a predictable result (spacers for the transistor).

68. I have been asked to assume a scenario in which Cappellani alone does not disclose or suggest depositing a dielectric material layer over the sacrificial gate and then forming gate spacers from a portion of that dielectric material as recited in claim 1. With such a scenario in mind, it is my opinion that a person of ordinary skill in the art would have been motivated to form gate spacers for a transistor like that disclosed by Cappellani in view of Siddiqui. Siddiqui discloses forming spacers on sidewalls of a gate structure in a transistor using a deposition and etch process, and, in view of Siddiqui and their knowledge of the state of the art, a person of ordinary skill in the art would have had good reason to form the spacers in a transistor like that disclosed by Cappellani by first blanket depositing the dielectric material and then etching that material to form the spacers.

69. Siddiqui, like Cappellani, discloses a transistor structure where a sacrificial gate is first formed, and then later removed and replaced with a functional

gate structure. (Ex. 1006, Abstract, ¶[0022] (“Still referring to FIG. 1, a replacement gate structure 4 is formed overlying a channel region of the substrate 5. As used herein, a ‘replacement gate structure’ is a material having a geometry and location on the substrate 5 that determines the location for the later formed functional gate structure that is substituted for the replacement gate structure once the replacement gate structure has been removed.”).)

70. As shown in annotated figure 1 of Siddiqui below, protective dielectric layers 18 (i.e., spacers) are formed on the sides of the replacement gate structure 4 of the transistor. (Ex. 1006, ¶[0018] (“protective dielectric layers 18 that are present on sidewalls of the replacement gate structure 4.”), ¶[0032] (“FIG. 1 further depicts forming a protective dielectric layer 18 on the sidewall of the replacement gate structure 4. ... In one embodiment, the protective dielectric layer 18 is provided by at least one spacer.”).)

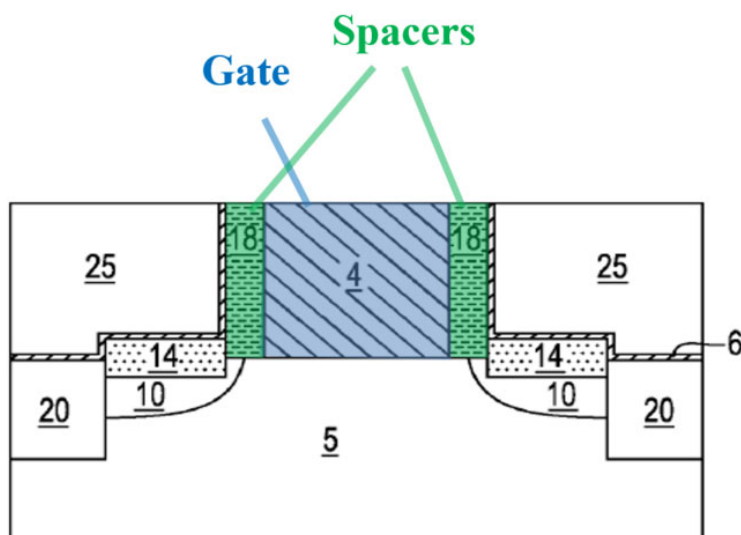


FIG. 1

(Ex. 1006, FIG. 1 (annotated).)

71. Siddiqui further discloses that the spacers can be formed of silicon nitride using a deposition and etch process. (Ex. 1006, ¶[0033] (“The protective dielectric layer may be comprised of a dielectric material, such as a nitride, e.g., silicon nitride.”), ¶[0034], ¶[0032] (“The at least one spacer may be formed on the sidewall of the replacement gate structure 4 using **deposition and etch process.**”)) (emphasis added).)

72. While Siddiqui does not expressly state that the deposition performed is a “blanket deposition” that covers the sacrificial gate and other structures of the transistor, a person of ordinary skill in the art would have had good reason to use such a blanket deposition in forming the gate spacers in a transistor like that of Cappellani. Siddiqui forms the spacers based on a deposition followed by an etch,

which would have disclosed or suggested a blanket deposition to a person of ordinary skill in the art because, as I discuss above, a blanket deposition followed by etching was well-known and widely used. Moreover, such an operation is simple and straightforward as opposed to other more complex options that might exist. Furthermore, a person of ordinary skill in the art would have been motivated to use a blanket deposition, which covers the sacrificial gate structure and the fins, followed by etching in order to be able to produce the gate and fin spacers in the same step as is disclosed by Cappellani. (Ex. 1005, ¶[0032].)

73. A person of ordinary skill in the art implementing a transistor device like that disclosed by Cappellani would have looked to Siddiqui, particularly because Cappellani and Siddiqui are references in the same field and disclose transistor devices that utilize replacement gate structures with gate spacers on the sidewall of the replacement gate structure. Having looked to Siddiqui, such a person of ordinary skill in the art would have had good reason to form the gate spacers 319 in Cappellani using a deposition and etch process like that disclosed by Siddiqui, where the deposition of the dielectric material (e.g., silicon nitride) deposits material over the sacrificial non-planar transistor gate and the non-planar transistor fin.

74. Cappellani discloses that the spacers are formed of “conventional dielectric materials” including, for example, silicon nitride (Ex. 1005, ¶[0032]), but Cappellani does not disclose the details as to how the silicon nitride spacers are

formed. Therefore, having looked to Siddiqui, a person of ordinary skill in the art would have had good reason to use a deposition and etch technique as disclosed by Siddiqui to form the spacers in a transistor like that disclosed by Cappellani, where, in view of their knowledge of the state of the art, such a person of ordinary skill in the art would have performed a blanket deposition as was common in spacer formation, where such a blanket deposition promotes Cappellani's simultaneous formation of gate and fin spacers.

75. Based on their knowledge of such well-known spacer formation techniques and Siddiqui's disclosure of using deposition and etching to form the gate spacers, a person of ordinary skill in the art would have had a reasonable likelihood of success. A person of ordinary skill in the art would have understood that, to the extent Siddiqui's disclosure is directed to a planar MOS device, Siddiqui's teachings would also be applicable to non-planar devices like the FinFET disclosed by Cappellani. While FinFET's have more complex gate and channel structures, it was well understood that they could be fabricated using conventional process technologies like those used to manufacture planar MOSFETs. (Ex. 1009<sup>2</sup>, Abstract ("a novel self-aligned double-gate MOSFET, FinFET is proposed...The quasiplanar

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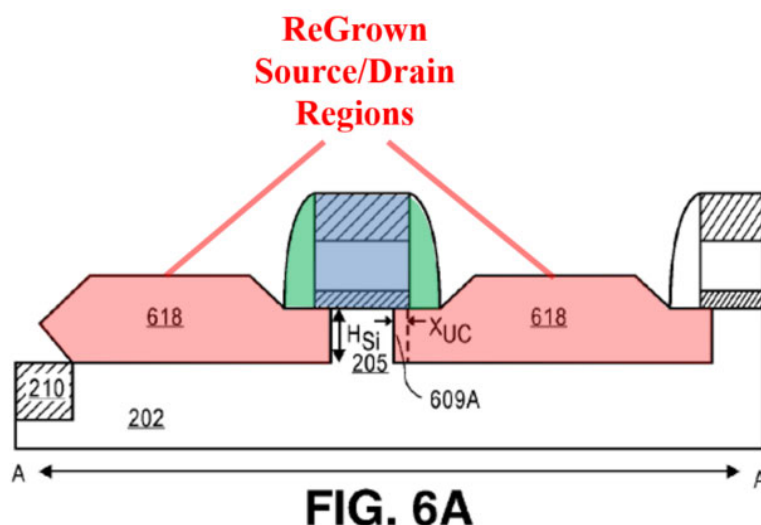
<sup>2</sup> I cite to Hisamoto to demonstrate the knowledge of a person of ordinary skill in the art at the time of the alleged invention.

nature of the new variant of the vertical double-gate MOSFETs can be fabricated relatively easily using the conventional planar MOSFET process technologies.”), 2324 (“In spite of its double-gate structure, FinFET is close to its root, the conventional MOSFET in terms of layout and fabrication.”).) Indeed, the ’699 patent states that “[a]lthough embodiments herein are described in terms of non-planar transistors and replacement gate techniques, the subject matter is not so limited, as the subject matter may be used in planar transistors and in non-replacement gate applications” without any further explanation. (Ex. 1001, 3:47-51.) Such a statement supports the understanding that a person of ordinary skill in the art would have understood that techniques for forming aspects of planar transistors are applicable to non-planar transistors and vice-versa.

**e) “forming a source/drain region;”**

76. In my opinion, the Cappellani-Siddiqui combination discloses or suggests this feature. For example, as shown in annotated figure 6A below, which is a cross-sectional view of a stage of fabrication of Cappellani’s multi-gate device, source/drain regions are regrown (“formed”) using epitaxial deposition. (Ex. 1005, ¶[0040] (“Returning to FIG. 1, at operation 114, the **source/drain cavity 420**, including the source/drain extension cavity 421, **is filled with a material using a selective epitaxial deposition process to form regrown source/drain fin**. In an embodiment depicted in FIGS. 6A and 6B, the material forming the source/drain fin

618 induces a strain on the channel region 205.”) (emphasis added), ¶[0041] (“The epitaxial deposition operation 114 therefore **regrows source/drain regions** and source/drain extensions in one process.”) (emphasis added).)

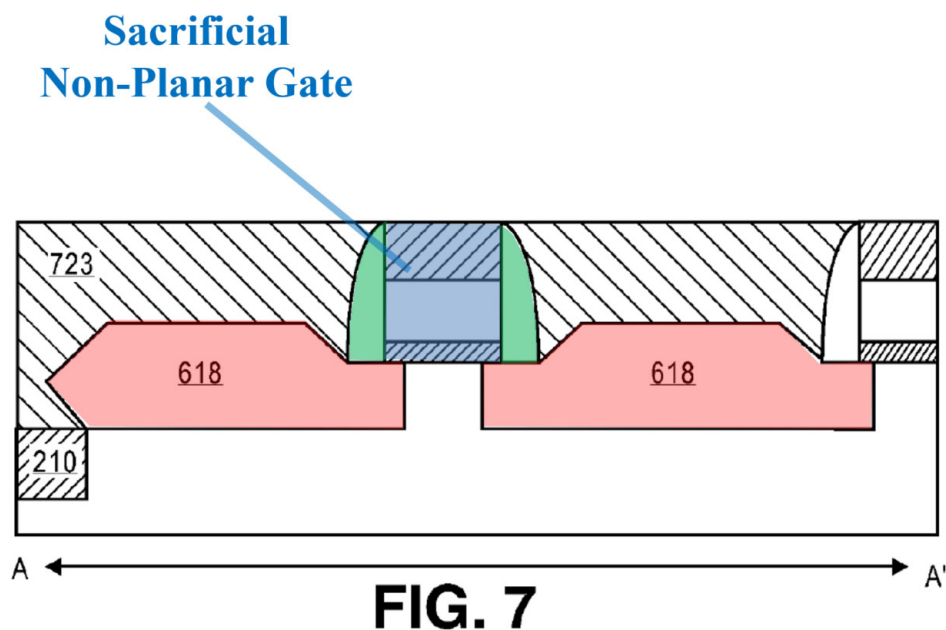


(*Id.*, FIG. 6A (annotated).)

- f) **“removing the sacrificial non-planar transistor gate to form a gate trench between the non-planar transistor gate spacers and expose a portion of the non-planar transistor fin;”**

77. In my opinion, the Cappellani-Siddiqui combination discloses or suggests this feature. For example, Cappellani discloses removing the sacrificial gate structure (“sacrificial non-planar transistor gate”) shown in figure 7 to form a trench opening (“gate trench between the non-planar gate spacers”) shown in figure 8, where the removal of the gate structure exposes the channel region 205 (“a portion of the non-planar transistor fin”). (Ex. 1005, ¶[0047] (“Next, for embodiments of

the invention in which a replacement metal gate process is used, the gate stack 217 is removed using an etching process at operation 118 to expose the regrown drain/source extension 618A which filled in the extension cavity 421. Methods for removing layers of the gate stack 217 are well known in the art. ... FIG. 8 illustrates the trench opening that is formed when the gate stack is etched away.”), ¶[0048] (“Returning to FIG. 1, if the gate dielectric layer is removed, a new gate dielectric layer may be deposited into the trench opening over the channel region 205 at operation 120.”).)



(*Id.*, FIG. 7 (annotated).)

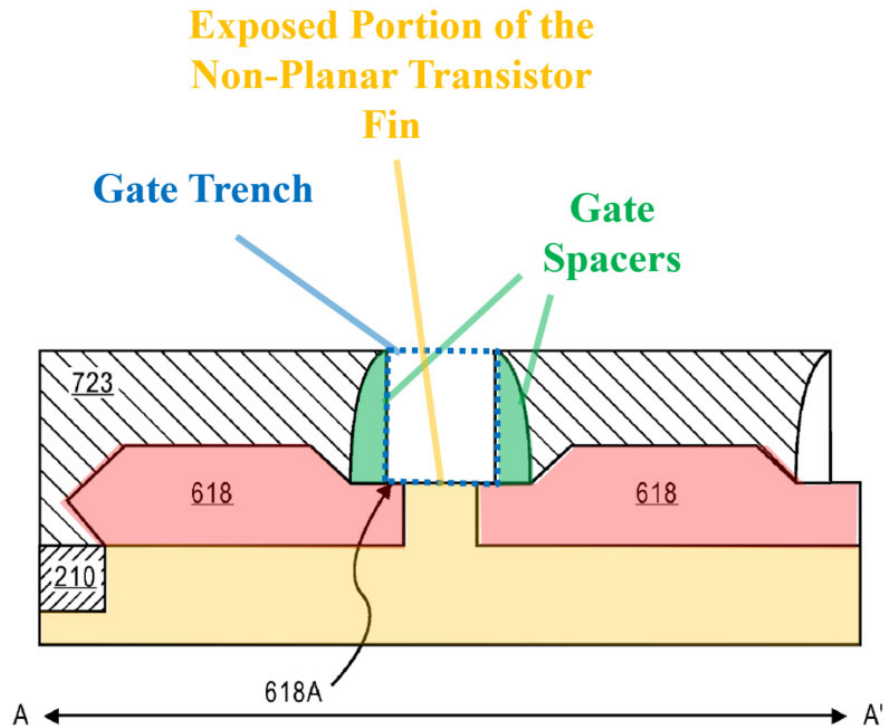


**FIG. 8**

(*Id.*, FIG. 8 (annotated).)

- g) “forming a gate dielectric adjacent the non-planar transistor fin within the gate trench;”
- h) “depositing conductive gate material within the gate trench;”

78. In my opinion, the Cappellani-Siddiqui combination discloses or suggests these features. For example, as shown in annotated figure 9 below, Cappellani discloses forming a gate dielectric layer 924 in the gate trench on the channel region 205 of the fin (“adjacent the non-planar transistor fin within the gate trench”) and then depositing a metal gate electrode layer 926 (“conductive gate material”) within the gate trench overlying the gate dielectric layer 924. (Ex. 1005,

¶[0048] (“Returning to FIG. 1, if the gate dielectric layer is removed, a new gate dielectric layer may be deposited into the trench opening over the channel region 205 at operation 120. ... Replacement of the gate dielectric layer may be used to address any damage that may have occurred to the original gate dielectric layer during application of the dry and wet etch processes. A metal gate electrode layer may then be deposited over the gate dielectric layer. Conventional metal deposition processes may be used to form the metal gate electrode layer, such as CVD, ALD, PVD, electroless plating, or electro plating. FIG. 9 illustrates a high-k gate dielectric layer 924 and a gate electrode layer 926 that have been deposited into the trench opening ....”), ¶[0049] (“The gate electrode layer 926 may consist of a P-type workfunction metal or an N-type workfunction metal, depending on whether the transistor is to be a PMOS or an NMOS transistor.”).)

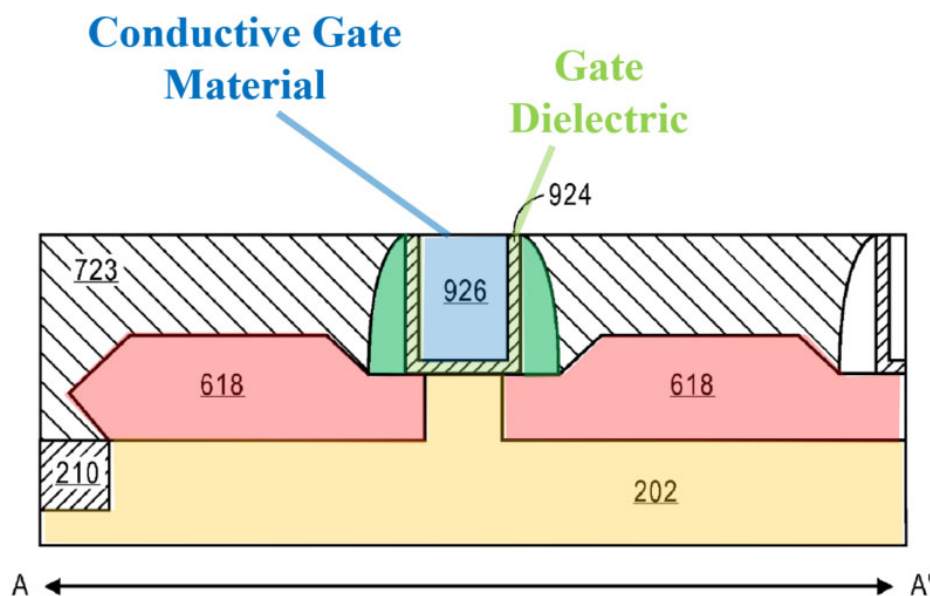


**FIG. 9**

(*Id.*, FIG. 9 (annotated).)

- i) **“removing a portion of the conductive gate material to form a recess between the non-planar transistor gate spacers;”**
- j) **“forming a capping dielectric structure within the recess by high density plasma depositing a dielectric material;”**

79. In my opinion, the Cappellani-Siddiqui combination discloses or suggests these features. As I discuss above for claim elements 1[a]-1[h], the Cappellani-Siddiqui combination discloses or suggests the formation of a non-planar transistor that includes a replacement gate structure. (*See* my discussion above in sections IX.A.1[a]-[h].) Cappellani does not explicitly disclose the additional steps that are taken after formation of the non-planar transistor in order to provide the

needed connections (e.g., electrical connections to the source and drain regions) for such a transistor. While Cappellani specifically contemplates that such connections are required, Cappellani does not provide explicit disclosure of providing a source/drain contact to the non-planar transistor. (Ex. 1005, ¶[0046] (“**As will be appreciated by those of skill in the art, the multi-gate MOS transistor may undergo further processing**, such as replacement gate oxide processes, replacement metal gate processes, annealing, or salicidation processes, **that may further modify the transistor and/or provide the necessary electrical interconnections.**”)) (emphasis added).)

80. Siddiqui, however, discloses additional steps that enable the interconnection of a transistor to surrounding circuitry using a self-aligned source/drain contact, and a person of ordinary skill in the art would have had good reason, based on Siddiqui’s teachings, to implement such a self-aligned source/drain contact in conjunction with the Cappellani-Siddiqui transistor that I discuss above with respect to claim features 1[a]-[h]. (Ex. 1006, ¶[0017] (“The present disclosure relates to structures and methods for forming semiconductor devices including gate structures having work function metal layers present therein, in which the contacts to the source and drain regions are formed using a self aligning process.”).) As I discuss above for claim element 1[c], Siddiqui, like Cappellani, is related to transistors that utilize sacrificial gate structures, and a person of ordinary skill in the

art implementing a transistor like that disclosed by Cappellani would have had reason to look to Siddiqui. (*See* my discussion above in section IX.A.1(c).)

81. As I also discuss above for claim element 1[c], Siddiqui discloses forming dielectric spacers 18 on the sidewalls of the sacrificial gate structure, and Siddiqui further discloses that by forming the dielectric spacers 18 using silicon nitride, the spacers 18 can be used together with a silicon nitride protective capping layer over the replacement gate to provide the ability to control etching of the opening in which the self-aligned source/drain contacts are formed. (*See* my discussion above in section IX.A.1(c); Ex. 1006, ¶¶[0032]-[0034].)

82. Specifically, as shown in annotated figure 3 below, Siddiqui discloses that after removing a sacrificial gate layer, a gate dielectric layer 30 is formed “at least on the channel region of the substrate 5.” (Ex. 1006, ¶[0043]; *see also id.*, ¶[0040].) A work function metal layer 35 is formed on the gate dielectric layer (*id.*, ¶[0043]), and metal fill material 40 is formed on the work function metal layer 35 (*id.*, ¶[0056]). As disclosed by Siddiqui, “[t]he metal fill material 40, work function metal layer 35 and the gate dielectric layer 30 provide a functional gate structure” (*id.*, ¶[0057]), where, as shown in annotated figure 3 below, the metal fill material 40 and work function metal layer 35 are conductive gate material. Therefore, like Cappellani, Siddiqui discloses reforming a gate structure that includes a gate dielectric and conductive gate material.

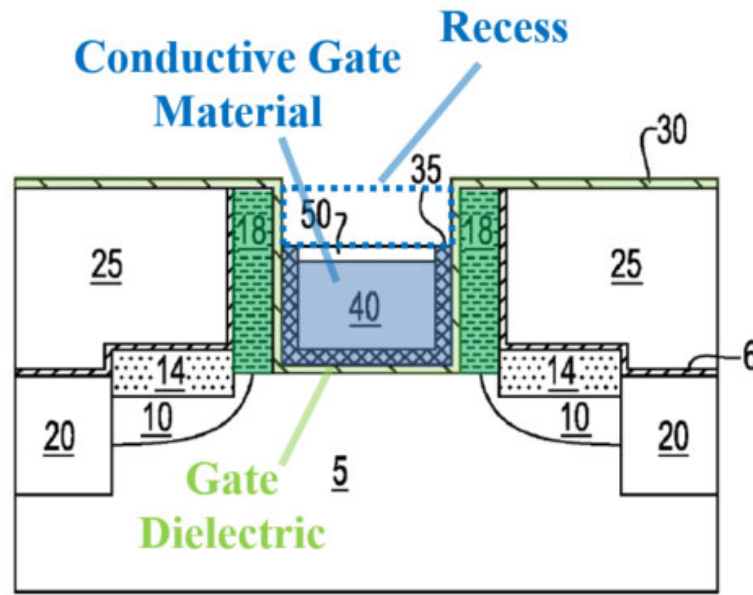


FIG. 3

(*Id.*, FIG. 6A (annotated).)

83. Siddiqui further discloses that the conductive gate material shown in annotated figure 3 above has been recessed using, for example, an anisotropic reactive ion etch (RIE) or an isotropic wet etch:

Still referring to FIG. 3, the metal fill material 40 may be recessed below the upper surface of the mandrel dielectric layer 25 and the protective dielectric layer 18. In one embodiment, the **metal fill material 40 may be recessed using an etch process** that is selective to the work function metal layer 35. The etch process may be an anisotropic etch, such [as a] reactive ion etch (RIE), or the etch process may be an isotropic etch, such as a wet etch

(*Id.*, ¶[0058] (emphasis added); *see also id.*, ¶¶[0059]-[0061].)

84. Following recessing of the metal fill material and selective removal of the portions of the work function metal layer 35, a dielectric protective cap structure, which is shown in annotated figure 4 below, is formed over the functional gate structure, where the cap structure protects the gate during the etching for the self-aligned contact:

FIG. 4 depicts forming a protective cap structure 60 over the functional gate structure. In one embodiment, the protective cap structure 60 is composed of a dielectric material, and fills the upper portion of the opening that is present over the recessed surface of the metal fill 40. The protective cap structure 60 may be composed of any dielectric material that can protect the functional gate from being damaged during the etch process that provides the opening to the source regions 10 and the drain regions 15. The protective cap structure 60 is typically composed of at least one of an oxide, nitride or oxynitride material. In one embodiment, in which the protective dielectric layer 18 is composed of a nitride, such as silicon nitride, and the mandrel dielectric layer 25 is composed of boron phosphorus silicate glass (BPSP), the protective cap structure 60 is composed of a nitride, such as silicon nitride.

(*Id.*, ¶[0062].)

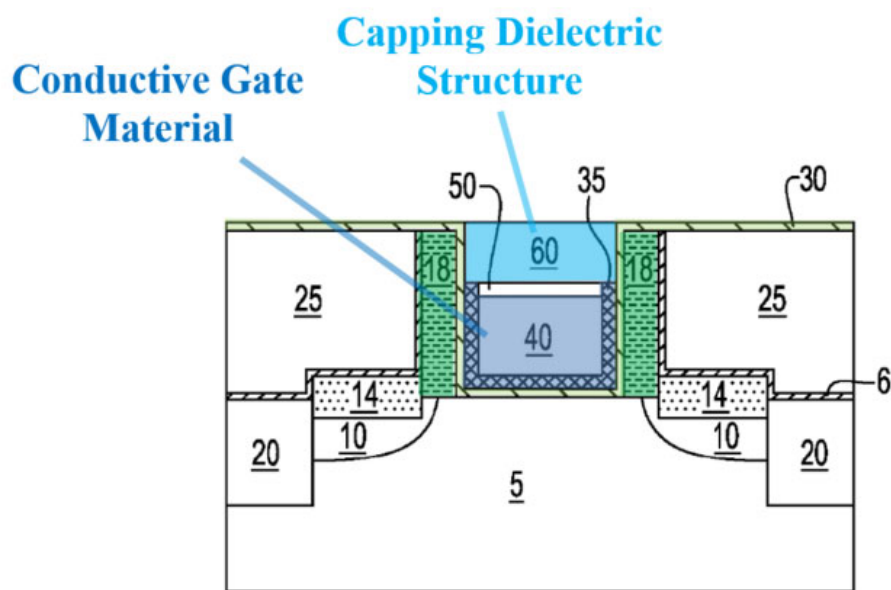
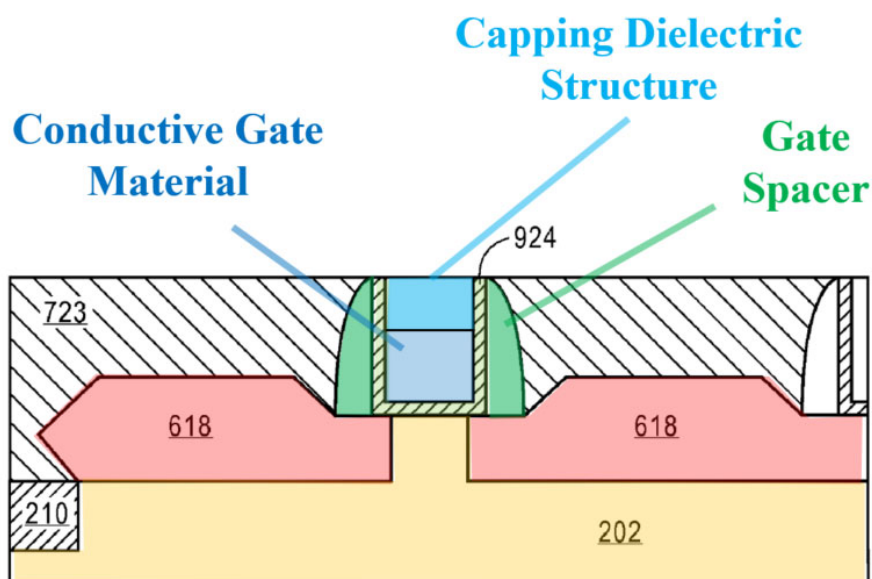


FIG. 4

(*Id.*, FIG. 4 (annotated).)

85. Therefore, Siddiqui discloses that, in order to form a self-aligned source/drain contact, a capping dielectric structure like that shown in figure 4 above is used as an etch stop and protects the gate structure during subsequent etching to form the openings for the contacts. In view of Siddiqui's disclosure, a person of ordinary skill in the art would have had good reason to recess the conductive material of the gate in a transistor like that disclosed by Cappellani to form a recess between the transistor gate spacers, where a capping dielectric structure is then formed in the recess. As disclosed by Siddiqui, these steps are part of the process for forming self-aligned source/drain contacts. (Ex. 1006, ¶[0070] ("The contacts 90 are self-aligned to the diffusion regions, i.e., source regions 10 and drain regions 15, because the

functional gate is protected from being damaged by the etch process that forms the vias 75 for the contacts 90 by the protective cap structure 60 that is present over the functional gate, and the protective dielectric layer 18 that is present on the sidewall of the functional gate.”.) The non-limiting demonstrative below, which is based on figure 9 of Cappellani, shows the transistor structure of the Cappellani-Siddiqui combination where the conductive gate material has been recessed and a capping dielectric structure has been formed in the recess.



86. As I noted above, Cappellani expressly contemplates the need for electrical connections to the transistor, but does not disclose the steps to form source/drain contacts. Siddiqui, however, provides such disclosure and a person of ordinary skill in the art would have had good reason to use Siddiqui’s self-aligned contact-formation method in conjunction with a transistor as disclosed by

Cappellani. Formation of the source/drain contacts in a transistor as disclosed by Cappellani using the methodology disclosed by Siddiqui would have been nothing more than the application of a known technique (Siddiqui's self-aligned contact formation) to a known device (Cappellani's transistor) ready for improvement (adding electrical connections acknowledged as necessary by Cappellani) to yield predictable results (a transistor having connectivity to other circuit elements).

87. A person of ordinary skill in the art would have been motivated to use Siddiqui's self-aligned contact formation technique both because Cappellani does not provide any description as to how to form contacts and because the self-aligned contact formation technique of Siddiqui provides advantages applicable to FinFET devices like that discussed above for the Cappellani-Siddiqui combination. As a person of ordinary skill in the art would have known, self-aligned contacts, which are sometimes referred to as "borderless contacts," are useful in devices having small critical dimensions (e.g. gate length) such as FinFETs. (Ex. 1007, ¶¶[0008]-[0009].) Such contacts, which are self-aligned to the gate electrode, allow the contact to be formed closer to the gate structure than non-self-aligned contacts while reducing the risk of shorting the electrodes, thereby reducing the area needed to form the transistor and associated interconnect. (See my discussion above in section V.C.) A person of ordinary skill in the art would also have known that such self-aligned contacts allow for increased tolerance with respect to possible lithographic

misalignment in the formation of the different structures of the transistor. (*Id.*) Therefore, a person of ordinary skill in the art would have been motivated to form self-aligned contacts to provide the needed connections to the transistor of the Cappellani-Siddiqui combination. As I discuss above for claim elements 1[c]-[d], a person of ordinary skill in the art would have understood that techniques applicable to planar MOSFETs, like that disclosed by Siddiqui, are also applicable to non-planar FETs, like Cappellani's FinFET. As such, a person of ordinary skill in the art implementing contacts in a FinFET like Cappellani's would have had good reason to look to Siddiqui's disclosure regarding contact formation. (Ex. 1009, Abstract, 2324; Ex. 1001, 3:47-51.)

88. Siddiqui further discloses that protective cap structure 60 may be a dielectric material formed using high-density chemical vapor deposition (HDCVD). (Ex. 1006, ¶[0062] (“In one embodiment, the protective cap structure 60 is composed of a dielectric material, and fills the upper portion of the opening that is present over the recessed surface of the metal fill 40.”), ¶[0063] (“The protective cap structure 60 may be formed by a deposition process including...chemical vapor deposition (CVD),” including “high-density chemical vapor deposition (HDCVD)”)). A person of ordinary skill in the art would have understood that HDCVD is “high density plasma deposition” as recited in claim element 1[j]. (Ex.

1011<sup>3</sup>, 5:56-57 (“high-density plasma chemical vapor deposition (HDCVD) process”); Ex. 1012, 3:62-63 (“a high-density plasma chemical deposition (HDCVD).”); Ex. 1013, 10:9-10 (“high density plasma CVD (HDCVD) method”); Ex. 1014, ¶[0039] (“High-Density Plasma CVD (HDCVD)”).)

89. Therefore, the Cappellani-Siddiqui combination discloses or suggests claim elements 1[i] and 1[j], as these steps are included in the self-aligned contact formation process disclosed by Siddiqui that a person of ordinary skill in the art would have had good reason to use in conjunction with a transistor as disclosed or suggested by the Cappellani-Siddiqui combination discussed above for claim elements 1[a]-1[h].

**k) “forming at least one dielectric material over the source/drain region, the non-planar transistor gate spacers, and the capping dielectric structure; and”**

90. In my opinion, the Cappellani-Siddiqui combination discloses or suggests this feature. As I discuss above for claim elements 1[i]-1[j], the Cappellani-Siddiqui combination discloses or suggests the formation self-aligned contacts for the transistor as disclosed by Cappellani. (See my discussion above in sections IX.A.1[i]-[j].) Siddiqui discloses that, before etching to form via 75 as a part of the

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<sup>3</sup> I cite to Chen, Su, Kikuchi, and Joo to demonstrate the knowledge of a person of ordinary skill in the art at the time of the alleged invention.

contact formation process, an interlayer dielectric layer 85 is blanket deposited over the protective cap structure, gate spacers, and source/drain regions. (Ex. 1006, ¶[0065] (“In some embodiments, prior to etching to form the via 75, an interlevel dielectric layer 85 is blanket deposited atop the structure depicted in FIG. 5.”); *see also id.*, ¶¶[0066]-[0067].)

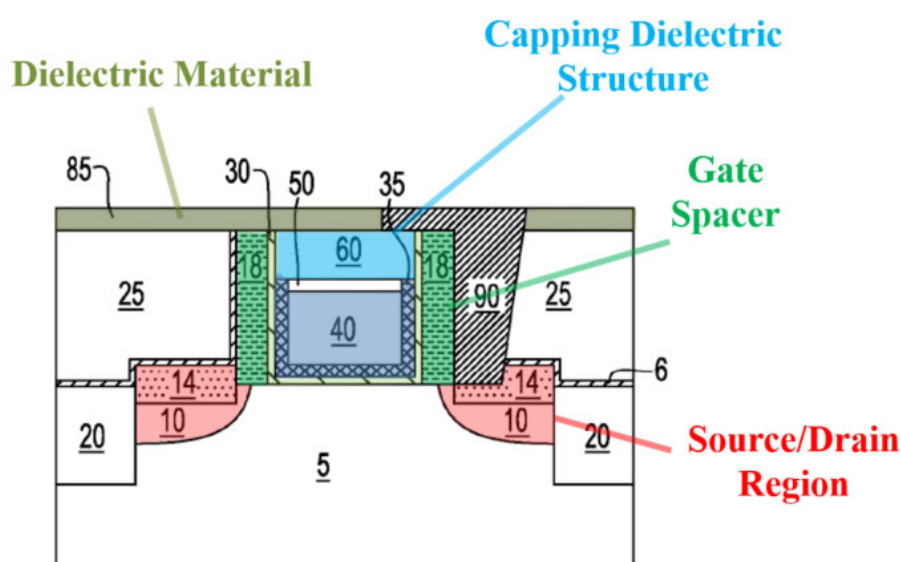


FIG. 6

(*Id.*, FIG. 6 (annotated).)

91. A person of ordinary skill in the art would have understood that the interlevel dielectric layer is used to separate different connective layers within the integrated circuit structure and isolate different contact structures (e.g., source/drain contacts) that are on the same layer. As such, a person of ordinary skill in the art would have had good reason to form such a dielectric layer as a part of the contact

formation process as disclosed or suggested by Siddiqui. The non-limiting demonstrative below shows the transistor of the Cappellani-Siddiqui combination discussed above for claim elements 1[i]-[j] with the addition of such an interlevel dielectric layer in a manner consistent with Siddiqui's disclosure. Therefore, the Cappellani-Siddiqui combination discloses or suggests "forming at least one dielectric material over the source/drain region, the non-planar transistor gate spacers, and the capping dielectric structure" as recited in claim element 1[k].

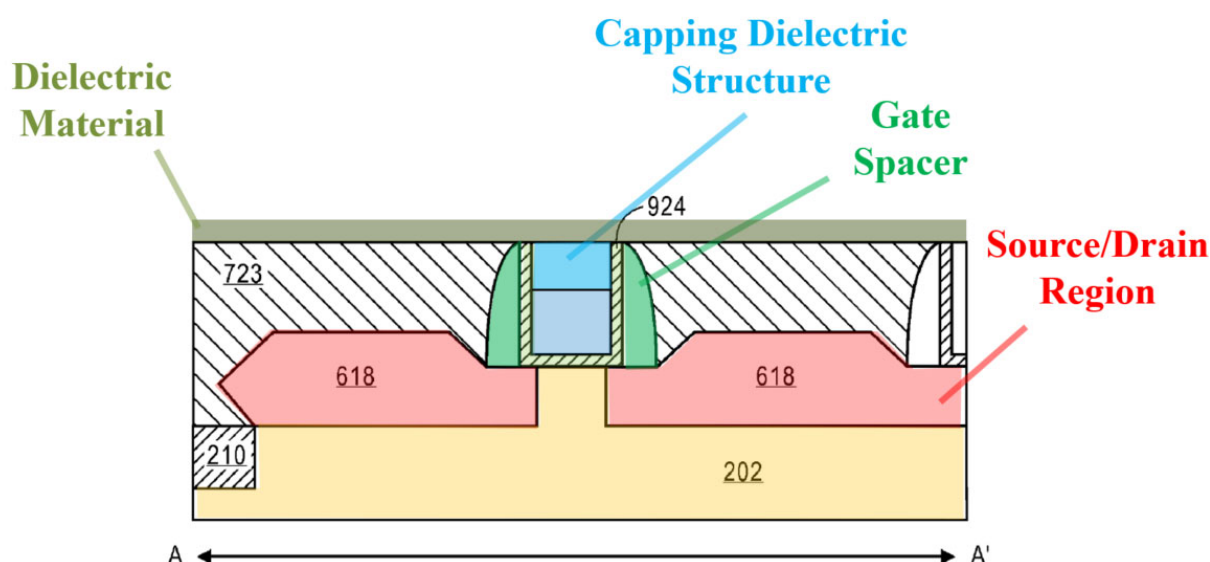


**FIG. 9**

- l) "forming a contact opening through the at least one dielectric material to expose at least a portion of the source/drain region."**

92. In my opinion, the Cappellani-Siddiqui combination discloses or suggests this feature. As discussed above for claim elements 1[i]-1[j], the Cappellani-Siddiqui combination discloses or suggests the formation self-aligned

contacts as disclosed by Siddiqui. (*See* my discussion above in sections IX.A.1[i]-[j].) As a part of the contact formation process, Siddiqui discloses etching to form via 75 (“contact opening”) through the interlevel dielectric layer 85 (“the at least one dielectric material”) and the mandrel dielectric layer 25 to expose the underlying source/drain region as a part of the contact formation process:

The interlevel dielectric layer 85 and the mandrel dielectric layer 25 are then patterned and etched to form vias 75 to the source regions 10 and the drain regions 15 using patterning and selective etch process. More specifically, a pattern is produced by applying a photoresist to the surface to be etched, exposing the photoresist to a pattern of radiation, and then developing the pattern into the photoresist using a resist developer. Once the patterning of the photoresist is completed, the sections covered by the photoresist are protected while the exposed regions are removed using a selective etching process that removes the unprotected regions to provide the vias 75.

(Ex. 1006, ¶[0068].)

93. Annotated figure 6 of Siddiqui below shows the via 75 after conductive metal has been deposited in the contact opening to form the contact 90. (*Id.*, ¶[0070].)

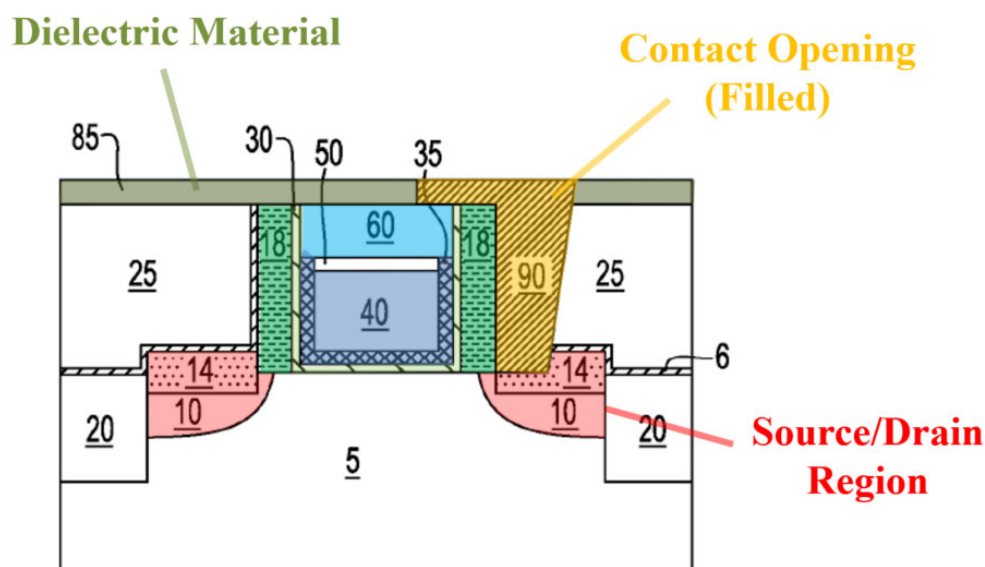
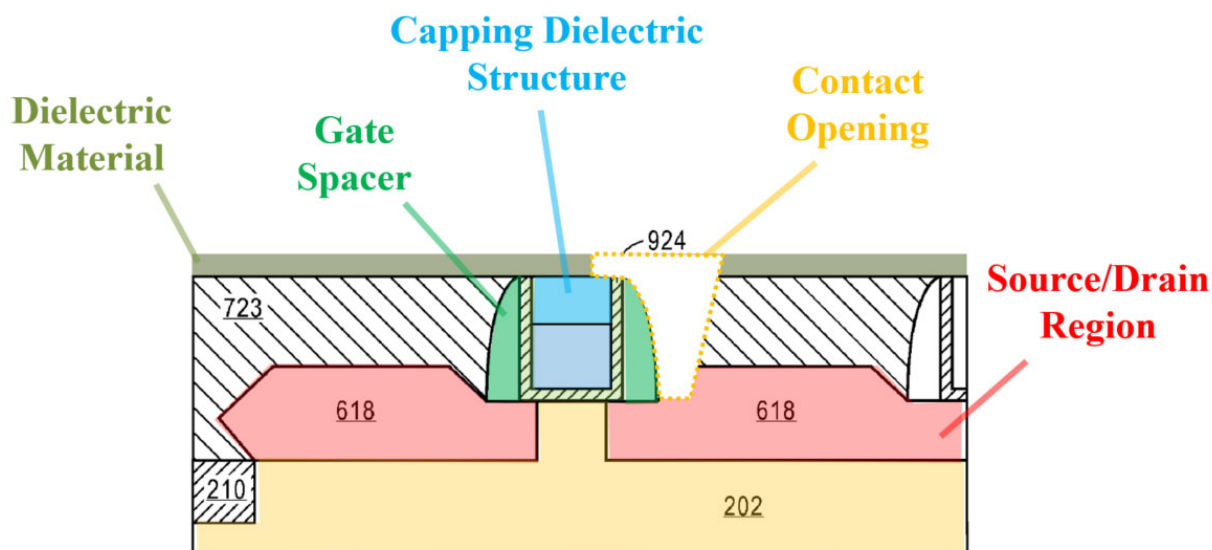


FIG. 6

(*Id.*, FIG. 6 (annotated).)

94. The non-limiting demonstrative below shows the “contact opening” formed “through the at least one dielectric material to expose at least a portion of the source/drain region” according to the Cappellani-Siddiqui combination.



95. Consistent with the disclosure of Siddiqui, a person of ordinary skill in the art would have understood that such an opening allows for the subsequent deposition of conductive material to provide electrical contact to the source/drain region. (Ex. 1006, ¶[0070] (“Following via formation, contacts 90 are formed by depositing a conductive metal into the vias using deposition processing, such as CVD or plating.”).) Therefore, the Cappellani-Siddiqui combination discloses or suggests claim element 1[i].

## 2. Claim 2

**“The method of claim 1, wherein high density plasma depositing the capping dielectric structure comprises high density plasma depositing a silicon nitride capping dielectric structure.”**

96. In my opinion, Cappellani-Siddiqui combination discloses or suggests this feature. As I discuss above for claim element 1[j], the Cappellani-Siddiqui combination discloses or suggests forming protective cap structure (“capping dielectric structure”) over the conductive material of the gate structure using high density plasma depositing as disclosed by Siddiqui. (See my discussion above in section IX.A.1(j).) Siddiqui further discloses that, in order to provide the desired protection for the gate structure during the subsequent selective etch used to form the via 75, the dielectric material can be silicon nitride. (Ex. 1006, ¶[0062] (“The protective cap structure 60 is typically composed of at least one of an oxide, nitride or oxynitride material. In one embodiment, in which the protective dielectric layer

18 is composed of a nitride, such as silicon nitride, and the mandrel dielectric layer 25 is composed of boron phosphorus silicate glass (BPSP), the protective cap structure 60 is composed of a nitride, such as **silicon nitride.**") (emphasis added).) Therefore the Cappellani-Siddiqui combination discloses or suggests claim 2.)

### 3. Claim 5

**"The method of claim 1, wherein forming a capping dielectric structure comprises: high density plasma depositing capping dielectric material within the recess; and removing excess capping dielectric material."**

97. In my opinion, the Cappellani-Siddiqui combination discloses or suggests this feature. As discussed above for claim element 1[j], the Cappellani-Siddiqui combination discloses or suggests forming protective cap structure ("capping dielectric structure") over the conductive material of the gate structure using high density plasma depositing as disclosed by Siddiqui. (See my discussion above in section IX.A.1(j).) Siddiqui further discloses that, after deposition of the capping dielectric material in the recess, chemical mechanical planarization (CMP) is used to planarize the cap structure, which removes excess capping dielectric material:

Following deposition, the dielectric material that provides the protective cap structure 60 may be planarized stopping on the gate dielectric layer 30 that is present on an upper surface of the mandrel dielectric layer 25. In one

example, the planarization process is provided by chemical mechanical planarization (CMP). In some embodiments, the planarization process may be continued until the gate dielectric layer 30 is removed from the upper surface of the mandrel dielectric layer 25, as depicted in FIG. 5.

(Ex. 1006, ¶[0064].)

98. A person of ordinary skill in the art would have understood that such planarization steps that remove excess material are commonplace in the fabrication of integrated circuits, and, consistent with the disclosure of Siddiqui, would have been motivated to include such a step in the self-aligned contact formation process as such planarization promotes formation of subsequent overlying layers.

#### 4. Claim 6

**“The method of claim 1, wherein forming a contact opening through the dielectric material to expose at least a portion of the source/drain region further comprises forming a contact opening through the dielectric material which exposes at least a portion of the source/drain region and at least a portion of one non-planar transistor gate spacer.”**

99. In my opinion, the Cappellani-Siddiqui combination discloses or suggests this feature. As I discuss above for claim element 1[1], the Cappellani-Siddiqui combination discloses or suggests forming a contact opening to expose a portion of the source/drain region. (*See* my discussion above in section IX.A.1(l).) Siddiqui further discloses that the etching operation used to form that opening is a

selective etch that etches the protective cap structure 60 and protective dielectric layer 18 (e.g., gate spacers) at a slower rate than the dielectric material of the interlevel dielectric layer 85 and the mandrel dielectric layer 25:

The interlevel dielectric layer 85 and the mandrel dielectric layer 25 are then patterned and etched to form vias 75 to the source regions 10 and the drain regions 15 using patterning and selective etch process. More specifically, a pattern is produced by applying a photoresist to the surface to be etched, exposing the photoresist to a pattern of radiation, and then developing the pattern into the photoresist using a resist developer. Once the patterning of the photoresist is completed, the sections covered by the photoresist are protected while the exposed regions are removed using a selective etching process that removes the unprotected regions to provide the vias 75.

(Ex. 1006, ¶[0068].)

In one embodiment, the etch chemistry that provides the vias 75 removes at least the material of the mandrel dielectric layer 25 selective to the protective cap structure 60 and the protective dielectric layer 18, wherein the protective cap structure 60 and the protective dielectric layer 18 protect the functional gate structure from being damaged by the via 75 etch.

(Ex. 1006, ¶[0069]; *see also id.*, ¶[0070] (“the functional gate is protected from being damaged by the etch process that forms the vias 75 for the contacts 90 by the protective cap structure 60 that is present over the functional gate, and the **protective dielectric layer 18** that is present on the sidewall of the functional gate.”).)

100. Therefore, Siddiqui discloses that the selective etch removes portions the interlevel dielectric layer 85 and the mandrel dielectric layer 25, while the protective cap structure 60 and the protective dielectric layer 18 act as an etch stop and protect the functional gate structure from the etch by preventing the etchants from reaching the gate structure. In other words, the etching operation stops or slows the rate of removal of material when it reaches (and hence exposes) the protective cap structure 60 and the protective dielectric layer 18. (*See* my discussion above in section V.C.) Therefore, as shown in annotated figure 6 of Siddiqui and the non-limiting demonstrative below corresponding to the Cappellani-Siddiqui combination, the etch (“forming a contact opening through the dielectric material which exposes at least a portion of the source/drain region”) also exposes a portion of a gate spacer (“at least a portion of one non-planar transistor gate spacer”).

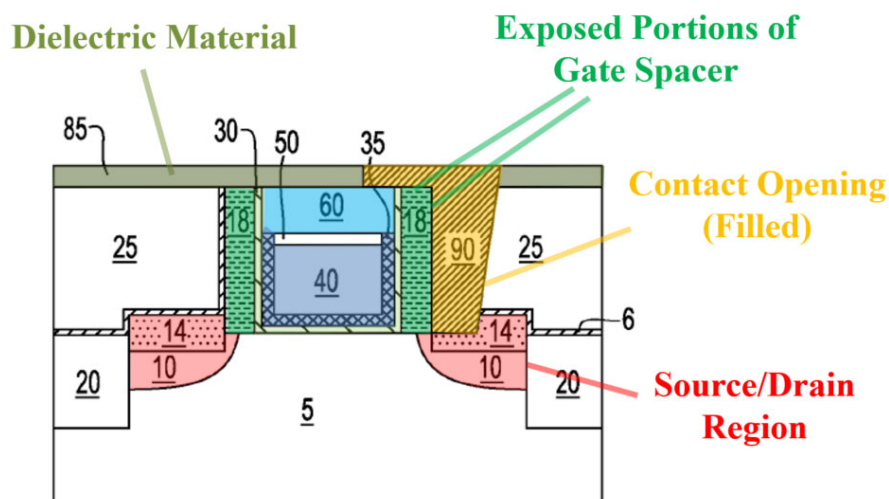
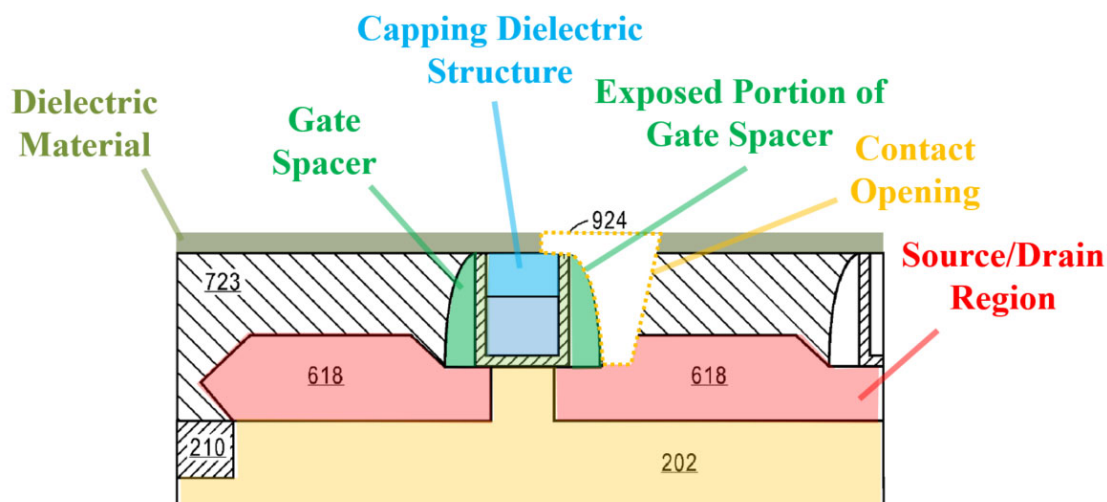


FIG. 6

(Ex. 1006, FIG. 6 (annotated).)



## 5. Claim 7

**“The method of claim 6, further comprising forming a source/drain contact to abut the exposed portion of the source/drain region and exposed portion of the non-planar transistor gate spacer.”**

101. In my opinion, the Cappellani-Siddiqui combination discloses or suggests this feature. As I discuss above for claim element 1[1] and claim 6, the Cappellani-Siddiqui combination discloses or suggests forming a contact opening to expose a portion of the source/drain region and a portion of the gate spacer. (*See my discussion above in sections IX.A.1(l), IX.A.4.*) Siddiqui further discloses that the via 75 corresponding to the contact opening is filled with conductive metal to form the contact 90 for the transistor. (Ex. 1006, ¶[0070] (“Following via formation, contacts 90 are formed by depositing a conductive metal into the vias using deposition processing, such as CVD or plating.”).) Consistent with the teachings of Siddiqui, the self-aligned contact formation of the Cappellani-Siddiqui combination fills the contact hole with conductive material to form a source/drain contact, where, because it fills the contact hole, the contact abuts the exposed portions of the source/drain region and the gate spacer.

102. While Siddiqui discloses that “metal semiconductor alloy regions 14 may be formed atop the source regions 10 and the drain regions 15,” a person of ordinary skill in the art would have understood that such alloy regions are meant to provide improved contact to the source/drain regions and are optional based on Siddiqui’s disclosure. (Ex. 1006, ¶[0035].) Indeed, Siddiqui’s disclosure regarding formation of the via 75 indicates that the via exposes the source/drain region (Ex. 1006, ¶[0065] (“etching a via 75 ... to expose at least one of the source region 10

and the drain region 15”), thereby confirming that regions 14 are optional and/or can be included as a part of the source/drain region. Moreover, such a person of ordinary skill in the art would have understood that such alloy regions need not be included in the Cappellani-Siddiqui transistor.

103. Annotated figure 6 of Siddiqui and the non-limiting demonstrative for the Cappellani-Siddiqui combination below show the filled contact abutting the exposed portions of the source/drain region and gate spacer.

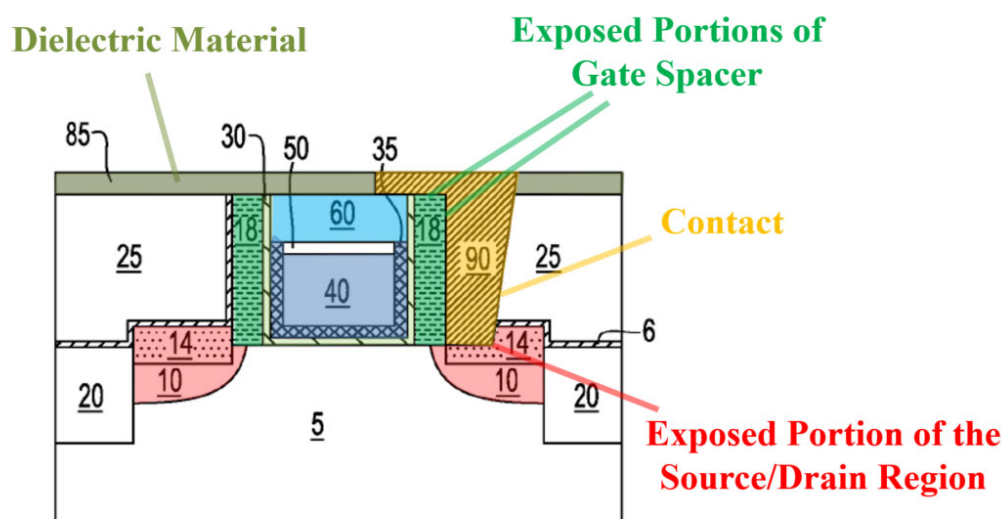
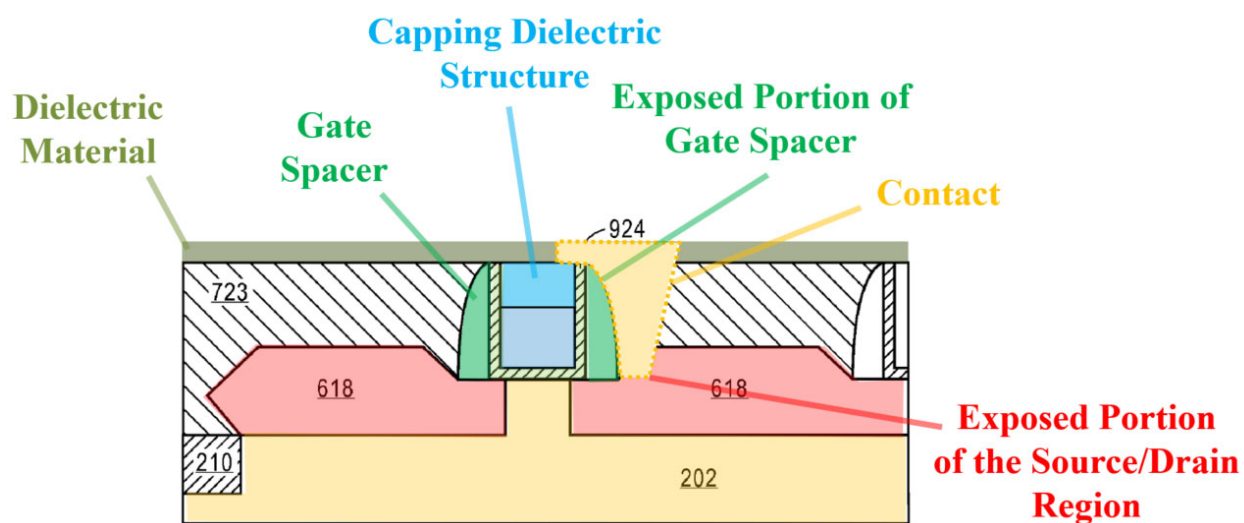


**FIG. 6**

(Ex. 1006, FIG. 6 (annotated).)



## 6. Claim 8

**“The method of claim 1, wherein forming a contact opening through the dielectric material to expose at least a portion of the source/drain region further comprises forming a contact opening through the dielectric material which exposes at least a portion of the source/drain region and at least a portion of the capping dielectric structure.”**

104. In my opinion, the Cappellani-Siddiqui combination discloses or suggests this feature. As I discuss above for claim element 1[l], the Cappellani-Siddiqui combination discloses or suggests forming a contact opening to expose a portion of the source/drain region. (See my discussion above in section IX.A.1(l).) Siddiqui further discloses that the etching operation used to form that opening is a selective etch that etches the protective cap structure 60 and protective dielectric layer 18 (e.g., gate spacers) at a slower rate than the dielectric material of the interlevel dielectric layer 85 and the mandrel dielectric layer 25:

The **interlevel dielectric layer 85 and the mandrel dielectric layer 25** are then patterned and etched to form **vias 75 to the source regions 10 and the drain regions 15 using patterning and selective etch process**. More specifically, a pattern is produced by applying a photoresist to the surface to be etched, exposing the photoresist to a pattern of radiation, and then developing the pattern into the photoresist using a resist developer. Once the patterning of the photoresist is completed, the sections covered by the photoresist are protected while the exposed regions are removed using a selective etching process that removes the unprotected regions to provide the vias 75.

(Ex. 1006, ¶[0068] (emphasis added).)

In one embodiment, the etch chemistry that provides the vias 75 removes at least the material of the mandrel dielectric layer 25 selective to the protective cap structure 60 and the protective dielectric layer 18, wherein the protective cap structure 60 and the protective dielectric layer 18 protect the functional gate structure from being damaged by the via 75 etch.

(*Id.*, ¶[0069]; *see also id.*, ¶[0070] (“the functional gate is protected from being damaged by the etch process that forms the vias 75 for the contacts 90 by the **protective cap structure 60** that is present over the functional gate, and the

protective dielectric layer 18 that is present on the sidewall of the functional gate.”)  
(emphasis added).)

105. Therefore, Siddiqui discloses that the selective etch removes portions the interlevel dielectric layer 85 and the mandrel dielectric layer 25, while the protective cap structure 60 and the protective dielectric layer 18 act as an etch stop and protect the functional gate structure from the etch by preventing the etchants from reaching the gate structure. In other words, the etching operation stops or slows the rate of removal of material when it reaches the protective cap structure 60 and the protective dielectric layer 18. (*See* my discussion in section V.C.) Therefore, as shown in annotated figure 6 of Siddiqui and the non-limiting demonstrative below corresponding to the Cappellani-Siddiqui combination, the etch (“forming a contact opening through the dielectric material which exposes at least a portion of the source/drain region”) also exposes a portion of the capping dielectric structure.

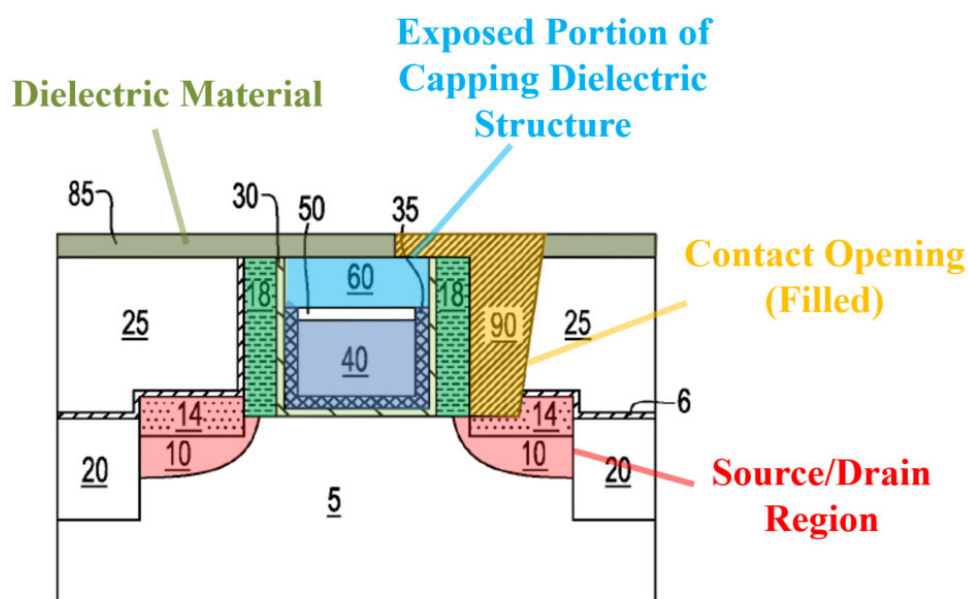
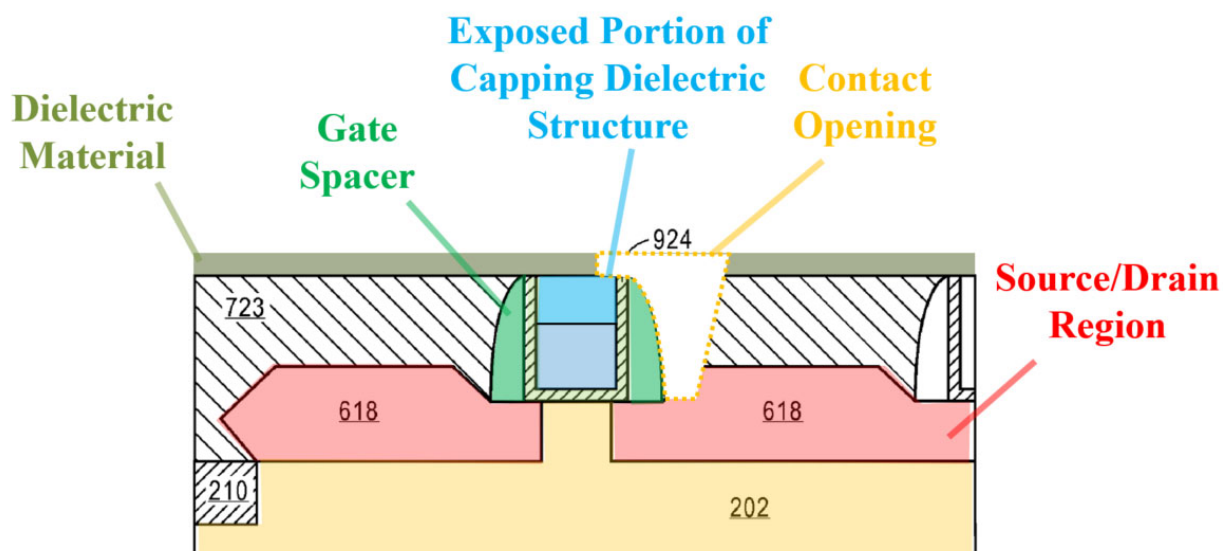


FIG. 6

(*Id.*, FIG. 6 (annotated).)



## 7. Claim 9

“The method of claim 8, further comprising forming a source/drain contact abuts the exposed portion of the source/drain region and the exposed portion of the capping dielectric structure.”

106. I have been asked to assume that claim 9 should read “forming a source/drain contact [abuts] to abut the exposed portion of the source/drain region and the exposed portion of the capping dielectric structure.” Under that assumption, it is my opinion that the Cappellani-Siddiqui combination discloses or suggests this feature. As I discuss above for claim element 1[1], the Cappellani-Siddiqui combination discloses or suggests forming a contact opening to expose a portion of the source/drain region. (See my discussion above in section IX.A.1(l).) Siddiqui further discloses that the via 75 corresponding to the contact opening is filled with conductive metal to form the contact 90 for the transistor. (Ex. 1006, ¶[0070] (“Following via formation, contacts 90 are formed by depositing a conductive metal into the vias using deposition processing, such as CVD or plating.”).) Consistent with the teachings of Siddiqui, the self-aligned contact formation of the Cappellani-Siddiqui combination fills the contact hole with conductive material to form a source/drain contact, where, because it fills the contact hole, the contact abuts the exposed portions of the source/drain region and the capping dielectric structure.

107. Annotated figure 6 of Siddiqui and the non-limiting demonstrative for the Cappellani-Siddiqui combination below show the filled contact abutting the exposed portions of the source/drain region and capping dielectric structure.



(Ex. 1006, FIG. 6 (annotated).)



**8. Claim 10**

**“The method of claim 1, wherein forming a contact opening through the dielectric material to expose at least a portion of the source/drain region further comprises forming a contact opening through the dielectric material exposes at least a portion of the source/drain region, at least a portion of the non-planar transistor gate spacer, and at least a portion of the capping dielectric structure.”**

108. In my opinion, the Cappellani-Siddiqui combination discloses or suggests this feature for the reasons I discuss above for claims 6 and 8. (*See my discussion above in sections IX.A.4, 6.*)

**9. Claim 11**

**“The method of claim 10, further comprising forming a source/drain contact to abut the exposed portion of the source/drain region, the exposed portion of non-planar gate spacer, and the exposed portion of the capping dielectric structure.”**

109. In my opinion, the Cappellani-Siddiqui combination discloses or suggests this feature for the reasons I discuss above for claims 7 and 9. (*See my discussion above in sections IX.A.5, 7.*)

**B. Cappellani in Combination with Siddiqui and Park Discloses or Suggests the Features of Claims 1, 2, and 4-11**

**1. Claims 1, 2, and 5-11**

**“A computing system comprising the integrated circuit of claim 1.”**

110. As I discuss above in section IX.A, the Cappellani-Siddiqui combination discloses or suggests the features of claims 1, 2, and 5-11, including claim element 1[j], which requires “forming a capping dielectric structure within the recess by high density plasma depositing a dielectric material.” (See my discussion above in Section IX.A.) I have been asked to assume a scenario where the Cappellani-Siddiqui combination does not disclose or suggest forming the capping dielectric by “high density plasma deposition.” Under such a scenario, it is my opinion that a person of ordinary skill in the art would had good reason to form the capping layer using high density plasma chemical vapor deposition (HDPCVD) in view of Park and their knowledge of the state of the art.

111. Park, like Cappellani and Siddiqui, is directed to forming transistors with improved performance, where, like Siddiqui, Park discloses a nitride capping layer overlying the transistor structure. (Ex. 1010, Abstract (“forming a first capping nitride layer covering the gate electrode and the source/drain regions, the first capping nitride layer including a Si—H rich SiN layer”), 1:14-17.) Park further discloses that the nitride capping layer can be formed using high density plasma

chemical vapor deposition (HDPCVD). (Ex. 1010, 6:32-37 (“The capping nitride layer 37 may be formed at a temperature of about 350° C. to about 500° C. using, e.g., low pressure chemical vapor deposition (LPCVD), plasma enhanced chemical vapor deposition (PECVD), high density plasma chemical vapor deposition (HDPCVD), or a combination thereof.”).)

112. In view of Park, a person of ordinary skill in the art would have had good reason to form the silicon nitride capping layer in a transistor of the Cappellani-Siddiqui combination discussed above in section IX.A using HDPCVD. Such a person of ordinary skill in the art would have understood that HDPCVD is one of a finite number of identified and predictable options for depositing silicon nitride capping layers (as disclosed by Park), and would have had good reason to try using HDPCVD to form the silicon nitride capping layer with a reasonable expectation of success. A person of ordinary skill in the art would have understood that doing so would have been nothing more than the application of a known technique (HDPCVD deposition of silicon nitride) to a known device ready for improvement (the transistor of the Cappellani-Siddiqui combination) to yield predictable results (a functional transistor with a silicon nitride capping layer).

113. A person of ordinary skill in the art would also have understood that using HDPCVD to form the silicon nitride cap provides certain advantages, including improved gap-fill capability, which such a skilled person would have

recognized is particularly relevant to formation of the capping dielectric structure in the recessed gate region in the Cappellani-Siddiqui combination. (Ex. 1015<sup>4</sup>, 1:65-2:2 (“HDP-CVD processes generally have superior gapfill capabilities as compared to these other types of CVD processes because HDP-CVD deposition process provide[s] for a sputtering component to the deposition process simultaneous with film growth.”); Ex. 1016, 1:65-2:6.) Therefore a person of ordinary skill in the art would have been motivated to use HDPCVD for forming the capping dielectric structure in order to avoid voids in the dielectric that could result in unwanted short circuits, or damage to the gate structure the dielectric is protecting. Based on their knowledge of the state of the art and Park’s disclosure, a person of ordinary skill in the art would have had a high likelihood of success in using HDPCVD to form the silicon nitride capping layer. Therefore, the Cappellani-Siddiqui-Park combination discloses or suggests claim element 1[j], whereas the remaining features of claims 1, 2, and 5-11 are disclosed or suggested for the reasons I discuss above in section IX.A. (*See my discussion above in sections IX.A.1-9.*)

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<sup>4</sup> I cite to Ahmad and Vassilev to demonstrate the knowledge of a person of ordinary skill in the art at the time of the alleged invention.

**2. Claim 4**

**“The method of claim 1, wherein high density plasma depositing the capping dielectric structure comprises high density plasma depositing the capping dielectric structure at a temperature between about 300° C. and 600° C.”**

114. In my opinion, the Cappellani-Siddiqui-Park combination discloses or suggests this feature. As I discuss above in section IX.B.1, the Cappellani-Siddiqui-Park combination discloses or suggests forming protective cap structure (“capping dielectric structure”) over the conductive material of the gate structure using high density plasma depositing. (*See* my discussion above in section IX.B.1.) Park further discloses that the nitride capping layer can be formed using high density plasma chemical vapor deposition (HDPCVD) at a temperature of 350-500° C., which is within the claimed range of 300-600° C. (Ex. 1010, 6:32-37 (“The capping nitride layer 37 may be formed at a temperature of about 350° C. to about 500° C. using, e.g., low pressure chemical vapor deposition (LPCVD), plasma enhanced chemical vapor deposition (PECVD), high density plasma chemical vapor deposition (HDPCVD), or a combination thereof.”).) Therefore, a person of ordinary skill in the art would have been motivated to perform the deposition at a temperature within the range disclosed by Park, and the Cappellani-Siddiqui-Park combination discloses or suggests claim 4.

**C. Brask in Combination with Cheng Discloses or Suggests the Features of Claims 1, 2, and 5-11**

115. In my opinion, Brask in combination with Cheng discloses or suggests the features of claims 1, 2, and 5-11 of the '699 patent.

**1. Claim 1**

**a) “A method comprising:”**

116. I understand that “[a] method, comprising” is the preamble to claim 1 of the '699 patent. I have been asked to assume that the preamble is a claim limitation. Under that assumption, in my opinion, Brask discloses a method. For example, Brask is entitled “Nonplanar Transistors with Metal Gate Electrodes” (Ex. 1008, Title) and discloses a method for forming p-type and n-type non-planar transistors with metal gate electrodes by “utilizing a replacement gate technique.” (Ex. 1008, ¶[0058] (“FIGS. 6A-6O illustrate a method of forming a p type nonplanar device with a metal gate electrode and a n type nonplanar device with a metal gate electrode utilizing a replacement gate technique”).) Such a method is further discussed below for claim elements 1[b]-1[l]. (See my discussion below in sections IX.C.1(b)-(l).)

**b) “forming a sacrificial non-planar transistor gate over a non-planar transistor fin;”**

117. In my opinion, Brask discloses this claim feature. As shown in annotated figure 6A below, Brask discloses forming a sacrificial gate dielectric layer

602 and a sacrificial gate electrode layer 604 (together “a sacrificial non-planar transistor gate”) over a semiconductor body 510 (“non-planar transistor fin”):

The replacement gate process begins with the formation of a semiconductor body or bodies 510 for the n type device and a semiconductor body or bodies 512 for the p type device as discussed above. After the patterning of a semiconductor film to form the semiconductor bodies 510 and 512 (and source/drain landing pads, if desired) a sacrificial gate dielectric layer 602 and a sacrificial gate electrode 604 are formed over the top surface and sidewalls of the silicon bodies 510 and 512 as shown in FIG. 6A.

(Ex. 1008, ¶[0059]; *see also id.*, ¶[0046] (“the semiconductor bodies or fins 510 and 512”).)

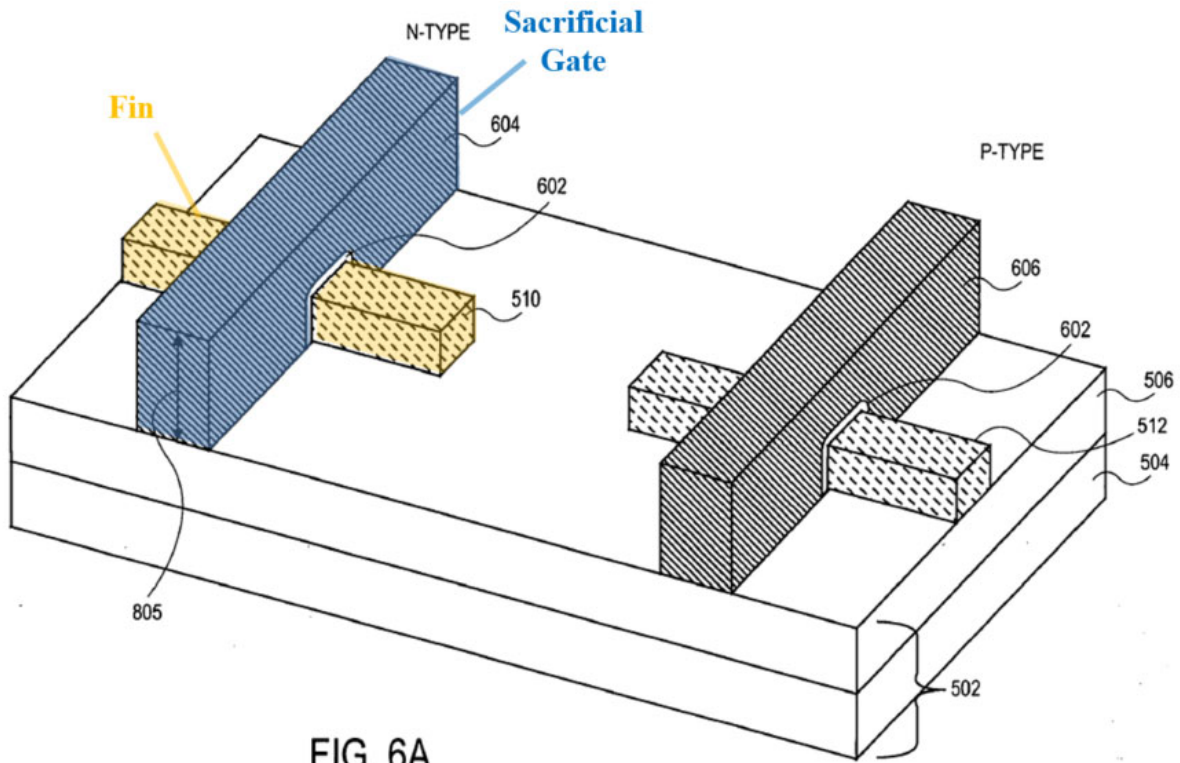


FIG. 6A

(*Id.*, FIG. 6A (annotated).)

- c) “depositing a dielectric material layer over the sacrificial non-planar transistor gate and the non-planar transistor fin;”
- d) “forming non-planar transistor gate spacers from a portion of the dielectric material layer adjacent the sacrificial non-planar transistor gate;”

118. In my opinion, Brask discloses these limitations. For example, as shown in annotated figure 6D below, Brask discloses forming dielectric sidewall spacers 612 (“non-planar transistor gate spacers”) adjacent to the sacrificial gate 604. (Ex. 1008, ¶[0065].)

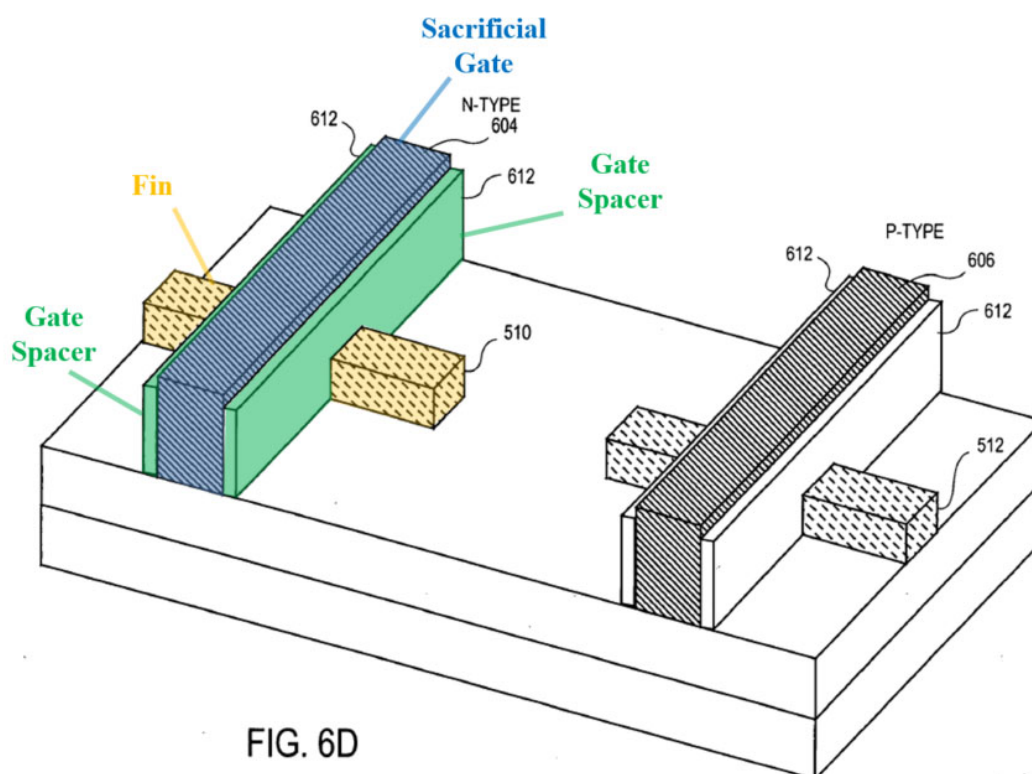


FIG. 6D

(*Id.*, FIG. 6D (annotated).)

119. Brask discloses that the gate spacers are formed by blanket depositing a dielectric layer (“depositing a dielectric material layer over the sacrificial non-planar transistor gate and the non-planar transistor fin”) and then etching to remove the dielectric material from the areas other than the sidewalls of the gate electrode (“forming non-planar transistor gate spacers from a portion of the dielectric material layer adjacent the sacrificial non-planar transistor gate”):

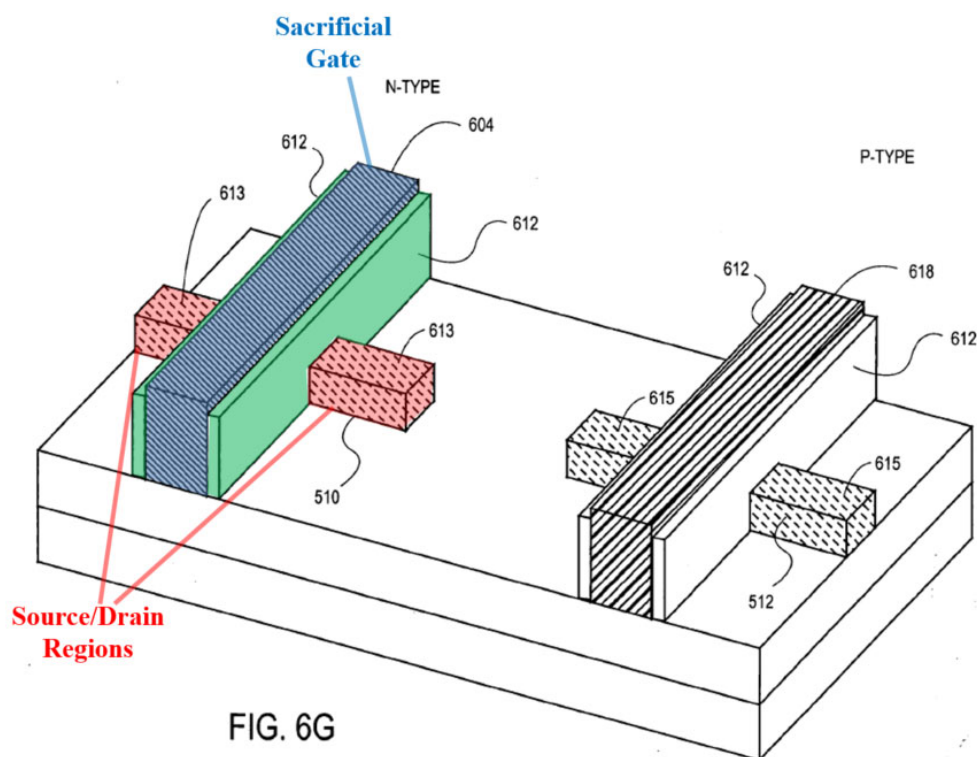
Next, if desired, dielectric sidewall spacers 612 can be formed along opposite sidewalls of the sacrificial gate electrodes 604 and 606 as shown in FIG. 6D. The sidewall spacers can be formed by any well known techniques, such

as by blanket depositing the conformal sidewall spacer dielectric over the substrate including the top surface and sidewalls of the sacrificial gate electrodes 604 and 606 as well as on the top surface and sidewalls of semiconductor bodies 510 and 512 as well as onto the exposed surface of the insulating substrate. The dielectric spacer material is deposited to a thickness which is approximately equal to the width desired for spacers 612. In an embodiment of the present invention, the dielectric spacer material is deposited to a thickness between 20-200 Å. The spacer material can be a dielectric, such as silicon nitride, silicon oxide, silicon oxynitride or combinations thereof. In an embodiment of the present invention, the spacer material is silicon nitride formed by hot wall low-pressure chemical vapor deposition (LPCVD) process. The dielectric spacer material is then anisotropically etched back to remove the dielectric spacer material from a horizontal surface (e.g., top surface) of the sacrificial gate electrodes 604 and 606 and the top surface of the semiconductor bodies 510 and 512 and insulating substrate 602, while leaving spacer material on the vertical surfaces (e.g., sidewalls) of sacrificial gate electrodes 604 and 606 to form sidewall spacers 612 as shown in FIG. 6D.

(*Id.*, ¶[0065].)

**e) “forming a source/drain region;”**

120. In my opinion, Brask discloses this feature. For example, Brask discloses that “additional silicon can be formed onto the exposed top surface and sidewalls of the semiconductor bodies 510 and 512 in order to form raised source and drain regions.” (Ex. 1008, ¶[0066].) Heavy source/drain contact regions are then formed in the semiconductor bodies 510 and 512 on opposite sides of the sacrificial gate (*id.*, ¶¶[0067]-[0068]), and then annealing is used to activate the dopants in the semiconductor bodies 510 and 512 to form the n-type source source/drain regions 613 and p-type source/drain regions 615 (*id.*, ¶[0069].) The resulting source/drain regions for the n-type transistor are shown in annotated figure 6G below.



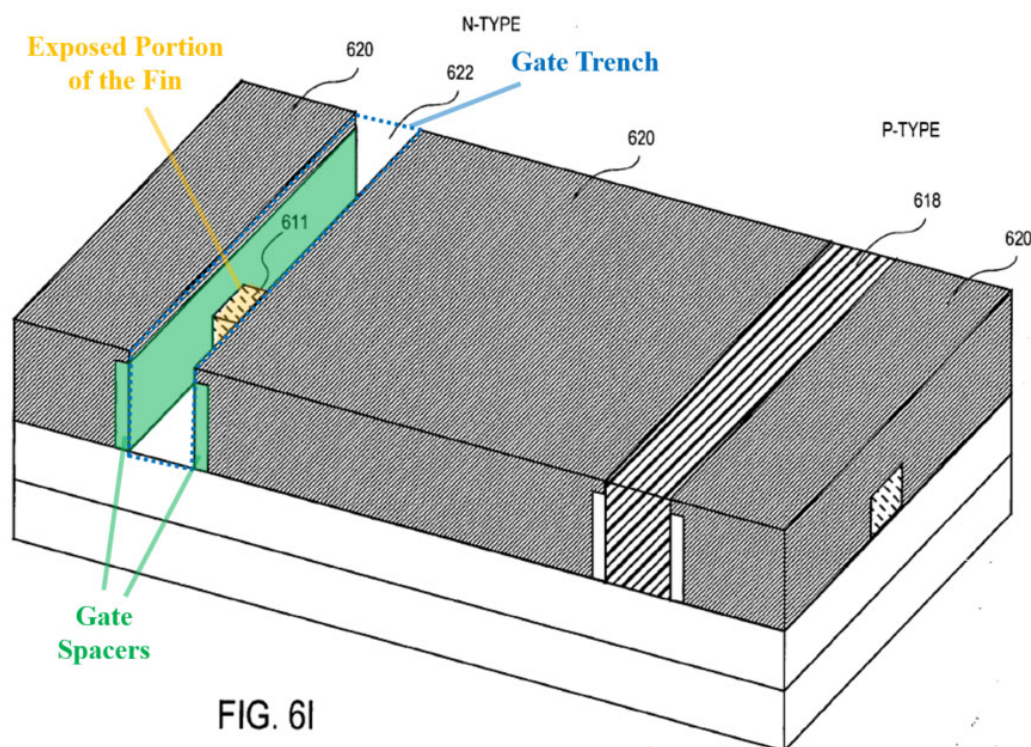
(*Id.*, FIG. 6G (annotated).)

- f) “removing the sacrificial non-planar transistor gate to form a gate trench between the non-planar transistor gate spacers and expose a portion of the non-planar transistor fin;”

121. In my opinion, Brask discloses these features. For example, as illustrated in annotated figure 6I below, Brask discloses removing the sacrificial gate structure, which includes the gate electrode 604 and gate dielectric layer 602 for the n-type transistor, to form opening 622 between the spacers (“gate trench between the non-planar transistor gate spacers”) that exposes the channel region 611 of the semiconductor body 510 (“a portion of the non-planar transistor fin”):

Next, as shown in FIG. 6I, the sacrificial gate electrode 604 is now removed without removing altered sacrificial gate electrode 618. After sacrificial gate electrode 604 is removed, the sacrificial gate dielectric layer 602 is also removed. Removal of the sacrificial gate electrode 604 forms an opening 622 where the gate electrode for the n type device will be formed. Removing the sacrificial gate electrode 604 and the sacrificial dielectric layer 602 exposes the channel region 611 of the semiconductor body 510 of the nonplanar n type device as shown in FIG. 6I.

(Ex. 1008, ¶[0072]; *see also id.*, ¶[0073].)



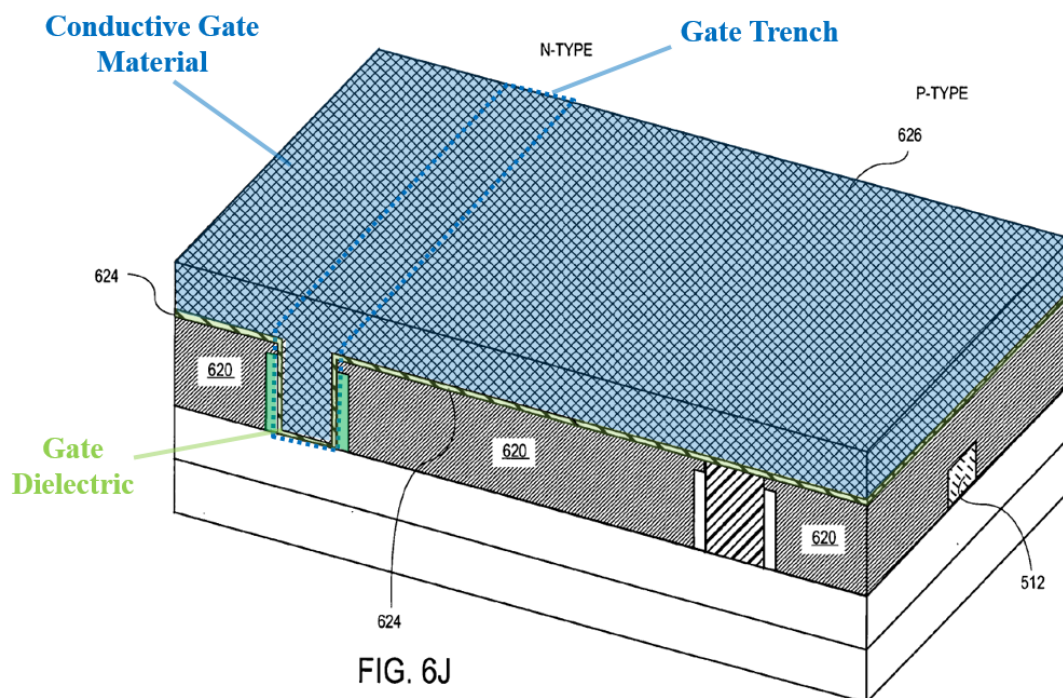
(*Id.*, FIG. 6I (annotated).)

- g) “forming a gate dielectric adjacent the non-planar transistor fin within the gate trench;”**
- h) “depositing conductive gate material within the gate trench;”**

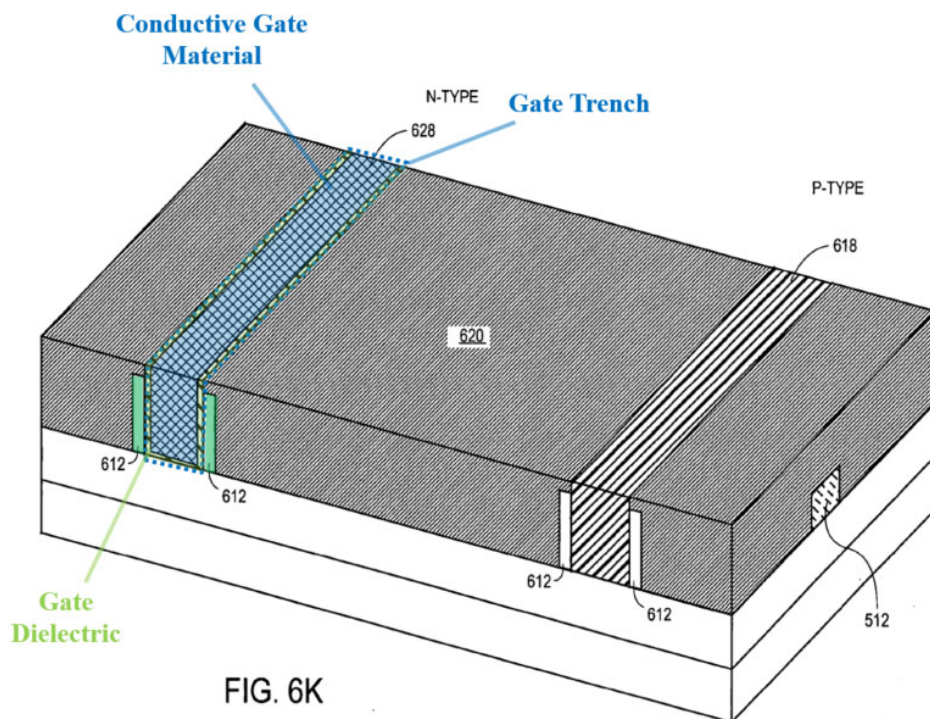
122. In my opinion, Brask discloses these features. For example, as illustrated in annotated figures 6J and 6K below, Brask discloses forming a replacement gate structure in the opening 622 (“gate trench”), where the replacement gate structure includes gate dielectric film 624 formed on the channel region 611 (“adjacent the non-planar transistor fin”) and gate electrode material 626 for the n-type transistor:

Next, the gate dielectric layer and the gate electrode material for the n type device are formed in the openings 622 as shown in FIG. 6J. First the gate dielectric film 624 is blanket deposited over the substrate. The gate dielectric material covers the top surface of the sidewalls of the channel region of semiconductor body 510 as described above. ... Next, a gate electrode material for the n type device is blanket deposited over the gate dielectric. ... Next, the gate electrode material 626 is planarized until the top surface of the dielectric layer 260 is revealed as shown in FIG. 6K. Once a gate electrode material and the gate dielectric material are polished back or removed from the top dielectric film 620, a gate electrode 628 is formed for the n type nonplanar device.

(Ex. 1008, ¶[0074].)



(*Id.*, FIG. 6J (annotated).)



(*Id.*, FIG. 6K (annotated).)

- i) **“removing a portion of the conductive gate material to form a recess between the non-planar transistor gate spacers;”**
- j) **“forming a capping dielectric structure within the recess by high density plasma depositing a dielectric material;”**

123. In my opinion, the Brask-Cheng combination discloses or suggests these features. As I discuss above for claim elements 1[a]-1[h], Brask discloses the formation of a non-planar transistor that includes a replacement gate structure. (*See* my discussion above in sections IX.C.1[a]-[h].) Brask does not explicitly disclose the additional steps that are taken after formation of the non-planar transistor in order to provide the needed connections (e.g., electrical connections to the source and drain regions) for such a transistor. While Brask specifically contemplates that such connections are required, Brask does not provide explicit disclosure of providing a source/drain contact to the non-planar transistor. (Ex. 1008, ¶[0079] (“At this point, fabrication on an n type device with a metal gate electrode and a p type device with a metal gate electrode utilizing a replacement gate process has been formed. ... Processing can now be utilized to form, for example, silicide on the source and drain regions and to interconnect the n type non planar transistor and p type non planar transistor together into functional integrated circuits to form a complementary metal oxide semiconductor (CMOS) integrated circuit.”).)

124. Cheng, however, discloses additional steps that enable the interconnection of a transistor to surrounding circuitry using a borderless (self-aligned) contact, and a person of ordinary skill in the art would have found it had good reason, based on Cheng's teachings, to implement such a borderless source/drain contact in conjunction with Brask's transistor.

125. Like Brask, Cheng's third embodiment is related to field effect transistors (FETs) that utilize sacrificial gate structures, and a person of ordinary skill in the art implementing a transistor like that disclosed by Brask would have had reason to look to Cheng. (Ex. 1007, ¶[0052] ("In comparison to the conventional FETs of FIG. 1 and the first and second exemplary embodiments, the initial FETs of the third exemplary embodiment comprise dummy gates. That is, since the third exemplary embodiment utilizes a gate-last technique, the initial gates are dummy gates (e.g., placeholders) that will be replaced at a later time.")) Cheng further discloses that FinFETs have allowed the size of FET transistors to be reduced, which in turn has reduced the critical dimensions (CDs) of those transistors, thereby making the formation of contacts more difficult:

The size of FETs has been successfully reduced through the use of one or more fin-shaped channels. A FET employing such a channel structure may be referred to as a FinFET. Previously, CMOS devices were substantially planar along the surface of the semiconductor

substrate, the exception being the FET gate that was disposed over the top of the channel. Fins break from this paradigm by using a vertical channel structure in order to maximize the surface area of the channel that is exposed to the gate. The gate controls the channel more strongly because it extends over more than one side (surface) of the channel. For example, the gate can enclose three surfaces of the three-dimensional channel, rather than being disposed only across the top surface of the traditional planar channel.

As the CDs of CMOS devices are being aggressively scaled, forming contacts on those small devices is becoming more and more difficult [due] to the tight overlay tolerance.

(*Id.*, ¶¶[0008]-[0009].)

126. In this context, Cheng discloses that “[b]orderless contacts and techniques relating thereto help reduce the amount of space required for contacts, and enable production of smaller devices having a tighter pitch.” (*Id.*, ¶[0009]; *see also id.*, ¶[0031] (“As noted above, device scaling results in a small space for forming the borderless contact.”).) Therefore, a person of ordinary skill in the art would have understood that Cheng discloses or suggests that borderless contacts (i.e., self-aligned contacts), as taught by Cheng, are applicable to devices with reduced critical dimensions like the FinFETs disclosed by Brask.

127. Cheng's transistor formation, like that of Brask, includes removal of dummy gates (e.g. sacrificial gates) and then formation of a replacement gate structure in the resulting opening between the spacers, where the gate is formed by first depositing a dielectric layer and then depositing conductive gate material in the form of a metal gate. (Ex. 1007, ¶[0053] (“As depicted in FIG. 22, a high-k dielectric (HKD) 330 is deposited over the structure (e.g., the entire structure, including the ILD 324). Subsequently, and as shown in FIG. 23, a metal gate (MG) 332 is deposited, planarized and recessed.”), ¶[0043], [0051].)

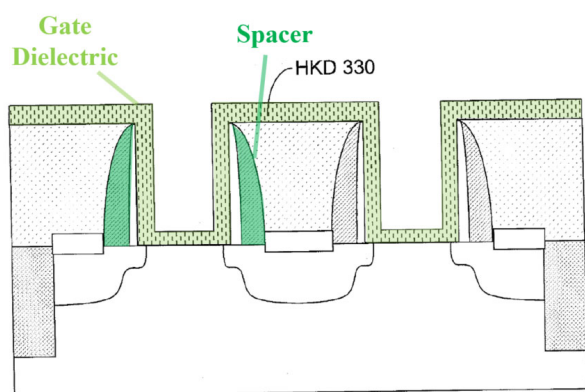


FIG. 22

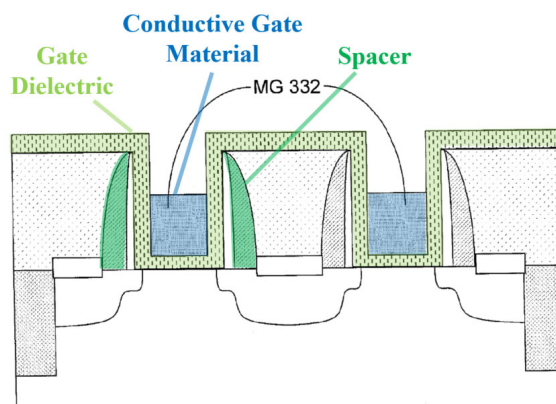


FIG. 23

(*Id.*, FIGs. 22, 23 (annotated).)

128. Cheng further discloses that after depositing the material for the metal gate, the gate material is recessed in order to allow for formation of a cap (*id.*, ¶[0054]) that, along with spacers, isolates the gate from a subsequently formed borderless contact:

The exemplary technique illustrated by FIGS. 20-26 depict the formation of a borderless contact (e.g., in a MOSFET) with a gate-last (e.g., a metal gate.) As a non-limiting example, the final structure of the gate stack may include a metal gate core (MG 332) that is surrounded (e.g., adjacent) on at least two sides/surfaces by a dielectric (e.g., a high-k dielectric such as HKD 330, which is adjacent to at least sidewall surfaces and a bottom surface of the MG 332). The dielectric may not be adjacent to a top surface of the metal gate core. **The borderless contact is isolated from the gate by a spacer(s) and insulating cap layer (CAP2 340).**

(*Id.*, ¶[0055] (emphasis added).)

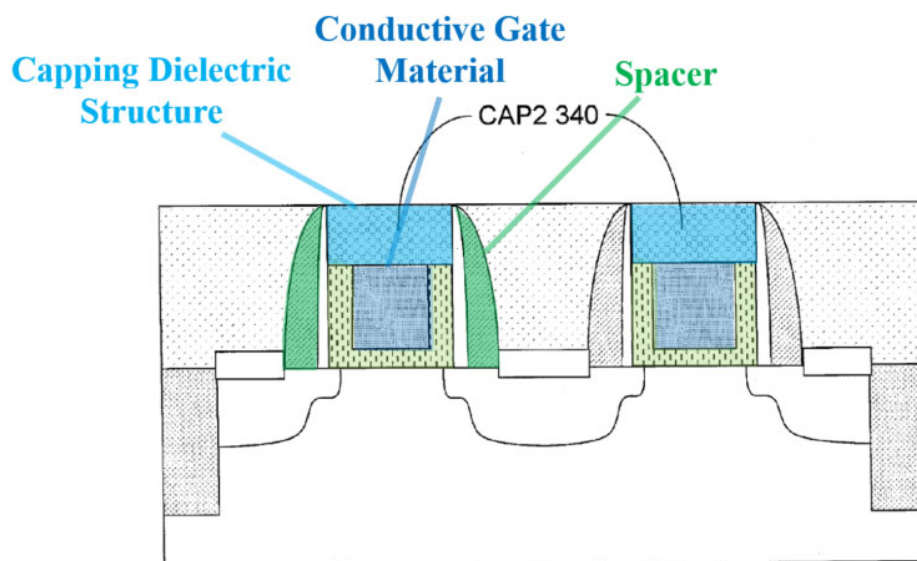


FIG. 25

(*Id.*, FIG. 25 (annotated).)

129. Therefore, having looked to Cheng, a person of ordinary skill in the art would have had good reason to form a contact to the source/drain region in a transistor like that disclosed by Brask based on the disclosure of Cheng. A person of ordinary skill in the art would have been motivated to use Cheng's contact formation technique both because Brask does not provide any description as to how to form such contacts and because the borderless or self-aligned contact formation technique of Cheng provides advantages applicable to FinFET devices. (*See* my discussion above in section V.C.) As Cheng discloses, self-aligned borderless contacts are useful in devices having reduced critical dimensions (e.g. gate length) such as FinFETs. (Ex. 1007, ¶¶[0008]-[0009].) Such contacts, which are self-aligned to the gate electrode, allow the contact to be formed closer to the gate structure than non-self-aligned contacts while reducing the risk of shorting the electrodes, thereby reducing the area needed to form the transistor and associated interconnect. (*See* my discussion above in section V.C.) A person of ordinary skill in the art would also have known that such self-aligned contacts allow for increased tolerance with respect to possible lithographic misalignment in the formation of the different structures of the transistor. (*Id.*) Therefore, a person of ordinary skill in the art would have been motivated to form self-aligned borderless contacts to provide the needed connections to the transistor of the Brask-Cheng combination.

130. Such contact formation includes removing a portion of the conductive material corresponding to the gate electrode to form a recess between the gate spacers as recited in claim element 1[i]. Following recessing of the gate material, a cap (“capping dielectric structure”) is formed in the recess, where, as disclosed by Cheng, the cap is a nitride cap. (Ex. 1007, ¶[0054], (“CAP2 340 may comprise a nitride cap”).) A person of ordinary skill in the art would have understood that the cap protects the gate electrode from being damaged during the etching process and provides electrical isolation for the gate structure to avoid unwanted shorts between the gate and other contacts (e.g., source/drain contacts). (*Id.*, ¶[0055]; Ex. 1006, ¶¶[0059]-[0072] (disclosing a protective cap structure to protect the gate structure from being damaged by an etching process to form a contact hole).)

131. Cheng discloses that “CAP2 340 may be formed by deposition and planarization” (Ex. 1007, ¶[0054]), where Cheng further discloses that such deposition can be performed using high density plasma CVD (HDPCVD):

Unless described otherwise herein, “depositing” may include any now known or later developed techniques appropriate for the material to be deposited, including, but not limited to: CVD, LPCVD, PECVD, semi-atmosphere CVD (SACVD), **high density plasma CVD (HDPCVD)**, rapid thermal CVD (RTCVD), ultra-high vacuum CVD (UHVCVD), limited reaction processing CVD (LRPCVD), metalorganic CVD (MOCVD), sputtering

deposition, ion beam deposition, electron beam deposition, laser assisted deposition, thermal oxidation, thermal nitridation, spin-on methods, physical vapor deposition (PVD), atomic level deposition (ALD), chemical oxidation, molecular beam epitaxy (MBE), plating or evaporation.

(*Id.*, ¶[0085] (emphasis added).)

132. A person of ordinary skill in the art would have known that high density plasma CVD (HDPCVD) is an appropriate deposition method for the nitride used to form the dielectric cap. (Ex. 1010, 6:32-37.) Therefore, the Brask-Cheng combination discloses or suggests that the dielectric cap (“capping dielectric structure”) is formed by high density plasma depositing as recited in claim element 1[j]. Indeed, a person of ordinary skill in the art would have had good reason to use high density plasma deposition to form the dielectric cap based on Cheng’s disclosure and their knowledge that such deposition provides superior gap-filling capabilities and therefore is suited to filling the recess formed between the spacers in the transistor of the Brask-Cheng combination. (Ex. 1015, 1:65-2:2 (“HDP-CVD processes generally have superior gapfill capabilities as compared to these other types of CVD processes because HDP-CVD deposition process provide[s] for a sputtering component to the deposition process simultaneous with film growth.”); Ex. 1016, 1:65-2:6.)

133. The self-aligned contact of the Brask-Cheng combination would have simply been the use of known techniques (e.g., forming borderless source/drain contacts as disclosed by Cheng) to a known device (Brask's FinFET) ready for improvement to yield predictable results of a FinFET device having a borderless source/drain contact. Therefore, the Brask-Cheng combination discloses or suggests claim elements 1[i] and 1[j], as these steps are included in the borderless contact formation process disclosed by Cheng that a person of ordinary skill in the art would have been motivated to use in conjunction with a transistor as disclosed by Brask.

**k) “forming at least one dielectric material over the source/drain region, the non-planar transistor gate spacers, and the capping dielectric structure; and”**

134. In my opinion, the Brask-Cheng combination discloses or suggests this feature. As I discuss above for claim elements 1[i]-1[j], the Brask-Cheng combination discloses or suggests the formation of a borderless contact according to the teachings of Cheng. (*See* my discussion above in sections IX.C.1[i]-[j].) Cheng discloses that, as a part of the contact formation process and before etching to form contact area 326, an interlayer dielectric layer ILD2 is deposited over the cap 340, gate spacers, and source/drain regions. (Ex. 1007, ¶[0054] (“[A]s shown in FIG. 26, a second layer of ILD (ILD2) 342 is deposited and planarized. A contact mask and a contact RIE are used to remove the ILD material from between the gates, thus

forming the space for the borderless contact.”), FIG. 26; *see also id.*, ¶[0029] (“an interlevel dielectric (ILD) 24 (e.g., an oxide) is deposited over the structure 10”).)

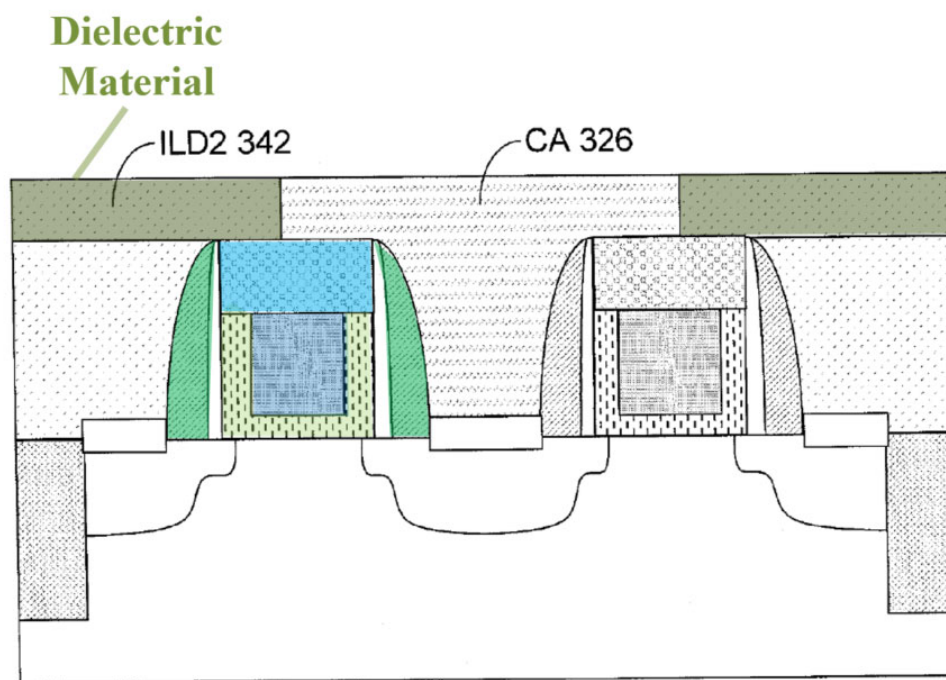


FIG. 26

(*Id.*, FIG. 26 (annotated).)

135. A person of ordinary skill in the art would have understood that the interlevel dielectric layer is used to separate different layers within the integrated circuit structure and isolate different contact structures (e.g., source/drain contacts) that are on the same layer. As such, a person of ordinary skill in the art would have been motivated to form such a dielectric layer as a part of the contact formation process as disclosed or suggested by Cheng.

**l) “forming a contact opening through the at least one dielectric material to expose at least a portion of the source/drain region.”**

136. In my opinion, the Brask-Cheng combination discloses or suggests this feature. As discussed above for claim elements 1[i]-1[j], the Brask-Cheng combination discloses or suggests the formation of a borderless contact according to the teachings of Cheng. (*See* my discussion above in sections IX.C.1[i]-[j].) Cheng discloses etching to form the space (“contact opening”) for contact area (CA) 326 through the interlevel dielectric layer 342 (“the at least one dielectric material”) and ILD 324 to expose the underlying source/drain region as a part of the contact formation process. (Ex. 1007, ¶[0054] (“A contact mask and a contact RIE are used to remove the ILD material from between the gates, thus forming the space for the borderless contact.”), FIG. 26.)

137. While Cheng discloses that “[s]ilicide may be formed at the source/drain regions” (Ex. 1007, ¶[0051]), a person of ordinary skill in the art would have understood that such silicides are meant to provide improved contact to the source/drain regions and are optional, which is consistent with the disclosure of Cheng. (Ex. 1007, ¶[0048] (“To reduce resistance, there may be a silicide (SIL) 22 over the S/D 216.”).) Moreover, such a person of ordinary skill in the art would have understood that such silicides need not be included in the Brask-Cheng transistor. Therefore, while annotated figure 26 below shows silicide 222 as part of

the source/drain region, a person of ordinary skill in the art would have known that such a silicide is optional such that the opening exposes the source/drain region directly.

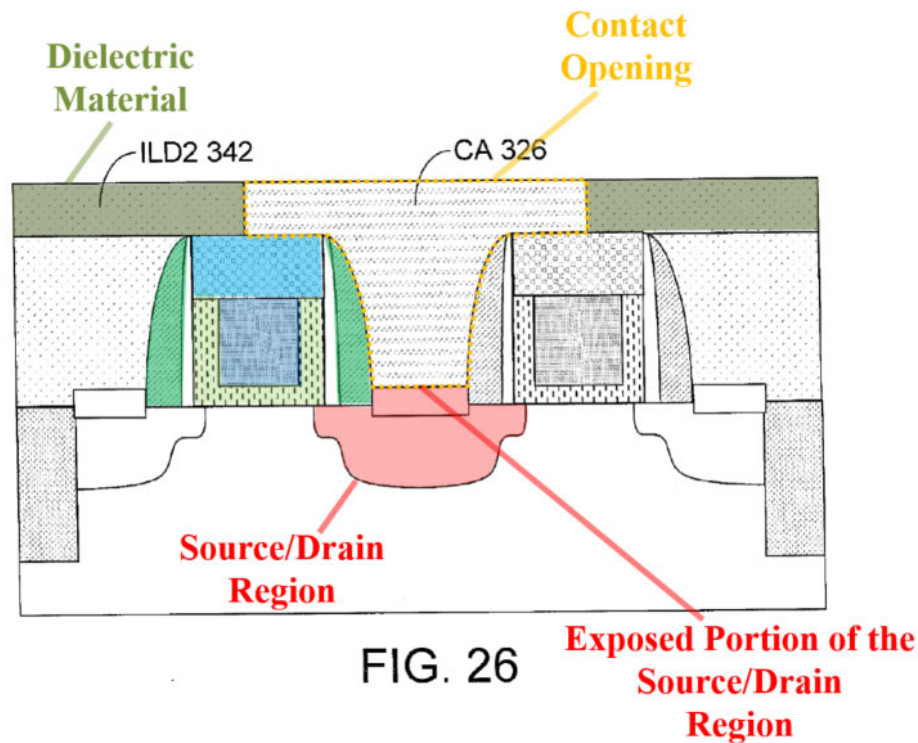


FIG. 26

(*Id.*, FIG. 26 (annotated).)

138. Consistent with the disclosure of Cheng, a person of ordinary skill in the art would have understood that such an opening allows for the subsequent deposition of conductive material to provide electrical contact to the source/drain region. (Ex. 1007, ¶[0054] (“The mask is removed and the contact area (CA) 326 is formed, as illustrated in FIG. 26, by filling the contact with conductive material, such as a metal, a metal containing material or a material comprising a metal, as non-

limiting examples.”).) Therefore, the Brask-Cheng combination discloses or suggests claim element 1[1].

## 2. Claim 2

**“The method of claim 1, wherein high density plasma depositing the capping dielectric structure comprises high density plasma depositing a silicon nitride capping dielectric structure.”**

139. In my opinion, Brask-Cheng combination discloses or suggests this feature. As I discuss above for claim element 1[j], the Brask-Cheng combination discloses or suggests forming a dielectric (“capping dielectric structure”) over the conductive material of the gate structure using high density plasma depositing according to the teaching of Cheng. (See my discussion above in section IX.C.1(j).) Cheng further discloses that the dielectric material can be “nitride.” (Ex. 1007, ¶[0054] (“CAP2 340 may comprise a nitride cap.”).)

140. To the extent that Cheng does not disclose that the “nitride” used to form the cap is silicon nitride, a person of ordinary skill in the art would have had good reason to form the nitride capping layer using silicon nitride. Cheng discloses that the spacers and capping layer isolate the gate region from the formed contact, and that the dielectric material of the spacers and capping layer is not removed when the etch to form the contact hole is performed. (Ex. 1007, ¶[0054].) Cheng further discloses that the spacers can be formed of silicon nitride (Ex. 1007, ¶[0043]), and a person of ordinary skill in the art would have understood that using silicon nitride

for both the cap and the spacers would be consistent with those layers not being removed during the etch.

141. Moreover, a person of ordinary skill in the art would have known that silicon nitride is an appropriate nitride to use for such a dielectric capping layer as it provides the ability to perform selective etches that remove the interlayer dielectric while leaving the silicon nitride capping layer and spacers. (Ex. 1006, ¶[0062] (“The protective cap structure 60 is typically composed of at least one of an oxide, nitride or oxynitride material. In one embodiment, in which the protective dielectric layer 18 is composed of a nitride, such as silicon nitride, and the mandrel dielectric layer 25 is composed of boron phosphorus silicate glass (BPSP), the protective cap structure 60 is composed of a nitride, such as silicon nitride.”).) Therefore, a person of ordinary skill in the art would have been motivated to use silicon nitride for the cap (“capping dielectric structure”) in the Brask-Cheng combination.

### 3. Claim 5

**“The method of claim 1, wherein forming a capping dielectric structure comprises: high density plasma depositing capping dielectric material within the recess; and removing excess capping dielectric material.”**

142. In my opinion, the Brask-Cheng combination discloses or suggests this feature. As discussed above for claim element 1[j], the Brask-Cheng combination discloses or suggests forming a cap (“capping dielectric structure”) over the

conductive material of the gate structure using high density plasma depositing, which is consistent with the disclosure of Cheng. (*See* my discussion above in section IX.C.1(j).) Cheng further discloses that after deposition of the material for the cap, planarization occurs, which a person of ordinary skill in the art would have understood removes excess capping dielectric material. (Ex. 1007, ¶[0054] (“The CAP2 340 may be formed by deposition and planarization.”); *see also* Ex. 1006, ¶[0064].)

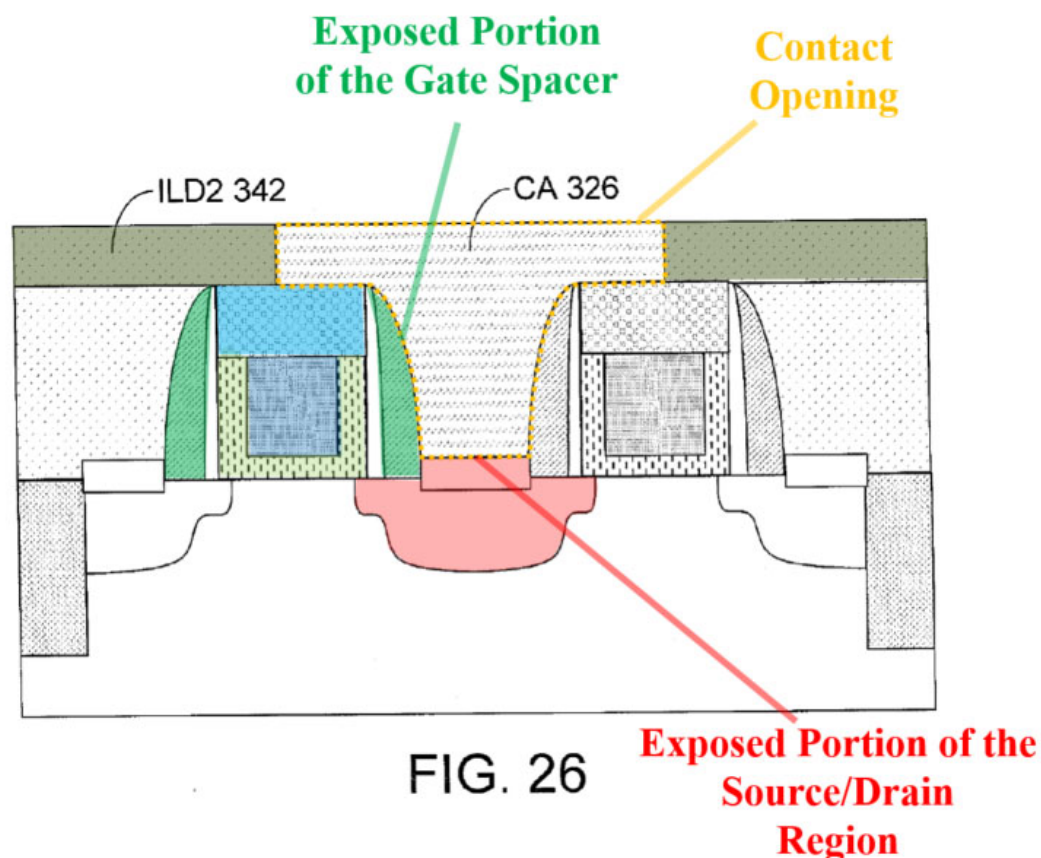
143. A person of ordinary skill in the art would have understood that such planarization steps are commonplace in the fabrication of integrated circuits, and, consistent with the disclosure of Cheng, would have been motivated to include such a step in the borderless contact formation process of the Brask-Cheng combination as such planarization promotes formation of subsequent overlying layers.

#### 4. Claim 6

**“The method of claim 1, wherein forming a contact opening through the dielectric material to expose at least a portion of the source/drain region further comprises forming a contact opening through the dielectric material which exposes at least a portion of the source/drain region and at least a portion of one non-planar transistor gate spacer.”**

144. In my opinion, the Brask-Cheng combination discloses or suggests this feature. As I discuss above for claim element 1[l], the Brask-Cheng combination discloses or suggests forming a contact opening as disclosed by Cheng to expose a

portion of the source/drain region. (See my discussion above in section IX.C.1(l).) Cheng further discloses that the etching operation used to form that opening does not remove the cap and spacers, which isolate the gate from the subsequently formed contact. (Ex. 1007, ¶[0055], FIG. 26.) As shown in annotated figure 26 below, the space formed for the deposition of the conductive material of the contact exposes a portion of the spacer.



(Ex. 1007, FIG. 26 (annotated).)

145. A person of ordinary skill in the art would have understood that in performing the etch to form the contact opening in the Brask-Cheng combination,

the spacers and cap would be exposed by the etch. Such an understanding is supported by Cheng's disclosure that the spacers and cap isolate the gate from the contact. (Ex. 1007, ¶[0055].) Moreover, such an understanding is also supported by a person of ordinary skill in the art's knowledge of borderless (e.g., self-aligned) contact formation. (Ex. 1006, ¶¶[0068]-[0070]; *see* my discussion above in section V.C.)

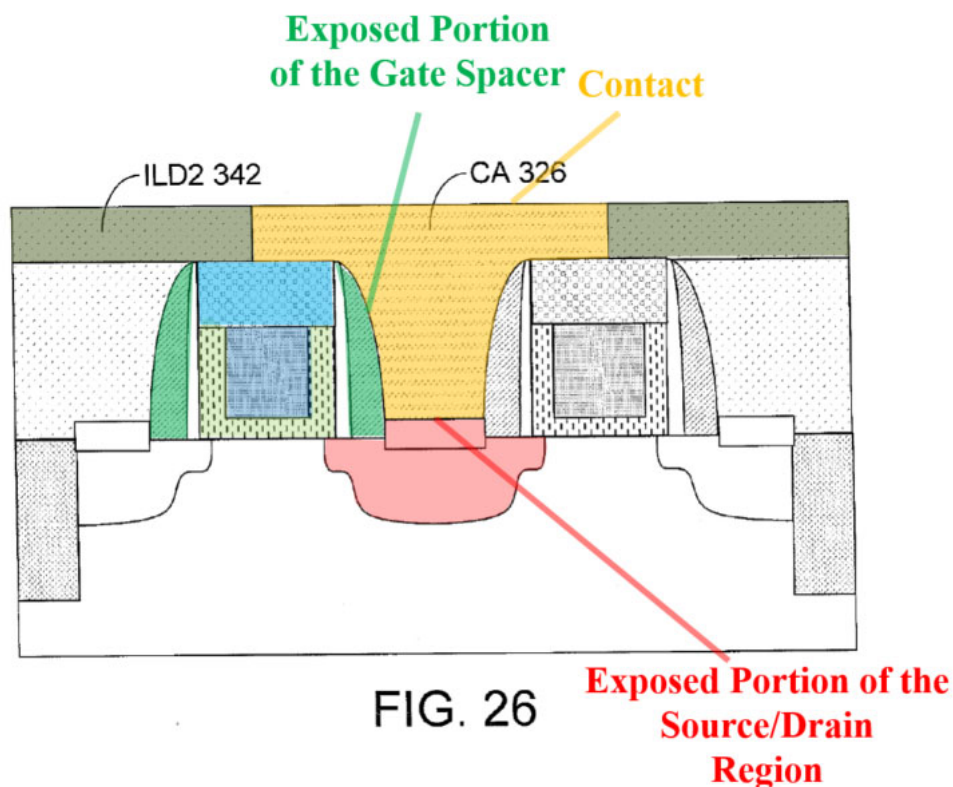
146. Therefore, in the Brask-Cheng combination, the etch ("forming a contact opening through the dielectric material which exposes at least a portion of the source/drain region") also exposes a portion of a gate spacer ("at least a portion of one non-planar transistor gate spacer").

## 5. Claim 7

**"The method of claim 6, further comprising forming a source/drain contact to abut the exposed portion of the source/drain region and exposed portion of the non-planar transistor gate spacer."**

147. In my opinion, the Brask-Cheng combination discloses or suggests this feature. As I discuss above for claim element 1[l], the Brask-Cheng combination discloses or suggests forming a contact opening to expose a portion of the source/drain region. (*See* my discussion above in section IX.C.1(l).) Cheng further discloses that the space corresponding to the contact area (CA) 326 is filled with conductive metal to form the contact for the transistor. (Ex. 1007, ¶[0054] ("The mask is removed and the contact area (CA) 326 is formed, as illustrated in FIG. 26,

by filling the contact with conductive material, such as a metal, a metal containing material or a material comprising a metal, as non-limiting examples.”). Consistent with the teachings of Cheng, the self-aligned contact formation of the Brask-Cheng combination fills the contact hole with conductive material to form a source/drain contact, where the contact abuts the exposed portions of the source/drain region and the gate spacer. Annotated figure 26 of Cheng shows the filled contact abutting the exposed portions of the source/drain region and gate spacer. Note that as I discussed above, a person of ordinary skill in the art would have understood that the silicide 222 shown in figure 26 is optional.

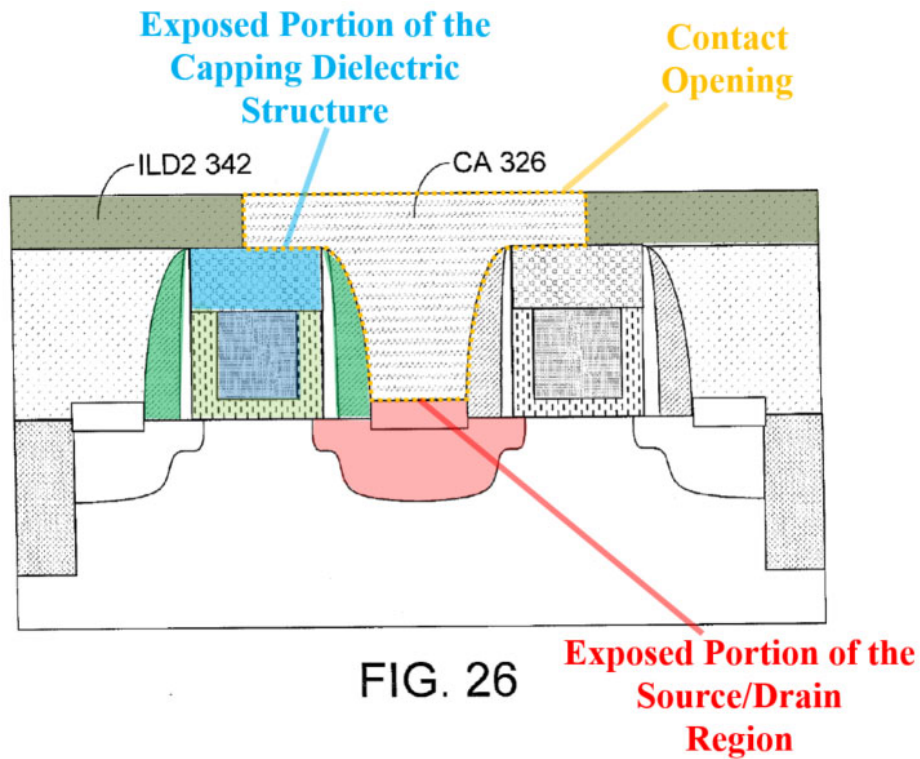


(Ex. 1007, FIG. 26 (annotated).)

**6. Claim 8**

**“The method of claim 1, wherein forming a contact opening through the dielectric material to expose at least a portion of the source/drain region further comprises forming a contact opening through the dielectric material which exposes at least a portion of the source/drain region and at least a portion of the capping dielectric structure.”**

148. In my opinion, the Brask-Cheng combination discloses or suggests this feature. As I discuss above for claim element 1[l], the Brask-Cheng combination discloses or suggests forming a contact opening to expose a portion of the source/drain region. (See my discussion above in section IX.C.1(l).) Cheng further discloses that the etching operation used to form that opening does not remove the cap and spacers, which isolate the gate from the subsequently formed contact. (Ex. 1007, ¶[0055], FIG. 26.) As shown in annotated figure 26 below, the space formed for the deposition of the conductive material of the contact exposes a portion of the cap (“capping dielectric structure”).



(*Id.*, FIG. 26 (annotated).)

149. A person of ordinary skill in the art would have understood that in performing the etch to form the contact opening in the Brask-Cheng combination, the spacers and cap would be exposed by the etch. Such an understanding is supported by Cheng's disclose that the spacers and cap isolate the gate from the contact. (Ex. 1007, ¶[0055].) Moreover, such an understanding is also supported by a person of ordinary skill in the art's knowledge of borderless (e.g., self-aligned) contact formation. (Ex. 1006, ¶¶[0068]-[0070]; *see* my discussion above in section V.C.) Therefore, in the Brask-Cheng combination, the etch ("forming a contact opening through the dielectric material which exposes at least a portion of the

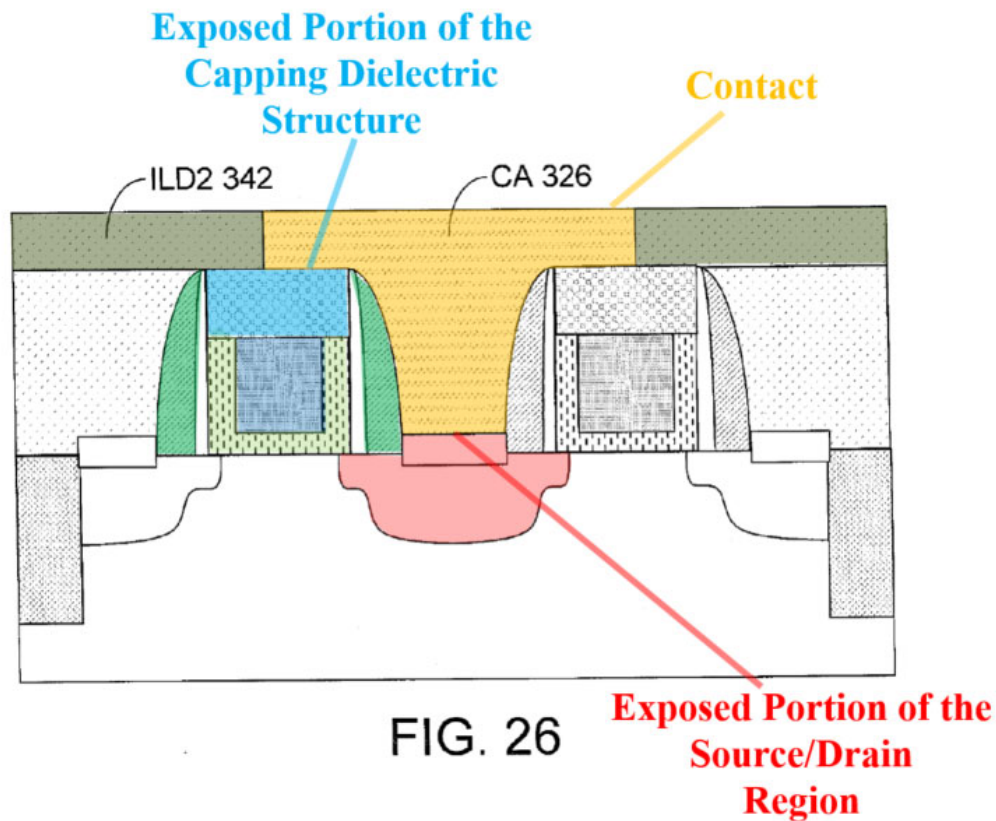
source/drain region”) also exposes a portion of the cap (“at least a portion of the capping dielectric structure”).

**7. Claim 9**

**“The method of claim 8, further comprising forming a source/drain contact abuts the exposed portion of the source/drain region and the exposed portion of the capping dielectric structure.”**

150. I have been asked to assume that claim 9 should read “forming a source/drain contact [abuts] to abut the exposed portion of the source/drain region and the exposed portion of the capping dielectric structure.” Under that assumption, it is my opinion that the Brask-Cheng combination discloses or suggests this feature. As I discuss above for claim element 1[1], the Brask-Cheng combination discloses or suggests forming a contact opening to expose a portion of the source/drain region. (See my discussion above in section IX.C.1(l).) Cheng further discloses that the space corresponding to the contact area (CA) 326 is filled with conductive metal to form the contact for the transistor. (Ex. 1007, ¶[0054] (“The mask is removed and the contact area (CA) 326 is formed, as illustrated in FIG. 26, by filling the contact with conductive material, such as a metal, a metal containing material or a material comprising a metal, as non-limiting examples.”).) Consistent with the teachings of Cheng, the self-aligned contact formation of the Brask-Cheng combination fills the contact hole with conductive material to form a source/drain contact, where the contact abuts the exposed portions of the source/drain region and the cap (“capping

dielectric structure”). Annotated figure 26 of Cheng shows the filled contact abutting the exposed portions of the source/drain region and cap. As I discuss above, the silicide 222 shown in figure 26 is optional.



(Ex. 1007, FIG. 26 (annotated).)

**8. Claim 10**

**“The method of claim 1, wherein forming a contact opening through the dielectric material to expose at least a portion of the source/drain region further comprises forming a contact opening through the dielectric material exposes at least a portion of the source/drain region, at least a portion of the non-planar transistor gate spacer, and at least a portion of the capping dielectric structure.”**

151. In my opinion, the Brask-Cheng combination discloses or suggests this feature for the reasons I discuss above for claims 6 and 8. (*See* my discussion above in sections IX.C.4, 6.)

**9. Claim 11**

**“The method of claim 10, further comprising forming a source/drain contact to abut the exposed portion of the source/drain region, the exposed portion of non-planar gate spacer, and the exposed portion of the capping dielectric structure.”**

152. In my opinion, the Brask-Cheng combination discloses or suggests this feature for the reasons I discuss above for claims 7 and 9. (*See* my discussion above in sections IX.C.5, 7.)

**D. Brask in Combination with Cheng and Park Discloses or Suggests the Features of Claims 1, 2, and 4-11**

**1. Claims 1, 2, and 5-11**

**“A computing system comprising the integrated circuit of claim 1.”**

153. As I discuss above in section IX.C, the Brask-Cheng combination discloses or suggests the features of claims 1, 2, and 5-11, including claim element 1[j], which requires “forming a capping dielectric structure within the recess by high density plasma depositing a dielectric material.” (See my discussion above in Section IX.C.) I have been asked to assume a scenario where the Brask-Cheng combination does not disclose or suggest forming the capping dielectric by “high density plasma deposition.” Under such a scenario, it is my opinion that a person of ordinary skill in the art would had good reason to form the capping layer using high density plasma chemical vapor deposition (HDPCVD) in view of Park and their knowledge of the state of the art.

154. Park, like Brask and Cheng, is directed to forming transistors with improved performance, where, like Cheng, Park discloses a nitride capping layer overlying the transistor structure, where Park is specific that the “nitride” capping layer is silicon nitride. (Ex. 1010, Abstract (“forming a first capping nitride layer covering the gate electrode and the source/drain regions, the first capping nitride layer including a Si—H rich SiN layer”), 1:14-17.) Park further discloses that the

nitride capping layer can be formed using high density plasma chemical vapor deposition (HDPCVD). (Ex. 1010, 6:32-37 (“The capping nitride layer 37 may be formed at a temperature of about 350° C. to about 500° C. using, e.g., low pressure chemical vapor deposition (LPCVD), plasma enhanced chemical vapor deposition (PECVD), high density plasma chemical vapor deposition (HDPCVD), or a combination thereof.”).)

155. In view of Park, a person of ordinary skill in the art would have had good reason to form the nitride capping layer in a transistor of the Brask-Cheng combination discussed above in section IX.C using HDPCVD to deposit silicon nitride. Park discloses that silicon nitride is an appropriate material to use for a capping layer, and further discloses that HDPCVD is an appropriate method to deposit such a capping layer. (Ex. 1010, 6:32-37.) A person of ordinary skill in the art would have understood that HDPCVD is one of a finite number of identified and predictable options for depositing silicon nitride capping layers (as disclosed by Park), and would have had good reason to try using HDPCVD to form the silicon nitride capping layer with a reasonable expectation of success. Moreover, doing so would have been nothing more than the application of a known technique (HDPCVD deposition of silicon nitride) to a known device ready for improvement (the transistor of the Brask-Cheng combination) to yield predictable results (a functional transistor with a silicon nitride capping layer).

156. A person of ordinary skill in the art would have understood that using HDPCVD to form the silicon nitride cap provides certain advantages, including improved gap-fill capability, which such a skilled person would have recognized is particularly relevant to formation of the capping dielectric structure in the recessed gate region in the Brask-Cheng combination. (Ex. 1015, 1:65-2:2 (“HDP-CVD processes generally have superior gapfill capabilities as compared to these other types of CVD processes because HDP-CVD deposition process provide[s] for a sputtering component to the deposition process simultaneous with film growth.”); Ex. 1016, 1:65-2:6.) Therefore a person of ordinary skill in the art would have been motivated to use HDPCVD for forming the capping dielectric structure in order to avoid voids in the dielectric that could result in unwanted short circuits, or damage to the gate structure the dielectric is protecting. Based on their knowledge of the state of the art and Park’s disclosure, a person of ordinary skill in the art would have had a high likelihood of success. Therefore, the Brask-Cheng-Park combination discloses or suggests claim element 1[j], whereas the remaining features of claims 1, 2, and 5-11 are disclosed or suggested for the reasons I discuss above in section IX.C. (See my discussion above in sections IX.C.1-9.) Moreover, the Brask-Cheng-Park combination also discloses or suggests that the nitride material for the cap (“capping dielectric structure”) is silicon nitride, as recited in claim 2.

**2. Claim 4**

**“The method of claim 1, wherein high density plasma depositing the capping dielectric structure comprises high density plasma depositing the capping dielectric structure at a temperature between about 300° C. and 600° C.”**

157. In my opinion, the Brask-Cheng-Park combination discloses or suggests this feature. As I discuss above in section IX.D.1, the Brask-Cheng-Park combination discloses or suggests forming protective cap structure (“capping dielectric structure”) over the conductive material of the gate structure using high density plasma depositing. (*See* my discussion above in section IX.D.1.) Park further discloses that the nitride capping layer can be formed using high density plasma chemical vapor deposition (HDPCVD) at a temperature of 350-500° C., which is within the claimed range of 300-600° C. (Ex. 1010, 6:32-37 (“The capping nitride layer 37 may be formed at a temperature of about 350° C. to about 500° C. using, e.g., low pressure chemical vapor deposition (LPCVD), plasma enhanced chemical vapor deposition (PECVD), high density plasma chemical vapor deposition (HDPCVD), or a combination thereof.”).) Therefore, the Brask-Cheng-Park combination discloses or suggests claim 4.

**E. Brask in Combination with Siddiqui Discloses or Suggests the Features of Claims 1, 2, and 5-11**

158. In my opinion, Brask in combination with Siddiqui discloses or suggests the features of claims 1, 2, and 5-11 of the '699 patent.

**1. Claim 1**

**a) “A method comprising:”**

159. I understand that “[a] method, comprising” is the preamble to claim 1 of the ’699 patent. I have been asked to assume that the preamble is a claim limitation. Under that assumption, in my opinion, Brask discloses a method for the same reasons I discuss above in section IX.C.1(a) above. (*See* my discussion above in section IX.C.1(a).)

**b) “forming a sacrificial non-planar transistor gate over a non-planar transistor fin;”**

160. In my opinion, Brask discloses this claim feature for the same reasons I discuss above in section IX.C.1(b) above. (*See* my discussion above in section IX.C.1(b).)

**c) “depositing a dielectric material layer over the sacrificial non-planar transistor gate and the non-planar transistor fin;”**

**d) “forming non-planar transistor gate spacers from a portion of the dielectric material layer adjacent the sacrificial non-planar transistor gate;”**

161. In my opinion, Brask discloses these limitations for the same reasons I discuss above in sections IX.C.1(c)-(d) above. (*See* my discussion above in sections IX.C.1(c)-(d).)

**e) “forming a source/drain region;”**

162. In my opinion, Brask discloses this feature for the same reasons I discuss above in section IX.C.1(e) above. (*See* my discussion above in section IX.C.1(e).)

**f) “removing the sacrificial non-planar transistor gate to form a gate trench between the non-planar transistor gate spacers and expose a portion of the non-planar transistor fin;”**

163. In my opinion, Brask discloses these features for the same reasons I discuss above in section IX.C.1(f) above. (*See* my discussion above in section IX.C.1(f).)

**g) “forming a gate dielectric adjacent the non-planar transistor fin within the gate trench;”**

**h) “depositing conductive gate material within the gate trench;”**

164. In my opinion, Brask discloses these features for the same reasons I discuss above in section IX.C.1(g)-(h) above. (*See* my discussion above in sections IX.C.1(g)-(h).)

- i) **“removing a portion of the conductive gate material to form a recess between the non-planar transistor gate spacers;”**
- j) **“forming a capping dielectric structure within the recess by high density plasma depositing a dielectric material;”**

165. In my opinion, the Brask-Siddiqui combination discloses or suggests these features. As I discuss above for claim elements 1[a]-1[h], Brask discloses the formation of a non-planar transistor that includes a replacement gate structure. (*See* my discussion above in sections IX.C.1[a]-[h].) Brask does not explicitly disclose the additional steps that are taken after formation of the non-planar transistor in order to provide the needed connections (e.g., electrical connections to the source and drain regions) for such a transistor. While Brask specifically contemplates that such connections are required, Brask does not provide explicit disclosure of providing a source/drain contact to the non-planar transistor. (Ex. 1008, ¶[0079] (“At this point, fabrication on an n type device with a metal gate electrode and a p type device with a metal gate electrode utilizing a replacement gate process has been formed. ... Processing can now be utilized to form, for example, silicide on the source and drain regions and to interconnect the n type non planar transistor and p type non planar transistor together into functional integrated circuits to form a complementary metal oxide semiconductor (CMOS) integrated circuit.”).)

166. Siddiqui, however, discloses additional steps that enable the interconnection of a transistor to surrounding circuitry using a self-aligned source/drain contact, and a person of ordinary skill in the art would have had good reason, based on Siddiqui's teachings, to implement such a self-aligned source/drain contact in conjunction with Brask's transistor.

167. Like Brask, Siddiqui is related to field effect transistors (FETs) that utilize sacrificial gate structures, and a person of ordinary skill in the art implementing a transistor like that disclosed by Brask would have had reason to look to Siddiqui. (Ex. 1006, Abstract, ¶[0022] ("Still referring to FIG. 1, a replacement gate structure 4 is formed overlying a channel region of the substrate 5. As used herein, a 'replacement gate structure' is a material having a geometry and location on the substrate 5 that determines the location for the later formed functional gate structure that is substituted for the replacement gate structure once the replacement gate structure has been removed.").)

168. As I discuss above in section IX.A.1(c) for the Cappellani-Siddiqui combination, Siddiqui discloses forming dielectric spacers 18 on the sidewalls of the sacrificial gate structure, and Siddiqui further discloses that by forming the dielectric spacers 18 using silicon nitride, the spacers 18 can be used together with a silicon nitride protective capping layer over the replacement gate to provide the ability to

control later etching of the opening in which the source/drain contacts are formed.  
(See my discussion above in sections IX.A.1(c)-(d); Ex. 1006, ¶[0032]-[0034].)

169. Specifically, as shown in annotated figure 3 below, Siddiqui discloses that after removing a sacrificial gate layer, a gate dielectric layer 30 is formed “at least on the channel region of the substrate 5.” (Ex. 1006, ¶[0043]; *see also id.*, ¶[0040].) A work function metal layer 35 is formed on the gate dielectric layer (*id.*, ¶[0043]), and metal fill material 40 is formed on the work function metal layer 35 (*id.*, ¶[0056]). As disclosed by Siddiqui, “[t]he metal fill material 40, work function metal layer 35 and the gate dielectric layer 30 provide a functional gate structure” (*id.*, ¶[0057]), where, as shown in annotated figure 3 below, the metal fill material 40 and work function metal layer 35 are conductive gate material. Therefore, like Brask, Siddiqui discloses reforming a gate structure that includes a gate dielectric and conductive gate material.

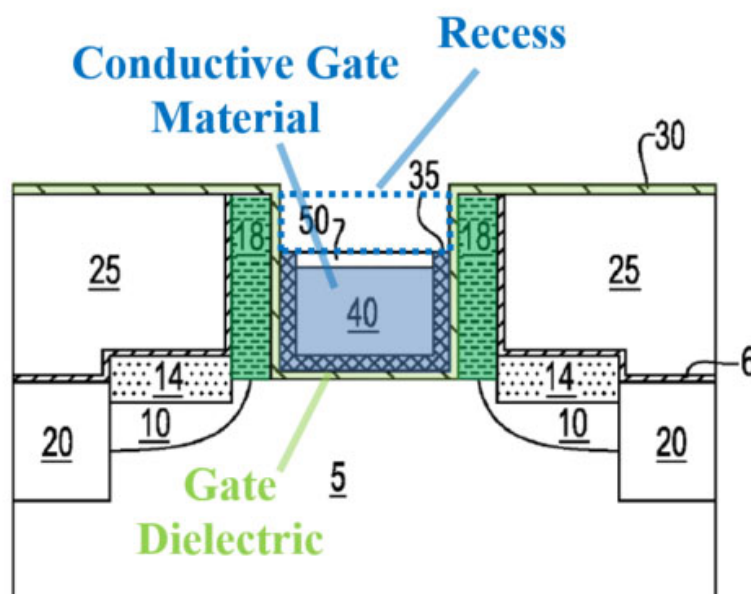


FIG. 3

(Ex. 1006, FIG. 3 (annotated).)

170. Siddiqui further discloses that the conductive gate material shown in annotated figure 3 above has been recessed to form a recess using, for example, an anisotropic reactive ion etch (RIE) or an isotropic wet etch:

Still referring to FIG. 3, the metal fill material 40 may be recessed below the upper surface of the mandrel dielectric layer 25 and the protective dielectric layer 18. In one embodiment, the **metal fill material 40 may be recessed using an etch process** that is selective to the work function metal layer 35. The etch process may be an anisotropic etch, such [as a] reactive ion etch (RIE), or the etch process may be an isotropic etch, such as a wet etch.

(Ex. 1006, ¶[0058] (emphasis added); *see also id.*, ¶¶[0059]-[0061].)

171. Following recessing of the metal fill material and selective removal of the portions of the work function metal layer 35, a dielectric protective cap structure, which is shown in annotated figure 4 below, is formed over the functional gate structure:

FIG. 4 depicts forming a protective cap structure 60 over the functional gate structure. In one embodiment, the protective cap structure 60 is composed of a dielectric material, and fills the upper portion of the opening that is present over the recessed surface of the metal fill 40. The protective cap structure 60 may be composed of any dielectric material that can protect the functional gate from being damaged during the etch process that provides the opening to the source regions 10 and the drain regions 15. The protective cap structure 60 is typically composed of at least one of an oxide, nitride or oxynitride material. In one embodiment, in which the protective dielectric layer 18 is composed of a nitride, such as silicon nitride, and the mandrel dielectric layer 25 is composed of boron phosphorus silicate glass (BPSP), the protective cap structure 60 is composed of a nitride, such as silicon nitride.

(*Id.*, ¶[0062].)

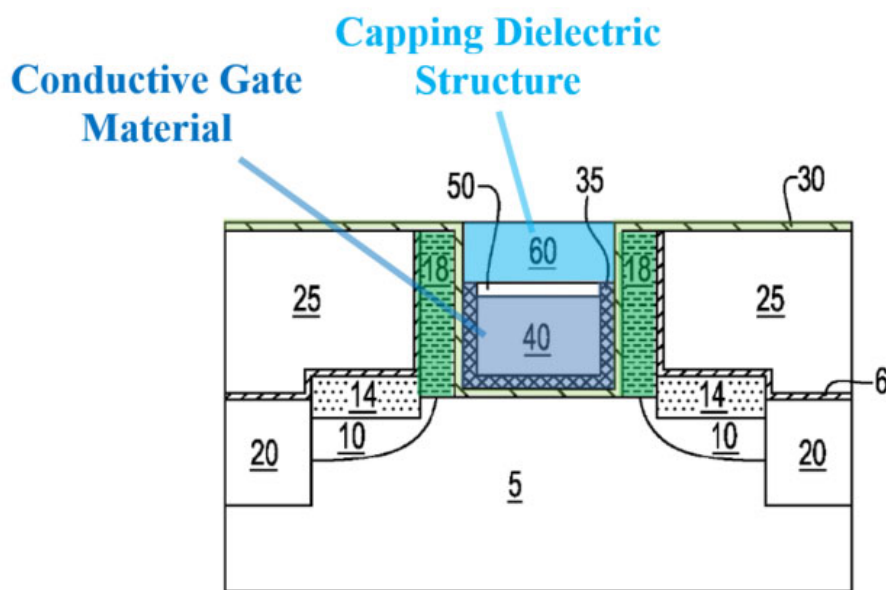


FIG. 4

(*Id.*, FIG. 4 (annotated).)

172. Therefore, Siddiqui discloses that, in order to form a self-aligned source/drain contact, a capping dielectric structure like that shown in figure 4 above is used to act as an etch stop and protect the gate structure during subsequent etching to form the openings for the contacts. In view of Siddiqui's disclosure, a person of ordinary skill in the art would have had good reason to recess the conductive material of the gate in a transistor like that disclosed by Brask to form a recess between the transistor gate spacers, where a capping dielectric structure is then formed in the recess. As disclosed by Siddiqui, these steps are part of the process for forming self-aligned source/drain contacts. (Ex. 1006, ¶[0070] ("The contacts 90 are self-aligned to the diffusion regions, i.e., source regions 10 and drain regions 15, because the

functional gate is protected from being damaged by the etch process that forms the vias 75 for the contacts 90 by the protective cap structure 60 that is present over the functional gate, and the protective dielectric layer 18 that is present on the sidewall of the functional gate.”.)

173. As noted above and as would have been understood by a person of ordinary skill in the art, Brask contemplates the need for electrical connections to the transistor (e.g., source/drain contacts), but does not disclose the steps to form such electrical connections. Siddiqui, however, provides such disclosure, and a person of ordinary skill in the art would have had good reason to use Siddiqui’s contact-formation method in conjunction with a transistor as disclosed by Brask. Formation of the source/drain contacts in a transistor as disclosed by Brask using the methodology disclosed by Siddiqui would have been nothing more than the application of a known technique (Siddiqui’s self-aligned contact formation) to a known device (Brask’s transistor) ready for improvement (adding electrical connections known to be needed) to yield predictable results (a transistor having connectivity to other circuit elements).

174. A person of ordinary skill in the art would have been motivated to use Siddiqui’s contact formation technique both because Brask does not provide any description as to how to form such contacts and because the self-aligned contact formation technique of Siddiqui provides advantages applicable to FinFET devices

like that disclosed by Brask. As a person of ordinary skill in the art would have known, self-aligned contacts, which are sometimes referred to as “borderless contacts,” are useful in devices having small critical dimensions (e.g. gate length) such as FinFETs. (Ex. 1007, ¶¶[0008]-[0009].) Such contacts, which are self-aligned to the gate electrode, allow the contact to be formed closer to the gate structure than non-self-aligned contacts while reducing the risk of shorting the electrodes, thereby reducing the area needed to form the transistor and associated interconnect. (*See* my discussion above in section V.C.) A person of ordinary skill in the art would also have known that such self-aligned contacts allow for increased tolerance with respect to possible lithographic misalignment in the formation of the different structures of the transistor. (*Id.*) Therefore, a person of ordinary skill in the art would have been motivated to form self-aligned contacts to provide the needed connections to the transistor of the Brask-Siddiqui combination.

175. Siddiqui further discloses that protective cap structure 60 may be a dielectric material formed using high-density chemical vapor deposition (HDCVD). (Ex. 1006, ¶[0062] (“In one embodiment, the protective cap structure 60 is composed of a dielectric material, and fills the upper portion of the opening that is present over the recessed surface of the metal fill 40.”), ¶[0063] (“The protective cap structure 60 may be formed by a deposition process including...chemical vapor deposition (CVD),” including “high-density chemical vapor deposition

(HDCVD)).) A person of ordinary skill in the art would have understood that HDCVD is “high density plasma deposition” as recited in claim element 1[j]. (Ex. 1011, 5:56-57 (“high-density plasma chemical vapor deposition (HDCVD) process”); Ex. 1012, 3:62-63 (“a high-density plasma chemical deposition (HDCVD).”); Ex. 1013, 10:9-10 (“high density plasma CVD (HDCVD) method”); Ex. 1014, ¶[0039] (“High-Density Plasma CVD (HDCVD)).”)

176. Therefore, the Brask-Siddiqui combination discloses or suggests claim elements 1[i] and 1[j], as these steps are included in the self-aligned contact formation process disclosed by Siddiqui that a person of ordinary skill in the art would have been motivated to use in conjunction with a transistor as disclosed by Brask.

**k) “forming at least one dielectric material over the source/drain region, the non-planar transistor gate spacers, and the capping dielectric structure; and”**

177. In my opinion, the Brask-Siddiqui combination discloses or suggests this feature. As I discuss above for claim elements 1[i]-1[j], the Brask-Siddiqui combination discloses or suggests the formation self-aligned contacts for the transistor as disclosed by Siddiqui. (See my discussion above in sections IX.E.1[i]-[j].) Siddiqui discloses, before etching to form via 75 as a part of the contact formation process, an interlayer dielectric layer 85 is blanket deposited over the protective cap structure, gate spacers, and source/drain regions. (Ex. 1006, ¶[0065]

(“In some embodiments, prior to etching to form the via 75, an interlevel dielectric layer 85 is blanket deposited atop the structure depicted in FIG. 5.”); *see also id.*, ¶¶[0066]-[0067].)

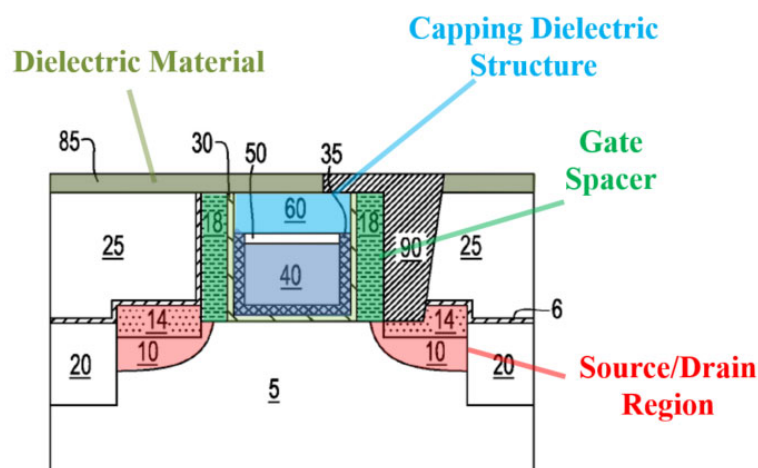


FIG. 6

(*Id.*, FIG. 6 (annotated).)

178. A person of ordinary skill in the art would have understood that the interlevel dielectric layer is used to separate different layers within the integrated circuit structure and isolate different contact structures (e.g., source/drain contacts) that are on the same layer. As such, a person of ordinary skill in the art would have been motivated to form such a dielectric layer as a part of the contact formation process as disclosed or suggested by Siddiqui.

- I) **“forming a contact opening through the at least one dielectric material to expose at least a portion of the source/drain region.”**

179. In my opinion, the Brask-Siddiqui combination discloses or suggests this feature. As I discuss above for claim elements 1[i]-1[j], the Brask-Siddiqui combination discloses or suggests the formation self-aligned contacts as disclosed by Siddiqui. (*See* my discussion above in sections IX.E.1[i]-[j].) As a part of the contact formation process, Siddiqui discloses etching to form via 75 (“contact opening”) through the interlevel dielectric layer 85 (“the at least one dielectric material”) and the mandrel dielectric layer 25 to expose the underlying source/drain region as a part of the contact formation process:

The interlevel dielectric layer 85 and the mandrel dielectric layer 25 are then patterned and etched to form vias 75 to the source regions 10 and the drain regions 15 using patterning and selective etch process. More specifically, a pattern is produced by applying a photoresist to the surface to be etched, exposing the photoresist to a pattern of radiation, and then developing the pattern into the photoresist using a resist developer. Once the patterning of the photoresist is completed, the sections covered by the photoresist are protected while the exposed regions are removed using a selective etching process that removes the unprotected regions to provide the vias 75.

(Ex. 1006, ¶[0068].)

180. Annotated figure 6 of Siddiqui shows the via 75 after conductive metal has been deposited in the contact opening to form the contact 90. (*Id.*, ¶¶0070[.] )

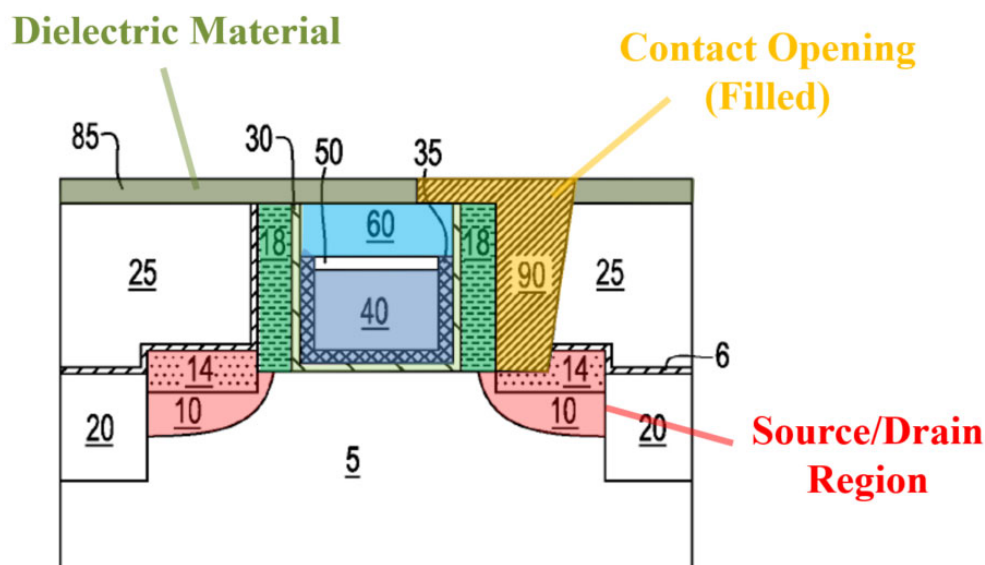


FIG. 6

(*Id.*, FIG. 6 (annotated).)

181. Consistent with the disclosure of Siddiqui, a person of ordinary skill in the art would have understood that such an opening allows for the subsequent deposition of conductive material to provide electrical contact to the source/drain region. (Ex. 1006, ¶[0070] (“Following via formation, contacts 90 are formed by depositing a conductive metal into the vias using deposition processing, such as CVD or plating.”).) Therefore, the Brask-Siddiqui combination discloses or suggests claim element 1[1].

**2. Claim 2**

**“The method of claim 1, wherein high density plasma depositing the capping dielectric structure comprises high density plasma depositing a silicon nitride capping dielectric structure.”**

182. In my opinion, Brask-Siddiqui combination discloses or suggests this feature. As I discuss above for claim element 1[j], the Brask-Siddiqui combination discloses or suggests forming protective cap structure (“capping dielectric structure”) over the conductive material of the gate structure using high density plasma depositing as disclosed by Siddiqui. (See my discussion above in section IX.E.1(j).) Siddiqui further discloses that, in order to provide the desired protection for the gate structure during the subsequent selective etch used to form the via 75, the dielectric material can be silicon nitride. (Ex. 1006, ¶[0062] (“The protective cap structure 60 is typically composed of at least one of an oxide, nitride or oxynitride material. In one embodiment, in which the protective dielectric layer 18 is composed of a nitride, such as silicon nitride, and the mandrel dielectric layer 25 is composed of boron phosphorus silicate glass (BPSP), the protective cap structure 60 is composed of a nitride, such as **silicon nitride.**”) (emphasis added).) Therefore the Brask-Siddiqui combination discloses or suggests claim 2.

**3. Claim 5**

**“The method of claim 1, wherein forming a capping dielectric structure comprises: high density plasma depositing capping dielectric material within the recess; and removing excess capping dielectric material.”**

183. In my opinion, the Brask-Siddiqui combination discloses or suggests this feature. As discussed above for claim element 1[j], the Brask-Siddiqui combination discloses or suggests forming protective cap structure (“capping dielectric structure”) over the conductive material of the gate structure using high density plasma depositing as disclosed by Siddiqui. (See my discussion above in section IX.E.1(j).) Siddiqui further discloses that, after deposition of the capping dielectric material in the recess, chemical mechanical planarization (CMP) is used to planarize the cap structure, which removes excess capping dielectric material:

Following deposition, the dielectric material that provides the protective cap structure 60 may be planarized stopping on the gate dielectric layer 30 that is present on an upper surface of the mandrel dielectric layer 25. In one example, the planarization process is provided by chemical mechanical planarization (CMP). In some embodiment, the planarization process may be continued until the gate dielectric layer 30 is removed from the upper surface of the mandrel dielectric layer 25, as depicted in FIG. 5.

(Ex. 1006, ¶[0064].)

184. A person of ordinary skill in the art would have understood that such planarization steps that remove excess material are commonplace in the fabrication of integrated circuits, and, consistent with the disclosure of Siddiqui, would have been motivated to include such a step in the self-aligned contact formation process as such planarization promotes formation of subsequent overlying layers.

#### 4. Claim 6

**“The method of claim 1, wherein forming a contact opening through the dielectric material to expose at least a portion of the source/drain region further comprises forming a contact opening through the dielectric material which exposes at least a portion of the source/drain region and at least a portion of one non-planar transistor gate spacer.”**

185. In my opinion, the Brask-Siddiqui combination discloses or suggests this feature. As I discuss above for claim element 1[l], the Brask-Siddiqui combination discloses or suggests forming a contact opening to expose a portion of the source/drain region. (See my discussion above in section IX.E.1(l).) Siddiqui further discloses that the etching operation used to form that opening is a selective etch that etches the protective cap structure 60 and protective dielectric layer 18 (e.g., gate spacers) at a slower rate than the dielectric material of the interlevel dielectric layer 85 and the mandrel dielectric layer 25:

The interlevel dielectric layer 85 and the mandrel dielectric layer 25 are then patterned and etched to form vias 75 to the source regions 10 and the drain regions 15

using patterning and selective etch process. More specifically, a pattern is produced by applying a photoresist to the surface to be etched, exposing the photoresist to a pattern of radiation, and then developing the pattern into the photoresist using a resist developer. Once the patterning of the photoresist is completed, the sections covered by the photoresist are protected while the exposed regions are removed using a selective etching process that removes the unprotected regions to provide the vias 75.

(Ex. 1006, ¶[0068].)

In one embodiment, the etch chemistry that provides the vias 75 removes at least the material of the mandrel dielectric layer 25 selective to the protective cap structure 60 and the protective dielectric layer 18, wherein the protective cap structure 60 and the protective dielectric layer 18 protect the functional gate structure from being damaged by the via 75 etch.

(*Id.*, ¶[0069]; *see also id.*, ¶[0070] (“the functional gate is protected from being damaged by the etch process that forms the vias 75 for the contacts 90 by the protective cap structure 60 that is present over the functional gate, and the **protective dielectric layer 18** that is present on the sidewall of the functional gate.”).)

186. Therefore, Siddiqui discloses that the selective etch removes portions the interlevel dielectric layer 85 and the mandrel dielectric layer 25, while the

protective cap structure 60 and the protective dielectric layer 18 act as an etch stop and protect the functional gate structure from the etch by preventing the etchants from reaching the gate structure. In other words, the etching operation stops or slows the rate of removal of material when it reaches (and hence exposes) the protective cap structure 60 and the protective dielectric layer 18. (See my discussion above in section V.C.) Therefore, as shown in annotated figure 6 of Siddiqui below, the etch (“forming a contact opening through the dielectric material which exposes at least a portion of the source/drain region”) also exposes a portion of a gate spacer (“at least a portion of one non-planar transistor gate spacer”).

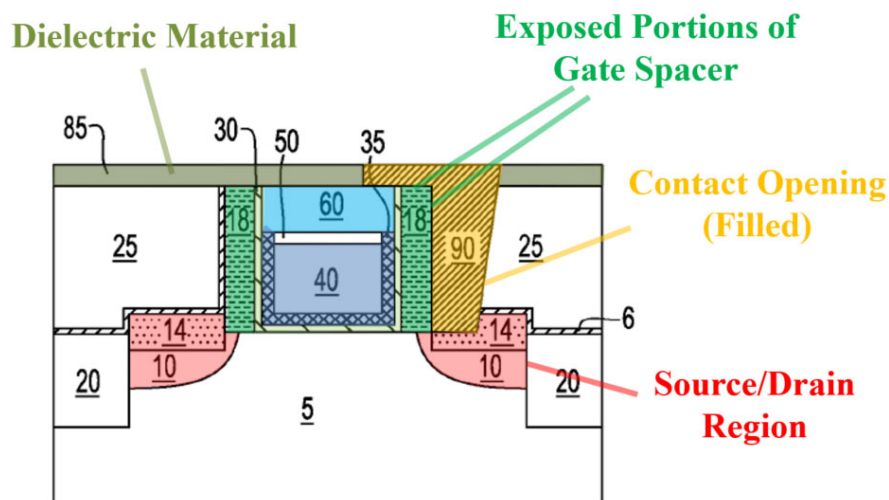


FIG. 6

(Ex. 1006, FIG. 6 (annotated).)

**5. Claim 7**

**“The method of claim 6, further comprising forming a source/drain contact to abut the exposed portion of the source/drain region and exposed portion of the non-planar transistor gate spacer.”**

187. In my opinion, the Brask-Siddiqui combination discloses or suggests this feature. As I discuss above for claim element 1[I], the Brask-Siddiqui combination discloses or suggests forming a contact opening to expose a portion of the source/drain region and a portion of the gate spacer. (See my discussion above in sections IX.E.1(I), IX.E.4.) Siddiqui further discloses that the via 75 corresponding to the contact opening is filled with conductive metal to form the contact 90 for the transistor. (Ex. 1006, ¶[0070] (“Following via formation, contacts 90 are formed by depositing a conductive metal into the vias using deposition processing, such as CVD or plating.”).) Consistent with the teachings of Siddiqui, the self-aligned contact formation of the Brask-Siddiqui combination fills the contact hole with conductive material to form a source/drain contact, where, because it fills the contact hole, the contact abuts the exposed portions of the source/drain region and the gate spacer.

188. Annotated figure 6 of Siddiqui below shows the filled contact abutting the exposed portions of the source/drain region and gate spacer. Note that as I discussed above, a person of ordinary skill in the art would have understood that the

“metal semiconductor alloy regions 14” are optional. (See my discussion above in section IX.E.5.)

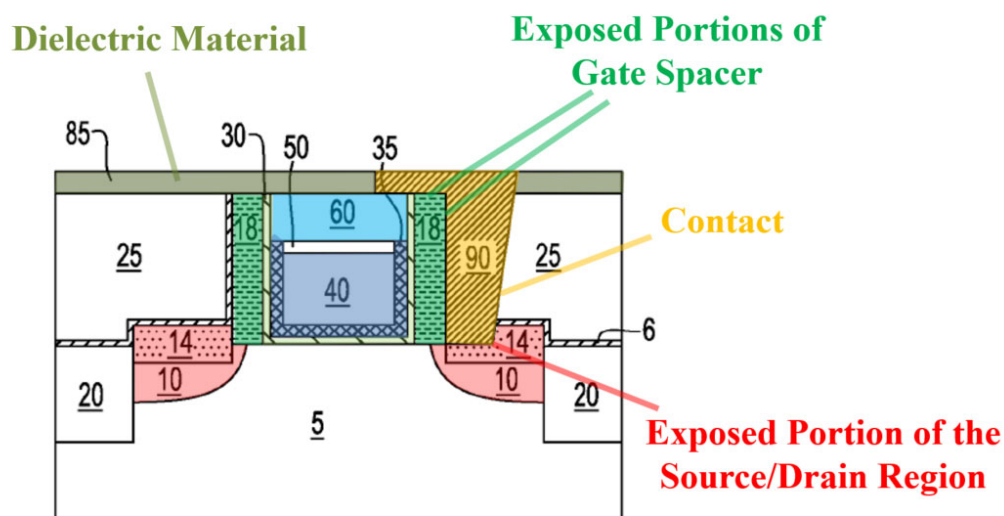


FIG. 6

(Ex. 1006, FIG. 6 (annotated).)

## 6. Claim 8

**“The method of claim 1, wherein forming a contact opening through the dielectric material to expose at least a portion of the source/drain region further comprises forming a contact opening through the dielectric material which exposes at least a portion of the source/drain region and at least a portion of the capping dielectric structure.”**

189. In my opinion, the Brask-Siddiqui combination discloses or suggests this feature. As I discuss above for claim element 1[l], the Brask-Siddiqui combination discloses or suggests forming a contact opening to expose a portion of the source/drain region. (See my discussion above in section IX.E.1(l).) Siddiqui

further discloses that the etching operation used to form that opening is a selective etch that etches the protective cap structure 60 and protective dielectric layer 18 (e.g., gate spacers) at a slower rate than the dielectric material of the interlevel dielectric layer 85 and the mandrel dielectric layer 25:

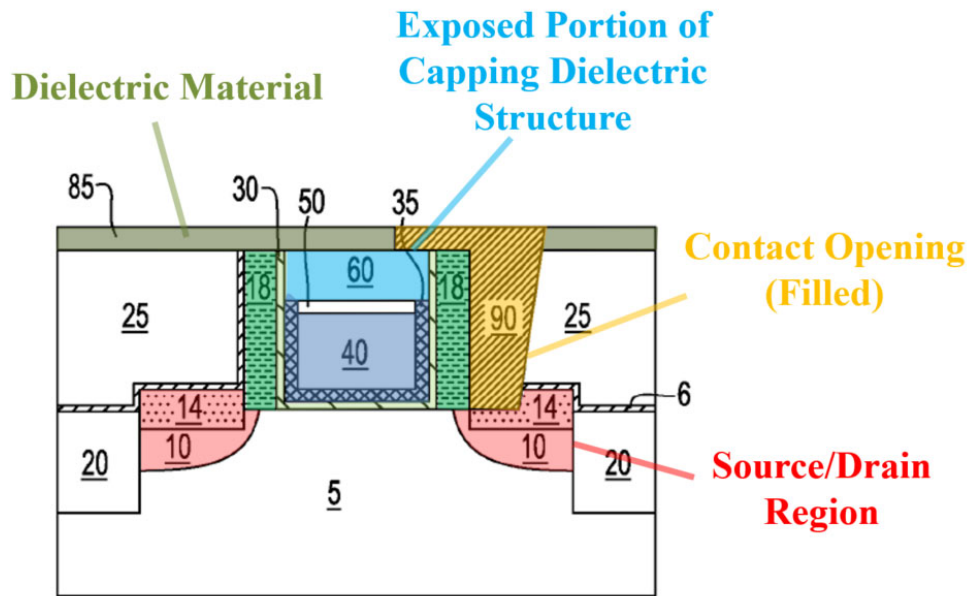
The interlevel dielectric layer 85 and the mandrel dielectric layer 25 are then patterned and etched to form vias 75 to the source regions 10 and the drain regions 15 using patterning and selective etch process. More specifically, a pattern is produced by applying a photoresist to the surface to be etched, exposing the photoresist to a pattern of radiation, and then developing the pattern into the photoresist using a resist developer. Once the patterning of the photoresist is completed, the sections covered by the photoresist are protected while the exposed regions are removed using a selective etching process that removes the unprotected regions to provide the vias 75.

(Ex. 1006, ¶[0068].)

In one embodiment, the etch chemistry that provides the vias 75 removes at least the material of the mandrel dielectric layer 25 selective to the protective cap structure 60 and the protective dielectric layer 18, wherein the protective cap structure 60 and the protective dielectric layer 18 protect the functional gate structure from being damaged by the via 75 etch.

(Ex. 1006, ¶[0069]; *see also id.*, ¶[0070] (“the functional gate is protected from being damaged by the etch process that forms the vias 75 for the contacts 90 by the **protective cap structure 60** that is present over the functional gate, and the protective dielectric layer 18 that is present on the sidewall of the functional gate.”) (emphasis added).)

190. Therefore, Siddiqui discloses that the selective etch removes portions the interlevel dielectric layer 85 and the mandrel dielectric layer 25, while the protective cap structure 60 and the protective dielectric layer 18 act as an etch stop and protect the functional gate structure from the etch by preventing the etchants from reaching the gate structure. In other words, the etching operation stops or slows the rate of removal of material when it reaches the protective cap structure 60 and the protective dielectric layer 18. (*See* my discussion in section V.C.) Therefore, as shown in annotated figure 6 of Siddiqui below, the etch (“forming a contact opening through the dielectric material which exposes at least a portion of the source/drain region”) also exposes a portion of the capping dielectric structure.



(Ex. 1006, FIG. 6 (annotated).)

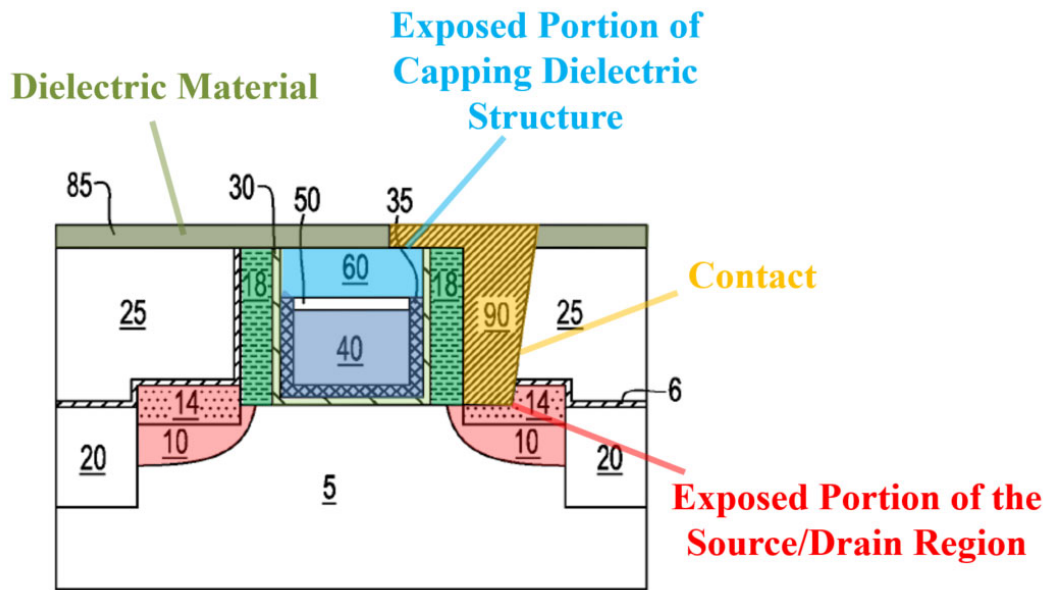
#### 7. Claim 9

**“The method of claim 8, further comprising forming a source/drain contact abuts the exposed portion of the source/drain region and the exposed portion of the capping dielectric structure.”**

191. I have been asked to assume that claim 9 should read “forming a source/drain contact [abuts] to abut the exposed portion of the source/drain region and the exposed portion of the capping dielectric structure.” Under that assumption, it is my opinion that the Brask-Siddiqui combination discloses or suggests this feature. As I discuss above for claim element 1[1], the Brask-Siddiqui combination discloses or suggests forming a contact opening to expose a portion of the source/drain region. (*See* my discussion above in section IX.E.1(1).) Siddiqui

further discloses that the via 75 corresponding to the contact opening is filled with conductive metal to form the contact 90 for the transistor. (Ex. 1006, ¶[0070] (“Following via formation, contacts 90 are formed by depositing a conductive metal into the vias using deposition processing, such as CVD or plating.”).) Consistent with the teachings of Siddiqui, the self-aligned contact formation of the Brask-Siddiqui combination fills the contact hole with conductive material to form a source/drain contact, where, because it fills the contact hole, the contact abuts the exposed portions of the source/drain region and the capping dielectric structure.

192. Annotated figure 6 of Siddiqui below shows the filled contact abutting the exposed portions of the source/drain region and capping dielectric structure. As I discuss above, the while Siddiqui discloses that “metal semiconductor alloy regions 14 may be formed atop the source regions 10 and the drain regions,” a person of ordinary skill in the art would have understood that such alloy regions are meant to provide improved contact to the source/drain regions and are optional. (*See my discussion above in IX.E.5.*)



(Ex. 1006, FIG. 6 (annotated).)

#### 8. Claim 10

“The method of claim 1, wherein forming a contact opening through the dielectric material to expose at least a portion of the source/drain region further comprises forming a contact opening through the dielectric material exposes at least a portion of the source/drain region, at least a portion of the non-planar transistor gate spacer, and at least a portion of the capping dielectric structure.”

193. In my opinion, the Brask-Siddiqui combination discloses or suggests this feature for the reasons I discuss above for claims 6 and 8. (See my discussion above in sections IX.E.4, 6.)

**9. Claim 11**

**“The method of claim 10, further comprising forming a source/drain contact to abut the exposed portion of the source/drain region, the exposed portion of non-planar gate spacer, and the exposed portion of the capping dielectric structure.”**

194. In my opinion, the Brask-Siddiqui combination discloses or suggests this feature for the reasons I discuss above for claims 7 and 9. (*See* my discussion above in sections IX.E.5, 7.)

**F. Brask in Combination with Siddiqui and Park Discloses or Suggests the Features of Claims 1, 2, and 4-11**

**1. Claims 1, 2, and 5-11**

195. As I discuss above in section IX.E, the Brask-Siddiqui combination discloses or suggests the features of claims 1, 2, and 5-11, including claim element 1[j], which requires “forming a capping dielectric structure within the recess by high density plasma depositing a dielectric material.” (*See* my discussion above in Section IX.E.) To the extent PO argues that the Brask-Siddiqui combination does not disclose or suggest forming the capping dielectric by “high density plasma deposition,” a person of ordinary skill in the art would have had good reason to form the capping layer using high density plasma chemical vapor deposition (HDPCVD) in view of Park and their knowledge of the state of the art.

196. Park, like Brask and Siddiqui, is directed to forming transistors with improved performance, where, like Siddiqui, Park discloses a nitride capping layer

overlying the transistor structure, where Park is specific that the “nitride” capping layer is silicon nitride. (Ex. 1010, Abstract (“forming a first capping nitride layer covering the gate electrode and the source/drain regions, the first capping nitride layer including a Si—H rich SiN layer”), 1:14-17.) Park further discloses that the nitride capping layer can be formed using high density plasma chemical vapor deposition (HDPCVD). (Ex. 1010, 6:32-37 (“The capping nitride layer 37 may be formed at a temperature of about 350° C. to about 500° C. using, e.g., low pressure chemical vapor deposition (LPCVD), plasma enhanced chemical vapor deposition (PECVD), high density plasma chemical vapor deposition (HDPCVD), or a combination thereof.”).)

197. In view of Park, a person of ordinary skill in the art would have had good reason to form the silicon nitride protective cap structure in a transistor of the Brask-Siddiqui combination discussed above in section IX.E using HDPCVD to deposit the silicon nitride. (*See* my discussion above in sections IX.E.1(j), IX.E.2.) Park discloses that silicon nitride is an appropriate material to use for a capping layer, and further discloses that HDPCVD is an appropriate method to deposit such a capping layer. (Ex. 1010, 6:32-37.) A person of ordinary skill in the art would have understood that HDPCVD is one of a finite number of identified and predictable options for depositing silicon nitride capping layers (as disclosed by Park), and would have had good reason to try using HDPCVD to form the silicon nitride

capping layer with a reasonable expectation of success. Moreover, doing so would have been nothing more than the application of a known technique (HDPCVD deposition of silicon nitride) to a known device ready for improvement (the transistor of the Brask-Siddiqui combination) to yield predictable results (a functional transistor with a silicon nitride capping layer).

198. A person of ordinary skill in the art would also have understood that using HDPCVD to form the silicon nitride can provide certain advantages, including improved gap-fill capability, which such a skilled person would have recognized is particularly relevant to formation of the capping dielectric structure in the recessed gate region in the Brask-Siddiqui combination. (Ex. 1015, 1:65-2:2 (“HDP-CVD processes generally have superior gapfill capabilities as compared to these other types of CVD processes because HDP-CVD deposition process provide[s] for a sputtering component to the deposition process simultaneous with film growth.”); Ex. 1016, 1:65-2:6.) Therefore, a person of ordinary skill in the art would have been motivated to use HDPCVD for forming the capping dielectric structure in order to avoid voids in the dielectric that could result in unwanted short circuits or damage to the gate structure the dielectric is protecting. Based on their knowledge of the state of the art and Park’s disclosure, a person of ordinary skill in the art would have had a high likelihood of success.

199. As such, the Brask-Siddiqui-Park combination discloses or suggests claim element 1[j], whereas the remaining features of claims 1, 2, and 5-11 are disclosed or suggested for the reasons provided above in section IX.E. (*See my discussion above in sections IX.E.1-9.*)

**2. Claim 4**

**“The method of claim 1, wherein high density plasma depositing the capping dielectric structure comprises high density plasma depositing the capping dielectric structure at a temperature between about 300° C. and 600° C.”**

200. In my opinion, the Brask-Siddiqui-Park combination discloses or suggests this feature. As I discuss above in section IX.F.1, the Brask-Siddiqui-Park combination discloses or suggests forming protective cap structure (“capping dielectric structure”) over the conductive material of the gate structure using high density plasma depositing. (*See my discussion above in section IX.F.1.*) Park further discloses that the nitride capping layer can be formed using high density plasma chemical vapor deposition (HDPCVD) at a temperature of 350-500° C., which is within the claimed range of 300-600° C. (Ex. 1010, 6:32-37 (“The capping nitride layer 37 may be formed at a temperature of about 350° C. to about 500° C. using, e.g., low pressure chemical vapor deposition (LPCVD), plasma enhanced chemical vapor deposition (PECVD), high density plasma chemical vapor

deposition (HDPCVD), or a combination thereof.”.) Therefore, the Brask-Siddiqui-Park combination discloses or suggests claim 4.

## **X. CONCLUSION**

201. In summary, it is my opinion that all of the features recited in claims 1, 2, and 4-11 of the '699 patent are disclosed or suggested by the prior art.

202. I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.



Dated: April 19, 2023

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Stanley Shanfield