PTO-1390 (03-13)
Approved for use through 4/30/2013. OMB 0651-0021
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A SUBMISSION UNDER 35 U.S.C. 371

Attorney Docket No.	
P38683US	
U.S. Application No. (if known, see 37 CFR 1.5)	
New Application	

International Application No.	International Filing Date	Priority Date Claimed
PCT/US2011/054464	September 30, 2011	September 30, 2011

Title of Invention
CAPPING DIELECTRIC STRUCTURE FOR TRANSISTOR GATES

First Named Inventor
Aaron W. Rosenbaum

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information.

1. ☑ This is an express request to begin national examination procedures (35 U.S.C. 371(f)). NOTE: The express request under 35 U.S.C. 371(f) will not be effective unless the requirements under 35 U.S.C. 371(c)(1), (2), and (4) for payment of the basic national fee, copy of the International Application and English translation thereof (if required), and the oath or declaration of the inventor(s) have been received.
2. ☑ A copy of the International Application (35 U.S.C. 371(c)(2)) is attached hereto (not required if the International Application was previously communicated by the International Bureau or was filed in the United States Receiving Office (RO/US)).
3. An English language translation of the International Application (35 U.S.C. 371(c)(2))
   a. ☑ is attached hereto.
   b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4).
4. An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4))
   a. ☑ is attached.
   b. ☐ was previously filed in the international phase under PCT Rule 4.17(iv).

Items 5 to 8 below concern amendments made in the international phase.

PCT Article 19 and 34 amendments

5. ☐ Amendments to the claims under PCT Article 19 are attached (not required if communicated by the International Bureau) (35 U.S.C. 371(c)(3)).
6. ☐ English translation of the PCT Article 19 amendment is attached (35 U.S.C. 371(c)(3)).
7. ☐ English translation of annexes (Article 19 and/or 34 amendments only) of the International Preliminary Examination Report is attached (35 U.S.C. 371(c)(5)).

Cancellation of amendments made in the international phase

8a. ☐ Do not enter the amendment made in the international phase under PCT Article 19.

8b. ☐ Do not enter the amendment made in the international phase under PCT Article 34.

NOTE: A proper amendment made in English under Article 19 or 34 will be entered in the U.S. national phase application absent a clear instruction from applicant not to enter the amendment(s).

The following items 9 to 17 concern a document(s) or information included.

9. ☐ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
10. ☐ A preliminary amendment.
11. ☑ An Application Data Sheet under 37 CFR 1.76.
12. ☐ A substitute specification. NOTE: A substitute specification cannot include claims. See 37 CFR 1.125(b).
13. ☐ A power of attorney and/or change of address letter.
14. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13*ter*.3 and 37 CFR 1.821-1.825.
15. ☐ Assignment papers *(cover sheet and document(s))*. Name of Assignee: _____
16. ☐ 37 CFR 3.73(c) Statement *(when there is an Assignee)*.

This collection of information is required by 37 CFR 1.414 and 1.491-1.492. The information is required to obtain or retain a benefit by the public, which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 15 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop PCT, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

PTO-1390 (03-13)
Approved for use through 4/30/2013. OMB 0651-0021
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

U.S. APPLN. No. (if known – see 37 CFR 1.5)	INTERNATIONAL APPLICATION No.	ATTORNEY DOCKET No.
	PCT/US2011/054464	P38683US

17. ☑ Other items or information:

International Search Report and Written Opinion

The following fees have been submitted.	CALCULATIONS	PTO USE ONLY
18. ☑ Basic national fee (37 CFR 1.492(a)) **$280**	$ 280	
19. ☑ Examination fee (37 CFR 1.492(c)) If the written opinion prepared by ISA/US or the international preliminary examination report prepared by IPEA/US indicates all claims satisfy provisions of PCT Article 33(1)-(4) ..... **$0** All other situations **$720**	720 $	
20. ☑ Search fee (37 CFR 1.492(b)) If the written opinion prepared by ISA/US or the international preliminary examination report prepared by IPEA/US indicates all claims satisfy provisions of PCT Article 33(1)-(4) ..... **$0** Search fee (37 CFR 1.445(a)(2)) has been paid on the international application to the USPTO as an International Searching Authority .....**$120** International Search Report prepared by an ISA other than the US and provided to the Office or previously communicated to the US by the IB .....**$480** All other situations **$600**	480 $	
TOTAL OF 18, 19, and 20 =	$ 1480	
☐ Additional fee for specification and drawings filed in paper over 100 sheets (excluding sequence listing in compliance with 37 CFR 1.821(c) or (e) in an electronic medium or computer program listing in an electronic medium) (37 CFR 1.492(j)). Fee for each additional 50 sheets of paper or fraction thereof **$400**		

Total Sheets	Extra Sheets	Number of each addition 50 or fraction thereof (round **up** to a whole number)	RATE	
- 100 =	/ 50 =		x **$400**	$

Surcharge of **$140.00** for furnishing any of the search fee, examination fee, or the oath or declaration after the date of commencement of the national stage (37 CFR 1.492(h)).	$	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	25 - 20 =	5	x **$80**	$ 400	
Independent claims	4 - 3 =	1	x **$420**	$ 420	
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ **$780**	$	
Processing fee of **$140.00** for furnishing the English translation later than 30 months from the earliest claimed priority date (37 CFR 1.492(i)). +				$	
TOTAL OF ABOVE CALCULATIONS =				$ 820	
☐ **Applicant asserts small entity status.** See 37 CFR 1.27. Fees above are reduced by ½.					
☐ **Applicant certifies micro entity status.** See 37 CFR 1.29. Fees above are reduced by ¾. Applicant must attach form PTO/SB/15A or B or equivalent.					
TOTAL NATIONAL FEE =				$ 2300	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00** per property. +				$	
TOTAL FEES ENCLOSED =				$ 2300	
				Amount to be refunded:	$
				Amount to be charged:	$

a. ☐ A check in the amount of $_____ to cover the above fees is enclosed.

b. ☑ Please charge my Deposit Account No. 504238 in the amount of $ 2300 to cover the above fees.

c. ☑ The Director is hereby authorized to charge additional fees which may be required, or credit any overpayment, to Deposit Account No. 504238 as follows:

i. ☑ any required fee.

ii. ☐ any required fee except for excess claims fees required under 37 CFR 1.492(d) and (e) and multiple dependent claim fee required under 37 CFR 1.492(f).

d. ☐ Fees are to be charged to a credit card. **WARNING:** Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038. The PTO-2038 should only be mailed or faxed to the USPTO. However, when paying the basic national fee, the PTO-2038 may NOT be faxed to the USPTO.

ADVISORY: If filing by EFS-Web, do **NOT** attach the PTO-2038 form as a PDF along with your EFS-Web submission. Please be advised that this is **not** recommended and by doing so your **credit card information may be displayed via PAIR**. To protect your information, it is recommended to pay fees online by using the electronic payment method.

NOTE: Where an appropriate time limit under 37 CFR 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the International Application to pending status.

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File)Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013, and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.

NOTE: A U.S. national stage application may not claim priority to the international application of which it is the national phase. The filing date of a U.S. national stage application is the international filing date. See 35 U.S.C. 363.

Correspondence Address

☑ The address associated with Customer Number: 92265 **OR** ☐ Correspondence address below

Name					
Address					
City		State		Zip Code	
Country		Telephone			
Email					

Signature	/Robert G. Winkle/	Date	2013-06-06
Name (Print/Type)	Robert G. Winkle	Registration No. (Attorney/Agent)	37,474

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/AIA/14 (03-13)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P38683US
	Application Number	
Title of Invention	CAPPING DIELECTRIC STRUCTURE FOR TRANSISTOR GATES	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	AARON	W.	ROSENBAUM	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Portland	State/Province	OR	Country of Residence i	US

Mailing Address of Inventor:

Address 1	5530 Nw Osprey Place
Address 2	

City	Portland	State/Province	OR
Postal Code	97229	Country i	US

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	DIN-HOW		MEI	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Portland	State/Province	OR	Country of Residence i	US

Mailing Address of Inventor:

Address 1	5366 NW 132nd Ave.
Address 2	

City	Portland	State/Province	OR
Postal Code	97229	Country i	US

Inventor 3 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	SAMEER	S.	PRADHAN	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

PTO/AIA/14 (03-13)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P38683US
	Application Number	
Title of Invention	CAPPING DIELECTRIC STRUCTURE FOR TRANSISTOR GATES	

City	Portland	State/Province	OR	Country of Residence i	US

Mailing Address of Inventor:

Address 1	17923 NW Sylvania Lane		
Address 2			
City	Portland	State/Province	OR
Postal Code	97229	Country i	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	92265		
Email Address	inteldocs@cpaglobal.com	Add Email	Remove Email

Application Information:

Title of the Invention	CAPPING DIELECTRIC STRUCTURE FOR TRANSISTOR GATES		
Attorney Docket Number	P38683US	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)		Suggested Figure for Publication (if any)	

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P38683US
	Application Number	
Title of Invention	CAPPING DIELECTRIC STRUCTURE FOR TRANSISTOR GATES	

Customer Number	92265

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	a 371 of international	PCT/US2011/054464	2011-09-30

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(d). When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX) [i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(h)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

Application Number	Country [i]	Filing Date (YYYY-MM-DD)	Access Code [i] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.

Authorization to Permit Access:

PTO/AIA/14 (03-13)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P38683US
	Application Number	
Title of Invention	CAPPING DIELECTRIC STRUCTURE FOR TRANSISTOR GATES	

☒ Authorization to Permit Access to the Instant Application by the Participating Offices

If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application.

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date of filing this Authorization.

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1 Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

◯ Assignee	◯ Legal Representative under 35 U.S.C. 117	◯ Joint Inventor
◯ Person to whom the inventor is obligated to assign.	◯ Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor :

If the Applicant is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P38683US
	Application Number	
Title of Invention	CAPPING DIELECTRIC STRUCTURE FOR TRANSISTOR GATES	

Mailing Address Information:			
Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Non-Applicant Assignee Information:

Providing assignment information in this section does not subsitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Assignee 1

Complete this section only if non-applicant assignee information is desired to be included on the patent application publication in accordance with 37 CFR 1.215(b). Do not include in this section an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest), as the patent application publication will include the name of the applicant(s).

Remove

If the Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information:			
Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee Data may be generated within this form by selecting the Add button. Add

PTO/AIA/14 (03-13)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P38683US
	Application Number	
Title of Invention	CAPPING DIELECTRIC STRUCTURE FOR TRANSISTOR GATES	

Signature:

Remove

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications					
Signature	/Robert G. Winkle/			Date (YYYY-MM-DD)	2013-06-06
First Name	Robert G.	Last Name	Winkle	Registration Number	37474
Additional Signature may be generated within this form by selecting the Add button. Add					

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal	
Application Number:	
Filing Date:	
Title of Invention:	CAPPING DIELECTRIC STRUCTURE FOR TRANSISTOR GATES
First Named Inventor/Applicant Name:	AARON W. ROSENBAUM
Filer:	Robert G. Winkle
Attorney Docket Number:	P38683US
Filed as Large Entity	

U.S. National Stage under 35 USC 371 Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
National Stage Fee	1631	1	280	280
Natl Stage Search Fee - Report provided	1642	1	480	480
National Stage Exam - all other cases	1633	1	720	720
Pages:				
Claims:				
Claims in excess of 20	1615	5	80	400
Independent claims in excess of 3	1614	1	420	420
Miscellaneous-Filing:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**2300**

Electronic Acknowledgement Receipt	
EFS ID:	15971155
Application Number:	13992598
International Application Number:	PCT/US11/54464
Confirmation Number:	5215
Title of Invention:	CAPPING DIELECTRIC STRUCTURE FOR TRANSISTOR GATES
First Named Inventor/Applicant Name:	AARON W. ROSENBAUM
Customer Number:	92265
Filer:	Robert G. Winkle/Leon Hammer
Filer Authorized By:	Robert G. Winkle
Attorney Docket Number:	P38683US
Receipt Date:	07-JUN-2013
Filing Date:	
Time Stamp:	17:02:38
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$2300
RAM confirmation Number	4290
Deposit Account	504238
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. 1.492 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		P38683PCT_Spec.pdf	105720 a5d6a2960ef53e7cb3c7b7b30c0839e059ff26b6	yes	15
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Specification		1	11	
	Claims		12	14	
	Abstract		15	15	
Warnings:					
Information:					
2	Drawings-only black and white line drawings	P38683PCT_Figs.pdf	558232 2199c5e0186bd42dbc559124d46b592750f8635d	no	13
Warnings:					
Information:					
3	Oath or Declaration filed	P38683PCT_Dec_use.pdf	45711 a726e0db3b08589a09dee9fd0de2d498f13f878b	no	2
Warnings:					
Information:					
4	Documents submitted with 371 Applications	P38683PCT_ISR_WO.pdf	360042 82c9c3dbfc0756fdce72ba4622a31de0adcbce5f	no	9
Warnings:					
Information:					
5	Transmittal of New Application	P38683US_1390.pdf	222552 78714f7473c3b5badf50d7354e0528933dd3f5f3	no	4
Warnings:					
Information:					
6	Application Data Sheet	P38683US_ADS.pdf	1502947 10738e9a0dc52ddad1f5813f8a5e60da8111ef9c	no	7
Warnings:					

Information:					
7	Fee Worksheet (SB06)	fee-info.pdf	38110 9d5fb2efcf2bae0827c259be6a31ad04602c0e9d	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	2833314	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

CAPPING DIELECTRIC STRUCTURE FOR TRANSISTOR GATES

BACKGROUND

Embodiments of the present description generally relate to the field of microelectronic device fabrication and, more particularly, to the fabrication of capping dielectric structures within non-planar transistor gates.

BRIEF DESCRIPTION OF THE DRAWINGS

The subject matter of the present disclosure is particularly pointed out and distinctly claimed in the concluding portion of the specification. The foregoing and other features of the present disclosure will become more fully apparent from the following description and appended claims, taken in conjunction with the accompanying drawings. It is understood that the accompanying drawings depict only several embodiments in accordance with the present disclosure and are, therefore, not to be considered limiting of its scope. The disclosure will be described with additional specificity and detail through use of the accompanying drawings, such that the advantages of the present disclosure can be more readily ascertained, in which:

FIG. 1 is a perspective view of a non-planar transistor, according to an embodiment of the present description.

FIG. 2 illustrates a side cross-sectional view of a non-planar transistor fin formed in or on a microelectronic substrate.

FIG. 3 illustrates a side cross-sectional view of a sacrificial material deposited over the non-planar transistor fin of FIG. 2, according to an embodiment of the present description.

FIG. 4 illustrates a side cross-sectional view of a trench formed in the sacrificial material deposited to expose a portion of the non-planar transistor fin of FIG. 3, according to an embodiment of the present description.

FIG. 5 illustrates a side cross-sectional view of a sacrificial gate formed in the trench of FIG. 4, according to an embodiment of the present description.

FIG. 6 illustrates a side cross-sectional view of the sacrificial gate after the removal of the sacrificial material of FIG. 5, according to an embodiment of the present description.

FIG. 7 illustrates a side cross-sectional view of a conformal dielectric layer deposited over the sacrificial gate and microelectronic substrate of FIG. 6, according to an embodiment of the present description.

FIG. 8 illustrates a side cross-sectional view of gate spacers formed from the conformal dielectric layer of FIG. 7, according to an embodiment of the present description.

FIG. 9 illustrates a side cross-sectional view of a source region and a drain region formed in the non-planar transistor fin on either side of the gate spacers of FIG. 8, according to an embodiment of the present description.

FIG. 10 illustrates a side cross-sectional view of a first dielectric material deposited over the gate spacers, the sacrificial gate, the non-planar transistor fin, and the microelectronic substrate of FIG. 9, according to an embodiment of the present description.

FIG. 11 illustrates a side cross-sectional view of the structure of FIG. 10 after planarizing the first dielectric material to expose a top surface of the sacrificial gate, according to an embodiment of the present description.

FIG. 12 illustrates a side cross-sectional view of the structure of FIG. 11 after the removal of the sacrificial gate to form a gate trench, according to an embodiment of the present description.

FIG. 13 illustrates a side cross-sectional view of the structure of FIG. 12 after the formation of a gate dielectric adjacent the non-planar transistor fin between the gate spacers, according to an embodiment of the present description.

FIG. 14 illustrates a side cross-sectional view of a conductive gate material deposited in the gate trench of FIG. 13, according to an embodiment of the present description.

FIG. 15 illustrates a side cross-sectional view of the structure of FIG. 14 after the removal of excess conductive gate material to form a non-planar transistor gate, according to an embodiment of the present description.

FIG. 16 illustrates a side cross-sectional view of the structure of FIG. 15 after etching away a portion of the non-planar transistor gate to form a recessed non-planar transistor gate, according to an embodiment of the present description.

FIG. 17 illustrates a side cross-sectional view of the structure of FIG. 16 after depositing a capping dielectric material into the recess resulting from the formation of the recessed non-planar transistor gate, according to an embodiment of the present description.

FIG 18 illustrates a flow diagram of a high density deposition process for the deposition of the capping dielectric material of FIG. 17, according to an embodiment of the present description.

FIG. 19 illustrates a side cross-sectional view of the structure of FIG. 17 after the removal of excess capping dielectric material to form a capping dielectric structure on the non-planar transistor gate, according to an embodiment of the present description.

FIG. 20 illustrates a side cross-sectional view of a second dielectric material deposited over the first dielectric material layer, the gate spacers, and the sacrificial gate top surface of FIG. 19, according to an embodiment of the present description.

FIG. 21 illustrates a side cross-sectional view of an etch mask patterned on the second dielectric material of FIG. 20, according to an embodiment of the present description.

FIG. 22 illustrates a side cross-sectional view of a contact opening formed through the first and second dielectric material layer of FIG. 21, according to an embodiment of the present description.

FIG. 23 illustrates a side cross-sectional view of the structure of FIG. 22 after the removal of the etch mask, according to an embodiment of the present description.

FIG. 24 illustrates a side cross-sectional view of a conductive contact material deposited in the contact opening of FIG. 23, according to an embodiment of the present description.

FIG. 25 illustrates a side cross-sectional view of the structure of FIG. 24 after the removal of the excess conductive contact material to form a source/drain contact, according to an embodiment of the present description.

DETAILED DESCRIPTION

In the following detailed description, reference is made to the accompanying drawings that show, by way of illustration, specific embodiments in which the claimed subject matter may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the subject matter. It is to be understood that the various embodiments, although different, are not necessarily mutually exclusive. For example, a particular feature, structure, or characteristic described herein, in connection with one embodiment, may be implemented within other embodiments without departing from the spirit and scope of the claimed subject matter. References within this specification to "one embodiment" or "an embodiment" mean that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one implementation encompassed within the present invention. Therefore, the use of the phrase "one embodiment" or "in an embodiment" does not necessarily refer to the same embodiment. In addition, it is to be understood that the location or arrangement of

individual elements within each disclosed embodiment may be modified without departing from the spirit and scope of the claimed subject matter. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the subject matter is defined only by the appended claims, appropriately interpreted, along with the full range of equivalents to which the appended claims are entitled. In the drawings, like numerals refer to the same or similar elements or functionality throughout the several views, and that elements depicted therein are not necessarily to scale with one another, rather individual elements may be enlarged or reduced in order to more easily comprehend the elements in the context of the present description.

In the fabrication of non-planar transistors, such as tri-gate transistors and FinFETs, non-planar semiconductor bodies may be used to form transistors capable of full depletion with very small gate lengths (e.g., less than about 30 nm). These semiconductor bodies are generally fin-shaped and are, thus, generally referred to as transistor "fins". For example in a tri-gate transistor, the transistor fins have a top surface and two opposing sidewalls formed on a bulk semiconductor substrate or a silicon-on-insulator substrate. A gate dielectric may be formed on the top surface and sidewalls of the semiconductor body and a gate electrode may be formed over the gate dielectric on the top surface of the semiconductor body and adjacent to the gate dielectric on the sidewalls of the semiconductor body. Thus, since the gate dielectric and the gate electrode are adjacent to three surfaces of the semiconductor body, three separate channels and gates are formed. As there are three separate channels formed, the semiconductor body can be fully depleted when the transistor is turned on. With regard to finFET transistors, the gate material and the electrode only contact the sidewalls of the semiconductor body, such that two separate channels are formed (rather than three in tri-gate transistors).

Embodiments of the present description relate to the formation of microelectronic transistors, wherein the transistor includes a recessed gate electrode capped by a substantially void-free dielectric capping dielectric structure which may be formed with a high density plasma process. Although embodiments herein are described in terms of non-planar transistors and replacement gate techniques, the subject matter is not so limited, as the subject matter may be used in planar transistors and in non-replacement gate applications.

FIG. 1 is a perspective view of a non-planar transistor 100, including at least one gate formed on at least one transistor fin, which are formed on a microelectronic substrate 102. In an embodiment of the present disclosure, the microelectronic substrate 102 may

be a monocrystalline silicon substrate. The microelectronic substrate 102 may also be other types of substrates, such as silicon-on-insulator ("SOI"), germanium, gallium arsenide, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, gallium antimonide, and the like, any of which may be combined with silicon.

The non-planar transistor, shown as a tri-gate transistor, may include at least one non-planar transistor fin 112. The non-planar transistor fin 112 may have a top surface 114 and a pair of laterally opposite sidewalls, sidewall 116 and opposing sidewall 118, respectively.

As further shown in FIG. 1, at least one non-planar transistor gate 122 may be formed over the non-planar transistor fin 112. The non-planar transistor gate 122 may be fabricated by forming a gate dielectric layer 124 on or adjacent to the non-planar transistor fin top surface 114 and on or adjacent to the non-planar transistor fin sidewall 116 and the opposing non-planar transistor fin sidewall 118. A gate electrode 126 may be formed on or adjacent the gate dielectric layer 124. In one embodiment of the present disclosure, the non-planar transistor fin 112 may run in a direction substantially perpendicular to the non-planar transistor gate 122.

The gate dielectric layer 124 may be formed from any well-known gate dielectric material, including but not limited to silicon dioxide (SiO_2), silicon oxynitride (SiO_xN_y), silicon nitride (Si_3N_4), and high-k dielectric materials such as hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate. The gate dielectric layer 124 can be formed by well-known techniques, such as by conformally depositing a gate dielectric material and then patterning the gate dielectric material with well-known photolithography and etching techniques, as will be understood to those skilled in the art.

The gate electrode 126 can be formed of any suitable gate electrode material. In an embodiment of the present disclosure, the gate electrode 126 may be formed from materials that include, but are not limited to, polysilicon, tungsten, ruthenium, palladium, platinum, cobalt, nickel, hafnium, zirconium, titanium, tantalum, aluminum, titanium carbide, zirconium carbide, tantalum carbide, hafnium carbide, aluminum carbide, other metal carbides, metal nitrides, and metal oxides. The gate electrode 126 can be formed by well-known techniques, such as by blanket depositing a gate electrode material and then

patterning the gate electrode material with well-known photolithography and etching techniques, as will be understood to those skilled in the art.

A source region and a drain region (not shown in FIG. 1) may be formed in the non-planar transistor fin 112 on opposite sides of the gate electrode 126. In one embodiment, the source and drain regions may be formed by doping the non-planar transistor fins 112, as will be understood to those skilled in the art. In another embodiment, the source and drain regions may be formed by removing potions of the non-planar transistor fins 112 and replacing these portions with appropriate material(s) to form the source and drain regions, as will be understood to those skilled in the art.

FIGs. 2-26 illustrate side cross-sectional view of one embodiment of fabricating a non-planar transistor, wherein FIGs. 2-5 are views along arrows A-A and B-B of FIG. 1, FIGs. 6-15 are views along arrows A-A of FIG. 1, and FIG. 16-26 are views along arrows C-C of FIG. 1.

As shown in FIG. 2, the non-planar transistor fin 112 may be formed by etching the microelectronic substrate 102 or by forming the non-planar transistor fin 112 on the microelectronic substrate 102 by any technique known in the art. As illustrate in FIG. 3, a sacrificial material 132 may be deposited over the non-planar transistor fin 112, as shown in FIG. 3, and a trench 134 may be formed in the sacrificial material 132 to expose a potion of the non-planar transistor fin 112, as shown in FIG. 4. The sacrificial material 132 may be any appropriate material known in the art, and the trench 134 may be formed by any technique known in the art, including but not limited to lithographic masking and etching.

As shown in FIG. 5, a sacrificial gate 136 may be formed in the trench 134 (see FIG. 4). The sacrificial gate 136 may be any appropriate material, such as a polysilicon material and the like, and may be deposited in the trench 134 (see FIG. 4) by any technique known in the art, including but not limited to chemical vapor deposition ("CVD") and physical vapor deposition ("PVD").

As shown in FIG. 6, the sacrificial material 132 of FIG. 5 may be removed to expose the sacrificial gate 136 by any technique known in the art, such as selectively etching the sacrificial material 132. As shown in FIG. 7, a conformal dielectric layer 142 may be deposited over the sacrificial gate 136 and microelectronic substrate 102. The conformal dielectric layer 142 may be any appropriate material, including but not limited to silicon nitride (Si_3N_4) and silicon carbide (SiC), and may be formed by any appropriate technique including but not limited to atomic layer deposition ("ALD").

As shown in FIG. 8, the conformal dielectric layer 142 of FIG. 7 may be etched, such as by directional etch with an appropriate etchant, to form a pair of gate spacers 144 on sidewalls 146 of the sacrificial gate 136, while substantially removing the conformal dielectric material layer 142 adjacent the microelectronic substrate 102 and a top surface 148 of the sacrificial gate 136. It is understood that fin spacers (not shown) may be simultaneously formed on sidewalls 116 and 118 (see FIG. 1) of the non-planar transistor fin 112 during the formation of the gate spacers 144.

As shown in FIG. 9, a source region 150a and a drain region 150b may be formed on either side of the gate spacers 144. In one embodiment, the source region 150a and the drain region 150b may be formed in the non-planar transistor fin 112 with the implantation of dopants. As will be understood to those skilled in that art, dopant implantation is a process of introducing impurities into semiconducting materials for the purpose changing its conductivity and electronic properties. This is generally achieved by ion implantation of either P-type ions (e.g. boron) or N-type ions (e.g. phosphorus), collectively referred to as "dopants". In another embodiment, portions of the non-planar transistor fin 112 may be removed by any technique known in the art, such as etching, and the source region 150a and a drain region 150b may be formed in place of the removed portions. The source region 150a and the drain region will hereinafter be referred to collectively as "source/drain region 150".

As shown in FIG. 10, a first dielectric material layer 152 may be deposited over the gate spacers 144, the sacrificial gate top surface 148, the non-planar transistor fin 112, and the microelectronic substrate 102. The first dielectric material layer 152 may be planarizing to expose the sacrificial gate top surface 148, as shown in FIG. 11. The planarization of the first dielectric material layer 152 may be achieved by any technique known in the art, including but not limited to chemical mechanical polishing (CMP).

As shown in FIG. 12, the sacrificial gate 136 of FIG. 11 may be removed to form a gate trench 154. The sacrificial gate 136 may be removed by any technique known in the art, such as a selective etch. As shown in FIG. 13, the gate dielectric layer 124, as also illustrated in FIG. 1, may be formed to abut the non-planar transistor fin 112, as previously discussed.

As shown in FIG. 14, a conductive gate material 156 may be deposited in the gate trench 154, and excess conductive gate material 156 (e.g. conductive gate material 156 not within the gate trench 154 of FIG. 12) may be removed to from the non-planar transistor gate electrode 126 (see also FIG. 1), as shown in FIG. 15. The materials and methods of

forming the gate electrode 126 have been previously discussed. The removal of the excess conductive gate material 156 may be achieved by any technique known in the art, including but not limited to chemical mechanical polishing (CMP), etching, and the like.

As shown in FIG. 16, a portion of the non-planar transistor gate electrode 126 may be removed to form a recess 158 and a recessed non-planar transistor gate 162. The removal may be accomplished by any known technique, including but not limited to wet or dry etching.

As shown in FIG. 17, a capping dielectric material 164 may be deposited to fill the recess 158 of FIG. 16. The capping dielectric material 164 may be any appropriate material, including but not limited to silicon nitride (Si_xN_y) and silicon carbide (Si_xC_y). However, known processes for depositing dielectrics, such as plasma enhanced chemical vapor deposition, may not be capable of filing recesses 158 that have high aspect ratios (height to width ratio) and may result in voids forming in the capping dielectric material 164. Such voids may result in contact-to-gate short circuits, as will be discussed. To prevent voids from forming, high temperature deposition techniques (e.g. greater than 400°C) may be employed. However, high temperature deposition may affect the work function of the non-planar transistor gate electrode 126, as will be understood by those skilled in the art. Furthermore, high temperature deposition may result in dopant movement or deactivation in the source/drain regions 150.

FIG. 18 is a flow diagram of a high density plasma (HDP) dielectric deposition process 200 for forming substantially void free capping dielectric material 164 (see FIG. 17) within a high aspect ratio recesses 158 (see FIG. 17). As defined in block 210, walls of a high density plasma chamber may be coated with a desired dielectric film, i.e. the dielectric to be deposited. As defined in block 220, a microelectronic substrate, such as a silicon wafer, may be placed on a chuck in the high density plasma chamber. In one embodiment, the chuck may be a water-cooled ceramic electrostatic chuck at room temperature, e.g. about 75°C. As defined in block 230, the high density plasma chamber may be pressurized with an inert gas, such as argon. In one embodiment, the high density plasma chamber may be pressure to a pressure greater than about 40 mTorr to strike a sustainable low power radio frequency (RF) plasma. As defined in block 240, RF electrodes within the high density plasma chamber may be powered up while introducing at least one reactive gas into the high density plasma chamber. In one embodiment, each of the RF electrodes, such as top and side electrodes, may be powered up to a range between about 2kV and 8kV for a time duration between about 30 and 60 seconds. The

reactive gas may include, but is not limited to oxygen, nitrogen, and the like. The microelectronic substrate temperature can be modulated between less than about 300°C and 600°C by adjusting the temperature of the chuck. It is understood that the time duration, microelectronic substrate temperature, RF power, and reactive gas mixture may be adjusted for a desired deposition result. As defined in block 250, the deposition gas may be introduced to the high density plasma chamber while powering a bias RF electrode. In one embodiment, a deposition gas comprising silane (SiH_4), nitrogen (N_2), argon (Ar), and helium (He) may be used to deposit a silicon nitride dielectric. In another embodiment, a deposition gas comprising silane (SiH_4), methane (CH_4), argon (Ar), and helium (He) may be used to deposit a silicon carbide dielectric. The RF electrode may be power to a range between about 3kV and 5kV with a bias RF electrode ranging from about 1kV and 3kV. The ratio of the nitrogen gas volume to the silane gas volume for silicon nitride deposition and ratio of the methane gas volume to the silane gas volume may be between about 0.5 and 9, depending on the desired properties of the dielectric layer, while the silane gas flow is kept between about 30 and 70 sccm. Under these conditions, the deposition rate may be in a range between about 7 to 30 Angstroms per second. It is understood that the deposition duration may be calculated based on the desired dielectric layer thickness and deposition rate. As defined in block 260, the deposition process is discontinued by discontinuing the introduction of deposition gas into the high density plasma deposition chamber and discontinuing power to the bias RF. The power to the RF electrodes may be ramped down and electrostatic charges are dissipated off of the microelectronic substrate, so that the microelectronic substrate can be removed from the electrostatic chuck. After removal the high density plasma chamber may be cleaned, such as by a remote plasma unit, and the walls of the high density plasma chamber may be recoated with a desired dielectric film.

The above-described process may result in simultaneous deposition and sputtering of the dielectric layer, wherein an appropriate deposition to sputtering ratio may result in a substantially void-free dielectric layer.

After deposition, the capping dielectric material 164 may be planarized to remove excess capping dielectric material 164 (e.g. capping dielectric material 164 not within the recess of FIG. 16) to form a capping dielectric structure 166 on the recessed non-planar transistor gate 162 and between a gate spacers 144, as shown in FIG. 19. The removal of the excess capping dielectric material 164 may be achieved by any technique known in the

art, including but not limited to chemical mechanical polishing (CMP), etching, and the like.

As shown in FIG. 20, a second dielectric material layer 168 may be deposited over the first dielectric material layer 152, the gate spacers 144, and the capping dielectric structure 166. The second dielectric material layer 168 may be formed from any appropriate dielectric material, including but not limited to silicon dioxide (SiO_2), silicon oxynitride (SiO_xN_y), and silicon nitride (Si_3N_4), by any known deposition technique. As shown in FIG. 21, an etch mask 172 may be patterned with at least one opening 174 on the second dielectric material layer 168, such as by well known lithographic techniques.

As shown in FIG. 22, a contact opening 182 may be formed through the first dielectric material layer 152 and the second dielectric material layer 168 by etching through the etch mask opening 174 of FIG. 21 to expose a portion of the source/drain region 150. The etch mask 172 of FIG. 22 may be removed thereafter, as shown in FIG. 23. In one embodiment, the first dielectric material layer 152 and the dielectric material layer 168 differs from dielectric material of both the gate spacers 144 and the capping dielectric structure 166, such that the etching of the first dielectric material layer 152 and the second dielectric layer 168 may be selective to the gate spacers 144 and the capping dielectric structure 166 (i.e. etches faster). This is known in the art as a self-aligning.

As shown in FIG. 24, a conductive contact material 188 may be deposited in the contact opening 182 of FIG. 23. The conductive contact material 188 may include, but is not limited to, polysilicon, tungsten, ruthenium, palladium, platinum, cobalt, nickel, hafnium, zirconium, titanium, tantalum, aluminum, titanium carbide, zirconium carbide, tantalum carbide, hafnium carbide, aluminum carbide, other metal carbides, metal nitrides, and metal oxides. It is understood that various adhesion layers, barrier layers, silicide layers, and/or conductive layers may be conformally disposed or formed in the contact opening 182 of FIG. 23 prior to the deposition of the conductive contact material 188.

As shown in FIG. 25, excess conductive contact material 188 of FIG. 24 (e.g. conductive contact material 188 not within the contact opening 182 of FIG. 12) may be removed to form a source/drain contact 190. The removal of the excess conductive contact material 188 may be achieved by any technique known in the art, including but not limited to chemical mechanical polishing (CMP), etching, and the like.

As previously discussed, in one embodiment, the first dielectric material layer 152 and the dielectric material layer 168 differs from dielectric material of both the gate

spacers 144 and the capping dielectric structure 166, such that the etching of the first dielectric material layer 152 and the second dielectric layer 168 may be selective to the gate spacers 144 and the capping dielectric structure 166 (i.e. etches faster). Thus, the recessed non-planar transistor 162 is protected during the formation of the contact opening 182. This allows for the formation of a relatively large sized source/drain contact 190, which may increase the transistor drive current performance, without the risk of shorting between the source/drain contact 190 and the recessed non-planar transistor gate 162. This is not possible if voids exist in the capping dielectric structure 144, as the voids would increase the likelihood of shorting between the source/drain contact 190 and the recessed non-planar transistor gate 162.

It is understood that the subject matter of the present description is not necessarily limited to specific applications illustrated in FIGs. 1-25. It is understood that although the illustrated embodiments are directed to non-planar applications, the subject matter may be applied to non-planar transistors and to non-replacement gate applications. Furthermore, the subject matter may be applied to other microelectronic device fabrication applications, as will be understood to those skilled in the art.

Having thus described in detail embodiments of the present invention, it is understood that the invention defined by the appended claims is not to be limited by particular details set forth in the above description, as many apparent variations thereof are possible without departing from the spirit or scope thereof.

CLAIMS

What is claimed is:

1. A transistor gate, comprising:

a pair of gate spacers

a recessed gate electrode disposed between the pair of gate spacers; and

a substantially void free capping dielectric structure disposed adjacent the recessed gate electrode and between the pair of gate spacers.

2. The transistor gate of claim 1, wherein the substantially void free capping dielectric structure comprises silicon nitride.

3. The transistor gate of claim 1, wherein the substantially void free capping dielectric structure comprises silicon carbide.

4. The transistor gate of claim 1, wherein the recessed gate electrode is a non-planar gate electrode.

5. A microelectronic device, comprising:

a non-planar transistor gate over a non-planar transistor fin, wherein the non-planar transistor gate comprises a gate electrode recessed between a pair of gate spacers and a substantially void free capping dielectric structure disposed on the recessed gate electrode between the gate spacers,

a source/drain region;

at least one dielectric material layer over the source/drain region, the non-planar transistor gate spacers, and the substantially void free capping dielectric structure; and

a source/drain contact extending through a portion of the at least one dielectric material layer to contact the source/drain region.

6. The microelectronic device of claim 5, wherein the substantially void free capping dielectric structure comprises silicon nitride.

7. The microelectronic device of claim 5, wherein the substantially void free capping dielectric structure comprises silicon carbide.

8. The microelectronic device of claim 5, wherein the source/drain contact abuts at least a portion of one non-planar transistor gate spacer.

9. The microelectronic device of claim 5, wherein the source/drain contact abuts at least a portion of the capping dielectric structure.

10. A method of fabricating a transistor gate, comprising:

forming a pair of gate spacers;

forming a gate electrode disposed between the pair of gate spacers; and

high density plasma depositing a capping dielectric structure on a top surface of the recessed gate electrode and between the pair of gate spacers.

11. The method of claim 10, wherein high density plasma depositing the capping dielectric structure comprises high density plasma depositing a silicon nitride capping dielectric structure.

12. The method of claim 10, wherein high density plasma depositing the capping dielectric structure comprises high density plasma depositing a silicon carbide capping dielectric structure.

13. The method of claim 10, wherein high density plasma depositing the capping dielectric structure comprises high density plasma depositing the capping dielectric structure at a temperature between about 300 °C and 600°C.

14. The method of claim 10, wherein forming the gate electrode comprises forming a non-planar gate electrode.

15. A method comprising:

forming a sacrificial non-planar transistor gate over a non-planar transistor fin;

depositing a dielectric material layer over the sacrificial non-planar transistor gate and the non-planar transistor fin;

forming non-planar transistor gate spacers from a portion of the dielectric material layer adjacent the sacrificial non-planar transistor gate;

forming a source/drain region;

removing the sacrificial non-planar transistor gate to form a gate trench between the non-planar transistor gate spacers and expose a portion of the non-planar transistor fin;

forming a gate dielectric adjacent the non-planar transistor fin within the gate trench;

depositing conductive gate material within the gate trench;

removing a portion of the conductive gate material to form a recess between the non-planar transistor gate spacers;

forming a capping dielectric structure within the recess by high density plasma depositing a dielectric material;

forming at least one dielectric material over the source/drain region, the non-planar transistor gate spacers, and the capping dielectric structure; and

forming a contact opening through the at least one dielectric material to expose at least a portion of the source/drain region.

16. The method of claim 15, wherein high density plasma depositing the capping dielectric structure comprises high density plasma depositing a silicon nitride capping dielectric structure.

17. The method of claim 15, wherein high density plasma depositing the capping dielectric structure comprises high density plasma depositing a silicon carbide capping dielectric structure.

18. The method of claim 15, wherein high density plasma depositing the capping dielectric structure comprises high density plasma depositing the capping dielectric structure at a temperature between about 300 °C and 600°C.

19. The method of claim 15, wherein forming a capping dielectric structure comprises:

high density plasma depositing capping dielectric material within the recess; and

removing excess capping dielectric material.

20. The method of claim 15, wherein forming a contact opening through the dielectric material to expose at least a portion of the source/drain region further comprises forming a contact opening through the dielectric material which exposes at least a portion of the source/drain region and at least a portion of one non-planar transistor gate spacer.

21. The method of claim 20, further comprising forming a source/drain contact to abut the exposed portion of the source/drain region and exposed portion of the non-planar transistor gate spacer.

22. The method of claim 15, wherein forming a contact opening through the dielectric material to expose at least a portion of the source/drain region further comprises forming a contact opening through the dielectric material which exposes at least a portion of the source/drain region and at least a portion of the capping dielectric structure.

23. The method of claim 22, further comprising forming a source/drain contact abuts the exposed portion of the source/drain region and the exposed portion of the capping dielectric structure.

24. The method of claim 15, wherein forming a contact opening through the dielectric material to expose at least a portion of the source/drain region further comprises forming a contact opening through the dielectric material exposes at least a portion of the source/drain region, at least a portion of the non-planar transistor gate spacer, and at least a portion of the capping dielectric structure.

25. The method of claim 24, further comprising forming a source/drain contact to abut the exposed portion of the source/drain region, the exposed portion of non-planar gate spacer, and the exposed portion of the capping dielectric structure.

ABSTRACT OF THE DISCLOSURE

The present description relates to the field of fabricating microelectronic transistors, including non-planar transistors, for microelectronic devices. Embodiments of the present description relate to the formation a recessed gate electrode capped by a substantially void-free dielectric capping dielectric structure which may be formed with a high density plasma process.

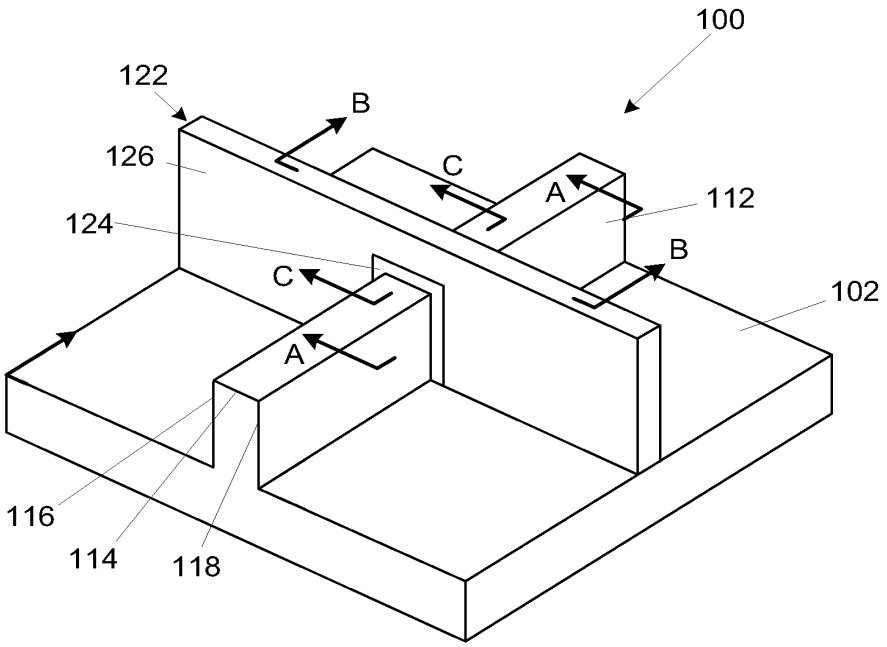


FIG. 1

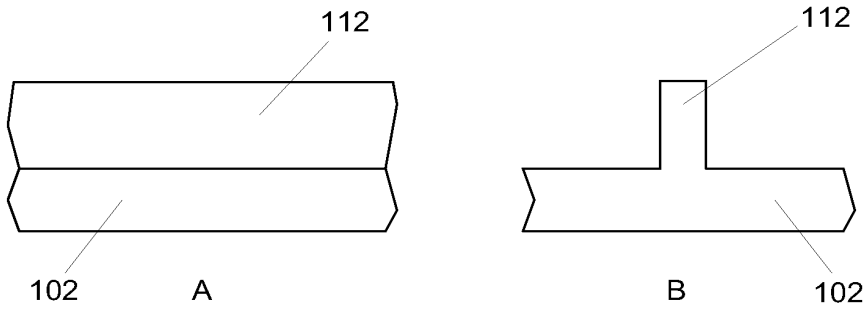


FIG. 2

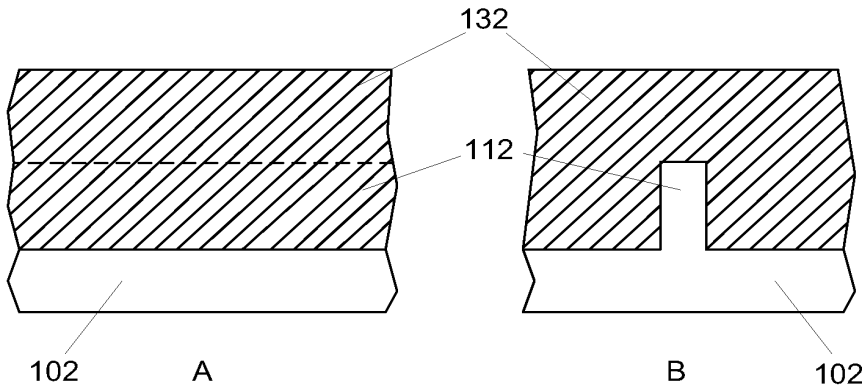


FIG. 3

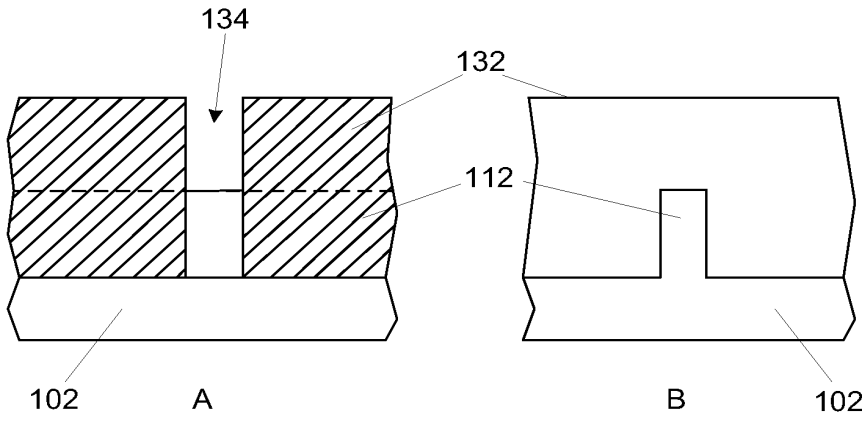


FIG. 4

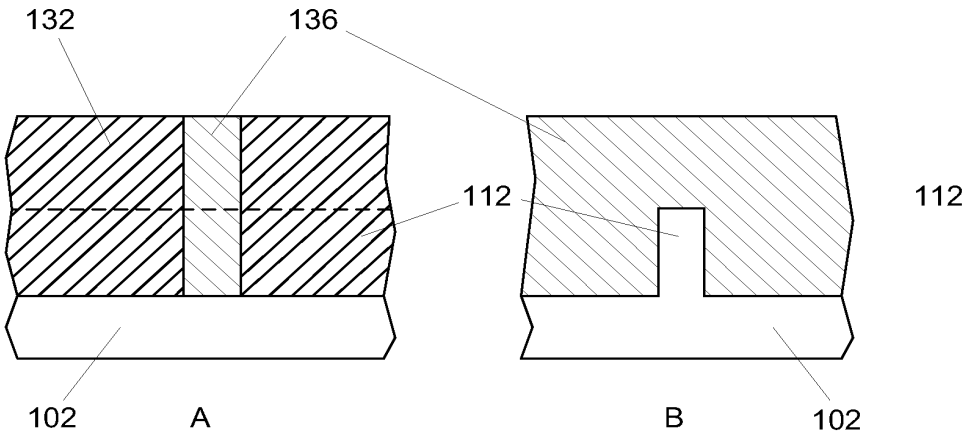


FIG. 5

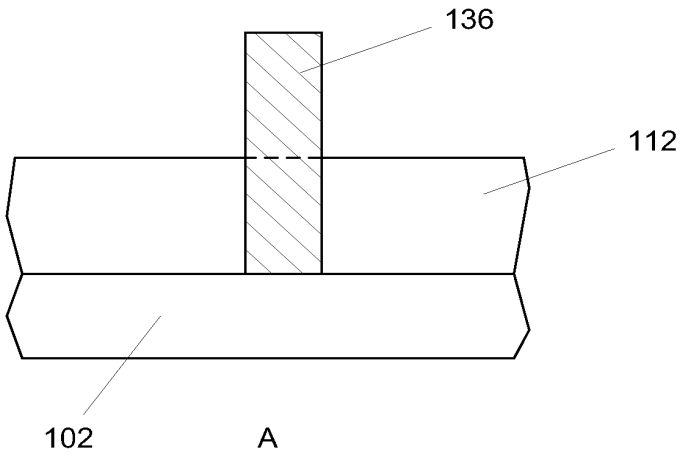


FIG. 6

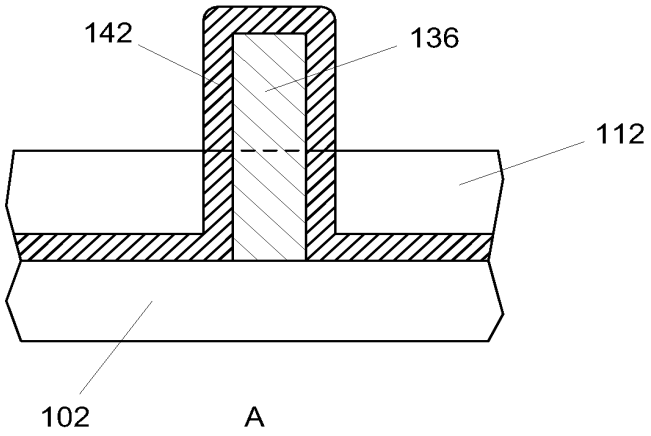


FIG. 7

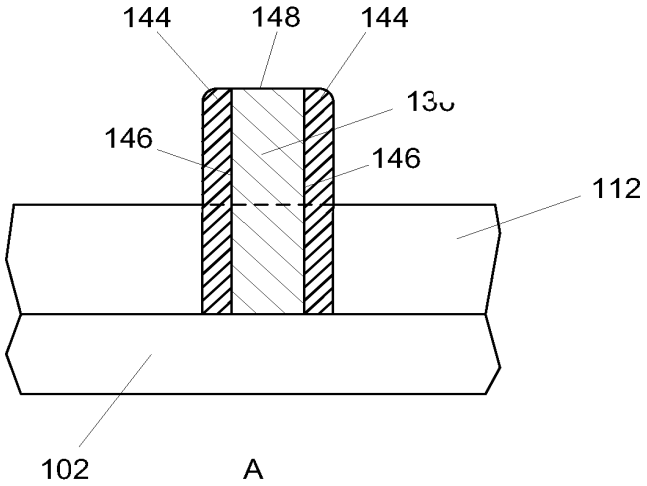


FIG. 8

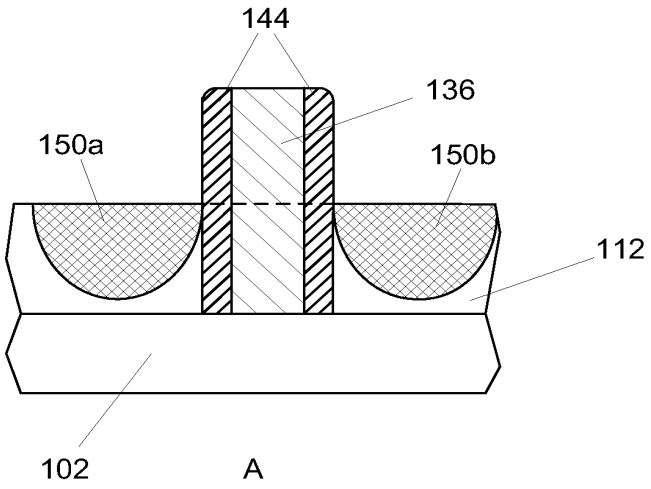


FIG. 9

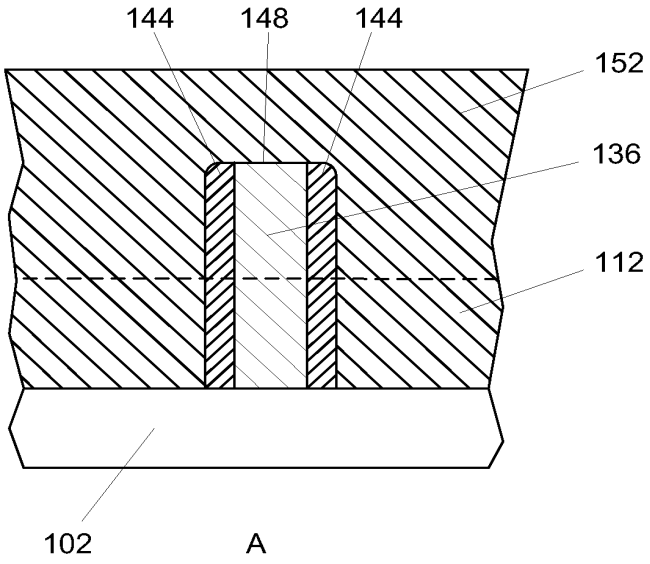


FIG. 10

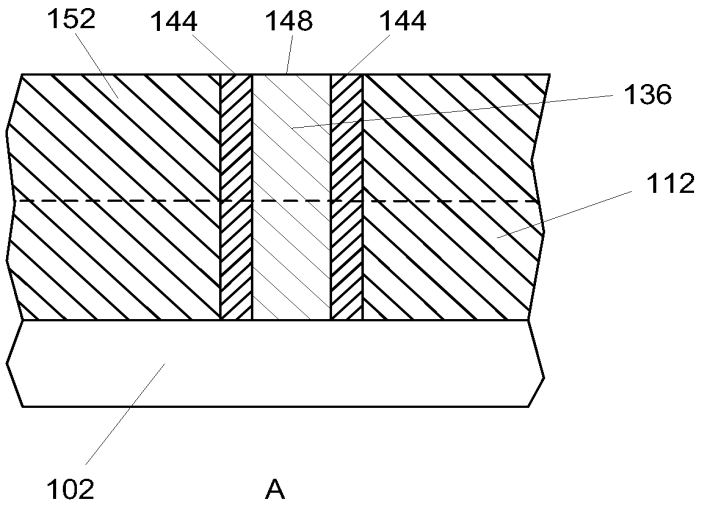


FIG. 11

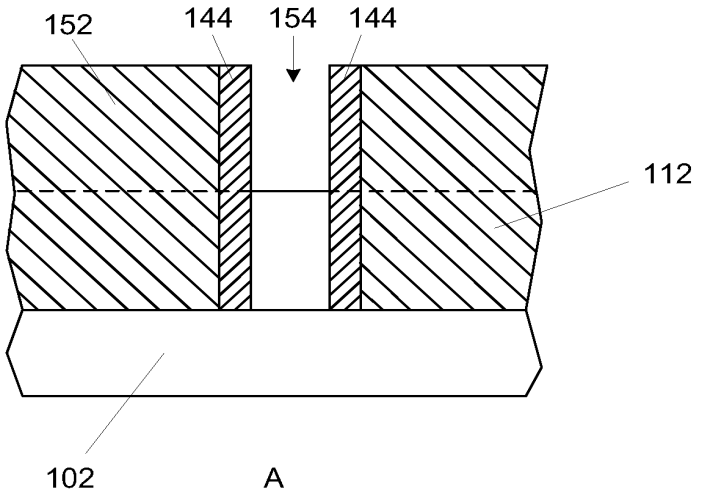


FIG. 12

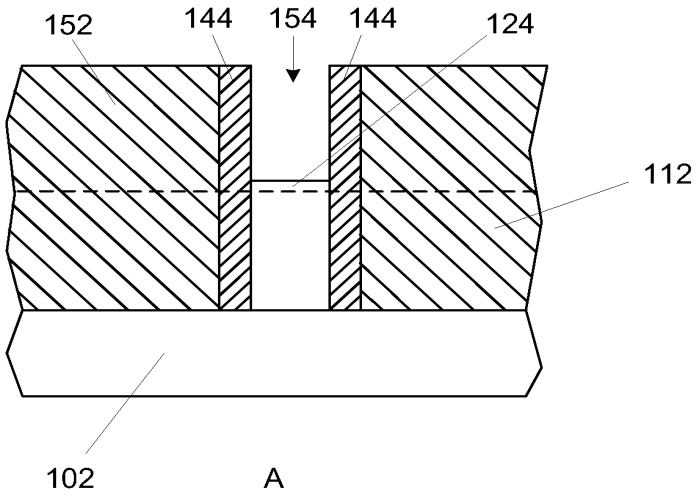


FIG. 13

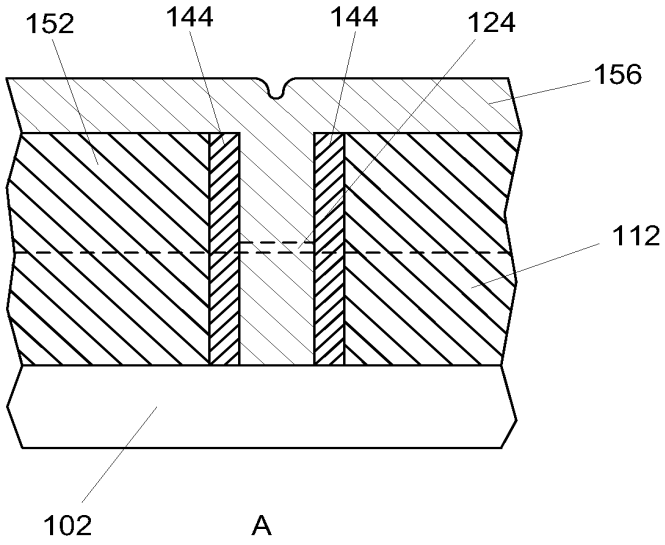


FIG. 14

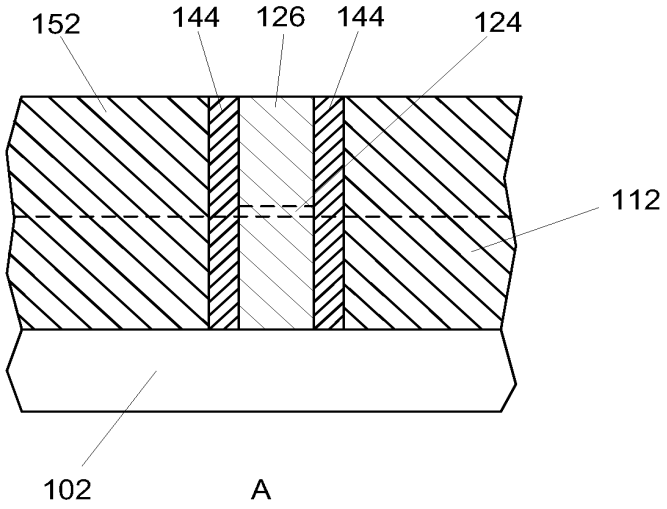

152
144
126
144
124
112
102
A

FIG. 15

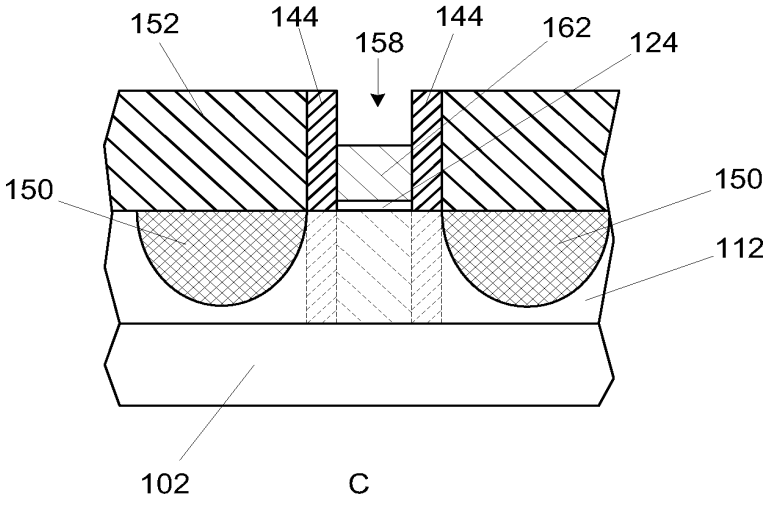

152
144
158
144
162
124
150
150
112
102
C

FIG. 16

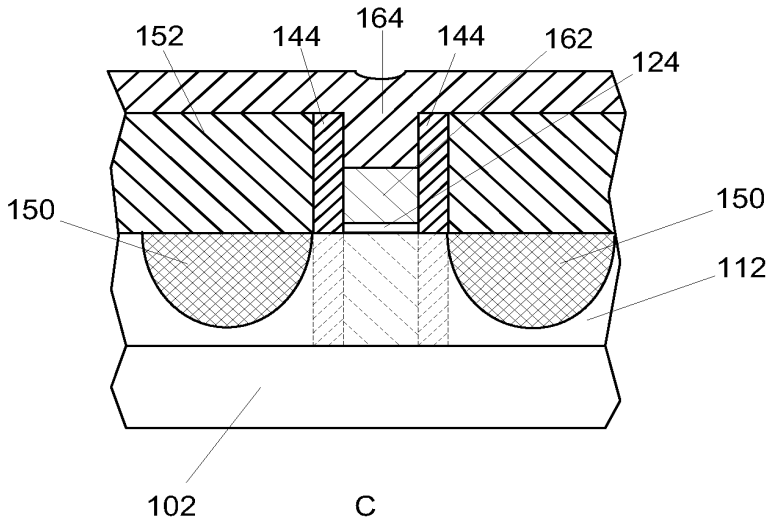

152
144
164
144
162
124
150
150
112
102
C

FIG. 17

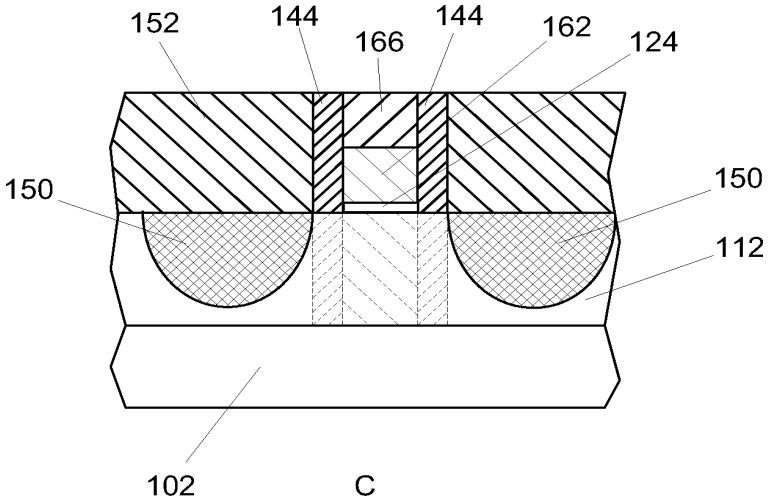

152
144
166
144
162
124
150
150
112
102
C

FIG. 19

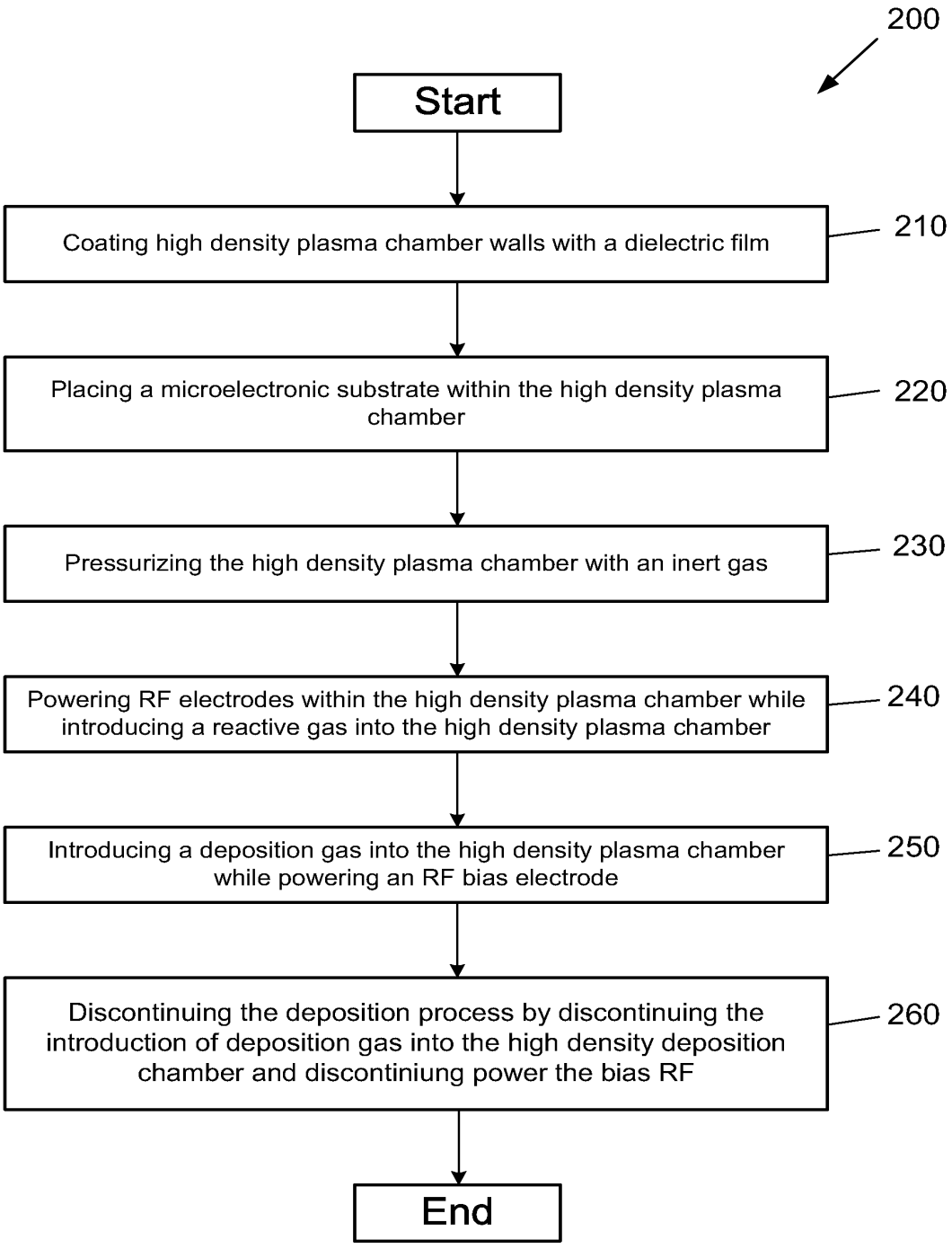

200
Start
Coating high density plasma chamber walls with a dielectric film
210
Placing a microelectronic substrate within the high density plasma chamber
220
Pressurizing the high density plasma chamber with an inert gas
230
Powering RF electrodes within the high density plasma chamber while introducing a reactive gas into the high density plasma chamber
240
Introducing a deposition gas into the high density plasma chamber while powering an RF bias electrode
250
Discontinuing the deposition process by discontinuing the introduction of deposition gas into the high density deposition chamber and discontiniung power the bias RF
260
End

FIG. 18

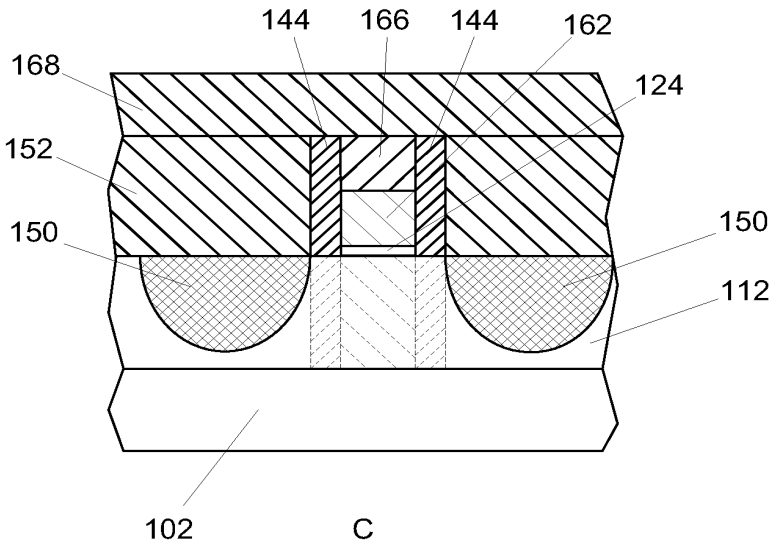

144
166
144
162
168
124
152
150
150
112
102
C

FIG. 20

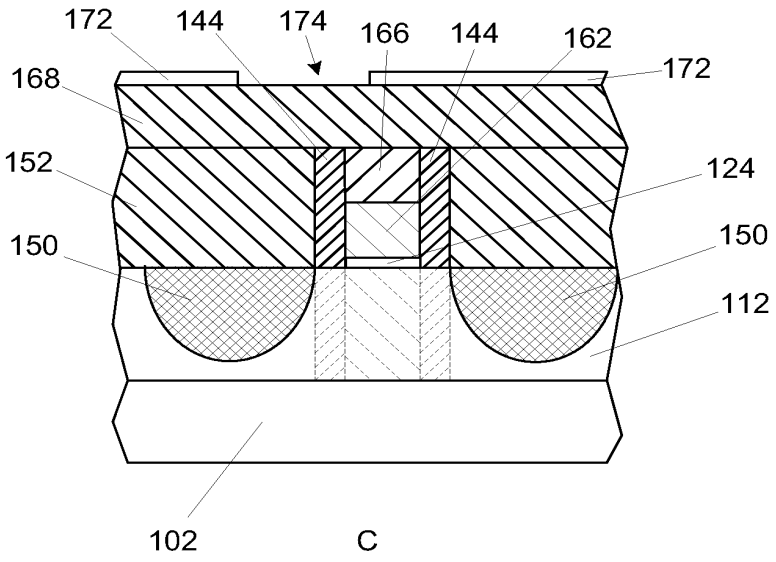

172
144
174
166
144
162
172
168
152
124
150
150
112
102
C

FIG. 21

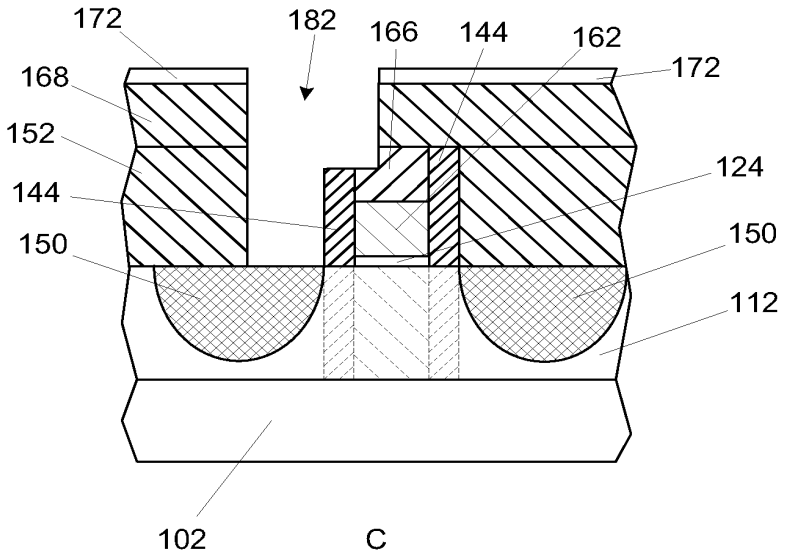

172
182
166
144
162
172
168
152
124
144
150
150
112
102
C

FIG. 22

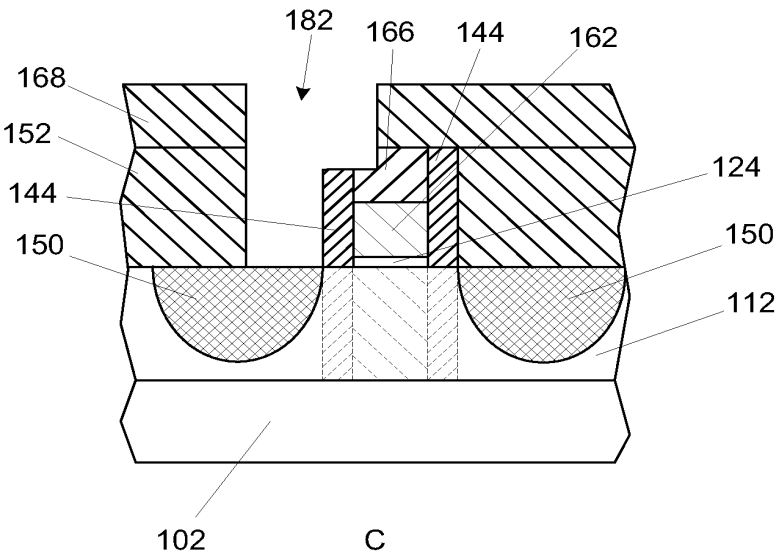

182
166
144
162
168
152
124
144
150
150
112
102
C

FIG. 23

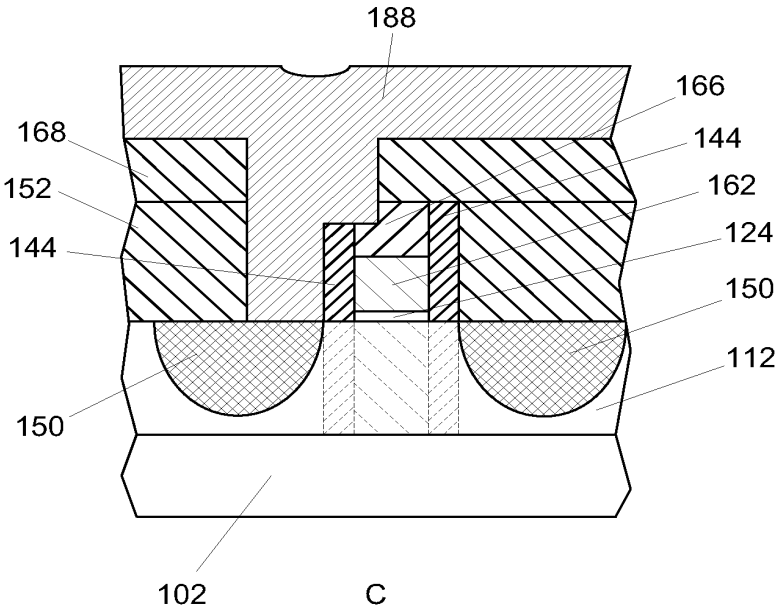

188
166
168
144
152
162
144
124
150
150
112
150
102
C

FIG. 24

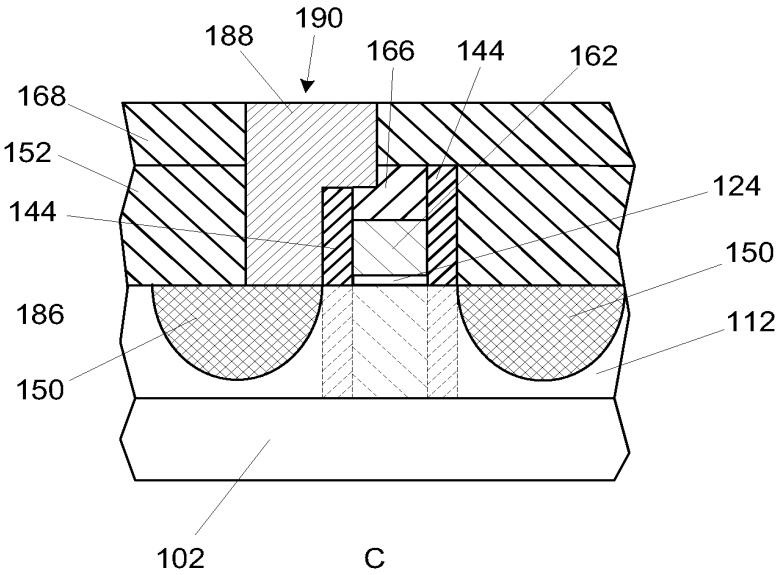

190
188
166
144
162
168
152
124
144
150
186
112
150
102
C

FIG. 25

Docket No.: P38683PCT
PATENT

Declaration of inventorship (Rules 4.17(iv) and 51*bis*.1(a)(iv)) for the purposes of the designation of the United States of America:

I hereby declare that I believe I am the original, first and sole (if only one inventor is listed below) or joint (if more than one inventor is listed below) inventor of the subject matter which is claimed and for which a patent is sought.

This declaration is directed to the international application of which it forms a part (if filing declaration with application).

This declaration is directed to international application No. PCT/US11/54464..... (if furnishing declaration pursuant to Rule 26*ter*).

I hereby declare that my residence, mailing address, and citizenship are as stated next to my name.

I hereby state that I have reviewed and understand the contents of the above-identified international application, including the claims of said application. I have identified in the request of said application, in compliance with PCT Rule 4.10, any claim to foreign priority, and I have identified below, under the heading "Prior Applications," by application number, country or Member of the World Trade Organization, day, month and year of filing, any application for a patent or inventor's certificate filed in a country other than the United States of America, including any PCT international application designating at least one country other than the United States of America, having a filing date before that of the application on which foreign priority is claimed.

Prior Applications: .....
.....

I hereby acknowledge the duty to disclose information that is known by me to be material to patentability as defined by 37 C.F.R. § 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the PCT international filing date of the continuation-in-part application.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Name: Aaron W. Rosenbaum

Residence: Portland, OR
(city and either US state, if applicable, or country)

Mailing Address: 5530 Nw Osprey Place, Portland, OR, US 97229

Citizenship: US

Inventor's Signature: ..... Date: 9/27/11.....
(The signature must be that of the inventor, not that of the agent)

Name: Din-How Mei

Residence: Portland, OR
(city and either US state, if applicable, or country)

Mailing Address: 5366 NW 132nd Ave, Portland, OR, US 97229

Citizenship: US

Inventor's Signature: ..... **Date:** 9/27/11
(The signature must be that of the inventor, not that of the agent)

Name: Sameer S. Pradhan

Residence: Portland, OR
(city and either US state, if applicable, or country)

Mailing Address: 17923 NW Sylvania Lane, Portland, OR, US 97229

Citizenship: India

Inventor's Signature: Sameer Pradhan **Date:** 9/27/11
(The signature must be that of the inventor, not that of the agent)

☐ This declaration is continued on the following sheet, "Continuation of Box No. VIII (iv)".

PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

Entered into FIP
By: M.T.

To:

BLAKELY SOKOLOFF TAYLOR&AZFMAN LLP

1279 OAKMEAD PARKWAY SUNNYVALE, CA 94086 USA

ENTERED

MAY 22 2012 M.T.

INTO DATABASE

RECEIVED
SUNNYVALE
MAY 21 2012
BLAKELY SOKOLOFF TAYLOR ZAFMAN

PCT

NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL SEARCH REPORT AND THE WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY, OR THE DECLARATION

(PCT Rule 44.1)

Applicant's or agent's file reference P38683PCT	Date of mailing *(day/month/year)* 15 MAY 2012 (15.05.2012)
	FOR FURTHER ACTION See paragraphs 1 and 4 below
International application No. **PCT/US2011/054464**	International filing date *(day/month/year)* **30 SEPTEMBER 2011 (30.09.2011)**

Applicant

INTEL CORPORATION et al

1. ☒ The applicant is hereby notified that the international search report and the written opinion of the International Searching Authority have been established and are transmitted herewith.

   Filing of amendments and statement under Article 19:

   The applicant is entitled, if he so wishes, to amend the claims of the international application (see Rule 46):

   When? The time limit for filing such amendments is normally two months from the date of transmittal of the international search report.

   Where? Directly to the International Bureau of WIPO, 34 chemin des Colombettes 1211 Geneva 20, Switzerland, Facsimile No.: +41 22 338 82 70

   For more detailed instructions, see *PCT Applicant's Guide*, International Phase, paragraphs 9.004 . 9.011.

2. ☐ The applicant is hereby notified that no international search report will be established and that the declaration under Article 17(2)(a) to that effect and the written opinion of the International Searching Authority are transmitted herewith.

3. ☐ **With regard to any protest** against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that:

   ☐ the protest together with the decision thereon has been transmitted to the International Bureau together with any request to forward the texts of both the protest and the decision thereon to the designated Offices.

   ☐ no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.

4. **Reminders**

The applicant may submit comments on an informal basis on the written opinion of the International Searching Authority to the International Bureau. The International Bureau will send a copy of such comments to all designated Offices unless an international preliminary examination report has been or is to be established. Following the expiration of 30 months from the priority date, these comments will also be made available to the public.

Shortly after the expiration of **18 months** from the priority date, the international application will be published by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau before the completion of the technical preparations for international publication (Rules 90bis.1 and 90bis.3).

Within **19 months** from the priority date, but only in respect of some designated Offices, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase **until 30 months** from the priority date (in some Offices even later); otherwise, the applicant must, **within 20 months** from the priority date, perform the prescribed acts for entry into the national phase before those designated Offices.

In respect of other designated Offices, the time limit of **30 months** (or later) will apply even if no demand is filed within 19months.

For details about the applicable time limits, Office by Office, see www.wipo.int/pct/en/texts/time_limits.html and the PCT Applicant's Guide, National Chapters.

Name and mailing address of the ISA/KR Korean Intellectual Property Office Government Complex-Daejeon, 189 Cheongsa-ro, Seo-gu, Daejeon 302-701, Republic of Korea	Authorized officer COMMISSIONER
Facsimile No. 82-42-472-7140	Telephone No. 82-42-481-8755

CPA GLOBAL
JUN 04 2012
RECEIVED
Coded _____ Verified _____

Form PCT/ISA/220 (July 2010)

* Attention

Copies of the documents cited in the international search report can be searched in the following Korean Intellectual Property Office English website for three months from the date of mailing of the international search report.

http://www.kipo.go.kr/en/ => PCT Services => PCT Services

ID : PCT international application number
PW : **XF2JQG6C**

Inquiries related to PCT International Search Report or Written Opinion prepared by KIPO as an International Searching Authority can be answered not only by KIPO but also through IPKC (Intellectual Property Korea Center), located in Vienna, VA, which functions as a PCT Help Desk for PCT applicants.

Homepage: http://www.ipkcenter.com
Email: ipkc@ipkcenter.com
Phone: +1 703 388 1066
Fax: +1 703 388 1084

Notes to Form PCT/ISA/220 (July 2010)

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference	FOR FURTHER ACTION	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
P38683PCT		
International application No.	International filing date *(day/month/year)*	(Earliest) Priority Date *(day/month/year)*
PCT/US2011/054464	**30 SEPTEMBER 2011 (30.09.2011)**	

Applicant

INTEL CORPORATION et al

This International search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 3 sheets.

☐ It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**
   a. With regard to the **language**, the international search was carried out on the basis of:
      ☒ the international application in the language in which it was filed
      ☐ a translation of the international application into _____, which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))
   b. ☐ This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6*bis*(a)).
   c. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.
2. ☐ **Certain claims were found unsearchable** (See Box No. II)
3. ☐ **Unity of invention is lacking** (See Box No. III)
4. With regard to the **title,**
   ☒ the text is approved as submitted by the applicant.
   ☐ the text has been established by this Authority to read as follows:
5. With regard to the **abstract,**
   ☒ the text is approved as submitted by the applicant.
   ☐ the text has been established, according to Rule 38.2, by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.
6. With regard to the drawings,
   a. the figure of the **drawings** to be published with the abstract is Figure No. 1
      ☒ as suggested by the applicant.
      ☐ as selected by this Authority, because the applicant failed to suggest a figure.
      ☐ as selected by this Authority, because this figure better characterizes the invention.
   b. ☐ none of the figure is to be published with the abstract.

Form PCT/ISA/210 (first sheet) (July 2009)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2011/054464

A. CLASSIFICATION OF SUBJECT MATTER

H01L 29/78(2006.01)i, H01L 21/336(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 29/78; H01L 21/336; H01L 21/306; H01L 21/28; H01L 21/335

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: capping, dielectric, and transistor

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2008-0233699 A1 (BOOTH ROGER ALLEN et al.) 25 September 2008 See the abstract; figs. 1-11; paragraphs [0016]-[0036].	1-25
A	US 2010-0048007 A1 (LEE SHEN-NAN et al.) 25 February 2010 See the abstract; figs. 1-3; paragraphs [0011]-[0039].	1-25
A	KR 10-0653711 B1 (SAMSUNG ELECTRONICS CO., LTD.) 05 December 2006 See the abstract; figs. 1-12; claims 1-23.	1-25

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15 MAY 2012 (15.05.2012)	**15 MAY 2012 (15.05.2012)**

Name and mailing address of the ISA/KR

Korean Intellectual Property Office
Government Complex-Daejeon, 189 Cheongsa-ro,
Seo-gu, Daejeon 302-701, Republic of Korea

Facsimile No. 82-42-472-7140

Authorized officer

Lee,Sang Ho

Telephone No. 82-42-481-8221

Form PCT/ISA/210 (second sheet) (July 2009)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2011/054464

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2008-0233699 A1	25.09.2008	CN 101097956 A	02.01.2008
		CN 101097956 C0	02.01.2008
		JP 2008-010876 A	17.01.2008
		TW 200807717 A	01.02.2008
		US 2008-0001187 A1	03.01.2008
		US 2008-0042219 A1	21.02.2008
		US 2008-0142891 A1	19.06.2008
		US 7517764 B2	14.04.2009
		US 7667248 B2	23.02.2010
		US 7863122 B2	04.01.2011
US 2010-0048007 A1	25.02.2010	CN 101659034 A	03.03.2010
		CN 101659034 B	09.11.2011
		TW 201009925 A	01.03.2010
		US 8153526 B2	10.04.2012
KR 10-0653711 B1	05.12.2006	US 2007-0111435 A1	17.05.2007
		US 2010-0197099 A1	05.08.2010
		US 7723762 B2	25.05.2010
		US 7851287 B2	14.12.2010

Form PCT/ISA/210 (patent family annex) (July 2009)

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:
BLAKELY SOKOLOFF TAYLOR&AZFMAN LLP

1279 OAKMEAD PARKWAY SUNNYVALE, CA 94086
USA

PCT

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43bis.1)

Date of mailing *(day/month/year)*	**15 MAY 2012 (15.05.2012)**
Applicant's or agent's file reference P38683PCT	**FOR FURTHER ACTION** See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US2011/054464	**30 SEPTEMBER 2011 (30.09.2011)**	

International Patent Classification (IPC) or both national classification and IPC

H01L 29/78(2006.01)i, H01L 21/336(2006.01)i

ENTERED
MAY 22 2012 M.T.
Entered into FIP
By: M.T.
INTO DATABASE

Applicant

INTEL CORPORATION et al

1. This opinion contains indications relating to the following items:

- [X] Box No. I Basis of the opinion
- [ ] Box No. II Priority
- [ ] Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- [ ] Box No. IV Lack of unity of invention
- [X] Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- [ ] Box No. VI Certain documents cited
- [ ] Box No. VII Certain defects in the international application
- [ ] Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1bis(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.
For further options, see Form PCT/ISA/220.

Name and mailing address of the ISA/KR	Date of completion of this opinion	Authorized officer
Korean Intellectual Property Office Government Complex-Daejeon, 189 Cheongsa-ro, Seo-gu, Daejeon 302-701, Republic of Korea Facsimile No. 82-42-472-7140	15 MAY 2012 (15.05.2012)	Lee,Sang Ho Telephone No.82-42-481-8221

Form PCT/ISA/237 (cover sheet) (July 2011)

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2011/054464

Box No. I Basis of this opinion

1. With regard to the **language**, this opinion has been established on the basis of:

   ☒ the international application in the language in which it was filed

   ☐ a translation of the international application into _____, which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(a))

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of:

   a. a sequence listing filed or furnished
      ☐ on paper
      ☐ in electronic form

   b. time of filing or furnishing
      ☐ contained in the international application as filed.
      ☐ filed together with the international application in electronic form.
      ☐ furnished subsequently to this Authority for the purposes of search.

4. ☐ In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additioanl copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2011/054464

Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Claims	1-25	YES
	Claims	NONE	NO
Inventive step (IS)	Claims	1-25	YES
	Claims	NONE	NO
Industrial applicability (IA)	Claims	1-25	YES
	Claims	NONE	NO

2. Citations and explanations :

Reference is made to the following documents:

D1: US 2008-0233699 A1 (BOOTH ROGER ALLEN et al.) 25 September 2008
D2: US 2010-0048007 A1 (LEE SHEN-NAN et al.) 25 February 2010
D3: KR 10-0653711 B1 (SAMSUNG ELECTRONICS CO., LTD.) 05 December 2006

1. Novelty and Inventive Step

1.1 claims 1-4
The subject matter of claim 1 differs from the disclosure of D1 in that the transistor gate comprises a substantially void free capping dielectric structure disposed adjacent the recessed gate electrode and between the pair of gate spacers. As the subject matter of claim 1 is not shown in any other prior art documents cited in the ISR, claim 1 is not anticipated by any of the prior art documents including D1, nor obvious to the person skilled in the art.
Therefore, claim 1 is novel and involves an inventive step under PCT Article 33(2) and (3).

Claims 2-4 which are dependent on claim 1 also meet the requirements of PCT Article 33(2)-(3) with respect to novelty and inventive step.

1.2 claims 5-9
The subject matter of claim 5 differs from the disclosure of D1 in that the microelectronic device comprises at least one dielectric material layer over the source/drain region, the non-planar transistor gate spacers, and the substantially void free capping dielectric structure. As the subject matter of claim 5 is not shown in any other prior art documents cited in the ISR, claim 5 is not anticipated by any of the prior art documents including D1, nor obvious to the person skilled in the art.
Therefore, claim 5 is novel and involves an inventive step under PCT Article 33(2) and (3).

Claims 6-9 which are dependent on claim 5 also meet the requirements of PCT Article 33(2)-(3) with respect to novelty and inventive step.

1.3 claims 10-14
The method of fabricating a transistor gate of claim 10 differs from the disclosure of D1 in that the third step in the method of claim 10 comprises high density plasma depositing a capping dielectric structure on a top surface of the recessed gate electrode and between the pair of gate spacers. As the subject matter of claim 10 is not shown in any other prior art documents cited in the ISR, claim 10 is not anticipated by any of the prior art documents including D1, nor obvious to the person skilled in the art.
Therefore, claim 10 is novel and involves an inventive step under PCT Article 33(2) and (3).

Claims 11-14 which are dependent on claim 10 also meet the requirements of PCT Article 33(2)-(3) with respect to novelty and inventive step.

(Continued on the Supplemental Box.)

Supplemental Box

In case **the space in any of the preceding boxes is not sufficient.**
Continuation of:

Box V.

1.4 claims 15-25
The method of claim 15 differs from the disclosure of D1 in that the ninth step in the method of claim 15 forms a capping dielectric structure within the recess by high density plasma depositing a dielectric material. As the subject matter of claim 15 is not shown in any other prior art documents cited in the ISR, claim 15 is not anticipated by any of the prior art documents including D1, nor obvious to the person skilled in the art.
Therefore, claim 15 is novel and involves an inventive step under PCT Article 33(2) and (3).

Claims 16-25 which are dependent on claim 15 also meet the requirements of PCT Article 33(2)-(3) with respect to novelty and inventive step.

2. Industrial Applicability
Claims 1-25 have industrial applicability (PCT Article 33(4)).

Declaration of inventorship (Rules 4.17(iv) and 51*bis*.1(a)(iv))
for the purposes of the designation of the United States of America:

I hereby declare that I believe I am the original, first and sole (if only one inventor is listed below) or joint (if more than one inventor is listed below) inventor of the subject matter which is claimed and for which a patent is sought.

This declaration is directed to the international application of which it forms a part (if filing declaration with application).

This declaration is directed to international application No. PCT/US11/54464..... (if furnishing declaration pursuant to Rule 26*ter*).

I hereby declare that my residence, mailing address, and citizenship are as stated next to my name.

I hereby state that I have reviewed and understand the contents of the above-identified international application, including the claims of said application. I have identified in the request of said application, in compliance with PCT Rule 4.10, any claim to foreign priority, and I have identified below, under the heading "Prior Applications," by application number, country or Member of the World Trade Organization, day, month and year of filing, any application for a patent or inventor's certificate filed in a country other than the United States of America, including any PCT international application designating at least one country other than the United States of America, having a filing date before that of the application on which foreign priority is claimed.

Prior Applications: .....
.....

I hereby acknowledge the duty to disclose information that is known by me to be material to patentability as defined by 37 C.F.R. § 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the PCT international filing date of the continuation-in-part application.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Name: Aaron W. Rosenbaum

Residence: Portland, OR
(city and either US state, if applicable, or country)

Mailing Address: 5530 Nw Osprey Place, Portland, OR, US 97229

Citizenship: US

Inventor's Signature: ..... Date: 9/27/11.....
(The signature must be that of the inventor, not that of the agent)

Name: Din-How Mei

Residence: Portland, OR
(city and either US state, if applicable, or country)

Mailing Address: 5366 NW 132nd Ave, Portland, OR, US 97229

Citizenship: US

Inventor's Signature: ..... **Date**: 9/27/11
(The signature must be that of the inventor, not that of the agent)

Name: Sameer S. Pradhan

Residence: Portland, OR
(city and either US state, if applicable, or country)

Mailing Address: 17923 NW Sylvania Lane, Portland, OR, US 97229

Citizenship: India

Inventor's Signature: Sameer Pradhan **Date**: 9/27/11
(The signature must be that of the inventor, not that of the agent)

☐ This declaration is continued on the following sheet, "Continuation of Box No. VIII (iv)".

From the INTERNATIONAL BUREAU

PCT

NOTIFICATION OF THE RECORDING OF A CHANGE

(PCT Rule 92*bis*.1 and Administrative Instructions, Section 422)

To:

BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP
1279 Oakmead Parkway
Sunnyvale, CA 94086
ETATS-UNIS D'AMERIQUE

Date of mailing *(day/month/year)*
30 November 2011 (30.11.2011)

Applicant's or agent's file reference
P38683PCT

IMPORTANT NOTIFICATION

International application No.
PCT/US2011/054464

International filing date *(day/month/year)*
30 September 2011 (30.09.2011)

1. The following indications appeared on record concerning:

☐ the applicant ☐ the inventor ☒ the agent ☐ the common representative

Name and Address
WINKLE, Robert G.
Winkle, PLLC
c/o CPA GLOBAL
P.O. Box 52050
Minneapolis, MN 55402
United States of America

State of Nationality | State of Residence

Telephone No.

Facsimile No.

E-mail address

2. The International Bureau hereby notifies the applicant that the following change has been recorded concerning:

☒ the person ☐ the name ☐ the address ☐ the nationality ☐ the residence

Name and Address
BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP
1279 Oakmead Parkway
Sunnyvale, CA 94086
United States of America

State of Nationality | State of Residence

Telephone No.

Facsimile No.

E-mail address
☐ Notifications by e-mail authorized

3. Further observations, if necessary:

4. A copy of this notification has been sent to:

☒ the receiving Office
☒ the International Searching Authority
☐ the Authority(ies) specified for supplementary search
☐ the International Preliminary Examining Authority
☐ the designated Offices concerned
☐ the elected Offices concerned
☐ other:

The International Bureau of WIPO
34, chemin des Colombettes
1211 Geneva 20, Switzerland

Facsimile No. +41 22 338 71 30

Authorized officer
Ben-Mansour Naceur
e-mail pt09.pct@wipo.int
Telephone No. +41 22 338 74 09

Form PCT/IB/306 (January 2009) 1/JEP64A4LPEKYT0

PCT REQUEST

Original (for **SUBMISSION**)

0	**For receiving Office use only**	
0-1	International Application No.	PCT/US11/54464
0-2	International Filing Date	30 SEP 2011 (30.09.11)
0-3	Name of receiving Office and "PCT International Application"	PCT INTERNATIONAL APPLICATION RO/US

0-4	**Form PCT/RO/101 PCT Request**	
0-4-1	Prepared Using	PCT-SAFE [EASY/EFS-Web mode] Version 3.51.050.226 MT/FOP 20110701/0.20.5.19
0-5	**Petition** The undersigned requests that the present international application be processed according to the Patent Cooperation Treaty	
0-6	**Receiving Office (specified by the applicant)**	United States Patent and Trademark Office (USPTO) (RO/US)
0-7	**Applicant's or agent's file reference**	P38683PCT
I	**Title of Invention**	CAPPING DIELECTRIC STRUCTURE FOR TRANSISTOR GATES
II	**Applicant**	
II-1	This person is	Applicant only
II-2	Applicant for	All designated States except US
II-4	Name	INTEL CORPORATION
II-5	Address	2200 Mission College Boulevard Santa Clara, California 95052 United States of America
II-6	State of nationality	US
II-7	State of residence	US
II-8	Telephone No.	480-948-3745
II-9	Facsimile No.	480-948-3766
III-1	**Applicant and/or inventor**	
III-1-1	This person is	Applicant and inventor
III-1-2	Applicant for	US only
III-1-4	Name (LAST, First)	ROSENBAUM, Aaron W.
III-1-5	Address	5530 NW Osprey Place Portland, Oregon 97229 United States of America
III-1-6	State of nationality	US
III-1-7	State of residence	US

PCT REQUEST

Original (for **SUBMISSION**)

III-2	**Applicant and/or inventor**	
III-2-1	This person is	Applicant and inventor
III-2-2	Applicant for	US only
III-2-4	Name (LAST, First)	MEI, Din-How
III-2-5	Address	5366 NW 132nd Ave. Portland, Oregon 97229 United States of America
III-2-6	State of nationality	US
III-2-7	State of residence	US
III-3	**Applicant and/or inventor**	
III-3-1	This person is	Applicant and inventor
III-3-2	Applicant for	US only
III-3-4	Name (LAST, First)	PRADHAN, Sameer S.
III-3-5	Address	17923 NW Sylvania Lane Portland, Oregon 97229 United States of America
III-3-6	State of nationality	IN
III-3-7	State of residence	US
IV-1	**Agent or common representative; or address for correspondence**	
	The person identified below is hereby/ has been appointed to act on behalf of the applicant(s) before the competent International Authorities as:	Agent
IV-1-1	Name (LAST, First)	WINKLE, Robert G.
IV-1-2	Address	WINKLE, PLLC c/o CPA GLOBAL P.O. Box 52050 Minneapolis, Minnesota 55402 United States of America
IV-1-6	Agent's registration No.	37474
IV-2	**Additional agent(s)**	additional agent(s) with same address as first named agent
IV-2-1	Name(s)	DRAEGER, Jeffrey S.(41000)
V	**DESIGNATIONS**	
V-1	**The filing of this request constitutes under Rule 4.9(a), the designation of all Contracting States bound by the PCT on the international filing date, for the grant of every kind of protection available and, where applicable, for the grant of both regional and national patents.**	
VI-1	**Priority Claim**	NONE
VII-1	**International Searching Authority Chosen**	Korean Intellectual Property Office (ISA/KR)

PCT REQUEST

Original (for **SUBMISSION**)

VIII	**Declarations**	Number of declarations	
VIII-1	Declaration as to the identity of the inventor	–	
VIII-2	Declaration as to the applicant's entitlement, as at the international filing date, to apply for and be granted a patent	–	
VIII-3	Declaration as to the applicant's entitlement, as at the international filing date, to claim the priority of the earlier application	–	
VIII-4	Declaration of inventorship (only for the purposes of the designation of the United States of America)	–	
VIII-5	Declaration as to non-prejudicial disclosures or exceptions to lack of novelty	–	
IX	**Check list**	Number of sheets	Electronic file(s) attached
IX-1	Request (including declaration sheets)	4	✓
IX-2	Description	11	–
IX-3	Claims	3	–
IX-4	Abstract	1	✓
IX-5	Drawings	13	–
IX-7	TOTAL	32	
	Accompanying Items	Paper document(s) attached	Electronic file(s) attached
IX-8	Fee calculation sheet	✓	–
IX-20	**Figure of the drawings which should accompany the abstract**	1	
IX-21	**Language of filing of the international application**	English	
X-1	**Signature of applicant, agent or common representative**	/Jeffrey S. Draeger/	
X-1-1	Name	INTEL CORPORATION	
X-1-2	Name of signatory	DRAEGER, Jeffrey S.	
X-1-3	Capacity (if such capacity is not obvious from reading the request)	Reg. No. 41000	

PCT REQUEST

Original (for **SUBMISSION**)

FOR RECEIVING OFFICE USE ONLY

10-1	**Date of actual receipt of the purported international application**	30 SEP 2011 (30.09.11)
10-2	**Drawings:**	
10-2-1	Received	
10-2-2	Not received	
10-3	**Corrected date of actual receipt due to later but timely received papers or drawings completing the purported international application**	
10-4	**Date of timely receipt of the required corrections under PCT Article 11(2)**	
10-5	**International Searching Authority**	ISA/KR
10-6	**Transmittal of search copy delayed until search fee is paid**	

FOR INTERNATIONAL BUREAU USE ONLY

11-1	**Date of receipt of the record copy by the International Bureau**	

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
4 April 2013 (04.04.2013)

WIPO | PCT

(10) International Publication Number
WO 2013/048516 A1

(51) International Patent Classification:
H01L 29/78 (2006.01) *H01L 21/336* (2006.01)

(21) International Application Number:
PCT/US2011/054464

(22) International Filing Date:
30 September 2011 (30.09.2011)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant *(for all designated States except US)*: **INTEL CORPORATION** [US/US]; 2200 Mission College Boulevard, Santa Clara, California 95052 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **ROSENBAUM, Aaron W.** [US/US]; 5530 NW Osprey Place, Portland, Oregon 97229 (US). **MEI, Din-How** [US/US]; 5366 NW 132nd Ave., Portland, Oregon 97229 (US). **PRADHAN, Sameer S.** [IN/US]; 17923 NW Sylvania Lane, Portland, Oregon 97229 (US).

(74) Agent: **BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP**; 1279 Oakmead Parkway, Sunnyvale, CA 94086 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *of inventorship (Rule 4.17(iv))*

Published:

— *with international search report (Art. 21(3))*

WO 2013/048516 A1

(54) **Title**: CAPPING DIELECTRIC STRUCTURE FOR TRANSISTOR GATES

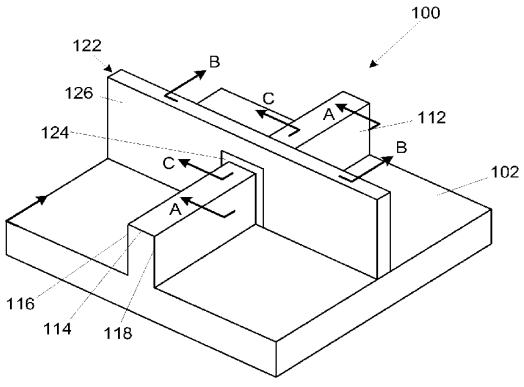


FIG. 1

(57) **Abstract**: The present description relates to the field of fabricating microelectronic transistors, including non-planar transistors, for microelectronic devices. Embodiments of the present description relate to the formation a recessed gate electrode capped by a substantially void-free dielectric capping dielectric structure which may be formed with a high density plasma process.

CAPPING DIELECTRIC STRUCTURE FOR TRANSISTOR GATES

BACKGROUND

Embodiments of the present description generally relate to the field of microelectronic device fabrication and, more particularly, to the fabrication of capping dielectric structures within non-planar transistor gates.

BRIEF DESCRIPTION OF THE DRAWINGS

The subject matter of the present disclosure is particularly pointed out and distinctly claimed in the concluding portion of the specification. The foregoing and other features of the present disclosure will become more fully apparent from the following description and appended claims, taken in conjunction with the accompanying drawings. It is understood that the accompanying drawings depict only several embodiments in accordance with the present disclosure and are, therefore, not to be considered limiting of its scope. The disclosure will be described with additional specificity and detail through use of the accompanying drawings, such that the advantages of the present disclosure can be more readily ascertained, in which:

FIG. 1 is a perspective view of a non-planar transistor, according to an embodiment of the present description.

FIG. 2 illustrates a side cross-sectional view of a non-planar transistor fin formed in or on a microelectronic substrate.

FIG. 3 illustrates a side cross-sectional view of a sacrificial material deposited over the non-planar transistor fin of FIG. 2, according to an embodiment of the present description.

FIG. 4 illustrates a side cross-sectional view of a trench formed in the sacrificial material deposited to expose a portion of the non-planar transistor fin of FIG. 3, according to an embodiment of the present description.

FIG. 5 illustrates a side cross-sectional view of a sacrificial gate formed in the trench of FIG. 4, according to an embodiment of the present description.

FIG. 6 illustrates a side cross-sectional view of the sacrificial gate after the removal of the sacrificial material of FIG. 5, according to an embodiment of the present description.

FIG. 7 illustrates a side cross-sectional view of a conformal dielectric layer deposited over the sacrificial gate and microelectronic substrate of FIG. 6, according to an embodiment of the present description.

FIG. 8 illustrates a side cross-sectional view of gate spacers formed from the conformal dielectric layer of FIG. 7, according to an embodiment of the present description.

FIG. 9 illustrates a side cross-sectional view of a source region and a drain region formed in the non-planar transistor fin on either side of the gate spacers of FIG. 8, according to an embodiment of the present description.

FIG. 10 illustrates a side cross-sectional view of a first dielectric material deposited over the gate spacers, the sacrificial gate, the non-planar transistor fin, and the microelectronic substrate of FIG. 9, according to an embodiment of the present description.

FIG. 11 illustrates a side cross-sectional view of the structure of FIG. 10 after planarizing the first dielectric material to expose a top surface of the sacrificial gate, according to an embodiment of the present description.

FIG. 12 illustrates a side cross-sectional view of the structure of FIG. 11 after the removal of the sacrificial gate to form a gate trench, according to an embodiment of the present description.

FIG. 13 illustrates a side cross-sectional view of the structure of FIG. 12 after the formation of a gate dielectric adjacent the non-planar transistor fin between the gate spacers, according to an embodiment of the present description.

FIG. 14 illustrates a side cross-sectional view of a conductive gate material deposited in the gate trench of FIG. 13, according to an embodiment of the present description.

FIG. 15 illustrates a side cross-sectional view of the structure of FIG. 14 after the removal of excess conductive gate material to form a non-planar transistor gate, according to an embodiment of the present description.

FIG. 16 illustrates a side cross-sectional view of the structure of FIG. 15 after etching away a portion of the non-planar transistor gate to form a recessed non-planar transistor gate, according to an embodiment of the present description.

FIG. 17 illustrates a side cross-sectional view of the structure of FIG. 16 after depositing a capping dielectric material into the recess resulting from the formation of the recessed non-planar transistor gate, according to an embodiment of the present description.

FIG 18 illustrates a flow diagram of a high density deposition process for the deposition of the capping dielectric material of FIG. 17, according to an embodiment of the present description.

FIG. 19 illustrates a side cross-sectional view of the structure of FIG. 17 after the removal of excess capping dielectric material to form a capping dielectric structure on the non-planar transistor gate, according to an embodiment of the present description.

FIG. 20 illustrates a side cross-sectional view of a second dielectric material deposited over the first dielectric material layer, the gate spacers, and the sacrificial gate top surface of FIG. 19, according to an embodiment of the present description.

FIG. 21 illustrates a side cross-sectional view of an etch mask patterned on the second dielectric material of FIG. 20, according to an embodiment of the present description.

FIG. 22 illustrates a side cross-sectional view of a contact opening formed through the first and second dielectric material layer of FIG. 21, according to an embodiment of the present description.

FIG. 23 illustrates a side cross-sectional view of the structure of FIG. 22 after the removal of the etch mask, according to an embodiment of the present description.

FIG. 24 illustrates a side cross-sectional view of a conductive contact material deposited in the contact opening of FIG. 23, according to an embodiment of the present description.

FIG. 25 illustrates a side cross-sectional view of the structure of FIG. 24 after the removal of the excess conductive contact material to form a source/drain contact, according to an embodiment of the present description.

DETAILED DESCRIPTION

In the following detailed description, reference is made to the accompanying drawings that show, by way of illustration, specific embodiments in which the claimed subject matter may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the subject matter. It is to be understood that the various embodiments, although different, are not necessarily mutually exclusive. For example, a particular feature, structure, or characteristic described herein, in connection with one embodiment, may be implemented within other embodiments without departing from the spirit and scope of the claimed subject matter. References within this specification to "one embodiment" or "an embodiment" mean that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one implementation encompassed within the present invention. Therefore, the use of the phrase "one embodiment" or "in an embodiment" does not necessarily refer to the same embodiment. In addition, it is to be understood that the location or arrangement of

individual elements within each disclosed embodiment may be modified without departing from the spirit and scope of the claimed subject matter. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the subject matter is defined only by the appended claims, appropriately interpreted, along with the full range of equivalents to which the appended claims are entitled. In the drawings, like numerals refer to the same or similar elements or functionality throughout the several views, and that elements depicted therein are not necessarily to scale with one another, rather individual elements may be enlarged or reduced in order to more easily comprehend the elements in the context of the present description.

In the fabrication of non-planar transistors, such as tri-gate transistors and FinFETs, non-planar semiconductor bodies may be used to form transistors capable of full depletion with very small gate lengths (e.g., less than about 30 nm). These semiconductor bodies are generally fin-shaped and are, thus, generally referred to as transistor "fins". For example in a tri-gate transistor, the transistor fins have a top surface and two opposing sidewalls formed on a bulk semiconductor substrate or a silicon-on-insulator substrate. A gate dielectric may be formed on the top surface and sidewalls of the semiconductor body and a gate electrode may be formed over the gate dielectric on the top surface of the semiconductor body and adjacent to the gate dielectric on the sidewalls of the semiconductor body. Thus, since the gate dielectric and the gate electrode are adjacent to three surfaces of the semiconductor body, three separate channels and gates are formed. As there are three separate channels formed, the semiconductor body can be fully depleted when the transistor is turned on. With regard to finFET transistors, the gate material and the electrode only contact the sidewalls of the semiconductor body, such that two separate channels are formed (rather than three in tri-gate transistors).

Embodiments of the present description relate to the formation of microelectronic transistors, wherein the transistor includes a recessed gate electrode capped by a substantially void-free dielectric capping dielectric structure which may be formed with a high density plasma process. Although embodiments herein are described in terms of non-planar transistors and replacement gate techniques, the subject matter is not so limited, as the subject matter may be used in planar transistors and in non-replacement gate applications.

FIG. 1 is a perspective view of a non-planar transistor 100, including at least one gate formed on at least one transistor fin, which are formed on a microelectronic substrate 102. In an embodiment of the present disclosure, the microelectronic substrate 102 may

be a monocrystalline silicon substrate. The microelectronic substrate 102 may also be other types of substrates, such as silicon-on-insulator ("SOI"), germanium, gallium arsenide, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, gallium antimonide, and the like, any of which may be combined with silicon.

The non-planar transistor, shown as a tri-gate transistor, may include at least one non-planar transistor fin 112. The non-planar transistor fin 112 may have a top surface 114 and a pair of laterally opposite sidewalls, sidewall 116 and opposing sidewall 118, respectively.

As further shown in FIG. 1, at least one non-planar transistor gate 122 may be formed over the non-planar transistor fin 112. The non-planar transistor gate 122 may be fabricated by forming a gate dielectric layer 124 on or adjacent to the non-planar transistor fin top surface 114 and on or adjacent to the non-planar transistor fin sidewall 116 and the opposing non-planar transistor fin sidewall 118. A gate electrode 126 may be formed on or adjacent the gate dielectric layer 124. In one embodiment of the present disclosure, the non-planar transistor fin 112 may run in a direction substantially perpendicular to the non-planar transistor gate 122.

The gate dielectric layer 124 may be formed from any well-known gate dielectric material, including but not limited to silicon dioxide (SiO_2), silicon oxynitride (SiO_xN_y), silicon nitride (Si_3N_4), and high-k dielectric materials such as hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate. The gate dielectric layer 124 can be formed by well-known techniques, such as by conformally depositing a gate dielectric material and then patterning the gate dielectric material with well-known photolithography and etching techniques, as will be understood to those skilled in the art.

The gate electrode 126 can be formed of any suitable gate electrode material. In an embodiment of the present disclosure, the gate electrode 126 may be formed from materials that include, but are not limited to, polysilicon, tungsten, ruthenium, palladium, platinum, cobalt, nickel, hafnium, zirconium, titanium, tantalum, aluminum, titanium carbide, zirconium carbide, tantalum carbide, hafnium carbide, aluminum carbide, other metal carbides, metal nitrides, and metal oxides. The gate electrode 126 can be formed by well-known techniques, such as by blanket depositing a gate electrode material and then

patterning the gate electrode material with well-known photolithography and etching techniques, as will be understood to those skilled in the art.

A source region and a drain region (not shown in FIG. 1) may be formed in the non-planar transistor fin 112 on opposite sides of the gate electrode 126. In one embodiment, the source and drain regions may be formed by doping the non-planar transistor fins 112, as will be understood to those skilled in the art. In another embodiment, the source and drain regions may be formed by removing potions of the non-planar transistor fins 112 and replacing these portions with appropriate material(s) to form the source and drain regions, as will be understood to those skilled in the art.

FIGs. 2-26 illustrate side cross-sectional view of one embodiment of fabricating a non-planar transistor, wherein FIGs. 2-5 are views along arrows A-A and B-B of FIG. 1, FIGs. 6-15 are views along arrows A-A of FIG. 1, and FIG. 16-26 are views along arrows C-C of FIG. 1.

As shown in FIG. 2, the non-planar transistor fin 112 may be formed by etching the microelectronic substrate 102 or by forming the non-planar transistor fin 112 on the microelectronic substrate 102 by any technique known in the art. As illustrate in FIG. 3, a sacrificial material 132 may be deposited over the non-planar transistor fin 112, as shown in FIG. 3, and a trench 134 may be formed in the sacrificial material 132 to expose a potion of the non-planar transistor fin 112, as shown in FIG. 4. The sacrificial material 132 may be any appropriate material known in the art, and the trench 134 may be formed by any technique known in the art, including but not limited to lithographic masking and etching.

As shown in FIG. 5, a sacrificial gate 136 may be formed in the trench 134 (see FIG. 4). The sacrificial gate 136 may be any appropriate material, such as a polysilicon material and the like, and may be deposited in the trench 134 (see FIG. 4) by any technique known in the art, including but not limited to chemical vapor deposition ("CVD") and physical vapor deposition ("PVD").

As shown in FIG. 6, the sacrificial material 132 of FIG. 5 may be removed to expose the sacrificial gate 136 by any technique known in the art, such as selectively etching the sacrificial material 132. As shown in FIG. 7, a conformal dielectric layer 142 may be deposited over the sacrificial gate 136 and microelectronic substrate 102. The conformal dielectric layer 142 may be any appropriate material, including but not limited to silicon nitride (Si_3N_4) and silicon carbide (SiC), and may be formed by any appropriate technique including but not limited to atomic layer deposition ("ALD").

As shown in FIG. 8, the conformal dielectric layer 142 of FIG. 7 may be etched, such as by directional etch with an appropriate etchant, to form a pair of gate spacers 144 on sidewalls 146 of the sacrificial gate 136, while substantially removing the conformal dielectric material layer 142 adjacent the microelectronic substrate 102 and a top surface 148 of the sacrificial gate 136. It is understood that fin spacers (not shown) may be simultaneously formed on sidewalls 116 and 118 (see FIG. 1) of the non-planar transistor fin 112 during the formation of the gate spacers 144.

As shown in FIG. 9, a source region 150a and a drain region 150b may be formed on either side of the gate spacers 144. In one embodiment, the source region 150a and the drain region 150b may be formed in the non-planar transistor fin 112 with the implantation of dopants. As will be understood to those skilled in that art, dopant implantation is a process of introducing impurities into semiconducting materials for the purpose changing its conductivity and electronic properties. This is generally achieved by ion implantation of either P-type ions (e.g. boron) or N-type ions (e.g. phosphorus), collectively referred to as "dopants". In another embodiment, portions of the non-planar transistor fin 112 may be removed by any technique known in the art, such as etching, and the source region 150a and a drain region 150b may be formed in place of the removed portions. The source region 150a and the drain region will hereinafter be referred to collectively as "source/drain region 150".

As shown in FIG. 10, a first dielectric material layer 152 may be deposited over the gate spacers 144, the sacrificial gate top surface 148, the non-planar transistor fin 112, and the microelectronic substrate 102. The first dielectric material layer 152 may be planarizing to expose the sacrificial gate top surface 148, as shown in FIG. 11. The planarization of the first dielectric material layer 152 may be achieved by any technique known in the art, including but not limited to chemical mechanical polishing (CMP).

As shown in FIG. 12, the sacrificial gate 136 of FIG. 11 may be removed to form a gate trench 154. The sacrificial gate 136 may be removed by any technique known in the art, such as a selective etch. As shown in FIG. 13, the gate dielectric layer 124, as also illustrated in FIG. 1, may be formed to abut the non-planar transistor fin 112, as previously discussed.

As shown in FIG. 14, a conductive gate material 156 may be deposited in the gate trench 154, and excess conductive gate material 156 (e.g. conductive gate material 156 not within the gate trench 154 of FIG. 12) may be removed to from the non-planar transistor gate electrode 126 (see also FIG. 1), as shown in FIG. 15. The materials and methods of

forming the gate electrode 126 have been previously discussed. The removal of the excess conductive gate material 156 may be achieved by any technique known in the art, including but not limited to chemical mechanical polishing (CMP), etching, and the like.

As shown in FIG. 16, a portion of the non-planar transistor gate electrode 126 may be removed to form a recess 158 and a recessed non-planar transistor gate 162. The removal may be accomplished by any known technique, including but not limited to wet or dry etching.

As shown in FIG. 17, a capping dielectric material 164 may be deposited to fill the recess 158 of FIG. 16. The capping dielectric material 164 may be any appropriate material, including but not limited to silicon nitride (Si_xN_y) and silicon carbide (Si_xC_y). However, known processes for depositing dielectrics, such as plasma enhanced chemical vapor deposition, may not be capable of filing recesses 158 that have high aspect ratios (height to width ratio) and may result in voids forming in the capping dielectric material 164. Such voids may result in contact-to-gate short circuits, as will be discussed. To prevent voids from forming, high temperature deposition techniques (e.g. greater than 400°C) may be employed. However, high temperature deposition may affect the work function of the non-planar transistor gate electrode 126, as will be understood by those skilled in the art. Furthermore, high temperature deposition may result in dopant movement or deactivation in the source/drain regions 150.

FIG. 18 is a flow diagram of a high density plasma (HDP) dielectric deposition process 200 for forming substantially void free capping dielectric material 164 (see FIG. 17) within a high aspect ratio recesses 158 (see FIG. 17). As defined in block 210, walls of a high density plasma chamber may be coated with a desired dielectric film, i.e. the dielectric to be deposited. As defined in block 220, a microelectronic substrate, such as a silicon wafer, may be placed on a chuck in the high density plasma chamber. In one embodiment, the chuck may be a water-cooled ceramic electrostatic chuck at room temperature, e.g. about 75°C. As defined in block 230, the high density plasma chamber may be pressurized with an inert gas, such as argon. In one embodiment, the high density plasma chamber may be pressure to a pressure greater than about 40 mTorr to strike a sustainable low power radio frequency (RF) plasma. As defined in block 240, RF electrodes within the high density plasma chamber may be powered up while introducing at least one reactive gas into the high density plasma chamber. In one embodiment, each of the RF electrodes, such as top and side electrodes, may be powered up to a range between about 2kV and 8kV for a time duration between about 30 and 60 seconds. The

reactive gas may include, but is not limited to oxygen, nitrogen, and the like. The microelectronic substrate temperature can be modulated between less than about 300°C and 600°C by adjusting the temperature of the chuck. It is understood that the time duration, microelectronic substrate temperature, RF power, and reactive gas mixture may be adjusted for a desired deposition result. As defined in block 250, the deposition gas may be introduced to the high density plasma chamber while powering a bias RF electrode. In one embodiment, a deposition gas comprising silane (SiH_4), nitrogen (N_2), argon (Ar), and helium (He) may be used to deposit a silicon nitride dielectric. In another embodiment, a deposition gas comprising silane (SiH_4), methane (CH_4), argon (Ar), and helium (He) may be used to deposit a silicon carbide dielectric. The RF electrode may be power to a range between about 3kV and 5kV with a bias RF electrode ranging from about 1kV and 3kV. The ratio of the nitrogen gas volume to the silane gas volume for silicon nitride deposition and ratio of the methane gas volume to the silane gas volume may be between about 0.5 and 9, depending on the desired properties of the dielectric layer, while the silane gas flow is kept between about 30 and 70 sccm. Under these conditions, the deposition rate may be in a range between about 7 to 30 Angstroms per second. It is understood that the deposition duration may be calculated based on the desired dielectric layer thickness and deposition rate. As defined in block 260, the deposition process is discontinued by discontinuing the introduction of deposition gas into the high density plasma deposition chamber and discontinuing power to the bias RF. The power to the RF electrodes may be ramped down and electrostatic charges are dissipated off of the microelectronic substrate, so that the microelectronic substrate can be removed from the electrostatic chuck. After removal the high density plasma chamber may be cleaned, such as by a remote plasma unit, and the walls of the high density plasma chamber may be recoated with a desired dielectric film.

The above-described process may result in simultaneous deposition and sputtering of the dielectric layer, wherein an appropriate deposition to sputtering ratio may result in a substantially void-free dielectric layer.

After deposition, the capping dielectric material 164 may be planarized to remove excess capping dielectric material 164 (e.g. capping dielectric material 164 not within the recess of FIG. 16) to form a capping dielectric structure 166 on the recessed non-planar transistor gate 162 and between a gate spacers 144, as shown in FIG. 19. The removal of the excess capping dielectric material 164 may be achieved by any technique known in the

art, including but not limited to chemical mechanical polishing (CMP), etching, and the like.

As shown in FIG. 20, a second dielectric material layer 168 may be deposited over the first dielectric material layer 152, the gate spacers 144, and the capping dielectric structure 166. The second dielectric material layer 168 may be formed from any appropriate dielectric material, including but not limited to silicon dioxide (SiO_2), silicon oxynitride (SiO_xN_y), and silicon nitride (Si_3N_4), by any known deposition technique. As shown in FIG. 21, an etch mask 172 may be patterned with at least one opening 174 on the second dielectric material layer 168, such as by well known lithographic techniques.

As shown in FIG. 22, a contact opening 182 may be formed through the first dielectric material layer 152 and the second dielectric material layer 168 by etching through the etch mask opening 174 of FIG. 21 to expose a portion of the source/drain region 150. The etch mask 172 of FIG. 22 may be removed thereafter, as shown in FIG. 23. In one embodiment, the first dielectric material layer 152 and the dielectric material layer 168 differs from dielectric material of both the gate spacers 144 and the capping dielectric structure 166, such that the etching of the first dielectric material layer 152 and the second dielectric layer 168 may be selective to the gate spacers 144 and the capping dielectric structure 166 (i.e. etches faster). This is known in the art as a self-aligning.

As shown in FIG. 24, a conductive contact material 188 may be deposited in the contact opening 182 of FIG. 23. The conductive contact material 188 may include, but is not limited to, polysilicon, tungsten, ruthenium, palladium, platinum, cobalt, nickel, hafnium, zirconium, titanium, tantalum, aluminum, titanium carbide, zirconium carbide, tantalum carbide, hafnium carbide, aluminum carbide, other metal carbides, metal nitrides, and metal oxides. It is understood that various adhesion layers, barrier layers, silicide layers, and/or conductive layers may be conformally disposed or formed in the contact opening 182 of FIG. 23 prior to the deposition of the conductive contact material 188.

As shown in FIG. 25, excess conductive contact material 188 of FIG. 24 (e.g. conductive contact material 188 not within the contact opening 182 of FIG. 12) may be removed to form a source/drain contact 190. The removal of the excess conductive contact material 188 may be achieved by any technique known in the art, including but not limited to chemical mechanical polishing (CMP), etching, and the like.

As previously discussed, in one embodiment, the first dielectric material layer 152 and the dielectric material layer 168 differs from dielectric material of both the gate

spacers 144 and the capping dielectric structure 166, such that the etching of the first dielectric material layer 152 and the second dielectric layer 168 may be selective to the gate spacers 144 and the capping dielectric structure 166 (i.e. etches faster). Thus, the recessed non-planar transistor 162 is protected during the formation of the contact opening 182. This allows for the formation of a relatively large sized source/drain contact 190, which may increase the transistor drive current performance, without the risk of shorting between the source/drain contact 190 and the recessed non-planar transistor gate 162. This is not possible if voids exist in the capping dielectric structure 144, as the voids would increase the likelihood of shorting between the source/drain contact 190 and the recessed non-planar transistor gate 162.

It is understood that the subject matter of the present description is not necessarily limited to specific applications illustrated in FIGs. 1-25. It is understood that although the illustrated embodiments are directed to non-planar applications, the subject matter may be applied to non-planar transistors and to non-replacement gate applications. Furthermore, the subject matter may be applied to other microelectronic device fabrication applications, as will be understood to those skilled in the art.

Having thus described in detail embodiments of the present invention, it is understood that the invention defined by the appended claims is not to be limited by particular details set forth in the above description, as many apparent variations thereof are possible without departing from the spirit or scope thereof.

CLAIMS

What is claimed is:

1. A transistor gate, comprising:

a pair of gate spacers

a recessed gate electrode disposed between the pair of gate spacers; and

a substantially void free capping dielectric structure disposed adjacent the recessed gate electrode and between the pair of gate spacers.

2. The transistor gate of claim 1, wherein the substantially void free capping dielectric structure comprises silicon nitride.

3. The transistor gate of claim 1, wherein the substantially void free capping dielectric structure comprises silicon carbide.

4. The transistor gate of claim 1, wherein the recessed gate electrode is a non-planar gate electrode.

5. A microelectronic device, comprising:

a non-planar transistor gate over a non-planar transistor fin, wherein the non-planar transistor gate comprises a gate electrode recessed between a pair of gate spacers and a substantially void free capping dielectric structure disposed on the recessed gate electrode between the gate spacers,

a source/drain region;

at least one dielectric material layer over the source/drain region, the non-planar transistor gate spacers, and the substantially void free capping dielectric structure; and

a source/drain contact extending through a portion of the at least one dielectric material layer to contact the source/drain region.

6. The microelectronic device of claim 5, wherein the substantially void free capping dielectric structure comprises silicon nitride.

7. The microelectronic device of claim 5, wherein the substantially void free capping dielectric structure comprises silicon carbide.

8. The microelectronic device of claim 5, wherein the source/drain contact abuts at least a portion of one non-planar transistor gate spacer.

9. The microelectronic device of claim 5, wherein the source/drain contact abuts at least a portion of the capping dielectric structure.

10. A method of fabricating a transistor gate, comprising:

forming a pair of gate spacers;

forming a gate electrode disposed between the pair of gate spacers; and

high density plasma depositing a capping dielectric structure on a top surface of the recessed gate electrode and between the pair of gate spacers.

11. The method of claim 10, wherein high density plasma depositing the capping dielectric structure comprises high density plasma depositing a silicon nitride capping dielectric structure.

12. The method of claim 10, wherein high density plasma depositing the capping dielectric structure comprises high density plasma depositing a silicon carbide capping dielectric structure.

13. The method of claim 10, wherein high density plasma depositing the capping dielectric structure comprises high density plasma depositing the capping dielectric structure at a temperature between about 300 °C and 600°C.

14. The method of claim 10, wherein forming the gate electrode comprises forming a non-planar gate electrode.

15. A method comprising:

forming a sacrificial non-planar transistor gate over a non-planar transistor fin;

depositing a dielectric material layer over the sacrificial non-planar transistor gate and the non-planar transistor fin;

forming non-planar transistor gate spacers from a portion of the dielectric material layer adjacent the sacrificial non-planar transistor gate;

forming a source/drain region;

removing the sacrificial non-planar transistor gate to form a gate trench between the non-planar transistor gate spacers and expose a portion of the non-planar transistor fin;

forming a gate dielectric adjacent the non-planar transistor fin within the gate trench;

depositing conductive gate material within the gate trench;

removing a portion of the conductive gate material to form a recess between the non-planar transistor gate spacers;

forming a capping dielectric structure within the recess by high density plasma depositing a dielectric material;

forming at least one dielectric material over the source/drain region, the non-planar transistor gate spacers, and the capping dielectric structure; and

forming a contact opening through the at least one dielectric material to expose at least a portion of the source/drain region.

16. The method of claim 15, wherein high density plasma depositing the capping dielectric structure comprises high density plasma depositing a silicon nitride capping dielectric structure.

17. The method of claim 15, wherein high density plasma depositing the capping dielectric structure comprises high density plasma depositing a silicon carbide capping dielectric structure.

18. The method of claim 15, wherein high density plasma depositing the capping dielectric structure comprises high density plasma depositing the capping dielectric structure at a temperature between about 300 °C and 600°C.

19. The method of claim 15, wherein forming a capping dielectric structure comprises:

high density plasma depositing capping dielectric material within the recess; and

removing excess capping dielectric material.

20. The method of claim 15, wherein forming a contact opening through the dielectric material to expose at least a portion of the source/drain region further comprises forming a contact opening through the dielectric material which exposes at least a portion of the source/drain region and at least a portion of one non-planar transistor gate spacer.

21. The method of claim 20, further comprising forming a source/drain contact to abut the exposed portion of the source/drain region and exposed portion of the non-planar transistor gate spacer.

22. The method of claim 15, wherein forming a contact opening through the dielectric material to expose at least a portion of the source/drain region further comprises forming a contact opening through the dielectric material which exposes at least a portion of the source/drain region and at least a portion of the capping dielectric structure.

23. The method of claim 22, further comprising forming a source/drain contact abuts the exposed portion of the source/drain region and the exposed portion of the capping dielectric structure.

24. The method of claim 15, wherein forming a contact opening through the dielectric material to expose at least a portion of the source/drain region further comprises forming a contact opening through the dielectric material exposes at least a portion of the source/drain region, at least a portion of the non-planar transistor gate spacer, and at least a portion of the capping dielectric structure.

25. The method of claim 24, further comprising forming a source/drain contact to abut the exposed portion of the source/drain region, the exposed portion of non-planar gate spacer, and the exposed portion of the capping dielectric structure.

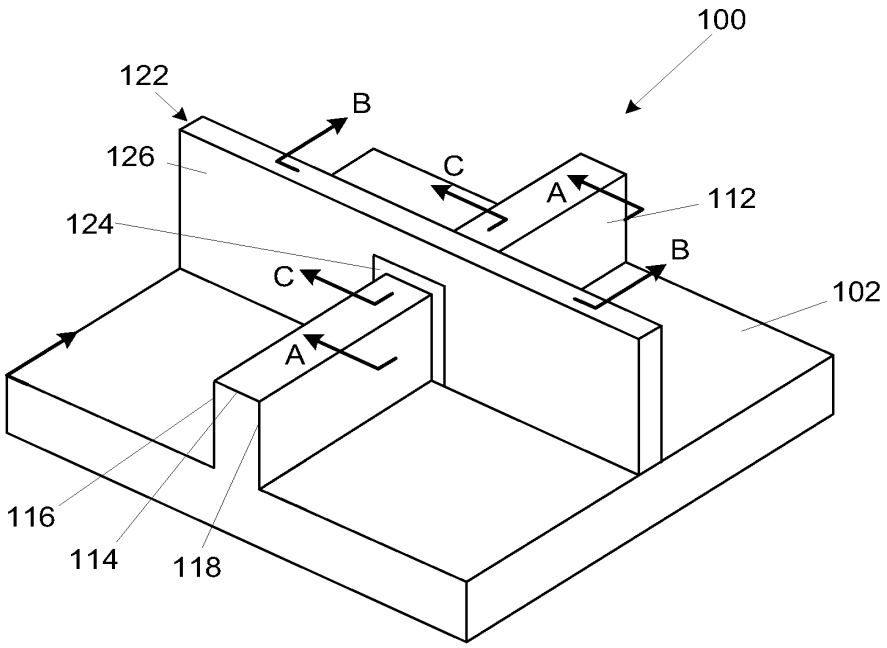


FIG. 1

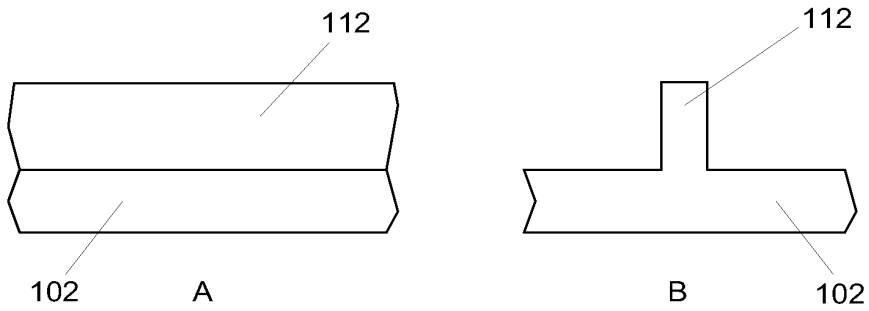


FIG. 2

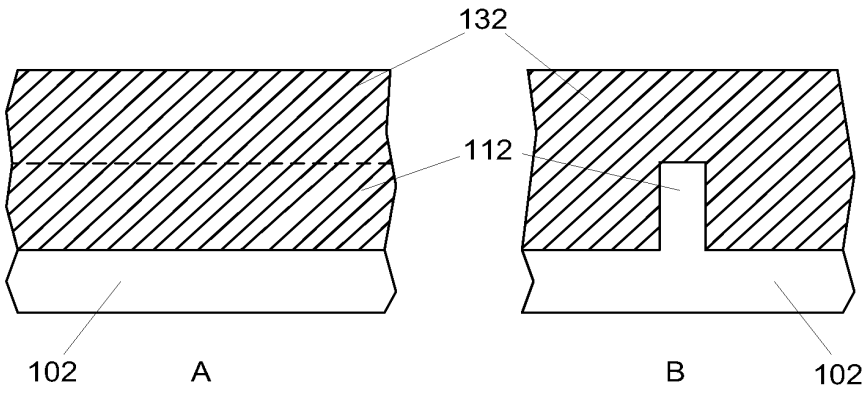


FIG. 3

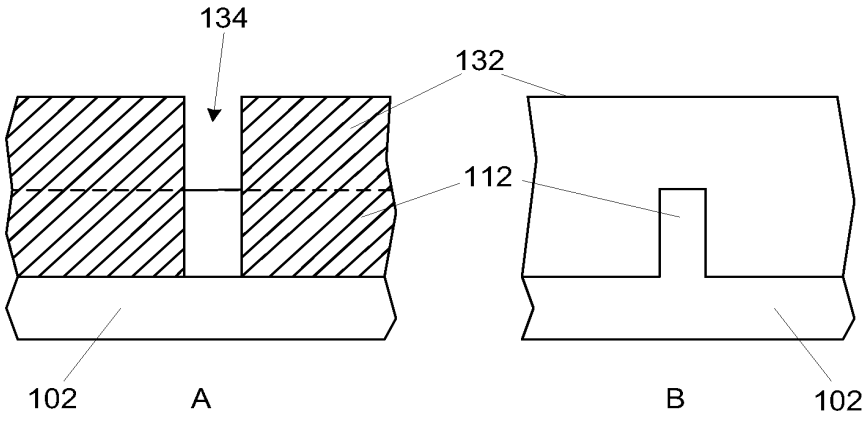


FIG. 4

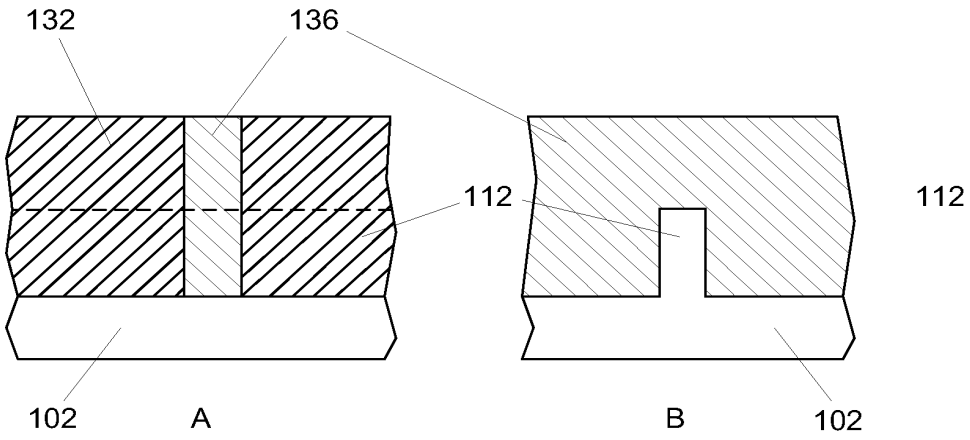


FIG. 5

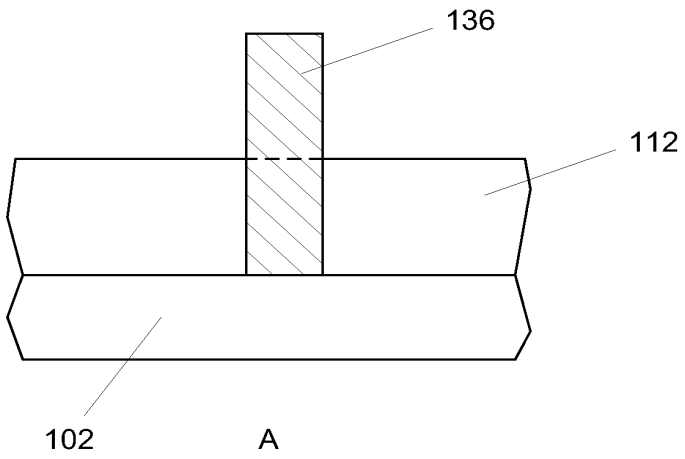


FIG. 6

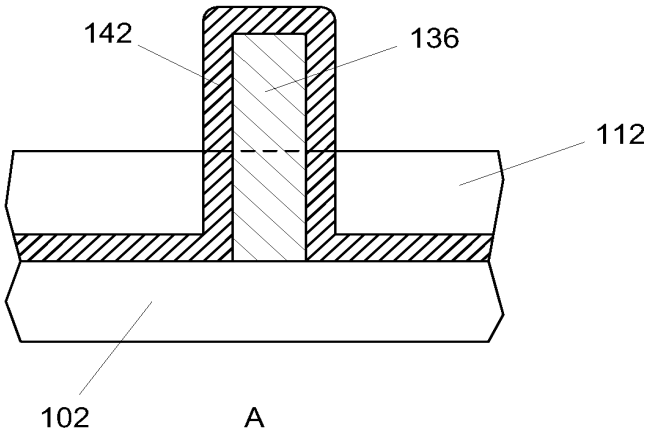


FIG. 7

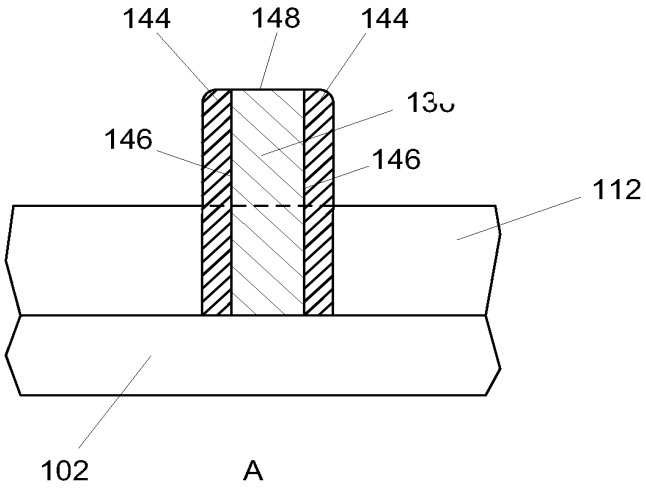


FIG. 8

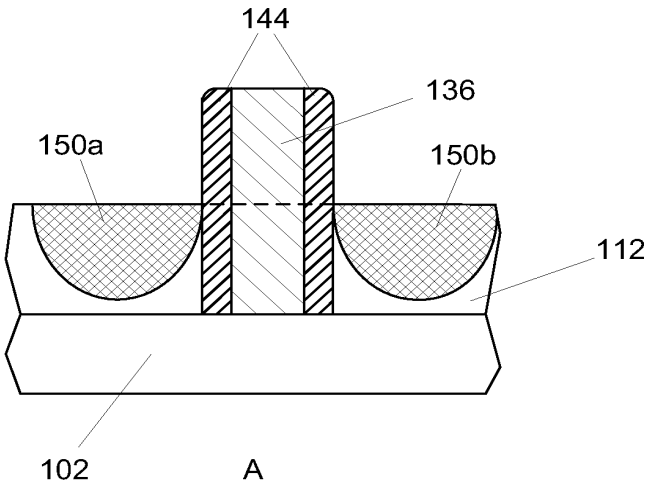


FIG. 9

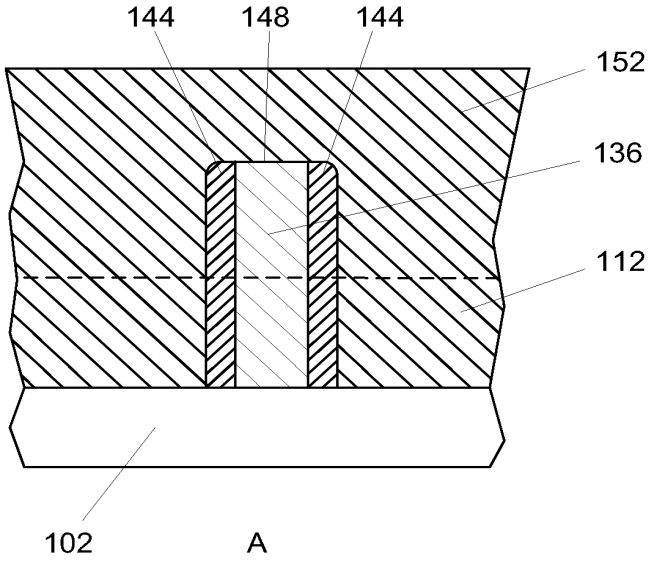


FIG. 10

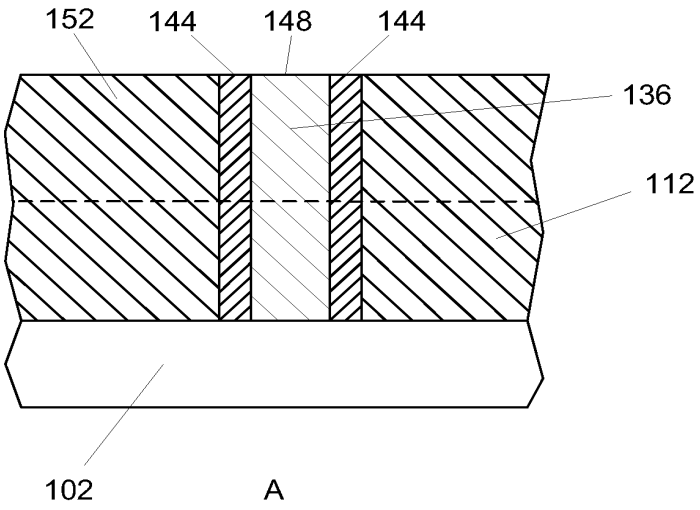


FIG. 11

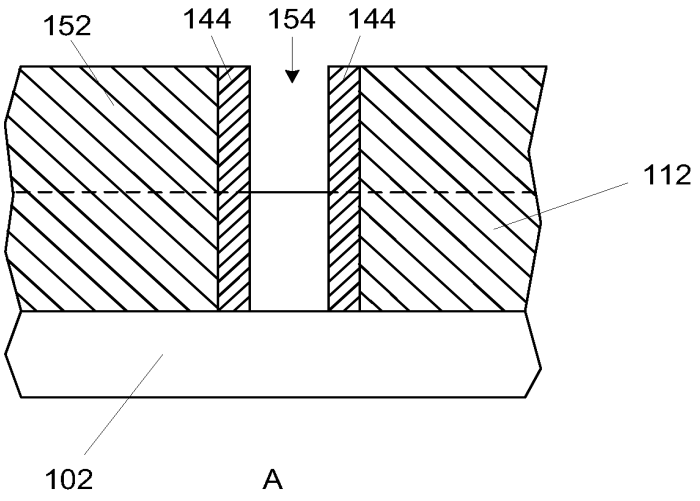


FIG. 12

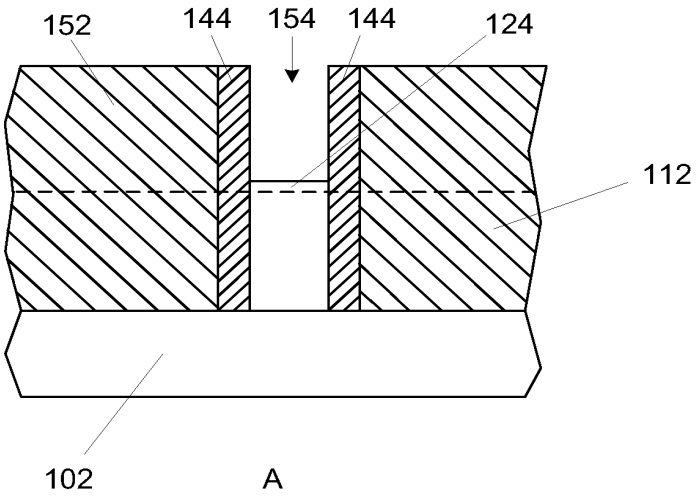


FIG. 13

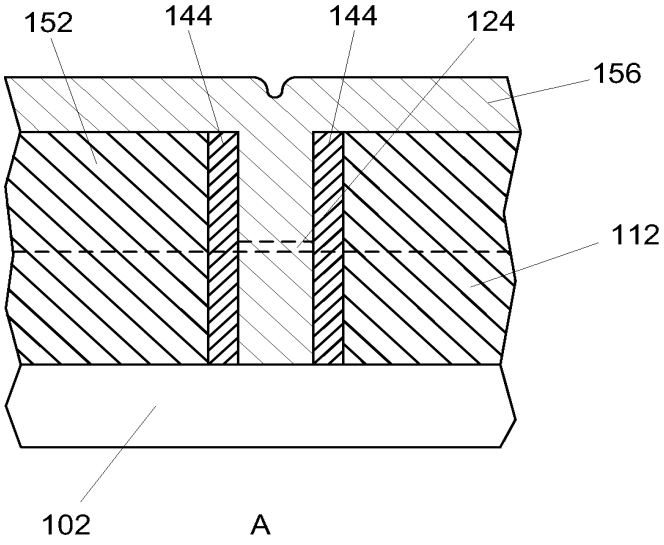


FIG. 14

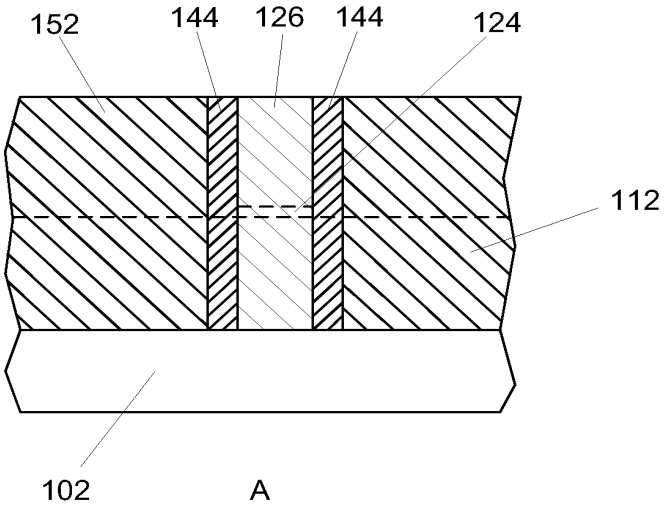

152
144
126
144
124
112
102
A

FIG. 15

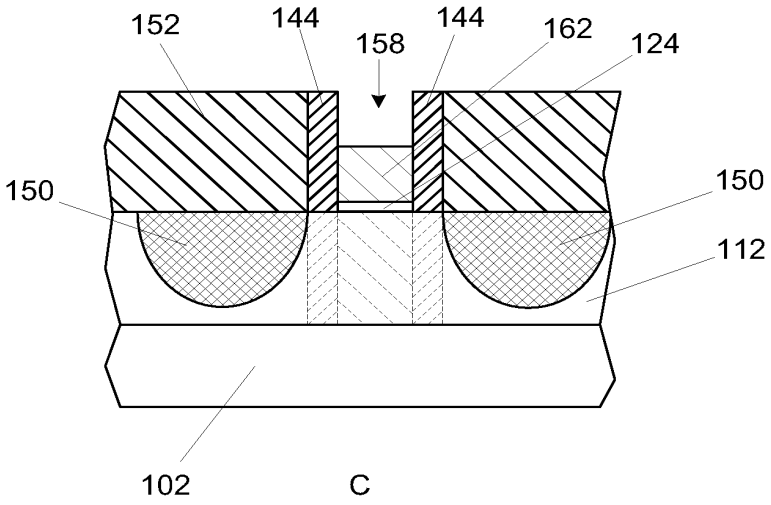

152
144
158
144
162
124
150
150
112
102
C

FIG. 16

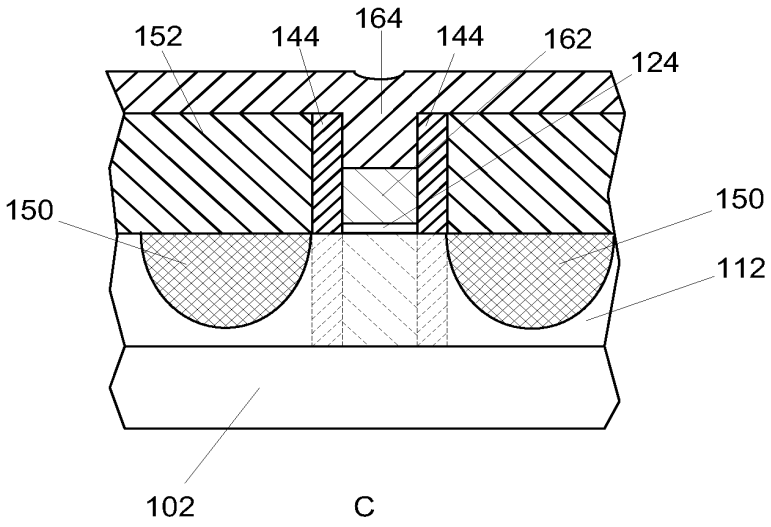

152
144
164
144
162
124
150
150
112
102
C

FIG. 17

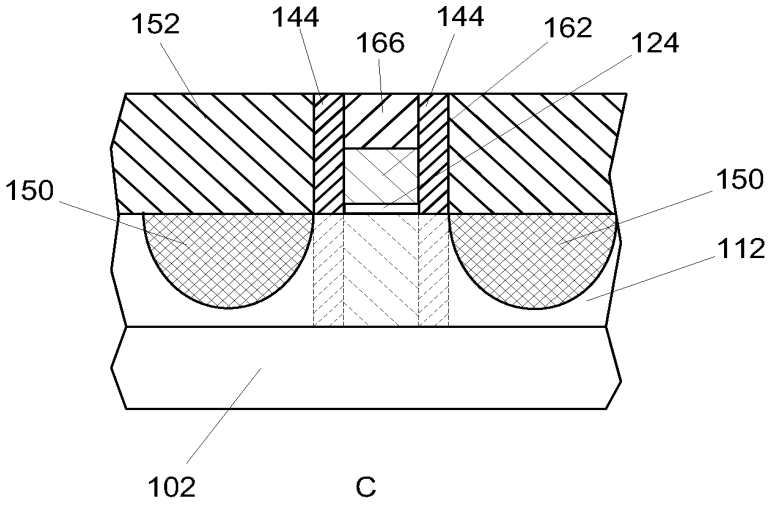

152
144
166
144
162
124
150
150
112
102
C

FIG. 19

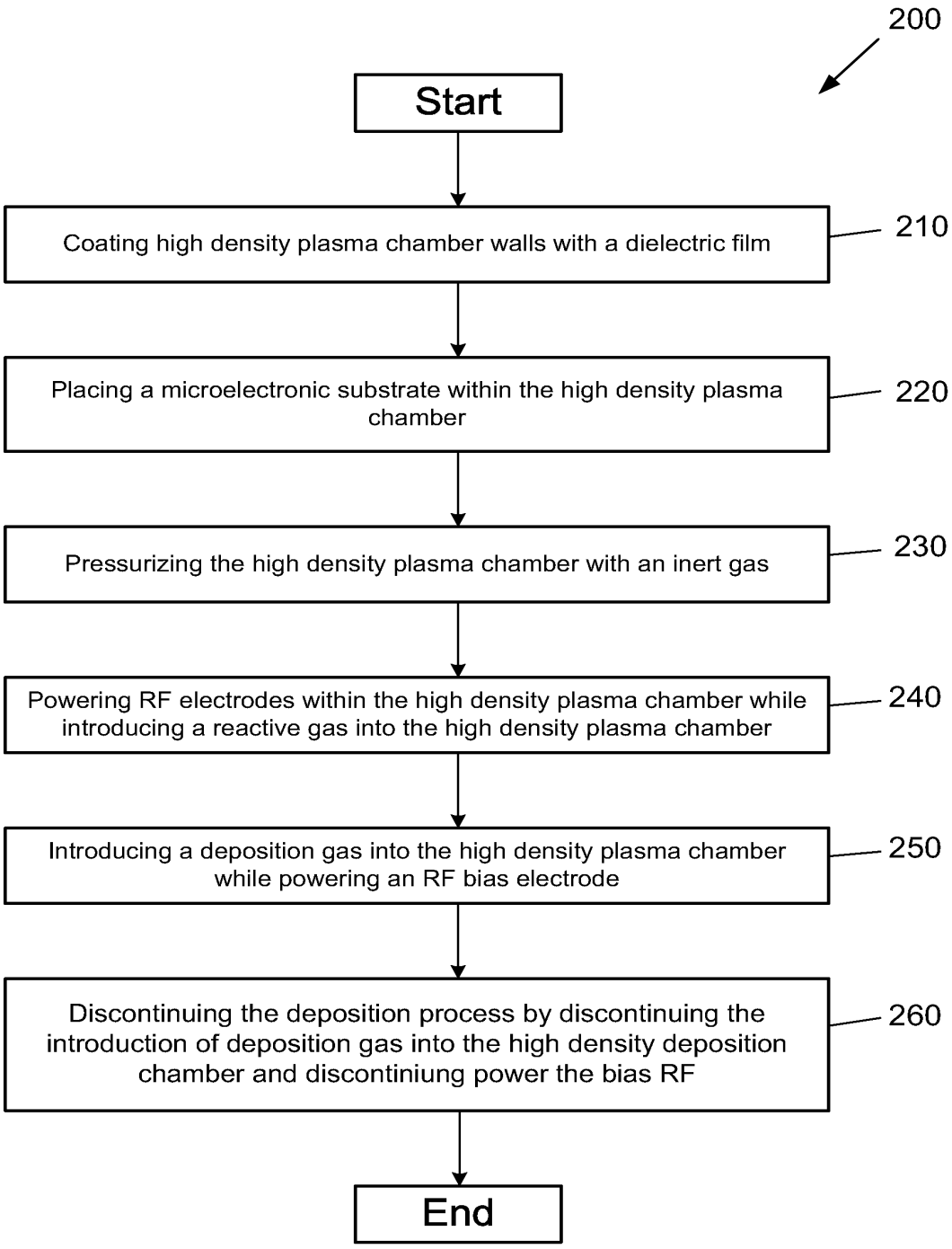

200
Start
Coating high density plasma chamber walls with a dielectric film
210
Placing a microelectronic substrate within the high density plasma chamber
220
Pressurizing the high density plasma chamber with an inert gas
230
Powering RF electrodes within the high density plasma chamber while introducing a reactive gas into the high density plasma chamber
240
Introducing a deposition gas into the high density plasma chamber while powering an RF bias electrode
250
Discontinuing the deposition process by discontinuing the introduction of deposition gas into the high density deposition chamber and discontiniung power the bias RF
260
End

FIG. 18

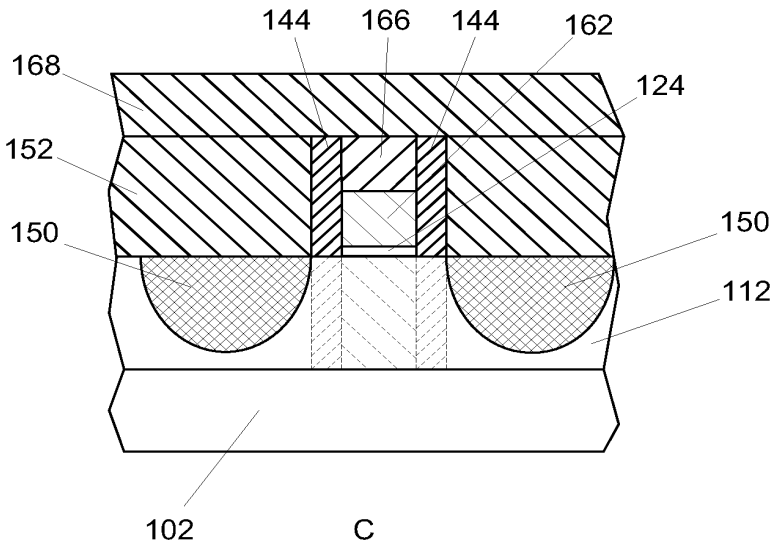

144
166
144
162
168
124
152
150
150
112
102
C

FIG. 20

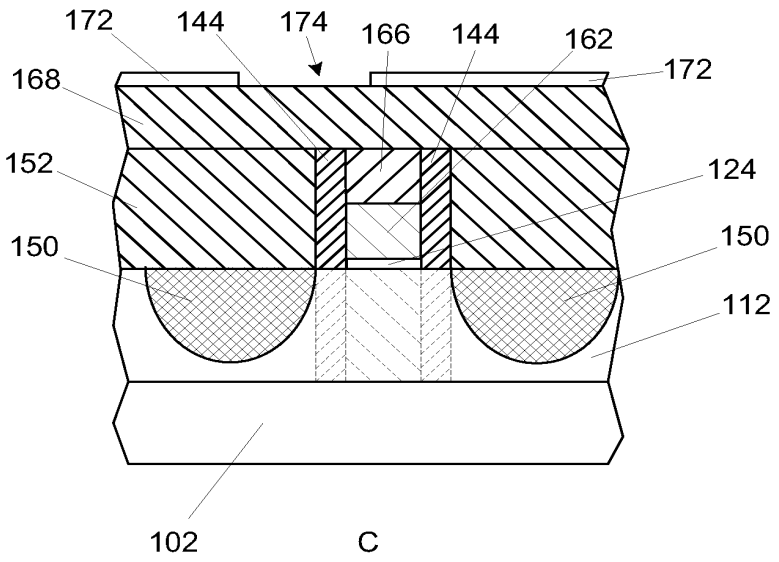

172
144
174
166
144
162
172
168
152
124
150
150
112
102
C

FIG. 21

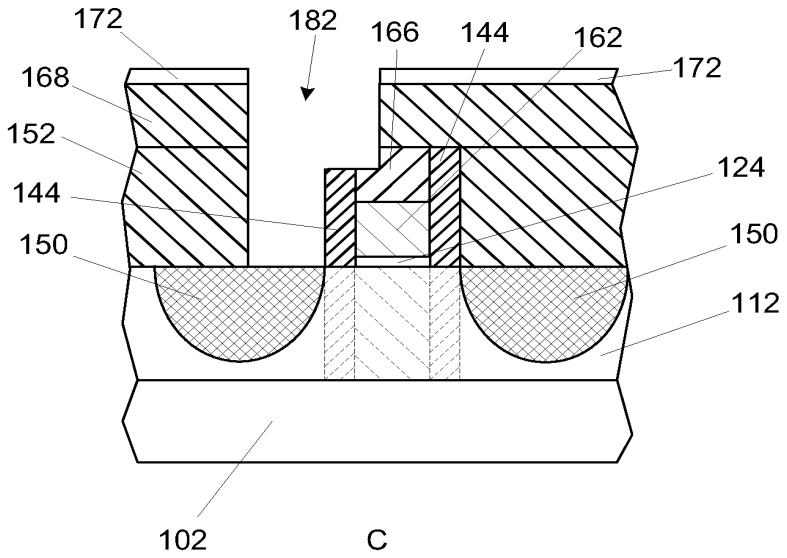

172
182
166
144
162
172
168
152
124
144
150
150
112
102
C

FIG. 22

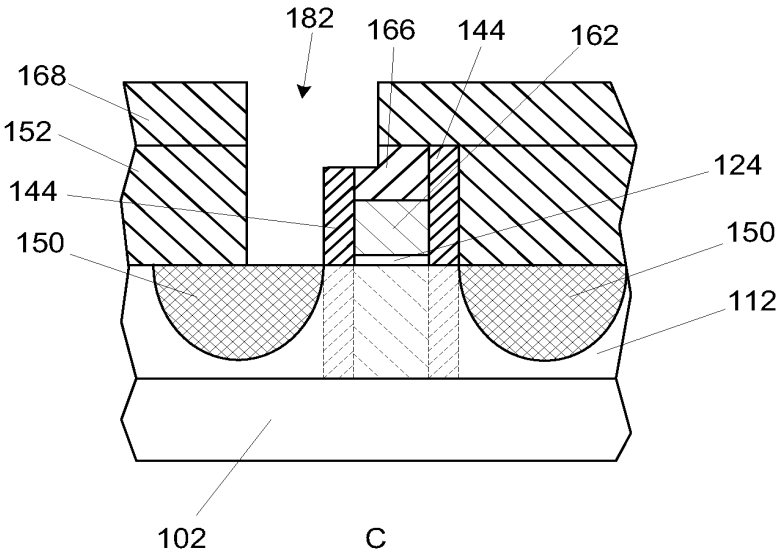

182
166
144
162
168
152
124
144
150
150
112
102
C

FIG. 23

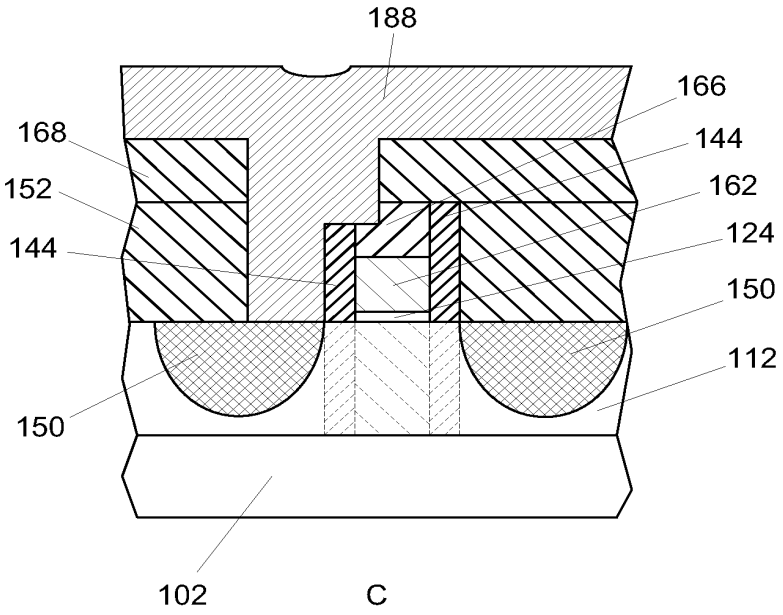

188
166
168
144
152
162
144
124
150
112
150
102
C

FIG. 24

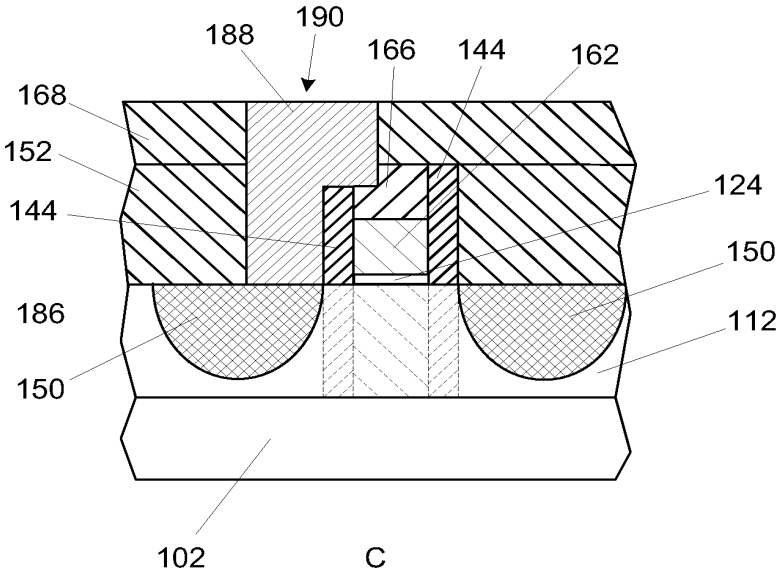

190
188
166
144
162
168
152
124
144
150
186
112
150
102
C

FIG. 25

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

U.S. APPLICATION NUMBER NO.	FIRST NAMED APPLICANT	ATTY. DOCKET NO.
13/992,598	Aaron W. Rosenbaum	P38683US

92265
Winkle, PLLC
c/o CPA Global
P.O. Box 52050
Minneapolis, MN 55402

INTERNATIONAL APPLICATION NO.	
PCT/US11/54464	
I.A. FILING DATE	PRIORITY DATE
09/30/2011	

CONFIRMATION NO. 5215
371 ACCEPTANCE LETTER

OC000000062009146

Date Mailed: 06/18/2013

NOTICE OF ACCEPTANCE OF APPLICATION UNDER 35 U.S.C 371 AND 37 CFR 1.495

The applicant is hereby advised that the United States Patent and Trademark Office in its capacity as a Designated / Elected Office (37 CFR 1.495), has determined that the above identified international application has met the requirements of 35 U.S.C. 371, and is ACCEPTED for national patentability examination in the United States Patent and Trademark Office.

The United States Application Number assigned to the application is shown above and the relevant dates are:

06/07/2013	06/07/2013
DATE OF RECEIPT OF 35 U.S.C. 371(c)(1), (c)(2) and (c)(4) REQUIREMENTS	DATE OF COMPLETION OF ALL 35 U.S.C. 371 REQUIREMENTS

A Filing Receipt (PTO-103X) will be issued for the present application in due course. **THE DATE APPEARING ON THE FILING RECEIPT AS THE " FILING DATE" IS THE DATE ON WHICH THE LAST OF THE 35 U.S.C. 371 (c)(1), (c)(2) and (c)(4) REQUIREMENTS HAS BEEN RECEIVED IN THE OFFICE. THIS DATE IS SHOWN ABOVE.** *The filing date of the above identified application is the international filing date of the international application (Article 11(3) and 35 U.S.C. 363).* Once the Filing Receipt has been received, send all correspondence to the Group Art Unit designated thereon.

The following items have been received:

- Copy of the International Application filed on 06/07/2013
- Copy of the International Search Report filed on 06/07/2013
- Oath or Declaration filed on 06/07/2013
- Request for Immediate Examination filed on 06/07/2013
- U.S. Basic National Fees filed on 06/07/2013
- Authorization to Permit Access filed on 06/07/2013

Applicant is reminded that any communications to the United States Patent and Trademark Office must be mailed to the address given in the heading and include the U.S. application no. shown above (37 CFR 1.5)

KAREN R MCLEAN

Telephone: (571) 272-9093

FORM PCT/DO/EO/903 (371 Acceptance Notice)

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
13/992,598	06/07/2013		2300	P38683US	25	4

CONFIRMATION NO. 5215

92265
Winkle, PLLC
c/o CPA Global
P.O. Box 52050
Minneapolis, MN 55402

FILING RECEIPT

OC000000062009145

Date Mailed: 06/18/2013

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Aaron W. Rosenbaum, Portland, OR;
Din-How Mei, Portland, OR;
Sameer S. Pradhan, Portland, OR;

Applicant(s)

Aaron W. Rosenbaum, Portland, OR;
Din-How Mei, Portland, OR;
Sameer S. Pradhan, Portland, OR;

Power of Attorney: The patent practitioners associated with Customer Number 92265

Domestic Priority data as claimed by applicant

This application is a 371 of PCT/US11/54464 09/30/2011

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access - A proper **Authorization to Permit Access to Application by Participating Offices** (PTO/SB/39 or its equivalent) has been received by the USPTO.

If Required, Foreign Filing License Granted: 06/15/2013
The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/992,598**
Projected Publication Date: 09/26/2013

Non-Publication Request: No

Early Publication Request: No
Title

CAPPING DIELECTRIC STRUCTURE FOR TRANSISTOR GATES

Preliminary Class

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 13/992,598

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	480
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720
TOTAL CLAIMS (37 CFR 1.16(i))	25 minus 20 =	* 5			OR	x 80 =	400
INDEPENDENT CLAIMS (37 CFR 1.16(h))	4 minus 3 =	* 1				x 420 =	420
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	2300

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

MULTIPLE DEPENDENT CLAIM FEE CALCULATION SHEET

Substitute for Form PTO-1360
(For use with Form PTO/SB/06)

Application Number	Filing Date
13992598	

Applicant(s) Aaron Rosenbaum

* May be used for additional claims or amendments

CLAIMS	AS FILED		AFTER FIRST AMENDMENT		AFTER SECOND AMENDMENT	
	Indep	Depend	Indep	Depend	Indep	Depend
1	1					
2		1				
3		1				
4		1				
5	1					
6		1				
7		1				
8		1				
9		1				
10	1					
11		1				
12		1				
13		1				
14		1				
15	1					
16		1				
17		1				
18		1				
19		1				
20		1				
21		1				
22		1				
23		1				
24		1				
25		1				
26						
27						
28						
29						
30						
31						
32						
33						
34						
35						
36						
37						
38						
39						
40						
41						
42						
43						
44						
45						
46						
47						
48						
49						
50						
Total Indep	4		0		0	
Total Depend	21	↵	0	↵	0	↵
Total Claims	25		0		0	

	*		*		*	
	Indep	Depend	Indep	Depend	Indep	Depend
51						
52						
53						
54						
55						
56						
57						
58						
59						
60						
61						
62						
63						
64						
65						
66						
67						
68						
69						
70						
71						
72						
73						
74						
75						
76						
77						
78						
79						
80						
81						
82						
83						
84						
85						
86						
87						
88						
89						
90						
91						
92						
93						
94						
95						
96						
97						
98						
99						
100						

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/992,598	06/07/2013	Aaron W. Rosenbaum	P38683US

CONFIRMATION NO. 5215

92265
Winkle, PLLC
c/o CPA Global
P.O. Box 52050
Minneapolis, MN 55402

PUBLICATION NOTICE

OC000000064032531

Title:CAPPING DIELECTRIC STRUCTURE FOR TRANSISTOR GATES

Publication No.US-2013-0248952-A1
Publication Date:09/26/2013

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently http://pair.uspto.gov/. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99**)		
	Application Number	13992598
	Filing Date	2013-06-07
	First Named Inventor	Rosenbaum, Aaron W.
	Art Unit	2811
	Examiner Name	Unknown
	Attorney Docket Number	P38683US

U.S.PATENTS						
Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	6136697	A	2000-10-24	Wu	
	2	7456471	B2	2008-11-25	Anderson et al.	
	3	7528025	B2	2009-05-05	Brask et al.	
If you wish to add additional U.S. Patent citation information please click the Add button.						
U.S.PATENT APPLICATION PUBLICATIONS						
Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20020130372	A1	2002-09-19	Kwon et al.	
	2	20060189058	A1	2006-08-24	Lee et al.	
	3	20110147831	A1	2011-06-23	Steigerwald et al.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	13992598
	Filing Date	2013-06-07
	First Named Inventor	Rosenbaum, Aaron W.
	Art Unit	2811
	Examiner Name	Unknown
	Attorney Docket Number	P38683US

	4	20080233699	A1	2008-09-25	Booth et al.	
	5	20100048007	A1	2010-02-25	Lee et al.	

If you wish to add additional U.S. Published Application citation information please click the Add button.

FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2]	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	100585178	KR	B1	2006-05-24	Kim et al.	English Abstract Submitted	☐
	2	10-0653711	KR	B1	2006-12-05	Kim et al.	English Abstract Submitted	☐
	3	10-2004-0050519	KR	A	2004-06-16	Lee	English Abstract Submitted	☐
	4	10-2008-0021918	KR	A	2008-03-10	Shin	English Abstract Submitted	☐
	5	2013/048449	WO	A1	2013-04-04	Pradhan et al.		☐
	6	2013/048516	WO	A1	2013-04-04	Rosenbaum et al.		☐
	7	2013/048524	WO	A1	2013-04-04	Pradhan et al.		☐

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	13992598
	Filing Date	2013-06-07
	First Named Inventor	Rosenbaum, Aaron W.
	Art Unit	2811
	Examiner Name	Unknown
	Attorney Docket Number	P38683US

	8	2013/085490	WO	A1	2013-06-13	Pradhan et al.		☐

If you wish to add additional Foreign Patent Document citation information please click the Add button

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	International Search Report and Written Opinion Received for PCT Patent Application No. PCT/US2011/054294, Mailed on May 15, 2012, 8 pages.	☐
	2	International Search Report and Written Opinion Received for PCT Patent Application No. PCT/US2011/054464, Mailed on May 15, 2012, 9 pages.	☐
	3	International Search Report and Written Opinion Received for PCT Patent Application No. PCT/US2011/054479, Mailed on May 16, 2012, 9 pages.	☐
	4	International Search Report and Written Opinion Received for PCT Patent Application No. PCT/US2011/063433, Mailed on July 20, 2012, 9 pages.	☐

If you wish to add additional non-patent literature document citation information please click the Add button

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	13992598
	Filing Date	2013-06-07
	First Named Inventor	Rosenbaum, Aaron W.
	Art Unit	2811
	Examiner Name	Unknown
	Attorney Docket Number	P38683US

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Robert G. Winkle/	Date (YYYY-MM-DD)	2013-10-23
Name/Print	Robert G. Winkle	Registration Number	37,474

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

(19) KOREAN INTELLECTUAL PROPERTY OFFICE

KOREAN PATENT ABSTRACTS

(11) Registration number: 100585178 B1
(45) Issue date: 30.05.2006
(24) Registration date: 24.05.2006

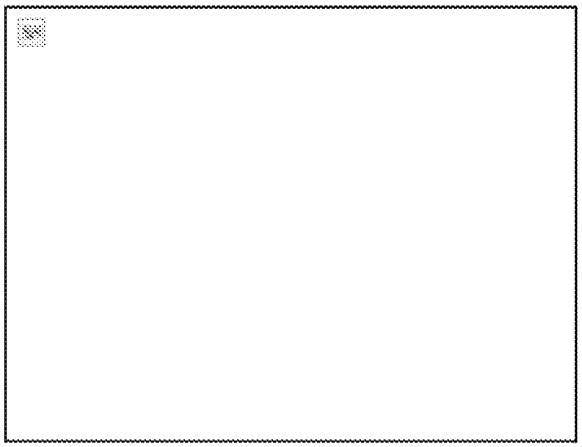
(21) Application number: 1020050011018
(22) Application date: 05.02.2005

(51) Int. Cl: H01L 21/336
H01L 27/12

(73) Proprietor:

(72) Inventor:
- KIM, SUNG MIN
- KIM, DONG WON
- KIM, MIN SANG
- YUN, EUN JUNG

(54) SEMICONDUCTOR DEVICE INCLUDING FinFET HAVING METAL GATE ELECTRODE AND MANUFACTURING METHOD THEREOF USING CENTRAL TRENCH



(57) Abstract:

PURPOSE: A semiconductor device including a FinFET(Fin Field Effect Transistor) having a metal gate electrode and its manufacturing method are provided to prevent decrease of source/drain regions by using a central trench formed on a center of an active region.

CONSTITUTION: An active region is formed on a semiconductor substrate(10) and protruded more than a surface of the substrate. A central trench is formed on a center of the active region. A fin has a first protrusion and a second protrusion which are in parallel to each other and made of a surface of the active region. The fin uses upper surfaces and sides of the first protrusion and the second protrusion as a channel region. A gate dielectric is formed on the active region having the fin. A metal gate electrode (80) is formed on the gate dielectric. A gate spacer (65) is formed on a sidewall of the metal gate electrode. A source and a drain are formed on the active region at both sides of the metal gate electrode. The metal gate electrode includes a barrier layer(72a) connected to the gate spacer and the gate dielectric and a metal layer(74a) on an upper portion of the barrier layer.

copyright KIPO 2006

(19)대한민국특허청(KR)
(12) 등록특허공보(B1)

(51) 。Int. Cl.
H01L 21/336 (2006.01)
H01L 27/12 (2006.01)

(45) 공고일자 2006년05월30일
(11) 등록번호 10-0585178
(24) 등록일자 2006년05월24일

(21) 출원번호 10-2005-0011018
(22) 출원일자 2005년02월05일

(65) 공개번호
(43) 공개일자

(73) 특허권자 삼성전자주식회사
경기도 수원시 영통구 매탄동 416

(72) 발명자 김성인
인천 부평구 부개3동 삼부아파트 108동 2204호

김동원
경기 성남시 분당구 정자동 192번지 정든마을 506동 1602호

김민상
서울 동작구 신대방1동 696-15

윤은정
서울 서초구 잠원동 신반포한신아파트 323동 403호

(74) 대리인 리엔목특허법인
이해영

(56) 선행기술조사문헌
JP63094668 A
KR1020050035712 A
KR1020060000275 A
KR100521377 B1
KR1020050056858 A
* 심사관에 의하여 인용된 문헌

심사관 : 오창석

(54) 금속 게이트 전극을 가지는 F i n F E T을 포함하는반도체 소자 및 그 제조방법

요약

본 발명에 따른 반도체 소자는, 반도체 기판에 형성되고 기판 표면보다 돌출된 활성영역을 가진다. 활성영역에는 그 중심부에 형성된 중심 트렌치를 사이에 두고 활성영역 표면으로 이루어진 서로 평행한 제1 돌출부 및 제2 돌출부를 가지며 제1 돌출부와 제2 돌출부의 상부면들 및 측면들을 채널 영역으로 이용하는 핀이 형성되어 있다. 이러한 핀을 가지는 활성영역 상에는 게이트 절연막과 금속 게이트 전극이 형성되어 있다. 금속 게이트 전극 측벽 상에는 게이트 스페이서가 구비되어 있으며, 금속 게이트 전극 양 옆의 활성영역에는 소오스와 드레인이 형성되어 있다. 특히, 금속 게이트 전극은 게이트 스페이서 및 게이트 절연막에 접하는 배리어막과 상기 배리어막 상부의 금속막을 포함한다.

대표도

도 14

명세서

도면의 간단한 설명

도 1은 본 발명에 따른 반도체 소자의 제조방법의 실시예들에서 제조하려고 하는 반도체 소자의 레이아웃이다.

도 2 내지 도 10, 도 12 내지 도 14는 도 1과 같은 레이아웃을 가지는 반도체 소자의 제조방법의 제1 실시예를 설명하기 위한 공정 단계별 중간 구조물들을 도시한다.

도 11은 도 10의 Y 방향 단면도이고 도 15는 도 14의 Y 방향 단면도이다.

도 16은 본 발명의 제2 실시예에 따른 반도체 소자의 단면도이다.

도 17은 본 발명의 제3 실시예에 따른 반도체 소자의 제조방법을 설명하기 위한 중간 구조물을 도시한다.

도 18은 65nm TiN/W 게이트 전극을 가지는 FinFET SRAM 셀 트랜지스터의 SEM 이미지와 TEM 이미지이다.

도 19는 본 발명에서와 같은 TiN/W 전극을 가지는 FinFET, 종래 폴리실리콘 게이트 전극을 가지는 FinFET 및 종래 폴리실리콘 게이트 전극을 가지는 플래너(planar) MOSFET의 드레인 전류(I_D)-게이트 전압(V_G) 그래프이다.

도 20은 본 발명에서와 같은 TiN/W 전극을 가지는 FinFET, 종래 폴리실리콘 게이트 전극을 가지는 FinFET 및 종래 폴리실리콘 게이트 전극을 가지는 플래너 MOSFET의 구동전류 그래프이다.

도 21은 본 발명의 제조방법에 따른 카운터 도핑(counter doping)의 효과를 보이는 그래프이다.

발명의 상세한 설명

발명의 목적

발명이 속하는 기술 및 그 분야의 종래기술

본 발명은 반도체 소자 및 그 제조방법에 관한 것으로, 보다 상세하게는 FinFET(Fin Field Effect Transistor)을 포함하는 반도체 소자 및 그 제조방법에 관한 것이다.

반도체 소자 성능을 향상시키고 제조 비용을 절감하기 위해 반도체 소자의 밀도를 지속적으로 증가시키고 있다. 소자 밀도를 증가시키기 위해, 반도체 소자의 피쳐 사이즈(feature size)를 감소시킬 수 있는 기술이 필요하다.

그동안 반도체 소자의 제조 공정에서는 반도체 소자의 속도 및 집적도를 향상시키기 위해서 MOSFET(Metal-Oxide-Semiconductor Field Effect Transistor) 채널 길이를 짧게 하여 왔다. 그러나, 이런 경우 소자의 소오스와 드레인 사이의 간격이 극히 짧아짐에 따른 단채널 효과(short channel effect)로 인하여 소오스와 채널 전위가 드레인 전위의 영향을 받는 것을 효율적으로 억제하기가 어려워지는 등 소자의 능동 스위치로서의 특성 열화를 가져오게 된다. 그러나, 반도체 표면에 평행하게 채널이 형성되는 종래의 MOSFET은 플래너(planar) 채널 소자이기 때문에 구조적으로 소자 크기의 축소화에 불리할 뿐만 아니라, 단채널 효과의 발생을 억제하기가 어렵다.

FinFET은 핀(fin : 물고기의 지느러미) 형태의 입체적인 활성영역 형성 후 게이트가 핀의 양측면과 상면을 감싸는 트리-게이트(tri-gate) 구조가 되게 함으로써 평면이 아닌 삼차원 구조의 채널을 이용하는 것이다. 이러한 구조는 플래너

MOSFET과는 달리 기판 표면에 수직한 채널을 구비하여 소자 크기의 축소화에 유리할 뿐만 아니라, 드레인의 집합 정전 용량을 크게 줄여 단채널 효과를 줄일 수 있는 장점이 있다. 이러한 장점을 이용하고자 기존의 MOSFET을 FinFET으로 대체하려는 노력이 진행되고 있다. 예컨대 미국특허 제6,391,782호, 제6,664,582호 등이 있다.

그러나 종래의 FinFET은 얇은 바디 효과 때문에 문턱전압이 낮아 성능의 열화없이 CMOS 회로 동작을 달성하기가 어렵다. 이러한 문제를 해결하기 위해 듀얼 금속 게이트 공정, 게이트에 이온주입을 실시한 단일 금속 게이트 공정, 및 전체가 실리사이드화된 게이트 공정과 같은 게이트 일함수 엔지니어링이 제안되었지만 CMOS 동작에서 실현하기에는 아직 어려움이 많다.

발명이 이루고자 하는 기술적 과제

본 발명이 이루고자 하는 기술적 과제는 저전압 고성능 구동에 적당한 문턱전압을 가지는 FinFET을 포함하는 반도체 소자를 제공하는 것이다.

본 발명이 이루고자 하는 다른 기술적 과제는 저전압 고성능 구동에 적당한 문턱전압을 가지는 FinFET을 포함하는 반도체 소자를 쉽게 제조하는 방법을 제공하는 것이다.

발명의 구성 및 작용

상기 기술적 과제를 달성하기 위한 본 발명에 따른 반도체 소자는, 반도체 기판에 형성되고 상기 기판 표면보다 돌출된 활성영역을 가진다. 상기 활성영역 중심부에는 형성된 중심 트렌치를 사이에 두고 상기 활성영역 표면으로 이루어진 서로 평행한 제1 돌출부 및 제2 돌출부를 가지며 상기 제1 돌출부와 제2 돌출부의 상부면들 및 측면들을 채널 영역으로 이용하는 핀이 형성되어 있다. 상기 핀을 가지는 활성영역 상에는 게이트 절연막이 형성되어 있고, 상기 게이트 절연막 상에는 금속 게이트 전극이 형성되어 있다. 상기 금속 게이트 전극 측벽 상에는 게이트 스페이서가 구비되어 있으며, 상기 금속 게이트 전극 양 옆의 상기 활성영역에는 소오스와 드레인이 형성되어 있다. 특히, 상기 금속 게이트 전극은 상기 게이트 스페이서 및 상기 게이트 절연막에 접하는 배리어막과 상기 배리어막 상부의 금속막을 포함한다.

본 발명에 따른 반도체 소자에 있어서, 상기 배리어막은 TiN막이고 상기 금속막은 W막인 것이 바람직하다. 상기 핀의 하부에는 채널 이온주입이 되어 있고 상기 핀의 상부에는 상기 채널 이온주입의 불순물과 반대되는 도전형의 불순물이 주입되어 있는 것이 바람직하다. 상기 활성영역 주위에는 상기 중심 트렌치 바닥과 동일한 표면 높이를 갖는 소자분리막을 더 포함할 수 있다. 대신에, 소자분리막은 상기 중심 트렌치 바닥보다는 높고 상기 활성영역 표면보다는 낮은 표면 높이를 갖는 것일 수도 있다. 상기 금속 게이트 전극은 상기 중심 트렌치와 동일하거나 더 넓은 폭을 가지고 상기 제1 돌출부 및 제2 돌출부의 상부면들 및 측면들을 덮으면서 신장한다. 상기 게이트 절연막은 실리콘 산화막, 하프늄 산화막, 지르코늄 산화막, 알루미늄 산화막, 실리콘 질화막 또는 실리콘 산화질화막일 수 있다. 상기 금속 게이트 전극의 너비보다 상기 소오스 및 드레인에 형성되는 콘택 영역의 너비가 클 수 있으며, 상기 반도체 기판은 실리콘 웨이퍼, SOI(Silicon-On-Insulator) 기판, SGOI(Silicon Germanium-On-Insulator) 기판 또는 실리콘 저메늄(SiGe) 웨이퍼일 수 있다.

상기 다른 기술적 과제를 달성하기 위한 본 발명에 따른 반도체 소자의 제조방법의 일 태양에서는, 반도체 기판에 상기 기판 표면보다 돌출된 활성영역을 정의한다. 상기 활성영역 중심부를 식각하여 중심 트렌치를 형성함으로써, 상기 중심 트렌치를 사이에 두고 상기 활성영역 표면으로 이루어진 서로 평행한 제1 돌출부 및 제2 돌출부를 가지며 상기 제1 돌출부와 제2 돌출부의 상부면들 및 측면들을 채널 영역으로 이용하는 핀을 형성한다. 상기 핀을 가지는 상기 활성영역 상에 게이트 절연막을 형성한 다음, 상기 게이트 절연막 상에 더미 게이트 전극을 형성한다. 상기 더미 게이트 전극 측벽에 게이트 스페이서를 형성한 후, 상기 더미 게이트 전극 양 옆의 상기 활성영역에 소오스 및 드레인을 형성한다. 상기 반도체 기판에 절연막을 증착한 후 상기 더미 게이트 전극 상면이 드러나도록 평탄화하고 상기 더미 게이트 전극을 제거한다. 그런 다음, 상기 더미 게이트 전극이 제거된 영역에 금속 게이트 전극을 형성한다.

상기 다른 기술적 과제를 달성하기 위한 본 발명에 따른 반도체 소자의 제조방법의 다른 태양에서는, 반도체 기판 상에 활성영역 하드 마스크를 형성한 다음, 상기 활성영역 하드 마스크를 식각 마스크로 하여 상기 기판을 식각함으로써, 상기 기판 표면보다 돌출된 활성영역을 정의하고, 상기 활성영역을 둘러싸는 트렌치를 형성한다. 상기 활성영역 하드 마스크를 등방성 식각하여 상기 활성영역의 가장자리를 노출시키는 하드 마스크 패턴을 형성한 다음, 상기 트렌치 안에 갭 필(gap fill) 산화막을 채우고 상기 하드 마스크 패턴을 평탄화 종료점으로 하여 평탄화한다. 상기 갭 필 산화막과 하드 마스크 패턴을 라인 타입으로 패터닝하여 중심에 적어도 하나의 채널 영역 정의 패턴을 포함하는 더미 패턴을 형성한 후, 상기 더미 패턴 위로 차단막을 증착하고 상기 채널 영역 정의 패턴을 평탄화 종료점으로 하여 평탄화한다. 상기 차단막의 평탄화 단계에 의해 드러나 있는 상기 채널 영역 정의 패턴을 제거하여 상기 활성영역 표면을 노출시키는 개구부를 형성한 다음, 상기 개

구부 아래에 있는 상기 활성영역을 식각하여 핀 채널로 사용될 부위에 중심 트렌치를 형성한다. 상기 차단막과 갭 필 산화막을 리세스시켜 드러난 상기 활성영역 측벽으로 소자분리막을 형성하고, 상기 활성영역에서 상기 중심 트렌치와 상기 소자분리막 사이에 상기 기판 표면으로 이루어지고 상기 중심 트렌치를 사이에 두고 서로 평행한 제1 돌출부 및 제2 돌출부를 가지며 상기 제1 돌출부와 제2 돌출부의 상부면들 및 측면들을 채널 영역으로 이용하는 핀을 노출시킨다. 상기 핀을 가지는 상기 활성영역 상에 게이트 절연막을 형성한 후, 상기 게이트 절연막 상에 더미 게이트 전극을 형성한다. 상기 더미 게이트 전극 측벽에 게이트 스페이서를 형성하고 나서, 상기 더미 게이트 전극 양 옆의 상기 활성영역에 소오스 및 드레인을 형성한다. 상기 반도체 기판에 절연막을 증착한 후 상기 더미 게이트 전극 상면이 드러나도록 평탄화한다. 상기 더미 게이트 전극을 제거한 다음, 상기 더미 게이트 전극이 제거된 영역에 금속 게이트 전극을 형성한다.

이 두 번째 태양에 있어서, 상기 활성영역 하드 마스크는 실리콘 질화막으로 형성하고 상기 등방성 식각은 인산(H_3PO_4)을 이용한 습식 식각으로 실시할 수 있다. 상기 등방성 식각은 습식 식각 또는 플라즈마를 이용한 건식 식각으로 실시할 수 있다. 이때, 상기 등방성 식각 시간을 조절함으로써 상기 핀의 너비를 조절한다. 상기 갭 필 산화막 평탄화에는 CMP (Chemical Mechanical Polishing) 또는 전면 식각(blanket etch)을 이용할 수 있다. 상기 차단막은 실리콘 산화막으로 형성하는 것이 바람직하다. 상기 차단막의 평탄화에는 CMP 또는 전면 식각을 이용할 수 있다. 상기 게이트 절연막은 열산화 방법으로 실리콘 산화막을 성장시켜 형성하거나 ALD(Atomic Layer Deposition), CVD, PE-ALD(Plasma Enhanced-ALD) 또는 PE-CVD 방법으로 실리콘 산화막, 하프늄 산화막, 지르코늄 산화막, 알루미늄 산화막, 실리콘 질화막 또는 실리콘 산화질화막을 증착하거나 코팅 방법으로 형성할 수 있다. 상기 차단막과 갭 필 산화막을 상기 중심 트렌치 바닥과 동일한 높이까지 리세스시키거나 상기 중심 트렌치 바닥보다 높은 높이로 리세스시킬 수 있다. 상기 계구부를 형성하는 단계 이후 상기 계구부 내벽에 스페이서를 형성하는 단계를 더 포함하여 상기 중심 트렌치를 형성할 때에 이용한 다음 이를 제거할 수도 있다. 여기서의 스페이서는 실리콘 질화막으로 형성하는 것이 바람직하다.

본 발명에 따른 반도체 소자의 제조방법들에 있어서, 상기 더미 게이트 전극을 제거한 다음 상기 더미 게이트 전극이 제거된 영역에 제2의 게이트 절연막을 형성하는 단계를 더 포함할 수 있다. 상기 반도체 기판에 절연막을 증착한 후 상기 더미 게이트 전극 상면이 드러나도록 평탄화하는 단계는 CMP를 이용하는 것이 바람직하다. 상기 절연막은 HDP-CVD로 증착한 산화막인 것이 바람직하다. 상기 금속 게이트 전극을 형성하는 단계는, 상기 게이트 스페이서와 게이트 절연막에 접하는 배리어막을 형성하는 단계, 상기 배리어막 상에 금속막을 형성하는 단계, 및 상기 배리어막과 금속막을 CMP와 같은 방법으로 평탄화하는 단계를 포함할 수 있다. 상기 배리어막은 TiN막이고 상기 금속막은 W막인 것이 바람직하다. 상기 금속 게이트 전극은 상기 중심 트렌치와 동일하거나 더 넓은 폭을 가지고 상기 제1 돌출부 및 제2 돌출부의 상부면들 및 측면들을 덮으면서 신장하도록 형성할 수 있다. 상기 금속 게이트 전극의 너비보다 상기 소오스 및 드레인에 형성되는 콘택 영역의 너비가 크게 형성할 수 있다. 상기 활성영역을 정의하는 단계 다음에, 상기 활성영역 하부에 채널 이온주입을 수행하는 단계, 및 상기 활성영역 상부에 상기 채널 이온주입의 불순물과 반대되는 도전형의 불순물을 주입하는 단계를 더 포함할 수 있다.

본 발명의 이점 및 특징, 그리고 그것들을 달성하는 방법은 첨부되는 도면과 함께 상세하게 후술되어 있는 실시예들을 참조하면 명확해질 것이다. 그러나 본 발명은 이하에서 게시되는 실시예들에 한정되는 것이 아니라 서로 다른 다양한 형태로 구현될 것이며, 단지 본 실시예들은 본 발명의 게시가 완전하도록 하며, 통상의 지식을 가진 자에게 발명의 범주를 완전하게 알려주기 위해 제공되는 것이며, 본 발명은 청구항의 범주에 의해 정의될 뿐이다. 명세서 전체에 걸쳐 동일 참조 부호는 동일 구성 요소를 지칭한다.

제1 실시예

도 1은 본 발명의 제1 내지 제3 실시예에 따른 반도체 소자의 제조방법으로 제조하려고 하는 반도체 소자의 레이아웃이다.

도 1을 참조하면, 일 방향, 예컨대 X 방향으로 길쭉하게 신장하고 이 신장 방향과 직교하는 Y 방향으로는 A1의 소정 선폭을 가지는 활성영역(20)이 정의되어 있다. 활성영역(20) 위로는 Y 방향으로 신장하는 금속 게이트 전극(80)이 형성된다. 금속 게이트 전극(80) 양 옆의 활성영역(20) 안에는 소오스(S)와 드레인(D)이 형성된다.

도 1에서 볼 수 있는 바와 같이, 금속 게이트 전극(80)의 너비(X 방향 단면 길이)보다 소오스(S) 및 드레인(D)에 형성되는 콘택 영역의 너비가 크다. 본 발명에서는 이렇게 레이아웃을 설계할 수 있음으로 해서, 종래 패터닝 상의 문제로 인해 소오스/드레인 콘택 영역 확보에 제한이 있던 문제를 해결할 수 있다. 그러나, 본 발명에 따른 반도체 소자의 레이아웃에 반드시 도 1에 한정되는 것은 아니다. 예를 들어, 금속 게이트 전극(80)의 너비(X 방향 단면 길이)가 소오스(S) 및 드레인(D)에 형성되는 콘택 영역의 너비보다 클 수도 있다.

도 2 내지 도 9는 여러한 레이아웃을 가지는 반도체 소자 제조방법의 제1 실시예를 설명하기 위한 사시도들이다. 각 도면은 공정 단계별 중간 구조물을 도시한다.

먼저, 도 2를 참조하여, 도 1과 같은 활성영역(20)을 정의할 수 있도록 p형 벌크 실리콘 웨이퍼와 같은 반도체 기판(10) 상에 활성영역 하드 마스크(15)를 형성한다. 반도체 기판(10)으로는 실리콘 웨이퍼 이외에 SOI(Silicon-On-Insulator) 기판, SGOI(Silicon Germanium-On-Insulator) 기판 또는 실리콘 저매늄(SiGe) 웨이퍼를 이용하여도 된다. 활성영역 하드 마스크(15)는 실리콘 질화막과 같은 절연막을 PE-CVD(Plasma Enhanced-Chemical Vapor Deposition) 또는 LP-CVD(Low Pressure-CVD)와 같은 방법으로 기판(10) 상에 800Å 내지 2000Å 두께로 증착한 다음 소정 형상으로 패터닝하여 형성한다. 도시한 바와 같이 활성영역 하드 마스크는 Y방향으로는 A1이라는 소정 선폭을 가지고 X 방향으로 신장하게 형성된다. 활성영역 하드 마스크(15)와 기판(10) 사이의 응력 발생이 우려되는 경우, 활성영역 하드 마스크(15)와 기판(10) 사이에 열산화 방식으로 형성한 산화막을 더 형성할 수도 있다.

그런 다음, 활성영역 하드 마스크(15)를 식각 마스크로 하여 기판(10)을 식각함으로써, 필 영역 및 주변회로 영역에 기판(10) 표면보다 돌출된 활성영역(20)을 정의하고 활성영역(20)을 둘러싸는 트렌치(18)를 형성한다. 트렌치(18)의 깊이는 1000Å 내지 3000Å 정도로 할 수 있다. 기판(10)의 식각에는 예컨대 HBr 또는 Cl_2와 같은 할로겐 가스와 산소를 혼합하여 사용하는 건식 식각을 이용할 수 있다.

도 3을 참조한 단계에서, 활성영역 하드 마스크(15)를 등방성 식각하여 활성영역(20)의 가장자리를 노출시키는 하드 마스크 패턴(15a)을 형성한다. 여기서의 등방성 식각은 식각 마스크를 이용하지 않는 전면 식각(blanket etch)으로 활성영역 하드 마스크(15)를 식각하는 것으로, 풀 백(pull back)이라고도 한다. 활성영역 하드 마스크(15)가 실리콘 질화막으로 이루어진 경우에는 인산(H_3PO_4)을 이용한 습식 식각으로 실시하거나 플라즈마를 이용한 건식 식각으로 실시할 수 있다. 이렇게 하여, 활성영역 하드 마스크(15)보다 X 및 Y 방향 선폭이 축소된 하드 마스크 패턴(15a)을 형성한다. 하드 마스크 패턴(15a)의 Y 방향 선폭은 A1'가 된다고 하면, A1-A1'가 나중에 채널로 사용될 핀의 너비를 결정한다. 하드 마스크 패턴(15a)의 A1'가 작을수록 나중에 핀의 너비가 커지므로, 등방성 식각(풀 백) 시간을 적절히 조절함으로써 핀의 너비를 조절하도록 한다.

도 4를 참조하여, 트렌치(18) 안에 절연 물질, 예컨대 갭 필(gap fill) 산화막(30)을 채우고 하드 마스크 패턴(15a)을 평탄화 종료점으로 하여 평탄화한다. 갭 필 산화막(30) 증착에는 예컨대 HDP(High Density Plasma)-CVD를 이용할 수 있고, 갭 필 산화막(30) 평탄화에는 CMP 또는 전면 식각을 이용할 수 있다.

도 5를 참조하여 도 1과 같은 Y 방향으로 신장하는 금속 게이트 전극(80) 위치에 더미 패턴(35)이 형성되도록, 갭 필 산화막(30)과 하드 마스크 패턴(15a)을 패터닝한다. 이 때, 갭 필 산화막(30)과 하드 마스크 패턴(15a)에 대해 동일 내지 유사한 식각선택비 조건으로 식각하는 방법에 의할 수 있다. 더미 패턴(35) 형성에 의해, 하드 마스크 패턴(15a)의 대부분이 제거되고 활성영역(20) 중심에는 하나의 채널 영역 정의 패턴(15b)이 형성되며, 더미 패턴(35) 아래로 활성영역(20)이 일부 드러나게 된다.

도 6을 참조하면, 더미 패턴(35) 위로 실리콘 산화막과 같은 차단막(40)을 증착하고 채널 영역 정의 패턴(15b)을 평탄화 종료점으로 하여 평탄화한다. 차단막(40)의 증착에는 갭 필 산화막(30) 증착에 이용된 HDP-CVD를 이용할 수 있다. 그리고, 차단막(40)의 평탄화에는 CMP 또는 전면 식각을 이용할 수 있다. 차단막(40)과 갭 필 산화막(30)은 유사 또는 동일 종류의 산화막이므로 둘 사이의 계면은 실제로는 존재하지 않는다. 다만 이해를 돕기 위해 가상의 계면 위치를 점선으로 도시하였다.

도 7을 참조하여, 도 6의 평탄화 단계에 의해 드러나 있던 채널 영역 정의 패턴(15b)을 습식 또는 건식 식각의 방법으로 차단막(40), 갭 필 산화막(30) 및 기판(10)에 대해 선택적으로 제거한다. 실리콘 질화막으로 이루어진 채널 영역 정의 패턴(15b)을 습식으로 제거할 때에는 인산 스트립을 이용할 수 있다. 이렇게 하여, 채널 영역 정의 패턴(15b)이 있던 자리에는 개구부(45)가 형성되고 그 아래 기판(10) 표면, 즉 활성영역(20) 표면이 일부 노출된다. 그런 다음, 차단막(40)과 갭 필 산화막(30)을 식각 마스크로 하여 개구부(45) 아래에 있는 활성영역(20)을 식각하여 핀 채널로 사용될 부위를 한정한다. 앞에서도 이미 언급한 바와 같이, 핀 영역의 핀의 너비는 활성영역(20)의 Y 방향 선폭 A1과 하드 마스크 패턴(15a)의 Y 방향 선폭 A1'간의 차이, 즉 활성영역 하드 마스크(15)의 Y 방향 선폭 A1과 채널 영역 정의 패턴(15b)의 Y 방향 선폭 A1'간의 차이 A1-A1' 만큼으로 결정된다. 여기서 개구부(45) 아래에 있는 활성영역(20)을 식각하여 핀 채널로 사용될 부위를 한정하기 전에 채널 이온주입을 실시할 수 있는데, 바람직하게는 핀 하부(B)에 주입하는 불순물의 도전형과 핀 상부(A)에 주입

하는 불순물의 도전형을 반대로 한다. 이것을 카운터 도핑(counter doping)이라고 한다. 이렇게 반대되는 도전형의 불순물을 주입함에 따라 off-누설전류를 증가시키지 않고 문턱전압을 낮출 수 있게 된다. 이 때의 이온주입은 경사각없이 기판(10)에 대해 수직으로 실시한다.

도 8을 참조하여, 차단막(40)과 갭 필 산화막(30)을 패널 깊이와 같은 깊이가 되게 리세스시킨다. 차단막(40)과 갭 필 산화막(30)을 습식으로 리세스시킬 때에는 HF 희석액이나 BOE(Buffered Oxide Etchant) 용액을 이용할 수 있다. 이렇게 하면 드러난 활성영역(20) 주위로 소자분리막(30a)이 형성된다. 그리고, 활성영역(20)에는 도 7을 참조하여 설명한 단계에서 개구부(45)를 통한 식각에 의해 된 채널 부위에 중심 트렌치(22)가 파여져 있게 된다. 이에 따라, 활성영역(20)은 중심 트렌치(22)와 소자분리막(30a) 사이에 기판(10) 표면으로 이루어지는 제1 돌출부(23) 및 제2 돌출부(24)가 노출된다. 제1 돌출부(23) 및 제2 돌출부(24)의 상부면들 및 측면들은 삼차원 구조 채널 영역을 제공하고, 중심 트렌치(22)를 사이에 두고 서로 평행하다.

한편, 도 7을 참조하여 설명한 단계에서의 채널 이온주입을 실시하지 않은 경우에는, 도 8의 단계에서 핀을 노출시킨 다음에 실시할 수도 있다. 이 때에도 바람직하게는 핀 하부(B)와 상부(A)에 반대되는 도전형의 불순물로 주입하며, 이 경우에는 경사 이온주입으로 실시한다.

도 9를 참조하여, 활성영역(20) 상에 10Å 내지 70Å의 게이트 절연막(50)을 형성한다. 게이트 절연막(50)은 열산화 방법으로 실리콘 산화막을 성장시켜 형성할 수 있다. 대신에, ALD(Atomic Layer Deposition), CVD, PE-ALD(Plasma Enhanced-ALD) 또는 PE-CVD 방법으로 절연 물질, 예컨대 실리콘 산화막, 하프늄 산화막, 지르코늄 산화막, 알루미늄 산화막, 실리콘 질화막 또는 실리콘 산화질화막을 증착하거나 코팅 방법으로 형성할 수 있다. 그런 다음, 게이트 절연막(50) 위로 도 1의 금속 게이트 전극(80)과 같은 모양대로 더미 게이트 전극(60)을 형성한다. 더미 게이트 전극(60)은 언도프트 또는 도프트 폴리실리콘막으로 형성한 다음 Y 방향으로 신장하게 패터닝하여 형성한다. 여기서, 더미 게이트 전극(60)은 중심 트렌치(22)와 동일하거나 더 넓은 폭을 가지면서 채널 영역, 즉 제1 돌출부(23) 및 제2 돌출부(24)의 상부면들 및 측면들을 덮으면서 채널 영역을 가로지르도록 형성한다. 중심 트렌치(22)의 크기는 개구부(45)의 크기에 의해 결정되고, 개구부(45)의 크기는 채널 영역 정의 패턴(15b)의 크기에 의해 결정된다. 따라서, 소오스(S) 및 드레인(D)의 각 면적을 증가시키기 위해서는 채널 영역 정의 패턴(15b)의 크기가 가능한 한 작아야 한다. 본 실시예는 채널 영역 정의 패턴(15b)의 폭보다 더미 게이트 전극(60)의 폭이 넓은 경우를 예로 든다.

계속하여, 도 10에서와 같이 더미 게이트 전극(60)의 측벽에 게이트 스페이서(65)를 형성한다. 게이트 스페이서(65)는 실리콘 질화막으로 형성할 수 있다. 더미 게이트 전극(60)과 게이트 스페이서(65)를 이용한 자기정렬 방법으로 소오스/드레인 이온주입 후 열처리까지 진행하고 나면, 더미 게이트 전극(60) 양 옆의 활성영역(20)에 소오스(S)와 드레인(D)이 형성된다. 이 때, 테이아웃 설계상 더미 게이트 전극(60)의 너비보다 소오스(S) 및 드레인(D)에 형성되는 콘택 영역(미도시)의 너비가 크다. 따라서, 종래와 달리 소오스 및 드레인의 콘택 면적이 제한받지 않는다. 소오스(S)와 드레인(D)은 LDD (Lightly Doped Drain) 타입이 되게 형성할 수도 있으며, 그럴 경우 게이트 스페이서(65)는 고농도(E15/㎠ 수준) 이온주입과 저농도(E12/㎠ ~ E13/㎠ 수준)의 이온주입 사이에 형성한다.

도 11은 도 10의 Y 방향 단면도이다. 도 11에서 볼 수 있는 바와 같이, 도 8의 단계에서 차단막(40)과 갭 필 산화막(30)을 채널 깊이와 같은 깊이가 되게 리세스시키므로, 중심 트렌치(22)의 바닥은 소자분리막(30a) 표면과 같은 높이가 된다. 핀 하부(B)와 상부(A)에는 반대되는 도전형의 불순물이 주입되어 있다.

다음으로 도 12에서와 같이 반도체 기판(10)에 절연막(70)을 증착한 후 더미 게이트 전극(60) 상면이 드러나도록 평탄화한다. 절연막(70)으로는 HDP-CVD로 증착한 산화막을 형성할 수 있고 절연막(70)의 평탄화에는 CMP를 이용할 수 있다.

그런 다음, 도 13을 참조하여 더미 게이트 전극(60)을 제거한다. 이 때, 게이트 절연막(50)도 일부나 전부가 제거되거나 일부로 제거할 수도 있으므로, 그런 경우에는 제2의 게이트 절연막을 형성하는 단계를 진행하도록 한다. 더미 게이트 전극(60)이 제거된 영역에 TiN막과 같은 배리어막(72)을 형성한다. 그 위로 W막과 같은 금속막(74)을 형성하여 완전히 매립한다. TiN막과 W막의 증착에는 LP-CVD를 이용할 수 있다. 그러나, 본 발명에서 배리어막(72)과 금속막(74)의 조합이 반드시 TiN/W에 한정되는 것은 아니다.

이제 도 14에서와 같이 배리어막(72)과 금속막(74)을 CMP와 같은 방법으로 평탄화하여 배리어막(72a)과 금속막(74a)으로 이루어진 금속 게이트 전극(80)을 완성한다. 일반적으로 금속 게이트 전극은 그 패터닝이 어려운데 본 발명에서는 어려운 패터닝없이 금속 게이트 전극(80)을 다마신 방법으로 형성한다.

도 15는 도 14의 Y 방향 단면도이다. 도 15에서 볼 수 있는 바와 같이, 금속 게이트 전극(80)은 게이트 스페이서(65) 및 게이트 절연막(50)에 접하는 배리어막(72a)과 배리어막(72a) 상부의 금속막(74a)을 포함한다.

도 1 내지 도 15를 참조하여 설명한 바로부터 알 수 있듯이, 본 실시예에 따른 반도체 소자는 반도체 기판(10)과, 반도체 기판(10)에 형성되고 기판(10) 표면보다 돌출된 활성영역(20)을 포함한다. 활성영역(20)은 X 방향으로 길쭉한 라인 타입이다. 활성영역(20)은 그 중심부에 형성된 중심 트렌치(22)를 사이에 두고 활성영역(20) 표면으로 이루어진 서로 평행한 제1 돌출부(23) 및 제2 돌출부(24)를 가지며 그 상부면들 및 측면들을 채널 영역으로 이용하는 핀을 구비한다.

활성영역(20) 상에는 게이트 절연막(50)과 금속 게이트 전극(80)이 구비된다. 금속 게이트 전극(80)은 중심 트렌치(22)와 동일한 폭을 가지고 제1 돌출부(23) 및 제2 돌출부(24)의 상부면들 및 측면들을 덮으면서 Y 방향으로 신장한다.

금속 게이트 전극(80) 양 옆의 활성영역(20)에는 소오스(S)와 드레인(D)이 형성되어 있다. 금속 게이트 전극(80)의 너비보다 소오스(S)와 드레인(D)에 형성되는 폰택 영역의 너비가 크다. 활성영역(20) 주위에는 중심 트렌치(22) 바닥과 동일한 표면 높이를 갖는 소자분리막(30a)을 포함한다. 금속 게이트 전극(80) 측벽에는 게이트 스페이서(65)가 형성되어 있으며, 금속 게이트 전극(80)은 게이트 스페이서(65) 및 게이트 절연막(50)에 접하는 배리어막(72a)과 배리어막(72a) 상부의 금속막(74a)을 포함한다.

이와 같이, 본 실시예에 따른 반도체 소자는 채널 너비보다 넓은 소오스 및 드레인 콘택 영역을 가지며, 활성영역에 중심 트렌치를 사이에 두고 두 개의 돌출부를 가지는 핀을 구비한다. 두 개의 돌출부를 가진 핀을 형성함에 따라 채널 면적의 증가로 소자 동작 속도를 빠르게 할 수 있다. 한편, 벌크 실리콘 기판을 사용하는 경우에는 SOI나 SGOI 기판을 사용하는 경우에 비하여 제조단가가 저렴하며, SOI나 SGOI MOSFET 소자에서 가능한 플로팅 바디 효과(floating body effect)나 드레인/소오스 사이의 항복 전압 강하, off-누설전류의 증가 문제가 없다. 반면, SOI나 SGOI 기판을 사용하는 경우에는 바닥 채널이 턴-온되는 것을 방지하는 효과가 있다. 또한, SGOI나 실리콘 저매늄 기판을 사용하는 경우에는 기판 물질의 빠른 이동도(mobility)를 이용할 수 있는 장점이 있다. 뿐만 아니라, 금속 게이트 전극을 구비함으로써 폴리실리콘 게이트 전극을 구비하는 경우보다 이점을 가진다.

제2 실시예

도 16은 본 발명의 제2 실시예에 따른 반도체 소자의 Y 방향 단면도로서, 도 2 내지 도 15에서 설명한 것과 동일 유사한 요소에 대해서는 동일한 참조번호를 부여하고 반복되는 설명은 생략한다.

본 실시예는 제1 실시예의 변형예이다.

먼저, 도 2 내지 도 6을 참조하여 설명한 단계까지는 제1 실시예에서와 동일하게 진행한다. 그런 다음, 도 7을 참조하여 설명한 단계를 수행할 때에 개구부(45) 아래에 있는 기판(10)을 제1 실시예에서보다 좀 더 깊은 깊이로 식각하여 핀 채널로 사용될 부위를 한정한다. 그리고 나서, 도 8을 참조하여 설명한 바와 같은 정도로 차단막(40)과 캡핑 산화막(30)을 리세스시킨다. 단, 채널 깊이보다 얇게 캡핑 산화막(30)을 리세스시킨다. 그런 다음, 도 9 내지 도 15를 참조하여 설명한 바와 같은 단계까지 제1 실시예에서와 동일하게 진행하면 도 16과 같은 단면도를 얻을 수 있다.

도 16에 도시되어 있는 바와 같이, 중심 트렌치(25)를 제1 실시예에서보다 깊게 형성하고 차단막(40)과 캡핑 산화막(30)을 채널 깊이보다 덜 리세스시키므로, 소자분리막(30a) 표면은 활성영역(20) 표면보다는 낮지만 중심 트렌치(25)의 바닥보다 높은 높이로 형성되어 있다. 바꾸어 말하면, 중심 트렌치(25)는 소자분리막(30a) 표면보다 깊게 형성되어 있다. 이렇게 구성함으로써 유효 채널 너비(effective channel width)를 극대화시킬 수 있는 특유의 효과가 있다.

제3 실시예

도 17은 본 발명의 제3 실시예에 따른 반도체 소자의 제조방법을 도시하는 사시도로서, 도 2 내지 도 7에서 설명한 것과 동일 유사한 요소에 대해서는 동일한 참조번호를 부여하고 반복되는 설명은 생략한다.

먼저, 도 2 내지 도 6을 참조하여 설명한 단계까지는 제1 실시예에서와 동일하게 진행한다. 그런 다음, 도 6의 평탄화 단계에 의해 드러나 있던 채널 영역 정의 패턴(15b)을 습식 또는 건식 식각의 방법으로 차단막(40), 캡핑 산화막(30) 및 기판

(10)에 대해 선택적으로 제거한다. 실리콘 질화막으로 이루어진 채널 영역 정의 패턴(15b)을 습식으로 제거할 때에는 인산 스트립을 이용할 수 있다. 이렇게 하여, 채널 영역 정의 패턴(15b)이 있던 자리에는 개구부(45)가 형성되고 그 아래 기판(10) 표면, 즉 활성영역(20) 표면이 일부 노출된다.

그런 다음, 도 17에서와 같이 개구부(45)의 내벽에 실리콘 질화막으로 스페이서(85)를 형성한다. 이 스페이서(85)와 차단막(40)과 패드 산화막(30)을 식각 마스크로 하여 개구부(45) 아래에 있는 활성영역(20)을 식각하여 핀 채널로 사용될 부위를 한정한다. 이렇게 스페이서(85)를 이용함으로써 핀의 너비를 조절할 수 있다. 그런 다음, 스페이서(85)를 제거하고 이후의 공정은 제1 실시예를 참조하여 진행한다.

실험예

본 발명을 이용해 122M SRAM의 풀-업(pull-up) p-채널 FinFET과 풀-다운(pull-down) n-채널 FinFET을 제조하였다. 게이트 절연막으로는 2nm의 실리콘 산화막을, 게이트 전극으로는 TiN/W 게이트 전극을 형성하였다. 이러한 FinFET과 비교하기 위해 종래 폴리실리콘 게이트 전극의 FinFET과 플래너 MOSFET도 제조하였다. 이들은 1.4nm의 실리콘 산화막을 게이트 절연막으로 가지며 소오스 및 드레인에는 코발트 실리사이드를 가지게 제조하였다.

도 18은 65nm TiN/W 게이트 전극을 가지는 FinFET SRAM 셀 트랜지스터의 SEM 이미지와 TEM 이미지이다. 도 18로부터 알 수 있듯이, 10nm의 TiN막이 2nm의 게이트 산화막 위에 균일하게 증착되었다.

도 19는 본 발명에서와 같은 TiN/W 전극을 가지는 FinFET, 종래 폴리실리콘 게이트 전극을 가지는 FinFET 및 종래 폴리실리콘 게이트 전극을 가지는 플래너 MOSFET의 드레인 전류(I_D)-게이트 전압(V_G) 그래프이다. 도 19에서 좌측은 n-채널 트랜지스터에 관한 것이고, 우측은 p-채널 트랜지스터에 관한 것이다. 그래프에서 실선은 TiN/W 게이트 전극을 가지는 본 발명에 따른 FinFET의 결과이고, 동그라미(-○-)는 폴리실리콘 게이트 전극을 가지는 FinFET의 결과이며, 네모(-□-)는 폴리실리콘 게이트 전극을 가지는 플래너 MOSFET의 결과이다. TiN막의 일함수가 미드-갭(mid-gap)이므로 실리콘 바디(반도체 기판)와 일함수가 잘 매칭된다. TiN막 게이트 전극을 가지는 FinFET의 문턱전압이 폴리실리콘 게이트 전극을 가지는 FinFET에 비하여 n-채널의 경우 450mV, p-채널의 경우 200mV 증가했는데, 이는 1.0V 이하의 CMOS 동작에 적당한 수치이다.

뿐만 아니라, 도 20에서 볼 수 있는 바와 같이, 금속 게이트 전극을 사용함에 따라 TiN/W 금속 게이트 전극을 가지는 FinFET(실선)의 구동 전류는 폴리실리콘 게이트 전극 FinFET(네모 -□-)보다 높으며, 폴리실리콘 게이트 전극 플래너 MOSFET(동그라미 -○-)보다는 수 배 높다.

이온주입을 통한 문턱전압 조정을 검증하기 위해, 핀의 상부에 카운터 도핑을 실시한 FinFET을 조사하였다. 도 21에서 실선과 동그라미는 카운터 도핑을 실시했을 때의 결과이고 네모는 카운터 도핑을 실시하지 않았을 때의 결과이다. 도 21에서 볼 수 있는 바와 같이, n-채널 FinFET의 핀 상부에 2E13/cm^2의 As 이온을 도핑한 결과 문턱전압 균일도 저하없이 70mV 쉬프트하였다.

테스트 결과 정적 노이즈 마진(static noise margin)도 0.8V에서 310mV로 적절하였으며 2.1V에서 수명도 10년 이상 보장되었다.

본 발명의 특정 실시예에 대한 이상의 설명은 예시 및 설명을 목적으로 제공되었다. 본 발명은 상기 실시예들에 한정되지 않으며, 본 발명의 기술적 사상 내에서 당 분야에서 통상의 지식을 가진 자에 의하여 여러 가지 많은 수정 및 변형이 가능함은 명백하다. 본 발명의 범주는 첨부된 청구범위 및 그 등가물에 의해 한정된다.

발명의 효과

이상 상술한 바와 같이, 본 발명은 활성영역 내에 중심 트렌치를 형성하여 삼차원 구조의 채널을 형성한다. 그에 따라, 소오스/드레인 콘택 면적이 감소하는 것을 방지할 수 있다. 즉, 소자분리영역 형성시 정의된 활성영역의 면적 감소없이 입체 구조의 채널 영역을 형성할 수 있다.

본 발명은 활성영역 하드 마스크를 등방성 식각하여 채널 영역을 정의하는 패턴으로 이용한다. 따라서, 채널 영역 정의 패턴 형성을 위한 별도의 물질을 도포 또는 증착하는 공정을 생략하여 공정을 단순화시킬 수 있으며 제조비용을 절감할 수 있다.

한편 벌크 실리콘 기판을 사용함에 따라 SOI를 사용하는 경우에 비하여 제조단가가 저렴하며, SOI MOSFET 소자에서 가능한 플로팅 바디 효과나 드레인/소오스 사이의 항복 전압 강하, 오프-누설전류의 증가 문제가 없다.

본 발명에 따른 기술을 이용하여 65nm의 CMOS FinFET SRAM 셀 트랜지스터를 제조할 수 있고 이 소자는 적당한 문턱 전압, 서브스레시홀드 스윙, DIBL(drain induced barrier lowering)을 보여준다. 350mV의 정적 노이즈 마진을 가진 소자를 제조할 수 있다.

(57) 청구의 범위

청구항 1.

반도체 기판에 형성되고 상기 기판 표면보다 돌출된 활성영역;

상기 활성영역 중심부에 형성된 중심 트렌치를 사이에 두고 상기 활성영역 표면으로 이루어진 서로 평행한 제1 돌출부 및 제2 돌출부를 가지며 상기 제1 돌출부와 제2 돌출부의 상부면들 및 측면들을 채널 영역으로 이용하는 핀;

상기 핀을 가지는 활성영역 상에 형성된 게이트 절연막;

상기 게이트 절연막 상에 형성된 금속 게이트 전극;

상기 금속 게이트 전극 측벽 상의 게이트 스페이서; 및

상기 금속 게이트 전극 양 옆의 상기 활성영역에 형성된 소오스와 드레인을 포함하며,

상기 금속 게이트 전극은 상기 게이트 스페이서 및 상기 게이트 절연막에 접하는 배리어막과 상기 배리어막 상부의 금속막을 포함하는 것을 특징으로 하는 반도체 소자.

청구항 2.

제1항에 있어서, 상기 배리어막은 TiN막이고 상기 금속막은 W막인 것을 특징으로 하는 반도체 소자.

청구항 3.

제1항에 있어서, 상기 핀의 하부에는 채널 이온주입이 되어 있고 상기 핀의 상부에는 상기 채널 이온주입의 불순물과 반대되는 도전형의 불순물이 주입되어 있는 것을 특징으로 하는 반도체 소자.

청구항 4.

제1항에 있어서, 상기 활성영역 주위에 상기 중심 트렌치 바닥과 동일한 표면 높이를 갖는 소자분리막을 더 포함하는 것을 특징으로 하는 반도체 소자.

청구항 5.

제1항에 있어서, 상기 활성영역 주위에 상기 중심 트렌치 바닥보다는 높고 상기 활성영역 표면보다는 낮은 표면 높이를 갖는 소자분리막을 더 포함하는 것을 특징으로 하는 반도체 소자.

청구항 6.

제1항에 있어서, 상기 금속 게이트 전극은 상기 중심 트렌치와 동일하거나 더 넓은 폭을 가지고 상기 제1 돌출부 및 제2 돌출부의 상부면들 및 측면들을 덮으면서 신장하는 것을 특징으로 하는 반도체 소자.

청구항 7.

제1항에 있어서, 상기 게이트 절연막은 실리콘 산화막, 하프늄 산화막, 지르코늄 산화막, 알루미늄 산화막, 실리콘 질화막 또는 실리콘 산화질화막인 것을 특징으로 하는 반도체 소자.

청구항 8.

제1항에 있어서, 상기 금속 게이트 전극의 너비보다 상기 소오스 및 드레인에 형성되는 콘택 영역의 너비가 큰 것을 특징으로 하는 반도체 소자.

청구항 9.

제1항에 있어서, 상기 반도체 기판은 실리콘 웨이퍼, SOI(Silicon-On-Insulator) 기판, SGOI(Silicon Germanium-On-Insulator) 기판 또는 실리콘 저매늄(SiGe) 웨이퍼인 것을 특징으로 하는 반도체 소자.

청구항 10.

반도체 기판에 상기 기판 표면보다 돌출된 활성영역을 정의하는 단계;

상기 활성영역 중심부를 식각하여 중심 트렌치를 형성함으로써, 상기 중심 트렌치를 사이에 두고 상기 활성영역 표면으로 이루어진 서로 평행한 제1 돌출부 및 제2 돌출부를 가지며 상기 제1 돌출부와 제2 돌출부의 상부면들 및 측면들을 채널 영역으로 이용하는 핀을 형성하는 단계;

상기 핀을 가지는 상기 활성영역 상에 게이트 절연막을 형성하는 단계;

상기 게이트 절연막 상에 더미 게이트 전극을 형성하는 단계;

상기 더미 게이트 전극 측벽에 게이트 스페이서를 형성하는 단계;

상기 더미 게이트 전극 양 옆의 상기 활성영역에 소오스 및 드레인을 형성하는 단계;

상기 반도체 기판에 절연막을 증착한 후 상기 더미 게이트 전극 상면이 드러나도록 평탄화하는 단계;

상기 더미 게이트 전극을 제거하는 단계; 및

상기 더미 게이트 전극이 제거된 영역에 금속 게이트 전극을 형성하는 단계를 포함하는 반도체 소자의 제조방법.

청구항 11.

반도체 기판 상에 활성영역 하드 마스크를 형성하는 단계;

상기 활성영역 하드 마스크를 식각 마스크로 하여 상기 기판을 식각함으로써, 상기 기판 표면보다 돌출된 활성영역을 정의하고, 상기 활성영역을 둘러싸는 트렌치를 형성하는 단계;

상기 활성영역 하드 마스크를 등방성 식각하여 상기 활성영역의 가장자리를 노출시키는 하드 마스크 패턴을 형성하는 단계;

상기 트렌치 안에 갭 필(gap fill) 산화막을 채우고 상기 하드 마스크 패턴을 평탄화 종료점으로 하여 평탄화하는 단계;

상기 갭 필 산화막과 하드 마스크 패턴을 라인 타입으로 패터닝하여 중심에 적어도 하나의 채널 영역 정의 패턴을 포함하는 더미 패턴을 형성하는 단계;

상기 더미 패턴 위로 차단막을 증착하고 상기 채널 영역 정의 패턴을 평탄화 종료점으로 하여 평탄화하는 단계;

상기 차단막의 평탄화 단계에 의해 드러나 있는 상기 채널 영역 정의 패턴을 제거하여 상기 활성영역 표면을 노출시키는 개구부를 형성하는 단계;

상기 개구부 아래에 있는 상기 활성영역을 식각하여 핀 채널로 사용될 부위에 중심 트렌치를 형성하는 단계;

상기 차단막과 갭 필 산화막을 리세스시켜 드러난 상기 활성영역 주위로 소자분리막을 형성하고, 상기 활성영역에서 상기 중심 트렌치와 상기 소자분리막 사이에 상기 기판 표면으로 이루어지고 상기 중심 트렌치를 사이에 두고 서로 평행한 제1 돌출부 및 제2 돌출부를 가지며 상기 제1 돌출부와 제2 돌출부의 상부면들 및 측면들을 채널 영역으로 이용하는 핀을 노출시키는 단계;

상기 핀을 가지는 상기 활성영역 상에 게이트 절연막을 형성하는 단계;

상기 게이트 절연막 상에 더미 게이트 전극을 형성하는 단계;

상기 더미 게이트 전극 측벽에 게이트 스페이서를 형성하는 단계;

상기 더미 게이트 전극 양 옆의 상기 활성영역에 소오스 및 드레인을 형성하는 단계;

상기 반도체 기판에 절연막을 증착한 후 상기 더미 게이트 전극 상면이 드러나도록 평탄화하는 단계;

상기 더미 게이트 전극을 제거하는 단계; 및

상기 더미 게이트 전극이 제거된 영역에 금속 게이트 전극을 형성하는 단계를 포함하는 반도체 소자의 제조방법.

청구항 12.

제10항 또는 제11항에 있어서, 상기 더미 게이트 전극을 제거한 다음 상기 더미 게이트 전극이 제거된 영역에 제2의 게이트 절연막을 형성하는 단계를 더 포함하는 것을 특징으로 하는 반도체 소자의 제조방법.

청구항 13.

제10항 또는 제11항에 있어서, 상기 반도체 기판에 절연막을 증착한 후 상기 더미 게이트 전극 상면이 드러나도록 평탄화하는 단계는 CMP(Chemical Mechanical Polishing)를 이용하는 것을 특징으로 하는 반도체 소자의 제조방법.

청구항 14.

제10항 또는 제11항에 있어서, 상기 절연막은 HDP-CVD로 증착한 산화막인 것을 특징으로 하는 반도체 소자의 제조방법.

청구항 15.

제10항 또는 제11항에 있어서, 상기 금속 게이트 전극을 형성하는 단계는

상기 게이트 스페이서와 게이트 절연막에 접하는 배리어막을 형성하는 단계;

상기 배리어막 상에 금속막을 형성하는 단계; 및

상기 배리어막과 금속막을 평탄화하는 단계를 포함하는 것을 특징으로 하는 반도체 소자의 제조방법.

청구항 16.

제15항에 있어서, 상기 배리어막은 TiN막이고 상기 금속막은 W막인 것을 특징으로 하는 반도체 소자의 제조방법.

청구항 17.

제15항에 있어서, 상기 평탄화하는 단계는 CMP를 이용하는 것을 특징으로 하는 반도체 소자의 제조방법.

청구항 18.

제10항 또는 제11항에 있어서, 상기 금속 게이트 전극은 상기 중심 트렌치와 동일하거나 더 넓은 폭을 가지고 상기 제1 돌출부 및 제2 돌출부의 상부면들 및 측면들을 덮으면서 신장하도록 형성하는 것을 특징으로 하는 반도체 소자의 제조방법.

청구항 19.

제10항 또는 제11항에 있어서, 상기 금속 게이트 전극의 너비보다 상기 소오스 및 드레인에 형성되는 콘택 영역의 너비가 크게 형성하는 것을 특징으로 하는 반도체 소자의 제조방법.

청구항 20.

제10항 또는 제11항에 있어서, 상기 활성영역을 정의하는 단계 다음에,

상기 활성영역 하부에 채널 이온주입을 수행하는 단계; 및

상기 활성영역 상부에 상기 채널 이온주입의 불순물과 반대되는 도전형의 불순물을 주입하는 단계를 더 포함하는 것을 특징으로 하는 반도체 소자의 제조방법.

청구항 21.

제11항에 있어서, 상기 활성영역 하드 마스크는 실리콘 질화막으로 형성하고 상기 등방성 식각은 인산(H_3PO_4)을 이용한 습식 식각으로 실시하는 것을 특징으로 하는 반도체 소자의 제조방법.

청구항 22.

제11항에 있어서, 상기 등방성 식각은 습식 식각 또는 플라즈마를 이용한 건식 식각으로 실시하는 것을 특징으로 하는 반도체 소자의 제조방법.

청구항 23.

제11항에 있어서, 상기 등방성 식각 시간을 조절함으로써 상기 핀의 너비를 조절하는 것을 특징으로 하는 반도체 소자의 제조방법.

청구항 24.

제11항에 있어서, 상기 갭 필 산화막 평탄화에는 CMP(Chemical Mechanical Polishing) 또는 전면 식각(blanket etch)을 이용하는 것을 특징으로 하는 반도체 소자의 제조방법.

청구항 25.

제11항에 있어서, 상기 차단막은 실리콘 산화막으로 형성하는 것을 특징으로 하는 반도체 소자의 제조방법.

청구항 26.

제11항에 있어서, 상기 차단막의 평탄화에는 CMP(Chemical Mechanical Polishing) 또는 전면 식각을 이용하는 것을 특징으로 하는 반도체 소자의 제조방법.

청구항 27.

제11항에 있어서, 상기 게이트 절연막은 열산화 방법으로 실리콘 산화막을 성장시켜 형성하거나 ALD(Atomic Layer Deposition), CVD, PE-ALD(Plasma Enhanced-ALD) 또는 PE-CVD 방법으로 실리콘 산화막, 하프늄 산화막, 지르코늄 산화막, 알루미늄 산화막, 실리콘 질화막 또는 실리콘 산화질화막을 증착하거나 코팅 방법으로 형성하는 것을 특징으로 하는 반도체 소자의 제조방법.

청구항 28.

제11항에 있어서, 상기 차단막과 갭 필 산화막을 상기 중심 트렌치 바닥과 동일한 높이까지 리세스시키는 것을 특징으로 하는 반도체 소자의 제조방법.

청구항 29.

제11항에 있어서, 상기 차단막과 갭 필 산화막을 상기 중심 트렌치 바닥보다 높은 높이로 리세스시키는 것을 특징으로 하는 반도체 소자의 제조방법.

청구항 30.

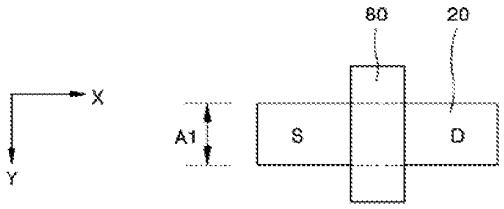
제11항에 있어서, 상기 개구부를 형성하는 단계 이후 상기 개구부 내벽에 스페이서를 형성하는 단계를 더 포함하여 상기 중심 트렌치를 형성할 때에 이용한 마스 이를 제거하는 것을 특징으로 하는 반도체 소자의 제조방법.

청구항 31.

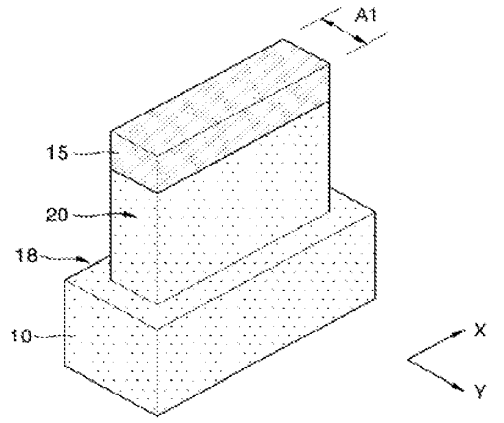
제11항에 있어서, 상기 스페이서는 실리콘 질화막으로 형성하는 것을 특징으로 하는 반도체 소자의 제조방법.

도면

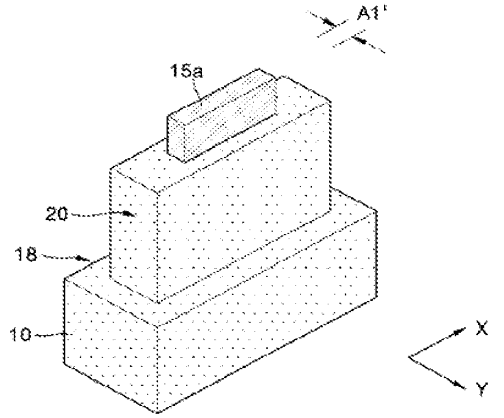
도면1



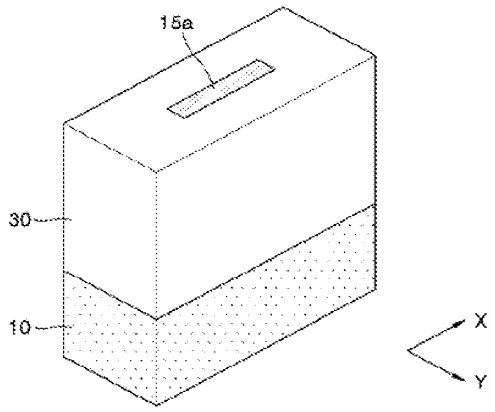
도면2



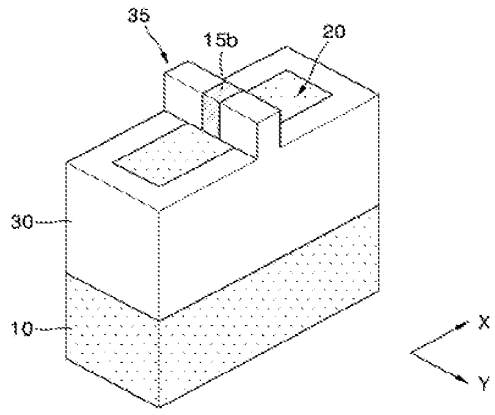
도면3



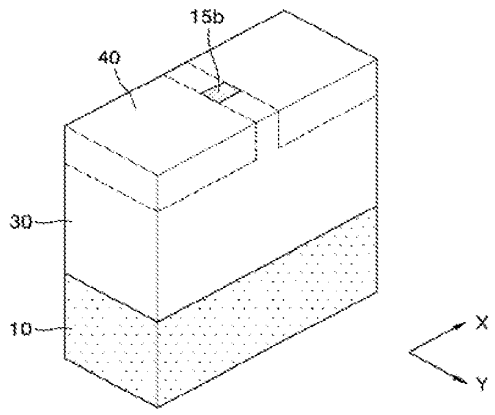
도면4



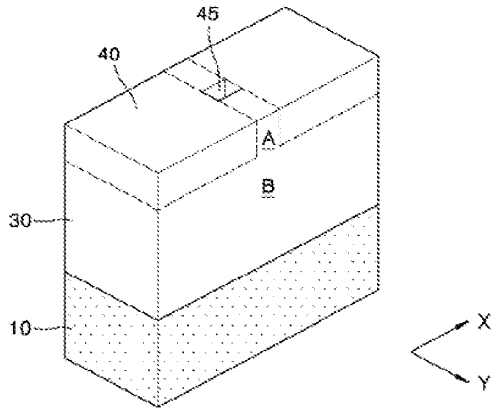
도면5



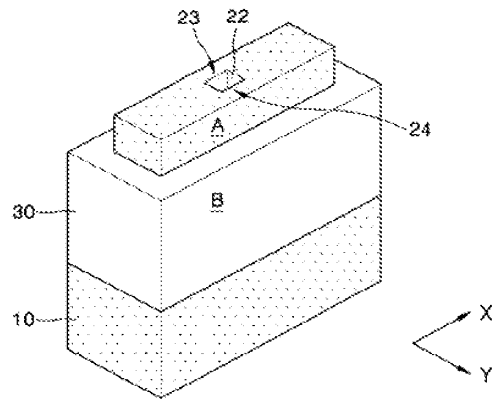
도면6



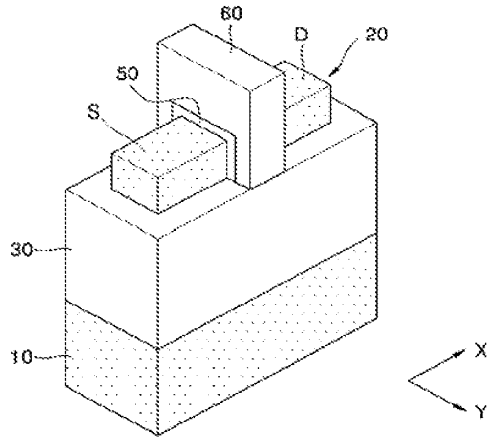
도면17



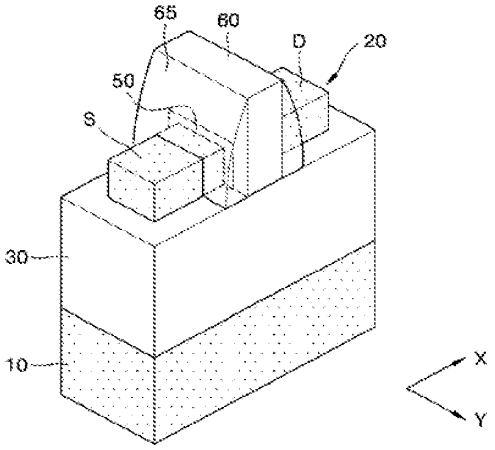
도면18



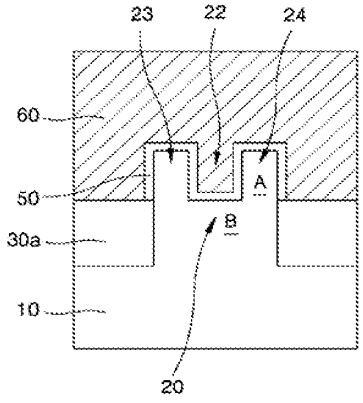
도면19



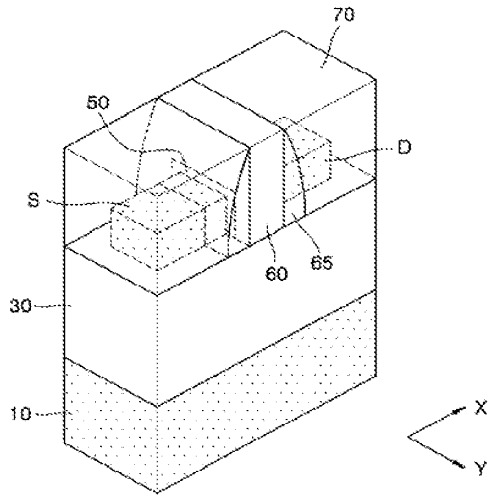
도면10



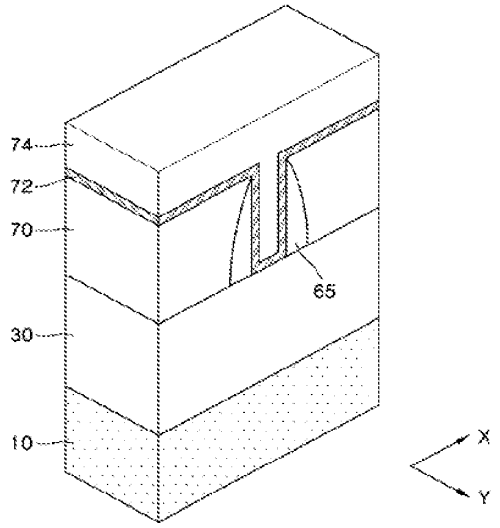
도면11



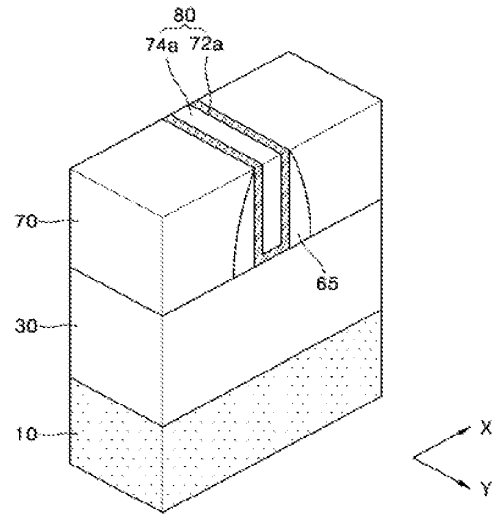
도면12



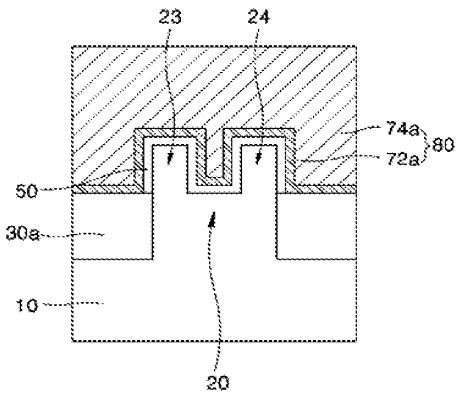
도면13



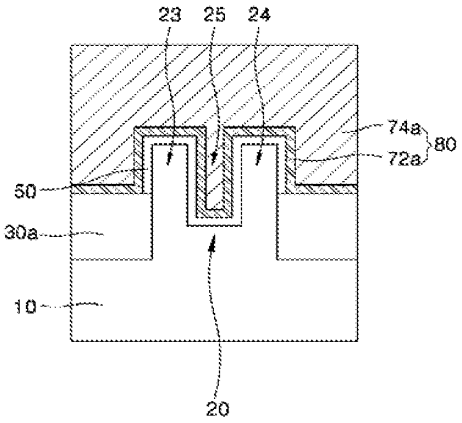
도면14



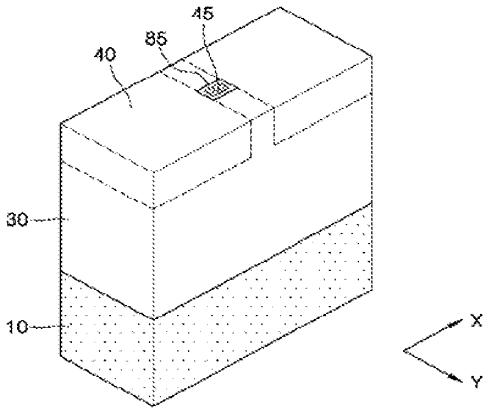
도면15



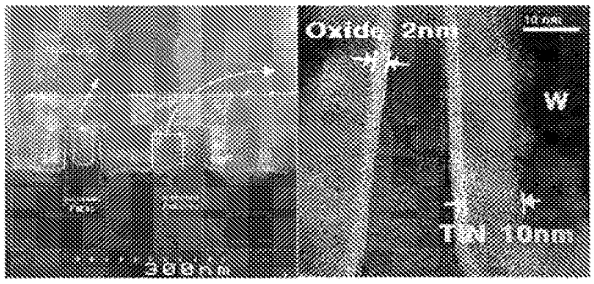
도면16



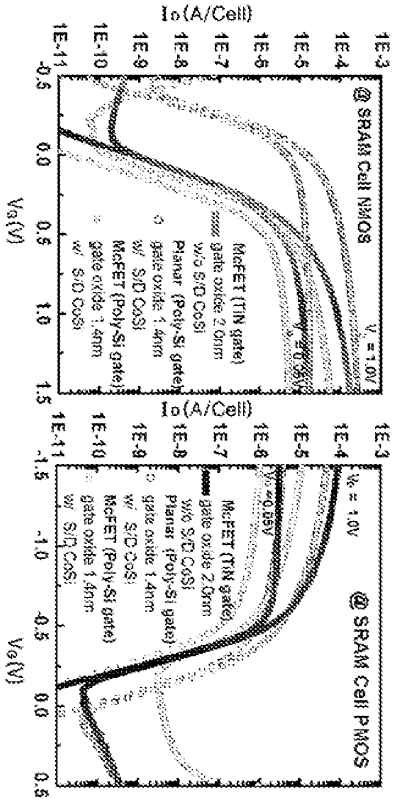
도면17



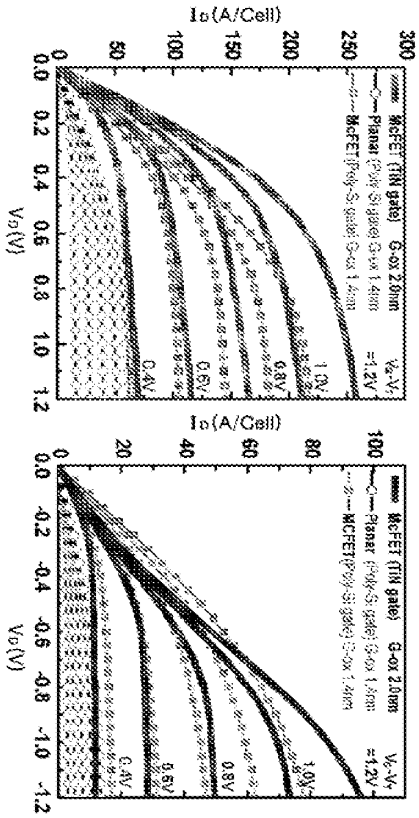
도면13


Oxide 2nm
W
TiN 10nm
300nm

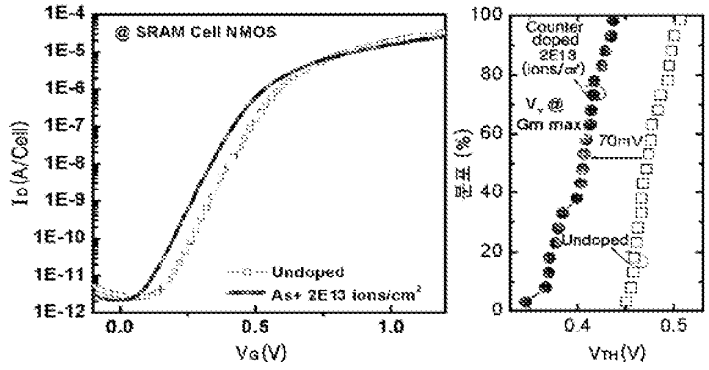
도면14


@ SRAM Cell NMOS
@ SRAM Cell PMOS
Io(A/Cell)
Vg(V)
McFET (TiN gate)
gate oxide 2.0nm
w/o S/D CoSi
Planar (Poly-Si gate)
gate oxide 1.4nm
w/ S/D CoSi
McFET (Poly-Si gate)
gate oxide 1.4nm
w/ S/D CoSi

도면20


ID(A/Cell)
VG(V)
McFET (TiN gate) Tox 2.0nm
Planar (Poly-Si gate) Tox 1.4nm
McFET(Poly-Si gate) Tox 1.4nm
VD-VT =1.2V
0.4V
0.6V
0.8V
1.0V

도면21


@ SRAM Cell NMOS
ID(A/Cell)
VG(V)
Undoped
As+ 2E13 ions/cm²
Counter doped 2E13 (ions/㎠)
Vt @ Gm max
70mV
Undoped
분포 (%)
VTH(V)

(19) KOREAN INTELLECTUAL PROPERTY OFFICE

KOREAN PATENT ABSTRACTS

(11) Registration number: 100653711 B1
(45) Issue date: 05.12.2006
(24) Registration date: 28.11.2006

(21) Application number: 1020050108790
(22) Application date: 14.11.2005

(51) Int. Cl: H01L 21/335

(73) Proprietor:
(72) Inventor:
- KIM, SUNG MIN
- YUN, EUN JUNG
- KIM, DONG WON

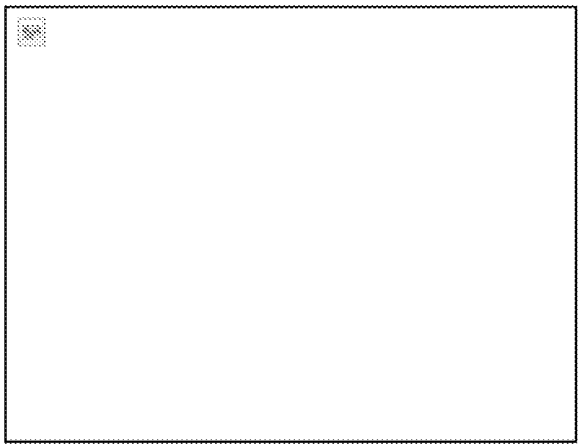
(54) SCHOTTKY BARRIER FINFET DEVICE AND FABRICATING METHOD THEREOF, CAPABLE OF IMPROVING CURRENT DRIVING CAPABILITY AND OPERATION SPEED

(57) Abstract:

PURPOSE: A Schottky barrier finFET(fin-type field effect transistor) is provided to reduce a channel length and increase a channel width by forming a Schottky barrier finFET including a source/drain made of a metal material layer.

CONSTITUTION: A lower fin body(131) is formed on a substrate(100). An upper fin body(132) is extended upward from the center part of the lower fin body, including first and second sidewalls confronting each other. The upper surface of the upper fin body and the first and second sidewalls are covered with a gate structure(110) crossing the upper part of the upper fin body. A source/drain (140) is formed on the surface of the sidewalls of the upper fin body adjacent to the sidewalls of the gate structure, made of a metal material layer formed on the upper surface of the lower fin body positioned at both sides of the upper fin body. The source/drain forms a Schottky barrier with respect to the lower and upper fin bodies. The first and second sidewalls of the upper fin body are self-aligned with the sidewalls of the lower fin body.

copyright KIPO 2007



(19)대한민국특허청(KR)
(12) 등록특허공보(B1)

(51) 。Int. Cl.
H01L 21/335 (2006.01)

(45) 공고일자 2006년12월05일
(11) 등록번호 10-0653711
(24) 등록일자 2006년11월28일

(21) 출원번호 10-2005-0108790
(22) 출원일자 2005년11월14일
심사청구일자 2005년11월14일

(65) 공개번호
(43) 공개일자

(73) 특허권자 삼성전자주식회사
경기도 수원시 영통구 매탄동 416

(72) 발명자 김성민
인천 부평구 부개3동 삼부아파트 108동 2204호

윤은정
서울 서초구 잠원동 신반포한신아파트 316동 403호

김동원
경기 성남시 분당구 정자동 정든마을신화5단지아파트 506동1602호

(74) 대리인 박상수

(56) 선행기술조사문헌
KR1020030027228 A
KR1020040022605 A
* 심사관에 의하여 인용된 문헌

심사관 : 백양규

전체 청구항 수 : 총 23 항

(54) 쇼트키 배리어 핀 펫 소자 및 그 제조방법

(57) 요약

쇼트키 배리어 핀펫 소자 및 그 제조방법을 제공한다. 이 소자는 기판 상에 제공된 하부 핀 바디를 구비한다. 상기 하부 핀 바디의 중심부로부터 상부로 연장되고 서로 마주보는 제1 및 제2 측벽들을 갖는 상부 핀 바디가 제공된다. 상기 상부 핀 바디 상부를 가로지르며 상기 상부 핀 바디의 상부면 및 상기 제1 및 제2 측벽들을 덮는 게이트 구조체가 제공된다. 상기 게이트 구조체의 측벽들에 인접한 상기 상부 핀 바디의 측벽들의 표면에 형성되고 상기 상부 핀 바디 양 옆에 위치하는 상기 하부 핀 바디의 상부 표면에 형성된 금속 물질막으로 이루어진 소스/드레인을 포함하되, 상기 소스/드레인은 상기 하부 및 상부 핀 바디들에 대하여 쇼트키 배리어를 형성한다.

대표도

도 5

특허청구의 범위

청구항 1.

기판 상에 제공된 하부 핀 바디;

상기 하부 핀 바디의 중심부로부터 상부로 연장되고 서로 마주보는 제1 및 제2 측벽들을 갖는 상부 핀 바디;

상기 상부 핀 바디 상부를 가로지르며 상기 상부 핀 바디의 상부면 및 상기 제1 및 제2 측벽들을 덮는 게이트 구조체; 및

상기 게이트 구조체의 측벽들에 인접한 상기 상부 핀 바디의 측벽들의 표면에 제공되고 상기 상부 핀 바디 양 옆에 위치하는 상기 하부 핀 바디의 상부 표면에 제공된 금속 물질막으로 이루어진 소스/드레인을 포함하되, 상기 소스/드레인은 상기 하부 및 상부 핀 바디들에 대하여 쇼트키 베리어를 형성하는 것을 특징으로 하는 핀 펫 소자.

청구항 2.

제 1 항에 있어서,

상기 상부 핀 바디의 상기 제1 및 제2 측벽들은 상기 하부 핀 바디의 측벽들과 자기정렬된 것을 특징으로 하는 핀 펫 소자.

청구항 3.

제 1 항에 있어서,

상기 게이트 구조체는 상기 상부 핀 바디의 상기 제1 및 제2 측벽들로부터 상기 상부 핀 바디의 상기 제1 및 제2 측벽들과 인접한 상기 하부 핀 바디의 측벽들을 덮도록 연장된 것을 특징으로 하는 핀 펫 소자.

청구항 4.

제 1 항에 있어서,

상기 하부 및 상부 핀 바디들은 같은 물질막으로 이루어지되, 상기 하부 및 상부 핀 바디들은 실리콘(Si)막, 게르마늄(Ge)막, 실리콘 게르마늄(SiGe)막, 실리콘 게르마늄 카바이드(SiGeC)막, 또는 실리콘 카바이드(SiC)막으로 이루어진 것을 특징으로 하는 핀 펫 소자.

청구항 5.

제 1 항에 있어서,

상기 금속 물질막은 금속 실리사이드막인 것을 특징으로 하는 핀 펫 소자.

청구항 6.

제 5 항에 있어서,

상기 금속 실리사이드막은 탄탈륨 실리사이드(TaSi)막, 타이타늄 실리사이드(TiSi)막, 텅스텐 실리사이드(WSi)막, 니켈 실리사이드(NiSi)막, 코발트 실리사이드(CoSi)막, 백금 실리사이드(PtSi)막, 에르븀 실리사이드(ErSi)막, 이터븀 실리사이드(YbSi)막, 이트륨 실리사이드(YSi)막, 가돌리늄 실리사이드(GdSi)막, 터븀 실리사이드(TbSi)막, 디스프로슘 실리사이드(DySi)막, 홀뮴 실리사이드(HoSi)막, 툴륨 실리사이드(TmSi)막, 루테늄 실리사이드(LuSi)막, 팔라듐 실리사이드(PdSi)막, 오스뮴 실리사이드(OsSi)막, 이리듐 실리사이드(IrSi)막, 및 레늄 실리사이드(ReSi)막으로 이루어진 그룹 중에서 선택된 적어도 하나의 막을 포함하는 것을 특징으로 하는 핀 펫 소자.

청구항 7.

제 1 항에 있어서,

상기 게이트 구조체의 측벽들을 덮는 게이트 스페이서를 더 포함하는 핀 펫 소자.

청구항 8.

기판 상에 예비 핀 바디를 형성하고,

상기 예비 핀 바디 상부를 가로지르며 상기 예비 핀 바디의 상부면 및 측벽들을 덮는 게이트 구조체를 형성하고,

상기 게이트 구조체의 측벽들을 덮는 게이트 스페이서를 형성하고,

상기 게이트 스페이서 및 상기 게이트 구조체를 식각마스크로 하여 상기 예비 핀 바디를 부분 식각하여 상기 게이트 구조체 하부에 위치한 상부 핀 바디 및 상기 상부 핀 바디 보다 낮은 레벨에 위치하는 하부 핀 바디를 형성하되, 상기 상부 핀 바디는 노출된 양 측벽들을 갖고,

상기 노출된 상부 핀 바디의 측벽들의 표면들 및 상기 상부 핀 바디 양 옆에 위치하는 상기 하부 핀 바디의 상부 표면에 상기 상부 및 하부 핀 바디들에 대하여 쇼트키 배리어를 형성하는 금속 물질막으로 이루어진 소스/드레인을 형성하는 것을 포함하는 핀 펫 소자의 제조방법.

청구항 9.

제 8 항에 있어서,

상기 예비 핀 바디는 실리콘(Si)막, 게르마늄(Ge)막, 실리콘 게르마늄(SiGe)막, 실리콘 게르마늄 카바이드(SiGeC)막, 또는 실리콘 카바이드(SiC)막으로 형성되는 것을 특징으로 하는 핀 펫 소자의 제조방법.

청구항 10.

제 8 항에 있어서,

상기 소스/드레인은 금속 실리사이드막으로 형성되는 것을 특징으로 하는 핀 펫 소자의 제조방법.

청구항 11.

제 10 항에 있어서,

상기 금속 실리사이드막은 탄탈륨 실리사이드(TaSi)막, 타이타늄 실리사이드(TiSi)막, 텅스텐 실리사이드(WSi)막, 니켈 실리사이드(NiSi)막, 코발트 실리사이드(CoSi)막, 백금 실리사이드(PtSi)막, 에르븀 실리사이드(ErSi)막, 이터븀 실리사이드(YbSi)막, 이트륨 실리사이드(YSi)막, 가돌리늄 실리사이드(GdSi)막, 터븀 실리사이드(TbSi)막, 디스프로슘 실리사이드(DySi)막, 홀뮴 실리사이드(HoSi)막, 툴륨 실리사이드(TmSi)막, 루테늄 실리사이드(LuSi)막, 팔라듐 실리사이드(PdSi)막, 오스뮴 실리사이드(OsSi)막, 이리듐 실리사이드(IrSi)막, 및 레늄 실리사이드(ReSi)막로 이루어진 그룹 중에서 선택된 적어도 하나의 막을 포함하는 것을 특징으로 하는 핀 펫 소자의 제조방법.

청구항 12.

제 8 항에 있어서,

상기 소스/드레인을 형성하는 것은

상기 하부 및 상부 핀 바디들을 갖는 기판의 전면 상에 금속막을 형성하고,

상기 금속막을 갖는 기판을 열처리하여 상기 하부 및 상부 핀 바디들과 상기 금속막을 반응시키고,

미반응된 금속막을 제거하는 것을 포함하는 핀 펫 소자의 제조방법.

청구항 13.

제 8 항에 있어서,

상기 소스/드레인은 상기 게이트 구조체의 측벽들과 자기정렬되거나, 또는 상기 게이트 구조체와 중첩되도록 형성되는 것을 특징으로 하는 핀 펫 소자의 제조방법.

청구항 14.

기판 상에 핀 바디를 형성하고,

상기 핀 바디 상부를 가로지르며 상기 핀 바디의 상부면 및 측벽들을 덮는 희생 마스크를 형성하고,

상기 희생 마스크의 양옆에 위치하는 상기 핀 바디의 표면에 상기 핀 바디에 대하여 쇼트키 배리어를 형성하는 금속 물질막으로 이루어진 소스/드레인을 형성하고,

상기 희생 마스크의 측벽들을 감싸며 상기 핀 바디를 덮는 절연 패턴을 형성하고,

상기 희생 마스크를 제거하여 상기 핀 바디의 일부분을 노출시키는 개구부를 형성하고,

상기 노출된 핀 바디를 덮는 게이트 구조체를 형성하는 것을 포함하는 핀 펫 소자의 제조방법.

청구항 15.

제 14 항에 있어서,

상기 핀 바디는 실리콘(Si)막, 게르마늄(Ge)막, 실리콘 게르마늄(SiGe)막, 실리콘 게르마늄 카바이드(SiGeC)막, 또는 실리콘 카바이드(SiC)막으로 형성되는 것을 특징으로 하는 핀 펫 소자의 제조방법.

청구항 16.

제 14 항에 있어서,

상기 소스/드레인은 금속막 또는 금속 실리사이드막으로 형성되는 것을 특징으로 하는 핀 펫 소자의 제조방법.

청구항 17.

제 16 항에 있어서,

상기 금속 실리사이드막은 탄탈륨 실리사이드(TaSi)막, 타이타늄 실리사이드(TiSi)막, 텅스텐 실리사이드(WSi)막, 니켈 실리사이드(NiSi)막, 코발트 실리사이드(CoSi)막, 백금 실리사이드(PtSi)막, 에르븀 실리사이드(ErSi)막, 이터븀 실리사이드(YbSi)막, 이트륨 실리사이드(YSi)막, 가돌리늄 실리사이드(GdSi)막, 터븀 실리사이드(TbSi)막, 디스프로슘 실리사이드(DySi)막, 홀뮴 실리사이드(HoSi)막, 툴륨 실리사이드(TmSi)막, 루테늄 실리사이드(LuSi)막, 팔라듐 실리사이드(PdSi)막, 오스뮴 실리사이드(OsSi)막, 이리듐 실리사이드(IrSi)막, 및 레늄 실리사이드(ReSi)막으로 이루어진 그룹 중에서 선택된 적어도 하나의 막을 포함하는 것을 특징으로 하는 핀 펫 소자의 제조방법.

청구항 18.

제 14 항에 있어서,

상기 소스/드레인을 형성하는 것은

상기 희생 마스크를 갖는 기판 상에 금속막을 형성하고,

상기 금속막을 갖는 기판을 열처리하여 상기 핀 바디와 상기 금속막을 반응시키고,

미반응된 금속막을 제거하는 것을 포함하는 핀 펫 소자의 제조방법.

청구항 19.

제 14 항에 있어서,

상기 절연 패턴은 상기 희생 마스크에 대하여 식각선택비를 갖는 물질막으로 형성하는 것을 특징으로 하는 핀 펫 소자의 제조방법.

청구항 20.

제 14 항에 있어서,

상기 게이트 구조체는 차례로 적층된 게이트 절연막 및 게이트 전극으로 형성하는 것을 특징으로 핀 펫 소자의 제조방법.

청구항 21.

제 20 항에 있어서,

상기 게이트 절연막은 화학 기상 증착법 또는 원자층 증착법에 의해 형성되고, 상기 게이트 전극은 실리콘막, 금속막, 및 금속 실리사이드막으로 이루어진 그룹 중에서 선택된 적어도 하나의 막으로 형성되는 것을 특징으로 하는 핀 펫 소자의 제조방법.

청구항 22.

제 14 항에 있어서,

상기 소스/드레인은 상기 게이트 구조체의 측벽들과 자기정렬되거나, 또는 상기 게이트 구조체와 중첩되도록 형성되는 것을 특징으로 하는 핀 펫 소자의 제조방법.

청구항 23.

제 14 항에 있어서,

상기 희생 마스크를 형성하는 것은

상기 핀 바디 상부를 가로지르며 상기 핀 바디의 상부면 및 측벽들을 덮는 예비 희생 마스크를 형성하되, 상기 예비 희생 마스크는 제1 폭을 갖도록 형성되고,

상기 핀 바디 상부를 상기 제1 폭 보다 작은 제2 폭으로 가로지르도록 상기 예비 희생 마스크를 등방성 식각하는 것을 포함하는 핀 펫 소자의 제조방법.

명세서

발명의 상세한 설명

발명의 목적

발명이 속하는 기술 및 그 분야의 종래기술

본 발명은 반도체소자 및 그 제조방법에 관한 것으로, 특히 쇼트키 배리어 핀 펫 소자 및 그 제조방법에 관한 것이다.

반도체소자는 PN 접합구조를 갖는 모스펫(MOSFET)과 같은 개별 소자(discrete device)를 스위칭 소자로써 널리 채택하고 있다. 최근, 반도체 소자의 고집적화 및 고성능화 경향에 따라 모스펫을 소형화(scaling down)시키는 연구들을 진행하고 있다. 이러한, 모스펫의 소형화는 반도체 소자의 집적도를 향상시키고, 소자의 크기를 줄여 스위칭 동작 속도를 줄이며, 소자와 소자 사이의 거리를 줄여서 신호전달 속도를 향상시킬 수 있다. 그러나, 종래의 모스펫의 소형화에는 한계가 있다. 즉, 모스펫이 소형화되면서, 게이트 길이, 게이트 절연막의 두께, 동작전압, 불순물 접합의 깊이 등에서 문제가 발생하고 있다. 모스펫을 소형화시키기 위해서는 게이트 길이를 작게 하고, 게이트 절연막의 두께를 감소시키고, 동작전압을 낮추고, 불순물 접합의 깊이를 얕게 형성해야 한다. 그런데, 게이트 길이를 작게 함으로써 단채널 효과가 발생할 수 있고, 게이트 절연막의 두께를 감소시킴으로써 누설 전류 특성을 고려해야 하고, 동작전압을 낮춤으로써 문턱전압이 낮아지게 되며, 이에 따라 모스펫의 누설 전류의 영향이 커지게 되며, 불순물 접합 깊이를 얕게 형성함으로써 얕은 불순물 접합 깊이로 형성된 접합에서의 면저항 특성을 고려해야 한다. 이와 같이, 종래의 PN 접합을 이용한 모스펫을 소형화시키는 데 한계가 있다.

이에 대한 대안으로 종래의 PN 접합을 이용한 모스펫 대신에 소스/드레인을 쇼트키 접합으로 한 쇼트키 배리어 터널 트랜지스터(Schottky Barrier Tunnel Transistor; SBTT)가 제안되고 있다. 이와 같은 쇼트키 배리어 터널 트랜지스터는 불순물의 확산을 이용하지 않고 금속으로 소스/드레인 영역을 형성하므로 매우 얕은 접합을 형성할 수 있다. 또한, 금속 자체의 저항이 매우 낮으므로 기생 저항의 저감을 달성할 수 있고, 이온 주입 프로세스를 생략할 수 있는 등의 다양한 이점이 있기 때문에, 차세대 트랜지스터로써 기대되고 있다.

한편, 쇼트키 배리어 터널 트랜지스터(SBTT)가 미국 특허 제 6,744,103 B2 호에 "단채널 쇼트키-배리어 모스펫 소자 및 그 제조방법(Short-Channel schottky-barrier MOSFET device and manufacturing method)"이라는 제목으로 스나이더(Snyder)에 의하여 개시된 바 있다. 미국 특허 제 6,744,103 B2 호에 개시된 쇼트키 배리어 모스펫의 제조방법에 의하면, 반도체 기판 상에 실리콘 게이트 전극을 형성하고, 상기 실리콘 게이트 전극의 측벽을 덮는 얇은 절연막(thin insulating layer), 즉 측벽 산화막(oxide sidewalls)을 대략 100Å정도의 두께로 형성하고, 상기 실리콘 게이트 전극 양 측의 기판 상에 소스/드레인 전극들을 형성하여 쇼트키 배리어 모스펫을 제조할 수 있다. 여기서, 소스/드레인 전극들은 금속 실리사이드막으로 형성할 수 있다.

통상 금속 실리사이드를 형성하는 공정은 반도체 기판 상에 금속막을 증착하고, 열처리를 진행하여 금속막과 반도체 기판을 반응시키는 것을 포함할 수 있다. 이와 같이 형성된 금속 실리사이드막은 상기 금속막과 상기 반도체 기판이 접촉하는 면에서 대부분 형성될 수 있다. 따라서, 금속막과 접촉하지 않고, 금속막에 인접하는 반도체 기판 내에 형성되는 금속 실리사이드막은 매우 적기 때문에, 미국 특허 제 6,744,103 B2 호에서는 상기 측벽 산화막의 두께를 얇게 형성하여 소스/드레인 전극으로 사용되는 금속 실리사이드막이 상기 게이트 전극에 보다 인접하여 형성될 수 있게 하고 있다. 그러나, 이와 같은 방법으로는 얇은 소스/드레인 접합을 형성하기 위해 금속 실리사이드막의 두께를 얇게 형성하면서, 상기 금속 실리사이드막이 상기 게이트 전극에 보다 인접하여 형성될 수 있게 하는데 어려움이 있을 수 있다.

발명이 이루고자 하는 기술적 과제

본 발명이 이루고자 하는 기술적 과제는 쇼트키 배리어 핀 펫 소자를 제공하는데 있다.

본 발명이 이루고자 하는 다른 기술적 과제는 쇼트키 배리어 핀 펫 소자의 제조방법을 제공하는데 있다.

본 발명이 이루고자 하는 또 다른 기술적 과제는 단 채널 길이를 갖는 쇼트키 배리어 핀 펫 소자의 제조방법을 제공하는데 있다.

발명의 구성

본 발명의 일 태양은 쇼트키 배리어 핀 펫 소자를 제공한다. 이 소자는 기판 상에 제공된 하부 핀 바디를 구비한다. 상기 하부 핀 바디의 중심부로부터 상부로 연장되고 서로 마주보는 제1 및 제2 측벽들을 갖는 상부 핀 바디가 제공된다. 상기 상부 핀 바디 상부를 가로지르며 상기 상부 핀 바디의 상부면 및 상기 제1 및 제2 측벽들을 덮는 게이트 구조체가 제공된다. 상기 게이트 구조체의 측벽들에 인접한 상기 상부 핀 바디의 측벽들의 표면에 형성되고 상기 상부 핀 바디 양 옆에 위치하는 상기 하부 핀 바디의 상부 표면에 형성된 금속 물질막으로 이루어진 소스/드레인을 포함하되, 상기 소스/드레인은 상기 하부 및 상부 핀 바디들에 대하여 쇼트키 배리어를 형성한다.

본 발명의 몇몇 실시예들에서, 상기 상부 핀 바디의 상기 제1 및 제2 측벽들은 상기 하부 핀 바디와 자기정렬되도록 배치될 수 있다.

다른 실시예들에서, 상기 게이트 구조체는 상기 상부 핀 바디의 상기 제1 및 제2 측벽들로부터 상기 상부 핀 바디의 상기 제1 및 제2 측벽들과 인접한 상기 하부 핀 바디의 측벽들을 덮도록 연장될 수 있다.

또 다른 실시예들에서, 상기 하부 및 상부 핀 바디들은 같은 물질막으로 이루어지되, 상기 하부 및 상부 핀 바디들은 실리콘(Si)막, 게르마늄(Ge)막, 실리콘 게르마늄(SiGe)막, 실리콘 게르마늄 카바이드(SiGeC)막, 또는 실리콘 카바이드(SiC)막으로 이루어질 수 있다.

또 다른 실시예들에서, 상기 금속 물질막은 금속 실리사이드막일 수 있다. 상기 금속 실리사이드막은 탄탈륨 실리사이드(TaSi)막, 타이타늄 실리사이드(TiSi)막, 텅스텐 실리사이드(WSi)막, 니켈 실리사이드(NiSi)막, 코발트 실리사이드(CoSi)막, 백금 실리사이드(PtSi)막, 에르븀 실리사이드(ErSi)막, 이터븀 실리사이드(YbSi)막, 이트륨 실리사이드(YSi)막, 가돌리늄 실리사이드(GdSi)막, 터븀 실리사이드(TbSi)막, 디스프로슘 실리사이드(DySi)막, 홀뮴 실리사이드(HoSi)막, 툴륨 실리사이드(TmSi)막, 루테늄 실리사이드(LuSi)막, 팔라듐 실리사이드(PdSi)막, 오스뮴 실리사이드(OsSi)막, 이리듐 실리사이드(IrSi)막, 및 레늄 실리사이드(ReSi)막으로 이루어진 그룹 중에서 선택된 적어도 하나의 막을 포함할 수 있다.

또 다른 실시예들에서, 상기 게이트 구조체의 측벽들을 덮는 게이트 스페이서를 더 포함할 수 있다.

본 발명의 다른 태양은 핀 펫 소자의 제조방법을 제공한다. 이 방법은 기판 상에 예비 핀 바디를 형성하고, 상기 예비 핀 바디 상부를 가로지르며 상기 예비 핀 바디의 상부면 및 측벽들을 덮는 게이트 구조체를 형성하는 것을 포함한다. 상기 게이트 구조체의 측벽들을 덮는 게이트 스페이서를 형성한다. 상기 게이트 스페이서 및 상기 게이트 구조체를 식각마스크로 하여 상기 예비 핀 바디를 부분 식각하여 상기 게이트 구조체 하부에 위치한 상부 핀 바디 및 상기 상부 핀 바디 보다 낮은 레벨에 위치하는 하부 핀 바디를 형성하되, 상기 상부 핀 바디는 노출된 양 측벽들을 갖는다. 상기 노출된 상부 핀 바디의 측벽들 및 상기 상부 핀 바디 양 옆에 위치하는 상기 하부 핀 바디 상에 상기 상부 및 하부 핀 바디들과 쇼트키 배리어를 형성하는 금속 물질막으로 이루어진 소스/드레인을 형성한다.

본 발명의 몇몇 실시예들에서, 상기 예비 핀 바디는 실리콘(Si)막, 게르마늄(Ge)막, 실리콘 게르마늄(SiGe)막, 실리콘 게르마늄 카바이드(SiGeC)막, 또는 실리콘 카바이드(SiC)막으로 형성될 수 있다.

다른 실시예들에서, 상기 소스/드레인은 금속 실리사이드막으로 형성될 수 있다. 상기 금속 실리사이드막은 탄탈륨 실리사이드(TaSi)막, 타이타늄 실리사이드(TiSi)막, 텅스텐 실리사이드(WSi)막, 니켈 실리사이드(NiSi)막, 코발트 실리사이드(CoSi)막, 백금 실리사이드(PtSi)막, 에르븀 실리사이드(ErSi)막, 이터븀 실리사이드(YbSi)막, 이트륨 실리사이드(YSi)막, 가돌리늄 실리사이드(GdSi)막, 터븀 실리사이드(TbSi)막, 디스프로슘 실리사이드(DySi)막, 홀뮴 실리사이드(HoSi)막, 툴륨 실리사이드(TmSi)막, 루테늄 실리사이드(LuSi)막, 팔라듐 실리사이드(PdSi)막, 오스뮴 실리사이드(OsSi)막, 이리듐 실리사이드(IrSi)막, 및 레늄 실리사이드(ReSi)막로 이루어진 그룹 중에서 선택된 적어도 하나의 막을 포함할 수 있다.

또 다른 실시예들에서, 상기 소스/드레인을 형성하는 것은 상기 하부 및 상부 핀 바디들을 갖는 기판의 전면 상에 금속막을 형성하고, 상기 금속막을 갖는 기판을 열처리하여 상기 하부 및 상부 핀 바디들과 상기 금속막을 반응시키고, 미반응된 금속막을 제거하는 것을 포함할 수 있다.

또 다른 실시예들에서, 상기 소스/드레인은 상기 게이트 구조체의 측벽들과 자기정렬되거나, 또는 상기 게이트 구조체와 중첩되도록 형성될 수 있다.

본 발명의 또 다른 태양은 단 채널 길이를 갖는 쇼트키 배리어 핀 펫 소자의 제조방법을 제공한다. 이 방법은 기판 상에 핀 바디를 형성하는 것을 포함한다. 상기 핀 바디 상부를 가로지르며 상기 핀 바디의 상부면 및 측벽들을 덮는 희생 마스크를 형성한다. 상기 희생 마스크의 양옆에 위치하는 상기 핀 바디의 표면에 상기 핀 바디와 쇼트키 배리어를 형성하는 소스/드레인을 형성한다. 상기 희생 마스크의 측벽들을 감싸며 상기 핀 바디를 덮는 절연 패턴을 형성한다. 상기 희생 마스크를 제거하여 상기 핀 바디의 일부분을 노출시키는 개구부를 형성한다. 상기 노출된 핀 바디를 덮는 게이트 구조체를 형성한다.

본 발명의 몇몇 실시예들에서, 상기 핀 바디는 실리콘(Si)막, 게르마늄(Ge)막, 실리콘 게르마늄(SiGe)막, 실리콘 게르마늄 카바이드(SiGeC)막, 또는 실리콘 카바이드(SiC)막으로 형성될 수 있다.

다른 실시예들에서, 상기 소스/드레인은 금속막 또는 금속 실리사이드막으로 형성될 수 있다. 이 경우에, 상기 금속 실리사이드막은 탄탈륨 실리사이드(TaSi)막, 타이타늄 실리사이드(TiSi)막, 텅스텐 실리사이드(WSi)막, 니켈 실리사이드(NiSi)막, 코발트 실리사이드(CoSi)막, 백금 실리사이드(PtSi)막, 에르븀 실리사이드(ErSi)막, 이터븀 실리사이드(YbSi)막, 이트륨 실리사이드(YSi)막, 가돌리늄 실리사이드(GdSi)막, 터븀 실리사이드(TbSi)막, 디스프로슘 실리사이드(DySi)막, 홀뮴 실리사이드(HoSi)막, 툴륨 실리사이드(TmSi)막, 루테늄 실리사이드(LuSi)막, 팔라듐 실리사이드(PdSi)막, 오스뮴 실리사이드(OsSi)막, 이리듐 실리사이드(IrSi)막, 및 레늄 실리사이드(ReSi)막으로 이루어진 그룹 중에서 선택된 적어도 하나의 막을 포함할 수 있다.

또 다른 실시예들에서, 상기 소스/드레인을 형성하는 것은 상기 희생 마스크를 갖는 기판 상에 금속막을 형성하고, 상기 금속막을 갖는 기판을 열처리하여 상기 핀 바디와 상기 금속막을 반응시키고, 미반응된 금속막을 제거하는 것을 포함할 수 있다.

또 다른 실시예들에서, 상기 절연 패턴은 상기 희생 마스크에 대하여 식각선택비를 갖는 물질막으로 형성할 수 있다.

또 다른 실시예들에서, 상기 게이트 구조체는 차례로 적층된 게이트 절연막 및 게이트 전극으로 형성할 수 있다. 이 경우에, 상기 게이트 절연막은 화학 기상 증착법 또는 원자층 증착법에 의해 형성되고, 상기 게이트 전극은 실리콘막, 금속막, 및 금속 실리사이드막으로 이루어진 그룹 중에서 선택된 적어도 하나의 막으로 형성될 수 있다.

또 다른 실시예들에서, 상기 소스/드레인은 상기 게이트 구조체의 측벽들과 자기정렬되거나, 또는 상기 게이트 구조체와 중첩되도록 형성될 수 있다.

또 다른 실시예들에서, 상기 희생 마스크를 형성하는 것은 상기 핀 바디 상부를 가로지르며 상기 핀 바디의 상부면 및 측벽들을 덮는 예비 희생 마스크를 형성하되, 상기 예비 희생 마스크는 제1 폭을 갖도록 형성되고, 상기 핀 바디 상부를 상기 제1 폭 보다 작은 제2 폭으로 가로지르도록 상기 예비 희생 마스크를 등방성 식각하는 것을 포함할 수 있다.

이하, 첨부한 도면들을 참조하여 본 발명의 바람직한 실시 예들을 상세히 설명한다. 그러나, 본 발명은 여기서 설명되어지는 실시 예들에 한정되지 않고 다른 형태로 구체화될 수도 있다. 오히려, 여기서 소개되는 실시 예들은 개시된 내용이 철저하고 완전해질 수 있도록 그리고 당업자에게 본 발명의 사상이 충분히 전달될 수 있도록 하기 위해 제공되어지는 것이다. 도면들에 있어서, 층 및 영역들의 두께는 명확성을 기하여 위하여 과장되어진 것이다. 명세서 전체에 걸쳐서 동일한 참조 번호들은 동일한 구성요소들을 나타낸다.

도 1은 본 발명의 실시예들에 따른 핀 펫 소자를 나타낸 평면도이고, 도 2내지 도 5는 도 1의 I-I'선을 따라 취해진 단면도들이고, 도 6은 도 1의 II-II'선을 따라 취해진 단면도이다. 도 7은 본 발명의 다른 실시예들에 따른 핀 펫 소자를 나타낸 평면도이고, 도 8a 내지 도 12a는 도 7의 III-III'선을 따라 취해진 단면도들이고, 도 8b 내지 도 12b는 도 7의 IV-IV'선을 따라 취해진 단면도들이다.

먼저, 도 1, 도 5, 및 도 6을 참조하여 본 발명의 실시예들에 의한 핀 펫 소자의 구조를 설명하기로 한다.

도 1, 도 5, 및 도 6을 참조하면, 기판(100) 상에 적어도 하나의 하부 핀 바디(131)가 제공된다. 상기 기판(100)은 벌크 반도체 기판 또는 SOI(silicon on insulator) 기판 일 수 있다. 상기 기판(100)이 벌크 반도체 기판 인 경우에, 상기 하부 핀 바디(131)는 상기 기판(100)으로 이루어지고 상기 기판(100)으로부터 돌출될 수 있다. 이 경우에, 상기 하부 핀 바디(131)에 인접한 기판(100) 내에는 소자분리막이 제공될 수 있다. 이와는 달리, 상기 기판(100)이 SOI 기판으로 이루어진 경우에, 상기 기판(100)의 하부 영역은 반도체 기판이고, 상기 기판(100)의 상부 영역은 매립 절연막일 수 있다.

상기 하부 핀 바디(131) 상에 상기 하부 핀 바디(131)의 중심부로부터 상부로 연장되고 서로 마주보는 제1 및 제2 측벽들을 갖는 상부 핀 바디(132)가 제공된다. 상기 상부 핀 바디(132)의 상기 제1 및 제2 측벽들은 상기 하부 핀 바디(131)의 측벽들과 자기 정렬되도록 배치될 수 있다. 상기 하부 및 상부 핀 바디들(131, 132)은 핀 바디(105a)를 구성할 수 있다. 상기 하부 및 상부 핀 바디들(131, 132)은 같은 반도체 물질막으로 이루어질 수 있다. 예를 들어, 상기 하부 및 상부 핀 바디들(131, 132)은 실리콘(Si)막, 게르마늄(Ge)막, 실리콘 게르마늄(SiGe)막, 실리콘 게르마늄 카바이드(SiGeC)막, 또는 실리콘 카바이드(SiC)막으로 이루어질 수 있다.

상기 상부 핀 바디(132) 상부를 가로지르며 상기 상부 핀 바디(132)의 상부면 및 상기 제1 및 제2 측벽들을 덮는 게이트 구조체(110)가 제공된다. 상기 게이트 구조체(110)는 상기 상부 핀 바디(132)의 상부면 및 상기 제1 및 제2 측벽들을 덮으면서 가로지르며 상기 상부 핀 바디(132)의 상기 제1 및 제2 측벽들과 인접한 상기 하부 핀 바디(131)의 측벽들을 덮도록 연장될 수 있다. 상기 게이트 구조체(112)는 차례로 적층된 게이트 절연막(111), 게이트 전극(112), 및 하드 마스크(113)로 이루어질 수 있다. 상기 게이트 절연막(111)은 실리콘 산화막 또는 고유전막(high-k dielectric layer)일 수 있다. 상기 고유전막은 $(Ba_x, Sr_{1-x})TiO_3$(이하 BST라 함)막, TiO_2 막, Ta_2O_5막, ZrO_2막, Zr-실리케이트(Zr-silicate)막, HfO_2막, Hf-실리케이트막, Al_2O_3막, 및 Y_2O막으로 이루어진 그룹 중에서 선택된 적어도 하나의 막을 포함할 수 있다. 상기 게이트 전극(112)은 실리콘막, 금속 실리사이드막, 및 금속막으로 이루어진 그룹중에서 선택된 적어도 하나의 막을 포함할 수 있다. 상기 하드 마스크(113)는 실리콘 질화막 또는 실리콘 산화막일 수 있다.

한편, 상기 하드 마스크(113)는 생략될 수 있다. 이 경우에, 상기 게이트 구조체(110)는 차례로 적층된 게이트 절연막(111) 및 게이트 전극(112)으로 이루어질 수 있다.

상기 게이트 구조체(110)의 측벽들을 덮는 게이트 스페이서(121a)가 제공될 수 있다. 상기 게이트 스페이서(121a)는 실리콘 산화막 또는 실리콘 질화막을 포함할 수 있다.

상기 게이트 구조체(110)의 측벽들에 인접한 상기 상부 핀 바디(132)의 측벽들의 표면에 형성되고 상기 상부 핀 바디(132) 양 옆에 위치하는 상기 하부 핀 바디(131)의 상부 표면에 형성된 금속 물질막으로 이루어진 소스/드레인(140)이 제공된다. 상기 소스/드레인(140)은 상기 하부 및 상부 핀 바디들(131, 132)에 대하여 쇼트키 배리어를 형성할 수 있다. 예를

들어, 상기 소스/드레인(140)은 탄탈륨 실리사이드(TaSi)막, 타이타늄 실리사이드(TiSi)막, 텅스텐 실리사이드(WSi)막, 니켈 실리사이드(NiSi)막, 코발트 실리사이드(CoSi)막, 백금 실리사이드(PtSi)막, 에르븀 실리사이드(ErSi)막, 이터븀 실리사이드(YbSi)막, 이트륨 실리사이드(YSi)막, 가돌리늄 실리사이드(GdSi)막, 터븀 실리사이드(TbSi)막, 디스프로슘 실리사이드(DySi)막, 홀뮴 실리사이드(HoSi)막, 툴륨 실리사이드(TmSi)막, 루테늄 실리사이드(LuSi)막, 팔라듐 실리사이드(PdSi)막, 오스뮴 실리사이드(OsSi)막, 이리듐 실리사이드(IrSi)막, 및 레늄 실리사이드(ReSi)막으로 이루어진 그룹 중에서 선택된 적어도 하나의 막을 포함하는 금속 실리사이드막으로 이루어질 수 있다. 상기 소스/드레인(140)은 얇은 접합(shallow junction)을 형성하면서 상기 게이트 전극(112)의 측벽들과 자기정렬되거나, 상기 게이트 전극(112)과 중첩되도록 형성될 수 있다.

따라서, 상기 게이트 구조체(110)의 측벽들에 인접한 상기 상부 핀 바디(132)의 측벽들의 표면에 제공되고 상기 상부 핀 바디(132) 양 옆에 위치하는 상기 하부 핀 바디(131)의 상부 표면으로 연장된 금속 물질막으로 이루어진 상기 소스/드레인(140)이 제공된다. 그 결과, 상기 소스/드레인(140)을 포함하는 쇼트키 배리어 핀 펫 소자(schoutky barrier finFET 소자)가 제공될 수 있다. 이와 같이 제작된 쇼트키 배리어 핀 펫 소자는 종래의 쇼트키 배리어 모스펫 소자보다 짧은 채널 길이를 가질 수 있다. 더 나아가서, 상기 핀 바디(105a)를 채널 영역으로 이용하기 때문에 종래의 쇼트키 배리어 모스펫 소자보다 증가된 채널 폭을 가질 수 있다. 또한, 핀의 두께 및 채널 길이에 상관없이 소스/드레인(140) 전체가 금속 물질막으로 이루어질 수 있다. 즉, 상기 게이트 전극(112) 하부의 채널 영역에 인접한 상기 소스/드레인(140)은 금속 물질막으로 이루어지므로, 상기 소스/드레인(140)의 접합 누설전류(junction leakage)를 최소화할 수 있다. 또한, 상기 소스/드레인(140)은 얇은 접합(shallow junction)을 형성하면서, 상기 게이트 구조체(110)의 측벽들과 자기정렬되거나, 상기 게이트 구조체(110)와 중첩될 수 있다.

결과적으로, 전기적으로 안정된 단 채널 길이를 갖는 쇼트키 배리어 핀 펫 소자를 제공할 수 있다. 더 나아가서, 소자의 전류 구동 능력을 향상시킬 수 있고, 소자의 동작 속도를 향상시킬 수 있다.

다음으로, 도 1 내지 도 6을 참조하여 본 발명의 실시예들에 따른 핀 펫 소자의 제조방법을 설명하기로 한다.

도 1 및 도 2를 참조하면, 기판(100)을 준비한다. 상기 기판(100) 상에 적어도 하나의 예비 핀 바디(105)를 형성한다. 상기 예비 핀 바디(105)는 반도체 물질막으로 형성될 수 있다. 예를 들어, 상기 예비 핀 바디(105)는 실리콘(Si)막, 게르마늄(Ge)막, 실리콘 게르마늄(SiGe)막, 실리콘 게르마늄 카바이드(SiGeC)막, 또는 실리콘 카바이드(SiC)막으로 형성될 수 있다. 상기 예비 핀 바디(105)를 형성하는 방법은 상기 기판(100)의 종류에 따라 달라질 수 있다. 예를 들면, 상기 기판(100)이 벌크 반도체 기판일 경우에, 상기 기판(100)으로 이루어지고 상기 기판(100)으로부터 돌출된 상기 예비 핀 바디(105)를 형성할 수 있다. 이 경우에, 상기 예비 핀 바디(105)에 인접한 기판(100) 내에는 소자분리막이 제공될 수 있다. 따라서, 상기 예비 핀 바디(105)와 인접한 다른 예비 핀 바디와는 상기 기판(100) 내에 제공된 소자분리막에 의해 분리될 수 있다. 이와는 달리, 상기 기판(100)이 SOI기판으로 이루어진 경우에, 상기 기판(100)의 하부 영역은 반도체 기판이고, 상기 기판(100)의 상부 영역은 매립 절연막일 수 있다. 따라서, 상기 예비 핀 바디(105)는 매립 절연막 상에 형성되어 인접한 다른 예비 핀 바디들과 분리 될 수 있다.

상기 예비 핀 바디(105) 상부를 가로지르며 상기 예비 핀 바디(105)의 상부면 및 측벽들을 덮는 게이트 구조체(112)를 형성한다. 상기 게이트 구조체(112)는 차례로 적층된 게이트 절연막(111), 게이트 전극(112), 및 하드 마스크(113)로 형성될 수 있다. 상기 게이트 절연막(111)은 실리콘 산화막 또는 고유전막(high-k dielectric layer)으로 형성될 수 있다. 상기 고유전막은 $(Ba_x, Sr_{1-x})TiO_3$(이하 BST라 함)막, TiO_2 막, Ta_2O_5막, ZrO_2막, Zr-실리케이트(Zr-silicate)막, HfO_2막, Hf-실리케이트막, Al_2O_3막, 및 Y_2O막으로 이루어진 그룹 중에서 선택된 적어도 하나의 막을 포함할 수 있다. 상기 게이트 전극(112)은 실리콘막, 금속 실리사이드막, 및 금속막으로 이루어진 그룹중에서 선택된 적어도 하나의 막으로 형성될 수 있다. 상기 하드 마스크(113)는 실리콘 질화막 또는 실리콘 산화막으로 형성될 수 있다.

한편, 상기 하드 마스크(113)는 생략될 수 있다. 상기 하드 마스크(113)가 생략되는 경우에, 상기 게이트 구조체(110)는 차례로 적층된 상기 게이트 절연막(111) 및 상기 게이트 전극(112)으로 형성될 수 있다.

도 1 및 도 3을 참조하면, 상기 게이트 구조체(110)의 측벽들을 덮는 게이트 스페이서(121a)를 형성함과 아울러 상기 예비 핀 바디(105)의 측벽들을 덮는 핀 바디 스페이서(121b)를 형성한다. 상기 게이트 스페이서(121a) 및 핀 바디 스페이서(121b)를 형성하는 것은 상기 게이트 구조체(110)를 갖는 기판 상에 콘포멀한 스페이서 절연막을 형성하고, 상기 스페이서 절연막을 이방성 식각하는 것을 포함할 수 있다. 이와는 달리, 상기 게이트 전극(112)이 실리콘막으로 형성되는 경우에,

상기 게이트 구조체(110)를 갖는 기판을 열산화시키어 상기 게이트 전극(112) 및 상기 예비 핀 바디(105) 상에 열산화막을 형성하고, 상기 열산화막을 이방성 식각하는 것을 포함할 수 있다. 그 결과, 상기 게이트 구조체(110) 및 상기 게이트 스페이서(121a)가 형성된 영역을 제외한 상기 예비 핀 바디(105)의 상부면은 노출될 수 있다.

도 1 및 도 4를 참조하면, 상기 게이트 구조체(110) 및 상기 게이트 스페이서(121a)를 식각마스크로 하여 상기 예비 핀 바디(105)를 부분 식각하여 상기 게이트 구조체(110) 하부에 위치하는 상부 핀 바디(132) 및 상기 상부 핀 바디(132) 보다 낮은 레벨에 위치하는 하부 핀 바디(131)를 형성한다. 상기 하부 및 상부 핀 바디들(131, 132)은 핀 바디(105a)를 구성할 수 있다. 즉, 상기 게이트 구조체(110)의 양 옆에 위치하는 상기 예비 핀 바디(105)를 부분 식각하여 리세스 영역(125)을 형성할 수 있다. 그 결과, 상기 하부 및 상부 핀 바디들(131, 132)로 이루어진 상기 핀 바디(105a)가 형성될 수 있다.

도 1, 도 5, 및 도 6을 참조하면, 상기 게이트 구조체(110)의 측벽들에 인접한 상기 상부 핀 바디(132)의 측벽들의 표면들 및 상기 상부 핀 바디(132) 양 옆에 위치하는 상기 하부 핀 바디(131)의 표면에 소스/드레인(140)을 형성한다. 이 경우에, 상기 소스/드레인(140)은 상기 하부 및 상부 핀 바디들(131, 132)에 대하여 쇼트키 배리어를 형성하는 금속 실리사이드막과 같은 금속 물질막으로 형성된다. 구체적으로, 상기 소스/드레인(140)을 형성하는 것은 상기 핀 바디(105a)를 갖는 기판 상에 금속막을 형성하고, 상기 핀 바디(105a)와 상기 금속막을 반응시키기 위한 열처리 공정을 수행하여 금속 실리사이드막을 형성하고, 미반응된 금속막을 제거하는 것을 포함할 수 있다. 이 경우에, 상기 금속막이 상기 핀 바디(105a)와 반응하여 상기 금속 실리사이드막으로 형성되면서, 상기 금속 실리사이드막의 두께는 상기 게이트 구조체(110) 하부를 향하도록 증가될 수 있다. 즉, 상기 상부 핀 바디(132)의 측벽들의 표면들에 형성된 금속 실리사이드막들은 상기 게이트 구조체(110) 하부의 채널 영역을 사이에 두고 서로 마주보는 형상으로 형성된다. 따라서, 상기 금속 실리사이드막의 두께가 증가함으로 인하여, 상기 금속 실리사이드막과 상기 게이트 구조체(110)의 측벽들이 자기정렬되거나, 또는 상기 금속 실리사이드막과 상기 게이트 구조체(110)가 중첩되도록 상기 금속 실리사이드막을 형성할 수 있다. 상기 금속 실리사이드막의 두께는 상기 금속막의 종류, 상기 금속막의 최초 두께, 상기 열처리 공정의 온도 및 시간의 함수이므로 상기 금속 실리사이드막의 두께를 조절할 수 있다. 따라서, 핀의 두께 및 채널 길이에 상관없이 상기 소스/드레인(140) 전체를 금속 실리사이드막으로 형성할 수 있다. 상기 금속 실리사이드막 자체가 소스/드레인(140)이 되므로, 소스 및 드레인을 얇은 접합(shallow junction)으로 형성할 수 있고, 상기 소스/드레인(140)의 접합 누설전류(junction leakage)를 최소화할 수 있다. 상기 소스/드레인(140)은 얇은 접합(shallow junction)을 형성하면서, 상기 게이트 구조체(110)의 측벽들과 자기정렬되거나, 상기 게이트 구조체(110)와 중첩되도록 형성될 수 있다. 따라서, 단 채널 길이를 갖는 쇼트키 배리어 핀 펫 소자가 형성될 수 있다.

상기 소스/드레인(140)은 탄탈륨 실리사이드(TaSi)막, 타이타늄 실리사이드(TiSi)막, 텅스텐 실리사이드(WSi)막, 니켈 실리사이드(NiSi)막, 코발트 실리사이드(CoSi)막, 백금 실리사이드(PtSi)막, 에르븀 실리사이드(ErSi)막, 이터븀 실리사이드(YbSi)막, 이트륨 실리사이드(YSi)막, 가돌리늄 실리사이드(GdSi)막, 터븀 실리사이드(TbSi)막, 디스프로슘 실리사이드(DySi)막, 홀뮴 실리사이드(HoSi)막, 툴륨 실리사이드(TmSi)막, 루테늄 실리사이드(LuSi)막, 팔라듐 실리사이드(PdSi)막, 오스뮴 실리사이드(OsSi)막, 이리듐 실리사이드(IrSi)막, 및 레늄 실리사이드(ReSi)막으로 이루어진 그룹 중에서 선택된 적어도 하나의 막을 포함하는 금속 실리사이드막으로 형성될 수 있다.

도면에 도시되지 않았지만, 상기 소스/드레인(140)을 갖는 기판 상에 통상의 금속 배선 공정을 진행할 수 있다. 다시 말하면, 상기 소스/드레인(140)을 갖는 기판 상에 층간절연막을 형성하고, 상기 층간절연막을 관통하며 상기 소스/드레인(140)에 전기적으로 접속된 콘택 구조체를 형성하고, 상기 층간절연막 상에 상기 콘택 구조체를 덮는 금속 배선을 형성할 수 있다. 상기 금속 배선 공정을 진행하는 경우에, 상기 핀 바디 스페이서(121b)를 통상의 식각공정으로 제거한 후에, 상기 금속 배선 공정을 진행할 수도 있다.

결과적으로, 상기 게이트 구조체(110)의 측벽들에 인접한 상기 상부 핀 바디(132)의 측벽들의 표면에 제공되고 상기 상부 핀 바디(132) 양 옆에 위치하는 상기 하부 핀 바디(131)의 상부 표면으로 연장된 금속 물질막으로 이루어진 상기 소스/드레인(140)이 형성된다. 따라서, 상기 소스/드레인(140)을 포함하는 쇼트키 배리어 핀 펫 소자(schottky barrier finFET 소자)가 형성될 수 있다. 이와 같이 제작된 쇼트키 배리어 핀 펫 소자는 종래의 쇼트키 배리어 모스펫 소자보다 짧은 채널 길이를 가질 수 있다. 더 나아가서, 상기 핀 바디(105a)를 채널 영역으로 이용하기 때문에 종래의 쇼트키 배리어 모스펫 소자보다 증가된 채널 폭을 가질 수 있다. 또한, 핀의 두께 및 채널 길이에 상관없이 소스/드레인(140) 전체를 금속 물질막으로 형성할 수 있다. 상기 게이트 전극(112) 하부의 채널 영역에 인접한 상기 소스/드레인(140)은 금속 실리사이드막과 같은 금속 물질막으로 형성되므로, 상기 소스/드레인(140)의 접합 누설전류(junction leakage)를 최소화할 수 있다. 또한, 상기 소스/드레인(140)은 얇은 접합을 형성하면서 상기 게이트 구조체(110)의 측벽들과 자기정렬되거나, 상기 게이트 구조체(110)와 중첩되도록 형성될 수 있다.

결과적으로, 전기적으로 안정된 단 채널 길이를 갖는 쇼트키 배리어 핀 펫 소자를 형성할 수 있다. 더 나아가서, 소자의 전류 구동 능력을 향상시킬 수 있고, 소자의 동작 속도를 향상시킬 수 있다.

다음으로, 도 7, 도 8a 내지 도 12a, 및 도 8b 내지 도 12b를 참조하여 본 발명의 다른 실시예들에 따른 핀 펫 소자의 제조 방법들을 설명하기로 한다.

도 7, 도 8a, 및 도 8b를 참조하면, 기판(200)을 준비한다. 상기 기판(200) 상에 적어도 하나의 핀 바디(205)를 형성한다. 상기 핀 바디(205)는 반도체 물질막으로 형성될 수 있다. 핀 바디(205)를 형성하는 방법은 도 1 및 도 2를 참조하여 설명한 상기 예비 핀 바디(105)를 형성하는 방법과 실질적으로 동일하므로 상기 핀 바디(205)를 형성하기 위한 자세한 방법은 생략하기로 한다. 상기 핀 바디(205)는 실리콘(Si)막, 게르마늄(Ge)막, 실리콘 게르마늄(SiGe)막, 실리콘 게르마늄 카바이드(SiGeC)막, 또는 실리콘 카바이드(SiC)막으로 형성될 수 있다.

상기 핀 바디(205) 상부를 가로지르며 상기 핀 바디(205)의 상부면 및 측벽들을 덮는 희생 마스크(210)를 형성한다. 상기 희생 마스크(210)는 실리콘 산화막 또는 실리콘 질화막과 같은 절연막으로 형성될 수 있다.

한편, 상기 희생 마스크(210)는 사진 공정에 의해 형성될 수 있는 선 폭 보다 작은 선 폭을 갖도록 형성될 수 있다. 구체적으로, 상기 핀 바디(205) 상부를 가로지르며 상기 핀 바디(205)의 상부면 및 측벽들을 덮는 예비 희생 마스크(209)를 형성하고, 이어서 상기 예비 희생 마스크(209)를 등방성 식각하여 상기 예비 희생 마스크(209)의 폭 보다 작은 폭을 갖는 희생 마스크(210)를 형성할 수 있다.

도 7, 도 9a, 및 도 9b를 참조하면, 상기 희생 마스크(210) 양 옆에 위치하는 상기 핀 바디(205)의 표면에 소스/드레인(215)을 형성한다. 즉, 상기 소스 및 드레인(215)은 상기 희생 마스크(210)를 사이에 두고 이격될 수 있다. 상기 소스/드레인(215)은 상기 핀 바디(205)에 대하여 쇼트키 배리어를 형성하는 금속물질막으로 형성된다. 상기 금속 물질막은 금속막 또는 금속 실리사이드막일 수 있다. 상기 금속 실리사이드막으로 이루어진 상기 소스/드레인(215)을 형성하는 것은 상기 핀 바디(205)를 갖는 기판 상에 금속막을 형성하고, 상기 핀 바디(205)와 상기 금속막을 반응시키기 위한 열처리 공정을 수행하여 금속 실리사이드막을 형성하고, 미반응된 금속막을 제거하는 것을 포함할 수 있다. 이 경우에, 상기 금속 실리사이드막의 두께는 상기 금속막의 종류, 상기 금속막의 최초 두께, 상기 열처리 공정의 온도 및 시간에 따라 조절될 수 있다. 상기 소스/드레인(215)은 탄탈륨 실리사이드(TaSi)막, 타이타늄 실리사이드(TiSi)막, 텅스텐 실리사이드(WSi)막, 니켈 실리사이드(NiSi)막, 코발트 실리사이드(CoSi)막, 백금 실리사이드(PtSi)막, 에르븀 실리사이드(ErSi)막, 이터븀 실리사이드(YbSi)막, 이트륨 실리사이드(YSi)막, 가돌리늄 실리사이드(GdSi)막, 터븀 실리사이드(TbSi)막, 디스프로슘 실리사이드(DySi)막, 홀뮴 실리사이드(HoSi)막, 툴륨 실리사이드(TmSi)막, 루테늄 실리사이드(LuSi)막, 팔라듐 실리사이드(PdSi)막, 오스뮴 실리사이드(OsSi)막, 이리듐 실리사이드(IrSi)막, 및 레늄 실리사이드(ReSi)막으로 이루어진 그룹 중에서 선택된 적어도 하나의 막을 포함하는 금속 실리사이드막으로 형성될 수 있다.

도 7, 도 10a, 및 도 10b를 참조하면, 상기 희생 마스크(210)의 측벽들을 감싸며 상기 핀 바디(205)를 덮는 절연 패턴(220)을 형성한다. 상기 절연 패턴(220)은 상기 희생 마스크(210)에 대하여 식각 선택비를 갖는 물질막으로 형성될 수 있다. 예를 들어, 상기 희생 마스크(210)가 실리콘 산화막으로 형성되는 경우에, 상기 절연 패턴(220)은 실리콘 질화막으로 형성될 수 있다. 이와는 달리, 상기 희생 마스크(210)가 실리콘 질화막으로 형성되는 경우에, 상기 절연 패턴(220)은 실리콘 산화막으로 형성될 수 있다.

이어서, 상기 희생 마스크(210)를 선택적으로 제거하여 상기 핀 바디(205)의 일부분을 노출시키는 개구부를 형성한다. 상기 희생 마스크(210)는 통상의 식각 공정을 사용하여 제거할 수 있다. 상기 개구부는 제1 폭(W1)을 갖도록 형성될 수 있다.

한편, 상기 희생 마스크(210)를 식각 공정으로 제거하는 동안에 상기 절연 패턴(220)의 소정 부분이 식각 될 수 있다. 그 결과, 상기 개구부는 상기 제1 폭(W1) 보다 큰 상기 제2 폭(W2)을 가질 수 있다. 따라서, 상기 소스/드레인(215)의 소정 영역이 노출될 수 있다.

도 7, 도 11a, 및 도 11b를 참조하면, 상기 개구부에 의해 노출된 상기 핀 바디(205)를 덮는 게이트 구조체(225)를 형성한다. 상기 게이트 구조체(225)는 차례로 적층된 게이트 절연막(226) 및 게이트 전극(227)으로 형성될 수 있다. 상기 게이트 절연막(226)은 화학 기상 증착법 또는 원자층 증착법에 의해 형성될 수 있다. 예를 들어, 상기 게이트 절연막(226)은 실리콘 산화막, 실리콘 질화막, 또는 고유전막(high-k dielectric layer)으로 형성될 수 있다. 상기 고유전막은 (Ba_x, Sr_{1-x})

TiO_3(이하 BST라 함)막, TiO_2 막, Ta_2O_5막, ZrO_2막, Zr-실리케이트(Zr-silicate)막, HfO_2막, Hf-실리케이트막, Al_2O_3 막, 및 Y_2O막으로 이루어진 그룹 중에서 선택된 적어도 하나의 막을 포함할 수 있다. 상기 게이트 전극(227)은 실리콘막, 금속 실리사이드막, 및 금속막으로 이루어진 그룹중에서 선택된 적어도 하나의 막으로 형성될 수 있다.

한편, 상기 게이트 전극(227)은 텅스텐과 같은 금속막으로 형성할 수 있다. 다시 말하면, 상기 소스/드레인(215)을 형성한 후에, 상기 게이트 전극(227)을 형성함으로 인하여, 상기 게이트 전극(227)을 단일 금속막으로 형성할 수 있다. 종래의 다결정 실리콘막을 게이트 전극으로 사용하는 모스펫(MOSFET)에서는 게이트 절연막의 전기적인 등가두께(electrical equivalent thickness)를 증가시켜 구동 전류를 감소시키는 다결정 실리콘 공핍 현상이 발생하여 소자의 특성이 열화될 수 있다. 그러나, 상기 게이트 전극(227)을 금속막으로 형성할 수 있기 때문에 다결정 실리콘 공핍 현상이 발생하는 것을 방지할 수 있다.

상기 게이트 구조체(225)를 형성하는 것은 상기 절연 패턴(220)을 갖는 기판 상에 콘포멀한 예비 게이트 절연막을 형성하고, 상기 예비 게이트 절연막을 갖는 기판 상에 상기 개구부를 채우는 게이트 도전막을 형성하고, 상기 절연 패턴(220)의 상부면이 노출될때까지 상기 게이트 도전막을 평탄화하여 상기 개구부 내에 잔존하는 게이트 전극(227) 및 상기 게이트 전극(227)의 하부 및 측벽에 잔존하는 게이트 절연막(227)을 형성할 수 있다. 그 결과, 상기 핀 바디(205) 상에 형성된 상기 소스/드레인(215)을 포함하는 핀 펫 소자(FinFET device)가 형성될 수 있다. 또한, 상기 소스/드레인(215) 사이의 채널 영역 상부에 상기 게이트 절연막(226) 및 상기 게이트 전극(227)이 형성될 수 있다. 더 나아가서, 상기 게이트 전극(227)의 측벽들과 상기 소스/드레인(215)은 자기정렬되거나, 또는 상기 게이트 전극(227)과 상기 소스/드레인(215)은 중첩될 수 있다.

도 7, 도 12a 및 도 12b를 참조하면, 상기 게이트 구조체(225)를 갖는 기판 상에 층간절연막(240)을 형성하고, 상기 층간절연막(240) 및 상기 절연 패턴(220)을 관통하며 상기 소스/드레인(215)과 전기적으로 접속된 콘택 구조체들(245)를 형성할 수 있다. 이어서, 상기 층간절연막(240) 상에 상기 콘택 구조체들(245)를 덮는 금속 배선(250)을 형성할 수 있다.

한편, 상기 절연 패턴(220)을 선택적으로 제거한 후에, 층간절연막(240)을 형성하고, 상기 층간절연막(240)을 관통하며 상기 소스/드레인(215)과 전기적으로 접속된 콘택 구조체들(245)를 형성할 수 있다.

본 발명에서, 도 8a 및 도 8b를 참조하여 설명한 상기 희생 마스크(210)를 사진 공정에 의해 구현될 수 있는 선 폭 보다 작은 선 폭을 갖도록 형성할 수 있기 때문에, 결과적으로 상기 소스/드레인(215) 사이의 채널 길이를 짧게 형성할 수 있으며, 상기 게이트 전극(227)을 짧은 선 폭을 갖도록 형성할 수 있다. 따라서, 종래의 모스펫 소자보다 짧은 채널 길이를 갖는 소자를 형성할 수 있다.

또한, 금속 물질막으로 이루어진 상기 소스/드레인(215)은 상기 게이트 구조체(225)의 측벽들과 자기정렬되거나, 또는 상기 게이트 구조체(225)와 중첩될 수 있다. 그 결과, 쇼트키 베리어 핀 펫 소자가 형성될 수 있다.

또한, 상기 핀 바디(205)를 채널 영역으로 이용하기 때문에 종래의 쇼트키 배리어 모스 펫 소자보다 증가된 채널 폭을 갖도록 형성할 수 있다.

따라서, 소자의 전류 구동 능력을 향상시킬 수 있고, 소자의 동작 속도를 향상시킬 수 있다.

발명의 효과

상술한 바와 같이 본 발명에 따르면, 금속 물질막으로 이루어진 소스/드레인을 포함하는 쇼트키 배리어 핀 펫 소자(schottky barrier finFET 소자)를 제공할 수 있다. 이와 같은 쇼트키 배리어 핀 펫 소자는 짧은 채널 길이 및 증가된 채널 폭을 가질 수 있다. 본 발명에서, 게이트 전극 하부의 채널 영역에 인접한 소스/드레인은 핀의 두께 및 채널 길이에 상관없이 금속 물질막으로 이루어질 수 있다. 또한, 본 발명의 쇼트키 베리어 핀 펫 소자의 소스/드레인은 얇은 접합을 형성하면서 게이트 전극의 측벽들과 자기정렬되거나, 게이트 구조체과 중첩되도록 제공될 수 있다. 따라서, 전기적으로 안정된 단 채널 길이를 갖는 쇼트키 배리어 핀 펫 소자를 제공할 수 있다. 또한, 소자의 전류 구동 능력을 향상시킬 수 있고, 소자의 동작 속도를 향상시킬 수 있다.

도면의 간단한 설명

도 1은 본 발명의 실시예들에 따른 핀 펫 소자를 나타낸 평면도이다.

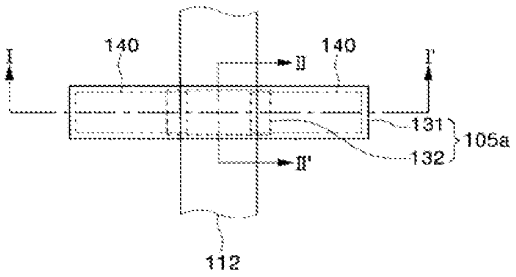
도 2내지 도 6은 본 발명의 실시예들에 따른 핀 펫 소자의 제조방법들을 나타낸 단면도들이다.

도 7은 본 발명의 다른 실시예들에 따른 핀 펫 소자를 나타낸 평면도이다.

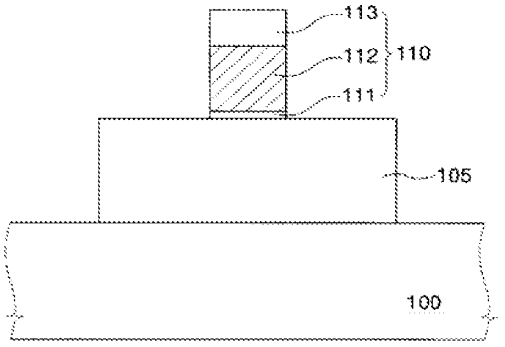
도 8a 내지 도 12a, 및 도 8b 내지 도 12b는 본 발명의 다른 실시예들에 따른 핀 펫 소자의 제조방법들을 나타낸 단면도들이다.

도면

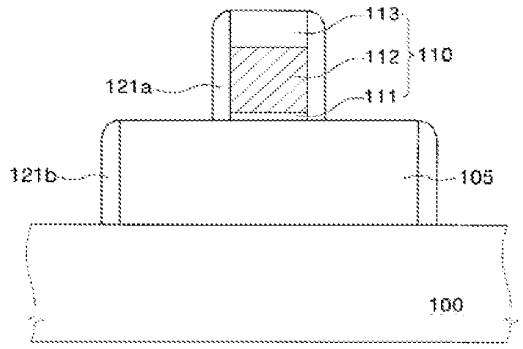
도면1



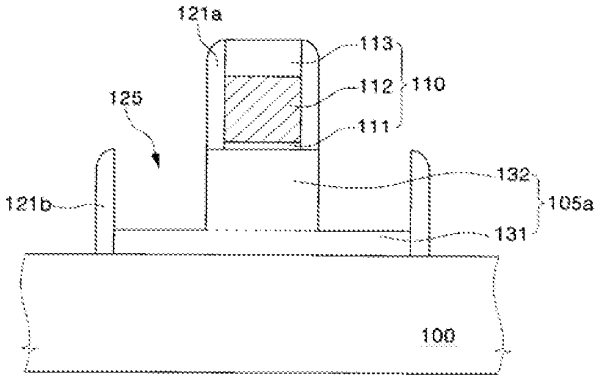
도면2



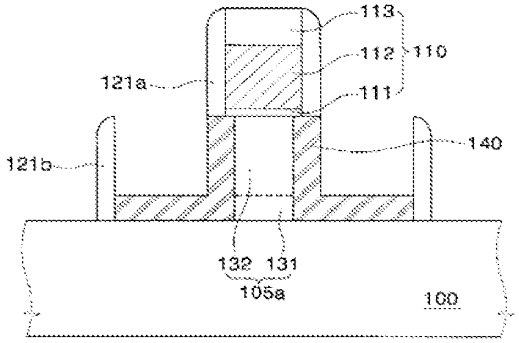
도면3


113
112
110
111
121a
121b
105
100

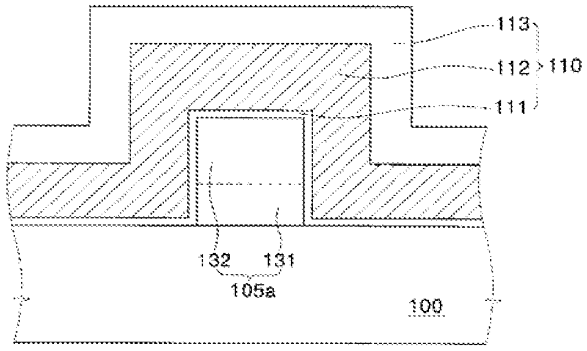
도면4


121a
113
112
110
111
125
132
105a
121b
131
100

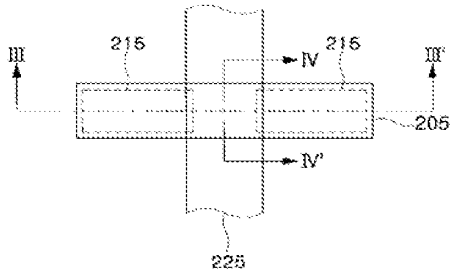
도면5


113
112
110
121a
111
140
121b
132
131
105a
100

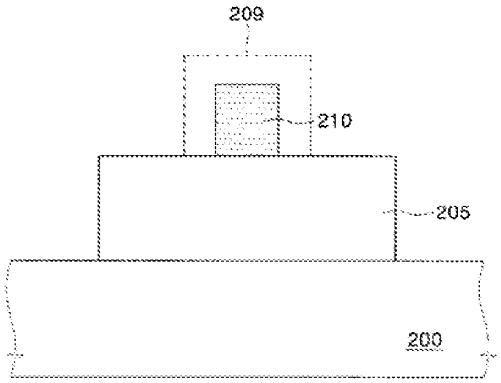
도면6


113
112
110
111
132
131
105a
100

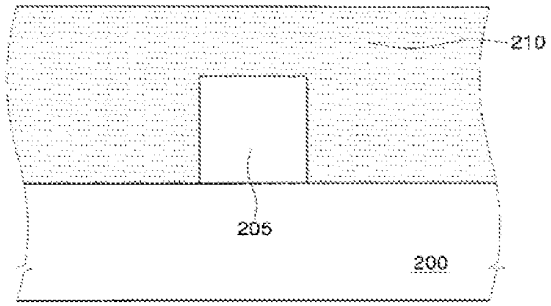
도면7


III
215
IV
215
III'
205
IV'
225

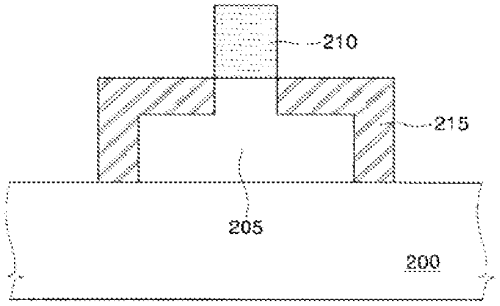
도면8a


209
210
205
200

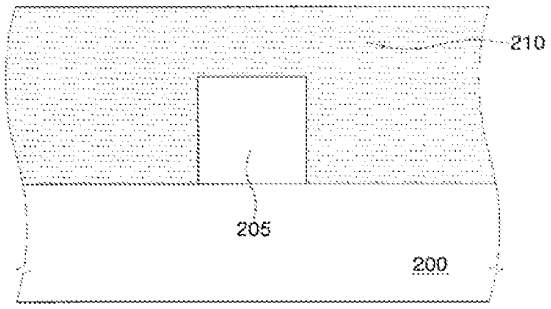
도면8b



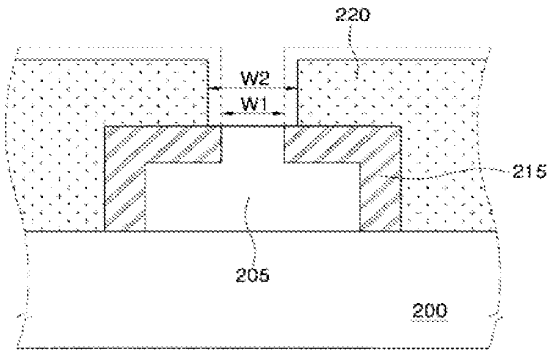
도면9a



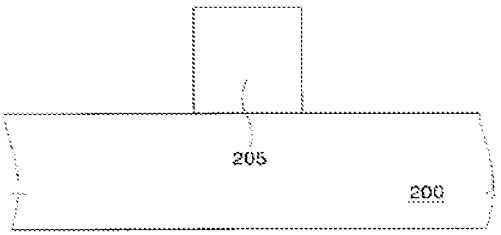
도면9b



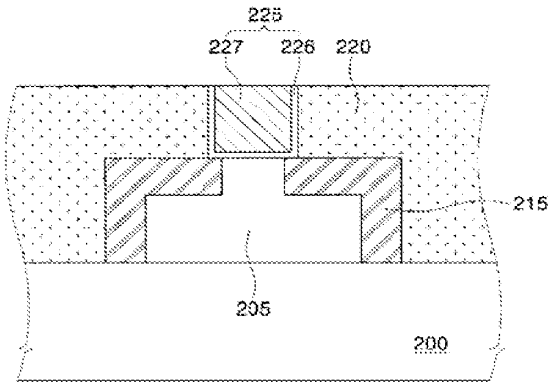
도면10a



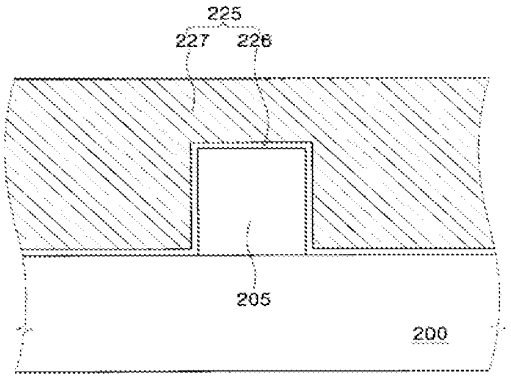
도면10b



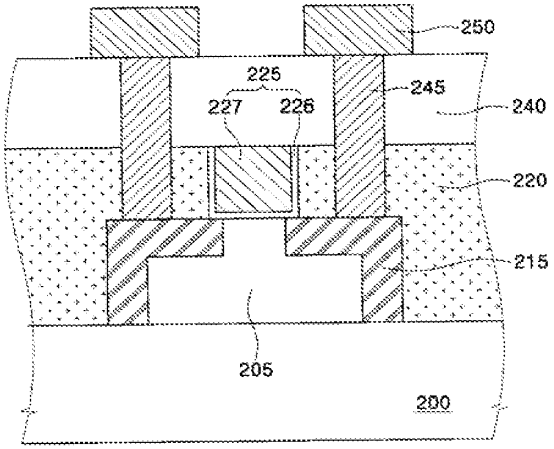
도면11a



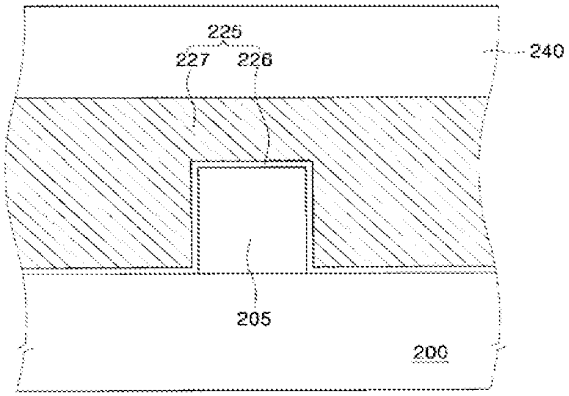
도면11b



도면12a



도면12b



KOREAN PATENT ABSTRACTS XML 1(1-1)

Print Save Error Report

(19) KOREAN INTELLECTUAL PROPERTY OFFICE

KOREAN PATENT ABSTRACTS

(11) Publication number: 1020040050519 A
(43) Publication date: 16.06.2004

(21) Application number: 1020020078371
(22) Application date: 10.12.2002

(51) Int. Cl: H01L 27/11

(71) Applicant: • HYNIX SEMICONDUCTOR INC.
(72) Inventor: • LEE, CHANG JIN

(54) METHOD FOR MANUFACTURING SRAM DEVICE

(57) Abstract:

PURPOSE: A method for manufacturing an SRAM(Static Random Access Memory) device is provided to prevent the generation of dislocation in RTP(Rapid Thermal Processing) and lessen the stress due to a BLC(Bit Line Contact) nitride layer by using a buffer oxide layer.

CONSTITUTION: A gate(5) is formed on a semiconductor substrate(1). An oxide layer(7) and a nitride layer(8) are sequentially formed on the entire surface of the resultant structure. A spacer(9) is formed at both sidewalls of the gate by selectively etching the nitride and oxide layer. A source/drain region are formed at both sides of the gate by using the residual oxide layer as a mask. A buffer oxide layer(10) is formed on the resultant structure. An RTP is carried out on the resultant structure for



(19)대한민국특허청(KR)
(12) 공개특허공보(A)

(51) 。Int. Cl.[7]
H01L 27/11

(11) 공개번호 10-2004-0050519
(43) 공개일자 2004년06월16일

(21) 출원번호 10-2002-0078371
(22) 출원일자 2002년12월10일

(71) 출원인 주식회사 하이닉스반도체
경기 이천시 부발읍 아미리 산136-1

(72) 발명자 이창진
경기도이천시증포동신한아파트108동1504호

(74) 대리인 강성배

심사청구 : 있음

(54) 에스램 소자의 제조방법

요약

본 발명은 에스램(SRAM) 소자의 제조방법을 개시한다. 개시된 본 발명의 에스램 소자의 제조방법은, 반도체 기판 상에 게이트를 형성하는 단계와, 상기 게이트를 포함한 기판 전 영역 상에 산화막과 질화막을 차례로 형성하는 단계와, 상기 산화막의 소정 두께가 잔류되도록 질화막과 산화막을 스페이서 식각하여 게이트의 양측벽에 스페이서를 형성하는 단계와, 상기 잔류된 산화막을 버퍼막으로 이용하여 스페이서를 포함한 게이트 양측의 기판 내에 소오스/드레인 이온주입을 수행하는 단계와, 상기 기판 표면에 잔류된 산화막을 제거하는 단계와, 상기 기판 결과물 상에 버퍼용 산화막을 형성하고 인-시튜로 N2 분위기 및 850℃에서 20분간 어닐링을 수행하는 단계와, 상기 소오스/드레인 이온주입된 도펀트가 활성화되도록 950℃에서 20초간 급속열공정을 수행하는 단계와, 상기 버퍼용 산화막 상에 BLC(Bit-Line Contact) 질화막을 증착하는 단계를 포함하며, 여기서, 상기 버퍼용 산화막은 680~830℃의 온도범위에서 80~120Å 두께로 형성하되, CVD 방식, 습식 또는 건식 산화 방식에 따라 형성한다. 본 발명에 따르면, 버퍼용 산화막의 형성시에 650℃ 이상의 열을 가해줌으로써 후속 RTP 공정시에 디스로케이션의 발생을 억제시킬 수 있으며, 아울러, 2단계의 어닐링을 통해 누설 특성을 개선시킬 수 있고, 또한, 버퍼용 산화막의 형성을 통해 BLC 질화막의 적용에 따른 스트레스를 완화시킬 수 있다.

대표도

도 1d

명세서

도면의 간단한 설명

도 1a 내지 도 1d는 본 발명의 실시예에 따른 에스램 소자의 제조방법을 설명하기 위한 공정별 단면도.

도 2는 소오스/드레인 이온주입 후의 어닐링 온도에 의존하는 디스로케이션 발생에 대한 임계 스트레스를 도시한 그래프.

도 3은 N+ 드레인에서 P+ 기판으로의 누설 전류 특성을 도시한 그래프.

* 도면의 주요 부분에 대한 부호의 설명 *

1 : 반도체 기판 2 : 게이트산화막

3 : 폴리실리콘막 4 : 캡핑질화막

5 : 게이트 6 : 산화막

7 : 스페이서 산화막 8 : 스페이서 질화막

9 : 스페이서 10 : 버퍼용 산화막

11 : BLC 질화막

발명의 상세한 설명

발명의 목적

발명이 속하는 기술 및 그 분야의 종래기술

본 발명은 에스램 소자의 제조방법에 관한 것으로, 특히, 도펀트 활성화를 위한 급속열공정시의 디스로케이션 발생을 방지하면서 BLC(Bit-Line Contact) 질화막 적용에 따른 스트레스를 완화시키기 위한 방법에 관한 것이다.

주지된 바와 같이, 에스램(SRAM : Static Random Access Memory) 소자는 빠른 스피드로 동작하며, 소비전력이 낮고, 단순한 동작 방식으로 구동된다는 잇점이 있다. 또한, 에스램 소자는 디램(DRAM : Dynamic RAM) 소자와는 달리 저장된 정보를 주기적으로 리프레시(refresh)할 필요가 없으며, 그 설계가 용이하다.

이하에서는 종래의 에스램 소자의 제조방법을 간략하게 설명하도록 한다.

먼저, 소자분리막이 구비된 반도체 기판 상에 공지의 공정에 따라 폴리실리콘 게이트를 형성한 후, 산화 공정 및 LDD 이온주입 공정을 차례로 수행한다. 그런다음, 기판의 전 영역 상에 스페이서 산화막을 200Å 정도의 두께로 증착한 후, LPCVD 방식에 따라 스페이서 질화막을 600~ 700Å 두께로 증착한다.

이어서, 상기 질화막과 산화막을 스페이서 식각하여 게이트의 측벽에 스페이서를 형성한다. 이때, 상기 스페이서 식각은 잔류 산화막의 두께(Rox)가 100± 50Å 정도가 되도록 조절한다. 그런다음, 게이트 양측의 기판 표면에 소오스/드레인 이온주입을 행한 후, 이온주입된 불순물이 활성화(activation)되도록 상기 기판 결과물에 대해 급속열공정(Rapid Thermal Process : 이하, RTP)을 수행한다.

그 다음, 후속 금속배선 공정에서 식각 정지막으로 이용될 BLC(Bit-Line Contact) 질화막을 대략 300Å 의 두께로 증착한다.

이후, 콘택 식각을 포함한 일련의 후속 에스램 공정을 진행한다. 상기 콘택 식각은 잔류 산화막의 두께(Rox)가 50Å 정도가 되도록 조절함이 바람직하다.

발명이 이루고자 하는 기술적 과제

그러나, 전술한 바와 같은 종래의 에스램 소자의 제조방법은 다음과 같은 문제점이 있다.

먼저, 소오스/드레인 이온주입 후에는 도펀트(dopant)의 활성화를 위해 RTP를 수행하는 것이 일반적인데, 이 경우 이온주입에 의해 비정질화된 기판 부분이 재결정화(Recrystalline)되면서 게이트 에지에서 디스로케이션(disolocation)이 발생하게 되며, 이로 인해, 소자 특성 저하가 유발된다.

그 다음, 잔류 산화막은 스페이서 식각시에 남겨둔 산화막으로서 그 두께 조절이 매우 중요한데, 상기 스페이서 식각 공정에서부터 잔류 두께 조절이 쉽지 않기 때문에 후속의 콘택 식각에서도 산화막 잔류 두께 조절이 쉽지 않은 실정

이다. 이에 따라, 잔류 산화막 두께(Rox)가 얇은 부분에서는 BLC 질화막의 스트레스가 기판에 그대로 전달됨으로써 소자 특성 열화가 유발된다.

따라서, 본 발명은 상기와 같은 문제점을 해결하기 위해 안출된 것으로서, RTP시의 디스로케이션 발생을 방지하면서 BLC 질화막의 적용에 따른 스트레스를 완화시킬 수 있는 에스램 소자의 제조방법을 제공함에 그 목적이 있다.

발명의 구성 및 작용

상기와 같은 목적을 달성하기 위하여, 본 발명은, 반도체 기판 상에 게이트를 형성하는 단계; 상기 게이트를 포함한 기판 전 영역 상에 산화막과 질화막을 차례로 형성하는 단계; 상기 산화막의 소정 두께가 잔류되도록 상기 질화막과 산화막을 스페이서 식각하여 상기 게이트의 양측벽에 스페이서를 형성하는 단계; 상기 잔 류된 산화막을 버퍼막으로 이용하여 스페이서를 포함한 게이트 양측의 기판 내에 소오스/드레인 이온주입을 수행하는 단계; 상기 기판 표면에 잔류된 산화막을 제거하는 단계; 상기 기판 결과물 상에 버퍼용 산화막을 형성하는 단계; 상기 소오스/드레인 이온주입된 도펀트가 활성화되도록 950℃에서 20초간 급속열공정을 수행하는 단계; 및 상기 버퍼용 산화막 상에 BLC 질화막을 증착하는 단계를 포함하는 에스램 소자의 제조방법을 제공한다.

여기서, 상기 버퍼용 산화막은 680~ 830℃의 온도범위에서 80~ 120Å 의 두께로 형성하되, CVD 방식에 따라 0.25~ 0.5Torr의 압력 및 810~ 830℃의 온도에서 SiH2Cl2 및 N20 가스를 이용하여 증착하거나, 0.25~ 0.5Torr의 압력 및 770~ 790℃의 온도에서 SiH4 및 N20 가스를 이용하여 증착하거나, 0.25~ 0.5Torr의 압력 및 680~ 710℃의 온도에서 Si(OC2H5)4 및 O2 가스를 이용하여 증착하여 형성한다.

또한, 상기 버퍼용 산화막은 680~ 830℃의 온도범위에서 80~ 120Å 의 두께로 형성하되, O2 가스를 이용하여 건식 산화 방식에 따라 성장시키거나, O2 및 H2 가스를 이용하여 습식 산화 방식에 따라 성장시켜 형성한다.

게다가, 상기 버퍼용 산화막을 증착하는 단계 후, 그리고, 급속열공정을 수행하는 단계 전, 퍼니스 내에서 인-시튜로 N2 가스를 이용하여 840~ 860℃에서 10~ 20분 동안 어닐링을 수행한다.

본 발명에 따르면, 버퍼용 산화막의 형성시에 650℃ 이상의 열을 가해줌으로써 후속 RTP 공정시에 디스로케이션의 발생을 억제시킬 수 있으며, 또한, 버퍼용 산화막의 형성을 통해 BLC 질화막의 적용에 따른 스트레스를 완화시킬 수 있다.

(실시예)

이하, 첨부된 도면을 참조하여 본 발명의 실시예를 보다 상세하게 설명하도록 한다.

도 1a 내지 도 1d는 본 발명의 실시예에 따른 에스램 소자의 제조방법을 설명하기 위한 공정별 단면도이다.

도 1a를 참조하면, 소자분리막(도시안됨)을 구비한 반도체 기판(1) 상에 게이트산화막(2)과 폴리실리콘막(3) 및 캡핑 질화막(4)을 차례로 형성한 후, 상기 막들(4, 3, 2)을 패터닝하여 게이트(5)를 형성한다. 그런다음, 산화 공정을 행하여 게이트(5) 및 기판(1) 표면 상에 박막의 산화막(6)을 형성한다.

이어서, 상기 기판 결과물 상에 스페이서 산화막(7)과 스페이서 질화막(8)을 차례로 형성한 후, 상기 막들(8, 7)을 스페이서 식각하여 박막의 산화막(6) 포함한 게이트(5)의 양측벽에 스페이서(9)를 형성한다. 이때, 상기 스페이서 식각은 스페이서(9)를 포함한 게이트(5)의 양측에 스페이서 산화막(7)이 소정 두께로 잔류되도록 수행한다.

도 1b를 참조하면, 기판 표면에 잔류된 스페이서 산화막을 버퍼막으로 이용해서 상기 스페이서(9)를 포함한 게이트(5) 양측의 기판 표면 내에 소오스/드레인 이온주입을 수행한다. 그런다음, 통상의 산화막 에천트(oxide etchant), 예컨데, HF 또는 BOE 용액을 이용한 습식 식각을 통해 기판 표면 상의 잔류 산화막을 제거한다.

도 1c를 참조하면, 상기 단계까지의 기판 결과물 상에 버퍼용 산화막(10)을 형성한다. 상기 버퍼용 산화막(10)은 680~ 830℃의 온도 범위에서 80~ 120Å 의 두께로 형성하며, CVD 방식 또는 산화 방식에 따라 형성한다.

자세하게, 상기 버퍼용 산화막(10)은 CVD 방식에 따라 0.25~ 0.5Torr의 압력 및 810~ 830℃의 온도에서 SiH2Cl2 및 N20 가스를 이용하여 DCS HTO로 증착해서 형성하거나, 0.25~ 0.5Torr의 압력 및 770~ 790℃의 온도에서 SiH4 및 N20 가스를 이용하여 HTO로 증착해서 형성하거나, 또는, 0.25~ 0.5Torr의 압력 및 680~ 710℃의 온도에서 TEOS(Tetra-Ethyl-Ortho-Silicate : Si(OC2H5)4) 및 O2 가스를 이용하여 증착해서 형성한다.

또한, 상기 버퍼용 산화막(10)은 O2 가스를 이용하여 건식 산화 방식에 따라 성장시켜 형성하거나, 또는, O2 및 H2 가스를 이용하여 습식 산화 방식에 따라 성장시켜 형성한다.

계속해서, CVD 방식 또는 산화 방식에 따라 버퍼용 산화막(10)이 형성된 상기 기판 결과물에 대해 퍼니스(furnace) 내에서 인-시튜(in-situ)로 N2 분위기 및 840~860℃, 바람직하게, 850℃에서 10~20분, 바람직하게, 20분간 어닐링을 수행한다.

그 다음, 이전 공정 단계에서 소오스/드레인 이온주입된 도펀트가 충분히 활성화될 수 있도록 기판 결과물에 대해 종래와 마찬가지로 950℃에서 20초간 RTP를 수행한다.

도 1d를 참조하면, 버퍼용 산화막(10) 상에 CVD 방식에 따라 710℃의 온도에서 300Å 의 두께로 BLC 질화막(11)을 증착한다.

이후, 도시하지는 않았으나, 콘택 식각을 포함한 일련의 후속 에스램 공정을 진행하여 본 발명에 따른 에스램 소자의 제조를 완성한다.

전술한 바와 같은 본 발명의 방법에 따르면, 다음과 같이 디스로케이션 및 스트레스로 인한 소자 특성 열화를 방지할 수 있다.

일반적으로 소오스/드레인 이온주입후 재결정화에 따른 디스로케이션을 유발하는 스트레스는 650℃ 이상의 열이 가해지는 경우에 현저하게 감소된다.

도 2는 소오스/드레인 이온주입 후의 어닐링 온도에 의존하는 디스로케이션 발생에 대한 임계 스트레스를 도시한 그래프로서, 디스로케이션 발생에 대한 임계 스트레스는 650℃ 이하의 어닐링 온도에서는 큰 변화가 없지만, 650℃ 이상에서는 임계 스트레스가 현저히 감소함을 볼 수 있다.

또한, 도 3은 N+ 드레인에서 P+ 기판으로의 누설 전류 특성을 도시한 그래프로서, 도펀트의 활성화 후에 N+ 드레인에서 P+ 기판으로의 누설 특성은 950℃에서의 어닐링이 1회 수행된 경우 보다는 850℃의 어닐링과 950℃의 어닐링의 2단계 어닐링이 수행된 경우가 향상됨을 볼 수 있다.

따라서, 본 발명의 방법은 버퍼용 산화막(10)의 형성 후, 인-시튜로 850℃에서의 어닐링을 행한 후, 후속에서 950℃에서의 RTP를 수행하기 때문에 전술한 디스로케이션 발생의 억제를 통한 임계 스트레스의 감소와 더불어 누설 특성도 향상시키게 된다.

한편, BLC 질화막을 적용함에 있어서는 스페이서 산화막의 잔류 두께(Rox)를 제어함이 매우 중요한데, 종래 기술에서는 실질적으로 그 제어에 어려움이 있는 바, 상기 BLC 질화막의 적용에 따라 스트레스로 인한 소자 특성 열화가 유발된다.

그러나, 본 발명의 방법은 잔류된 스페이서 산화막을 제거한 후에 새롭게 버퍼용 산화막을 형성해주며, 이때, 그 두께를 원하는 정도, 즉, BLC 질화막의 스트레스를 충분히 완화시킬 수 있을 정도의 두께로 다시 형성해 줌으로써, 상기 BLC 질화막의 적용에 따른 스트레스에 의한 소자 특성 열화를 방지할 수 있다.

결국, 본 발명의 방법은 650℃ 이상 온도에서의 버퍼용 산화막의 추가 형성 및 그 형성후의 인-시튜 어닐링을 추가 진행해주는 것으로부터 디스로케이션 및 스트레스로 인한 소자 특성 열화를 효과적으로 방지할 수 있다.

발명의 효과

이상에서와 같이, 본 발명은 소오스/드레인 이온주입 후, 그리고, BLC 질화막의 증착 전에 버퍼용 산화막을 형성해주며, 상기 버퍼용 산화막을 형성하는 과정에서 850℃에서의 어닐링을 추가 수행하고, 이어서, 도펀트 활성화를 위해 950℃에서의 RTP를 행함으로써 디스로케이션 발생을 효과적을 억제할 수 있으며, 또한, 상기 버퍼용 산화막의 형성을 통해서 BLC 질화막의 적용에 따른 스트레스를 완화시킬 수 있는 바, 결국, 소자 특성을 향상시킬 수 있다.

기타, 본 발명은 그 요지가 일탈하지 않는 범위에서 다양하게 변경하여 실시할 수 있다.

(57) 청구의 범위

청구항 1.
반도체 기판 상에 게이트를 형성하는 단계;

상기 게이트를 포함한 기판 전 영역 상에 산화막과 질화막을 차례로 형성하는 단계;

상기 산화막의 소정 두께가 잔류되도록 상기 질화막과 산화막을 스페이서 식각하여 상기 게이트의 양측벽에 스페이서를 형성하는 단계;

상기 잔류된 산화막을 버퍼막으로 이용하여 스페이서를 포함한 게이트 양측의 기판 내에 소오스/드레인 이온주입을 수행하는 단계;

상기 기판 표면에 잔류된 산화막을 제거하는 단계;

상기 기판 결과물 상에 버퍼용 산화막을 형성하는 단계;

상기 소오스/드레인 이온주입된 도펀트가 활성화되도록 950℃에서 20초간 급속열공정을 수행하는 단계; 및

상기 버퍼용 산화막 상에 BLC 질화막을 증착하는 단계를 포함하는 것을 특징으로 하는 에스램 소자의 제조방법.

청구항 2.
제 1 항에 있어서, 상기 버퍼용 산화막은 680~ 830℃의 온도범위에서 80~ 120Å 의 두께로 형성하는 것을 특징으로 하는 에스램 소자의 제조방법.

청구항 3.
제 1 항 또는 제 2 항에 있어서, 상기 버퍼용 산화막은 CVD 방식에 따라 0.25~ 0.5Torr의 압력 및 810~ 830℃의 온도에서 SiH2Cl2 및 N2O 가스를 이용하여 증착하는 것을 특징으로 하는 에스램 소자의 제조방법.

청구항 4.
제 1 항 또는 제 2 항에 있어서, 상기 버퍼용 산화막은 CVD 방식에 따라 0.25~ 0.5Torr의 압력 및 770~ 790℃의 온도에서 SiH4 및 N2O 가스를 이용하여 증착하는 것을 특징으로 하는 에스램 소자의 제조방법.

청구항 5.
제 1 항 또는 제 2 항에 있어서, 상기 버퍼용 산화막은 CVD 방식에 따라 0.25~ 0.5Torr의 압력 및 680~ 710℃의 온도에서 Si(OC2H5)4 및 O2 가스를 이용하여 증착하는 것을 특징으로 하는 에스램 소자의 제조방법.

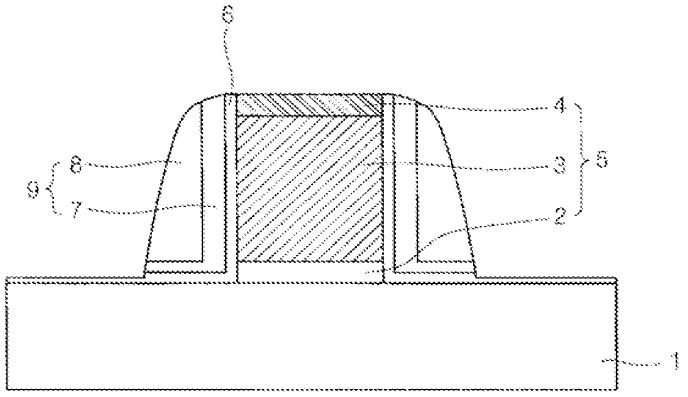
청구항 6.
제 1 항 또는 제 2 항에 있어서, 상기 버퍼용 산화막은 O2 가스를 이용하여 건식 산화 방식에 따라 성장시키는 것을 특징으로 하는 에스램 소자의 제조방법.

청구항 7.
제 1 항 또는 제 2 항에 있어서, 상기 버퍼용 산화막은 O2 및 H2 가스를 이용하여 습식 산화 방식에 따라 성장시키는 것을 특징으로 하는 에스램 소자의 제조방법.

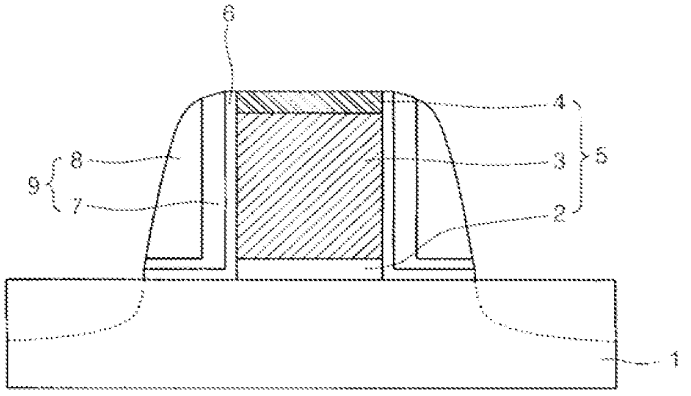
청구항 8.
제 1 항에 있어서, 상기 버퍼용 산화막을 증착하는 단계 후, 그리고, 급속열공정을 수행하는 단계 전, 퍼니스 내에서 인-시튜(in-situ)로 N2 가스를 이용하여 840~ 860℃에서 10~ 20분 동안 어닐링을 수행하는 것을 특징으로 하는 에스램 소자의 제조방법.

도면

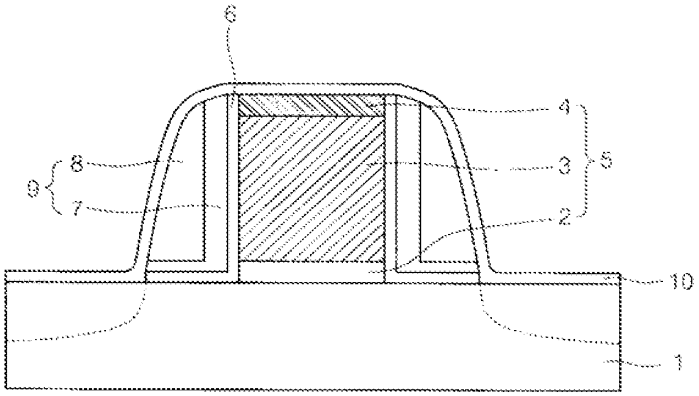
도면1a



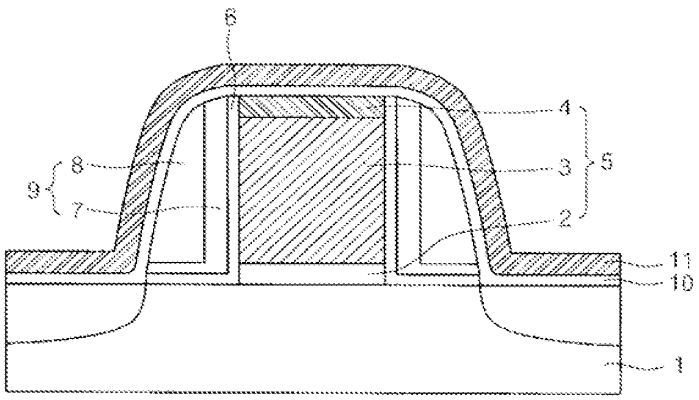
도면1b



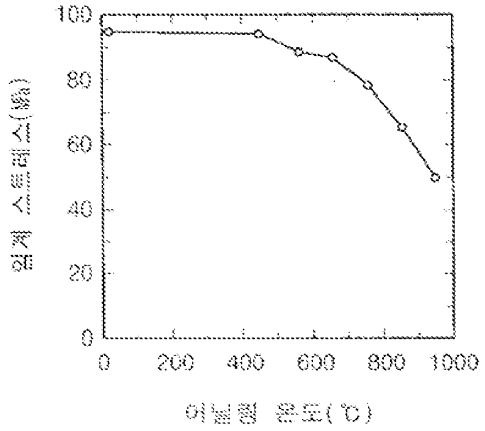
도면1c



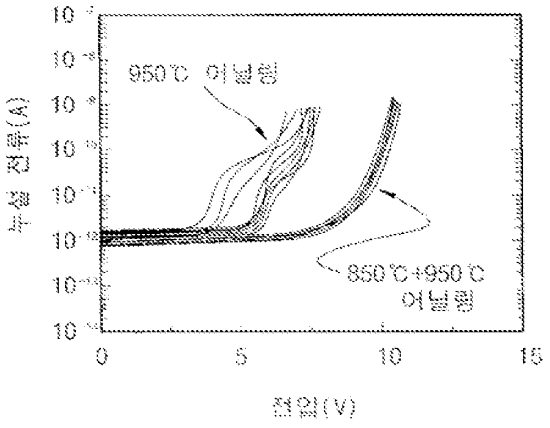
도면1d


6
4
3
2
5
8
9
7
11
10
1

도면2


100
80
60
40
20
0
0
200
400
600
800
1000
원계 스트레스(%)
어닐링 온도(℃)

도면3


950℃ 어닐링
850℃+950℃
어닐링
누설 전류(A)
0
5
10
15
전압(V)

KOREAN PATENT ABSTRACTS XML 1(1-1)

Print Save Error Report

(19) KOREAN INTELLECTUAL PROPERTY OFFICE

KOREAN PATENT ABSTRACTS

(11) Publication number: 1020080021918 A
(43) Publication date: 10.03.2008

(21) Application number: 1020060085113
(22) Application date: 05.09.2006

(51) Int. Cl: H01L 21/336
H01L 21/24

(71) Applicant: • DONGBU ELECTRONICS CO., LTD.

(72) Inventor: • SHIN, HYUN SOO

(54) MOS TRANSISTOR WITH A FULL SILICIDE GATE STRUCTURE HAVING AN OXIDE LAYER AND A THIN FILM WHICH IS SUBJECTED TO PLASMA NITRIDING, AND A MANUFACTURING METHOD THEREOF

(57) Abstract:

PURPOSE: A MOS transistor with a full silicide gate structure and a manufacturing method thereof are provided to reduce electrical leakage of a silicide gate electrode by forming a spacer on a sidewall of the gate electrode.

CONSTITUTION: A gate insulating layer(106) is deposited on an upper portion of a semiconductor substrate(100), and a gate electrode made of silicide is formed on the gate insulating layer. A spacer(114a) consisting of a silicon oxide layer and a thin film which is subjected to plasma nitriding is formed on a sidewall of the gate electrode, and a source/drain region(116) is formed on the substrate at an edge of the gate electrode. A silicide layer

(19) 대한민국특허청(KR)
(12) 공개특허공보(A)

(11) 공개번호 10-2008-0021918
(43) 공개일자 2008년03월10일

(51) Int. Cl.
H01L 21/336 (2006.01) *H01L 21/24* (2006.01)
(21) 출원번호 10-2006-0085113
(22) 출원일자 2006년09월05일
심사청구일자 2006년09월05일

(71) 출원인
동부일렉트로닉스 주식회사
서울 강남구 대치동 891-10
(72) 발명자
신현수
충북 음성군 금왕읍 무극리 503 우수장미아파트 101-가-207
(74) 대리인
김원준, 장성구

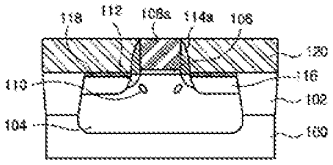
전체 청구항 수 : 총 6 항

(54) 완전 실리사이드 게이트 구조를 갖는 모스 트랜지스터 및 그 제조 방법

(57) 요 약

본 발명은 완전 실리사이드 게이트 구조를 갖는 모스 트랜지스터 및 그 제조 방법에 관한 것으로, 특히 본 발명의 제조 방법은, 반도체 기판 상부에 게이트 절연막과 폴리실리콘으로 이루어진 게이트 전극을 형성하고, 게이트 전극 측벽에 실리콘 산화막과 플라즈마 질화처리된 박막을 갖는 스페이서를 형성하고, 게이트 전극 에지의 외곽 반도체 기판에 소오스/드레인 영역을 형성하고, 게이트 전극 및 소오스/드레인 영역 상부에 실리사이드막을 각각 형성하고, 결과물 전면에 절연막을 형성하고, 절연막을 연마하면서 게이트 전극 상부면의 실리사이드막을 제거한 후에, 절연막 상부면에 실리사이드용 금속을 형성하고 열처리 공정을 수행하여 게이트 전극을 실리사이드화한 후에, 실리사이드용 금속을 제거한다. 그러므로, 본 발명은 게이트 전극 측벽에 실리콘 산화막 및 플라즈마 질화처리된 박막으로 이루어진 스페이서를 형성함으로써 실리사이드 게이트 전극의 전기적 누설을 줄일 수 있다.

대표도 - 도3j



특허청구의 범위

청구항 1

실리사이드 게이트 전극을 갖는 모스 트랜지스터에 있어서,

반도체 기판 상부에 적층된 게이트 절연막과,

상기 게이트 절연막 상부에 형성된 실리사이드로 이루어진 게이트 전극과,

상기 게이트 전극 측벽에 실리콘 산화막과 플라즈마 질화처리된 박막으로 형성된 스페이서와,

상기 게이트 전극 양지의 외곽 반도체 기판에 형성된 소오스/드레인 영역과,

상기 소오스/드레인 영역 상부에 형성된 실리사이드막

을 포함하는 완전 실리사이드 게이트 구조를 갖는 모스 트랜지스터.

청구항 2

제 1항에 있어서,

상기 플라즈마 질화처리된 박막을 500Å~2000Å 두께로 형성하는

완전 실리사이드 게이트 구조를 갖는 모스 트랜지스터.

청구항 3

실리사이드 게이트 전극을 갖는 모스 트랜지스터를 제조하는 방법에 있어서,

반도체 기판 상부에 게이트 절연막과 폴리실리콘으로 이루어진 게이트 전극을 형성하는 단계와,

상기 게이트 전극 측벽에 실리콘 산화막과 플라즈마 질화처리된 박막을 갖는 스페이서를 형성하는 단계와,

상기 게이트 전극 양지의 외곽 반도체 기판에 소오스/드레인 영역을 형성하는 단계와,

상기 게이트 전극 및 상기 소오스/드레인 영역 상부에 실리사이드막을 각각 형성하는 단계와,

상기 결과물 전면에 절연막을 형성하고, 상기 절연막을 연마하면서 상기 게이트 전극 상부면의 실리사이드막을 제거하는 단계와,

상기 절연막 상부면에 실리사이드용 금속을 형성하고 열처리 공정을 수행하여 상기 게이트 전극을 실리사이드화 한 후에, 상기 실리사이드용 금속을 제거하는 단계

를 포함하는 완전 실리사이드 게이트 구조를 갖는 모스 트랜지스터 제조 방법.

청구항 4

제 3항에 있어서,

상기 플라즈마 질화처리된 박막을 500Å~2000Å 두께로 형성하는

완전 실리사이드 게이트 구조를 갖는 모스 트랜지스터 제조 방법.

청구항 5

제 3항에 있어서,

상기 스페이서의 실리콘 산화막을 화학기상증착 공정으로 증착하되, 그 공정 온도를 800℃~1050℃로 하는

완전 실리사이드 게이트 구조를 갖는 모스 트랜지스터 제조 방법.

청구항 6

제 3항에 있어서,

상기 스페이서의 플라즈마 질화 처리 공정은, 질소 가스를 15~30% 농도 조건으로 하고, 공정 온도를 700℃~

850℃로 하고, RF 전원을 100W~1500W, 챔버 압력을 1mTorr~1000mTorr의 조건으로 수행하는

완전 실리사이드 게이트 구조를 갖는 모스 트랜지스터 제조 방법.

청 구 시

발명의 상세한 설명

발명의 목적

발명이 속하는 기술 및 그 분야의 종래기술

<12> 본 발명은 모스 트랜지스터(MOS transistor) 및 그 제조 방법에 관한 것으로서, 특히 게이트 전극의 누설(leakage)을 줄일 수 있는 완전 실리사이드 게이트(fully silicide gate) 구조를 갖는 모스 트랜지스터 및 그 제조 방법에 관한 것이다.

<13> 모스 트랜지스터의 집적도가 증가함에 따라, 모스 트랜지스터의 크기 또한 점점 스케일 다운되고 있다. 모스 트랜지스터가 스케일 다운됨에 따라, 단축된 채널 길이에 의한 쇼트 채널 효과(short channel effect)를 방지하면서 트랜지스터의 전류 구동 능력을 향상시키기 위해 게이트 절연막의 두께를 감소시키고 있다. 게이트 절연막의 두께 감소는 모스 트랜지스터의 커패시턴스를 증가시켜 전류 구동능력을 향상을 도모할 수 있다.

<14> 하지만, 게이트 절연막의 두께가 감소함에 따라, 폴리실리콘막을 게이트 전극으로 사용하는 모스 트랜지스터에서 폴리실리콘 공핍(poly depletion)이 발생하게 되고, 이로 인해 게이트 절연막의 전기적인 등가 두께(electrical equivalent thickness)가 증가되어 구동 전류(drive current)를 감소시킨다.

<15> 이러한 게이트 전극의 폴리실리콘 공핍을 해결하기 위한 방안으로서, 금속 게이트를 사용하고 있으나, 금속 게이트는 트랜지스터의 문턱 전압(threshold voltage)을 조절하기 어렵다는 단점이 있다.

<16> 이를 위하여, 폴리실리콘 게이트 전극을 형성하고 나서, 이후 실리사이드 공정으로 폴리실리콘 게이트를 실리사이드화하는 완전 실리사이드 게이트 전극 제조 공정이 사용되고 있다.

<17> 도 1a 내지 도 1j는 종래 기술에 의한 완전 실리사이드 게이트 구조를 갖는 모스 트랜지스터의 제조 공정을 순차적으로 나타낸 공정 순서도이다.

<18> 이들 도면을 참조하면, 종래 기술에 의한 완전 실리사이드 게이트 구조를 갖는 모스 트랜지스터 제조 공정은 다음과 같이 진행된다.

<19> 우선, 도 1a에 도시된 바와 같이, 반도체 기판(10)으로서 실리콘 기판에 활성 영역과 비활성 영역을 정의하는 소자 분리막(12)을 형성한다. 예를 들어, 반도체 기판(10)을 소정 깊이로 식각하여 트렌치를 형성하고, 트렌치를 채우는 절연 물질, HDP(High Density Plasma) 산화막을 증착하고 화학적기계적연마(CMP : Chemical Mechanical Polishing) 공정으로 절연 물질을 연마하여 소자 분리막(12)을 형성한다.

<20> 도 1b에 도시된 바와 같이, 소자 분리막(12)이 형성된 반도체 기판(10)에 n형 도펀트 또는 p형 도펀트를 이온 주입하여 웰(well)(14)을 형성한다.

<21> 도 1c에 도시된 바와 같이, 소자 분리막(12) 및 웰(14)이 형성된 반도체 기판(10) 전면에 절연막, 예를 들어 실리콘 산화막(SiO_2)을 약 100Å 정도 증착하고, 그 위에 게이트 도전막, 예를 들어 불순물이 도핑된 도프트 폴리실리콘을 약 3000Å 정도 증착한다.

<22> 사진 공정을 진행하여 게이트 도전막에 게이트 영역을 정의하는 포토레지스트 패턴(미도시됨)을 형성하고, 이 패턴에 의해 드러난 게이트 도전막을 건식 식각, 예를 들어 반응성 이온 식각(RIE : Reactive Ion Etching)하여 게이트 전극(18)을 형성하고, 그 아래의 절연층 또한 건식 식각하여 게이트 절연막(16)을 형성한다. 그리고 애싱(ashing) 공정으로 포토레지스트 패턴을 제거한다.

<23> 그리고, 이온 주입시 도펀트 이온에 의한 기판 표면 및 게이트 접합 누설(gate junction leakage)을 억제하기 위하여 기판 전면에 스크린 절연막(미도시됨)을 형성한다. 예를 들어, 실리콘 산화막(SiO_2)을 10Å~40Å 두께로 형성한다.

<24> 도 1d에 도시된 바와 같이, 게이트 전극(18)을 이온 주입 마스크로 이용하고, 도펀트 이온 주입 공정을 실시한다.

예를 들어, N형 모스 트랜지스터의 경우 p형 도펀트 불순물로서, 붕소(B)를 경사진 각도(예를 들어, 25° ~30°)와 20keV~30keV 에너지 세기, $1.3E13/cm^2$~$2.0E13/cm^2$의 농도 조건으로 이온 주입하여 게이트 전극(18) 에지 기판 아래에 포켓 영역(20)을 형성한다.

<25> 계속해서, 게이트 전극(18)을 이온 주입 마스크로 이용하여 저농도 이온 주입 공정을 실시한다. 예를 들어, n형 도펀트 불순물인 인(P)을 기 설정된 저농도로 이온 주입하여 게이트 전극(18) 에지와 소자 분리막(12) 사이의 기판 내에 LDD 영역(22)을 형성한다.

<26> 그 다음 습식 식각 공정을 진행하여 스크린 절연막막을 제거한다.

<27> 이어서 도 1e에 도시된 바와 같이, 반도체 기판(10) 전면에 절연 물질, 예를 들어 실리콘 질화막(SiN) 또는 실리콘 산화질화막(SiON)을 증착하고 이를 전식 식각, 예를 들어 반응성 이온 식각(RIE)하여 게이트 전극(18) 측벽에 스페이서(24)를 형성한다.

<28> 그리고, 도 1f에 도시된 바와 같이, 스페이서(24) 및 게이트 전극(18)을 이온 주입 마스크로 이용하여 고농도 이온주입 공정, 예를 들어, n형 불순물 도펀트를 고농도로 이온 주입하여 스페이서(24) 에지와 소자 분리막(12) 사이의 기판 내에 소오스/드레인 영역(26)을 형성한다.

<29> 그 다음, 도 1g에 도시된 바와 같이, 반도체 기판(10) 전면에 실리사이드용 금속 물질, 예를 들어 티타늄(Ti)을 증착하고 이를 열처리 공정을 실시하여 게이트 전극(18) 및 소오스/드레인 영역(26) 상부면에 각각 실리사이드막(28)을 형성한 후에, 실리사이드화되지 않은 금속 물질을 제거한다. 여기서, 실리사이드용 금속 물질은 예를 들어, 코발트(Co), 티타늄(Ti), 니켈(Ni), 텅스텐(W), Pt(백금), Hf(하프늄), Pd(팔라듐) 등의 희토류 금속 또는 이들의 합금 중에서 어느 하나의 금속으로 이루어진다. 이때, 열처리 공정은 1차로 400℃~600℃에서 급속 열처리(RTP : Rapid Thermal Process) 공정을 진행하고, 황산 등의 세정액으로 세정한 후에, 2차로 600℃~900℃에서 급속 열처리(RTP) 공정을 진행한다.

<30> 이로 인해 게이트 전극(18) 및 소오스/드레인 영역(26) 상부면에 텅스텐 실리사이드(WSi_2), 티타늄 실리사이드($TiSi_2$), 코발트 실리사이드(CoSi) 등과 같은 실리사이드막(28)이 형성된다.

<31> 계속해서, 도 1h에 도시된 바와 같이, 상기 결과물 전면에 절연막(30)으로서, 실리콘 산화막(SiO_2)을 두껍게 증착하고, 화학적기계적연마(CMP) 공정으로 절연막(30)을 연마하되, 게이트 전극(18) 표면이 드러나도록 식각한다. 즉, 게이트 전극(18) 상부의 실리사이드막을 제거하면서 상기 절연막(30)을 평탄화시킨다.

<32> 그리고 나서, 도 1i 및 도 1j에 도시된 바와 같이, 평탄화된 절연막(30) 상부에 실리사이드용 금속막(32), 예를 들어 티타늄(Ti)을 증착하고 이를 열처리 공정을 실시하여 게이트 전극을 실리사이드막(18a)으로 변화시키고, 이후 실리사이드화되지 않은 금속막을 제거한다. 여기서, 실리사이드용 금속막(32)은 예를 들어, 코발트(Co), 티타늄(Ti), 니켈(Ni), 텅스텐(W), Pt(백금), Hf(하프늄), Pd(팔라듐) 등의 희토류 금속 또는 이들의 합금 중에서 어느 하나의 금속으로 이루어진다.

<33> 그리고, 상기 열처리 공정은 1차로 400℃~600℃에서 급속 열처리(RTP) 공정을 진행하고, 황산 등의 세정액으로 세정한 후에, 2차로 600℃~900℃에서 급속 열처리(RTP) 공정을 진행한다.

<34> 이로 인해, 도프트 폴리실리콘으로 이루어진 게이트 전극은 실리사이드용 금속막(32)과의 반응에 의해 실리사이드 게이트 전극(18a)이 되고, 절연막(30)에 의해 소오스/드레인 영역(26), 스페이서(24) 등은 블록킹된다. 이때, 실리사이드 게이트 전극(18a)은 예를 들어, 텅스텐 실리사이드(WSi_2), 티타늄 실리사이드($TiSi_2$), 코발트 실리사이드(CoSi) 등으로 형성된다.

<35> 하지만, 종래 기술에 의한 완전 실리사이드 게이트 구조를 갖는 모스 트랜지스터는, 게이트 전극(18a) 및 소오스/드레인 영역(28) 상부 표면이 모두 실리사이드 막으로 이루어져 있기 때문에 게이트 전극 측벽의 스페이서(24)만으로 절연시키는데 한계가 있어 실리사이드 게이트 전극(18a) 에지와 소오스/드레인 영역(28) 사이에서 전기적인 누설이 발생하게 되는 문제점이 있다.

발명이 이루고자 하는 기술적 과제

<36> 본 발명의 목적은, 상기와 같은 종래 기술의 문제점을 해결하기 위하여, 게이트 전극 측벽에 실리콘 산화막 및 플라즈마 질화처리된 박막으로 이루어진 스페이서를 형성함으로써 실리사이드 게이트 전극의 전기적 누설을 줄

일 수 있는 완전 실리사이드 게이트 구조를 갖는 모스 트랜지스터를 제공하는데 있다.

<37> 본 발명의 다른 목적은, 게이트 전극을 형성하고 나서 실리콘 산화막을 증착하고 플라즈마 질화 처리 공정을 수행한 후에 이를 식각하여 게이트 전극 측벽에 스페이서를 형성함으로써 실리사이드 게이트 전극의 전기적 누설을 줄일 수 있는 완전 실리사이드 게이트 구조를 갖는 모스 트랜지스터 제조 방법을 제공하는데 있다.

발명의 구성 및 작용

<38> 전술한 목적을 달성하기 위하여 본 발명은, 실리사이드 게이트 전극을 갖는 모스 트랜지스터에 있어서, 반도체 기판 상부에 적층된 게이트 절연막과, 게이트 절연막 상부에 형성된 실리사이드로 이루어진 게이트 전극과, 게이트 전극 측벽에 실리콘 산화막과 플라즈마 질화처리된 박막으로 형성된 스페이서와, 게이트 전극 에지의 외곽 반도체 기판에 형성된 소오스/드레인 영역과, 소오스/드레인 영역 상부에 형성된 실리사이드막을 포함한다.

<39> 다른 목적을 달성하기 위하여 본 발명은, 실리사이드 게이트 전극을 갖는 모스 트랜지스터를 제조하는 방법에 있어서, 반도체 기판 상부에 게이트 절연막과 폴리실리콘으로 이루어진 게이트 전극을 형성하는 단계와, 게이트 전극 측벽에 실리콘 산화막과 플라즈마 질화처리된 박막을 갖는 스페이서를 형성하는 단계와, 게이트 전극 에지의 외곽 반도체 기판에 소오스/드레인 영역을 형성하는 단계와, 게이트 전극 및 소오스/드레인 영역 상부에 실리사이드막을 각각 형성하는 단계와, 결과물 전면에 절연막을 형성하고, 절연막을 연마하면서 게이트 전극 상부면의 실리사이드막을 제거하는 단계와, 절연막 상부면에 실리사이드용 금속을 형성하고 열처리 공정을 수행하여 게이트 전극을 실리사이드화한 후에, 실리사이드용 금속을 제거하는 단계를 포함한다.

<40> 이하, 본 발명의 가장 바람직한 실시 예를 첨부한 도면을 참조하여 본 발명의 기술분야에서 통상의 지식을 가진 자가 용이하게 실시할 수 있도록 더욱 상세히 설명하기로 한다.

<41> 도 2는 본 발명에 따른 완전 실리사이드 게이트 구조를 갖는 모스 트랜지스터 구조를 나타낸 수직 단면도이다.

<42> 도 2에 도시된 바와 같이, 본 발명에 따른 완전 실리사이드 게이트 구조를 갖는 모스 트랜지스터는, 반도체 기판(100)으로서, 실리콘 기판 상부에 게이트 절연막(106)이 형성되어 있고, 게이트 절연막(106) 상부에 실리사이드로 이루어진 게이트 전극(108a)이 형성되어 있다. 게이트 전극(108) 에지와 소자 분리막(102) 사이의 반도체 기판(100)내에 얇은 깊이로 불순물이 주입된 LDD 영역(112)이 형성되고, 게이트 전극(108) 측벽에 실리콘 산화막(SiO_2)과 플라즈마 질화 처리된 박막으로 이루어진 스페이서(114a)가 형성되어 있다.

<43> 그리고, 스페이서(114a) 에지와 소자 분리막(102) 사이의 반도체 기판(100)내에 소오스/드레인 영역(116)이 형성되어 있다.

<44> 또, 소오스/드레인 영역(116) 상부 표면에 실리사이드막(118)이 형성되어 있고, 실리사이드막(118) 상부에 스페이서(114a)와 분리되게 게이트 전극(108a) 높이만큼의 절연막(120)이 형성되어 있다.

<45> 그러므로, 본 발명에 따른 완전 실리사이드 게이트 구조를 갖는 모스 트랜지스터는, 실리사이드로 이루어진 게이트 전극(108a) 측벽에 실리콘 산화막 및 플라즈마 질화처리된 박막으로 이루어진 스페이서(114a)를 형성함으로써 실리사이드 게이트 전극(108a)의 전기적 누설을 줄일 수 있다.

<46> 도 3a 내지 도 3j는 본 발명에 따른 완전 실리사이드 게이트 구조를 갖는 모스 트랜지스터의 제조 공정을 순차적으로 나타낸 공정 순서도이다.

<47> 도 2a 내지 도 3j를 참조하면, 본 발명의 일 실시 예에 따른 완전 실리사이드 게이트 구조를 갖는 모스 트랜지스터의 제조 공정은 다음과 같이 진행된다.

<48> 우선, 도 3a에 도시된 바와 같이, 반도체 기판(100)으로서 실리콘 기판에 활성 영역과 비활성 영역을 정의하는 소자 분리막(102)을 형성한다. 예를 들어, 반도체 기판(100)을 소정 깊이로 식각하여 트렌치를 형성하고, 트렌치를 채우는 절연 물질, HDP 산화막을 매립하고 화학적기계적연마(CMP) 공정으로 절연 물질을 연마하여 소자 분리막(102)을 형성한다.

<49> 소자 분리막(102)이 형성된 반도체 기판(100)에 n형 도펀트 또는 p형 도펀트를 이온 주입하여 웰(104)을 형성한다.

<50> 그리고 도 3b에 도시된 바와 같이, 소자 분리막(102) 및 웰(104)이 형성된 반도체 기판(100) 전면에 절연막, 예를 들어 실리콘 산화막(SiO_2)을 약 100Å 정도 증착하고, 그 위에 게이트 도전막, 예를 들어 불순물이 도핑된

도프트 폴리실리콘을 약 3000Å 정도 증착한다.

<51> 사진 공정을 진행하여 게이트 도전막에 게이트 영역을 정의하는 포토레지스트 패턴(미도시됨)을 형성하고, 이 패턴에 의해 드러난 게이트 도전막을 건식 식각, 예를 들어 반응성 이온 식각(RIE)하여 게이트 전극(108)을 형성하고, 그 아래의 절연층만 건식 식각하여 게이트 절연막(106)을 형성한다. 그리고 애싱 공정으로 포토레지스트 패턴을 제거한다.

<52> 그 다음, 이온 주입시 도펀트 이온에 의한 기판 표면 및 게이트 전선 누설을 억제하기 위하여 기판 전면에 스크린 절연막막(미도시됨)을 형성한다. 예를 들어, 실리콘 산화막(SiO)을 10Å~40Å 두께로 형성한다.

<53> 계속해서 도 3c에 도시된 바와 같이, 게이트 전극(108)을 이온 주입 마스크로 이용하고, 포켓 이온 주입 공정을 실시한다. 예를 들어, N형 모스 트랜지스터의 경우 p형 도펀트 불순물로서, 붕소(B)를 경사진 각도(예를 들어, 25° ~30°)와 20keV~30keV 에너지 세기, 1.3E13/cm^2~2.0E13/cm^2의 농도 조건으로 이온 주입하여 게이트 전극(108) 에지 기판 아래에 포켓 영역(110)을 형성한다.

<54> 계속해서, 게이트 전극(108)을 이온 주입 마스크로 이용하여 저농도 이온 주입 공정을 실시한다. 예를 들어, n형 도펀트 불순물인 인(P)을 경사정된 저농도로 이온 주입하여 게이트 전극(108) 에지와 소자 분리막(102) 사이의 기판 내에 LDD 영역(112)을 형성한다.

<55> 그 다음, 습식 식각 공정을 진행하여 스크린 절연박막을 제거한다.

<56> 이어서, 도 3d에 도시된 바와 같이, 반도체 기판(100) 전면에 실리콘 산화막(SiO_2)(114)을 10Å~100Å 두께로 형성한다. 이때, 화학기상증착 공정으로 실리콘 산화막(114)을 증착하되, 그 공정 온도를 800℃~1050℃로 한다.

<57> 그 다음, 플라즈마 질화 처리 공정을 실시한다. 이때, 질소 가스를 18~30% 농도 조건으로 하여 질소 소오스 가스를 예컨대 NH_3 1500SCCM/N_2 1500SCCM만큼 공급하고, RF 전원을 100W~1500W, 챔버 압력을 1mTorr~1000mTorr의 조건으로 설정하며, 700℃~850℃의 공정 온도에서 30min~180min 동안 수행하여 플라즈마 질화처리된 실리콘 산화막을 500Å~2000Å의 두께로 형성한다.

<58> 계속해서 도 3e에 도시된 바와 같이, 플라즈마 질화처리된 실리콘 산화막을 건식 식각, 예를 들어 반응성 이온 식각(RIE)하여 게이트 전극(108) 측벽에 스페이서(114a)를 형성한다. 이때, 식각 공정 조건은 플라즈마 파워 300W~300W, 압력 125mTorr, 가스 HBr 30sccm/Cl_2 120sccm/O_2 10sccm, 온도 60℃, 시간 45sec로 설정한다.

<59> 그리고, 도 3f에 도시된 바와 같이, 스페이서(114a) 및 게이트 전극(108)을 이온 주입 마스크로 이용하여 고농도 이온주입 공정, 예를 들어, n형 불순물 도펀트를 고농도로 이온 주입하여 스페이서(114a) 에지와 소자 분리막(102) 사이의 기판 내에 소오스/드레인 영역(116)을 형성한다.

<60> 그 다음, 도 3g에 도시된 바와 같이, 반도체 기판(100) 전면에 실리사이드용 금속 물질, 예를 들어 티타늄(Ti)을 증착하고 이를 열처리 공정을 실시하여 게이트 전극(108) 및 소오스/드레인 영역(116) 상부면에 각각 실리사이드막(118)을 형성한 후에, 실리사이드화되지 않은 금속 물질을 제거한다. 여기서, 실리사이드용 금속 물질은 예를 들어, 코발트(Co), 티타늄(Ti), 니켈(Ni), 텅스텐(W), Pt(백금), Hf(하프늄), Pd(팔라듐) 등의 희토류 금속 또는 이들의 합금 중에서 어느 하나의 금속으로 이루어진다. 이때, 열처리 공정은 1차로 400℃~600℃에서 금속 열처리(RTP) 공정을 진행하고, 황산 등의 세정액으로 세정한 후에, 2차로 600℃~900℃에서 금속 열처리(RTP) 공정을 진행한다.

<61> 이로 인해 게이트 전극(108) 및 소오스/드레인 영역(16) 상부면에 텅스텐 실리사이드(WSi_2), 티타늄 실리사이드($TiSi_2$), 코발트 실리사이드(CoSi) 등과 같은 실리사이드막(18)이 형성된다.

<62> 계속해서, 도 3h에 도시된 바와 같이, 상기 결과물 전면에 절연막(120)으로서, 실리콘 산화막(SiO_2)을 두껍게 증착하고, 화학적기계적연마(CMP) 공정으로 절연막(120)을 연마하되, 게이트 전극(108) 표면이 드러나도록 식각한다. 즉, 게이트 전극(108) 상부의 실리사이드막을 제거하면서 상기 절연막(120)을 평탄화시킨다.

<63> 그리고 나서, 도 3i 및 도 3j에 도시된 바와 같이, 평탄화된 절연막(120) 상부에 실리사이드용 금속막(122), 예를 들어 티타늄(Ti)을 증착하고 이를 열처리 공정을 실시하여 게이트 전극을 실리사이드막(108a)으로 변화시키고, 이후 실리사이드화되지 않은 금속막을 제거한다. 여기서, 실리사이드용 금속막(122)은 예를 들어, 코발트

(Co), 티타늄(Ti), 니켈(Ni), 텅스텐(W), Pt(백금), Hf(하프늄), Pd(팔라듐) 등의 내화성 금속 또는 이들의 합금 중에서 어느 하나의 금속으로 이루어진다.

<64> 그리고, 상기 열처리 공정은 1차로 400℃~600℃에서 급속 열처리(RTP) 공정을 진행하고, 황산 등의 세정액으로 세정한 후에, 2차로 600℃~900℃에서 급속 열처리(RTP) 공정을 진행한다.

<65> 이로 인해, 도프드 폴리실리콘으로 이루어진 게이트 전극은 실리사이드용 금속막(122)과 반응하여 실리사이드 게이트 전극(108a)이 되고, 절연막(120)에 의해 소오스/드레인 영역(116), 플라즈마 질화 처리된 스페이서(114a) 등은 블록킹된다. 이때, 실리사이드 게이트 전극(108a)은 예를 들어, 텅스텐 실리사이드(WSi_2), 티타늄 실리사이드($TiSi_2$), 코발트 실리사이드($CoSi$) 등으로 형성된다.

<66> 그러므로, 본 발명에 따른 완전 실리사이드 게이트 구조를 갖는 모스 트랜지스터 제조 방법은, 실리사이드로 이루어진 게이트 전극(108a)과 소오스/드레인 영역(116) 사이에 실리콘 산화막 및 플라즈마 질화처리된 막막으로 스페이서(114a)를 형성함으로써 실리사이드 게이트 전극(108a) 에지와 소오스/드레인 영역(116) 사이에서의 전기적인 누설을 줄일 수 있다.

발명의 효과

<67> 상기한 바와 같이, 본 발명은 게이트 전극 측벽에 실리콘 산화막 및 플라즈마 질화처리된 박막으로 이루어진 스페이서를 형성함으로써 실리사이드 게이트 전극과 소오스/드레인 영역 사이의 전기적 누설을 줄일 수 있어 모스 트랜지스터의 전기적 특성을 향상시킬 수 있다.

<68> 한편, 본 발명은 상술한 실시 예에 국한되는 것이 아니라 후술되는 청구범위에 기재된 본 발명의 기술적 사상과 범주 내에서 당업자에 의해 여러 가지 변형이 가능하다.

도면의 간단한 설명

<1> 도 1a 내지 도 1j는 종래 기술에 의한 완전 실리사이드 게이트 구조를 갖는 모스 트랜지스터의 제조 공정을 순차적으로 나타낸 공정 순서도.

<2> 도 2는 본 발명에 따른 완전 실리사이드 게이트 구조를 갖는 모스 트랜지스터 구조를 나타낸 수직 단면도.

<3> 도 3a 내지 도 3j는 본 발명에 따른 완전 실리사이드 게이트 구조를 갖는 모스 트랜지스터의 제조 공정을 순차적으로 나타낸 공정 순서도.

<4> <도면의 주요부분에 대한 부호의 설명>

<5> 100 : 반도체 기판 102 : 소자 분리막

<6> 104 : 웰 106 : 게이트 절연막

<7> 108 : 게이트 전극 108a : 실리사이드 게이트 전극

<8> 110 : 포켓 영역 112 : LDD 영역

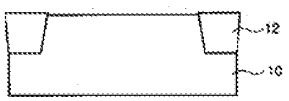
<9> 114a : 플라즈마 질화처리된 스페이서

<10> 116 : 소오스/드레인 영역 118 : 실리사이드막

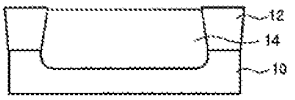
<11> 120 : 절연막 122 : 실리사이드용 금속

도면

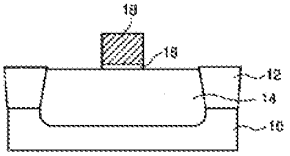
도면1a



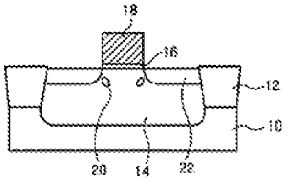
도면1b



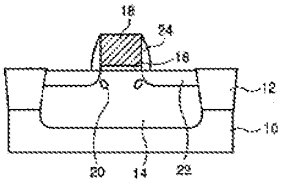
도면1c



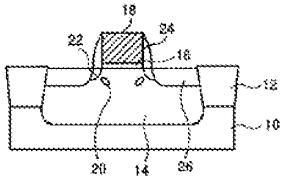
도면1d



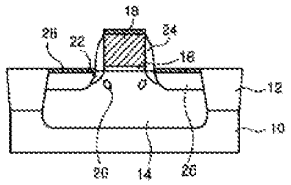
도면1e



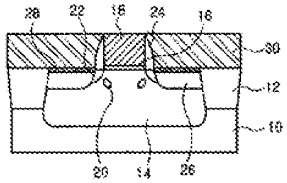
도면1f



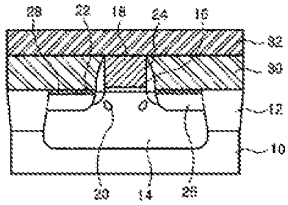
도면1g



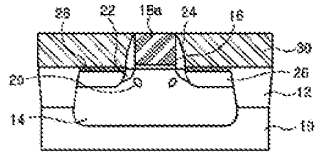
도면1h



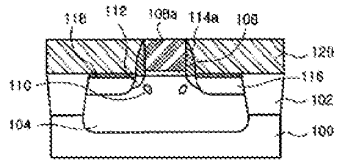
도면1i



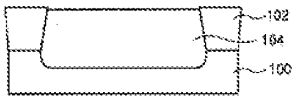
도면1j



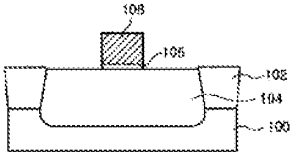
도면2



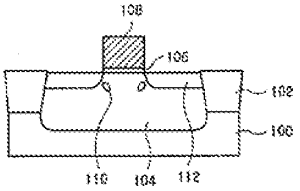
도면3a



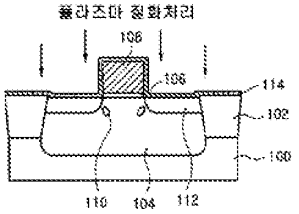
도면3b



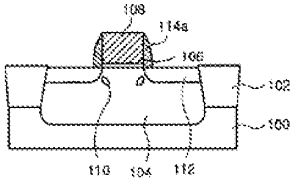
도면3c



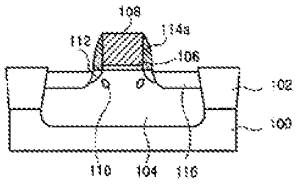
도면3d



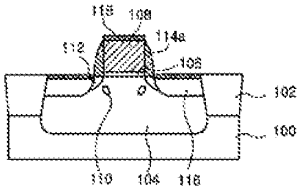
도면3e



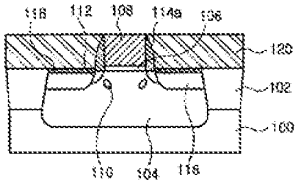
도면5f



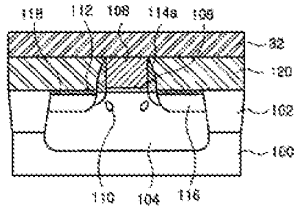
도면5g



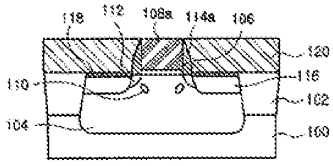
도면5h



도면5i



도면5j



(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
4 April 2013 (04.04.2013)

WIPO | PCT

(10) International Publication Number
WO 2013/048449 A1

(51) International Patent Classification:
H01L 29/78 (2006.01) *H01L 21/336* (2006.01)

(21) International Application Number:
PCT/US2011/054294

(22) International Filing Date:
30 September 2011 (30.09.2011)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant *(for all designated States except US)*: **INTEL CORPORATION** [US/US]; 2200 Mission College Boulevard, Santa Clara, California 95052 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **PRADHAN, Sameer S.** [IN/US]; 17923 NW Sylvania Lane, Portland, Oregon 97229 (US). **BERGSTROM, Daniel, B.** [US/US]; 5722 Southwood Dr., Lake Oswego, Oregon 97035 (US). **CHUN, Jin-Sung** [US/US]; 2501 NW 229th Ave, Mail-stop RA3-301, Hillsboro, Oregon 97124 (US). **CHIU, Julia** [US/US]; 2130 NW Sheffield Ave., Beaverton, Oregon 97006 (US).

(74) Agents: **WINKLE, Robert, G.** et al.; Winkle, PLLC, c/o CPA GLOBAL, P.O. Box 52050, Minneapolis, Minnesota 55402 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD,

[Continued on next page]

(54) Title: TUNGSTEN GATES FOR NON-PLANAR TRANSISTORS

(57) Abstract: The present description relates to the field of fabricating microelectronic devices having non-planar transistors. Embodiments of the present description relate to the formation of gates within non-planar NMOS transistors, wherein an NMOS work-function material, such as a composition of aluminum, titanium, and carbon, may be used in conjunction with a titanium-containing gate fill barrier to facilitate the use of a tungsten-containing conductive material in the formation of a gate electrode of the non-planar NMOS transistor gate.

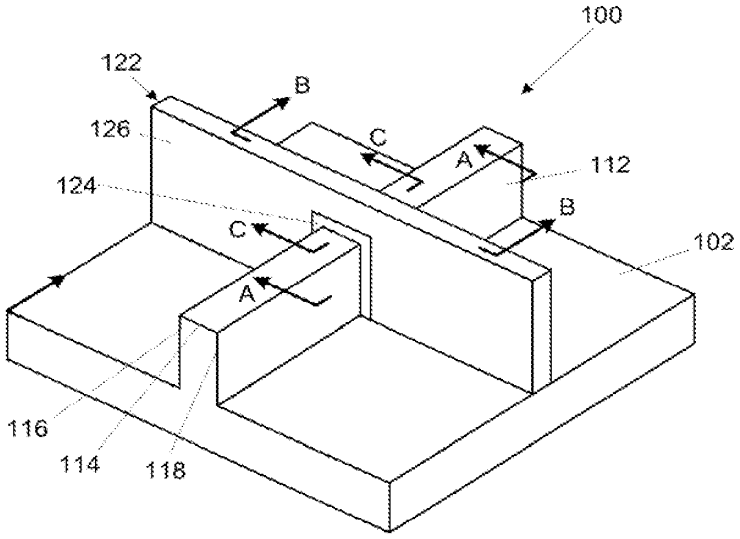


FIG. 1

WO 2013/048449 A1

SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) **Designated States** *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

---- *with international search report (Art. 21(3))*

TUNGSTEN GATES FOR NON-PLANAR TRANSISTORS

BACKGROUND

Embodiments of the present description generally relate to the field of microelectronic device fabrication and, more particularly, to the fabrication of tungsten gates within non-planar transistors.

BRIEF DESCRIPTION OF THE DRAWINGS

The subject matter of the present disclosure is particularly pointed out and distinctly claimed in the concluding portion of the specification. The foregoing and other features of the present disclosure will become more fully apparent from the following description and appended claims, taken in conjunction with the accompanying drawings. It is understood that the accompanying drawings depict only several embodiments in accordance with the present disclosure and are, therefore, not to be considered limiting of its scope. The disclosure will be described with additional specificity and detail through use of the accompanying drawings, such that the advantages of the present disclosure can be more readily ascertained, in which:

FIG. 1 is a perspective view of a non-planar transistor, according to an embodiment of the present description.

FIG. 2 illustrates a side cross-sectional view of a non-planar transistor fin formed in or on a microelectronic substrate.

FIG. 3 illustrates a side cross-sectional view of a sacrificial material deposited over the non-planar transistor fin of FIG. 2, according to an embodiment of the present description.

FIG. 4 illustrates a side cross-sectional view of a trench formed in the sacrificial material deposited to expose a portion of the non-planar transistor fin of FIG. 3, according to an embodiment of the present description.

FIG. 5 illustrates a side cross-sectional view of a sacrificial gate formed in the trench of FIG. 4, according to an embodiment of the present description.

FIG. 6 illustrates a side cross-sectional view of the sacrificial gate after the removal of the sacrificial material of FIG. 5, according to an embodiment of the present description.

FIG. 7 illustrates a side cross-sectional view of a conformal dielectric layer deposited over the sacrificial gate and microelectronic substrate of FIG. 6, according to an embodiment of the present description.

FIG. 8 illustrates a side cross-sectional view of gate spacers formed from the conformal dielectric layer of FIG. 7, according to an embodiment of the present description.

FIG. 9 illustrates a side cross-sectional view of a source region and a drain region formed in the non-planar transistor fin on either side of the gate spacers of FIG. 8, according to an embodiment of the present description.

FIG. 10 illustrates a side cross-sectional view of a first dielectric material deposited over the gate spacers, the sacrificial gate, the non-planar transistor fin, and the microelectronic substrate of FIG. 9, according to an embodiment of the present description.

FIG. 11 illustrates a side cross-sectional view of the structure of FIG. 10 after planarizing the first dielectric material to expose a top surface of the sacrificial gate, according to an embodiment of the present description.

FIG. 12 illustrates a side cross-sectional view of the structure of FIG. 11 after the removal of the sacrificial gate to form a gate trench, according to an embodiment of the present description.

FIG. 13 illustrates a side cross-sectional view of the structure of FIG. 12 after the formation of a gate dielectric adjacent the non-planar transistor fin between the gate spacers, according to an embodiment of the present description.

FIG. 14 illustrates a side cross-sectional view of the structure of FIG. 13 after the formation of an NMOS work-function material within the gate trench, according to an embodiment of the present description.

FIG. 15 illustrates a side cross-sectional view of the structure of FIG. 14 after the formation of a gate fill barrier deposited on the NMOS work-function material, according to an embodiment of the present description.

FIG. 16 illustrates a side cross-sectional view of a conductive gate material deposited in the gate trench of FIG. 15, according to an embodiment of the present description.

FIG. 17 illustrates a side cross-sectional view of the structure of FIG. 16 after the removal of excess conductive gate material to form a non-planar transistor gate, according to an embodiment of the present description.

FIG. 18 illustrates a side cross-sectional view of the structure of FIG. 17 after etching away a portion of the non-planar transistor gate to form a recessed non-planar transistor gate, according to an embodiment of the present description.

FIG. 19 illustrates a side cross-sectional view of the structure of FIG. 18 after depositing a capping dielectric material into the recess resulting from the formation of the recessed non-planar transistor gate, according to an embodiment of the present description.

FIG. 20 illustrates a side cross-sectional view of the structure of FIG. 19 after the removal of excess capping dielectric material to form a capping structure on the non-planar transistor gate, according to an embodiment of the present description.

FIG. 21 illustrates a side cross-sectional view of a second dielectric material deposited over the first dielectric material layer, the gate spacers, and the sacrificial gate top surface of FIG. 20, according to an embodiment of the present description.

FIG. 22 illustrates a side cross-sectional view of an etch mask patterned on the second dielectric material of FIG. 21, according to an embodiment of the present description.

FIG. 23 illustrates a side cross-sectional view of a contact opening formed through the first and second dielectric material layer of FIG. 22, according to an embodiment of the present description.

FIG. 24 illustrates a side cross-sectional view of the structure of FIG. 23 after the removal of the etch mask, according to an embodiment of the present description.

FIG. 25 illustrates a side cross-sectional view of a conductive contact material deposited in the contact opening of FIG. 24, according to an embodiment of the present description.

FIG. 26 illustrates a side cross-sectional view of the structure of FIG. 25 after the removal of the excess conductive contact material to form a source/drain contact, according to an embodiment of the present description.

FIG. 27 is a flow diagram of a process of forming a non-planar transistors, according to an embodiment of the present description.

FIG. 28 is a flow diagram of a process of forming a non-planar transistors, according to another embodiment of the present description.

DETAILED DESCRIPTION

In the following detailed description, reference is made to the accompanying drawings that show, by way of illustration, specific embodiments in which the claimed subject matter may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the subject matter. It is to be understood that the various embodiments, although different, are not necessarily mutually exclusive. For example, a particular feature, structure, or characteristic described herein, in connection

with one embodiment, may be implemented within other embodiments without departing from the spirit and scope of the claimed subject matter. References within this specification to "one embodiment" or "an embodiment" mean that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one implementation encompassed within the present invention. Therefore, the use of the phrase "one embodiment" or "in an embodiment" does not necessarily refer to the same embodiment. In addition, it is to be understood that the location or arrangement of individual elements within each disclosed embodiment may be modified without departing from the spirit and scope of the claimed subject matter. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the subject matter is defined only by the appended claims, appropriately interpreted, along with the full range of equivalents to which the appended claims are entitled. In the drawings, like numerals refer to the same or similar elements or functionality throughout the several views, and that elements depicted therein are not necessarily to scale with one another, rather individual elements may be enlarged or reduced in order to more easily comprehend the elements in the context of the present description.

In the fabrication of non-planar transistors, such as tri-gate transistors and FinFETs, non-planar semiconductor bodies may be used to form transistors capable of full depletion with very small gate lengths (e.g., less than about 30 nm). These semiconductor bodies are generally fin-shaped and are, thus, generally referred to as transistor "fins". For example in a tri-gate transistor, the transistor fins have a top surface and two opposing sidewalls formed on a bulk semiconductor substrate or a silicon-on-insulator substrate. A gate dielectric may be formed on the top surface and sidewalls of the semiconductor body and a gate electrode may be formed over the gate dielectric on the top surface of the semiconductor body and adjacent to the gate dielectric on the sidewalls of the semiconductor body. Thus, since the gate dielectric and the gate electrode are adjacent to three surfaces of the semiconductor body, three separate channels and gates are formed. As there are three separate channels formed, the semiconductor body can be fully depleted when the transistor is turned on. With regard to finFET transistors, the gate material and the electrode only contact the sidewalls of the semiconductor body, such that two separate channels are formed (rather than three in tri-gate transistors).

Embodiments of the present description relate to the formation of gates within non-planar transistors, wherein an NMOS work-function material, such as a composition of aluminum, titanium, and carbon, may be used in conjunction with a titanium-containing

gate fill barrier to facilitate the use of a tungsten-containing conductive material in the formation of gate electrodes of non-planar transistor gates.

FIG. 1 is a perspective view of a non-planar transistor 100, including at least one gate formed on at least one transistor fin, which are formed on a microelectronic substrate 102. In an embodiment of the present disclosure, the microelectronic substrate 102 may be a monocrystalline silicon substrate. The microelectronic substrate 102 may also be other types of substrates, such as silicon-on-insulator ("SOI"), germanium, gallium arsenide, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, gallium antimonide, and the like, any of which may be combined with silicon.

The non-planar transistor, shown as a tri-gate transistor, may include at least one non-planar transistor fin 112. The non-planar transistor fin 112 may have a top surface 114 and a pair of laterally opposite sidewalls, sidewall 116 and opposing sidewall 118, respectively.

As further shown in FIG. 1, at least one non-planar transistor gate 122 may be formed over the non-planar transistor fin 112. The non-planar transistor gate 122 may be fabricated by forming a gate dielectric layer 124 on or adjacent to the non-planar transistor fin top surface 114 and on or adjacent to the non-planar transistor fin sidewall 116 and the opposing non-planar transistor fin sidewall 118. A gate electrode 126 may be formed on or adjacent the gate dielectric layer 124. In one embodiment of the present disclosure, the non-planar transistor fin 112 may run in a direction substantially perpendicular to the non-planar transistor gate 122.

The gate dielectric layer 124 may be formed from any well-known gate dielectric material, including but not limited to silicon dioxide (SiO_2), silicon oxynitride (SiO_xN_y), silicon nitride (Si_3N_4), and high-k dielectric materials such as hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate. The gate dielectric layer 124 can be formed by well-known techniques, such as by conformally depositing a gate dielectric material and then patterning the gate dielectric material with well-known photolithography and etching techniques, as will be understood to those skilled in the art.

The gate electrode 126 may be formed by various embodiments of the present invention, as will be discussed.

A source region and a drain region (not shown in FIG. 1) may be formed in the non-planar transistor fin 112 on opposite sides of the gate electrode 126. In one embodiment, the source and drain regions may be formed by doping the non-planar transistor fins 112, as will be understood to those skilled in the art. In another embodiment, the source and drain regions may be formed by removing potions of the non-planar transistor fins 112 and replacing these portions with appropriate material(s) to form the source and drain regions, as will be understood to those skilled in the art. In still another embodiment, the source and drain regions may be formed by exitaxially growing doped or undoped strain layers on the fins 112.

FIGs. 2-26 illustrate side cross-sectional view of one embodiment of fabricating a non-planar transistor, wherein FIGs. 2-5 are views along arrows A-A and B-B of FIG. 1, FIGs. 6-15 are views along arrows A-A of FIG. 1, and FIG. 16-26 are views along arrows C-C of FIG. 1.

As shown in FIG. 2, the non-planar transistor fin 112 may be formed by etching the microelectronic substrate 102 or by forming the non-planar transistor fin 112 on the microelectronic substrate 102 by any technique known in the art. As illustrated in FIG. 3, a sacrificial material 132 may be deposited over the non-planar transistor fin 112, as shown in FIG. 3, and a trench 134 may be formed in the sacrificial material 132 to expose a potion of the non-planar transistor fin 112, as shown in FIG. 4. The sacrificial material 132 may be any appropriate material known in the art, and the trench 134 may be formed by any technique known in the art, including but not limited to lithographic masking and etching.

As shown in FIG. 5, a sacrificial gate 136 may be formed in the trench 134 (see FIG. 4). The sacrificial gate 136 may be any appropriate material, such as a polysilicon material and the like, and may be deposited in the trench 134 (see FIG. 4) by any technique known in the art, including but not limited to chemical vapor deposition ("CVD") and physical vapor deposition ("PVD").

As shown in FIG. 6, the sacrificial material 132 of FIG. 5 may be removed to expose the sacrificial gate 136 by any technique known in the art, such as selectively etching the sacrificial material 132. As shown in FIG. 7, a conformal dielectric layer 142 may be deposited over the sacrificial gate 136 and microelectronic substrate 102. The conformal dielectric layer 142 may be any appropriate material, including but not limited to silicon nitride (Si_3N_4) and silicon carbide (SiC), and may be formed by any appropriate technique including but not limited to atomic layer deposition ("ALD").

As shown in FIG. 8, the conformal dielectric layer 142 of FIG. 7 may be etched, such as by directional etch with an appropriate etchant, to form a pair of gate spacers 144 on sidewalls 146 of the sacrificial gate 136, while substantially removing the conformal dielectric material layer 142 adjacent the microelectronic substrate 102 and a top surface 148 of the sacrificial gate 136. It is understood that fin spacers (not shown) may be simultaneously formed on sidewalls 116 and 118 (see FIG. 1) of the non-planar transistor fin 112 during the formation of the gate spacers 144.

As shown in FIG. 9, a source region 150a and a drain region 150b may be formed on either side of the gate spacers 144. In one embodiment, the source region 150a and the drain region 150b may be formed in the non-planar transistor fin 112 with the implantation of N-type ion dopants. As will be understood to those skilled in that art, dopant implantation is a process of introducing impurities into semiconducting materials for the purpose changing its conductivity and electronic properties. This is generally achieved by ion implantation of either P-type ions (e.g. boron) or N-type ions (e.g. phosphorus), collectively referred to as "dopants". In another embodiment, portions of the non-planar transistor fin 112 may be removed by any technique known in the art, such as etching, and the source region 150a and the drain region 150b may be formed in place of the removed portions. In still another embodiment, the source and drain regions may be formed by exitaxially growing doped or undoped strain layers on the fins 112. The source region 150a and the drain region will hereinafter be referred to collectively as "source/drain region 150". As will be understood to those skilled in the art, transistors having P-type source and drains are referred to as "PMOS" or "p-channel metal-oxide-semiconductor" transistors, and transistors having N-type source and drains are referred to as "NMOS" or "n-channel metal-oxide-semiconductor" transistors. The present description relates to NMOS transistors. Thus, the source/drain region 150 may be N-type.

As shown in FIG. 10, a first dielectric material layer 152 may be deposited over the gate spacers 144, the sacrificial gate top surface 148, the non-planar transistor fin 112, and the microelectronic substrate 102. The first dielectric material layer 152 may be planarizing to expose the sacrificial gate top surface 148, as shown in FIG. 11. The planarization of the first dielectric material layer 152 may be achieved by any technique known in the art, including but not limited to chemical mechanical polishing (CMP).

As shown in FIG. 12, the sacrificial gate 136 of FIG. 11 may be removed to form a gate trench 154. The sacrificial gate 136 may be removed by any technique known

in the art, such as a selective etch. As shown in FIG. 13, the gate dielectric layer 124, as also illustrated in FIG. 1, may be formed to abut the non-planar transistor fin 112, as previously discussed. The materials and methods of forming the gate dielectric 124 have been previously discussed.

As shown in FIG. 14, an NMOS work-function material 156 may be conformally deposited within the gate trench 154. The NMOS work-function material 156 may comprise a composition including aluminum, titanium, and carbon. In one embodiment, the NMOS work-function material 156 may include between about 20 to 40% by weight aluminum, between about 30 to 50% by weight titanium, and between about 10 to 30% by weight carbon. In a further embodiment, the work-function material may include about 33% by weight aluminum, about 43% by weight titanium, and about 24% by weight carbon. The NMOS work-function material 156 may be conformally deposited by an ALD process to provide good coverage of the non-planar transistor fin 112 and achieve a uniform threshold voltage around the gate trench 154, as will be understood to those skilled in the art. It is further understood that the aluminum to titanium ratio may be adjusted to tune the work function of the non-planar transistor 100, whereas the carbon may be an artifact of the ALD process, rather than an added component.

As shown in FIG. 15, a gate fill barrier 158 may be conformally deposited on the NMOS work-function material 156. The gate fill barrier 158 may be a titanium-containing material, including but not limited to substantially pure titanium, titanium nitride, and the like. The gate fill barrier 158 may be formed by any known technique. In one embodiment, the gate fill barrier 158 may be titanium nitride formed by a chemical vapor deposition process comprising the decomposition of tetrakis(dimethylamino)titanium (TDMAT) with plasma densification at about 400°C. In another embodiment, the gate fill barrier 158 may be titanium nitride formed by an atomic layer deposition process comprising pulses of titanium chloride (TiCl) and ammonia (NH_3) at about 300 °C. In still another embodiment, the gate fill barrier 158 may be a bi-layer of titanium and titanium nitride, wherein a titanium layer maybe formed by physical vapor deposition and the titanium nitride may be formed as discussed above. The gate barrier layer 158 may allow for the use of tungsten hexafluoride to deposit tungsten in a subsequent step to prevent fluorine attack. The use of the titanium layer in the titanium/titanium nitride bi-layer may act as a gettering agent for any fluorine that may diffuse through the titanium nitride layer.

As shown in FIG. 16, a tungsten gate fill material 162 may be deposited on the gate fill barrier 158. The tungsten gate fill material 162 may be formed by any technique known in the art. In one embodiment, a nucleation layer may be formed, such as pulsed diborane and tungsten hexafluoride at about 300 °C, followed by bulk tungsten grown by a tungsten hexafluoride reacting with hydrogen at about 395 °C. In one embodiment, the tungsten gate fill material 162 is a tungsten-containing material. In another embodiment, the tungsten gate fill material 162 is substantially pure tungsten.

Excess tungsten gate fill material 162 (e.g. tungsten gate fill material 162 not within the gate trench 154 of FIG. 16) may be removed to form the non-planar transistor gate electrode 126 (see also FIG. 1), as shown in FIG. 17. The removal of the excess tungsten gate fill material 162 may be achieved by any technique known in the art, including but not limited to chemical mechanical polishing (CMP), etching, and the like.

As shown in FIG. 18, a portion of the non-planar transistor gate electrode 126 may be removed to form a recess 164 and a recessed non-planar transistor gate 166. The removal may be accomplished by any known technique, including but not limited to wet or dry etching. In one embodiment, the formation of the recess may result from a combination of a dry etch and a wet etch. For example, the tungsten gate fill material 162 may be recessed with a sulfur hexafluoride dry etch and the NMOS work-function material 156 may be recessed with a subsequent wet etch.

As shown in FIG. 19, a capping dielectric material 168 may be deposited to fill the recess 164 of FIG. 18. The capping dielectric material 168 may be any appropriate material, including but not limited to silicon nitride (Si_3N_4) and silicon carbide (SiC), and may be formed by any appropriate deposition technique. The capping dielectric material 168 may be planarized to remove excess capping dielectric material 168 (e.g. capping dielectric material 168 not within the recess of FIG. 16) to form a capping dielectric structure 170 on the recessed non-planar transistor gate 166 and between a gate spacers 144, as shown in FIG. 20. The removal of the excess capping dielectric material 168 may be achieved by any technique known in the art, including but not limited to chemical mechanical polishing (CMP), etching, and the like.

As shown in FIG. 21, a second dielectric material layer 172 may be deposited over the first dielectric material layer 152, the gate spacers 144, and the capping dielectric structure 170. The second dielectric material layer 172 may be formed from any appropriate dielectric material, including but not limited to silicon dioxide (SiO_2), silicon oxynitride (SiO_xN_y), and silicon nitride (Si_3N_4), by any known deposition technique. As

shown in FIG. 22, an etch mask 174 may be patterned with at least one opening 176 on the second dielectric material layer 172, such as by well known lithographic techniques.

As shown in FIG. 23, a contact opening 182 may be formed through the first dielectric material layer 152 and the second dielectric material layer 172 by etching through the etch mask opening 176 of FIG. 24 to expose a portion of the source/drain region 150. The etch mask 174 of FIG. 23 may be removed thereafter, as shown in FIG. 24. In one embodiment, the first dielectric material layer 152 and the second dielectric material layer 172 differs from dielectric material of both the gate spacers 144 and the capping dielectric structure 170, such that the etching of the first dielectric material layer 152 and the second dielectric layer 172 may be selective to the gate spacers 144 and the capping dielectric structure 170 (i.e. etches faster). This is known in the art as a self-aligning.

As shown in FIG. 25, a conductive contact material 188 may be deposited in the contact opening 182 of FIG. 23. The conductive contact material 188 may include, but is not limited to, polysilicon, tungsten, ruthenium, palladium, platinum, cobalt, nickel, hafnium, zirconium, titanium, tantalum, aluminum, titanium carbide, zirconium carbide, tantalum carbide, hafnium carbide, aluminum carbide, other metal carbides, metal nitrides, and metal oxides. It is understood that various adhesion layers, barrier layers, silicide layers, and/or conductive layers may be conformally disposed or formed in the contact opening 182 of FIG. 23 prior to the deposition of the conductive contact material 188.

As shown in FIG. 26, excess conductive contact material 188 of FIG. 27 (e.g. conductive contact material 188 not within the contact opening 182 of FIG. 24) may be removed to form a source/drain contact 190. The removal of the excess conductive contact material 188 may be achieved by any technique known in the art, including but not limited to chemical mechanical polishing (CMP), etching, and the like.

As previously discussed, in one embodiment, the first dielectric material layer 152 and the dielectric material layer 168 differs from dielectric material of both the gate spacers 144 and the capping dielectric structure 166, such that the etching of the first dielectric material layer 152 and the second dielectric layer 168 may be selective to the gate spacers 144 and the capping dielectric structure 166 (i.e. etches faster). Thus, the recessed non-planar transistor 162 is protected during the formation of the contact opening 182. This allows for the formation of a relatively large sized source/drain contact 190, which may increase the transistor drive current performance, without the risk of shorting between the source/drain contact 190 and the recessed non-planar transistor gate 162.

Although the present description relates to non-planar NMOS transistors, it is understood that integrated circuitry into which the non-planar NMOS transistor are incorporated may also include non-planar PMOS transistors. Thus, the process of fabricating non-planar NMOS transistors may be incorporated into an overall integrated circuitry fabrication process.

In one embodiment, as shown in the process 200 of flow diagram in FIG. 27, after the formation of the structures from FIG. 2-13, a PMOS work-function material, such as titanium nitride, may be deposited in the gate trench, as defined in block 210. As defined in block 220, a portion the PMOS work-function material, within areas for fabrication of NMOS gates may be removed, such as by resist patterning and etching, as known in the art. The process may then be continued starting at FIG. 14, such as leaving the patterned resist in place while depositing the NMOS work-function material.

In one embodiment, as shown in the process 300 of flow diagram in FIG. 28, after the formation of the structures from FIG. 2-14, a portion of the NMOS work-function material within areas for fabrication of PMOS gates may be removed, such as by resist patterning and etching, as known in the art. As define in block 310, a PMOS work-function material, such as titanium nitride, may be deposited in the gate trench, as defined in block 320. The process may then be continued starting at FIG. 15. It is understood that the separate formation of the gate fill barrier 158, as shown in FIG. 15, may not be required as the PMOS work-function deposited in block 310 may also serve as the gate fill barrier 158.

It is understood that the subject matter of the present description is not necessarily limited to specific applications illustrated in FIGs. 1-28. The subject matter may be applied to other microelectronic device fabrication applications, as will be understood to those skilled in the art.

Having thus described in detail embodiments of the present invention, it is understood that the invention defined by the appended claims is not to be limited by particular details set forth in the above description, as many apparent variations thereof are possible without departing from the spirit or scope thereof.

CLAIMS

What is claimed is:

1. A transistor gate, comprising:

a pair of gate spacers; and

a gate electrode disposed between the pair of gate spacers, wherein the gate electrode includes:

an NMOS work-function material adjacent at least a portion of the pair of gates spacers and comprising aluminum, titanium, and carbon;

a titanium-containing gate fill barrier adjacent the NMOS work-function material; and

a tungsten-containing gate fill material adjacent the gate fill barrier.

2. The transistor gate of claim 1, wherein the gate electrode is non-planar.

3. The transistor gate of claim 1, wherein the NMOS work-function material comprises between about 20 to 40% by weight aluminum, between about 30 to 50% by weight titanium, and between about 10 to 30% by weight carbon.

4. The transistor gate of claim 1, wherein the NMOS work-function material comprises about 33% by weight aluminum, about 43% by weight titanium, and about 24% by weight carbon.

5. The transistor gate of claim 1, further including a capping dielectric structure disposed adjacent the non-planar gate electrode and between the pair of gate spacers.

6. A method of fabricating a transistor gate, comprising:

forming a pair of gate spacers; and

forming a gate electrode disposed between the pair of gate spacers comprising

conformally depositing an NMOS work-function material adjacent the pair of gates spacers and comprising aluminum, titanium, and carbon;

conformally depositing a titanium-containing gate fill barrier adjacent the NMOS work-function material; and

depositing a tungsten-containing gate fill material adjacent the gate fill barrier.

7. The method of claim 6, wherein conformally depositing the NMOS work-function material comprises conformally depositing the NMOS work-function material having a composition between about 20 to 40% aluminum, between about 30 to 50% titanium, and between about 10 to 30% carbon.

8. The method of claim 7, wherein conformally depositing the NMOS work-function material comprises conformally depositing the NMOS work-function material having a composition of about 33% by weight aluminum, about 43% by weight titanium, and between about 24% by weight carbon.

9. The method of claim 6, further including:

conformally depositing a PMOS work-function material adjacent the pair of gates spacers; and

removing a portion of the PMOS work-function material within areas for fabrication of the NMOS gate electrode prior to depositing the NMOS work-function material.

10. The method of claim 9, wherein conformally depositing the PMOS work-function material comprises conformally depositing a titanium nitride PMOS work-function material.

11. The method of claim 6, further including:

removing a portion of the NMOS work-function material within areas for fabrication of PMOS gate electrodes; and

conformally depositing a PMOS work-function material adjacent the pair of gates spacers and on the NMOS work-function material within areas for fabrication of the NMOS gate electrodes.

12. The method of claim 11, wherein conformally depositing the PMOS work-function material comprises conformally depositing a titanium nitride PMOS work-function material.

13. The method of claim 6, further including:

removing a portion of the NMOS work-function material within areas for fabrication of PMOS gate electrodes; and

conformally depositing a titanium-containing layer as a gate fill barrier adjacent the NMOS work-function material within areas for fabrication of the NMOS gate electrodes and as a PMOS work-function material within areas for fabrication of PMOS gate electrodes.

14. The method of claim 13, wherein conformally depositing a titanium-containing layer comprises conformally depositing a titanium nitride layer.

15. The method of claim 6, further including forming a capping dielectric structure disposed adjacent the non-planar gate electrode and between the pair of gate spacers.

16. The method of claim 15, wherein forming a capping dielectric structure disposed adjacent the non-planar gate electrode and between the pair of gate spacers, comprises:

forming a recess between the gate spacers by removing a portion of the gate electrode; and

depositing a capping dielectric material within the recess.

17. A method of fabricating a non-planar transistor gate, comprising:

forming a sacrificial non-planar transistor gate over a non-planar transistor fin;

depositing a dielectric material layer over the sacrificial non-planar transistor gate and the non-planar transistor fin;

forming non-planar transistor gate spacers from a portion of the dielectric material layer adjacent the sacrificial non-planar transistor gate;

forming a source/drain region;

removing the sacrificial non-planar transistor gate to form a gate trench between the non-planar transistor gate spacers and expose a portion of the non-planar transistor fin;

forming a gate dielectric adjacent the non-planar transistor fin within the gate trench;

forming a gate electrode disposed between the pair of gate spacers, comprising

conformally depositing an NMOS work-function material adjacent the pair of gates spacers and comprising aluminum, titanium, and carbon;

conformally depositing a titanium-containing gate fill barrier adjacent the NMOS work-function material; and

depositing a tungsten-containing gate fill material adjacent the gate fill barrier;

removing a portion of the gate electrode to form a recess between the non-planar transistor gate spacers;

forming a capping dielectric structure within the recess;

forming at least one dielectric material layer over the source/drain region, the non-planar transistor gate spacers, and the capping dielectric structure; and

forming a contact opening through the at least one dielectric material to contact at least a portion of the source/drain region.

18. The method of claim 17, wherein conformally depositing the NMOS work-function material comprises conformally depositing the NMOS work-function material having a composition between about 20 to 40% by weight aluminum, between about 30 to 50% by weight titanium, and between about 10 to 30% by weight carbon.

19. The method of claim 17, wherein conformally depositing the NMOS work-function material comprises conformally depositing the NMOS work-function material having a composition of about 33% by weight aluminum, about 43% by weight titanium, and between about 24% by weight carbon.

20. The method of claim 17, further including:

conformally depositing a PMOS work-function material adjacent the pair of gates spacers; and

removing a portion of the PMOS work-function material within areas for fabrication of the NMOS gate electrode prior to depositing the NMOS work-function material.

21. The method of claim 20, wherein conformally depositing the PMOS work-function material comprises conformally depositing a titanium nitride PMOS work-function material.

22. The method of claim 17, further including:

removing a portion of the NMOS work-function material within areas for fabrication of PMOS gate electrodes; and

conformally depositing a PMOS work-function material adjacent the pair of gates spacers and on the NMOS work-function material within areas for fabrication of the NMOS gate electrodes.

23. The method of claim 22, wherein conformally depositing the PMOS work-function material comprises conformally depositing a titanium nitride PMOS work-function material.

24. The method of claim 17, further including:

removing a portion of the NMOS work-function material within areas for fabrication of PMOS gate electrodes; and

conformally depositing a titanium-containing layer as a gate fill barrier adjacent the NMOS work-function material within areas for fabrication of the NMOS gate electrodes and as a PMOS work-function material within areas for fabrication of PMOS gate electrodes.

25. The method of claim 22, wherein conformally depositing a titanium-containing gate fill barrier comprises conformally depositing a titanium nitride layer.

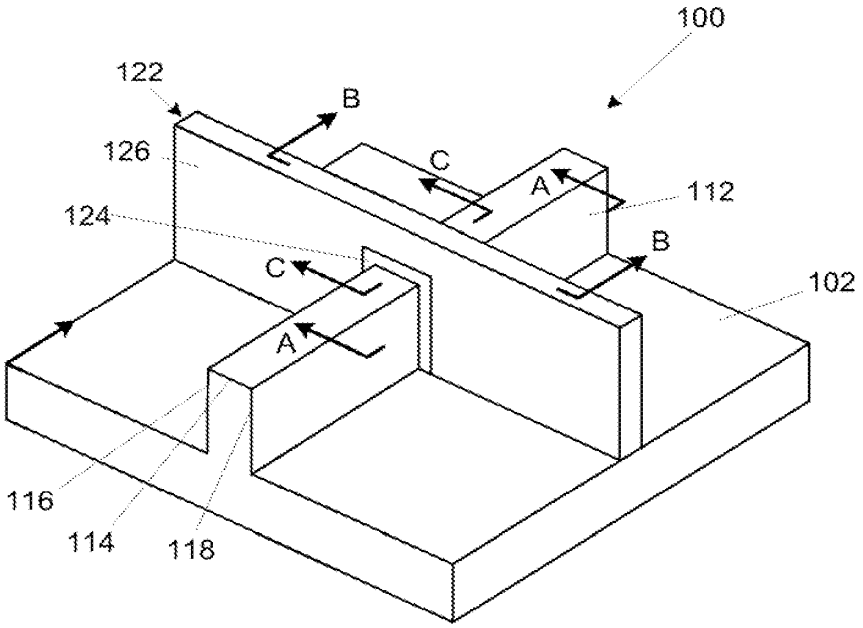


FIG. 1

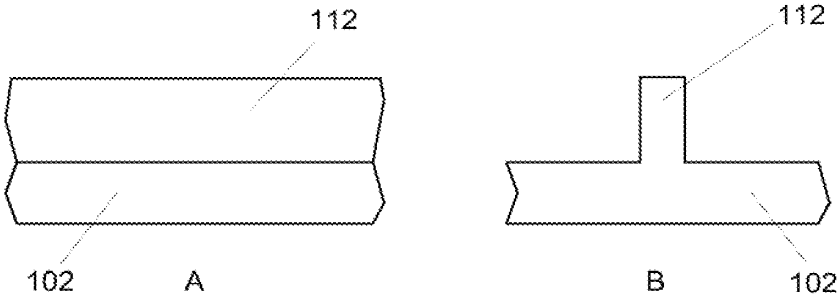


FIG. 2

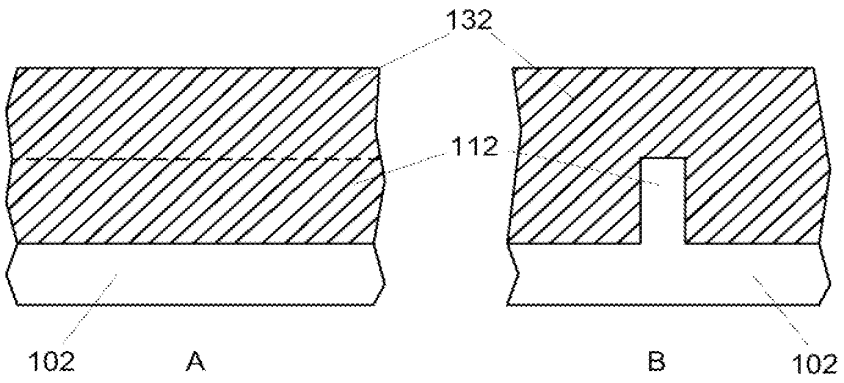


FIG. 3

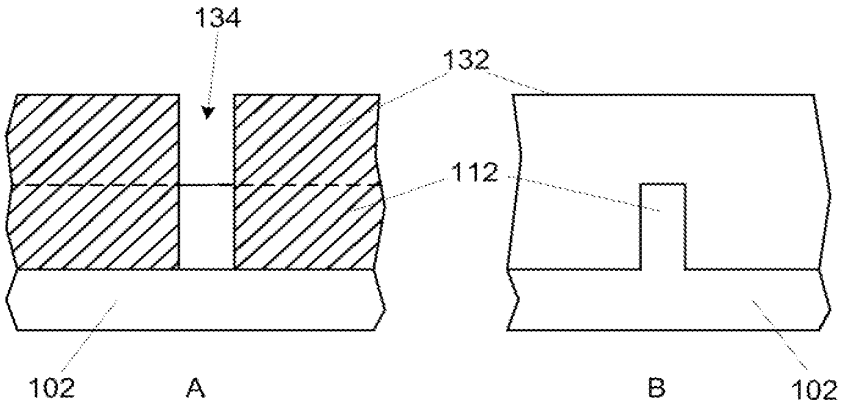


FIG. 4

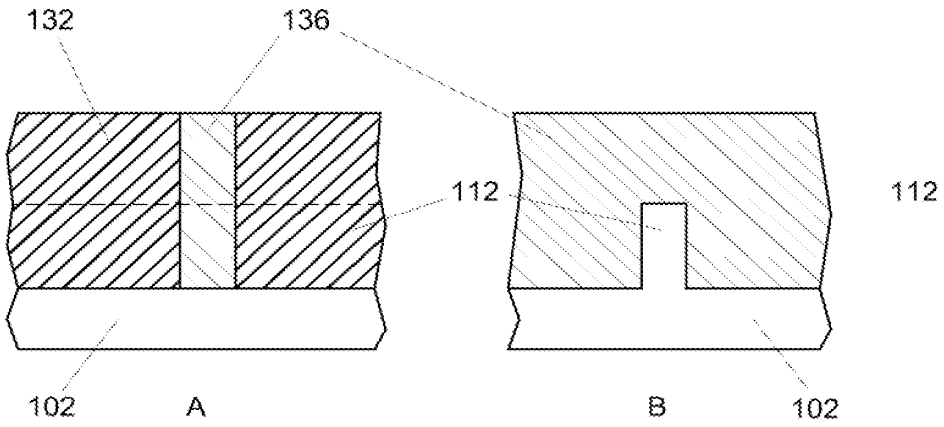


FIG. 5

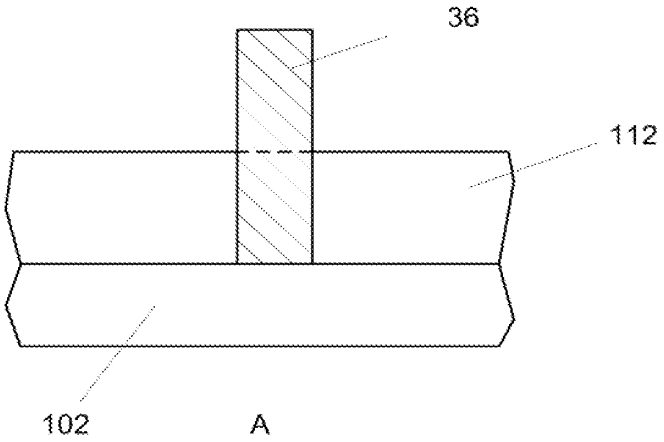


FIG. 6

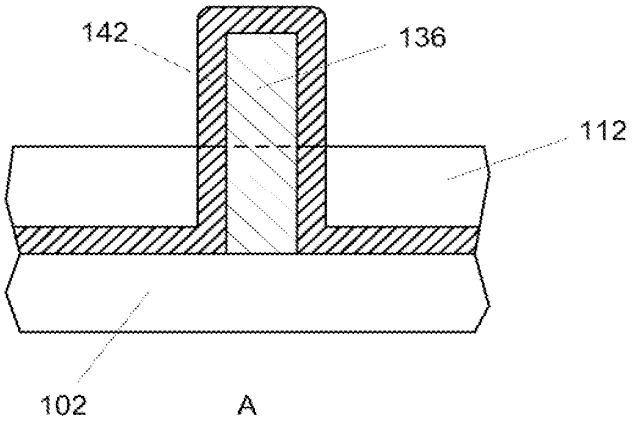


FIG. 7

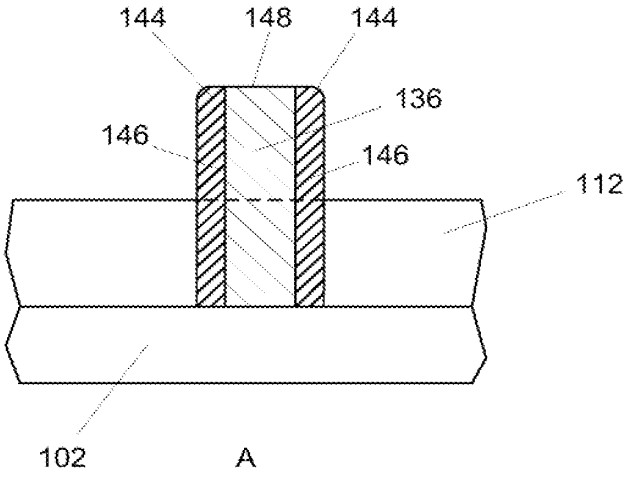


FIG. 8

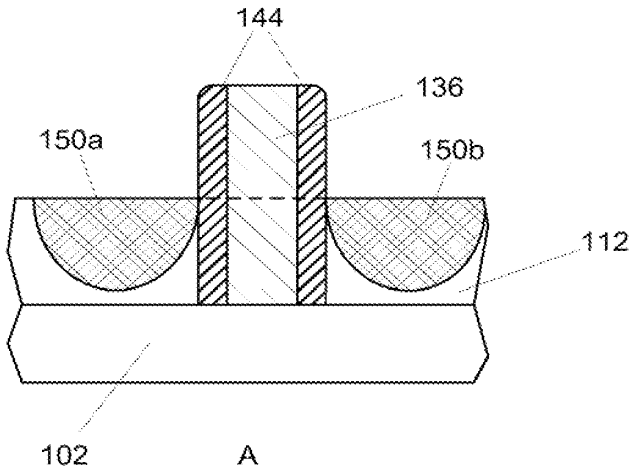


FIG. 9

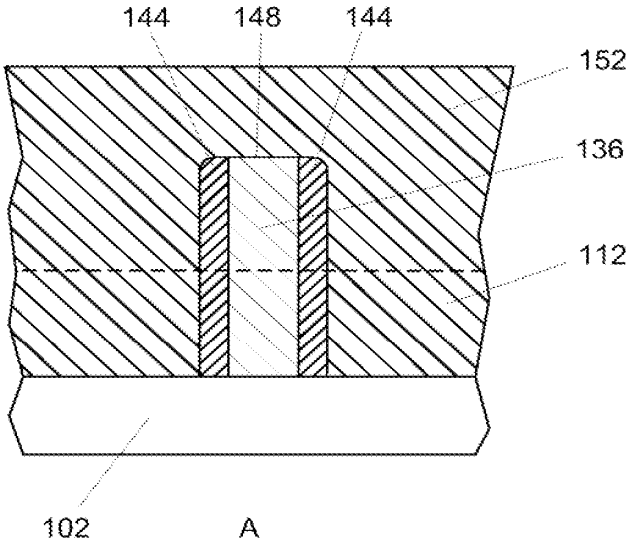


FIG. 10

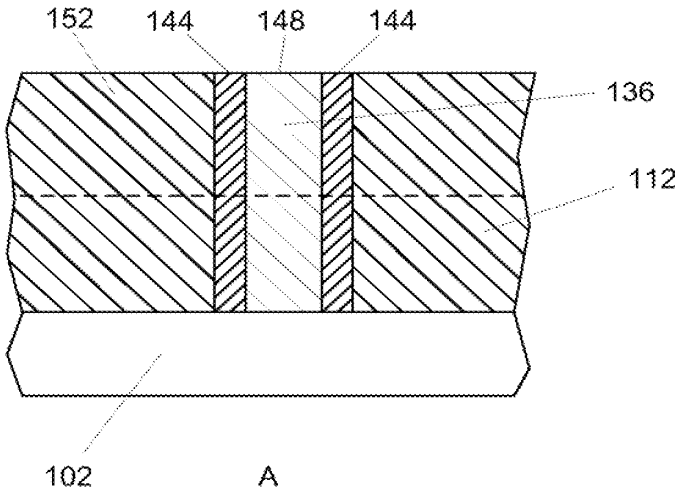


FIG. 11

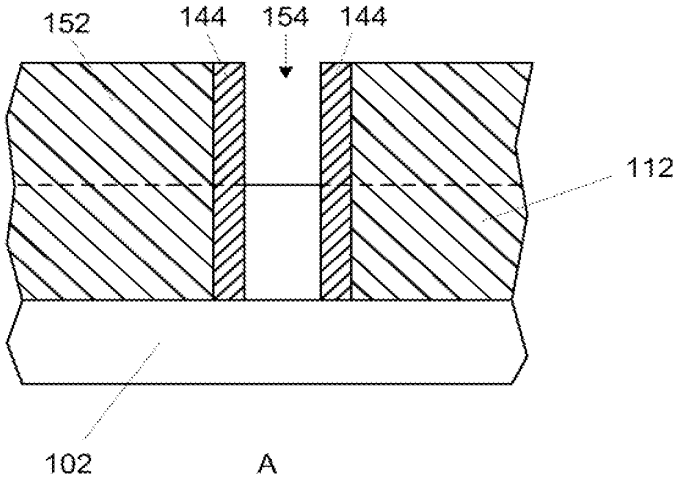


FIG. 12

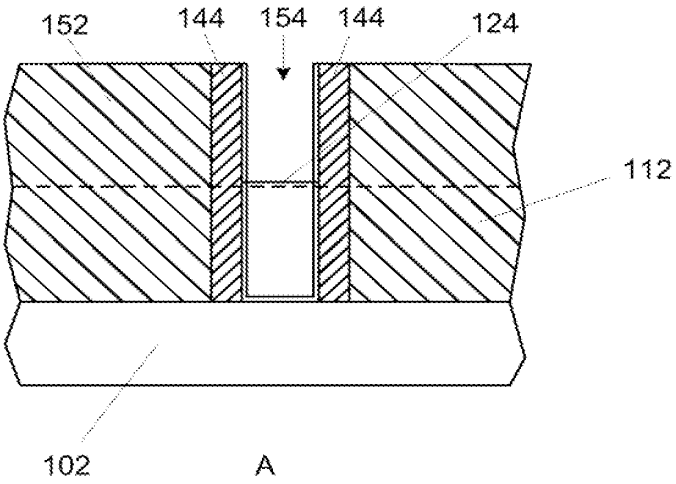


FIG. 13

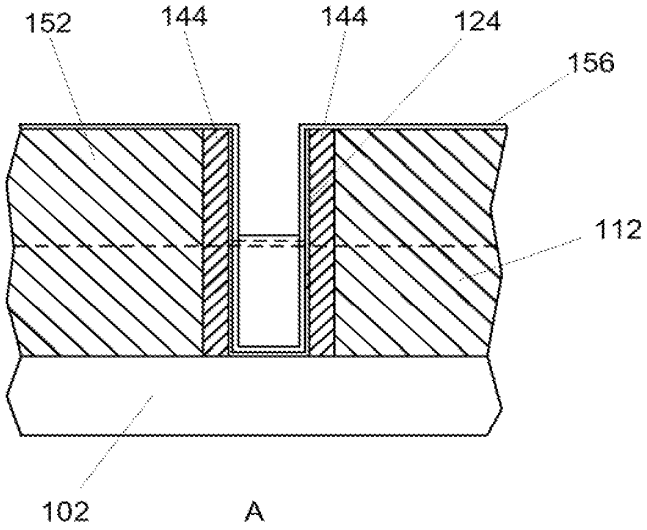


FIG. 14

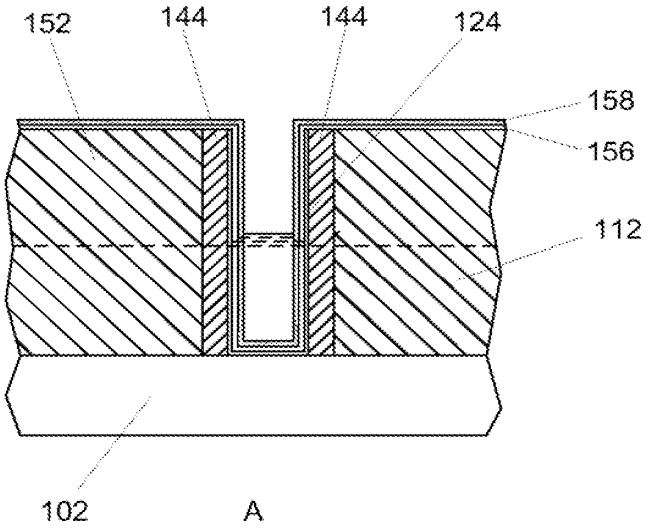

152
144
144
124
158
156
112
102
A

FIG. 15

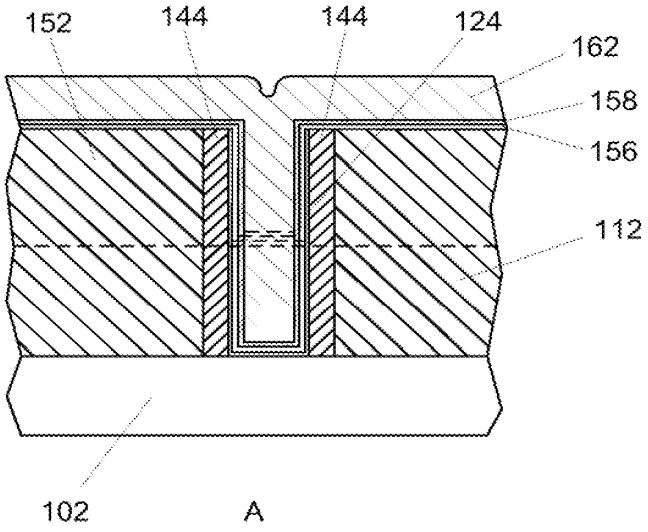

152
144
144
124
162
158
156
112
102
A

FIG. 16

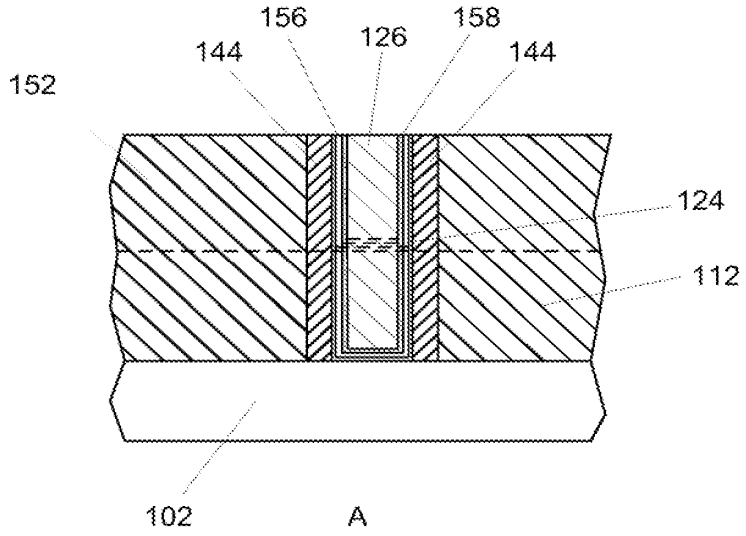

156
158
126
144
144
152
124
112
102
A

FIG. 17

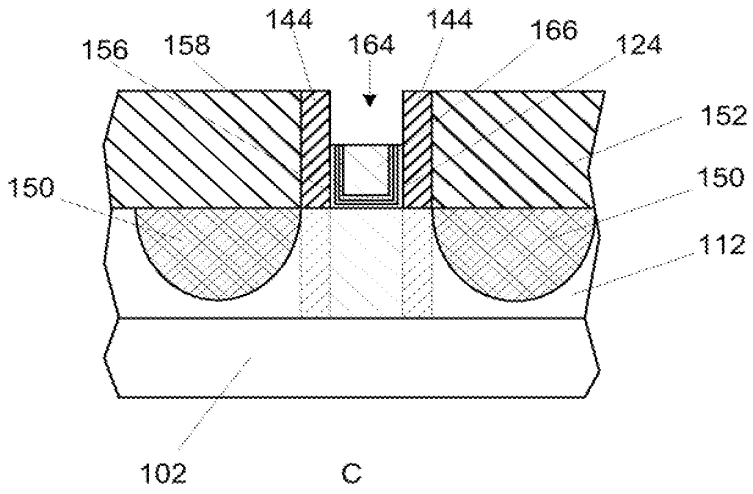

144
144
156
158
164
166
124
152
150
150
112
102
C

FIG. 18

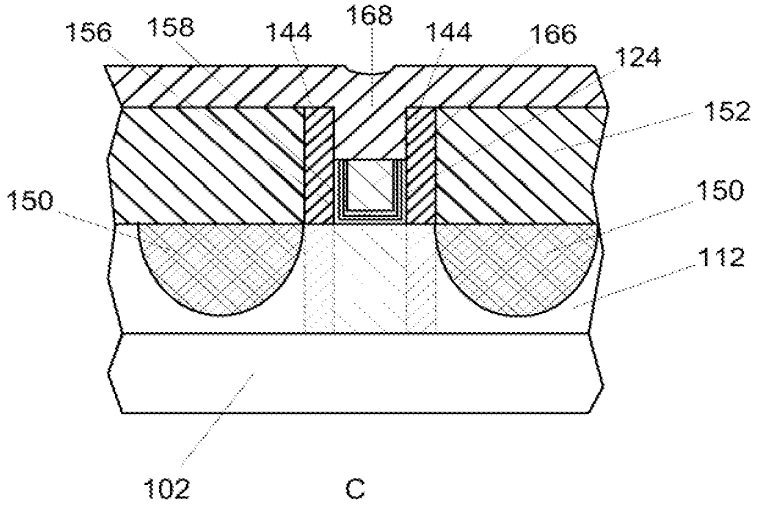

156
158
144
168
144
166
124
152
150
150
112
102
C

FIG. 19

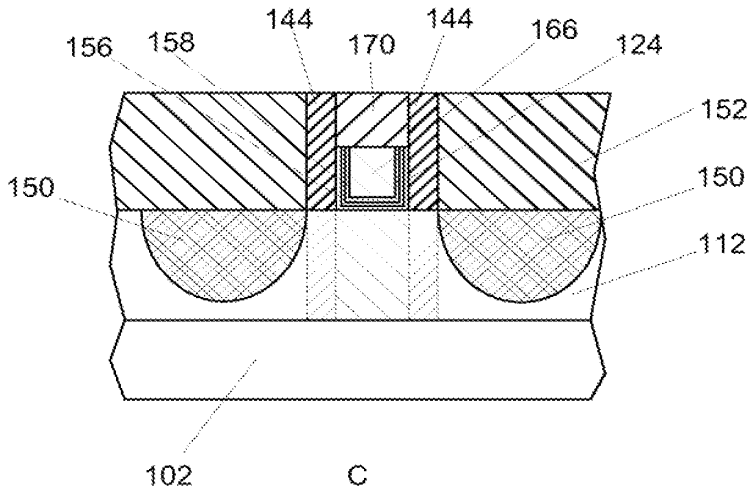

144
156
158
170
144
166
124
152
150
150
112
102
C

FIG. 20

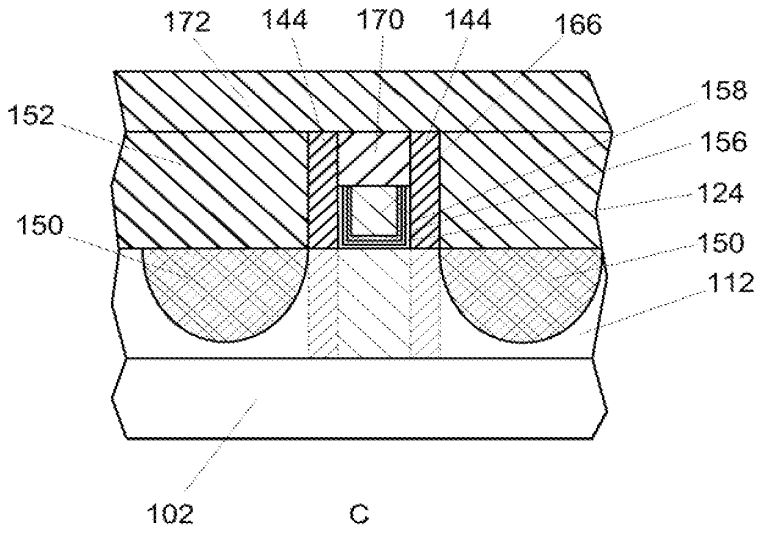

172
144
170
144
166
158
152
156
124
150
150
112
102
C

FIG. 21

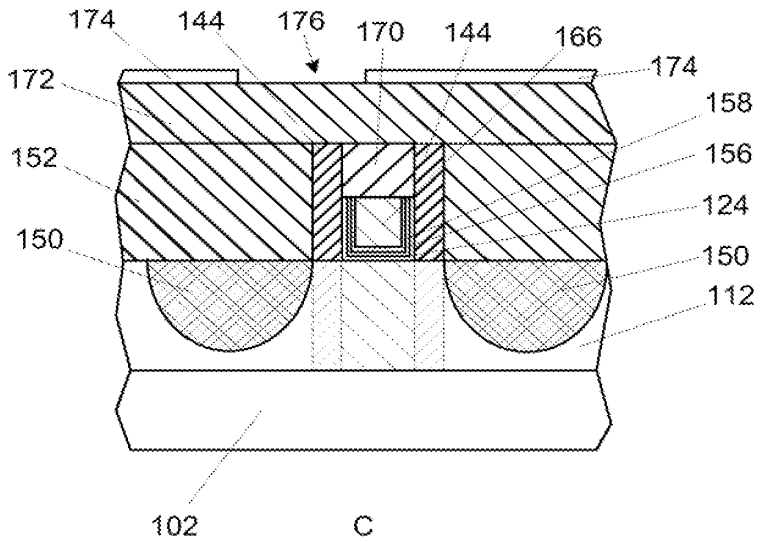

174
144
176
170
144
166
174
172
158
152
156
124
150
150
112
102
C

FIG. 22

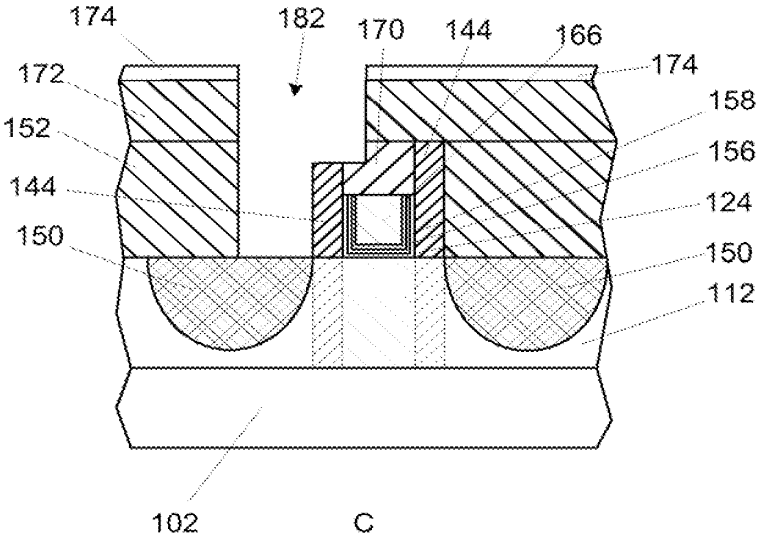

174
182
170
144
166
172
174
158
152
156
144
124
150
150
112
102
C

FIG. 23

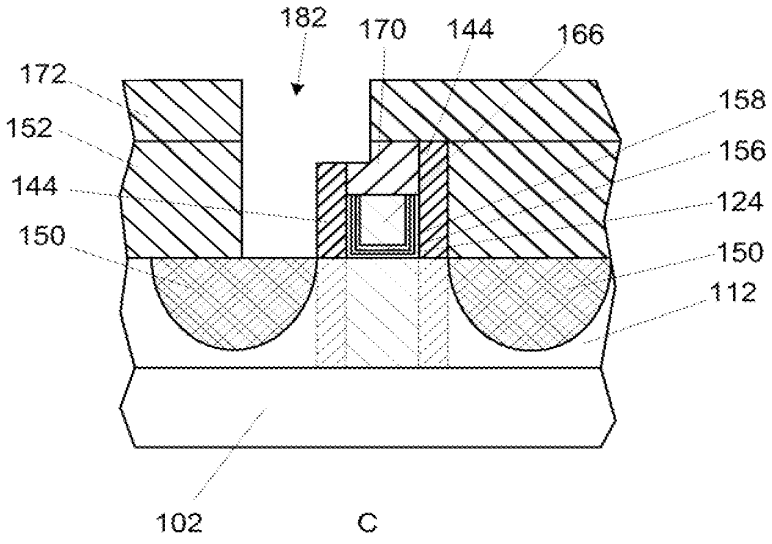

182
170
144
166
172
158
152
156
144
124
150
150
112
102
C

FIG. 24

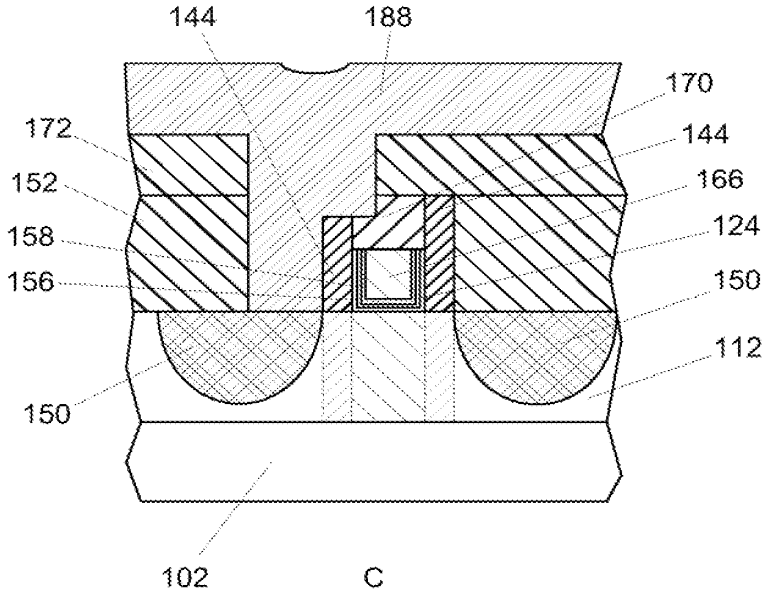

144
188
170
172
144
152
166
158
124
156
150
112
150
102
C

FIG. 25

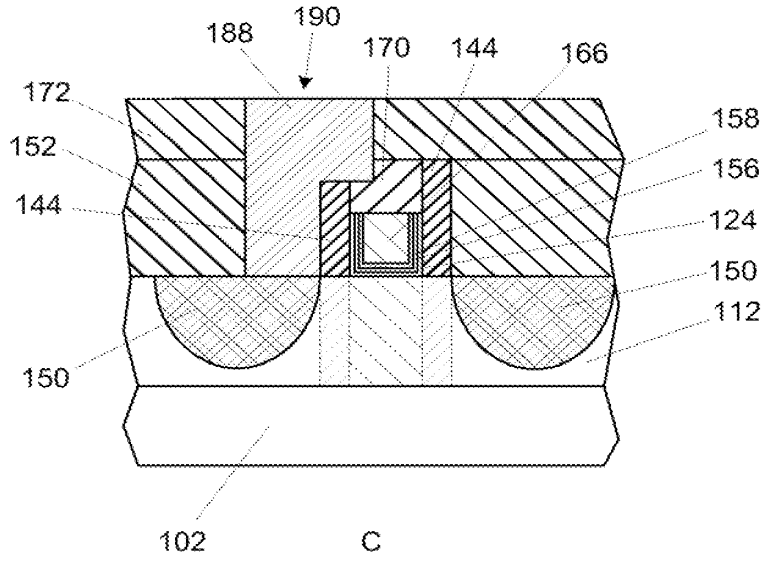

188
190
170
144
166
172
158
152
156
144
124
150
112
150
102
C

FIG. 26

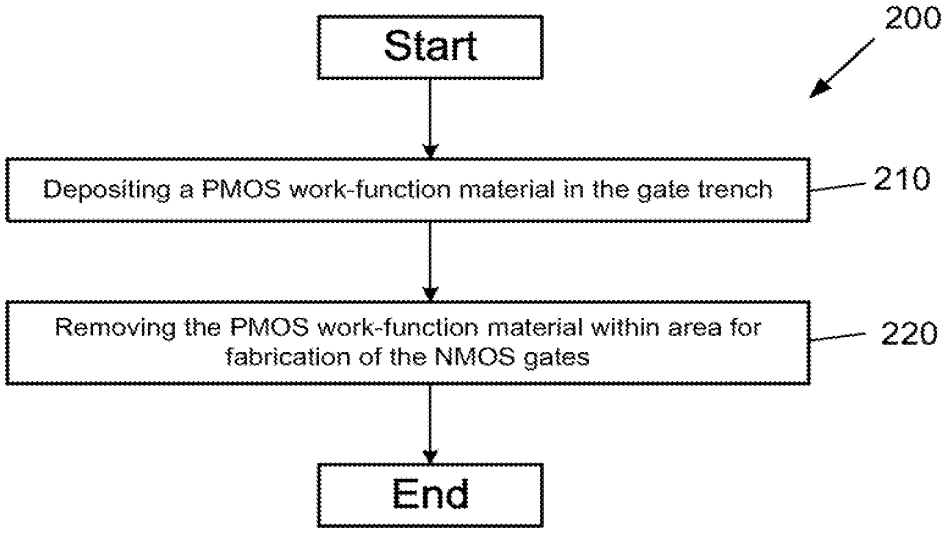

Start
200
Depositing a PMOS work-function material in the gate trench
210
Removing the PMOS work-function material within area for fabrication of the NMOS gates
220
End

FIG. 27

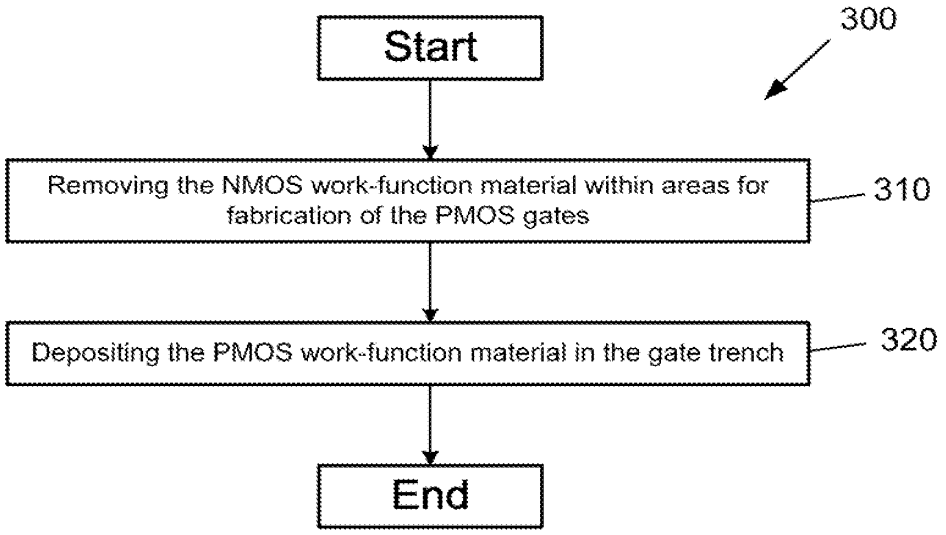

Start
300
Removing the NMOS work-function material within areas for fabrication of the PMOS gates
310
Depositing the PMOS work-function material in the gate trench
320
End

FIG. 28

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2011/054294

A. CLASSIFICATION OF SUBJECT MATTER

H01L 29/78(2006.01)i, H01L 21/336(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 29/78; H01L 21/336; H01L 21/28; H01L 21/338; H01L 27/12

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: non-planar, tungsten and gate

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 7528025 B2 (BRASK JUSTIN K. et al.) 05 May 2009 See the abstract; figs. 1-5; column 3, line 4 - column 25, line 47.	1-25
A	KR 10-0585178 B1 (SAMSUNG ELECTRONICS CO., LTD.) 30 May 2006 See the abstract; figs. 1-21; claims 1-31.	1-25
A	US 2011-0147831 A1 (STEIGERWALD JOSEPH M. et al.) 23 June 2011 See the abstract; figs. 1-4; paragraphs [0009]-[0029].	1-25

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15 MAY 2012 (15.05.2012)	**15 MAY 2012 (15.05.2012)**

Name and mailing address of the ISA/KR

Korean Intellectual Property Office
Government Complex-Daejeon, 189 Cheongsa-ro,
Seo-gu, Daejeon 302-701, Republic of Korea

Facsimile No. 82-42-472-7140

Authorized officer

Lee,Sang Ho

Telephone No. 82-42-481-8221

Form PCT/ISA/210 (second sheet) (July 2009)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2011/054294

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 7528025 B2	05.05.2009	US 2006-0071275 A1	06.04.2006
		US 2006-0138552 A1	29.06.2006
		US 2006-0138553 A1	29.06.2006
		US 2008-0090397 A1	17.04.2008
		US 2009-0149012 A1	11.06.2009
		US 7326656 B2	05.02.2008
		US 7361958 B2	22.04.2008
		US 7531437 B2	12.05.2009
KR 10-0585178 B1	30.05.2006	US 2006-0175669 A1	10.08.2006
US 2011-0147831 A1	23.06.2011	None	

Form PCT/ISA/210 (patent family annex) (July 2009)

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
4 April 2013 (04.04.2013)

WIPO | PCT

(10) International Publication Number
WO 2013/048516 A1

(51) International Patent Classification:
H01L 29/78 (2006.01) *H01L 21/336* (2006.01)

(21) International Application Number:
PCT/US2011/054464

(22) International Filing Date:
30 September 2011 (30.09.2011)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant *(for all designated States except US)*: **INTEL CORPORATION** [US/US]; 2200 Mission College Boulevard, Santa Clara, California 95052 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **ROSENBAUM, Aaron W.** [US/US]; 5530 NW Osprey Place, Portland, Oregon 97229 (US). **MEI, Din-How** [US/US]; 5366 NW 132nd Ave., Portland, Oregon 97229 (US). **PRADHAN, Sameer S.** [IN/US]; 17923 NW Sylvania Lane, Portland, Oregon 97229 (US).

(74) Agent: **BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP**; 1279 Oakmead Parkway, Sunnyvale, CA 94086 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

---- *of inventorship (Rule 4.17(iv))*

Published:

---- *with international search report (Art. 21(3))*

(54) Title: CAPPING DIELECTRIC STRUCTURE FOR TRANSISTOR GATES

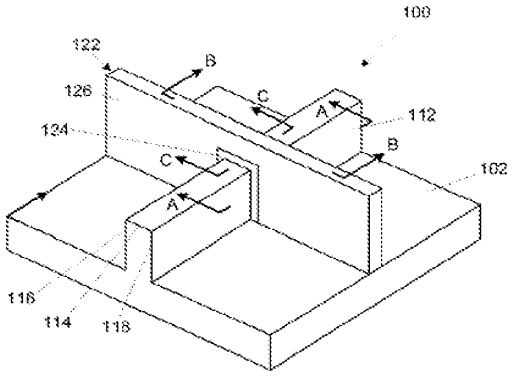


FIG. 1

(57) Abstract: The present description relates to the field of fabricating microelectronic transistors, including non-planar transistors, for microelectronic devices. Embodiments of the present description relate to the formation a recessed gate electrode capped by a substantially void-free dielectric capping dielectric structure which may be formed with a high density plasma process.

WO 2013/048516 A1

CAPPING DIELECTRIC STRUCTURE FOR TRANSISTOR GATES

BACKGROUND

Embodiments of the present description generally relate to the field of microelectronic device fabrication and, more particularly, to the fabrication of capping dielectric structures within non-planar transistor gates.

BRIEF DESCRIPTION OF THE DRAWINGS

The subject matter of the present disclosure is particularly pointed out and distinctly claimed in the concluding portion of the specification. The foregoing and other features of the present disclosure will become more fully apparent from the following description and appended claims, taken in conjunction with the accompanying drawings. It is understood that the accompanying drawings depict only several embodiments in accordance with the present disclosure and are, therefore, not to be considered limiting of its scope. The disclosure will be described with additional specificity and detail through use of the accompanying drawings, such that the advantages of the present disclosure can be more readily ascertained, in which:

FIG. 1 is a perspective view of a non-planar transistor, according to an embodiment of the present description.

FIG. 2 illustrates a side cross-sectional view of a non-planar transistor fin formed in or on a microelectronic substrate.

FIG. 3 illustrates a side cross-sectional view of a sacrificial material deposited over the non-planar transistor fin of FIG. 2, according to an embodiment of the present description.

FIG. 4 illustrates a side cross-sectional view of a trench formed in the sacrificial material deposited to expose a portion of the non-planar transistor fin of FIG. 3, according to an embodiment of the present description.

FIG. 5 illustrates a side cross-sectional view of a sacrificial gate formed in the trench of FIG. 4, according to an embodiment of the present description.

FIG. 6 illustrates a side cross-sectional view of the sacrificial gate after the removal of the sacrificial material of FIG. 5, according to an embodiment of the present description.

FIG. 7 illustrates a side cross-sectional view of a conformal dielectric layer deposited over the sacrificial gate and microelectronic substrate of FIG. 6, according to an embodiment of the present description.

FIG. 8 illustrates a side cross-sectional view of gate spacers formed from the conformal dielectric layer of FIG. 7, according to an embodiment of the present description.

FIG. 9 illustrates a side cross-sectional view of a source region and a drain region formed in the non-planar transistor fin on either side of the gate spacers of FIG. 8, according to an embodiment of the present description.

FIG. 10 illustrates a side cross-sectional view of a first dielectric material deposited over the gate spacers, the sacrificial gate, the non-planar transistor fin, and the microelectronic substrate of FIG. 9, according to an embodiment of the present description.

FIG. 11 illustrates a side cross-sectional view of the structure of FIG. 10 after planarizing the first dielectric material to expose a top surface of the sacrificial gate, according to an embodiment of the present description.

FIG. 12 illustrates a side cross-sectional view of the structure of FIG. 11 after the removal of the sacrificial gate to form a gate trench, according to an embodiment of the present description.

FIG. 13 illustrates a side cross-sectional view of the structure of FIG. 12 after the formation of a gate dielectric adjacent the non-planar transistor fin between the gate spacers, according to an embodiment of the present description.

FIG. 14 illustrates a side cross-sectional view of a conductive gate material deposited in the gate trench of FIG. 13, according to an embodiment of the present description.

FIG. 15 illustrates a side cross-sectional view of the structure of FIG. 14 after the removal of excess conductive gate material to form a non-planar transistor gate, according to an embodiment of the present description.

FIG. 16 illustrates a side cross-sectional view of the structure of FIG. 15 after etching away a portion of the non-planar transistor gate to form a recessed non-planar transistor gate, according to an embodiment of the present description.

FIG. 17 illustrates a side cross-sectional view of the structure of FIG. 16 after depositing a capping dielectric material into the recess resulting from the formation of the recessed non-planar transistor gate, according to an embodiment of the present description.

FIG 18 illustrates a flow diagram of a high density deposition process for the deposition of the capping dielectric material of FIG. 17, according to an embodiment of the present description.

FIG. 19 illustrates a side cross-sectional view of the structure of FIG. 17 after the removal of excess capping dielectric material to form a capping dielectric structure on the non-planar transistor gate, according to an embodiment of the present description.

FIG. 20 illustrates a side cross-sectional view of a second dielectric material deposited over the first dielectric material layer, the gate spacers, and the sacrificial gate top surface of FIG. 19, according to an embodiment of the present description.

FIG. 21 illustrates a side cross-sectional view of an etch mask patterned on the second dielectric material of FIG. 20, according to an embodiment of the present description.

FIG. 22 illustrates a side cross-sectional view of a contact opening formed through the first and second dielectric material layer of FIG. 21, according to an embodiment of the present description.

FIG. 23 illustrates a side cross-sectional view of the structure of FIG. 22 after the removal of the etch mask, according to an embodiment of the present description.

FIG. 24 illustrates a side cross-sectional view of a conductive contact material deposited in the contact opening of FIG. 23, according to an embodiment of the present description.

FIG. 25 illustrates a side cross-sectional view of the structure of FIG. 24 after the removal of the excess conductive contact material to form a source/drain contact, according to an embodiment of the present description.

DETAILED DESCRIPTION

In the following detailed description, reference is made to the accompanying drawings that show, by way of illustration, specific embodiments in which the claimed subject matter may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the subject matter. It is to be understood that the various embodiments, although different, are not necessarily mutually exclusive. For example, a particular feature, structure, or characteristic described herein, in connection with one embodiment, may be implemented within other embodiments without departing from the spirit and scope of the claimed subject matter. References within this specification to "one embodiment" or "an embodiment" mean that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one implementation encompassed within the present invention. Therefore, the use of the phrase "one embodiment" or "in an embodiment" does not necessarily refer to the same embodiment. In addition, it is to be understood that the location or arrangement of

individual elements within each disclosed embodiment may be modified without departing from the spirit and scope of the claimed subject matter. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the subject matter is defined only by the appended claims, appropriately interpreted, along with the full range of equivalents to which the appended claims are entitled. In the drawings, like numerals refer to the same or similar elements or functionality throughout the several views, and that elements depicted therein are not necessarily to scale with one another, rather individual elements may be enlarged or reduced in order to more easily comprehend the elements in the context of the present description.

In the fabrication of non-planar transistors, such as tri-gate transistors and FinFETs, non-planar semiconductor bodies may be used to form transistors capable of full depletion with very small gate lengths (e.g., less than about 30 nm). These semiconductor bodies are generally fin-shaped and are, thus, generally referred to as transistor "fins". For example in a tri-gate transistor, the transistor fins have a top surface and two opposing sidewalls formed on a bulk semiconductor substrate or a silicon-on-insulator substrate. A gate dielectric may be formed on the top surface and sidewalls of the semiconductor body and a gate electrode may be formed over the gate dielectric on the top surface of the semiconductor body and adjacent to the gate dielectric on the sidewalls of the semiconductor body. Thus, since the gate dielectric and the gate electrode are adjacent to three surfaces of the semiconductor body, three separate channels and gates are formed. As there are three separate channels formed, the semiconductor body can be fully depleted when the transistor is turned on. With regard to finFET transistors, the gate material and the electrode only contact the sidewalls of the semiconductor body, such that two separate channels are formed (rather than three in tri-gate transistors).

Embodiments of the present description relate to the formation of microelectronic transistors, wherein the transistor includes a recessed gate electrode capped by a substantially void-free dielectric capping dielectric structure which may be formed with a high density plasma process. Although embodiments herein are described in terms of non-planar transistors and replacement gate techniques, the subject matter is not so limited, as the subject matter may be used in planar transistors and in non-replacement gate applications.

FIG. 1 is a perspective view of a non-planar transistor 100, including at least one gate formed on at least one transistor fin, which are formed on a microelectronic substrate 102. In an embodiment of the present disclosure, the microelectronic substrate 102 may

be a monocrystalline silicon substrate. The microelectronic substrate 102 may also be other types of substrates, such as silicon-on-insulator ("SOI"), germanium, gallium arsenide, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, gallium antimonide, and the like, any of which may be combined with silicon.

The non-planar transistor, shown as a tri-gate transistor, may include at least one non-planar transistor fin 112. The non-planar transistor fin 112 may have a top surface 114 and a pair of laterally opposite sidewalls, sidewall 116 and opposing sidewall 118, respectively.

As further shown in FIG. 1, at least one non-planar transistor gate 122 may be formed over the non-planar transistor fin 112. The non-planar transistor gate 122 may be fabricated by forming a gate dielectric layer 124 on or adjacent to the non-planar transistor fin top surface 114 and on or adjacent to the non-planar transistor fin sidewall 116 and the opposing non-planar transistor fin sidewall 118. A gate electrode 126 may be formed on or adjacent the gate dielectric layer 124. In one embodiment of the present disclosure, the non-planar transistor fin 112 may run in a direction substantially perpendicular to the non-planar transistor gate 122.

The gate dielectric layer 124 may be formed from any well-known gate dielectric material, including but not limited to silicon dioxide (SiO_2), silicon oxynitride (SiO_xN_y), silicon nitride (Si_3N_4), and high-k dielectric materials such as hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate. The gate dielectric layer 124 can be formed by well-known techniques, such as by conformally depositing a gate dielectric material and then patterning the gate dielectric material with well-known photolithography and etching techniques, as will be understood to those skilled in the art.

The gate electrode 126 can be formed of any suitable gate electrode material. In an embodiment of the present disclosure, the gate electrode 126 may be formed from materials that include, but are not limited to, polysilicon, tungsten, ruthenium, palladium, platinum, cobalt, nickel, hafnium, zirconium, titanium, tantalum, aluminum, titanium carbide, zirconium carbide, tantalum carbide, hafnium carbide, aluminum carbide, other metal carbides, metal nitrides, and metal oxides. The gate electrode 126 can be formed by well-known techniques, such as by blanket depositing a gate electrode material and then

patterning the gate electrode material with well-known photolithography and etching techniques, as will be understood to those skilled in the art.

A source region and a drain region (not shown in FIG. 1) may be formed in the non-planar transistor fin 112 on opposite sides of the gate electrode 126. In one embodiment, the source and drain regions may be formed by doping the non-planar transistor fins 112, as will be understood to those skilled in the art. In another embodiment, the source and drain regions may be formed by removing potions of the non-planar transistor fins 112 and replacing these portions with appropriate material(s) to form the source and drain regions, as will be understood to those skilled in the art.

FIGs. 2-26 illustrate side cross-sectional view of one embodiment of fabricating a non-planar transistor, wherein FIGs. 2-5 are views along arrows A-A and B-B of FIG. 1, FIGs. 6-15 are views along arrows A-A of FIG. 1, and FIG. 16-26 are views along arrows C-C of FIG. 1.

As shown in FIG. 2, the non-planar transistor fin 112 may be formed by etching the microelectronic substrate 102 or by forming the non-planar transistor fin 112 on the microelectronic substrate 102 by any technique known in the art. As illustrate in FIG. 3, a sacrificial material 132 may be deposited over the non-planar transistor fin 112, as shown in FIG. 3, and a trench 134 may be formed in the sacrificial material 132 to expose a potion of the non-planar transistor fin 112, as shown in FIG. 4. The sacrificial material 132 may be any appropriate material known in the art, and the trench 134 may be formed by any technique known in the art, including but not limited to lithographic masking and etching.

As shown in FIG. 5, a sacrificial gate 136 may be formed in the trench 134 (see FIG. 4). The sacrificial gate 136 may be any appropriate material, such as a polysilicon material and the like, and may be deposited in the trench 134 (see FIG. 4) by any technique known in the art, including but not limited to chemical vapor deposition ("CVD") and physical vapor deposition ("PVD").

As shown in FIG. 6, the sacrificial material 132 of FIG. 5 may be removed to expose the sacrificial gate 136 by any technique known in the art, such as selectively etching the sacrificial material 132. As shown in FIG. 7, a conformal dielectric layer 142 may be deposited over the sacrificial gate 136 and microelectronic substrate 102. The conformal dielectric layer 142 may be any appropriate material, including but not limited to silicon nitride (Si_3N_4) and silicon carbide (SiC), and may be formed by any appropriate technique including but not limited to atomic layer deposition ("ALD").

As shown in FIG. 8, the conformal dielectric layer 142 of FIG. 7 may be etched, such as by directional etch with an appropriate etchant, to form a pair of gate spacers 144 on sidewalls 146 of the sacrificial gate 136, while substantially removing the conformal dielectric material layer 142 adjacent the microelectronic substrate 102 and a top surface 148 of the sacrificial gate 136. It is understood that fin spacers (not shown) may be simultaneously formed on sidewalls 116 and 118 (see FIG. 1) of the non-planar transistor fin 112 during the formation of the gate spacers 144.

As shown in FIG. 9, a source region 150a and a drain region 150b may be formed on either side of the gate spacers 144. In one embodiment, the source region 150a and the drain region 150b may be formed in the non-planar transistor fin 112 with the implantation of dopants. As will be understood to those skilled in that art, dopant implantation is a process of introducing impurities into semiconducting materials for the purpose changing its conductivity and electronic properties. This is generally achieved by ion implantation of either P-type ions (e.g. boron) or N-type ions (e.g. phosphorus), collectively referred to as "dopants". In another embodiment, portions of the non-planar transistor fin 112 may be removed by any technique known in the art, such as etching, and the source region 150a and a drain region 150b may be formed in place of the removed portions. The source region 150a and the drain region will hereinafter be referred to collectively as "source/drain region 150".

As shown in FIG. 10, a first dielectric material layer 152 may be deposited over the gate spacers 144, the sacrificial gate top surface 148, the non-planar transistor fin 112, and the microelectronic substrate 102. The first dielectric material layer 152 may be planarizing to expose the sacrificial gate top surface 148, as shown in FIG. 11. The planarization of the first dielectric material layer 152 may be achieved by any technique known in the art, including but not limited to chemical mechanical polishing (CMP).

As shown in FIG. 12, the sacrificial gate 136 of FIG. 11 may be removed to form a gate trench 154. The sacrificial gate 136 may be removed by any technique known in the art, such as a selective etch. As shown in FIG. 13, the gate dielectric layer 124, as also illustrated in FIG. 1, may be formed to abut the non-planar transistor fin 112, as previously discussed.

As shown in FIG. 14, a conductive gate material 156 may be deposited in the gate trench 154, and excess conductive gate material 156 (e.g. conductive gate material 156 not within the gate trench 154 of FIG. 12) may be removed to from the non-planar transistor gate electrode 126 (see also FIG. 1), as shown in FIG. 15. The materials and methods of

forming the gate electrode 126 have been previously discussed. The removal of the excess conductive gate material 156 may be achieved by any technique known in the art, including but not limited to chemical mechanical polishing (CMP), etching, and the like.

As shown in FIG. 16, a portion of the non-planar transistor gate electrode 126 may be removed to form a recess 158 and a recessed non-planar transistor gate 162. The removal may be accomplished by any known technique, including but not limited to wet or dry etching.

As shown in FIG. 17, a capping dielectric material 164 may be deposited to fill the recess 158 of FIG. 16. The capping dielectric material 164 may be any appropriate material, including but not limited to silicon nitride (Si_xN_y) and silicon carbide (Si_xC_y). However, known processes for depositing dielectrics, such as plasma enhanced chemical vapor deposition, may not be capable of filing recesses 158 that have high aspect ratios (height to width ratio) and may result in voids forming in the capping dielectric material 164. Such voids may result in contact-to-gate short circuits, as will be discussed. To prevent voids from forming, high temperature deposition techniques (e.g. greater than 400°C) may be employed. However, high temperature deposition may affect the work function of the non-planar transistor gate electrode 126, as will be understood by those skilled in the art. Furthermore, high temperature deposition may result in dopant movement or deactivation in the source/drain regions 150.

FIG. 18 is a flow diagram of a high density plasma (HDP) dielectric deposition process 200 for forming substantially void free capping dielectric material 164 (see FIG. 17) within a high aspect ratio recesses 158 (see FIG. 17). As defined in block 210, walls of a high density plasma chamber may be coated with a desired dielectric film, i.e. the dielectric to be deposited. As defined in block 220, a microelectronic substrate, such as a silicon wafer, may be placed on a chuck in the high density plasma chamber. In one embodiment, the chuck may be a water-cooled ceramic electrostatic chuck at room temperature, e.g. about 75°C. As defined in block 230, the high density plasma chamber may be pressurized with an inert gas, such as argon. In one embodiment, the high density plasma chamber may be pressure to a pressure greater than about 40 mTorr to strike a sustainable low power radio frequency (RF) plasma. As defined in block 240, RF electrodes within the high density plasma chamber may be powered up while introducing at least one reactive gas into the high density plasma chamber. In one embodiment, each of the RF electrodes, such as top and side electrodes, may be powered up to a range between about 2kV and 8kV for a time duration between about 30 and 60 seconds. The

reactive gas may include, but is not limited to oxygen, nitrogen, and the like. The microelectronic substrate temperature can be modulated between less than about 300°C and 600°C by adjusting the temperature of the chuck. It is understood that the time duration, microelectronic substrate temperature, RF power, and reactive gas mixture may be adjusted for a desired deposition result. As defined in block 250, the deposition gas may be introduced to the high density plasma chamber while powering a bias RF electrode. In one embodiment, a deposition gas comprising silane (SiH_4), nitrogen (N_2), argon (Ar), and helium (He) may be used to deposit a silicon nitride dielectric. In another embodiment, a deposition gas comprising silane (SiH_4), methane (CH_4), argon (Ar), and helium (He) may be used to deposit a silicon carbide dielectric. The RF electrode may be power to a range between about 3kV and 5kV with a bias RF electrode ranging from about 1kV and 3kV. The ratio of the nitrogen gas volume to the silane gas volume for silicon nitride deposition and ratio of the methane gas volume to the silane gas volume may be between about 0.5 and 9, depending on the desired properties of the dielectric layer, while the silane gas flow is kept between about 30 and 70 sccm. Under these conditions, the deposition rate may be in a range between about 7 to 30 Angstroms per second. It is understood that the deposition duration may be calculated based on the desired dielectric layer thickness and deposition rate. As defined in block 260, the deposition process is discontinued by discontinuing the introduction of deposition gas into the high density plasma deposition chamber and discontinuing power to the bias RF. The power to the RF electrodes may be ramped down and electrostatic charges are dissipated off of the microelectronic substrate, so that the microelectronic substrate can be removed from the electrostatic chuck. After removal the high density plasma chamber may be cleaned, such as by a remote plasma unit, and the walls of the high density plasma chamber may be recoated with a desired dielectric film.

The above-described process may result in simultaneous deposition and sputtering of the dielectric layer, wherein an appropriate deposition to sputtering ratio may result in a substantially void-free dielectric layer.

After deposition, the capping dielectric material 164 may be planarized to remove excess capping dielectric material 164 (e.g. capping dielectric material 164 not within the recess of FIG. 16) to form a capping dielectric structure 166 on the recessed non-planar transistor gate 162 and between a gate spacers 144, as shown in FIG. 19. The removal of the excess capping dielectric material 164 may be achieved by any technique known in the

art, including but not limited to chemical mechanical polishing (CMP), etching, and the like.

As shown in FIG. 20, a second dielectric material layer 168 may be deposited over the first dielectric material layer 152, the gate spacers 144, and the capping dielectric structure 166. The second dielectric material layer 168 may be formed from any appropriate dielectric material, including but not limited to silicon dioxide (SiO_2), silicon oxynitride (SiO_xN_y), and silicon nitride (Si_3N_4), by any known deposition technique. As shown in FIG. 21, an etch mask 172 may be patterned with at least one opening 174 on the second dielectric material layer 168, such as by well known lithographic techniques.

As shown in FIG. 22, a contact opening 182 may be formed through the first dielectric material layer 152 and the second dielectric material layer 168 by etching through the etch mask opening 174 of FIG. 21 to expose a portion of the source/drain region 150. The etch mask 172 of FIG. 22 may be removed thereafter, as shown in FIG. 23. In one embodiment, the first dielectric material layer 152 and the dielectric material layer 168 differs from dielectric material of both the gate spacers 144 and the capping dielectric structure 166, such that the etching of the first dielectric material layer 152 and the second dielectric layer 168 may be selective to the gate spacers 144 and the capping dielectric structure 166 (i.e. etches faster). This is known in the art as a self-aligning.

As shown in FIG. 24, a conductive contact material 188 may be deposited in the contact opening 182 of FIG. 23. The conductive contact material 188 may include, but is not limited to, polysilicon, tungsten, ruthenium, palladium, platinum, cobalt, nickel, hafnium, zirconium, titanium, tantalum, aluminum, titanium carbide, zirconium carbide, tantalum carbide, hafnium carbide, aluminum carbide, other metal carbides, metal nitrides, and metal oxides. It is understood that various adhesion layers, barrier layers, silicide layers, and/or conductive layers may be conformally disposed or formed in the contact opening 182 of FIG. 23 prior to the deposition of the conductive contact material 188.

As shown in FIG. 25, excess conductive contact material 188 of FIG. 24 (e.g. conductive contact material 188 not within the contact opening 182 of FIG. 12) may be removed to form a source/drain contact 190. The removal of the excess conductive contact material 188 may be achieved by any technique known in the art, including but not limited to chemical mechanical polishing (CMP), etching, and the like.

As previously discussed, in one embodiment, the first dielectric material layer 152 and the dielectric material layer 168 differs from dielectric material of both the gate

spacers 144 and the capping dielectric structure 166, such that the etching of the first dielectric material layer 152 and the second dielectric layer 168 may be selective to the gate spacers 144 and the capping dielectric structure 166 (i.e. etches faster). Thus, the recessed non-planar transistor 162 is protected during the formation of the contact opening 182. This allows for the formation of a relatively large sized source/drain contact 190, which may increase the transistor drive current performance, without the risk of shorting between the source/drain contact 190 and the recessed non-planar transistor gate 162. This is not possible if voids exist in the capping dielectric structure 144, as the voids would increase the likelihood of shorting between the source/drain contact 190 and the recessed non-planar transistor gate 162.

It is understood that the subject matter of the present description is not necessarily limited to specific applications illustrated in FIGs. 1-25. It is understood that although the illustrated embodiments are directed to non-planar applications, the subject matter may be applied to non-planar transistors and to non-replacement gate applications. Furthermore, the subject matter may be applied to other microelectronic device fabrication applications, as will be understood to those skilled in the art.

Having thus described in detail embodiments of the present invention, it is understood that the invention defined by the appended claims is not to be limited by particular details set forth in the above description, as many apparent variations thereof are possible without departing from the spirit or scope thereof.

CLAIMS

What is claimed is:

1. A transistor gate, comprising:

a pair of gate spacers

a recessed gate electrode disposed between the pair of gate spacers; and

a substantially void free capping dielectric structure disposed adjacent the recessed gate electrode and between the pair of gate spacers.

2. The transistor gate of claim 1, wherein the substantially void free capping dielectric structure comprises silicon nitride.

3. The transistor gate of claim 1, wherein the substantially void free capping dielectric structure comprises silicon carbide.

4. The transistor gate of claim 1, wherein the recessed gate electrode is a non-planar gate electrode.

5. A microelectronic device, comprising:

a non-planar transistor gate over a non-planar transistor fin, wherein the non-planar transistor gate comprises a gate electrode recessed between a pair of gate spacers and a substantially void free capping dielectric structure disposed on the recessed gate electrode between the gate spacers,

a source/drain region;

at least one dielectric material layer over the source/drain region, the non-planar transistor gate spacers, and the substantially void free capping dielectric structure; and

a source/drain contact extending through a portion of the at least one dielectric material layer to contact the source/drain region.

6. The microelectronic device of claim 5, wherein the substantially void free capping dielectric structure comprises silicon nitride.

7. The microelectronic device of claim 5, wherein the substantially void free capping dielectric structure comprises silicon carbide.

8. The microelectronic device of claim 5, wherein the source/drain contact abuts at least a portion of one non-planar transistor gate spacer.

9. The microelectronic device of claim 5, wherein the source/drain contact abuts at least a portion of the capping dielectric structure.

10. A method of fabricating a transistor gate, comprising:

forming a pair of gate spacers;

forming a gate electrode disposed between the pair of gate spacers; and

high density plasma depositing a capping dielectric structure on a top surface of the recessed gate electrode and between the pair of gate spacers.

11. The method of claim 10, wherein high density plasma depositing the capping dielectric structure comprises high density plasma depositing a silicon nitride capping dielectric structure.

12. The method of claim 10, wherein high density plasma depositing the capping dielectric structure comprises high density plasma depositing a silicon carbide capping dielectric structure.

13. The method of claim 10, wherein high density plasma depositing the capping dielectric structure comprises high density plasma depositing the capping dielectric structure at a temperature between about 300 °C and 600°C.

14. The method of claim 10, wherein forming the gate electrode comprises forming a non-planar gate electrode.

15. A method comprising:

forming a sacrificial non-planar transistor gate over a non-planar transistor fin;

depositing a dielectric material layer over the sacrificial non-planar transistor gate and the non-planar transistor fin;

forming non-planar transistor gate spacers from a portion of the dielectric material layer adjacent the sacrificial non-planar transistor gate;

forming a source/drain region;

removing the sacrificial non-planar transistor gate to form a gate trench between the non-planar transistor gate spacers and expose a portion of the non-planar transistor fin;

forming a gate dielectric adjacent the non-planar transistor fin within the gate trench;

depositing conductive gate material within the gate trench;

removing a portion of the conductive gate material to form a recess between the non-planar transistor gate spacers;

forming a capping dielectric structure within the recess by high density plasma depositing a dielectric material;

forming at least one dielectric material over the source/drain region, the non-planar transistor gate spacers, and the capping dielectric structure; and

forming a contact opening through the at least one dielectric material to expose at least a portion of the source/drain region.

16. The method of claim 15, wherein high density plasma depositing the capping dielectric structure comprises high density plasma depositing a silicon nitride capping dielectric structure.

17. The method of claim 15, wherein high density plasma depositing the capping dielectric structure comprises high density plasma depositing a silicon carbide capping dielectric structure.

18. The method of claim 15, wherein high density plasma depositing the capping dielectric structure comprises high density plasma depositing the capping dielectric structure at a temperature between about 300 °C and 600°C.

19. The method of claim 15, wherein forming a capping dielectric structure comprises:

high density plasma depositing capping dielectric material within the recess; and

removing excess capping dielectric material.

20. The method of claim 15, wherein forming a contact opening through the dielectric material to expose at least a portion of the source/drain region further comprises forming a contact opening through the dielectric material which exposes at least a portion of the source/drain region and at least a portion of one non-planar transistor gate spacer.

21. The method of claim 20, further comprising forming a source/drain contact to abut the exposed portion of the source/drain region and exposed portion of the non-planar transistor gate spacer.

22. The method of claim 15, wherein forming a contact opening through the dielectric material to expose at least a portion of the source/drain region further comprises forming a contact opening through the dielectric material which exposes at least a portion of the source/drain region and at least a portion of the capping dielectric structure.

23. The method of claim 22, further comprising forming a source/drain contact abuts the exposed portion of the source/drain region and the exposed portion of the capping dielectric structure.

24. The method of claim 15, wherein forming a contact opening through the dielectric material to expose at least a portion of the source/drain region further comprises forming a contact opening through the dielectric material exposes at least a portion of the source/drain region, at least a portion of the non-planar transistor gate spacer, and at least a portion of the capping dielectric structure.

25. The method of claim 24, further comprising forming a source/drain contact to abut the exposed portion of the source/drain region, the exposed portion of non-planar gate spacer, and the exposed portion of the capping dielectric structure.

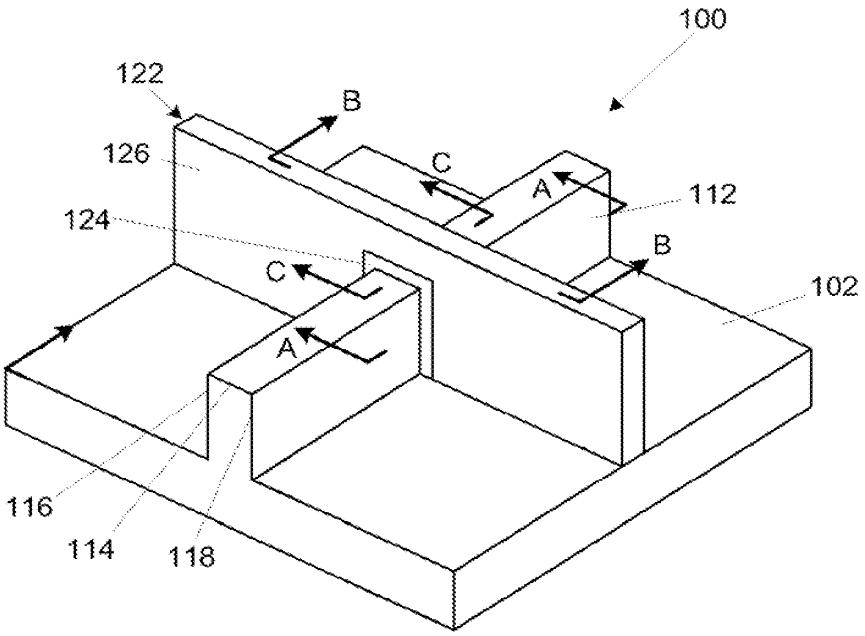


FIG. 1

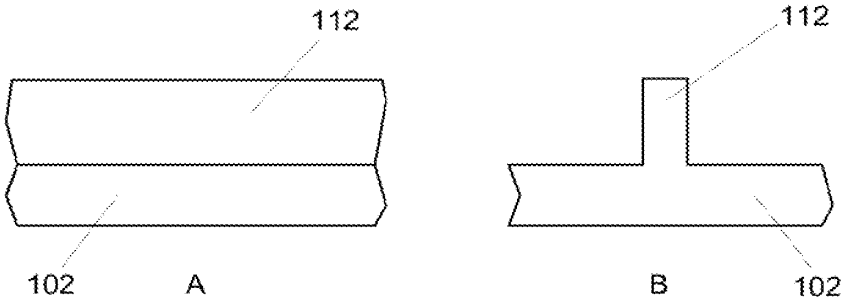


FIG. 2

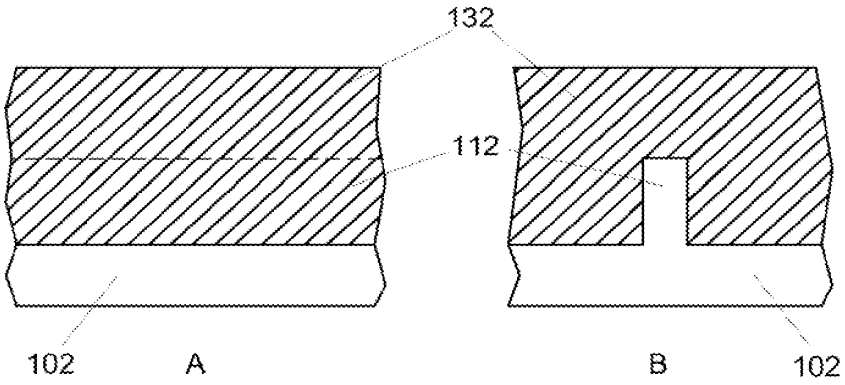


FIG. 3

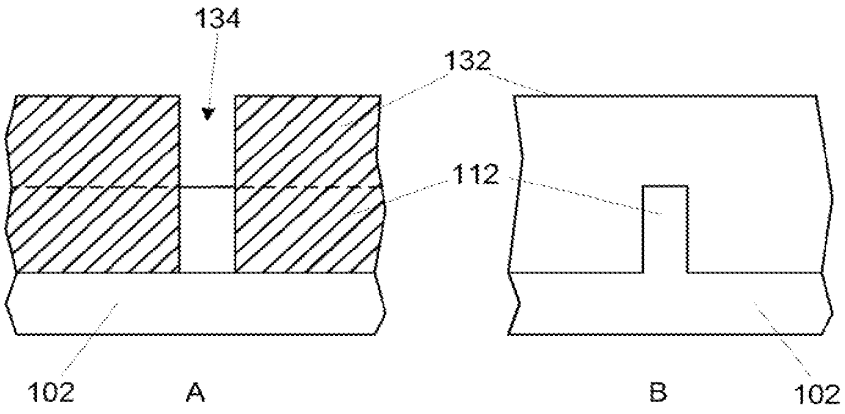


FIG. 4

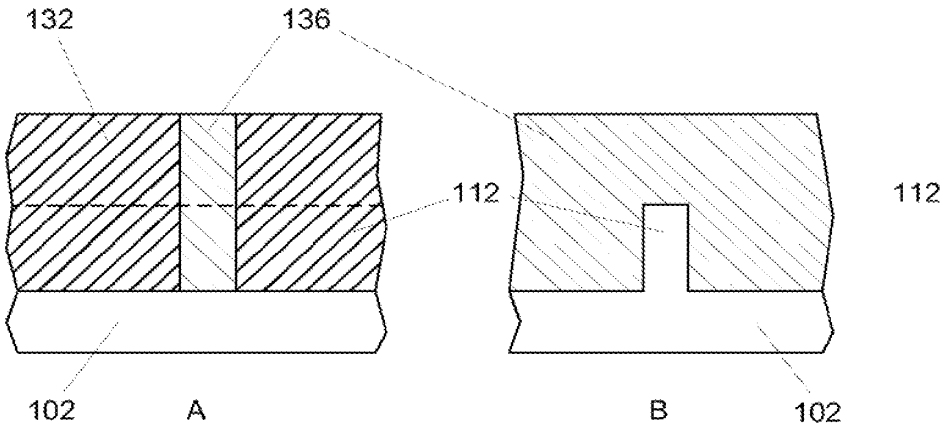


FIG. 5

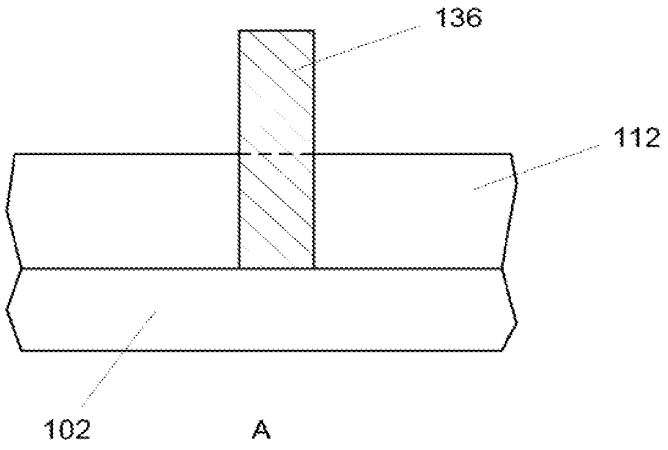


FIG. 6

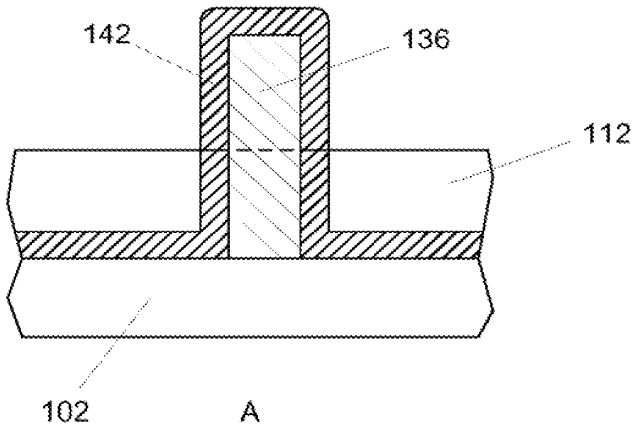


FIG. 7

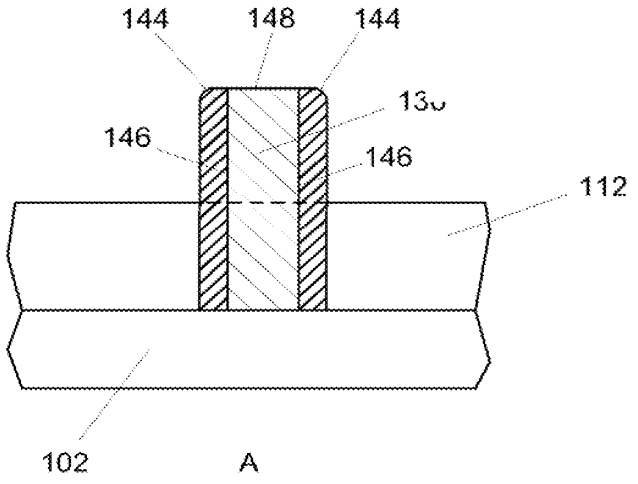


FIG. 8

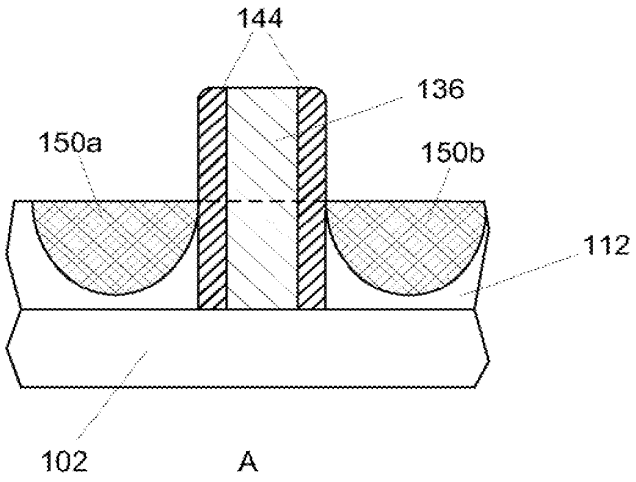


FIG. 9

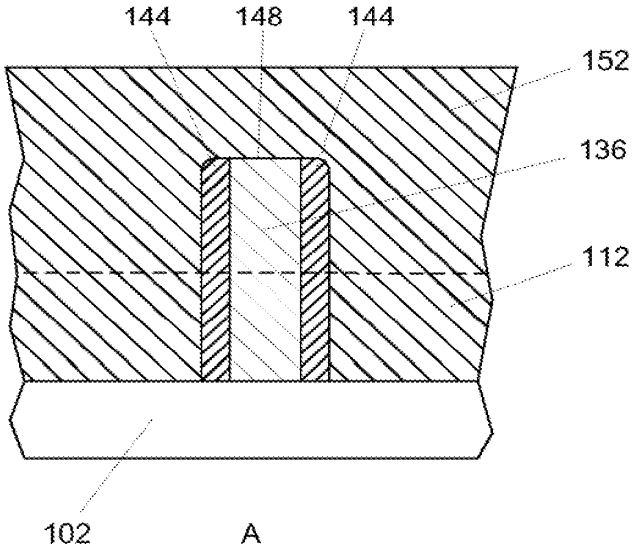


FIG. 10

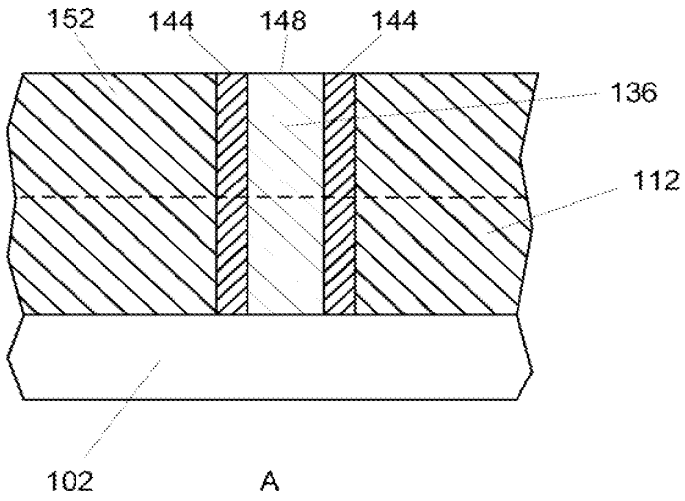


FIG. 11

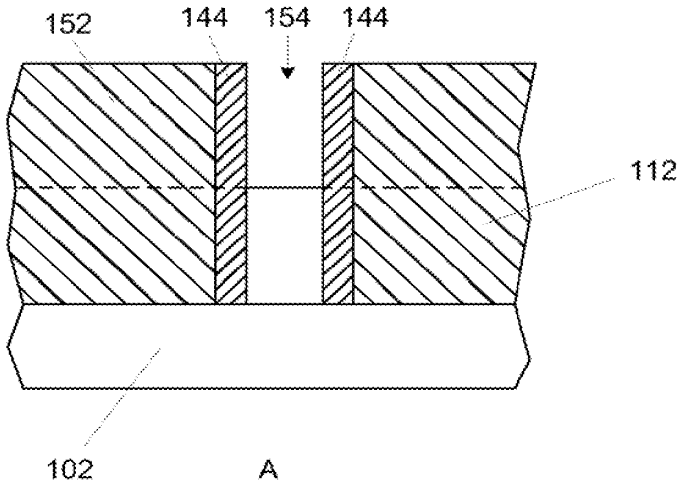


FIG. 12

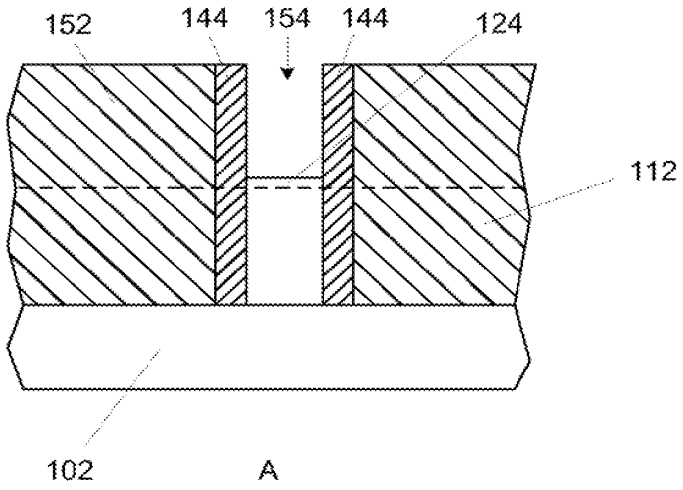


FIG. 13

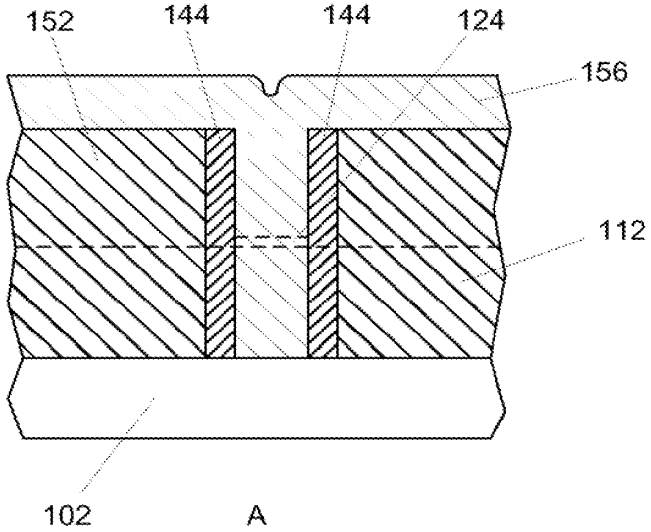


FIG. 14

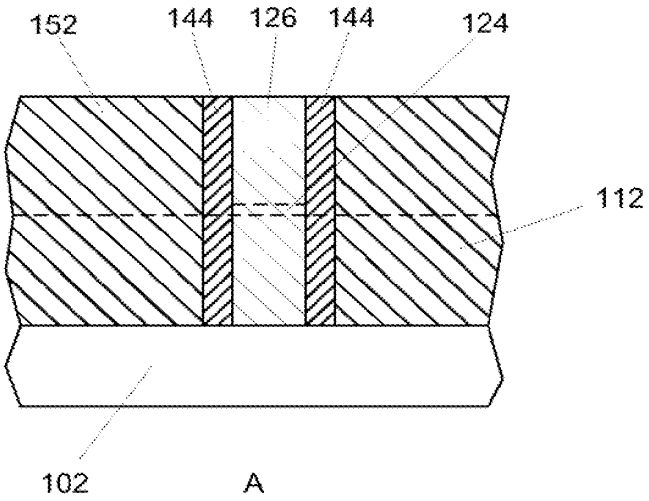

152
144
126
144
124
112
102
A

FIG. 15

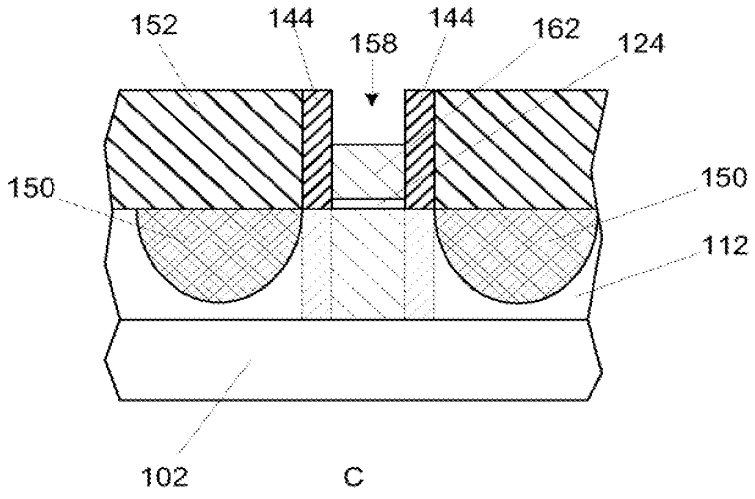

152
144
158
144
162
124
150
150
112
102
C

FIG. 16

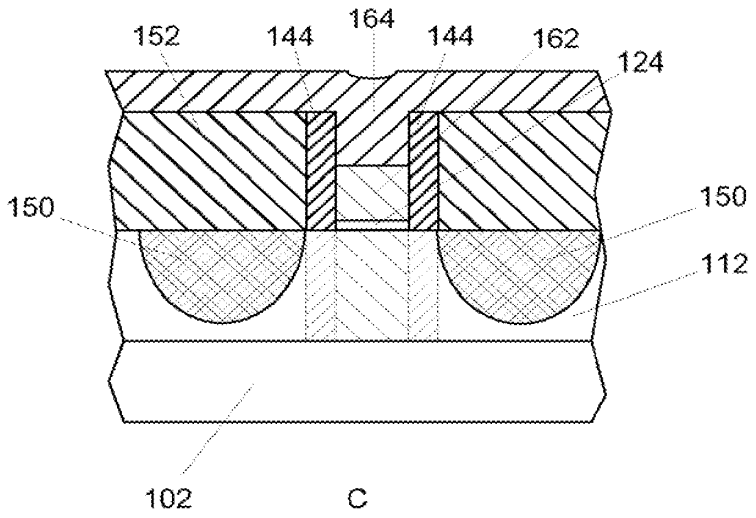

152
144
164
144
162
124
150
150
112
102
C

FIG. 17

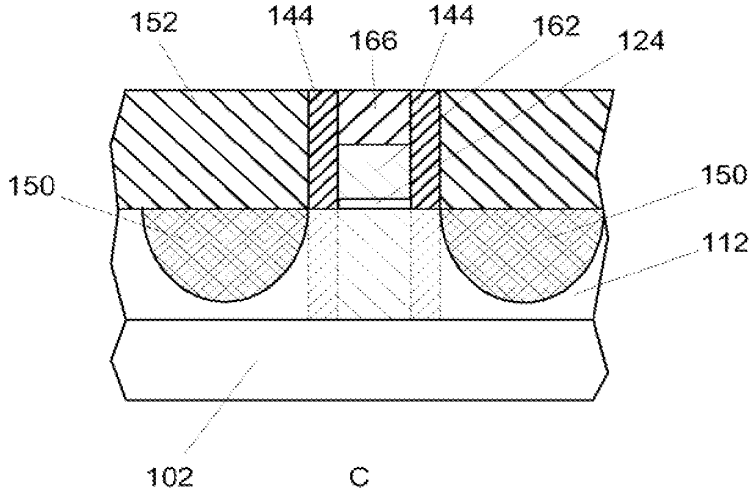

152
144
166
144
162
124
150
150
112
102
C

FIG. 19

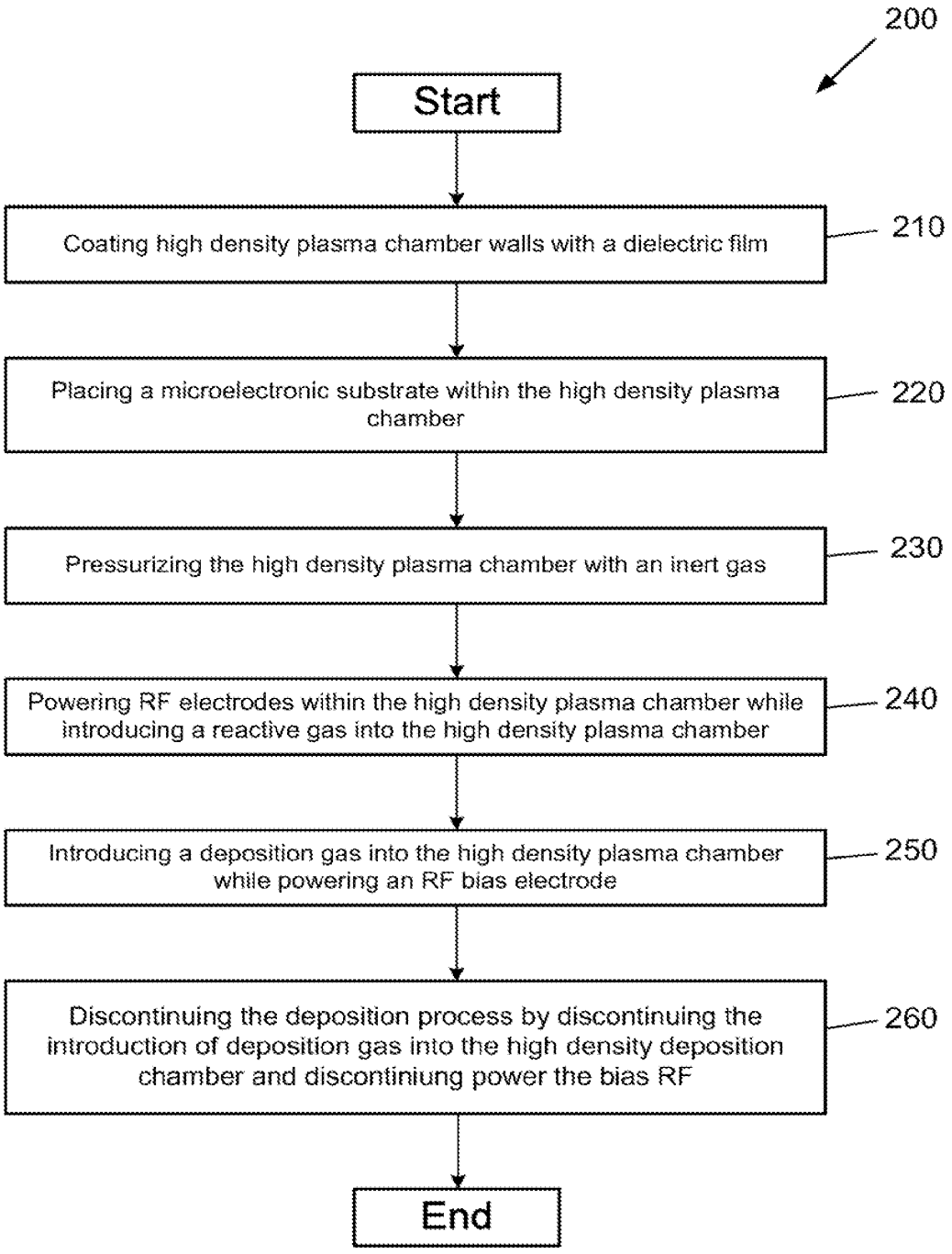

200
Start
Coating high density plasma chamber walls with a dielectric film
210
Placing a microelectronic substrate within the high density plasma chamber
220
Pressurizing the high density plasma chamber with an inert gas
230
Powering RF electrodes within the high density plasma chamber while introducing a reactive gas into the high density plasma chamber
240
Introducing a deposition gas into the high density plasma chamber while powering an RF bias electrode
250
Discontinuing the deposition process by discontinuing the introduction of deposition gas into the high density deposition chamber and discontiniung power the bias RF
260
End

FIG. 18

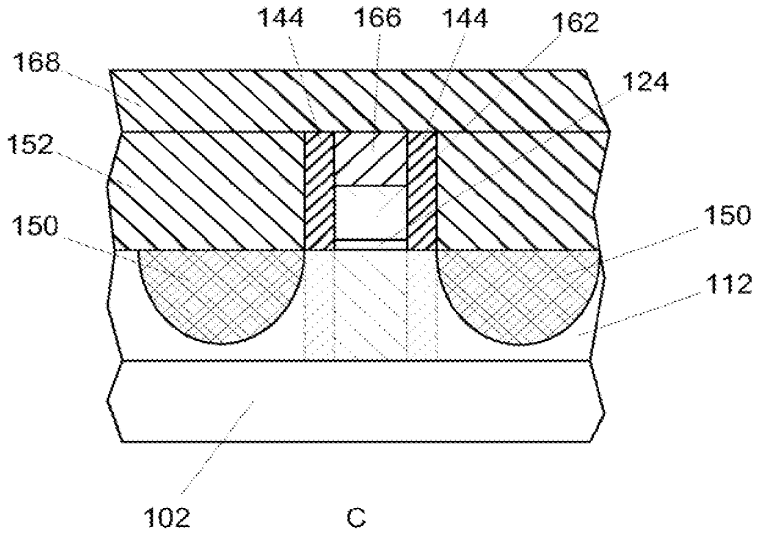

144
166
144
162
168
124
152
150
150
112
102
C

FIG. 20

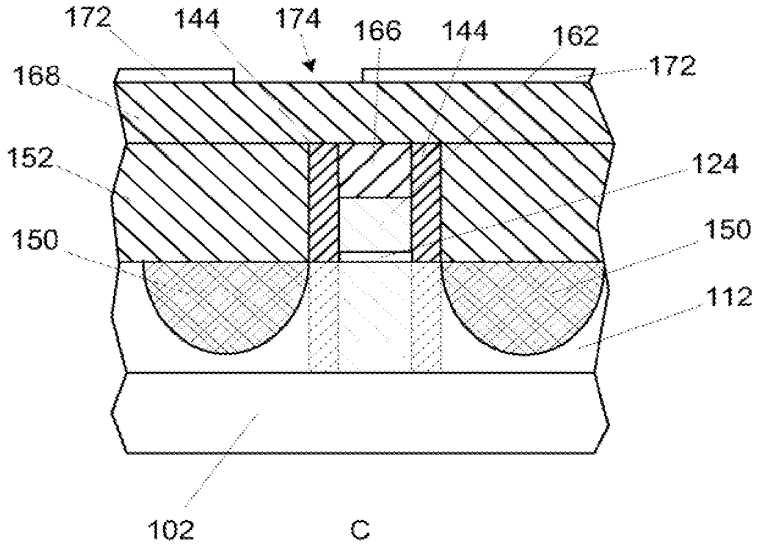

172
144
174
166
144
162
168
172
152
124
150
150
112
102
C

FIG. 21

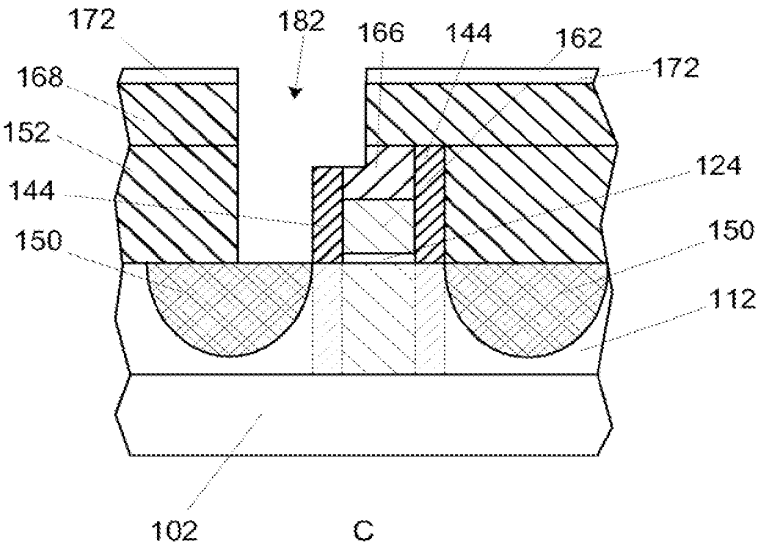

172
182
166
144
162
168
172
152
124
144
150
150
112
102
C

FIG. 22

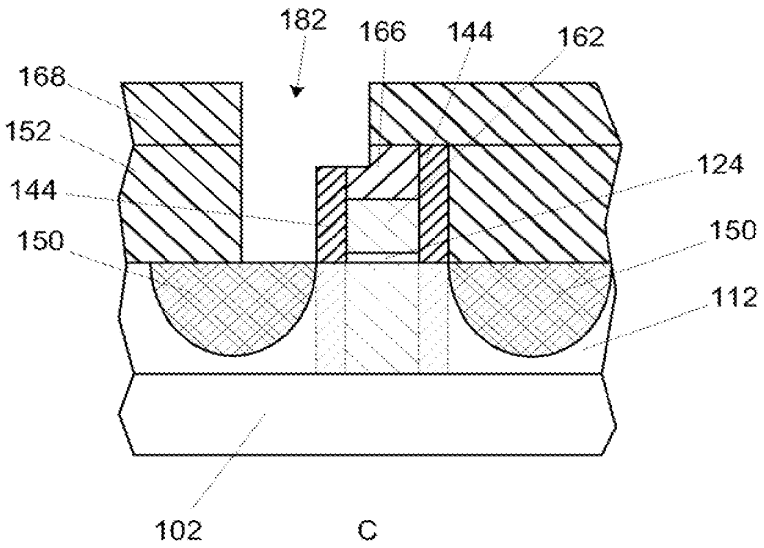

182
166
144
162
168
152
124
144
150
150
112
102
C

FIG. 23

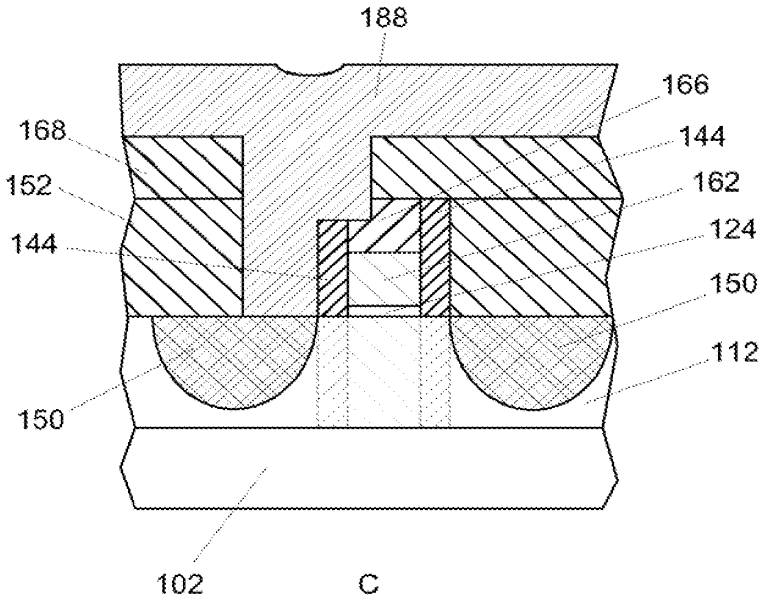

188
166
168
144
152
162
144
124
150
112
150
102
C

FIG. 24

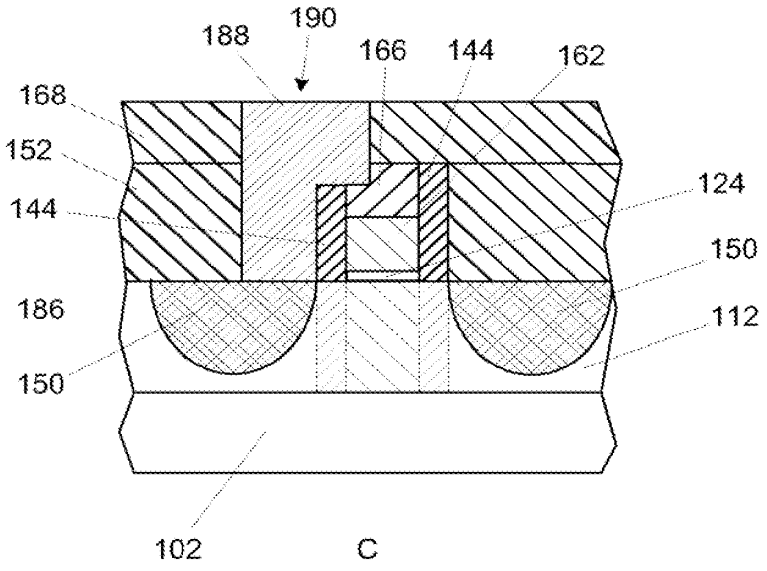

188
190
166
144
162
168
152
124
144
150
186
112
150
102
C

FIG. 25

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2011/054464

A. CLASSIFICATION OF SUBJECT MATTER

H01L 29/78(2006.01)i, H01L 21/336(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 29/78; H01L 21/336; H01L 21/306; H01L 21/28; H01L 21/335

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: capping, dielectric, and transistor

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2008-0223309 A1 (BOOTH ROGER ALLEN et al.) 25 September 2008 See the abstract; figs. 1-11; paragraphs [0016]-[0026].	1-25
A	US 2010-0048007 A1 (LEE SHEN-NAN et al.) 25 February 2010 See the abstract; figs. 1-3; paragraphs [0011]-[0039].	1-25
A	KR 10-0653711 B1 (SAMSUNG ELECTRONICS CO., LTD.) 05 December 2006 See the abstract; figs. 1-12; claims 1-23.	1-25

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15 MAY 2012 (15.05.2012)	**15 MAY 2012 (15.05.2012)**

Name and mailing address of the ISA/KR	Authorized officer
Korean Intellectual Property Office Government Complex-Daejeon, 189 Cheongsa-ro, Seo-gu, Daejeon 302-701, Republic of Korea	Lee,Sang Ho
Facsimile No. 82-42-472-7140	Telephone No. 82-42-481-8221

Form PCT/ISA/210 (second sheet) (July 2009)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2011/054464

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2008-0233699 A1	25.09.2008	CN 101097956 A	02.01.2008
		CN 101097956 C0	02.01.2008
		JP 2008-010876 A	17.01.2008
		TW 200807717 A	01.02.2008
		US 2008-0001187 A1	03.01.2008
		US 2008-0042219 A1	21.02.2008
		US 2008-0142891 A1	19.06.2008
		US 7517764 B2	14.04.2009
		US 7667248 B2	23.02.2010
		US 7863122 B2	04.01.2011
US 2010-0048007 A1	25.02.2010	CN 101659034 A	03.03.2010
		CN 101659034 B	09.11.2011
		TW 201009925 A	01.03.2010
		US 8153526 B2	10.04.2012
KR 10-0653711 B1	05.12.2006	US 2007-0111435 A1	17.05.2007
		US 2010-0197099 A1	05.08.2010
		US 7723762 B2	25.05.2010
		US 7851287 B2	14.12.2010

Form PCT/ISA/210 (patent family annex) (July 2009)

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
4 April 2013 (04.04.2013)

WIPO | PCT

(10) International Publication Number
WO 2013/048524 A1

(51) International Patent Classification:
H01L 29/78 (2006.01) *H01L 21/336* (2006.01)

(21) International Application Number:
PCT/US2011/054479

(22) International Filing Date:
1 October 2011 (01.10.2011)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant *(for all designated States except US)*: **INTEL CORPORATION** [US/US]; 2200 Mission College Boulevard, Santa Clara, California 95052 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **PRADHAN, Sameer S.** [IN/US]; 17923 NW Sylvania Lane, Portland, Oregon 97229 (US). **JOSHI, Subhash, M.** [IN/US]; 496 NE 61st Way, Hillsboro, Oregon 97124 (US). **CHUN, Jin-Sung** [US/US]; 12852 NW Bayonne Ln., Portland, Oregon 97229 (US).

(74) Agents: **DRAEGER, Jeffrey, S.** et al.; Winkle, PLLC, c/o CPA GLOBAL, P.O. Box 52050, Minneapolis, Minnesota 55402 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *as to the identity of the inventor (Rule 4.17(i))*

[Continued on next page]

(54) Title: SOURCE/DRAIN CONTACTS FOR NON-PLANAR TRANSISTORS

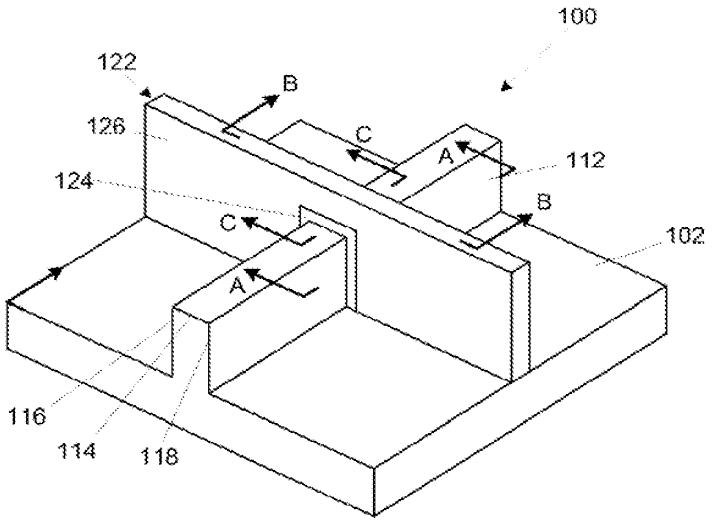


FIG. 1

(57) Abstract: The present description relates to the field of fabricating microelectronic devices having non-planar transistors. Embodiments of the present description relate to the formation of source/drain contacts within non-planar transistors, wherein a titanium-containing contact interface may be used in the formation of the source/drain contact with a discreet titanium silicide formed between the titanium-containing interface and a silicon-containing source/drain structure.

WO 2013/048524 A1

Published:

— *with international search report (Art. 21(3))*

SOURCE/DRAIN CONTACTS FOR NON-PLANAR TRANSISTORS

BACKGROUND

Embodiments of the present description generally relate to the field of microelectronic device fabrication and, more particularly, to the fabrication of source/drain contacts within non-planar transistors.

BRIEF DESCRIPTION OF THE DRAWINGS

The subject matter of the present disclosure is particularly pointed out and distinctly claimed in the concluding portion of the specification. The foregoing and other features of the present disclosure will become more fully apparent from the following description and appended claims, taken in conjunction with the accompanying drawings. It is understood that the accompanying drawings depict only several embodiments in accordance with the present disclosure and are, therefore, not to be considered limiting of its scope. The disclosure will be described with additional specificity and detail through use of the accompanying drawings, such that the advantages of the present disclosure can be more readily ascertained, in which:

FIG. 1 is a perspective view of a non-planar transistor, according to an embodiment of the present description.

FIG. 2 illustrates a side cross-sectional view of a non-planar transistor fin formed in or on a microelectronic substrate.

FIG. 3 illustrates a side cross-sectional view of a sacrificial material deposited over the non-planar transistor fin of FIG. 2, according to an embodiment of the present description.

FIG. 4 illustrates a side cross-sectional view of a trench formed in the sacrificial material deposited to expose a portion of the non-planar transistor fin of FIG. 3, according to an embodiment of the present description.

FIG. 5 illustrates a side cross-sectional view of a sacrificial gate formed in the trench of FIG. 4, according to an embodiment of the present description.

FIG. 6 illustrates a side cross-sectional view of the sacrificial gate after the removal of the sacrificial material of FIG. 5, according to an embodiment of the present description.

FIG. 7 illustrates a side cross-sectional view of a conformal dielectric layer deposited over the sacrificial gate and microelectronic substrate of FIG. 6, according to an embodiment of the present description.

FIG. 8 illustrates a side cross-sectional view of gate spacers formed from the conformal dielectric layer of FIG. 7, according to an embodiment of the present description.

FIG. 9 illustrates a side cross-sectional view of a source region and a drain region formed in the non-planar transistor fin on either side of the gate spacers of FIG. 8, according to an embodiment of the present description.

FIG. 10 illustrates a side cross-sectional view of a first dielectric material deposited over the gate spacers, the sacrificial gate, the non-planar transistor fin, and the microelectronic substrate of FIG. 9, according to an embodiment of the present description.

FIG. 11 illustrates a side cross-sectional view of the structure of FIG. 10 after planarizing the first dielectric material to expose a top surface of the sacrificial gate, according to an embodiment of the present description.

FIG. 12 illustrates a side cross-sectional view of the structure of FIG. 11 after the removal of the sacrificial gate to form a gate trench, according to an embodiment of the present description.

FIG. 13 illustrates a side cross-sectional view of the structure of FIG. 12 after the formation of a gate dielectric adjacent the non-planar transistor fin between the gate spacers, according to an embodiment of the present description.

FIG. 14 illustrates a side cross-sectional view of a conductive gate material deposited in the gate trench of FIG. 13, according to an embodiment of the present description.

FIG. 15 illustrates a side cross-sectional view of the structure of FIG. 14 after the removal of excess conductive gate material to form a non-planar transistor gate, according to an embodiment of the present description.

FIG. 16 illustrates a side cross-sectional view of the structure of FIG. 15 after etching away a portion of the non-planar transistor gate to form a recessed non-planar transistor gate, according to an embodiment of the present description.

FIG. 17 illustrates a side cross-sectional view of the structure of FIG. 16 after depositing a capping dielectric material into the recess resulting from the formation of the recessed non-planar transistor gate, according to an embodiment of the present description.

FIG. 18 illustrates a side cross-sectional view of the structure of FIG. 17 after the removal of excess capping dielectric material to form a capping structure on the non-planar transistor gate, according to an embodiment of the present description.

FIG. 19 illustrates a side cross-sectional view of a second dielectric material deposited over the first dielectric material layer, the gate spacers, and the sacrificial gate top surface of FIG. 18, according to an embodiment of the present description.

FIG. 20 illustrates a side cross-sectional view of an etch mask patterned on the second dielectric material of FIG. 19, according to an embodiment of the present description.

FIG. 21 illustrates a side cross-sectional view of a contact opening formed through the first and second dielectric material layer of FIG. 20, according to an embodiment of the present description.

FIG. 22 illustrates a side cross-sectional view of the structure of FIG. 21 after the removal of the etch mask, according to an embodiment of the present description.

FIG. 23 illustrates a side cross-sectional view of a titanium-containing contact interface layer formed in the contact opening of FIG. 22, according to an embodiment of the present description.

FIG. 24 illustrates a side cross-sectional view of a titanium silicide interface discretely formed between the titanium-containing contact interface layer and the source/drain region which has been formed in the non-planar transistor fin, according to an embodiment of the present description.

FIG. 25 illustrates a side cross-sectional view of a conductive contact material deposited in the contact opening of FIG. 24, according to an embodiment of the present description.

FIG. 26 illustrates a side cross-sectional view of the structure of FIG. 25 after the removal of the excess conductive contact material to form a source/drain contact, according to an embodiment of the present description.

DETAILED DESCRIPTION

In the following detailed description, reference is made to the accompanying drawings that show, by way of illustration, specific embodiments in which the claimed subject matter may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the subject matter. It is to be understood that the various embodiments, although different, are not necessarily mutually exclusive. For example, a particular feature, structure, or characteristic described herein, in connection with one embodiment, may be implemented within other embodiments without departing from the spirit and scope of the claimed subject matter. References within this specification to "one embodiment" or "an embodiment" mean that a particular feature,

structure, or characteristic described in connection with the embodiment is included in at least one implementation encompassed within the present invention. Therefore, the use of the phrase "one embodiment" or "in an embodiment" does not necessarily refer to the same embodiment. In addition, it is to be understood that the location or arrangement of individual elements within each disclosed embodiment may be modified without departing from the spirit and scope of the claimed subject matter. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the subject matter is defined only by the appended claims, appropriately interpreted, along with the full range of equivalents to which the appended claims are entitled. In the drawings, like numerals refer to the same or similar elements or functionality throughout the several views, and that elements depicted therein are not necessarily to scale with one another, rather individual elements may be enlarged or reduced in order to more easily comprehend the elements in the context of the present description.

In the fabrication of non-planar transistors, such as tri-gate transistors and FinFETs, non-planar semiconductor bodies may be used to form transistors capable of full depletion with very small gate lengths (e.g., less than about 30 nm). These semiconductor bodies are generally fin-shaped and are, thus, generally referred to as transistor "fins". For example in a tri-gate transistor, the transistor fins have a top surface and two opposing sidewalls formed on a bulk semiconductor substrate or a silicon-on-insulator substrate. A gate dielectric may be formed on the top surface and sidewalls of the semiconductor body and a gate electrode may be formed over the gate dielectric on the top surface of the semiconductor body and adjacent to the gate dielectric on the sidewalls of the semiconductor body. Thus, since the gate dielectric and the gate electrode are adjacent to three surfaces of the semiconductor body, three separate channels and gates are formed. As there are three separate channels formed, the semiconductor body can be fully depleted when the transistor is turned on. With regard to finFET transistors, the gate material and the electrode only contact the sidewalls of the semiconductor body, such that two separate channels are formed (rather than three in tri-gate transistors).

Embodiments of the present description relate to the formation of source/drain contacts within non-planar transistors, wherein a titanium-containing contact interface may be used in the formation of the source/drain contact with a discreet titanium silicide formed between the titanium-containing interface and a silicon-containing source/drain structure.

FIG. 1 is a perspective view of a non-planar transistor 100, including at least one gate formed on at least one transistor fin, which are formed on a microelectronic substrate 102. In an embodiment of the present disclosure, the microelectronic substrate 102 may be a monocrystalline silicon substrate. The microelectronic substrate 102 may also be other types of substrates, such as silicon-on-insulator ("SOI"), germanium, gallium arsenide, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, gallium antimonide, and the like, any of which may be combined with silicon.

The non-planar transistor, shown as a tri-gate transistor, may include at least one non-planar transistor fin 112. The non-planar transistor fin 112 may have a top surface 114 and a pair of laterally opposite sidewalls, sidewall 116 and opposing sidewall 118, respectively.

As further shown in FIG. 1, at least one non-planar transistor gate 122 may be formed over the non-planar transistor fin 112. The non-planar transistor gate 122 may be fabricated by forming a gate dielectric layer 124 on or adjacent to the non-planar transistor fin top surface 114 and on or adjacent to the non-planar transistor fin sidewall 116 and the opposing non-planar transistor fin sidewall 118. A gate electrode 126 may be formed on or adjacent the gate dielectric layer 124. In one embodiment of the present disclosure, the non-planar transistor fin 112 may run in a direction substantially perpendicular to the non-planar transistor gate 122.

The gate dielectric layer 124 may be formed from any well-known gate dielectric material, including but not limited to silicon dioxide (SiO_2), silicon oxynitride (SiO_xN_y), silicon nitride (Si_3N_4), and high-k dielectric materials such as hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate. The gate dielectric layer 124 can be formed by well-known techniques, such as by conformally depositing a gate dielectric material and then patterning the gate dielectric material with well-known photolithography and etching techniques, as will be understood to those skilled in the art.

The gate electrode 126 can be formed of any suitable gate electrode material. In an embodiment of the present disclosure, the gate electrode 126 may be formed from materials that include, but are not limited to, polysilicon, tungsten, ruthenium, palladium, platinum, cobalt, nickel, hafnium, zirconium, titanium, tantalum, aluminum, titanium carbide, zirconium carbide, tantalum carbide, hafnium carbide, aluminum carbide, other

metal carbides, metal nitrides, and metal oxides. The gate electrode 126 can be formed by well-known techniques, such as by blanket depositing a gate electrode material and then patterning the gate electrode material with well-known photolithography and etching techniques, as will be understood to those skilled in the art.

A source region and a drain region (not shown in FIG. 1) may be formed in the non-planar transistor fin 112 on opposite sides of the gate electrode 126. In one embodiment, the source and drain regions may be formed by doping the non-planar transistor fins 112, as will be understood to those skilled in the art. In another embodiment, the source and drain regions may be formed by removing potions of the non-planar transistor fins 112 and replacing these portions with appropriate material(s) to form the source and drain regions, as will be understood to those skilled in the art.

FIGs. 2-26 illustrate side cross-sectional view of one embodiment of fabricating a non-planar transistor, wherein FIGs. 2-5 are views along arrows A-A and B-B of FIG. 1, FIGs. 6-15 are views along arrows A-A of FIG. 1, and FIG. 16-26 are views along arrows C-C of FIG. 1.

As shown in FIG. 2, the non-planar transistor fin 112 may be formed by etching the microelectronic substrate 102 or by forming the non-planar transistor fin 112 on the microelectronic substrate 102 by any technique known in the art. As illustrate in FIG. 3, a sacrificial material 132 may be deposited over the non-planar transistor fin 112, as shown in FIG. 3, and a trench 134 may be formed in the sacrificial material 132 to expose a potion of the non-planar transistor fin 112, as shown in FIG. 4. The sacrificial material 132 may be any appropriate material known in the art, and the trench 134 may be formed by any technique known in the art, including but not limited to lithographic masking and etching.

As shown in FIG. 5, a sacrificial gate 136 may be formed in the trench 134 (see FIG. 4). The sacrificial gate 136 may be any appropriate material, such as a polysilicon material and the like, and may be deposited in the trench 134 (see FIG. 4) by any technique known in the art, including but not limited to chemical vapor deposition ("CVD") and physical vapor deposition ("PVD").

As shown in FIG. 6, the sacrificial material 132 of FIG. 5 may be removed to expose the sacrificial gate 136 by any technique known in the art, such as selectively etching the sacrificial material 132. As shown in FIG. 7, a conformal dielectric layer 142 may be deposited over the sacrificial gate 136 and microelectronic substrate 102. The conformal dielectric layer 142 may be any appropriate material, including but not limited

to silicon nitride (Si_3N_4) and silicon carbide (SiC), and may be formed by any appropriate technique including but not limited to atomic layer deposition ("ALD").

As shown in FIG. 8, the conformal dielectric layer 142 of FIG. 7 may be etched, such as by directional etch with an appropriate etchant, to form gate spacers 144 on sidewalls 146 of the sacrificial gate 136, while substantially removing the conformal dielectric material layer 142 adjacent the microelectronic substrate 102 and a top surface 148 of the sacrificial gate 136. It is understood that fin spacers (not shown) may be simultaneously formed on sidewalls 116 and 118 (see FIG. 1) of the non-planar transistor fin 112 during the formation of the gate spacers 144.

As shown in FIG. 9, a silicon-containing source region 150a and a silicon-containing drain region 150b may be formed on either side of the gate spacers 144. In one embodiment, the silicon-containing source region 150a and the silicon-containing drain region 150b may be formed in the non-planar transistor fin 112 with the implantation of dopants. As will be understood to those skilled in that art, dopant implantation is a process of introducing impurities into semiconducting materials for the purpose changing its conductivity and electronic properties. This is generally achieved by ion implantation of either P-type ions (e.g.boron) or N-type ions (e.g. phosphorus), collectively referred to as "dopants". In another embodiment, portions of the non-planar transistor fin 112 may be removed by any technique known in the art, such as etching, and the silicon-containing source region 150a and a silicon-containing drain region 150b may be formed in place of the removed portions. The silicon-containing source region 150a and the silicon-containing drain region will hereinafter be referred to collectively as "silicon-containing source/drain region 150".

As shown in FIG. 10, a first dielectric material layer 152 may be deposited over the gate spacers 144, the sacrificial gate top surface 148, the non-planar transistor fin 112, and the microelectronic substrate 102. The first dielectric material layer 152 may be planarizing to expose the sacrificial gate top surface 148, as shown in FIG. 11. The planarization of the first dielectric material layer 152 may be achieved by any technique known in the art, including but not limited to chemical mechanical polishing (CMP).

As shown in FIG. 12, the sacrificial gate 136 of FIG. 11 may be removed to form a gate trench 154. The sacrificial gate 136 may be removed by any technique known in the art, such as a selective etch. As shown in FIG. 13, the gate dielectric layer 124, as also illustrated in FIG. 1, may be formed to abut the non-planar transistor fin 112, as previously discussed.

As shown in FIG. 14, a conductive gate material 156 may be deposited in the gate trench 154, and excess conductive gate material 156 (e.g. conductive gate material 156 not within the gate trench 154 of FIG. 12) may be removed to from the non-planar transistor gate electrode 126 (see also FIG. 1), as shown in FIG. 15. The materials and methods of forming the gate electrode 126 have been previously discussed. The removal of the excess conductive gate material 156 may be achieved by any technique known in the art, including but not limited to chemical mechanical polishing (CMP), etching, and the like.

As shown in FIG. 16, a portion of the non-planar transistor gate electrode 126 may be removed to form a recess 158 and a recessed non-planar transistor gate 162. The removal may be accomplished by any known technique, including but not limited to wet or dry etching. As shown in FIG. 17, a capping dielectric material 164 may be deposited to fill the recess 158 of FIG. 16. The capping dielectric material 164 may be any appropriate material, including but not limited to silicon nitride (Si_3N_4) and silicon carbide (SiC), and may be formed by any appropriate deposition technique. The capping dielectric material 164 may be planarized to remove excess capping dielectric material 164 (e.g. capping dielectric material 164 not within the recess of FIG. 16) to from a capping structure 166 on the recessed non-planar transistor gate 162 and between a gate spacers 144, as shown in FIG. 18. The removal of the excess capping dielectric material 164 may be achieved by any technique known in the art, including but not limited to chemical mechanical polishing (CMP), etching, and the like.

As shown in FIG. 19, a second dielectric material layer 168 may be deposited over the first dielectric material layer 152, the gate spacers 144, and the capping structure 166. The second dielectric material layer 168 may be formed from any appropriate dielectric material, including but not limited to silicon dioxide (SiO_2), silicon oxynitride (SiO_xN_y), and silicon nitride (Si_3N_4), by any known deposition technique. As shown in FIG. 20, an etch mask 172 may be patterned with at least one opening 174 on the second dielectric material layer 168, such as by well known lithographic techniques.

As shown in FIG. 21, a contact opening 182 may be formed through the first dielectric material layer 152 and the second dielectric material layer 168 by etching through the etch mask opening 174 of FIG. 20 to expose a portion of the source/drain region 150. The etch mask 172 of FIG. 21 may be removed thereafter, as shown in FIG. 22. In one embodiment, the first dielectric material layer 152 and the dielectric material layer 168 differs from dielectric material of both the gate spacers 144 and the capping structure 166, such that the etching of the first dielectric material layer 152 and

the second dielectric layer 168 may be selective to the gate spacers 144 and the capping structure 166 (i.e. etches faster). This is known in the art as a self-aligning.

As shown in FIG. 23, a titanium-containing contact interface layer 184 may be conformally deposited in the contact opening 182 to abut the exposed portion of the source/drain region 150, wherein the titanium-containing contact interface layer 184 acts as the primary work-function metal, as will be understood to those skilled in the art. In one embodiment, the titanium-containing contact interface layer 184 comprises substantially pure titanium. The titanium-containing contact interface layer 184 may be formed by atomic layer deposition.

As shown in FIG. 24, a titanium silicide interface 186 may be discretely formed between the silicon-containing source/drain region 150 and the titanium-containing contact interface layer 184, such as by heating the structure of FIG. 23. The term "discretely" is defined to mean that titanium silicide is formed substantially only between the titanium-containing contact interface layer 184 and the silicon-containing source/drain region 150. The formation of the titanium silicide interface 186 may result in a low resistive contact, as will be understood to those skilled in the art.

As shown in FIG. 25, a conductive contact material 188 may be deposited in the contact opening 182 of FIG. 24 to reside approximate the titanium-containing contact interface layer 184. In one embodiment, the conductive contact material 188 may be a tungsten-containing conductive material. In another embodiment, the conductive contact material 188 may be substantially pure tungsten.

As shown in FIG. 26, excess conductive contact material 188 of FIG. 25 (e.g. conductive contact material 188 not within the contact opening 182 of FIG. 12) to form a source/drain contact 190. The removal of the excess conductive contact material 188 may be achieved by any technique known in the art, including but not limited to chemical mechanical polishing (CMP), etching, and the like.

As previously discussed, in one embodiment, the first dielectric material layer 152 and the dielectric material layer 168 differs from dielectric material of both the gate spacers 144 and the capping structure 166, such that the etching of the first dielectric material layer 152 and the second dielectric layer 168 may be selective to the gate spacers 144 and the capping structure 166 (i.e. etches faster). Thus, the recessed non-planar transistor 162 is protected during the formation of the contact opening 182. This allows for the formation of a relatively large sized source/drain contact 190, which may increase

the transistor drive current performance, without the risk of shorting between the source/drain contact 190 and the recessed non-planar transistor gate 162.

The use of the titanium-containing contact interface layer 184 may eliminate the conventional use of fully silicided nickel-containing contact interface layers, such nickel silicide and platinum nickel silicide. Nickel is a highly mobile element which tends to rapidly diffuse outside of an intended contact area. Such diffusion may result in source/drain shorts, as will be understood to those skilled in the art. Further, the use of the titanium-containing contact interface layer 184 may eliminate the need for a silicide pre-clean step, which may reduce the chance of having shorting between source/drain contact 190 and the recessed non-planar transistor gate 162, as previously discussed, as such a pre-clean step may remove material from the capping structure 166 and/or the gate spacers 144.

It is understood that the subject matter of the present description is not necessarily limited to specific applications illustrated in FIGs. 1-26. The subject matter may be applied to other microelectronic device fabrication applications, as will be understood to those skilled in the art.

Having thus described in detail embodiments of the present invention, it is understood that the invention defined by the appended claims is not to be limited by particular details set forth in the above description, as many apparent variations thereof are possible without departing from the spirit or scope thereof.

CLAIMS

What is claimed is:

1. A microelectronic device, comprising:

a silicon-containing source/drain region;

a source/drain contact adjacent the silicon-containing source/drain region, wherein the source/drain contact comprises a conductive contact material and a titanium-containing contact interface layer disposed between conductive contact material and the silicon-containing source/drain region; and

a titanium silicide interface disposed between the silicon-containing source/drain region and the titanium-containing contact interface layer.

2. The microelectronic device of claim 1, wherein the titanium-containing contact interface layer comprises substantially pure titanium.

3. The microelectronic device of claim 1, wherein the conductive contact material comprises tungsten.

4. The microelectronic device of claim 1, wherein the titanium silicide interface resides substantially only between the silicon-containing source/drain region and the titanium-containing contact interface layer.

5. A microelectronic device, comprising:

a non-planar transistor gate over a non-planar transistor fin, wherein the non-planar transistor gate comprises a gate electrode recessed between gate spacers and a capping structure disposed on the recessed gate electrode between the gate spacers,

a silicon-containing source/drain region;

at least one dielectric material layer over the source/drain region, the non-planar transistor gate spacers, and the capping structure;

a source/drain contact extending through a portion of the at least one dielectric material layer and comprising a conductive contact material and a titanium-containing contact interface layer disposed between conductive contact material and the silicon-containing source/drain region; and

a titanium silicide interface disposed between the silicon-containing source/drain region and the titanium-containing contact interface layer.

6. The microelectronic device of claim 5, wherein the titanium-containing contact interface layer comprises substantially pure titanium.

7. The microelectronic device of claim 5, wherein the conductive contact material comprises tungsten.

8. The microelectronic device of claim 5, wherein the titanium silicide interface resides substantially only between the silicon-containing source/drain region and the titanium-containing contact interface layer.

9. The microelectronic device of claim 5, wherein the titanium-containing contact interface layer abuts at least a portion of one non-planar transistor gate spacer.

10. The microelectronic device of claim 9, wherein the titanium-containing contact interface layer abuts at least a portion of the capping structure.

11. A method of fabricating a microelectronic device, comprising:

forming a silicon-containing source/drain region;

forming a dielectric material over the silicon-containing source/drain region;

forming a contact opening through the dielectric material to expose a portion of the source/drain region;

conformally depositing a titanium-containing contact interface layer within the contact opening to abut the silicon-containing source/drain region;

depositing a conductive contact material within the contact opening to abut the titanium-containing contact interface layer; and

forming a titanium silicide interface between the silicon-containing source/drain region and the titanium-containing contact interface layer.

12. The method of claim 11, wherein conformally depositing the titanium-containing contact interface layer comprises depositing a substantially pure titanium contact interface layer.

13. The method of claim 11, wherein depositing a conductive contact material within the contact opening comprises depositing tungsten within the contact opening.

14. The method of claim 11, wherein forming the titanium silicide interface between the silicon-containing source/drain region and the titanium-containing contact interface layer comprises forming the titanium silicide interface between the silicon-containing source/drain region and the titanium-containing contact interface layer by heating the silicon-containing source/drain region and the titanium-containing contact interface layer.

15. The method of claim 11, wherein forming the titanium silicide interface comprises forming the titanium silicide substantially only between the silicon-containing source/drain region and the titanium-containing contact interface layer.

16. A method comprising:

forming a sacrificial non-planar transistor gate over a non-planar transistor fin;

depositing a dielectric material layer over the sacrificial non-planar transistor gate and the non-planar transistor fin;

forming non-planar transistor gate spacers from a portion of the dielectric material layer adjacent the sacrificial non-planar transistor gate;

forming a source/drain region;

removing the sacrificial non-planar transistor gate to form a gate trench between the non-planar transistor gate spacers and expose a portion of the non-planar transistor fin;

forming a gate dielectric adjacent the non-planar transistor fin within the gate trench;

depositing conductive gate material within the gate trench

forming a capping structure within the recess;

forming at least one dielectric material over the source/drain region, the non-planar transistor gate spacers, and the capping structure;

forming a contact opening through the at least one dielectric material to expose at least a portion of the source/drain region;

conformally depositing a titanium-containing contact interface layer within the contact opening to abut the silicon-containing source/drain region;

depositing a conductive contact material within the contact opening to abut the titanium-containing contact interface layer; and

forming a titanium silicide interface between the silicon-containing source/drain region and the titanium-containing contact interface layer.

17. The method of claim 16, wherein conformally depositing the titanium-containing contact interface layer comprises conformally depositing a substantially pure titanium contact interface layer.

18. The method of claim 16, wherein depositing a conductive contact material within the contact opening comprises depositing tungsten within the contact opening.

19. The method of claim 16, wherein forming the titanium silicide interface between the silicon-containing source/drain region and the titanium-containing contact interface layer comprises forming the titanium silicide interface between the silicon-containing source/drain region and the titanium-containing contact interface layer by heating the silicon-containing source/drain region and the titanium-containing contact interface layer.

20. The method of claim 16, wherein forming the titanium silicide interface comprises forming the titanium silicide substantially only between the silicon-containing source/drain region and the titanium-containing contact interface layer.

21. The method of claim 16, wherein forming a contact opening through the dielectric material to expose at least a portion of the source/drain region further comprises forming a contact opening through the dielectric material to expose a portion of the source/drain region and at least a portion of one non-planar transistor gate spacer.

22. The method of claim 21, wherein the forming the titanium-containing contact interface layer further comprises forming the titanium-containing contact interface layer to abut at least a portion of one non-planar transistor gate spacer.

23. The method of claim 16, wherein forming a contact opening through the dielectric material to expose at least a portion of the source/drain region further comprises forming a contact opening through the dielectric material to expose a portion of the source/drain region and at least a portion of the capping structure.

24. The method of claim 23, wherein the forming the titanium-containing contact interface layer further comprises forming the titanium-containing contact interface layer to abut at least a portion of the capping structure.

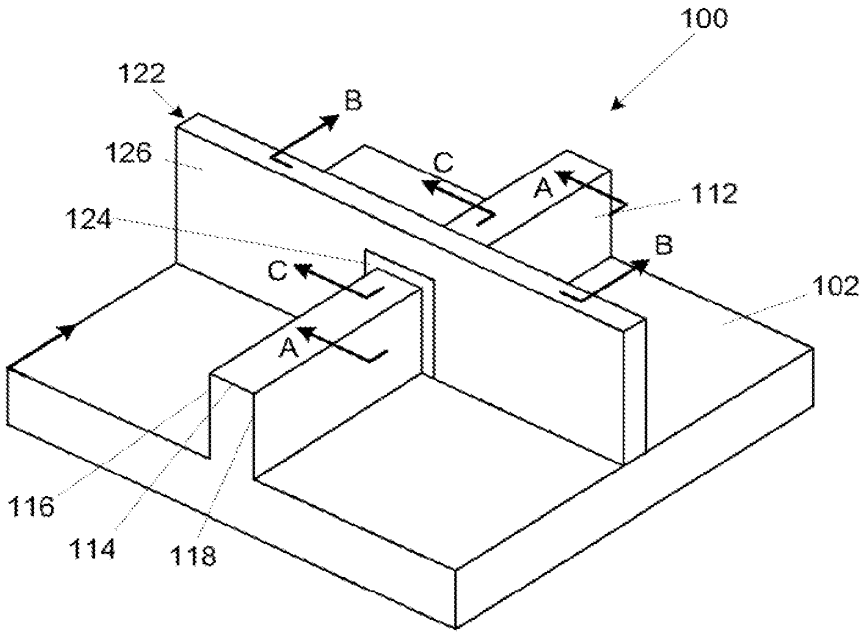


FIG. 1

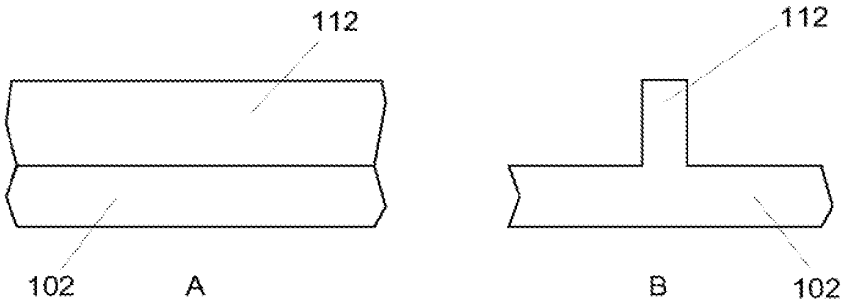


FIG. 2

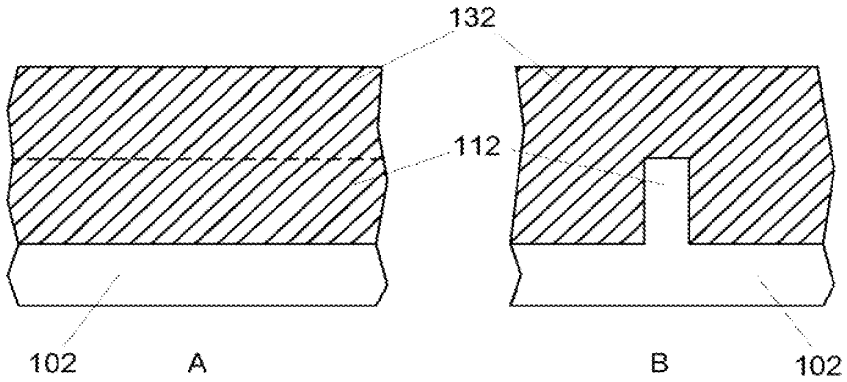


FIG. 3

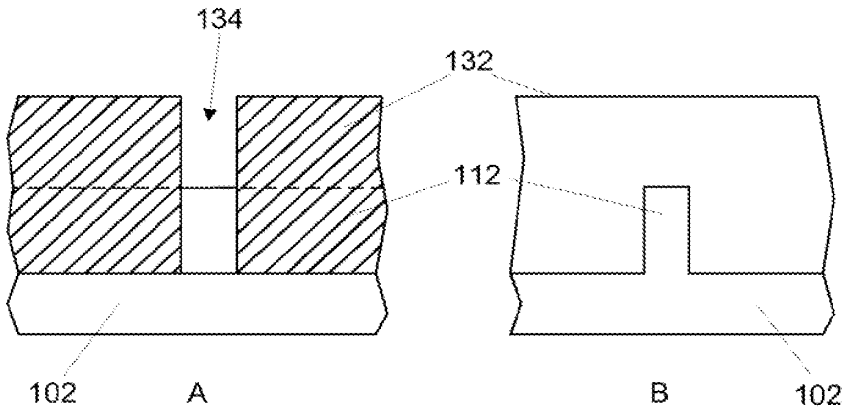


FIG. 4

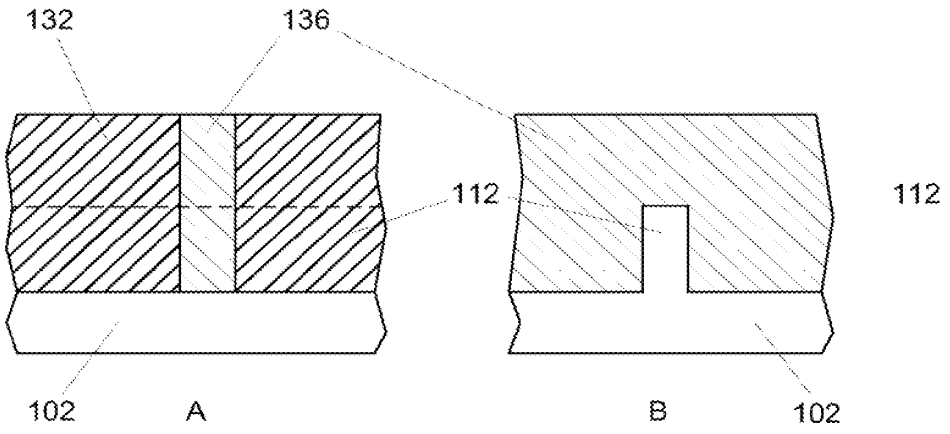


FIG. 5

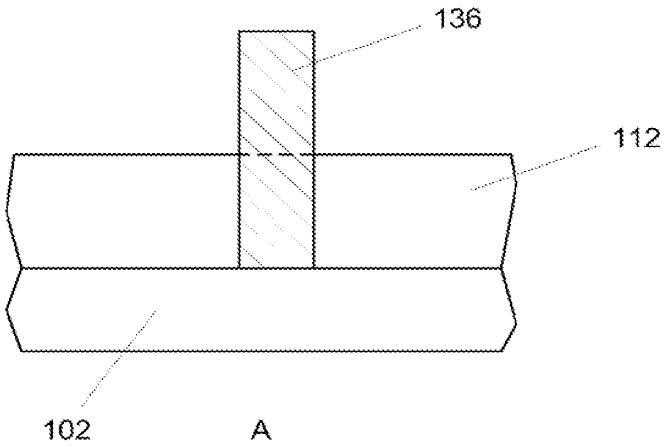


FIG. 6

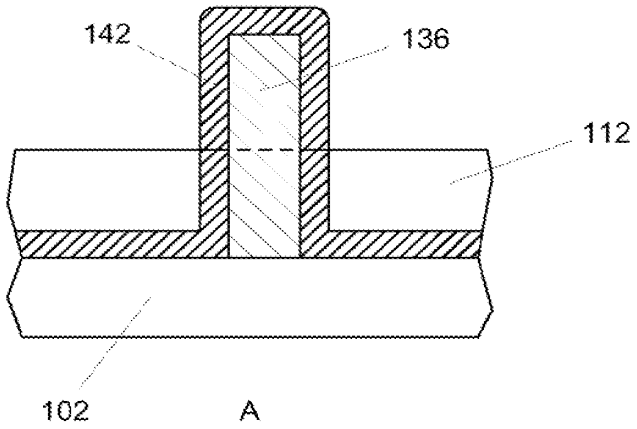


FIG. 7

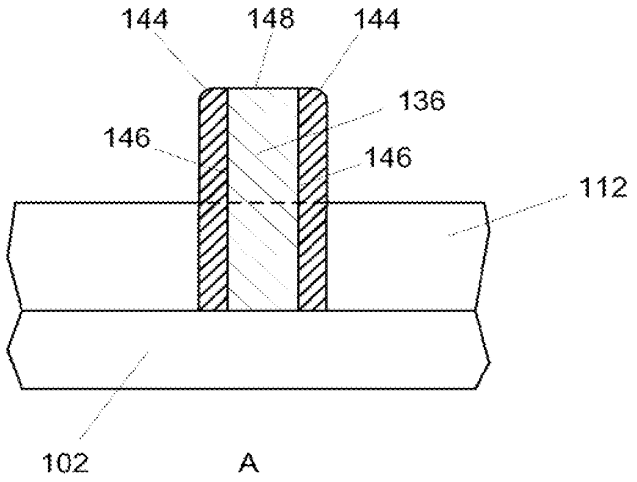


FIG. 8

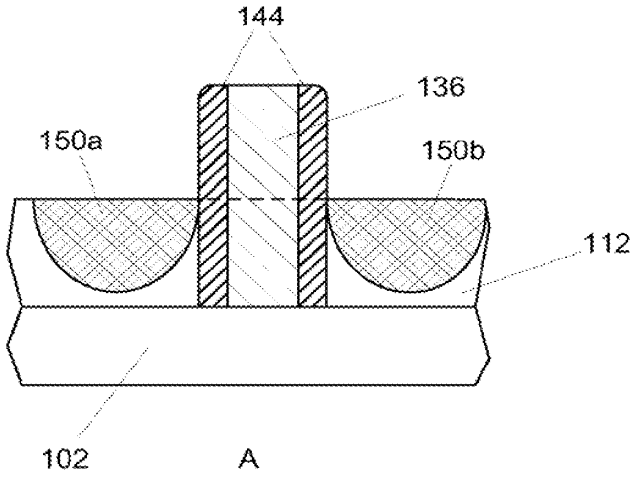


FIG. 9

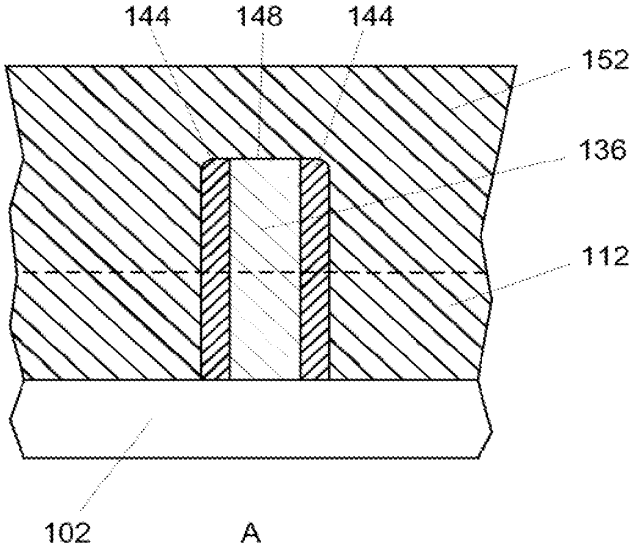


FIG. 10

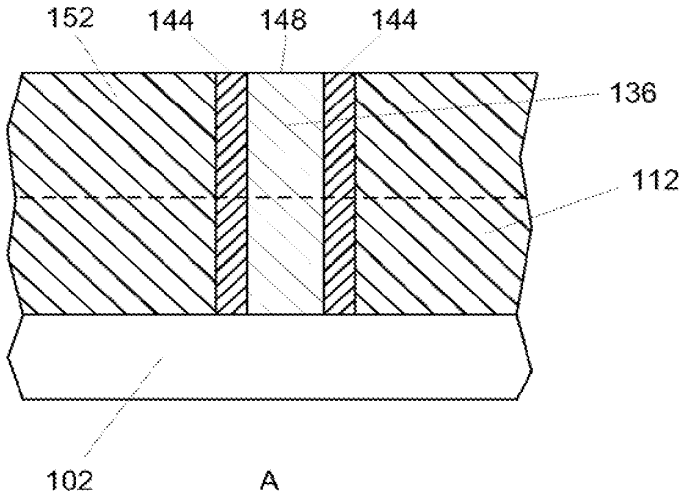


FIG. 11

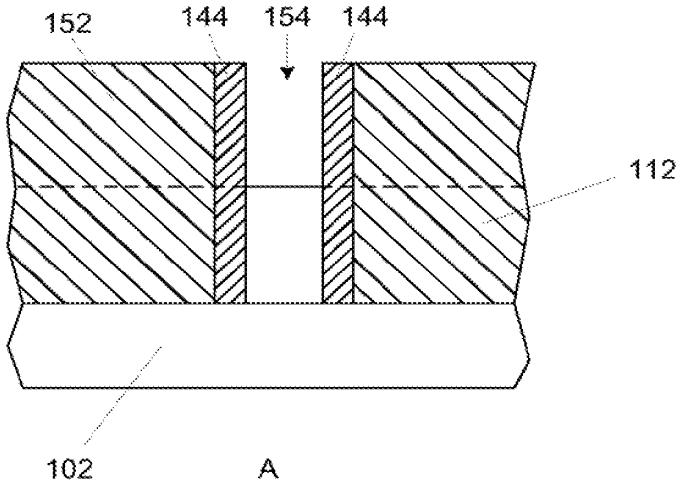


FIG. 12

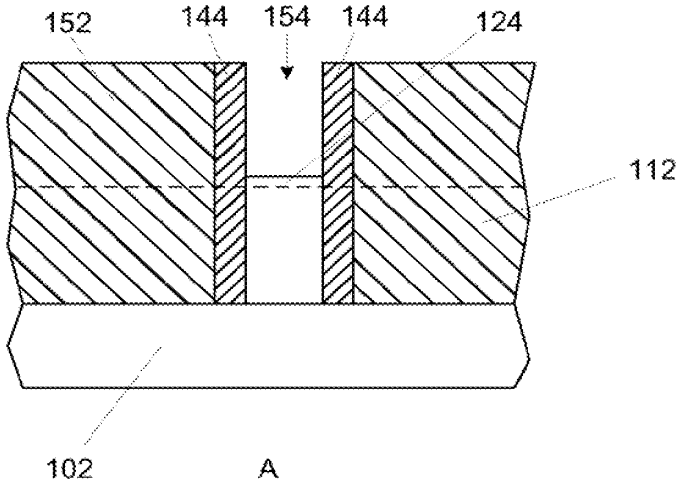


FIG. 13

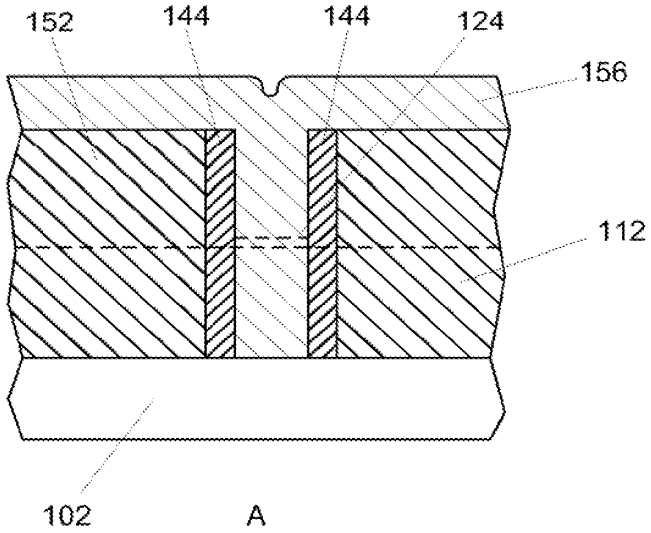


FIG. 14

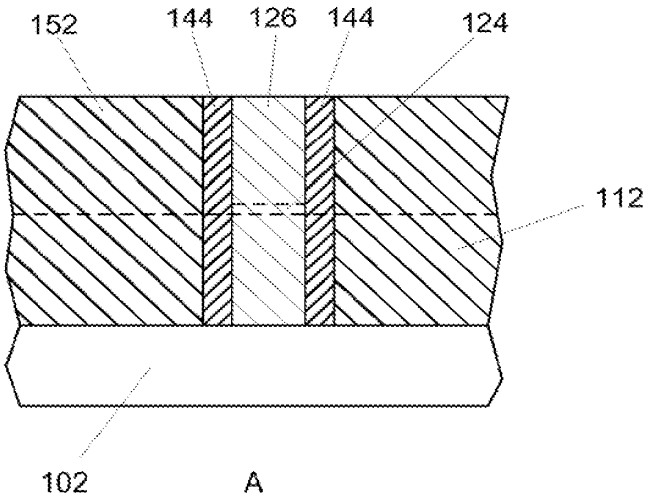

152
144
126
144
124
112
102
A

FIG. 15

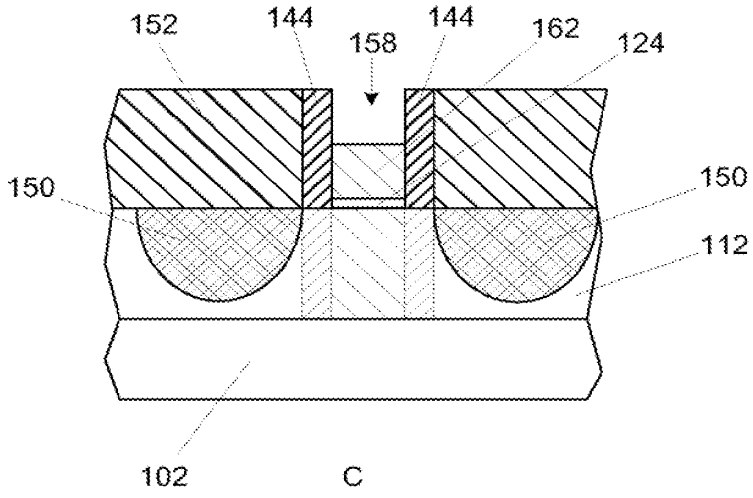

152
144
158
144
162
124
150
150
112
102
C

FIG. 16

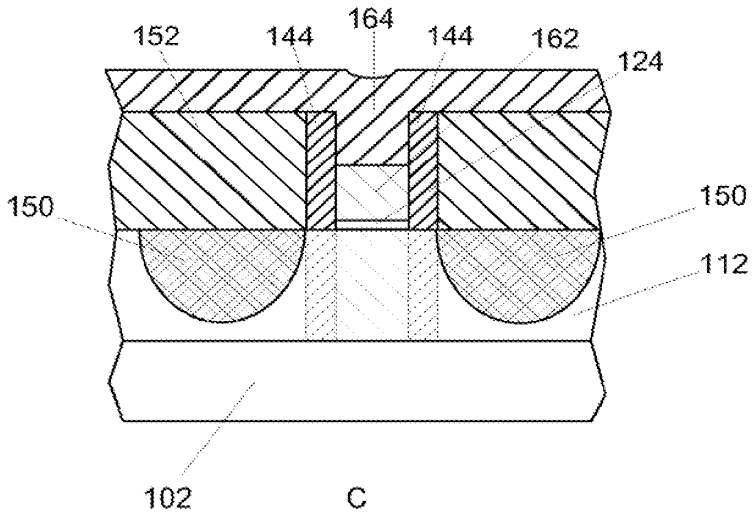

152
144
164
144
162
124
150
150
112
102
C

FIG. 17

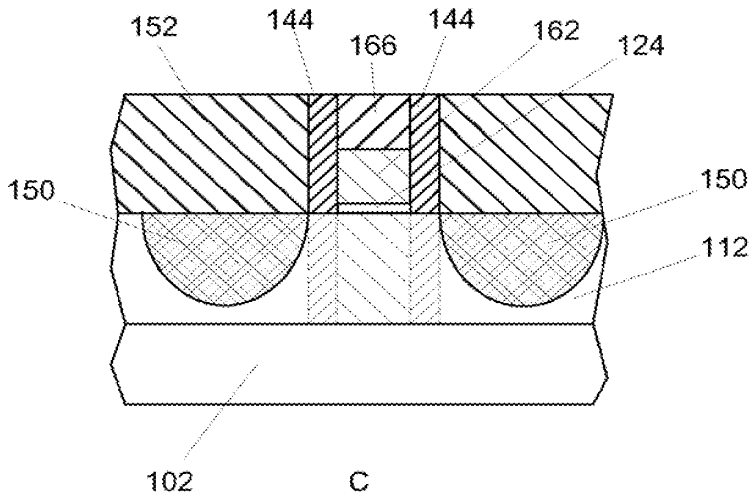

152
144
166
144
162
124
150
150
112
102
C

FIG. 18

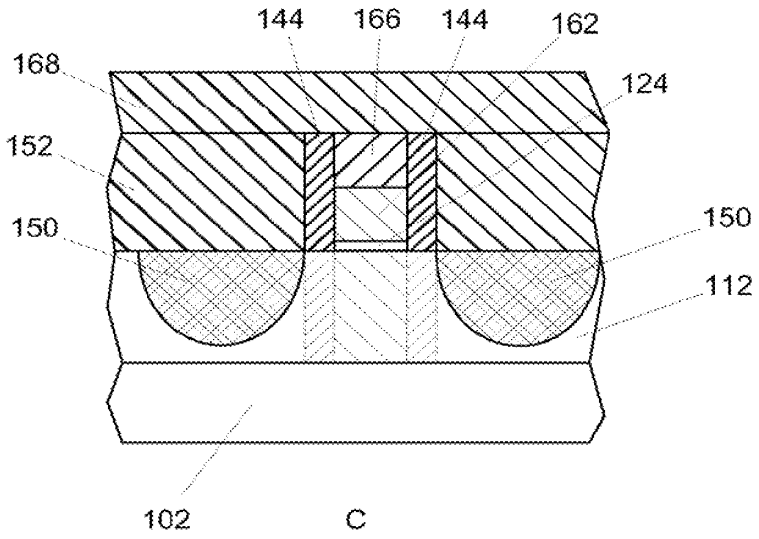

144
166
144
162
168
124
152
150
150
112
102
C

FIG. 19

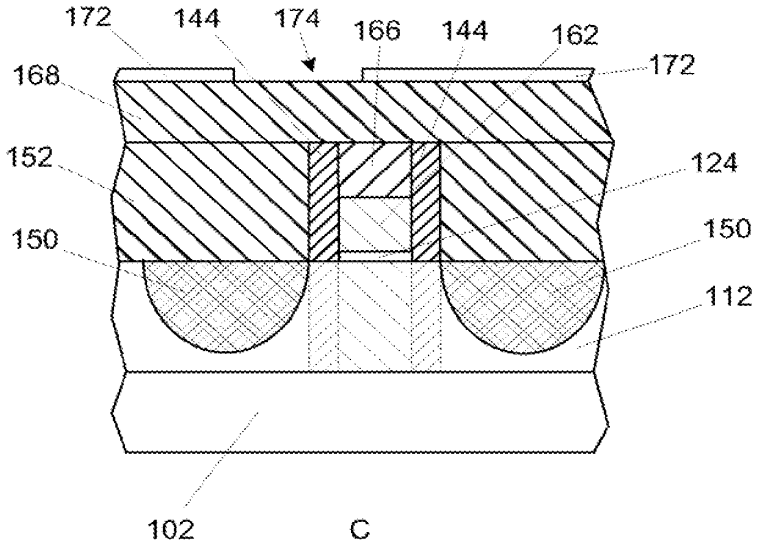

172
144
174
166
144
162
168
172
152
124
150
150
112
102
C

FIG. 20

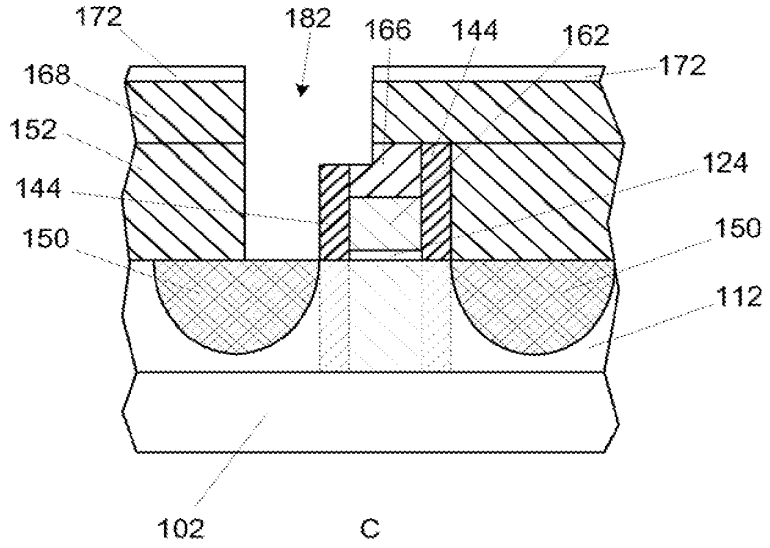

172
182
166
144
162
168
172
152
124
144
150
150
112
102
C

FIG. 21

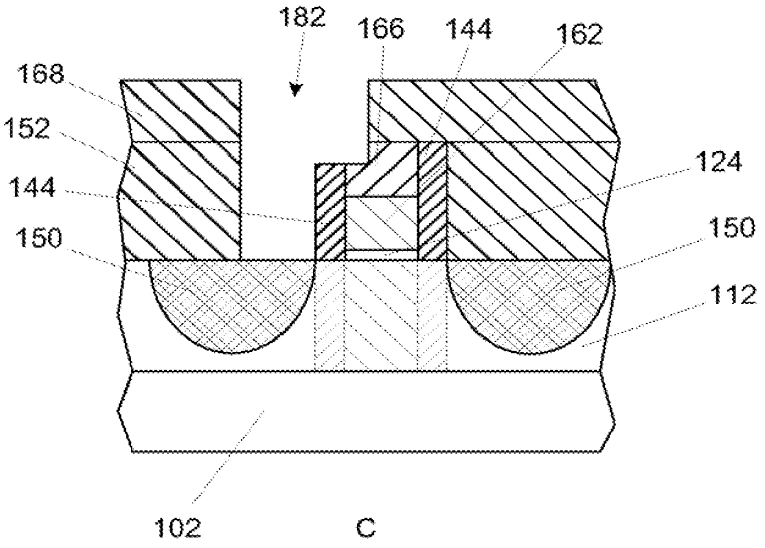

182
166
144
162
168
152
124
144
150
150
112
102
C

FIG. 22

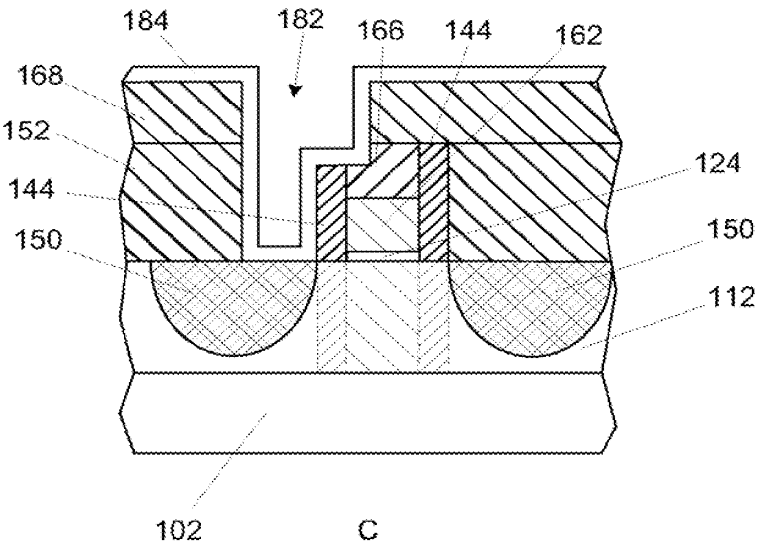

184
182
166
144
162
168
152
144
150
124
150
112
102
C

FIG. 23

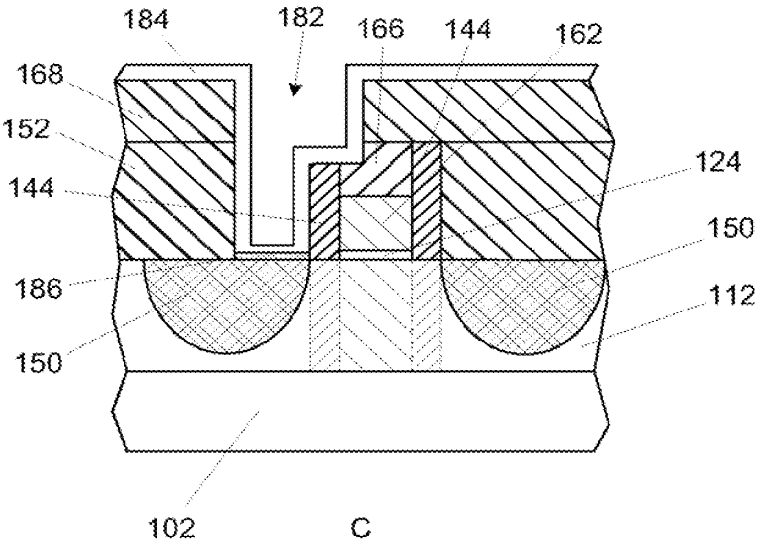

184
182
166
144
162
168
152
144
186
150
124
150
112
102
C

FIG. 24

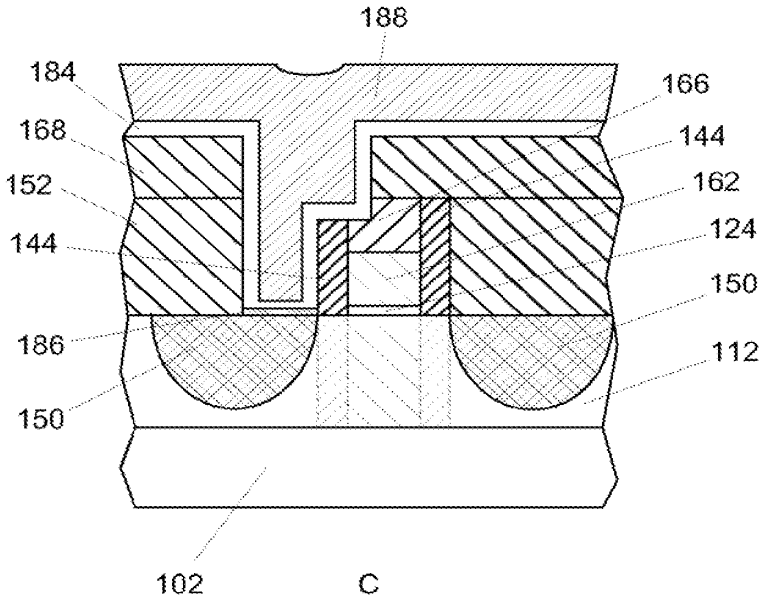

188
184
166
168
144
152
162
144
124
150
186
112
150
102
C

FIG. 25

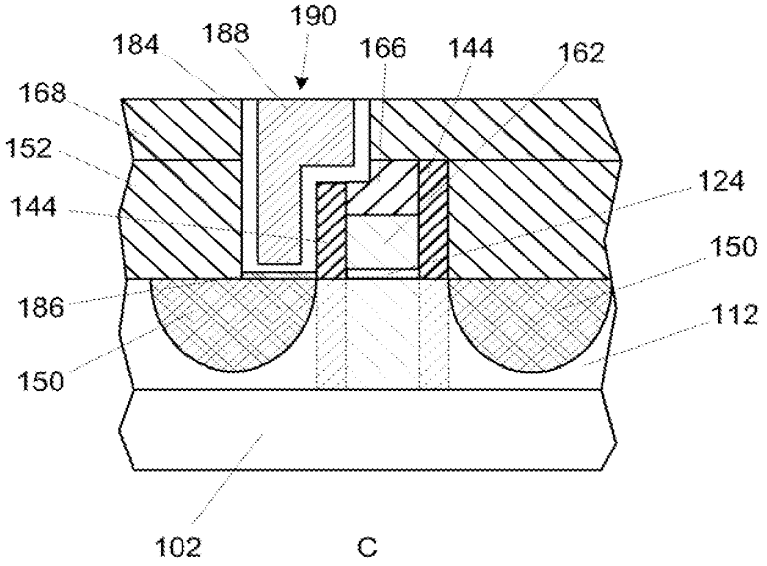

190
184
188
166
144
162
168
152
124
144
150
186
112
150
102
C

FIG. 26

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2011/054479

A. CLASSIFICATION OF SUBJECT MATTER

H01L 29/78(2006.01)i, H01L 21/336(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 29/78; H01L 21/4763; H01L 21/336; H01L 29/94; H01L 29/76; H01L 27/12

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: titanium, non-planar, and transistor

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 7456471 B2 (ANDERSON BRENT A. et al.) 25 November 2008 See the abstract; figs. 1-24; column 5, line 45 - column 11, line 55.	1-24
A	US 06136697 A (HU; SHYH-LIN) 24 October 2000 See the abstract; figs. 1-11; column 3, line 40 - column 51, line 41.	1-24
A	KR 10-0585178 B1 (SAMSUNG ELECTRONICS CO., LTD.) 24 May 2006 See the abstract; figs. 1-21; claims 1-31.	1-24

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15 MAY 2012 (15.05.2012)	**16 MAY 2012 (16.05.2012)**

Name and mailing address of the ISA/KR	Authorized officer
Korean Intellectual Property Office Government Complex-Daejeon, 189 Cheongsa-ro, Seo-gu, Daejeon 302-701, Republic of Korea	Lee,Sang Ho
Facsimile No. 82-42-472-7140	Telephone No. 82-42-481-8221

Form PCT/ISA/210 (second sheet) (July 2009)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2011/054479

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 7456471 B2	25.11.2008	EP 2070110 A2	17.06.2009
		JP 2010-503997 A	04.02.2010
		JP 2010-503997 T	04.02.2010
		KR 10-1104040 B1	06.01.2012
		KR 2009-0075822 A	09.07.2009
		US 2008-0067613 A1	20.03.2008
		US 2008-0286913 A1	20.11.2008
		US 7851283 B2	14.12.2010
		WO 2008-033982 A2	20.03.2008
		WO 2008-033982 A3	05.06.2008
		WO 2008-033982 A3	20.03.2008
US 06136697 A	24.10.2000	None	
KR 10-0585178 B1	30.05.2006	US 2006-0175669 A1	10.08.2006

Form PCT/ISA/210 (patent family annex) (July 2009)

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
13 June 2013 (13.06.2013)

WIPO | PCT

(10) International Publication Number
WO 2013/085490 A1

(51) International Patent Classification:
H01L 21/336 (2006.01) *H01L 21/31* (2006.01)
H01L 29/78 (2006.01)

(21) International Application Number:
PCT/US2011/063433

(22) International Filing Date:
6 December 2011 (06.12.2011)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant *(for all designated States except US)*: **INTEL CORPORATION** [US/US], 2200 Mission College Boulevard, Santa Clara, California 95052 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **PRADHAN, Sameer** [IN/US]; 17923 NW Sylvania Lane, Portland, Oregon 97229 (US). **LUCE, Jeanne** [US/US]; 4134 NE Azalea Street, Hillsboro, Oregon 97124 (US).

(74) Agent: **WINKLE, Robert**; Winkle, PLLC, c/o CPA Global, P.O. Box 52050, Minneapolis, Minnesota 55402 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK,

[Continued on next page]

(54) Title: INTERLAYER DIELECTRIC FOR NON-PLANAR TRANSISTORS

(57) Abstract: The present description relates the formation of a first level interlayer dielectric material layer within a non-planar transistor, which may be formed by a spin-on coating technique followed by oxidation and annealing. The first level interlayer dielectric material layer may be substantially void free and may exert a tensile strain on the source/drain regions of the non-planar transistor.

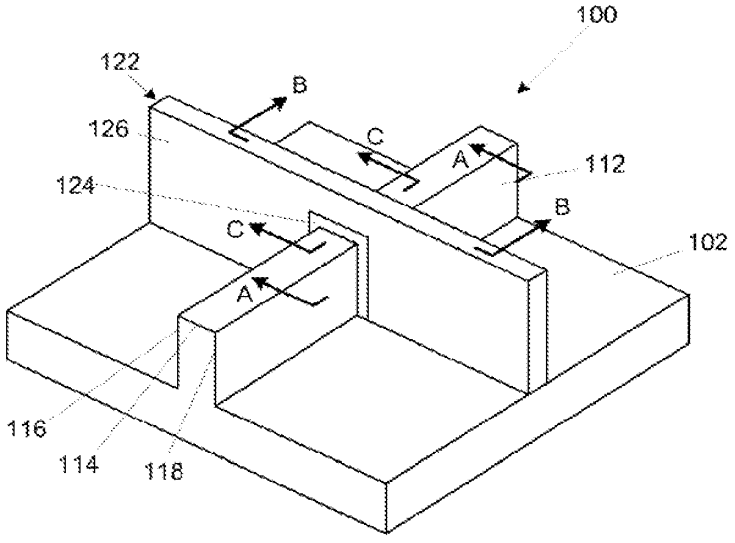


FIG. 1

WO 2013/085490 A1

SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *of inventorship (Rule 4.17(iv))*

Published:

— *with international search report (Art. 21(3))*

INTERLAYER DIELECTRIC FOR NON-PLANAR TRANSISTORS

BACKGROUND

Embodiments of the present description generally relate to the field of microelectronic device fabrication and, more particularly, to the fabrication of a first level interlayer dielectric material layer in a non-planar transistor.

BRIEF DESCRIPTION OF THE DRAWINGS

The subject matter of the present disclosure is particularly pointed out and distinctly claimed in the concluding portion of the specification. The foregoing and other features of the present disclosure will become more fully apparent from the following description and appended claims, taken in conjunction with the accompanying drawings. It is understood that the accompanying drawings depict only several embodiments in accordance with the present disclosure and are, therefore, not to be considered limiting of its scope. The disclosure will be described with additional specificity and detail through use of the accompanying drawings, such that the advantages of the present disclosure can be more readily ascertained, in which:

FIG. 1 is a perspective view of a non-planar transistor, according to an embodiment of the present description.

FIG. 2 illustrates side cross-sectional views of a non-planar transistor fin formed in or on a microelectronic substrate.

FIG. 3 illustrates side cross-sectional views of a sacrificial material deposited over the non-planar transistor fin of FIG. 2, according to an embodiment of the present description.

FIG. 4 illustrates side cross-sectional views of a trench formed in the sacrificial material deposited to expose a portion of the non-planar transistor fin of FIG. 3, according to an embodiment of the present description.

FIG. 5 illustrates side cross-sectional views of a sacrificial gate formed in the trench of FIG. 4, according to an embodiment of the present description.

FIG. 6 illustrates a side cross-sectional view of the sacrificial gate after the removal of the sacrificial material of FIG. 5, according to an embodiment of the present description.

FIG. 7 illustrates a side cross-sectional view of a conformal dielectric layer deposited over the sacrificial gate and microelectronic substrate of FIG. 6, according to an embodiment of the present description.

FIG. 8 illustrates a side cross-sectional view of gate spacers formed from the conformal dielectric layer of FIG. 7, according to an embodiment of the present description.

FIG. 9 illustrates a side cross-sectional view of a source region and a drain region formed in the non-planar transistor fin on either side of the gate spacers of FIG. 8, according to an embodiment of the present description.

FIG. 10 illustrates a side cross-sectional view of an adhesion layer formed on the structure of FIG. 9, according to an embodiment of the present description.

FIG. 11 illustrates a side cross-sectional view of a first interlayer dielectric material layer deposited over the gate spacers, the sacrificial gate, the non-planar transistor fin, and the microelectronic substrate of FIG. 10, according to an embodiment of the present description.

FIG. 12 illustrates a side cross-sectional view of the first interlayer dielectric material layer of FIG. 11 being oxidized and annealed, according to an embodiment of the present description.

FIG. 13 illustrates a side cross-section view of the structure of FIG. 12 wherein a portion of the first interlayer dielectric material layer is densified by the oxidization and annealing of FIG. 13, according to an embodiment of the present description.

FIG. 14 illustrates a side cross-sectional view of the structure of FIG. 13 after planarizing the first interlayer dielectric material layer to expose a top surface of the sacrificial gate, according to an embodiment of the present description.

FIG. 15 illustrates a side cross-sectional view of the structure of FIG. 14 after the removal of the sacrificial gate to form a gate trench, according to an embodiment of the present description.

FIG. 16 illustrates a side cross-sectional view of the structure of FIG. 15 after the formation of a gate dielectric adjacent the non-planar transistor fin between the gate spacers, according to an embodiment of the present description.

FIG. 17 illustrates a side cross-sectional view of a conductive gate material deposited in the gate trench of FIG. 16, according to an embodiment of the present description.

FIG. 18 illustrates a side cross-sectional view of the structure of FIG. 17 after the removal of excess conductive gate material to form a non-planar transistor gate, according to an embodiment of the present description.

FIG. 19 illustrates a side cross-sectional view of the structure of FIG. 18 after etching away a portion of the non-planar transistor gate to form a recessed non-planar transistor gate, according to an embodiment of the present description.

FIG. 20 illustrates a side cross-sectional view of the structure of FIG. 19 after depositing a capping dielectric material into the recess resulting from the formation of the recessed non-planar transistor gate, according to an embodiment of the present description.

FIG. 21 illustrates a side cross-sectional view of the structure of FIG. 20 after the removal of excess capping dielectric material to form a capping structure on the non-planar transistor gate, according to an embodiment of the present description.

FIG. 22 illustrates a side cross-sectional view of a second interlayer dielectric material layer deposited over the first interlayer dielectric material layer, the gate spacers, and the sacrificial gate top surface of FIG. 21, according to an embodiment of the present description.

FIG. 23 illustrates a side cross-sectional view of an etch mask patterned on the second dielectric material of FIG. 22, according to an embodiment of the present description.

FIG. 24 illustrates a side cross-sectional view of a contact opening formed through the first and second dielectric material layer of FIG. 23, according to an embodiment of the present description.

FIG. 25 illustrates a side cross-sectional view of the structure of FIG. 24 after the removal of the etch mask, according to an embodiment of the present description.

FIG. 26 illustrates a side cross-sectional view of a conductive contact material deposited in the contact opening of FIG. 25, according to an embodiment of the present description.

FIG. 27 illustrates a side cross-sectional view of the structure of FIG. 25 after the removal of the excess conductive contact material to form a source/drain contact, according to an embodiment of the present description.

FIG. 28 illustrates a computing device, according to one implementation of the present description.

DETAILED DESCRIPTIONIn the following detailed description, reference is made to the accompanying drawings that show, by way of illustration, specific embodiments in which the claimed subject matter may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the subject matter. It is to be understood that the various embodiments, although different, are not necessarily mutually exclusive. For example, a particular feature, structure, or characteristic described herein, in connection with one embodiment, may be implemented within other embodiments without departing from the spirit and scope of the claimed subject matter. References within this specification to "one embodiment" or "an embodiment" mean that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one implementation encompassed within the present invention. Therefore, the use of the phrase "one embodiment" or "in an embodiment" does not necessarily refer to the same embodiment. In addition, it is to be understood that the location or arrangement of individual elements within each disclosed embodiment may be modified without departing from the spirit and scope of the claimed subject matter. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the subject matter is defined only by the appended claims, appropriately interpreted, along with the full range of equivalents to which the appended claims are entitled. In the drawings, like numerals refer to the same or similar elements or functionality throughout the several views, and that elements depicted therein are not necessarily to scale with one another, rather individual elements may be enlarged or reduced in order to more easily comprehend the elements in the context of the present description.

In the fabrication of non-planar transistors, such as tri-gate transistors and FinFETs, non-planar semiconductor bodies may be used to form transistors capable of full depletion with very small gate lengths (e.g., less than about 30 nm). These semiconductor bodies are generally fin-shaped and are, thus, generally referred to as transistor "fins". For example in a tri-gate transistor, the transistor fins have a top surface and two opposing sidewalls formed on a bulk semiconductor substrate or a silicon-on-insulator substrate. A gate dielectric may be formed on the top surface and sidewalls of the semiconductor body and a gate electrode may be formed over the gate dielectric on the top surface of the semiconductor body and adjacent to the gate dielectric on the sidewalls of the semiconductor body. Thus, since the gate dielectric and the gate electrode are adjacent to three surfaces of the semiconductor body, three separate channels and gates are formed. As there are three separate channels formed, the semiconductor body can be fully depleted when the transistor is turned on. With regard to finFET transistors, the gate

material and the electrode only contact the sidewalls of the semiconductor body, such that two separate channels are formed (rather than three in tri-gate transistors).

Embodiments of the present description relate to the formation of a first level interlayer dielectric material layer within a non-planar transistors, which may be formed by a spin-on coating technique followed by oxidation and annealing. The first level interlayer dielectric material layer may be substantially void free and may exert a tensile strain on the source/drain regions of the non-planar transistor.

FIG. 1 is a perspective view of a non-planar transistor 100, including at least one gate formed on at least one transistor fin, which are formed on a microelectronic substrate 102. In an embodiment of the present disclosure, the microelectronic substrate 102 may be a monocrystalline silicon substrate. The microelectronic substrate 102 may also be other types of substrates, such as silicon-on-insulator ("SOI"), germanium, gallium arsenide, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, gallium antimonide, and the like, any of which may be combined with silicon.

The non-planar transistor, shown as a tri-gate transistor, may include at least one non-planar transistor fin 112. The non-planar transistor fin 112 may have a top surface 114 and a pair of laterally opposite sidewalls, sidewall 116 and opposing sidewall 118, respectively.

As further shown in FIG. 1, at least one non-planar transistor gate 122 may be formed over the non-planar transistor fin 112. The non-planar transistor gate 122 may be fabricated by forming a gate dielectric layer 124 on or adjacent to the non-planar transistor fin top surface 114 and on or adjacent to the non-planar transistor fin sidewall 116 and the opposing non-planar transistor fin sidewall 118. A gate electrode 126 may be formed on or adjacent the gate dielectric layer 124. In one embodiment of the present disclosure, the non-planar transistor fin 112 may run in a direction substantially perpendicular to the non-planar transistor gate 122.

The gate dielectric layer 124 may be formed from any well-known gate dielectric material, including but not limited to silicon dioxide (SiO_2), silicon oxynitride (SiO_xN_y), silicon nitride (Si_3N_4), and high-k dielectric materials such as hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate. The gate dielectric layer 124 can be formed by well-known techniques, such as by conformally depositing a gate dielectric material and then patterning the gate dielectric material with well-

known photolithography and etching techniques, as will be understood to those skilled in the art.

The gate electrode 126 can be formed of any suitable gate electrode material. In an embodiment of the present disclosure, the gate electrode 126 may be formed from materials that include, but are not limited to, polysilicon, tungsten, ruthenium, palladium, platinum, cobalt, nickel, hafnium, zirconium, titanium, tantalum, aluminum, titanium carbide, zirconium carbide, tantalum carbide, hafnium carbide, aluminum carbide, other metal carbides, metal nitrides, and metal oxides. The gate electrode 126 can be formed by well-known techniques, such as by blanket depositing a gate electrode material and then patterning the gate electrode material with well-known photolithography and etching techniques, as will be understood to those skilled in the art.

A source region and a drain region (not shown in FIG. 1) may be formed in the non-planar transistor fin 112 on opposite sides of the gate electrode 126. In one embodiment, the source and drain regions may be formed by doping the non-planar transistor fins 112, as will be understood to those skilled in the art. In another embodiment, the source and drain regions may be formed by removing potions of the non-planar transistor fins 112 and replacing these portions with appropriate material(s) to form the source and drain regions, as will be understood to those skilled in the art. In still another embodiment, the source and drain regions may be formed by exitaxially growing doped or undoped strain layers on the fins 112.

FIGs. 2-26 illustrate side cross-sectional view of one embodiment of fabricating a non-planar transistor, wherein FIGs. 2-5 are views along arrows A-A and B-B of FIG. 1, FIGs. 6-15 are views along arrows A-A of FIG. 1, and FIG. 16-26 are views along arrows C-C of FIG. 1.

As shown in FIG. 2, the non-planar transistor fin 112 may be formed by etching the microelectronic substrate 102 or by forming the non-planar transistor fin 112 on the microelectronic substrate 102 by any technique known in the art. As illustrated in FIG. 3, a sacrificial material 132 may be deposited over the non-planar transistor fin 112, as shown in FIG. 3, and a trench 134 may be formed in the sacrificial material 132 to expose a potion of the non-planar transistor fin 112, as shown in FIG. 4. The sacrificial material 132 may be any appropriate material known in the art, and the trench 134 may be formed by any technique known in the art, including but not limited to lithographic masking and etching.

As shown in FIG. 5, a sacrificial gate 136 may be formed in the trench 134 (see FIG. 4). The sacrificial gate 136 may be any appropriate material, such as a polysilicon material and the like, and may be deposited in the trench 134 (see FIG. 4) by any technique known in the art,

including but not limited to chemical vapor deposition ("CVD") and physical vapor deposition ("PVD").

As shown in FIG. 6, the sacrificial material 132 of FIG. 5 may be removed to expose the sacrificial gate 136 by any technique known in the art, such as selectively etching the sacrificial material 132. As shown in FIG. 7, a conformal dielectric layer 142 may be deposited over the sacrificial gate 136 and microelectronic substrate 102. The conformal dielectric layer 142 may be any appropriate material, including but not limited to silicon nitride (Si_3N_4) and silicon carbide (SiC), and may be formed by any appropriate technique including but not limited to atomic layer deposition ("ALD").

As shown in FIG. 8, the conformal dielectric layer 142 of FIG. 7 may be etched, such as by directional etch with an appropriate etchant, to form a pair of gate spacers 144 on sidewalls 146 of the sacrificial gate 136, while substantially removing the conformal dielectric layer 142 adjacent the microelectronic substrate 102 and a top surface 148 of the sacrificial gate 136. It is understood that fin spacers (not shown) may be simultaneously formed on sidewalls 116 and 118 (see FIG. 1) of the non-planar transistor fin 112 during the formation of the gate spacers 144.

As shown in FIG. 9, a source region 150a and a drain region 150b may be formed on either side of the gate spacers 144. In one embodiment, the source region 150a and the drain region 150b may be formed in the non-planar transistor fin 112 with the implantation of N-type or P-type ion dopants. As will be understood to those skilled in that art, dopant implantation is a process of introducing impurities into semiconducting materials for the purpose changing its conductivity and electronic properties. This is generally achieved by ion implantation of either P-type ions or N-type ions, collectively referred to as "dopants". In another embodiment, portions of the non-planar transistor fin 112 may be removed by any technique known in the art, such as etching, and the source region 150a and the drain region 150b may be formed in place of the removed portions. In still another embodiment, the source and drain regions may be formed by exitaxially growing doped or undoped strain layers on the fins 112. The source region 150a and the drain region will hereinafter be referred to collectively as "source/drain region 150". As will be understood to those skilled in the art, transistors having P-type source and drains are referred to as "PMOS" or "p-channel metal-oxide-semiconductor" transistors, and transistors having N-type source and drains are referred to as "NMOS" or "n-channel metal-oxide-semiconductor" transistors.

As shown in FIG. 10, an adhesion liner 152, such as silicon dioxide, may be conformally deposited over the gate spacers 144, the sacrificial gate top surface 148, the non-planar transistor

fin 112, and the microelectronic substrate 102. The adhesion line 152 may provide a sufficient adhesion between a subsequently formed interlayer dielectric material alyer, and the structure of FIG. 9, i.e., the gate spacers 144, the sacrificial gate top surface 148, the non-planar transistor fin 112, and the microelectronic substrate 102.

As shown in FIG. 11, a first interlayer dielectric material layer 154 may be formed on the adhesion liner 152 with a spin-on coating technique, which may be used to apply a substantially uniform thin film to a substrate. In one embodiment of the present description, an excess amount of interlayer dielectric material may be deposited on the adhesion liner 152. The microelectronic substrate 102 may then be rotated, generally at a high speed, to spread the interlayer dielectric material across the microelectronic substrate 102 by centrifugal force; thus, forming the first interlayer dielectric material layer 154. The spin-on coating technique may have the capability scale to relatively pitch sizes, while still achieving effective gap fill (e.g. little or substantially no void formation) even with high aspect ratio structures.

As shown in FIG. 12, the first interlayer dielectric material layer 154 may be oxidized follow by an annealing (the oxidation and annealing steps are illustrated as arrows 156). Although the oxidation and annealing steps are illustrated in a single drawing with common arrows 156, this is merely for conciseness in the illustrations. It is understood that the oxidation and annealing steps can be separated by one or more processing steps.

In one embodiment, the oxidation may be performed in a vertical diffusion furnace at about 410 degrees Celsius in about a 93% steam atmosphere for about 2 hours. The oxidation may drive out solvent from the first interlayer dielectric material layer 154 and may result in a volume shrinkage of the first interlayer dielectric material layer 154 of between about 10% and 12%. This shrinkage may exert a tensile strain and has been shown to increase drive currents of NMOS trigate transistors up to about 7% due to channel mobility enhancement, as will be understood to those skilled in the art. In one embodiment, the annealing may be achieved by a two step anneal in a high density plasma chamber with a helium gas (or other such inert gas) atmosphere. The first step may comprise powering up RF electrodes within the high density plasma chamber, such as top and side electrodes, to about 16kW for a time duration of about six (6) minutes. The second step may comprise powering up the high density plasma chamber RF electrodes, such as top and side electrodes, to about 6kW for a time duration of about two (2) minutes.

As shown in FIG. 13, a portion 158 of the first interlayer dielectric 154 may be densified as a result of the oxidation and annealing step previously described. The densified dielectric

portion 158 may assist in protecting the first interlayer dielectric 154 during downstream processing.

As shown in FIG. 14, the first interlayer dielectric layer 154 may be planarized to expose the sacrificial gate top surface 148. The planarization of the first dielectric material layer 154 may be achieved by any technique known in the art, including but not limited to chemical mechanical polishing (CMP). As shown in FIG. 14, a portion of the densified dielectric portion 158 may remain after planarization.

As shown in FIG. 15, the sacrificial gate 136 of FIG. 14 may be removed to form a gate trench 164. The sacrificial gate 136 may be removed by any technique known in the art, such as a selective etch. As shown in FIG. 16, the gate dielectric layer 124, as also illustrated in FIG. 1, may be formed to abut the non-planar transistor fin 112, as previously discussed. The materials and methods of forming the gate dielectric 124 have been previously discussed.

As shown in FIG. 17, a conductive gate material 166 may be deposited in the gate trench 164, and excess conductive gate material 166 (e.g. conductive gate material 166 not within the gate trench 166 of FIG. 16) may be removed to from the non-planar transistor gate electrode 126 (see also FIG. 1), as shown in FIG. 18. The materials and methods of forming the gate electrode 126 have been previously discussed. The removal of the excess conductive gate material 166 may be achieved by any technique known in the art, including but not limited to chemical mechanical polishing (CMP), etching, and the like.

As shown in FIG. 19, a portion of the non-planar transistor gate electrode 126 of FIG. 18 may be removed to form a recess 168 and a recessed non-planar transistor gate 172. The removal may be accomplished by any known technique, including but not limited to wet or dry etching. In one embodiment, the formation of the recess may result from a combination of a dry etch and a wet etch.

As shown in FIG. 20, a capping dielectric material 174 may be deposited to fill the recess 168 of FIG. 19. The capping dielectric material 174 may be any appropriate material, including but not limited to silicon nitride (Si_3N_4) and silicon carbide (SiC), and may be formed by any appropriate deposition technique. The capping dielectric material 174 may be planarized to remove excess capping dielectric material 174 (e.g. capping dielectric material 174 not within the recess of FIG. 19) to form a capping dielectric structure 176 on the recessed non-planar transistor gate 172 and between a gate spacers 144, as shown in FIG. 21. The removal of the excess capping dielectric material 174 may be achieved by any technique known in the art,

including but not limited to chemical mechanical polishing (CMP), etching, and the like.

As shown in FIG. 22, a second interlayer dielectric layer 178 may be deposited over the first dielectric material layer 154, the gate spacers 144, and the capping dielectric structure 176. The second interlayer dielectric layer 178 may be formed from any appropriate dielectric material, including but not limited to silicon dioxide (SiO_2), silicon oxynitride (SiO_xN_y), and silicon nitride (Si_3N_4), by any known deposition technique. As shown in FIG. 23, an etch mask 182 may be patterned with at least one opening 184 on the second interlayer dielectric layer 178, such as by well known lithographic techniques.

As shown in FIG. 24, a contact opening 192 may be formed through the first interlayer dielectric layer 154 and the second interlayer dielectric layer 178 by etching through the etch mask opening 184 of FIG. 23 to expose a portion of the source/drain region 150. The etch mask 182 of FIG. 24 may be removed thereafter, as shown in FIG. 25. In one embodiment, the first interlayer dielectric layer 154 and the second dielectric material layer 178 differs from dielectric material of both the gate spacers 144 and the capping dielectric structure 176, such that the etching of the first interlayer dielectric layer 154 and the second interlayer dielectric layer 178 may be selective to the gate spacers 144 and the capping dielectric structure 176 (i.e. etches faster). This is known in the art as a self-aligning.

As shown in FIG. 26, a conductive contact material 196 may be deposited in the contact opening 192 of FIG. 25. The conductive contact material 196 may include, but is not limited to, polysilicon, tungsten, ruthenium, palladium, platinum, cobalt, nickel, hafnium, zirconium, titanium, tantalum, aluminum, titanium carbide, zirconium carbide, tantalum carbide, hafnium carbide, aluminum carbide, other metal carbides, metal nitrides, and metal oxides. It is understood that various adhesion layers, barrier layers, silicide layers, and/or conductive layers may be conformally disposed or formed in the contact opening 192 of FIG. 25 prior to the deposition of the conductive contact material 196.

As shown in FIG. 27, excess conductive contact material 196 of FIG. 26 (e.g. conductive contact material 196 not within the contact opening 192 of FIG. 24) may be removed to form a source/drain contact 198. The removal of the excess conductive contact material 196 may be achieved by any technique known in the art, including but not limited to chemical mechanical polishing (CMP), etching, and the like.

As previously discussed, in one embodiment, the first interlayer dielectric layer 154 and the second interlayer dielectric layer 178 differs from dielectric material of both the gate spacers

144 and the capping dielectric structure 176, such that the etching of the first interlayer dielectric layer 154 and the second interlayer dielectric layer 178 may be selective to the gate spacers 144 and the capping dielectric structure 176 (i.e. etches faster). Thus, the recessed non-planar transistor 172 is protected during the formation of the contact opening 192. This allows for the formation of a relatively large sized source/drain contact 198, which may increase the transistor drive current performance, without the risk of shorting between the source/drain contact 198 and the recessed non-planar transistor gate 172.

FIG. 28 illustrates a computing device 1000 in accordance with one implementation of the present description. The computing device 1000 houses a board 1002. The board 1002 may include a number of components, including but not limited to a processor 1004 and at least one communication chip 1006. The processor 1004 is physically and electrically coupled to the board 1002. In some implementations the at least one communication chip 1006 is also physically and electrically coupled to the board 1002. In further implementations, the communication chip 1006 is part of the processor 1004.

Depending on its applications, computing device 1000 may include other components that may or may not be physically and electrically coupled to the board 1002. These other components include, but are not limited to, volatile memory (e.g., DRAM), non-volatile memory (e.g., ROM), flash memory, a graphics processor, a digital signal processor, a crypto processor, a chipset, an antenna, a display, a touchscreen display, a touchscreen controller, a battery, an audio codec, a video codec, a power amplifier, a global positioning system (GPS) device, a compass, an accelerometer, a gyroscope, a speaker, a camera, and a mass storage device (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth).

The communication chip 1006 enables wireless communications for the transfer of data to and from the computing device 1000. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip 1006 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device 1000 may include a plurality of communication chips 1006.

For instance, a first communication chip 1006 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip 1006 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

The processor 1004 of the computing device 1000 includes an integrated circuit die packaged within the processor 1004. In some implementations of the present description, the integrated circuit die of the processor includes one or more devices, such as non-planar transistors that are formed in accordance with implementations of the present description. The term "processor" may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

The communication chip 1006 also includes an integrated circuit die packaged within the communication chip 1006. In accordance with another implementation of the present description, the integrated circuit die of the communication chip includes one or more devices, such as non-planar transistors that are formed in accordance with implementations of the present description.

In further implementations, another component housed within the computing device 1000 may contain an integrated circuit die that includes one or more devices, such as non-planar transistors that are formed in accordance with implementations of the present description.

In various implementations, the computing device 1000 may be a laptop, a netbook, a notebook, an ultrabook, a smartphone, a tablet, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing device 1000 may be any other electronic device that processes data.

It is understood that the subject matter of the present description is not necessarily limited to specific applications illustrated in FIGs. 1-28. The subject matter may be applied to other microelectronic device fabrication applications, as will be understood to those skilled in the art.

Having thus described in detail embodiments of the present invention, it is understood that the invention defined by the appended claims is not to be limited by particular details set forth in the above description, as many apparent variations thereof are possible without departing from the spirit or scope thereof.

What is claimed is:

1. A method of fabricating a microelectronic transistor, comprising:

forming a transistor gate including a gate electrode adjacent a substrate and a pair of gates spacers on opposing sides of the gate electrode;

forming a source/drain region;

forming a first interlayer dielectric material layer adjacent the source/drain region and adjacent at least one gate spacer;

oxidizing the first interlayer dielectric material layer; and

annealing the first interlayer dielectric material layer.

2. The method of claim 1, wherein forming the first interlayer dielectric material layer comprises depositing the first interlayer dielectric material layer with a spin-on coating technique.

3. The method of claim 1, further including forming an adhesion liner adjacent the source/drain region and adjacent at least one gate spacer, prior to forming the first interlayer dielectric material layer.

4. The method of claim 1, wherein oxidizing the first interlayer dielectric material layer comprises heating the first interlayer dielectric material layer in a steam atmosphere.

5. The method of claim 4, wherein heating the first interlayer dielectric material layer in a steam atmosphere comprises heating the first interlayer dielectric material layer to a temperature of about 410 degrees Celsius in about a 93% steam atmosphere for about 2 hours.

6. The method of claim 1, wherein annealing the first interlayer dielectric material layer comprises annealing the first interlayer dielectric material layer with high density plasma in an inert atmosphere.

7. The method of claim 1, wherein oxidizing and annealing the first interlayer dielectric material layer shrinks the first interlayer dielectric material layer to exert a tensile strain on the source/drain region.

8. A method comprising:

forming a sacrificial non-planar transistor gate over a non-planar transistor fin;

depositing a dielectric material layer over the sacrificial non-planar transistor gate and the non-planar transistor fin;

forming non-planar transistor gate spacers from a portion of the dielectric material layer adjacent the sacrificial non-planar transistor gate;

forming a source/drain region;

removing the sacrificial non-planar transistor gate to form a gate trench between the non-planar transistor gate spacers and expose a portion of the non-planar transistor fin;

forming a gate dielectric adjacent the non-planar transistor fin within the gate trench;

depositing conductive gate material within the gate trench;

removing a portion of the conductive gate material to form a recess between the non-planar transistor gate spacers;

forming a capping dielectric structure within the recess;

forming a first interlayer dielectric material layer over the source/drain region, the non-planar transistor gate spacers, and the capping dielectric structure; and

oxidizing the first interlayer dielectric material layer; and

annealing the first interlayer dielectric material layer.

9. The method of claim 8, wherein forming the first interlayer dielectric material layer comprises depositing the first interlayer dielectric material layer with a spin-on coating technique.

10. The method of claim 8, further including forming an adhesion liner adjacent the source/drain region and adjacent at least one gate spacer, prior to forming the first interlayer dielectric material layer.

11. The method of claim 8, wherein oxidizing the first interlayer dielectric material layer comprises heating the first interlayer dielectric material layer in a steam atmosphere.

12. The method of claim 11, wherein heating the first interlayer dielectric material layer in a steam atmosphere comprises heating the first interlayer dielectric material layer to a temperature of about 410 degrees Celsius in about a 93% steam atmosphere for about 2 hours.

13. The method of claim 8, wherein annealing the first interlayer dielectric material layer comprises annealing the first interlayer dielectric material layer with high density plasma in an

inert atmosphere.

14. The method of claim 8, further including planarizing the first interlayer dielectric material layer.

15. The method of claim 8, further including forming a contact through the at least one dielectric material to contact at least a portion of the source/drain region.

16. The method of claim 8, wherein oxidizing and annealing the first interlayer dielectric material layer shrinks the first interlayer dielectric material layer to exert a tensile strain on the source/drain region.

17. A microelectronic transistor, comprising:

a transistor gate including a gate electrode formed adjacent a substrate and a pair of gate spacers disposed on opposing sides of the gate electrode;

a source/drain region adjacent the transistor gate; and

a first interlayer dielectric material layer formed adjacent the substrate, adjacent the source/drain region, and adjacent at least one gate spacer, wherein the first interlayer dielectric material layer includes a densified portion formed proximate a first surface of the first interlayer dielectric material layer.

18. The microelectronic transistor of claim 17, wherein the transistor gate is non-planar.

19. The microelectronic transistor of claim 17, wherein the source/drain region is non-planar.

20. The microelectronic transistor of claim 17, further including a capping dielectric structure disposed adjacent the non-planar gate electrode and between the pair of gate spacers.

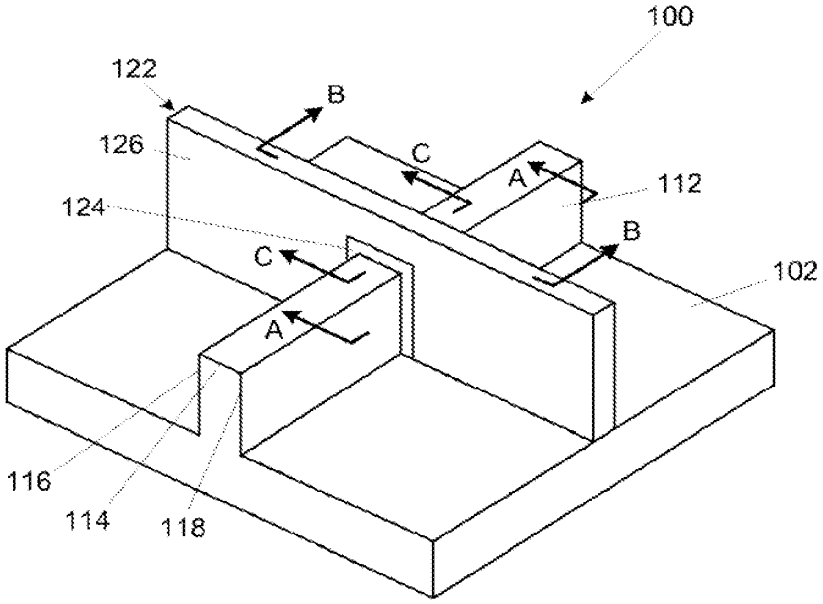


FIG. 1

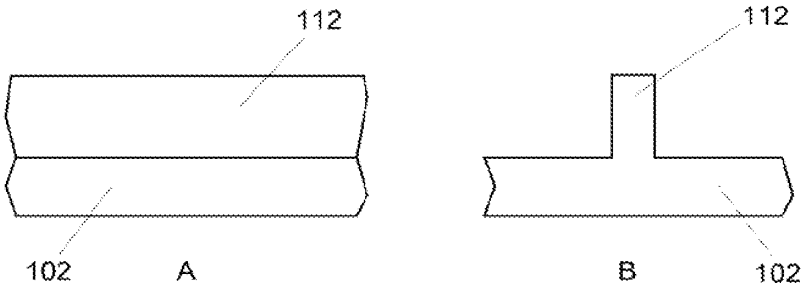


FIG. 2

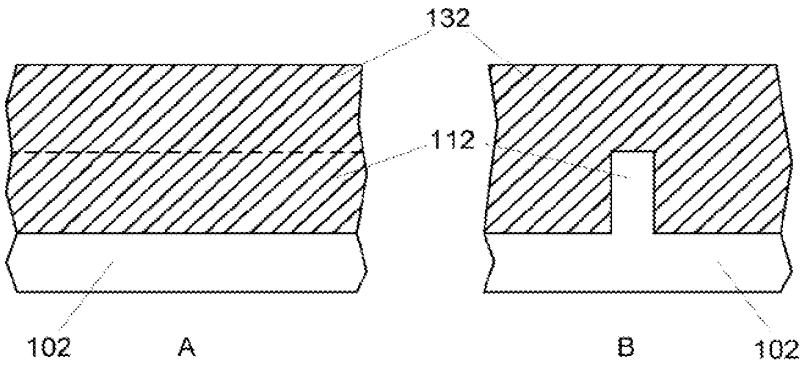


FIG. 3

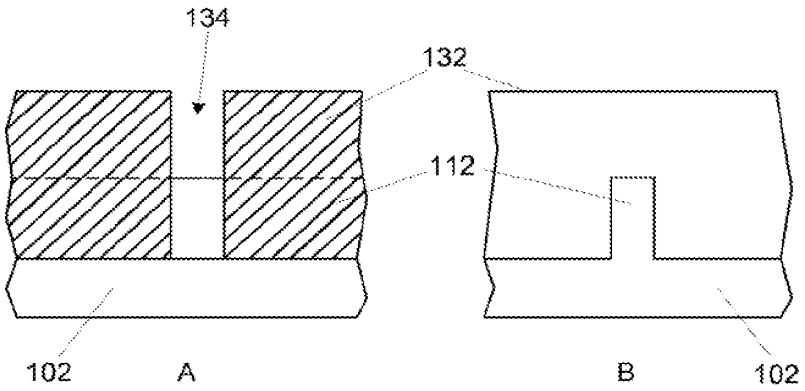


FIG. 4

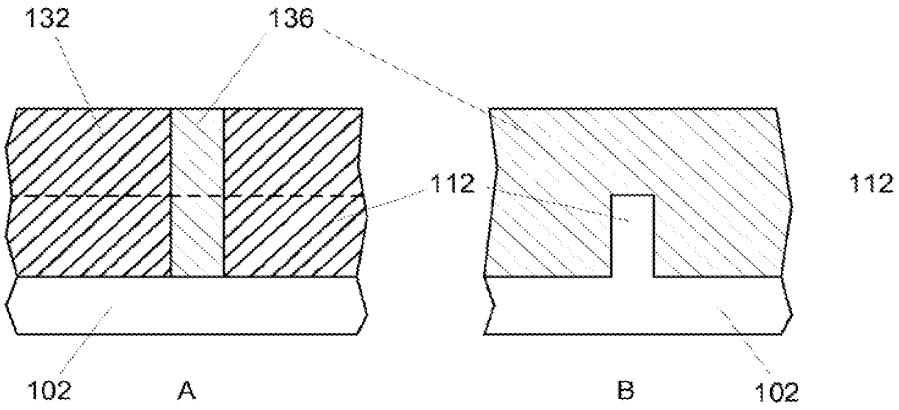


FIG. 5

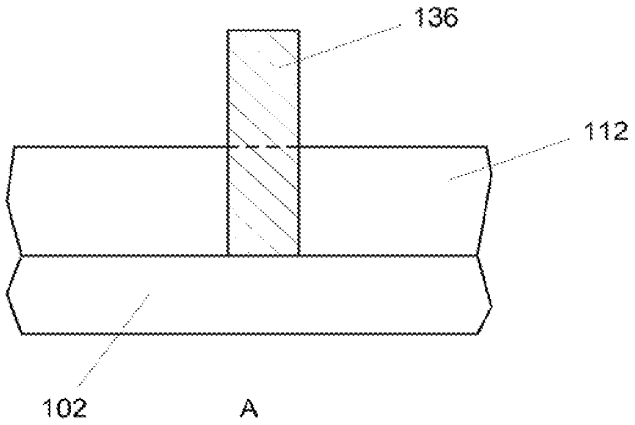


FIG. 6

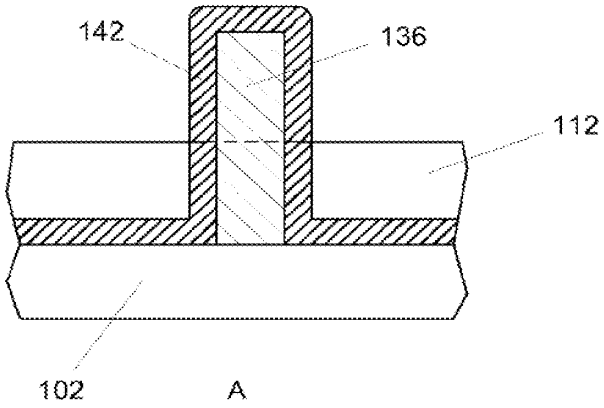


FIG. 7

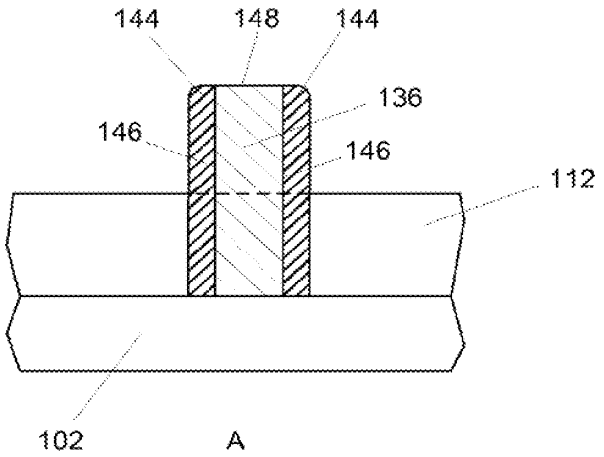


FIG. 8

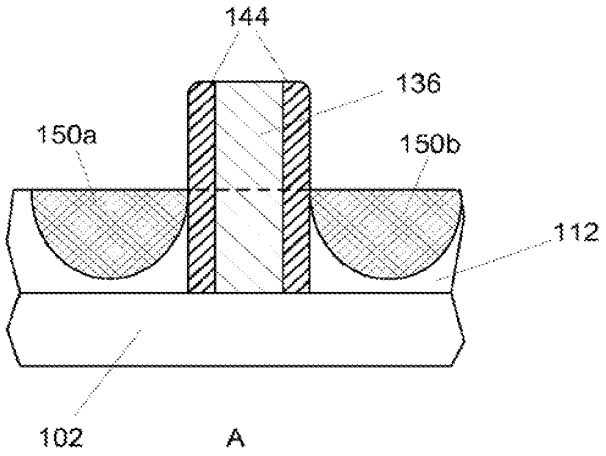


FIG. 9

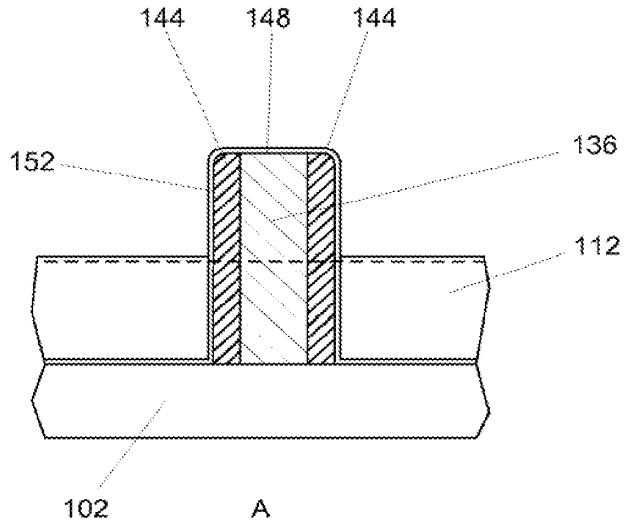


FIG. 10

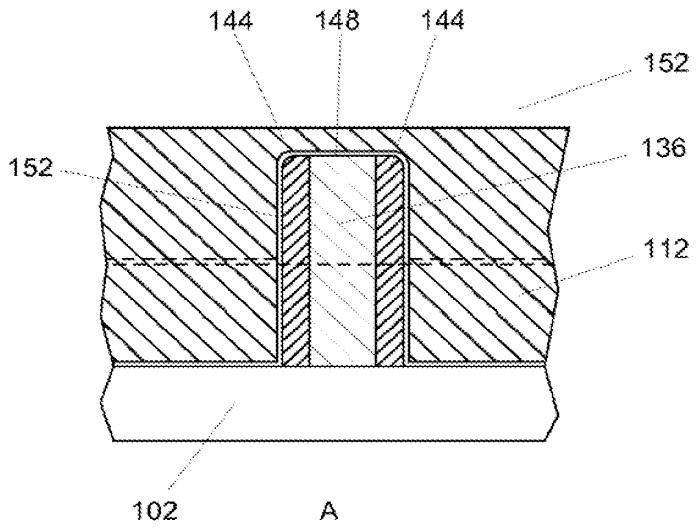

144
148
144
152
152
136
112
102
A

FIG. 11

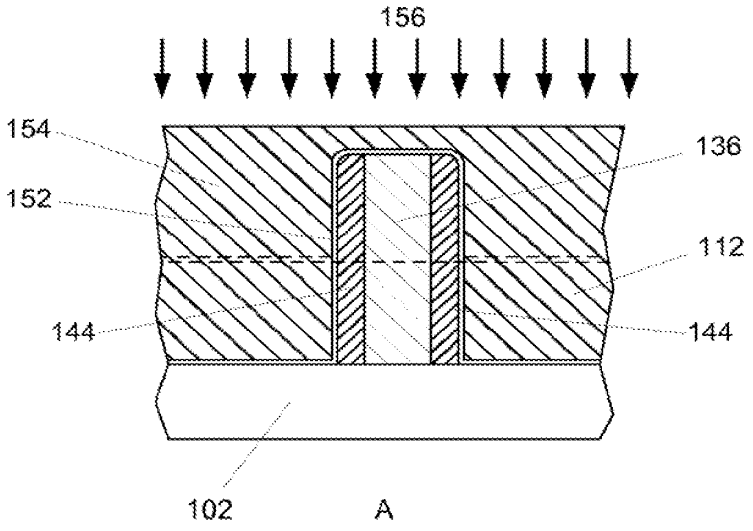

156
154
152
136
112
144
144
102
A

FIG. 12

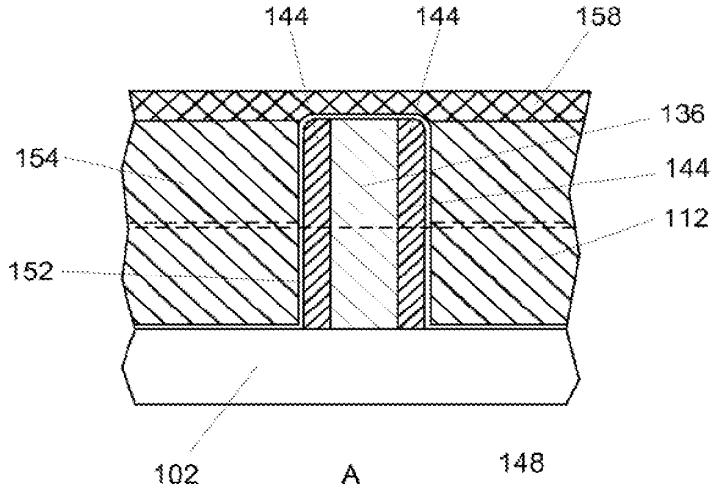

144
144
158
136
154
144
112
152
102
A
148

FIG. 13

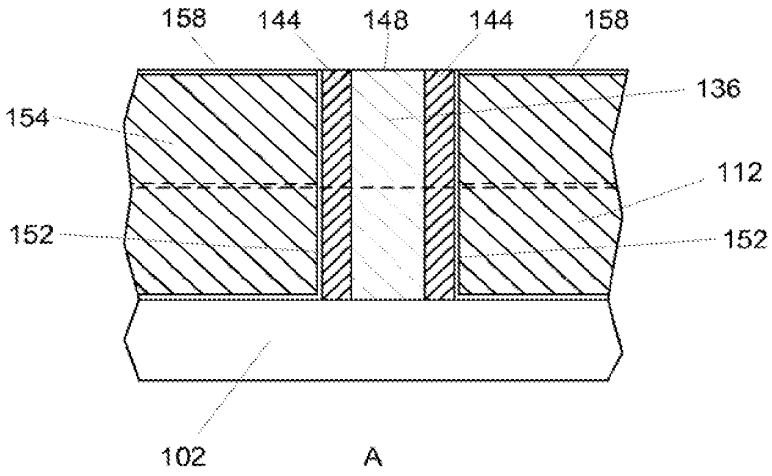

158
144
148
144
158
136
154
112
152
152
102
A

FIG. 14

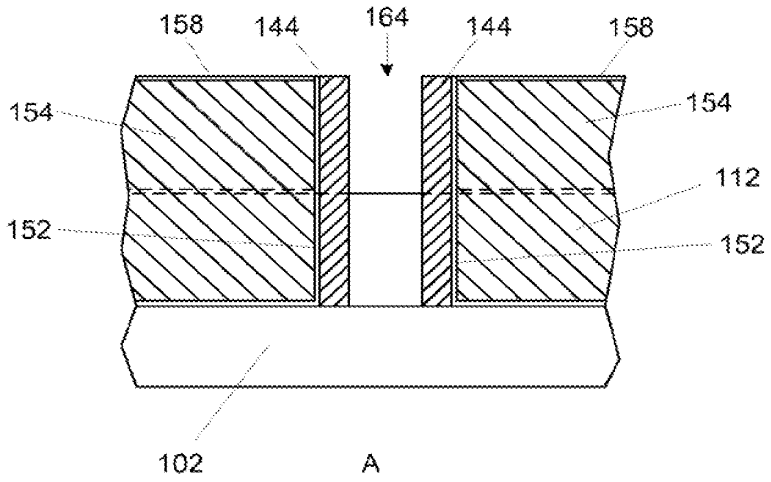

158
144
164
144
158
154
154
112
152
152
102
A

FIG. 15

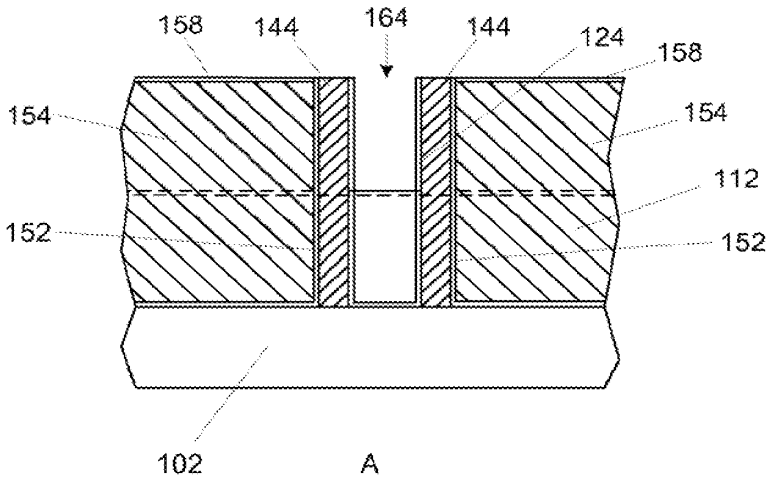

158
144
164
144
124
158
154
154
112
152
152
102
A

FIG. 16

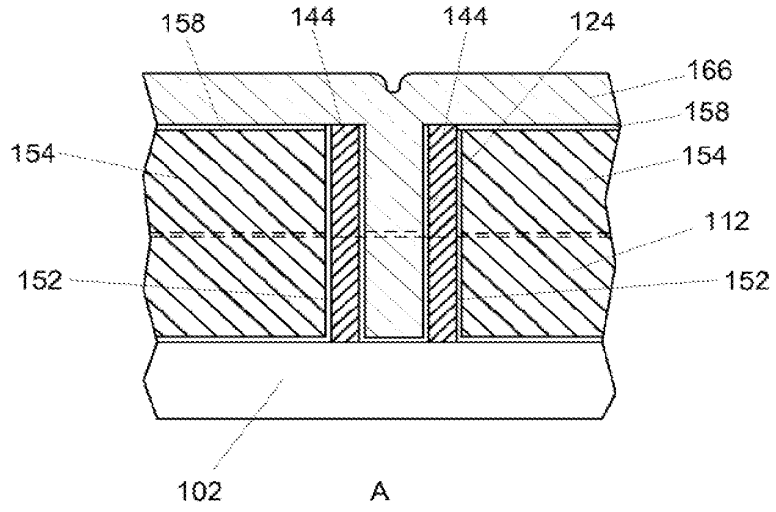

158
144
144
124
166
158
154
154
112
152
152
102
A

FIG. 17

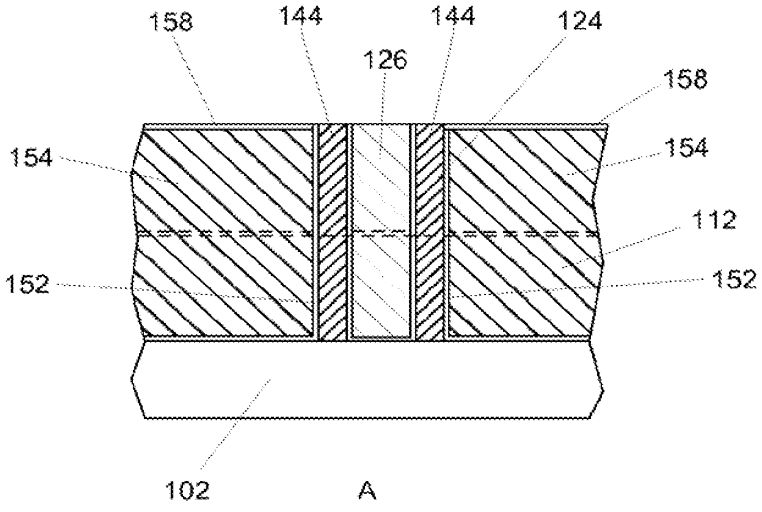

158
144
144
124
126
158
154
154
112
152
152
102
A

FIG. 18

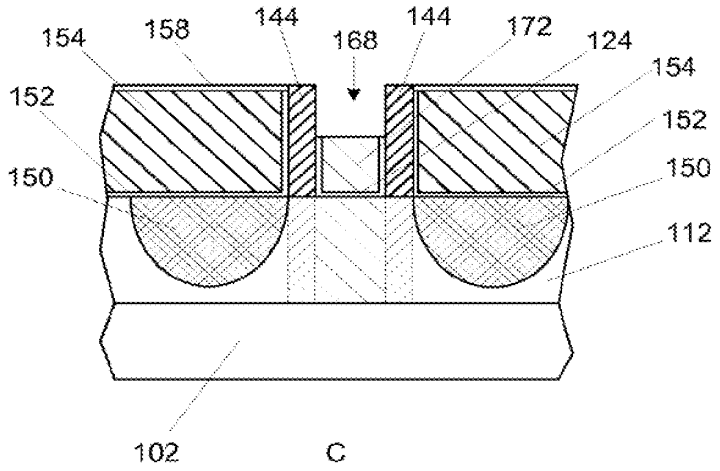

154
158
144
168
144
172
124
154
152
152
150
150
112
102
C

FIG. 19

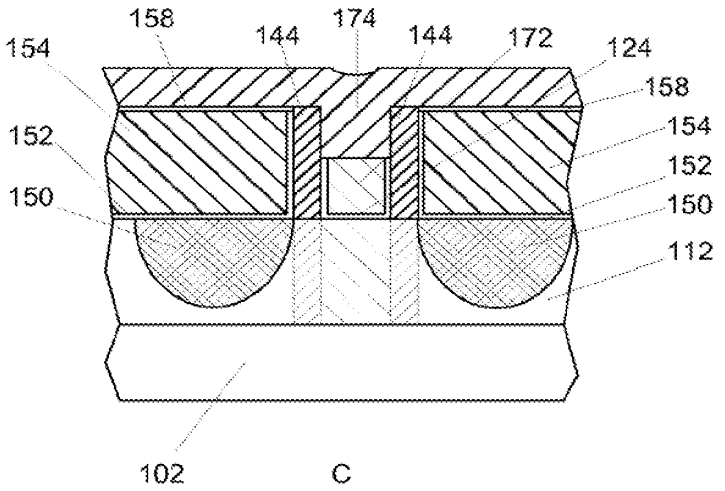

158
154
144
174
144
172
124
158
152
154
152
150
150
112
102
C

FIG. 20

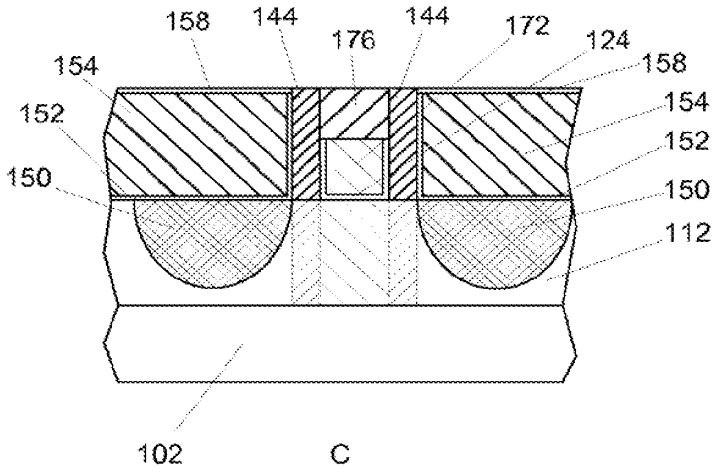

158
144
176
144
172
124
158
154
154
152
152
150
150
112
102
C

FIG. 21

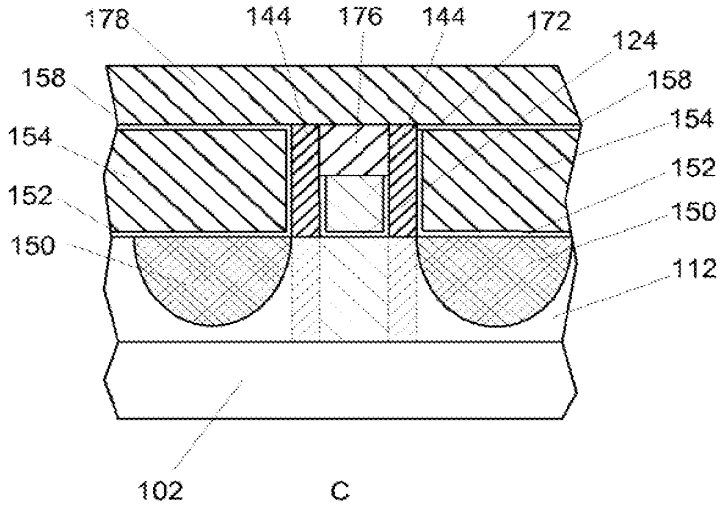

178
144
176
144
172
124
158
158
154
154
152
152
150
150
112
102
C

FIG. 22

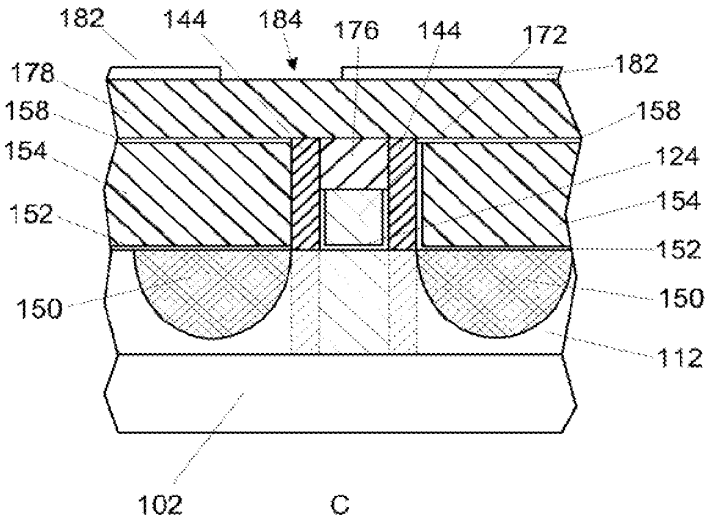

182
144
184
176
144
172
178
182
158
158
154
124
154
152
152
150
150
112
102
C

FIG. 23

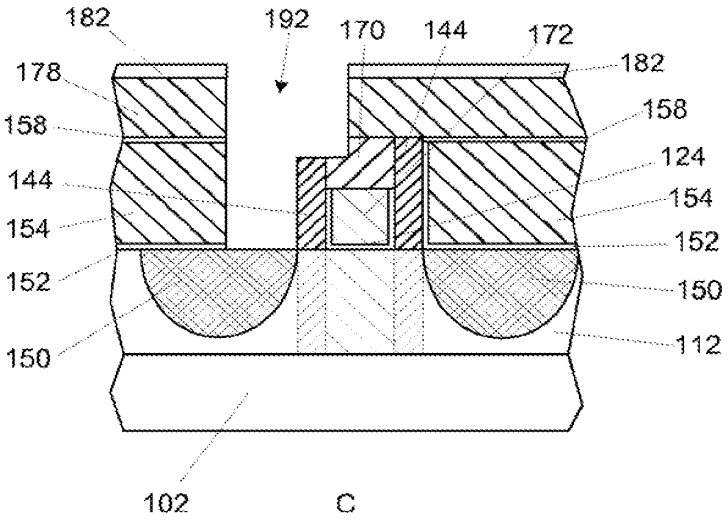

182
192
170
144
172
178
182
158
158
124
144
154
154
152
152
150
150
112
102
C

FIG. 24

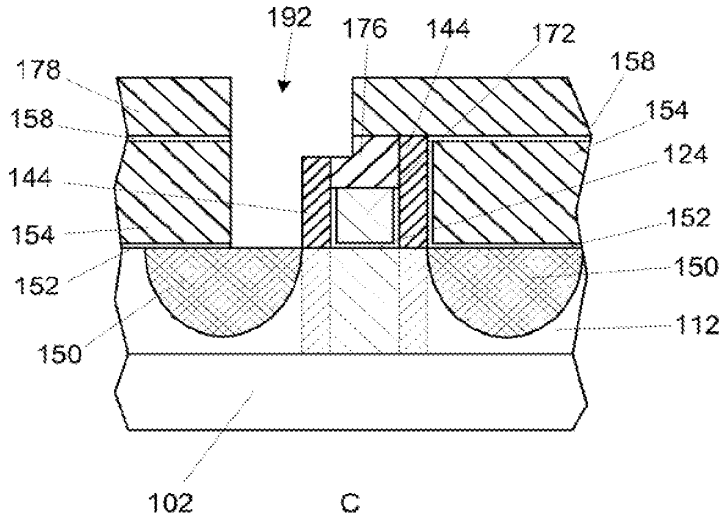

192
176
144
172
178
158
158
154
144
124
154
152
152
150
150
112
102
C

FIG. 25

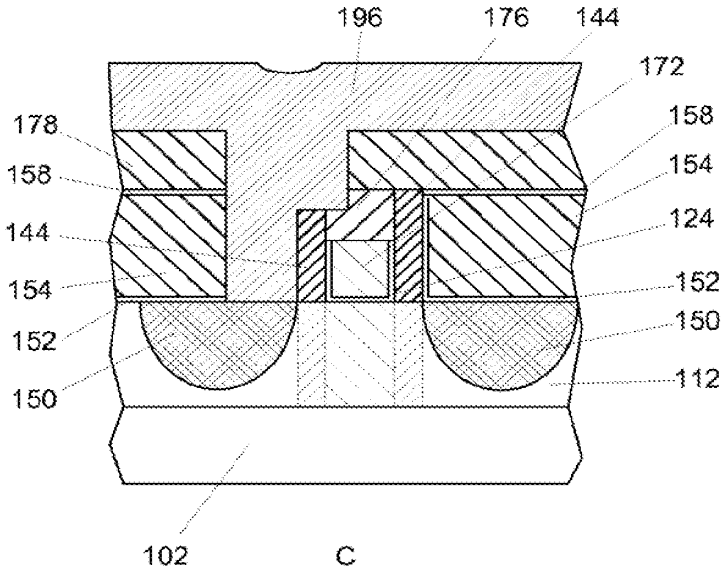

196
176
144
172
178
158
158
154
144
124
154
152
152
150
150
112
102
C

FIG. 26

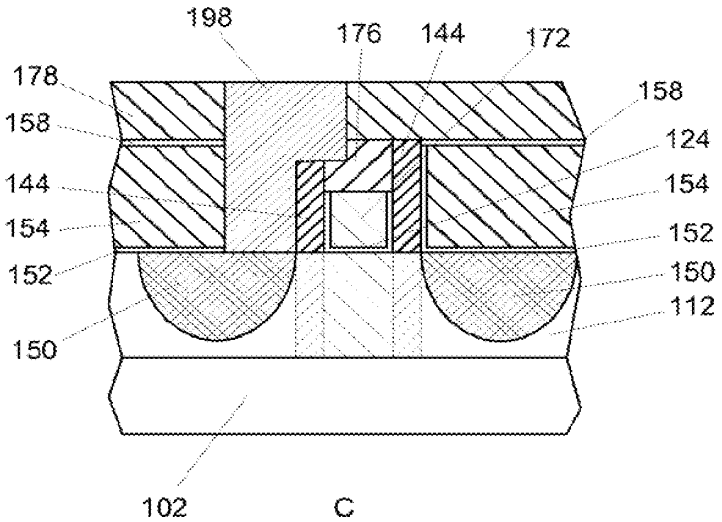

198
176
144
172
178
158
158
124
144
154
154
152
152
150
150
112
102
C

FIG. 27

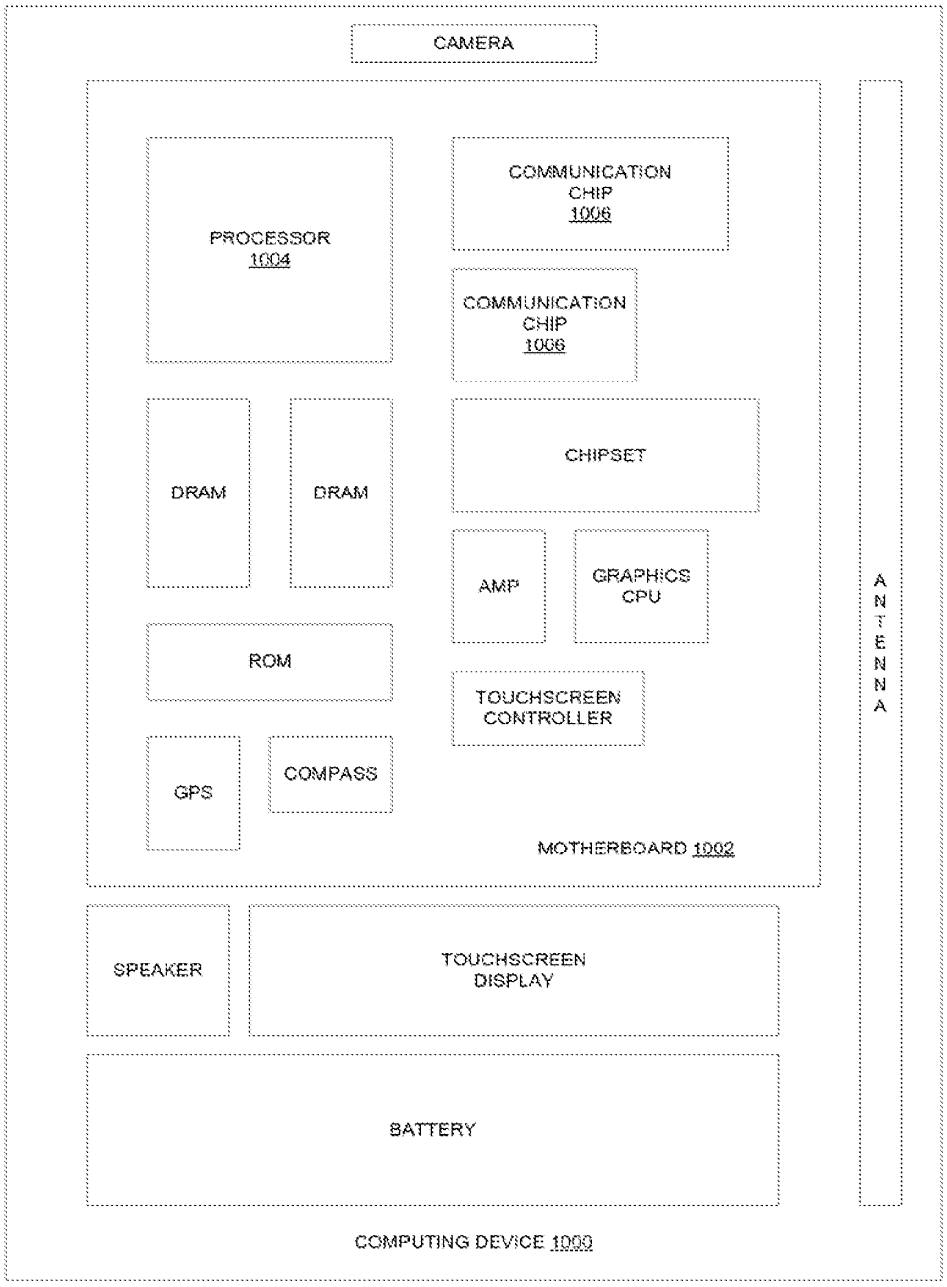

CAMERA
PROCESSOR
1004
COMMUNICATION
CHIP
1006
COMMUNICATION
CHIP
1006
DRAM
DRAM
CHIPSET
AMP
GRAPHICS
CPU
ROM
TOUCHSCREEN
CONTROLLER
GPS
COMPASS
MOTHERBOARD 1002
ANTENNA
SPEAKER
TOUCHSCREEN
DISPLAY
BATTERY
COMPUTING DEVICE 1000

FIG. 28

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2011/063433

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/336(2006.01)i, H01L 29/78(2006.01)i, H01L 21/31(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 21/336; H01L 21/8234; H01L 29/76; H01L 27/11; H01L 21/24

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: gate, dielectric, spacer, interlayer, oxidizing, annealing, tensile, electrode, capping, trench, non-planar.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	KR 10-2004-0050519 A (HYNIX SEMICONDUCTOR CO., LTD.) 16 June 2004 See abstract, page 3, claim 1 and figures 1a-1d.	1-20
A	US 2002-0130372 A1 (HYUNG-SHIN KWON et al.) 19 September 2002 See abstract, paragraphs [0025]-[0028], [0031]-[0037] and figures 10-12.	1-20
A	KR 10-2008-0021918 A (DONGBU ELECTRONICS CO., LTD.) 10 March 2008 See abstract, paragraphs [0042]-[0065], claims 1,3 and figures 3a-3j.	1-20
A	US 2006-0189058 A1 (JONG-WOOK LEE et al.) 24 August 2006 See abstract, paragraphs [0049]-[0086] and figures 7-15.	1-20

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
19 JULY 2012 (19.07.2012)	**20 JULY 2012 (20.07.2012)**

Name and mailing address of the ISA/KR
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City, 302-701, Republic of Korea
Facsimile No. 82-42-472-7140

Authorized officer
KIM, Jung Jin
Telephone No. 82-42-481-5962

Form PCT/ISA/210 (second sheet) (July 2009)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2011/063433

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
KR 10-2004-0050519 A	16.06.2004	None	
US 2002-0130372 A1	19.09.2002	KR 10-0398357 B1	26.09.2003
		US 2004-0198032 A1	07.10.2004
		US 2007-0290280 A1	20.12.2007
		US 2007-0293030 A1	20.12.2007
		US 6767814 B2	27.07.2004
		US 7385260 B2	10.06.2008
KR 10-2008-0021918 A	10.03.2008	None	
US 2006-0189058 A1	24.08.2006	KR 10-0578818 B1	11.05.2006
		US 7442598 B2	28.10.2008

Form PCT/ISA/210 (patent family annex) (July 2009)

PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

To:

WINKLE ROBERT C.

WINKLE, PLLC C/O CPA GLOBAL P.O. BOX 52050
MINNEAPOLIS MN 55402 USA

PCT

NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL SEARCH REPORT AND THE WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY, OR THE DECLARATION

(PCT Rule 44.1)

Date of mailing *(day/month/year)* 15 MAY 2012 (15.05.2012)

Applicant's or agent's file reference
P38946PCT

FOR FURTHER ACTION See paragraphs 1 and 4 below

International application No.
PCT/US2011/054294

International filing date *(day/month/year)*
30 SEPTEMBER 2011 (30.09.2011)

Applicant
INTEL CORPORATION et al

1. ☒ The applicant is hereby notified that the international search report and the written opinion of the International Searching Authority have been established and are transmitted herewith.

Filing of amendments and statement under Article 19:

The applicant is entitled, if he so wishes, to amend the claims of the international application (see Rule 46):

When? The time limit for filing such amendments is normally two months from the date of transmittal of the international search report.

Where? Directly to the International Bureau of WIPO, 34 chemin des Colombettes 1211 Geneva 20, Switzerland, Facsimile No.: +41 22 338 82 70

For more detailed instructions, see *PCT Applicant's Guide*, International Phase, paragraphs 9.004 - 9.011.

2. ☐ The applicant is hereby notified that no international search report will be established and that the declaration under Article 17(2)(a) to that effect and the written opinion of the International Searching Authority are transmitted herewith.

3. ☐ **With regard to any protest** against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that:

☐ the protest together with the decision thereon has been transmitted to the International Bureau together with any request to forward the texts of both the protest and the decision thereon to the designated Offices.

☐ no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.

4. **Reminders**

The applicant may submit comments on an informal basis on the written opinion of the International Searching Authority to the International Bureau. The International Bureau will send a copy of such comments to all designated Offices unless an international preliminary examination report has been or is to be established. Following the expiration of 30 months from the priority date, these comments will also be made available to the public.

Shortly after the expiration of **18 months** from the priority date, the international application will be published by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau before the completion of the technical preparations for international publication (Rules 90bis.1 and 90bis.3).

Within **19 months** from the priority date, but only in respect of some designated Offices, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase **until 30 months** from the priority date (in some Offices even later); otherwise, the applicant must, **within 20 months** from the priority date, perform the prescribed acts for entry into the national phase before those designated Offices.

In respect of other designated Offices, the time limit of **30 months** (or later) will apply even if no demand is filed within 19months.

For details about the applicable time limits, Office by Office, see www.wipo.int/pct/en/texts/time_limits.html and the PCT Applicant's Guide, National Chapters.

Name and mailing address of the ISA/KR
Korean Intellectual Property Office
Government Complex-Daejeon, 189 Cheongsa-ro, Seo-gu, Daejeon 302-701, Republic of Korea
Facsimile No. 82-42-472-7140

Authorized officer
COMMISSIONER

Telephone No. 82-42-48[illegible]-8754

CPA GLOBAL
MAY 22 2012
Coded _____ Verified _____

Form PCT/ISA/220 (July 2010)

* Attention

Copies of the documents cited in the international search report can be searched in the following Korean Intellectual Property Office English website for three months from the date of mailing of the international search report.

http://www.kipo.go.kr/en/ => PCT Services => PCT Services

ID : PCT international application number
PW : **7Z3LYG28**

Inquiries related to PCT International Search Report or Written Opinion prepared by KIPO as an International Searching Authority can be answered not only by KIPO but also through IPKC (Intellectual Property Korea Center), located in Vienna, VA, which functions as a PCT Help Desk for PCT applicants.

Homepage: http://www.ipkcenter.com
Email: ipkc@ipkcenter.com
Phone: +1 703 388 1066
Fax: +1 703 388 1084

Notes to Form PCT/ISA/220 (July 2010)

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference	FOR FURTHER ACTION	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
P38946PCT		
International application No.	International filing date *(day/month/year)*	(Earliest) Priority Date *(day/month/year)*
PCT/US2011/054294	**30 SEPTEMBER 2011 (30.09.2011)**	

Applicant

INTEL CORPORATION et al

This International search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 3 sheets.

☐ It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**
   a. With regard to the **language**, the international search was carried out on the basis of :
      ☒ the international application in the language in which it was filed
      ☐ a translation of the international application into _____, which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))
   b. ☐ This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6*bis*(a)).
   c. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.
2. ☐ **Certain claims were found unsearchable** (See Box No. II)
3. ☐ **Unity of invention is lacking** (See Box No. III)
4. With regard to the **title**,
   ☒ the text is approved as submitted by the applicant.
   ☐ the text has been established by this Authority to read as follows:
5. With regard to the **abstract**,
   ☒ the text is approved as submitted by the applicant.
   ☐ the text has been established, according to Rule 38.2, by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.
6. With regard to the drawings,
   a. the figure of the **drawings** to be published with the abstract is Figure No. 1
      ☒ as suggested by the applicant.
      ☐ as selected by this Authority, because the applicant failed to suggest a figure.
      ☐ as selected by this Authority, because this figure better characterizes the invention.
   b. ☐ none of the figure is to be published with the abstract

Form PCT/ISA/210 (first sheet) (July 2009)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2011/054294

A. CLASSIFICATION OF SUBJECT MATTER

H01L 29/78(2006.01)i, H01L 21/336(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 29/78; H01L 21/336; H01L 21/28; H01L 21/338; H01L 27/12

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: non-planar, tungsten and gate

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 7528025 B2 (BRASK JUSTIN K. et al.) 05 May 2009 See the abstract; figs. 1-5; column 3, line 4 ~ column 26, line 47.	1-25
A	KR 10-0585178 B1 (SAMSUNG ELECTRONICS CO., LTD.) 30 May 2006 See the abstract; figs. 1-21; claims 1-31.	1-25
A	US 2011-0147831 A1 (STEIGERWALD JOSEPH M. et al.) 23 June 2011 See the abstract; figs. 1-4; paragraphs [0009]-[0029].	1-25

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15 MAY 2012 (15.05.2012)	**15 MAY 2012 (15.05.2012)**

Name and mailing address of the ISA/KR	Authorized officer
Korean Intellectual Property Office Government Complex-Daejeon, 189 Cheongsa-ro, Seo-gu, Daejeon 302-701, Republic of Korea	Lee,Sang Ho
Facsimile No. 82-42-472-7140	Telephone No. 82-42-481-8221

Form PCT/ISA/210 (second sheet) (July 2009)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2011/054294

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 7528025 B2	05.05.2009	US 2006-0071275 A1	06.04.2006
		US 2006-0138552 A1	29.06.2006
		US 2006-0138553 A1	29.06.2006
		US 2008-0090397 A1	17.04.2008
		US 2009-0149012 A1	11.06.2009
		US 7326656 B2	05.02.2008
		US 7361958 B2	22.04.2008
		US 7531437 B2	12.05.2009
KR 10-0585178 B1	30.05.2006	US 2006-0175669 A1	10.08.2006
US 2011-0147831 A1	23.06.2011	None	

Form PCT/ISA/210 (patent family annex) (July 2009)

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:
WINKLE ROBERT C.

WINKLE, PLLC C/O CPA GLOBAL P.O. BOX 52050
MINNEAPOLIS MN 55402 USA

PCT

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43bis.1)

Date of mailing *(day/month/year)*	**15 MAY 2012 (15.05.2012)**
Applicant's or agent's file reference P38946PCT	**FOR FURTHER ACTION** See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US2011/054294	**30 SEPTEMBER 2011 (30.09.2011)**	

International Patent Classification (IPC) or both national classification and IPC

H01L 29/78(2006.01)i, H01L 21/336(2006.01)i

Applicant

INTEL CORPORATION et al

1. This opinion contains indications relating to the following items:

- [x] Box No. I Basis of the opinion
- [ ] Box No. II Priority
- [ ] Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- [ ] Box No. IV Lack of unity of invention
- [x] Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- [ ] Box No. VI Certain documents cited
- [ ] Box No. VII Certain defects in the international application
- [ ] Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1bis(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.
For further options, see Form PCT/ISA/220.

Name and mailing address of the ISA/KR	Date of completion of this opinion	Authorized officer
Korean Intellectual Property Office Government Complex-Daejeon, 189 Cheongsa-ro, Seo-gu, Daejeon 302-701, Republic of Korea Facsimile No. 82-42-472-7140	15 MAY 2012 (15.05.2012)	Lee,Sang Ho Telephone No.82-42-481-8221

Form PCT/ISA/237 (cover sheet) (July 2011)

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2011/054294

Box No. I Basis of this opinion

1. With regard to the **language**, this opinion has been established on the basis of:

   ☒ the international application in the language in which it was filed

   ☐ a translation of the international application into _____, which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(a))

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of:

   a. a sequence listing filed or furnished
      ☐ on paper
      ☐ in electronic form

   b. time of filing or furnishing
      ☐ contained in the international application as filed.
      ☐ filed together with the international application in electronic form.
      ☐ furnished subsequently to this Authority for the purposes of search.

4. ☐ In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additioanl copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2011/054294

Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Claims	1-25	YES
	Claims	NONE	NO
Inventive step (IS)	Claims	1-25	YES
	Claims	NONE	NO
Industrial applicability (IA)	Claims	1-25	YES
	Claims	NONE	NO

2. Citations and explanations :

Reference is made to the following documents:

D1: US 7528025 B2 (BRASK JUSTIN K. et al.) 05 May 2009
D2: KR 10-0585178 B1 (SAMSUNG ELECTRONICS CO., LTD.) 30 May 2006
D3: US 2011-0147831 A1 (STEIGERWALD JOSEPH M. et al.) 23 June 2011

1. Novelty and Inventive Step

1.1 claims 1-5
The subject matter of claim 1 differs from the disclosure of D1 in that the gate electrode includes a tungsten-containing gate fill material adjacent the gate fill barrier. As the subject matter of claim 1 is not shown in any other prior art documents cited in the ISR, claim 1 is not anticipated by any of the prior art documents including D1, nor obvious to the person skilled in the art.
Therefore, claim 1 is novel and involves an inventive step under PCT Article 33(2) and (3).

Claims 2-5 which are dependent on claim 1 also meet the requirements of PCT Article 33(2)-(3) with respect to novelty and inventive step.

1.2 claims 6-16
The method of claim 6 differs from the disclosure of D1 in that the second step in the method of claim 6 forms a gate electrode including the step of depositing a tungsten-containing gate fill material adjacent the gate fill barrier. As the subject matter of claim 6 is not shown in any other prior art documents cited in the ISR, claim 6 is not anticipated by any of the prior art documents including D1, nor obvious to the person skilled in the art.
Therefore, claim 6 is novel and involves an inventive step under PCT Article 33(2) and (3).

Claims 7-16 which are dependent on claim 6 also meet the requirements of PCT Article 33(2)-(3) with respect to novelty and inventive step.

1.3 claims 17-25
The method of claim 17 differs from the disclosure of D1 in that the seventh step in the method of claim 17 forms a gate electrode including the step of depositing a tungsten-containing gate fill material adjacent the gate fill barrier. As the subject matter of claim 17 is not shown in any other prior art documents cited in the ISR, claim 17 is not anticipated by any of the prior art documents including D1, nor obvious to the person skilled in the art.
Therefore, claim 17 is novel and involves an inventive step under PCT Article 33(2) and (3).

Claims 18-25 which are dependent on claim 17 also meet the requirements of PCT Article 33(2)-(3) with respect to novelty and inventive step.

2. Industrial Applicability
Claims 1-25 have industrial applicability (PCT Article 33(4)).

PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

Entered into FIP
By: M.T.

To:
BLAKELY SOKOLOFF TAYLOR&AZFMAN LLP
1279 OAKMEAD PARKWAY SUNNYVALE, CA 94086 USA

ENTERED
MAY 2 2 2012 M.T.
INTO DATABASE

RECEIVED
SUNNYVALE
MAY 21 2012
BLAKELY SOKOLOFF TAYLOR ZAFMAN

PCT

NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL SEARCH REPORT AND THE WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY, OR THE DECLARATION

(PCT Rule 44.1)

Applicant's or agent's file reference P38683PCT	Date of mailing *(day/month/year)* 15 MAY 2012 (15.05.2012)
International application No. PCT/US2011/054464	**FOR FURTHER ACTION** See paragraphs 1 and 4 below
Applicant **INTEL CORPORATION et al**	International filing date *(day/month/year)* **30 SEPTEMBER 2011 (30.09.2011)**

1. ☒ The applicant is hereby notified that the international search report and the written opinion of the International Searching Authority have been established and are transmitted herewith.

Filing of amendments and statement under Article 19:

The applicant is entitled, if he so wishes, to amend the claims of the international application (see Rule 46):

When? The time limit for filing such amendments is normally two months from the date of transmittal of the international search report.

Where? Directly to the International Bureau of WIPO, 34 chemin des Colombettes 1211 Geneva 20, Switzerland, Facsimile No.: +41 22 338 82 70

For more detailed instructions, see *PCT Applicant's Guide*, International Phase, paragraphs 9.004 - 9.011.

2. ☐ The applicant is hereby notified that no international search report will be established and that the declaration under Article 17(2)(a) to that effect and the written opinion of the International Searching Authority are transmitted herewith.

3. ☐ **With regard to any protest** against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that:

☐ the protest together with the decision thereon has been transmitted to the International Bureau together with any request to forward the texts of both the protest and the decision thereon to the designated Offices.

☐ no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.

4. **Reminders**

The applicant may submit comments on an informal basis on the written opinion of the International Searching Authority to the International Bureau. The International Bureau will send a copy of such comments to all designated Offices unless an international preliminary examination report has been or is to be established. Following the expiration of 30 months from the priority date, these comments will also be made available to the public.

Shortly after the expiration of **18 months** from the priority date, the international application will be published by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau before the completion of the technical preparations for international publication (Rules 90bis.1 and 90bis.3).

Within **19 months** from the priority date, but only in respect of some designated Offices, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase **until 30 months** from the priority date (in some Offices even later); otherwise, the applicant must, **within 20 months** from the priority date, perform the prescribed acts for entry into the national phase before those designated Offices.

In respect of other designated Offices, the time limit of **30 months** (or later) will apply even if no demand is filed within 19months.

For details about the applicable time limits, Office by Office, see www.wipo.int/pct/en/texts/time_limits.html and the PCT Applicant's Guide, National Chapters.

Name and mailing address of the ISA/KR Korean Intellectual Property Office Government Complex-Daejeon, 189 Cheongsa-ro, Seo-gu, Daejeon 302-701, Republic of Korea Facsimile No. 82-42-472-7140	Authorized officer COMMISSIONER Telephone No. 82-42-481-875

CPA GLOBAL
JUN 0 4
RECEIVED
Coded _____ Verified _____

Form PCT/ISA/220 (July 2010)

* Attention

Copies of the documents cited in the international search report can be searched in the following Korean Intellectual Property Office English website for three months from the date of mailing of the international search report.

http://www.kipo.go.kr/en/ => PCT Services => PCT Services

ID : PCT international application number
PW : **XF2JQG6C**

Inquiries related to PCT International Search Report or Written Opinion prepared by KIPO as an International Searching Authority can be answered not only by KIPO but also through IPKC (Intellectual Property Korea Center), located in Vienna, VA, which functions as a PCT Help Desk for PCT applicants.

Homepage: http://www.ipkcenter.com
Email: ipkc@ipkcenter.com
Phone: +1 703 388 1066
Fax: +1 703 388 1084

Notes to Form PCT/ISA/220 (July 2010)

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference	FOR FURTHER ACTION	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
P38683PCT		
International application No.	International filing date *(day/month/year)*	(Earliest) Priority Date *(day/month/year)*
PCT/US2011/054464	**30 SEPTEMBER 2011 (30.09.2011)**	

Applicant

INTEL CORPORATION et al

This International search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 3 sheets.

☐ It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**
   a. With regard to the **language**, the international search was carried out on the basis of:
      ☒ the international application in the language in which it was filed
      ☐ a translation of the international application into _____, which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))
   b. ☐ This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6*bis*(a)).
   c. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.
2. ☐ **Certain claims were found unsearchable** (See Box No. II)
3. ☐ **Unity of invention is lacking** (See Box No. III)
4. With regard to the **title,**
   ☒ the text is approved as submitted by the applicant.
   ☐ the text has been established by this Authority to read as follows:

5. With regard to the **abstract,**
   ☒ the text is approved as submitted by the applicant.
   ☐ the text has been established, according to Rule 38.2, by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.
6. With regard to the drawings,
   a. the figure of the **drawings** to be published with the abstract is Figure No. 1
      ☒ as suggested by the applicant.
      ☐ as selected by this Authority, because the applicant failed to suggest a figure.
      ☐ as selected by this Authority, because this figure better characterizes the invention.
   b. ☐ none of the figure is to be published with the abstract.

Form PCT/ISA/210 (first sheet) (July 2009)