INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2011/054464

A. CLASSIFICATION OF SUBJECT MATTER

H01L 29/78(2006.01)i, H01L 21/336(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 29/78; H01L 21/336; H01L 21/306; H01L 21/28; H01L 21/335

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: capping, dielectric, and transistor

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2008-0233699 A1 (BOOTH ROGER ALLEN et al.) 25 September 2008 See the abstract; figs. 1-11; paragraphs [0016]-[0036].	1-25
A	US 2010-0048007 A1 (LEE SHEN-NAN et al.) 25 February 2010 See the abstract; figs. 1-3; paragraphs [0011]-[0039].	1-25
A	KR 10-0653711 B1 (SAMSUNG ELECTRONICS CO., LTD.) 05 December 2006 See the abstract; figs. 1-12; claims 1-23.	1-25

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15 MAY 2012 (15.05.2012)	**15 MAY 2012 (15.05.2012)**
Name and mailing address of the ISA/KR Korean Intellectual Property Office Government Complex-Daejeon, 189 Cheongsa-ro, Seo-gu, Daejeon 302-701, Republic of Korea Facsimile No. 82-42-472-7140	Authorized officer Lee,Sang Ho Telephone No. 82-42-481-8221

Form PCT/ISA/210 (second sheet) (July 2009)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2011/054464

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2008-0233699 A1	25.09.2008	CN 101097956 A	02.01.2008
		CN 101097956 C0	02.01.2008
		JP 2008-010876 A	17.01.2008
		TW 200807717 A	01.02.2008
		US 2008-0001187 A1	03.01.2008
		US 2008-0042219 A1	21.02.2008
		US 2008-0142891 A1	19.06.2008
		US 7517764 B2	14.04.2009
		US 7667248 B2	23.02.2010
		US 7863122 B2	04.01.2011
US 2010-0048007 A1	25.02.2010	CN 101659034 A	03.03.2010
		CN 101659034 B	09.11.2011
		TW 201009925 A	01.03.2010
		US 8153526 B2	10.04.2012
KR 10-0653711 B1	05.12.2006	US 2007-0111435 A1	17.05.2007
		US 2010-0197099 A1	05.08.2010
		US 7723762 B2	25.05.2010
		US 7851287 B2	14.12.2010

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:
BLAKELY SOKOLOFF TAYLOR&AZFMAN LLP

1279 OAKMEAD PARKWAY SUNNYVALE, CA 94086
USA

PCT

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43bis.1)

Date of mailing *(day/month/year)*	**15 MAY 2012 (15.05.2012)**
Applicant's or agent's file reference P38683PCT	**FOR FURTHER ACTION** See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US2011/054464	**30 SEPTEMBER 2011 (30.09.2011)**	

International Patent Classification (IPC) or both national classification and IPC

H01L 29/78(2006.01)i, H01L 21/336(2006.01)i

ENTERED
MAY 22 2012 M.T.

Applicant

INTEL CORPORATION et al

Entered into FIP
By: M.T.
INTO DATABASE

1. This opinion contains indications relating to the following items:

- [X] Box No. I Basis of the opinion
- [ ] Box No. II Priority
- [ ] Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- [ ] Box No. IV Lack of unity of invention
- [X] Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- [ ] Box No. VI Certain documents cited
- [ ] Box No. VII Certain defects in the international application
- [ ] Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1bis(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.
For further options, see Form PCT/ISA/220.

Name and mailing address of the ISA/KR	Date of completion of this opinion	Authorized officer
Korean Intellectual Property Office Government Complex-Daejeon, 189 Cheongsa-ro, Seo-gu, Daejeon 302-701, Republic of Korea Facsimile No. 82-42-472-7140	15 MAY 2012 (15.05.2012)	Lee,Sang Ho Telephone No.82-42-481-8221

Form PCT/ISA/237 (cover sheet) (July 2011)

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2011/054464

Box No. I Basis of this opinion

1. With regard to the **language**, this opinion has been established on the basis of :

   ☒ the international application in the language in which it was filed

   ☐ a translation of the international application into _____, which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(a))

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of:

   a. a sequence listing filed or furnished
      ☐ on paper
      ☐ in electronic form

   b. time of filing or furnishing
      ☐ contained in the international application as filed
      ☐ filed together with the international application in electronic form.
      ☐ furnished subsequently to this Authority for the purposes of search.

4. ☐ In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additioanl copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2011/054464

Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Claims	1-25	YES
	Claims	NONE	NO
Inventive step (IS)	Claims	1-25	YES
	Claims	NONE	NO
Industrial applicability (IA)	Claims	1-25	YES
	Claims	NONE	NO

2. Citations and explanations :

Reference is made to the following documents:

D1: US 2008-0233699 A1 (BOOTH ROGER ALLEN et al.) 25 September 2008
D2: US 2010-0048007 A1 (LEE SHEN-NAN et al.) 25 February 2010
D3: KR 10-0653711 B1 (SAMSUNG ELECTRONICS CO., LTD.) 05 December 2006

1. Novelty and Inventive Step

1.1 claims 1-4
The subject matter of claim 1 differs from the disclosure of D1 in that the transistor gate comprises a substantially void free capping dielectric structure disposed adjacent the recessed gate electrode and between the pair of gate spacers. As the subject matter of claim 1 is not shown in any other prior art documents cited in the ISR, claim 1 is not anticipated by any of the prior art documents including D1, nor obvious to the person skilled in the art.
Therefore, claim 1 is novel and involves an inventive step under PCT Article 33(2) and (3).

Claims 2-4 which are dependent on claim 1 also meet the requirements of PCT Article 33(2)-(3) with respect to novelty and inventive step.

1.2 claims 5-9
The subject matter of claim 5 differs from the disclosure of D1 in that the microelectronic device comprises at least one dielectric material layer over the source/drain region, the non-planar transistor gate spacers, and the substantially void free capping dielectric structure. As the subject matter of claim 5 is not shown in any other prior art documents cited in the ISR, claim 5 is not anticipated by any of the prior art documents including D1, nor obvious to the person skilled in the art.
Therefore, claim 5 is novel and involves an inventive step under PCT Article 33(2) and (3).

Claims 6-9 which are dependent on claim 5 also meet the requirements of PCT Article 33(2)-(3) with respect to novelty and inventive step.

1.3 claims 10-14
The method of fabricating a transistor gate of claim 10 differs from the disclosure of D1 in that the third step in the method of claim 10 comprises high density plasma depositing a capping dielectric structure on a top surface of the recessed gate electrode and between the pair of gate spacers. As the subject matter of claim 10 is not shown in any other prior art documents cited in the ISR, claim 10 is not anticipated by any of the prior art documents including D1, nor obvious to the person skilled in the art.
Therefore, claim 10 is novel and involves an inventive step under PCT Article 33(2) and (3).

Claims 11-14 which are dependent on claim 10 also meet the requirements of PCT Article 33(2)-(3) with respect to novelty and inventive step.

(Continued on the Supplemental Box.)

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.
Continuation of:

Box V.

1.4 claims 15-25
The method of claim 15 differs from the disclosure of D1 in that the ninth step in the method of claim 15 forms a capping dielectric structure within the recess by high density plasma depositing a dielectric material. As the subject matter of claim 15 is not shown in any other prior art documents cited in the ISR, claim 15 is not anticipated by any of the prior art documents including D1, nor obvious to the person skilled in the art.
Therefore, claim 15 is novel and involves an inventive step under PCT Article 33(2) and (3).

Claims 16-25 which are dependent on claim 15 also meet the requirements of PCT Article 33(2)-(3) with respect to novelty and inventive step.

2. Industrial Applicability
Claims 1-25 have industrial applicability (PCT Article 33(4)).

PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

To:

WINKLE ROBERT G.

WINKLE, PLLC C/O CPA GLOBAL P.O. BOX 52050
MINNEAPOLIS MN 55402 USA

PCT

NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL SEARCH REPORT AND THE WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY, OR THE DECLARATION

(PCT Rule 44.1)

	Date of mailing *(day/month/year)* 16 MAY 2012 (16.05.2012)
Applicant's or agent's file reference P38682PCT	**FOR FURTHER ACTION** See paragraphs 1 and 4 below
International application No. **PCT/US2011/054479**	International filing date *(day/month/year)* **01 OCTOBER 2011 (01.10.2011)**

Applicant

INTEL CORPORATION et al

1. ☒ The applicant is hereby notified that the international search report and the written opinion of the International Searching Authority have been established and are transmitted herewith.

Filing of amendments and statement under Article 19:

The applicant is entitled, if he so wishes, to amend the claims of the international application (see Rule 46):

When? The time limit for filing such amendments is normally two months from the date of transmittal of the international search report.

Where? Directly to the International Bureau of WIPO, 34 chemin des Colombettes 1211 Geneva 20, Switzerland, Facsimile No.: +41 22 338 82 70

For more detailed instructions, see *PCT Applicant's Guide*, International Phase, paragraphs 9.004 , 9.011.

2. ☐ The applicant is hereby notified that no international search report will be established and that the declaration under Article 17(2)(a) to that effect and the written opinion of the International Searching Authority are transmitted herewith.

3. ☐ **With regard to any protest** against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that:

☐ the protest together with the decision thereon has been transmitted to the International Bureau together with any request to forward the texts of both the protest and the decision thereon to the designated Offices.

☐ no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.

4 **Reminders**

The applicant may submit comments on an informal basis on the written opinion of the International Searching Authority to the International Bureau. The International Bureau will send a copy of such comments to all designated Offices unless an international preliminary examination report has been or is to be established. Following the expiration of 30 months from the priority date, these comments will also be made available to the public.

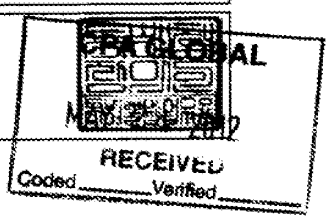
Shortly after the expiration of **18 months** from the priority date, the international application will be published by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau before the completion of the technical preparations for international publication (Rules 90bis.1 and 90bis.3).

Within **19 months** from the priority date, but only in respect of some designated Offices, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase **until 30 months** from the priority date (in some Offices even later); otherwise, the applicant must, **within 20 months** from the priority date, perform the prescribed acts for entry into the national phase before those designated Offices.

In respect of other designated Offices, the time limit of **30 months** (or later) will apply even if no demand is filed within 19months.

For details about the applicable time limits, Office by Office, see www.wipo.int/pct/en/texts/time_limits.html and the PCT Applicant's Guide, National Chapters.

Name and mailing address of the ISA/KR Korean Intellectual Property Office Government Complex-Daejeon, 189 Cheongsa-ro, Seo-gu, Daejeon 302-701, Republic of Korea Facsimile No. 82-42-472-7140	Authorized officer COMMISSIONER Telephone No. 82-42-481-8754



Form PCT/ISA/220 (July 2010)

* Attention

Copies of the documents cited in the international search report can be searched in the following Korean Intellectual Property Office English website for three months from the date of mailing of the international search report.

http://www.kipo.go.kr/en/ => PCT Services => PCT Services

ID : PCT international application number
PW : **USJHFVQV**

Inquiries related to PCT International Search Report or Written Opinion prepared by KIPO as an International Searching Authority can be answered not only by KIPO but also through IPKC (Intellectual Property Korea Center), located in Vienna, VA, which functions as a PCT Help Desk for PCT applicants.

Homepage: http://www.ipkcenter.com
Email: ipkc@ipkcenter.com
Phone: +1 703 388 1066
Fax: +1 703 388 1084

Notes to Form PCT/ISA/220 (July 2010)

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference	FOR FURTHER ACTION	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
P38682PCT		
International application No.	International filing date *(day/month/year)*	(Earliest) Priority Date *(day/month/year)*
PCT/US2011/054479	**01 OCTOBER 2011 (01.10.2011)**	

Applicant

INTEL CORPORATION et al

This International search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 3 sheets.

☐ It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**
   a. With regard to the **language**, the international search was carried out on the basis of :
      ☒ the international application in the language in which it was filed
      ☐ a translation of the international application into _____, which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))
   b. ☐ This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6*bis*(a)).
   c. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.
2. ☐ **Certain claims were found unsearchable** (See Box No. II)
3. ☐ **Unity of invention is lacking** (See Box No. III)
4. With regard to the **title**,
   ☒ the text is approved as submitted by the applicant.
   ☐ the text has been established by this Authority to read as follows:
5. With regard to the **abstract**,
   ☒ the text is approved as submitted by the applicant.
   ☐ the text has been established, according to Rule 38.2, by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.
6. With regard to the drawings,
   a. the figure of the **drawings** to be published with the abstract is Figure No. 1
      ☒ as suggested by the applicant.
      ☐ as selected by this Authority, because the applicant failed to suggest a figure.
      ☐ as selected by this Authority, because this figure better characterizes the invention.
   b. ☐ none of the figure is to be published with the abstract.

Form PCT/ISA/210 (first sheet) (July 2009)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2011/054479

A. CLASSIFICATION OF SUBJECT MATTER

H01L 29/78(2006.01)i, H01L 21/336(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 29/78; H01L 21/4763; H01L 21/336; H01L 29/94; H01L 29/76; H01L 27/12

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: titanium, non-planar, and transistor

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 7456471 B2 (ANDERSON BRENT A. et al.) 25 November 2008 See the abstract; figs. 1-24; column 5, line 45 - column 11, line 55.	1-24
A	US 06136697 A (WU; SHYE-LIN) 24 October 2000 See the abstract; figs. 1-11; column 3, line 40 - column 51, line 41.	1-24
A	KR 10-0585178 B1 (SAMSUNG ELECTRONICS CO., LTD.) 24 May 2006 See the abstract; figs. 1-21; claims 1-31.	1-24

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15 MAY 2012 (15.05.2012)	**16 MAY 2012 (16.05.2012)**
Name and mailing address of the ISA/KR Korean Intellectual Property Office Government Complex-Daejeon, 189 Cheongsa-ro, Seo-gu, Daejeon 302-701, Republic of Korea Facsimile No. 82-42-472-7140	Authorized officer Lee,Sang Ho Telephone No. 82-42-481-8221

Form PCT/ISA/210 (second sheet) (July 2009)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2011/054479

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 7456471 B2	25.11.2008	EP 2070110 A2	17.06.2009
		JP 2010-503997 A	04.02.2010
		JP 2010-503997 T	04.02.2010
		KR 10-1104040 B1	06.01.2012
		KR 2009-0075822 A	09.07.2009
		US 2008-0067613 A1	20.03.2008
		US 2008-0286913 A1	20.11.2008
		US 7851283 B2	14.12.2010
		WO 2008-033982 A2	20.03.2008
		WO 2008-033982 A3	05.06.2008
		WO 2008-033982 A3	20.03.2008
US 06136697 A	24.10.2000	None	
KR 10-0585178 B1	30.05.2006	US 2006-0175669 A1	10.08.2006

Form PCT/ISA/210 (patent family annex) (July 2009)

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:
WINKLE ROBERT G.

WINKLE, PLLC C/O CPA GLOBAL P.O. BOX 52050
MINNEAPOLIS MN 55402 USA

PCT

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43bis.1)

Date of mailing *(day/month/year)*	**16 MAY 2012 (16.05.2012)**
Applicant's or agent's file reference P38682PCT	**FOR FURTHER ACTION** See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US2011/054479	**01 OCTOBER 2011 (01.10.2011)**	

International Patent Classification (IPC) or both national classification and IPC

H01L 29/78(2006.01)i, H01L 21/336(2006.01)i

Applicant

INTEL CORPORATION et al

1. This opinion contains indications relating to the following items:

- [x] Box No. I Basis of the opinion
- [ ] Box No. II Priority
- [ ] Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- [ ] Box No. IV Lack of unity of invention
- [x] Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- [ ] Box No. VI Certain documents cited
- [ ] Box No. VII Certain defects in the international application
- [ ] Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1bis(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.
For further options, see Form PCT/ISA/220.

Name and mailing address of the ISA/KR	Date of completion of this opinion	Authorized officer
Korean Intellectual Property Office Government Complex-Daejeon, 189 Cheongsa-ro, Seo-gu, Daejeon 302-701, Republic of Korea Facsimile No. 82-42-472-7140	15 MAY 2012 (15.05.2012)	Lee,Sang Ho Telephone No.82-42-481-8221

Form PCT/ISA/237 (cover sheet) (July 2011)

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2011/054479

Box No. 1 Basis of this opinion

1. With regard to the **language**, this opinion has been established on the basis of :

   ☒ the international application in the language in which it was filed

   ☐ a translation of the international application into _____, which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(a))

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of:

   a. a sequence listing filed or furnished
      ☐ on paper
      ☐ in electronic form

   b. time of filing or furnishing
      ☐ contained in the international application as filed.
      ☐ filed together with the international application in electronic form.
      ☐ furnished subsequently to this Authority for the purposes of search.

4. ☐ In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additioanl copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2011/054479

Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Claims	1-24	YES
	Claims	NONE	NO
Inventive step (IS)	Claims	1-24	YES
	Claims	NONE	NO
Industrial applicability (IA)	Claims	1-24	YES
	Claims	NONE	NO

2. Citations and explanations :

Reference is made to the following documents:

D1: US 7456471 B2 (ANDERSON BRENT A. et al.) 25 November 2008
D2: US 06136697 A (WU; SHYE-LIN) 24 October 2000
D3: KR 10-0585178 B1 (SAMSUNG ELECTRONICS CO., LTD.) 24 May 2006

1. Novelty and Inventive Step

1.1 claims 1-4
The subject matter of claim 1 differs from the disclosure of D1 in that a microelectronic device comprises a titanium silicide interface disposed between the silicon-containing source/drain region and the titanium containing contact interface layer. As the subject matter of claim 1 is not shown in any other prior art documents cited in the ISR, claim 1 is not anticipated by any of the prior art documents including D1, nor obvious to the person skilled in the art.
Therefore, claim 1 is novel and involves an inventive step under PCT Article 33(2) and (3).

Claims 2-4 which are dependent on claim 1 also meet the requirements of PCT Article 33(2)-(3) with respect to novelty and inventive step.

1.2 claims 5-10
The subject matter of claim 5 differs from the disclosure of D1 in that the microelectronic device comprises a source/drain contact extending through a portion of the at least one dielectric material layer and comprising a conductive contact material and a titanium containing contact interface layer disposed between conductive contact material and the silicon-containing source/drain region. As the subject matter of claim 5 is not shown in any other prior art documents cited in the ISR, claim 5 is not anticipated by any of the prior art documents including D1, nor obvious to the person skilled in the art.
Therefore, claim 5 is novel and involves an inventive step under PCT Article 33(2) and (3).

Claims 6-10 which are dependent on claim 5 also meet the requirements of PCT Article 33(2)-(3) with respect to novelty and inventive step.

(Continued on the Supplemental Box.)

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2011/054479

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.
Continuation of :

Box V.

1.3 claims 11-15
The method of fabricating a microelectronic device of claim 11 differs from the disclosure of D1 in that the fourth step in the method of claim 11 comprises conformally deposits a titanium-containing contact interface layer within the contact opening to abut the silicon-containing source/drain region. As the subject matter of claim 11 is not shown in any other prior art documents cited in the ISR, claim 11 is not anticipated by any of the prior art documents including D1, nor obvious to the person skilled in the art.
Therefore, claim 11 is novel and involves an inventive step under PCT Article 33(2) and (3).

Claims 12-15 which are dependent on claim 11 also meet the requirements of PCT Article 33(2)-(3) with respect to novelty and inventive step.

1.4 claims 16-24
The method of claim 16 differs from the disclosure of D1 in that the eleventh step in the method of claim 16 comprises conformally deposits a titanium-containing contact interface layer within the contact opening to abut the silicon-containing source/drain region. As the subject matter of claim 16 is not shown in any other prior art documents cited in the ISR, claim 16 is not anticipated by any of the prior art documents including D1, nor obvious to the person skilled in the art.
Therefore, claim 16 is novel and involves an inventive step under PCT Article 33(2) and (3).

Claims 17-24 which are dependent on claim 16 also meet the requirements of PCT Article 33(2)-(3) with respect to novelty and inventive step.

2. Industrial Applicability
Claims 1-24 have industrial applicability (PCT Article 33(4)).

PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

To:

WINKLE ROBERT

WINKLE, PLLC C/O CPA GLOBAL P.O. BOX 52050
MINNEAPOLIS MN 55402 USA

PCT

NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL SEARCH REPORT AND THE WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY, OR THE DECLARATION

(PCT Rule 44.1)

	Date of mailing *(day/month/year)* 20 JULY 2012 (20.07.2012)
Applicant's or agent's file reference P38684PCT	**FOR FURTHER ACTION** See paragraphs 1 and 4 below
International application No. **PCT/US2011/063433**	International filing date *(day/month/year)* **06 DECEMBER 2011 (06.12.2011)**

Applicant

INTEL CORPORATION et al

1. ☒ The applicant is hereby notified that the international search report and the written opinion of the International Searching Authority have been established and are transmitted herewith.

   Filing of amendments and statement under Article 19:

   The applicant is entitled, if he so wishes, to amend the claims of the international application (see Rule 46):

   When? The time limit for filing such amendments is normally two months from the date of transmittal of the international search report.

   Where? Directly to the International Bureau of WIPO, 34 chemin des Colombettes 1211 Geneva 20, Switzerland, Facsimile No.: +41 22 338 82 70

   For more detailed instructions, see *PCT Applicant's Guide*, International Phase, paragraphs 9.004 , 9.011.

2. ☐ The applicant is hereby notified that no international search report will be established and that the declaration under Article 17(2)(a) to that effect and the written opinion of the International Searching Authority are transmitted herewith.

3. ☐ **With regard to any protest** against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that.

   ☐ the protest together with the decision thereon has been transmitted to the International Bureau together with any request to forward the texts of both the protest and the decision thereon to the designated Offices.

   ☐ no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.

4. **Reminders**

The applicant may submit comments on an informal basis on the written opinion of the International Searching Authority to the International Bureau. The International Bureau will send a copy of such comments to all designated Offices unless an international preliminary examination report has been or is to be established. Following the expiration of 30 months from the priority date, these comments will also be made available to the public.

Shortly after the expiration of **18 months** from the priority date, the international application will be published by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau before the completion of the technical preparations for international publication (Rules 90bis.1 and 90bis.3).

Within **19 months** from the priority date, but only in respect of some designated Offices, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase **until 30 months** from the priority date (in some Offices even later); otherwise, the applicant must, **within 20 months** from the priority date, perform the prescribed acts for entry into the national phase before those designated Offices.

In respect of other designated Offices, the time limit of **30 months** (or later) will apply even if no demand is filed within 19months.

For details about the applicable time limits, Office by Office, see www.wipo.int/pct/en/texts/time_limits.html and the PCT Applicant's Guide, National Chapters.

Name and mailing address of the ISA/KR Korean Intellectual Property Office 189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City, 302-701, Republic of Korea Facsimile No. 82-42-472-7140	Authorized officer COMMISSIONER Telephone No. 82-42-481-8753

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JUL 31 201
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Coded Verified

Form PCT/ISA/220 (July 2010)

* Attention

Copies of the documents cited in the international search report can be searched in the following Korean Intellectual Property Office English website for three months from the date of mailing of the international search report.

http://www.kipo.go.kr/en/ => PCT Services => PCT Services

ID : PCT international application number
PW : **EY3CAL8P**

Inquiries related to PCT International Search Report or Written Opinion prepared by KIPO as an International Searching Authority can be answered not only by KIPO but also through IPKC (Intellectual Property Korea Center), located in Vienna, VA, which functions as a PCT Help Desk for PCT applicants.

Homepage: http://www.ipkcenter.com
Email: ipkc@ipkcenter.com
Phone: +1 703 388 1066
Fax: +1 703 388 1084

Notes to Form PCT/ISA/220 (July 2010)

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference	FOR FURTHER ACTION	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
P38684PCT		
International application No.	International filing date *(day/month/year)*	(Earliest) Priority Date *(day/month/year)*
PCT/US2011/063433	**06 DECEMBER 2011 (06.12.2011)**	

Applicant

INTEL CORPORATION et al

This International search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 3 sheets.

☐ It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**
   a. With regard to the **language**, the international search was carried out on the basis of :
      ☒ the international application in the language in which it was filed
      ☐ a translation of the international application into _____, which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))
   b. ☐ This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6*bis*(a)).
   c. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.
2. ☐ **Certain claims were found unsearchable** (See Box No. II)
3. ☐ **Unity of invention is lacking** (See Box No. III)
4. With regard to the **title**,
   ☒ the text is approved as submitted by the applicant.
   ☐ the text has been established by this Authority to read as follows:
5. With regard to the **abstract**,
   ☒ the text is approved as submitted by the applicant.
   ☐ the text has been established, according to Rule 38.2, by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.
6. With regard to the drawings,
   a. the figure of the **drawings** to be published with the abstract is Figure No. 1
      ☒ as suggested by the applicant.
      ☐ as selected by this Authority, because the applicant failed to suggest a figure.
      ☐ as selected by this Authority, because this figure better characterizes the invention.
   b. ☐ none of the figure is to be published with the abstract.

Form PCT/ISA/210 (first sheet) (July 2009)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2011/063433

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/336(2006.01)i, H01L 29/78(2006.01)i, H01L 21/31(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 21/336; H01L 21/8234; H01L 29/76; H01L 27/11; H01L 21/24

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: gate, dielectric, spacer, interlayer, oxidizing, annealing, tensile, electrode, capping, trench, non-planar.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	KR 10-2004-0050519 A (HYNIX SEMICONDUCTOR CO., LTD.) 16 June 2004 See abstract, page 3, claim 1 and figures 1a-1d.	1-20
A	US 2002-0130372 A1 (HYUNG-SHIN KWON et al.) 19 September 2002 See abstract, paragraphs [0026]-[0028], [0031]-[0037] and figures 10-12.	1-20
A	KR 10-2008-0021918 A (DONGBU ELECTRONICS CO., LTD.) 10 March 2008 See abstract, paragraphs [0042]-[0065], claims 1,3 and figures 3a-3j.	1-20
A	US 2006-0189058 A1 (JONG-WOOK LEE et al.) 24 August 2006 See abstract, paragraphs [0049]-[0086] and figures 7-15.	1-20

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
19 JULY 2012 (19.07.2012)	**20 JULY 2012 (20.07.2012)**

Name and mailing address of the ISA/KR	Authorized officer
Korean Intellectual Property Office 189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City, 302-701, Republic of Korea Facsimile No. 82-42-472-7140	KIM, Jung Jin Telephone No. 82-42-481-5962

Form PCT/ISA/210 (second sheet) (July 2009)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2011/063433

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
KR 10-2004-0050519 A	16.06.2004	None	
US 2002-0130372 A1	19.09.2002	KR 10-0399357 B1	26.09.2003
		US 2004-0198032 A1	07.10.2004
		US 2007-0290280 A1	20.12.2007
		US 2007-0293030 A1	20.12.2007
		US 6767814 B2	27.07.2004
		US 7385260 B2	10.06.2008
KR 10-2008-0021918 A	10.03.2008	None	
US 2006-0189058 A1	24.08.2006	KR 10-0578818 B1	11.05.2006
		US 7442596 B2	28.10.2008

Form PCT/ISA/210 (patent family annex) (July 2009)

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:
WINKLE ROBERT

WINKLE, PLLC C/O CPA GLOBAL P.O. BOX 52050
MINNEAPOLIS MN 55402 USA

PCT

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43bis.1)

Date of mailing *(day/month/year)*	**20 JULY 2012 (20.07.2012)**
Applicant's or agent's file reference P38684PCT	**FOR FURTHER ACTION** See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US2011/063433	**06 DECEMBER 2011 (06.12.2011)**	

International Patent Classification (IPC) or both national classification and IPC

H01L 21/336(2006.01)i, H01L 29/78(2006.01)i, H01L 21/31(2006.01)i

Applicant

INTEL CORPORATION et al

1. This opinion contains indications relating to the following items:

- [x] Box No. I Basis of the opinion
- [ ] Box No. II Priority
- [ ] Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- [ ] Box No. IV Lack of unity of invention
- [x] Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability, citations and explanations supporting such statement
- [ ] Box No. VI Certain documents cited
- [ ] Box No. VII Certain defects in the international application
- [ ] Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1bis(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.
For further options, see Form PCT/ISA/220.

Name and mailing address of the ISA/KR	Date of completion of this opinion	Authorized officer
Korean Intellectual Property Office 189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City, 302-701, Republic of Korea Facsimile No. 82-42-472-7140	19 JULY 2012 (19.07.2012)	KIM, Jung Jin Telephone No.82-42-481-5962

Form PCT/ISA/237 (cover sheet) (July 2011)

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2011/063433

Box No. 1 Basis of this opinion

1. With regard to the **language**, this opinion has been established on the basis of:

   ☒ the international application in the language in which it was filed

   ☐ a translation of the international application into _____, which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(a))

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of:

   a. a sequence listing filed or furnished
      ☐ on paper
      ☐ in electronic form

   b. time of filing or furnishing
      ☐ contained in the international application as filed
      ☐ filed together with the international application in electronic form.
      ☐ furnished subsequently to this Authority for the purposes of search.

4. ☐ In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additioanl copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2011/063433

Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Claims	1-20	YES
	Claims	NONE	NO
Inventive step (IS)	Claims	1-20	YES
	Claims	NONE	NO
Industrial applicability (IA)	Claims	1-20	YES
	Claims	NONE	NO

2. Citations and explanations :

Reference is made to the following documents:

D1: KR 10-2004-0050519 A (HYNIX SEMICONDUCTOR CO., LTD.) 16 June 2004
D2: US 2002-0130372 A1 (HYUNG-SHIN KWON et al.) 19 September 2002
D3: KR 10-2008-0021918 A (DONGBU ELECTRONICS CO., LTD.) 10 March 2008
D4: US 2006-0189058 A1 (JONG-WOOK LEE et al.) 24 August 2006

1. Novelty and Inventive Step

1.1 Independent Claim [1]

The subject matter of claim 1 differs from these prior art documents in that claim 1 discloses a method of fabricating a micro-electronic transistor, comprising: oxidizing the first interlayer dielectric material layer.

And it is not obvious to a skilled person in the art by the documents, taken alone or in combination. Therefore, claim 1 meets the requirements of PCT Article 33(2) and (3) with respect to novelty and inventive step.

1.2 Dependent Claims [2-7]

Claims 2-7 are dependant on claim 1 and therefore meet the requirements of PCT Article 33(2) and (3).

(Continued on the supplemental box)

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.
Continuation of:

-BOX No. V-

1.3 Independent Claim [8]

The subject matter of claim 8 differs from these prior art documents in that claim 8 discloses a method comprising: forming a gate dielectric adjacent the non-planar transistor fin within the gate trench, removing a portion of the conductive gate material to form a recess between the non-planar transistor gate spacers, forming a capping dielectric structure within the recess and oxidizing the first interlayer dielectric material layer. And it is not obvious to a skilled person in the art by the documents, taken alone or in combination. Therefore, claim 8 meets the requirements of PCT Article 33(2) and (3) with respect to novelty and inventive step.

1.4 Dependent Claims [9-16]

Claims 9-16 are dependant on claim 8 and therefore meet the requirements of PCT Article 33(2) and (3).

1.5 Independent Claim [17]

The subject matter of claim 17 differs from these prior art documents in that claim 17 discloses a micro-electronic transistor, comprising: the first interlayer dielectric material layer includes a densified portion formed proximate a first surface of the first interlayer dielectric material layer.
And it is not obvious to a skilled person in the art by the documents, taken alone or in combination. Therefore, claim 17 meets the requirements of PCT Article 33(2) and (3) with respect to novelty and inventive step.

1.6 Dependent Claims [18-20]

Claims 18-20 are dependant on claim 17 and therefore meet the requirements of PCT Article 33(2) and (3).

2. Industrial Applicability:

Claims 1-20 of the present invention are considered to be industrially applicable under PCT Article 33(4).

Electronic Acknowledgement Receipt	
EFS ID:	17207740
Application Number:	13992598
International Application Number:	
Confirmation Number:	5215
Title of Invention:	CAPPING DIELECTRIC STRUCTURE FOR TRANSISTOR GATES
First Named Inventor/Applicant Name:	Aaron W. Rosenbaum
Customer Number:	92265
Filer:	Robert G. Winkle/Jodi Gandel-Klein
Filer Authorized By:	Robert G. Winkle
Attorney Docket Number:	P38683US
Receipt Date:	23-OCT-2013
Filing Date:	07-JUN-2013
Time Stamp:	16:28:17
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	P38683US_IDS.pdf	888651 290b966e9518c1eaa12de980396685d508f2d969	no	5
Warnings:					
Information:					

This is not an USPTO supplied IDS fillable form					
2	Foreign Reference	FR1.pdf	3612193 a9ce60fc2ea4aef1667565af7daed2ecf17f2d28	no	22
Warnings:					
Information:					
3	Foreign Reference	FR2.pdf	3677956 0722c1020c6149559f58f8d231a4ae9b659b9e55	no	20
Warnings:					
Information:					
4	Foreign Reference	FR3.pdf	1850337 0bc020121c013d71525a253d357fb9087cf86704	no	8
Warnings:					
Information:					
5	Foreign Reference	FR4.pdf	1970475 f231e40fe013f5aaa65fb6162e8dde8123e364ac	no	12
Warnings:					
Information:					
6	Foreign Reference	FR5.pdf	3803474 b06fc1e1eae82f9d11f3dce410c045ba57574876	no	33
Warnings:					
Information:					
7	Foreign Reference	FR6.pdf	3936254 1e7fcd2c97716ec4dfca292a046d611fdac2e1e6	no	30
Warnings:					
Information:					
8	Foreign Reference	FR7.pdf	3837769 292c43c0f1019e3d285e5ac0290d12b862947f66	no	31
Warnings:					
Information:					
9	Foreign Reference	FR8.pdf	4379672 46780cf1ad23142211840a5e7bacb6be04558132	no	34
Warnings:					
Information:					
10	Non Patent Literature	NPL1.pdf	1313550 54248866a7652da2f613db223375a1698c030d21	no	8

Warnings:					
Information:					
11	Non Patent Literature	NPL2.pdf	1457698 cd67319534643baf65800079e7a0cc7ff652a9b2	no	9
Warnings:					
Information:					
12	Non Patent Literature	NPL3.pdf	1433221 f7017a23ffacad15e12f10c0770f547fe01dfd53	no	9
Warnings:					
Information:					
13	Non Patent Literature	NPL4.pdf	1406532 aa19d3c5aac1c85fea4fdf77bd9bc700402e34e6	no	9
Warnings:					
Information:					
			Total Files Size (in bytes):	33567782	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/AIA/96 (08-12)
Approved for use through 01/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: Aaron W. Rosenbaum et al.

Application No./Patent No.: 13/992,598 Filed/Issue Date: June 7, 2013

Titled: CAPPING DIELECTRIC STRUCTURE FOR TRANSISTOR GATES

Intel Corporation, a Corporation

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☑ The assignee of the entire right, title, and interest.

2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):

☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

A. ☑ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 027089, Frame 0669, or for which a copy thereof is attached.

B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

2. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/96 (08-12)
Approved for use through 01/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

4. From: _____ To: _____

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Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☑ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Robert G. Winkle/	2013-11-07
Signature	Date
Robert G. Winkle	Attorney
Printed or Typed Name	Title or Registration Number

PTO/AIA/80 (07-12)
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POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(c).

I hereby appoint:

☑ Practitioners associated with Customer Number: 92265

OR

☐ Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

As attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications a ssigned only to the undersigned according to the USPTO assignment records or assignments docu ments attached to this form in accordance with 37 CFR 3.73(c).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(c) to:

☑ The address associated with Customer Number: 92265

OR

☐

Firm or Individual Name		
Address		
City		
Country		
Telephone		Email

Assignee Name and Address: INTEL CORPORATION
2200 MISSION COLLEGE BOULEVARD, SANTA CLARA, CA 95054

A copy of this form, together with a statement under 37 CFR 3.73(c) (Form PTO/SB/96 or equivalent) is required to be Filed in each application in which this form is used. The statement under 37 CFR 3.73(c) may be completed by one of The practitioners appointed in this form, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature	Heather Adamson	Date	1/2/2013
Name	Heather Adamson	Telephone	503-613-0191
Title	Administrator of Patents - Intel Corporation		

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/14 (03-13)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P38683US
	Application Number	
Title of Invention	CAPPING DIELECTRIC STRUCTURE FOR TRANSISTOR GATES	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 — Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	AARON	W.	ROSENBAUM	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Portland	State/Province	OR	Country of Residence	US

Mailing Address of Inventor:

Address 1	5530 Nw Osprey Place		
Address 2			
City	Portland	State/Province	OR
Postal Code	97229	Country	US

Inventor 2 — Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	DIN-HOW		MEI	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Portland	State/Province	OR	Country of Residence	US

Mailing Address of Inventor:

Address 1	5366 NW 132nd Ave.		
Address 2			
City	Portland	State/Province	OR
Postal Code	97229	Country	US

Inventor 3 — Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	SAMEER	S.	PRADHAN	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

SUPPLEMENTAL

PTO/AIA/14 (03-13)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P38683US
	Application Number	
Title of Invention	CAPPING DIELECTRIC STRUCTURE FOR TRANSISTOR GATES	

City	Portland	State/Province	OR	Country of Residence	US

Mailing Address of Inventor:

Address 1	17923 NW Sylvania Lane		
Address 2			
City	Portland	State/Province	OR
Postal Code	97229	Country	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	92265		
Email Address	inteldocs@cpaglobal.com	Add Email	Remove Email

Application Information:

Title of the Invention	CAPPING DIELECTRIC STRUCTURE FOR TRANSISTOR GATES		
Attorney Docket Number	P38683US	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	13	Suggested Figure for Publication (if any)	

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)

SUPPLEMENTAL

PTO/AIA/14 (03-13)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P38683US
	Application Number	
Title of Invention	CAPPING DIELECTRIC STRUCTURE FOR TRANSISTOR GATES	

Customer Number	92265

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	a 371 of international	PCT/US2011/054464	2011-09-30

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button.

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(d). When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(h)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

			Remove
Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button.

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P38683US
	Application Number	
Title of Invention	CAPPING DIELECTRIC STRUCTURE FOR TRANSISTOR GATES	

Authorization to Permit Access:

☒ Authorization to Permit Access to the Instant Application by the Participating Offices

If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application.

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date o f filing this Authorization.

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

◉ Assignee	○ Legal Representative under 35 U.S.C. 117	○ Joint Inventor
○ Person to whom the inventor is obligated to assign.	○ Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor :

If the Applicant is an Organization check here. ☒

Organization Name: Intel Corporation

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P38683US
	Application Number	
Title of Invention	CAPPING DIELECTRIC STRUCTURE FOR TRANSISTOR GATES	

Mailing Address Information For Applicant:			
Address 1	2200 Mission College Blvd.		
Address 2			
City	Santa Clara	State/Province	CA
Country[i]	USA	Postal Code	95054
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button.

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not subsitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication . An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

If the Assignee is an Organization check here. ☐

Prefix	Given Name	Middle Name	Family Name	Suffix

Mailing Address Information For Non-Applicant Assignee:			
Address 1			
Address 2			
City		State/Province	
Country[i]		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee Data may be generated within this form by selecting the Add button.

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PTO/AIA/14 (03-13)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P38683US
	Application Number	
Title of Invention	CAPPING DIELECTRIC STRUCTURE FOR TRANSISTOR GATES	

Signature:

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications.					
Signature	/Robert G. Winkle, Reg. No. 37,474/			Date (YYYY-MM-DD)	2013-11-07
First Name	Robert G.	Last Name	Winkle	Registration Number	37474
Additional Signature may be generated within this form by selecting the Add button.					

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent C o o p eration Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt	
EFS ID:	17340890
Application Number:	13992598
International Application Number:	
Confirmation Number:	5215
Title of Invention:	CAPPING DIELECTRIC STRUCTURE FOR TRANSISTOR GATES
First Named Inventor/Applicant Name:	Aaron W. Rosenbaum
Customer Number:	92265
Filer:	Robert G. Winkle/Jodi Gandel-Klein
Filer Authorized By:	Robert G. Winkle
Attorney Docket Number:	P38683US
Receipt Date:	08-NOV-2013
Filing Date:	07-JUN-2013
Time Stamp:	10:42:04
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	P38683US_RPOA.pdf	2711127 5d152ce3385e96dfb28976b0f818747180d05d31	no	3
Warnings:					
Information:					

2	Application Data Sheet	P38683US_SUPP_ADS.pdf	5044669 32f0faa927cde8b0f718f66f2a0178e83e49b0ff	no	7

Warnings:	
Information:	
This is not an USPTO supplied ADS fillable form	
Total Files Size (in bytes):	7755796

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
13/992,598	06/07/2013	2811	2300	P38683US	25	4

CONFIRMATION NO. 5215

CORRECTED FILING RECEIPT

92265
Winkle, PLLC
c/o CPA Global
P.O. Box 52050
Minneapolis, MN 55402

OC000000064936894

Date Mailed: 11/15/2013

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Aaron W. Rosenbaum, Portland, OR;
Din-How Mei, Portland, OR;
Sameer S. Pradhan, Portland, OR;

Applicant(s)

Intel Corporation, Santa Clara, CA

Assignment For Published Patent Application

Intel Corporation, Santa Clara, CA

Power of Attorney: The patent practitioners associated with Customer Number 92265

Domestic Priority data as claimed by applicant

This application is a 371 of PCT/US11/54464 09/30/2011

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access - A proper **Authorization to Permit Access to Application by Participating Offices** (PTO/SB/39 or its equivalent) has been received by the USPTO.

If Required, Foreign Filing License Granted: 06/15/2013
The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/992,598**
Projected Publication Date: Not Applicable

Non-Publication Request: No

Early Publication Request: No

Title

CAPPING DIELECTRIC STRUCTURE FOR TRANSISTOR GATES

Preliminary Class

257

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

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This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

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No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/992,598	06/07/2013	Aaron W. Rosenbaum	P38683US

CONFIRMATION NO. 5215

92265
Winkle, PLLC
c/o CPA Global
P.O. Box 52050
Minneapolis, MN 55402

POA ACCEPTANCE LETTER

OC000000064936736

Date Mailed: 11/15/2013

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 11/08/2013.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/tgebre/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	13992598
	Filing Date	2013-06-07
	First Named Inventor	Aaron W. Rosenbaum
	Art Unit	2896
	Examiner Name	Samuel L. Lair
	Attorney Docket Number	P38683US

U.S.PATENTS						
Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					
If you wish to add additional U.S. Patent citation information please click the Add button.						

U.S.PATENT APPLICATION PUBLICATIONS						
Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20050023133	A1	2005-02-03	Lippitt et al.	
	2	20060157749	A1	2006-07-20	Okuno, Masaki	
	3	20140117425	A1	2014-05-01	Pradhan et al.	
	4	20130256767	A1	2013-10-03	Pradhan et al.	
If you wish to add additional U.S. Published Application citation information please click the Add button.						

FOREIGN PATENT DOCUMENTS								
Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] ¡	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	13992598
	Filing Date	2013-06-07
	First Named Inventor	Aaron W. Rosenbaum
	Art Unit	2896
	Examiner Name	Samuel L. Lair
	Attorney Docket Number	P38683US

	1							☐

If you wish to add additional Foreign Patent Document citation information please click the Add button

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	International Preliminary Report on Patentability and Written Opinion received for PCT Patent Application No. PCT/US2011/054479, mailed on April 10, 2014, 6 pages.	☐
	2	International Preliminary Report on Patentability and Written Opinion received for PCT Patent Application No. PCT/US2011/054294, mailed on April 10, 2014, 5 pages.	☐
	3	International Preliminary Report on Patentability and Written Opinion received for PCT Patent Application No. PCT/US2011/054464, mailed on April 10, 2014, 6 pages.	☐
	4	International Preliminary Report on Patentability and Written Opinion received for PCT Patent Application No. PCT/US2011/063433, mailed on June 19, 2014, 6 pages.	☐

If you wish to add additional non-patent literature document citation information please click the Add button

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	13992598
	Filing Date	2013-06-07
	First Named Inventor	Aaron W. Rosenbaum
	Art Unit	2896
	Examiner Name	Samuel L. Lair
	Attorney Docket Number	P38683US

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Robert G. Winkle/	Date (YYYY-MM-DD)	2014-07-21
Name/Print	Robert G. Winkle	Registration Number	37,474

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PATENT COOPERATION TREATY

From the INTERNATIONAL BUREAU

PCT

NOTIFICATION CONCERNING
TRANSMITTAL OF COPY OF INTERNATIONAL
PRELIMINARY REPORT ON PATENTABILITY
(CHAPTER I OF THE PATENT COOPERATION
TREATY)
(PCT Rule 44bis.1(c))

To:

DRAEGER, Jeffrey, S.
Winkle, PLLC
c/o CPA GLOBAL
P.O. Box 52050
Minneapolis, Minnesota 55402
ETATS-UNIS D'AMERIQUE

Date of mailing *(day/month/year)* 10 April 2014 (10.04.2014)	
Applicant's or agent's file reference P38682PCT	**IMPORTANT NOTICE**

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US2011/054479	01 October 2011 (01.10.2011)	

Applicant
INTEL CORPORATION et al

The International Bureau transmits herewith a copy of the international preliminary report on patentability (Chapter I of the Patent Cooperation Treaty).

The International Bureau of WIPO
34, chemin des Colombettes
1211 Geneva 20, Switzerland

Facsimile No. +41 22 338 82 70

Authorized officer
Philippe Bécamel

e-mail: pt03.pct@wipo.int

Form PCT/IB/326 (January 2004)

PATENT COOPERATION TREATY

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INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY
(Chapter I of the Patent Cooperation Treaty)

(PCT Rule 44*bis*)

Applicant's or agent's file reference P38682PCT	**FOR FURTHER ACTION**	See item 4 below
International application No. PCT/US2011/054479	International filing date *(day/month/year)* 01 October 2011 (01.10.2011)	Priority date *(day/month/year)*
International Patent Classification (8th edition unless older edition indicated) See relevant information in Form PCT/ISA/237		
Applicant INTEL CORPORATION		

1. This international preliminary report on patentability (Chapter I) is issued by the International Bureau on behalf of the International Searching Authority under Rule 44 *bis*.1(a).

2. This REPORT consists of a total of 5 sheets, including this cover sheet.

   In the attached sheets, any reference to the written opinion of the International Searching Authority should be read as a reference to the international preliminary report on patentability (Chapter I) instead.

3. This report contains indications relating to the following items:

☒	Box No. I	Basis of the report
☐	Box No. II	Priority
☐	Box No. III	Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
☐	Box No. IV	Lack of unity of invention
☒	Box No. V	Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
☐	Box No. VI	Certain documents cited
☐	Box No. VII	Certain defects in the international application
☐	Box No. VIII	Certain observations on the international application

4. The International Bureau will communicate this report to designated Offices in accordance with Rules 44*bis*.3(c) and 93*bis*.1 but not, except where the applicant makes an express request under Article 23(2), before the expiration of 30 months from the priority date (Rule 44*bis* .2).

	Date of issuance of this report 01 April 2014 (01.04.2014)
The International Bureau of WIPO 34, chemin des Colombettes 1211 Geneva 20, Switzerland Facsimile No. +41 22 338 82 70	Authorized officer Philippe Bécamel e-mail: pt03.pct@wipo.int

Form PCT/IB/373 (January 2004)

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:
WINKLE ROBERT G.

WINKLE, PLLC C/O CPA GLOBAL P.O. BOX 52050
MINNEAPOLIS MN 55402 USA

PCT

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43bis.1)

Date of mailing *(day/month/year)*	**16 MAY 2012 (16.05.2012)**
Applicant's or agent's file reference: P38682PCT	**FOR FURTHER ACTION**: See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US2011/054479	**01 OCTOBER 2011 (01.10.2011)**	

International Patent Classification (IPC) or both national classification and IPC

H01L 29/78(2006.01)i, H01L 21/336(2006.01)i

Applicant

INTEL CORPORATION et al

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☐ Box No. VII Certain defects in the international application
- ☐ Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1bis(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.
For further options, see Form PCT/ISA/220.

Name and mailing address of the ISA/KR	Date of completion of this opinion	Authorized officer
Korean Intellectual Property Office Government Complex-Daejeon, 189 Cheongsa-ro, Seo-gu, Daejeon 302-701, Republic of Korea Facsimile No. 82-42-472-7140	15 MAY 2012 (15.05.2012)	Lee,Sang Ho Telephone No.82-42-481-8221

Form PCT/ISA/237 (cover sheet) (July 2011)

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2011/054479

Box No. I Basis of this opinion

1. With regard to the **language**, this opinion has been established on the basis of :

   ☒ the international application in the language in which it was filed

   ☐ a translation of the international application into _____ , which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(a))

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of:

   a. a sequence listing filed or furnished
      ☐ on paper
      ☐ in electronic form

   b. time of filing or furnishing
      ☐ contained in the international application as filed.
      ☐ filed together with the international application in electronic form.
      ☐ furnished subsequently to this Authority for the purposes of search.

4. ☐ In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additioanl copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2011/054479

Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Claims	1-24	YES
	Claims	NONE	NO
Inventive step (IS)	Claims	1-24	YES
	Claims	NONE	NO
Industrial applicability (IA)	Claims	1-24	YES
	Claims	NONE	NO

2. Citations and explanations :

Reference is made to the following documents:

D1: US 7456471 B2 (ANDERSON BRENT A. et al.) 25 November 2008
D2: US 06136697 A (WU; SHYE-LIN) 24 October 2000
D3: KR 10-0585178 B1 (SAMSUNG ELECTRONICS CO., LTD.) 24 May 2006

1. Novelty and Inventive Step

1.1 claims 1-4
The subject matter of claim 1 differs from the disclosure of D1 in that a microelectronic device comprises a titanium silicide interface disposed between the silicon-containing source/drain region and the titanium containing contact interface layer. As the subject matter of claim 1 is not shown in any other prior art documents cited in the ISR, claim 1 is not anticipated by any of the prior art documents including D1, nor obvious to the person skilled in the art.
Therefore, claim 1 is novel and involves an inventive step under PCT Article 33(2) and (3).

Claims 2-4 which are dependent on claim 1 also meet the requirements of PCT Article 33(2)-(3) with respect to novelty and inventive step.

1.2 claims 5-10
The subject matter of claim 5 differs from the disclosure of D1 in that the microelectronic device comprises a source/drain contact extending through a portion of the at least one dielectric material layer and comprising a conductive contact material and a titanium containing contact interface layer disposed between conductive contact material and the silicon-containing source/drain region. As the subject matter of claim 5 is not shown in any other prior art documents cited in the ISR, claim 5 is not anticipated by any of the prior art documents including D1, nor obvious to the person skilled in the art.
Therefore, claim 5 is novel and involves an inventive step under PCT Article 33(2) and (3).

Claims 6-10 which are dependent on claim 5 also meet the requirements of PCT Article 33(2)-(3) with respect to novelty and inventive step.

(Continued on the Supplemental Box.)

Supplemental Box

In case **the space in any of the preceding boxes is not sufficient.**
Continuation of :

Box V.

1.3 claims 11-15
The method of fabricating a microelectronic device of claim 11 differs from the disclosure of D1 in that the fourth step in the method of claim 11 comprises conformally deposits a titanium-containing contact interface layer within the contact opening to abut the silicon-containing source/drain region. As the subject matter of claim 11 is not shown in any other prior art documents cited in the ISR, claim 11 is not anticipated by any of the prior art documents including D1, nor obvious to the person skilled in the art.
Therefore, claim 11 is novel and involves an inventive step under PCT Article 33(2) and (3).

Claims 12-15 which are dependent on claim 11 also meet the requirements of PCT Article 33(2)-(3) with respect to novelty and inventive step.

1.4 claims 16-24
The method of claim 16 differs from the disclosure of D1 in that the eleventh step in the method of claim 16 comprises conformally deposits a titanium-containing contact interface layer within the contact opening to abut the silicon-containing source/drain region. As the subject matter of claim 16 is not shown in any other prior art documents cited in the ISR, claim 16 is not anticipated by any of the prior art documents including D1, nor obvious to the person skilled in the art.
Therefore, claim 16 is novel and involves an inventive step under PCT Article 33(2) and (3).

Claims 17-24 which are dependent on claim 16 also meet the requirements of PCT Article 33(2)-(3) with respect to novelty and inventive step.

2. Industrial Applicability
Claims 1-24 have industrial applicability (PCT Article 33(4)).

PATENT COOPERATION TREATY

From the INTERNATIONAL BUREAU

PCT

NOTIFICATION CONCERNING TRANSMITTAL OF COPY OF INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY (CHAPTER I OF THE PATENT COOPERATION TREATY)
(PCT Rule 44bis.1(c))

To:

WINKLE, Robert, G.
Winkle, PLLC
c/o CPA GLOBAL
P.O. Box 52050
Minneapolis, Minnesota 55402
ETATS-UNIS D'AMERIQUE

Date of mailing *(day/month/year)* 10 April 2014 (10.04.2014)	
Applicant's or agent's file reference P38946PCT	**IMPORTANT NOTICE**

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US2011/054294	30 September 2011 (30.09.2011)	

Applicant
INTEL CORPORATION et al

The International Bureau transmits herewith a copy of the international preliminary report on patentability (Chapter I of the Patent Cooperation Treaty).

The International Bureau of WIPO
34, chemin des Colombettes
1211 Geneva 20, Switzerland

Facsimile No. +41 22 338 82 70

Authorized officer
Kihwan Moon

e-mail: pt01.pct@wipo.int

Form PCT/IB/326 (January 2004)

PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY
(Chapter I of the Patent Cooperation Treaty)

(PCT Rule 44*bis*)

Applicant's or agent's file reference P38946PCT	**FOR FURTHER ACTION**	See item 4 below
International application No. PCT/US2011/054294	International filing date *(day/month/year)* 30 September 2011 (30.09.2011)	Priority date *(day/month/year)*
International Patent Classification (8th edition unless older edition indicated) See relevant information in Form PCT/ISA/237		
Applicant INTEL CORPORATION		

1. This international preliminary report on patentability (Chapter I) is issued by the International Bureau on behalf of the International Searching Authority under Rule 44 *bis*.1(a).

2. This REPORT consists of a total of 4 sheets, including this cover sheet.

   In the attached sheets, any reference to the written opinion of the International Searching Authority should be read as a reference to the international preliminary report on patentability (Chapter I) instead.

3. This report contains indications relating to the following items:

☒	Box No. I	Basis of the report
☐	Box No. II	Priority
☐	Box No. III	Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
☐	Box No. IV	Lack of unity of invention
☒	Box No. V	Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
☐	Box No. VI	Certain documents cited
☐	Box No. VII	Certain defects in the international application
☐	Box No. VIII	Certain observations on the international application

4. The International Bureau will communicate this report to designated Offices in accordance with Rules 44*bis*.3(c) and 93*bis*.1 but not, except where the applicant makes an express request under Article 23(2), before the expiration of 30 months from the priority date (Rule 44*bis* .2).

	Date of issuance of this report 01 April 2014 (01.04.2014)
The International Bureau of WIPO 34, chemin des Colombettes 1211 Geneva 20, Switzerland Facsimile No. +41 22 338 82 70	Authorized officer Kihwan Moon e-mail: pt01.pct@wipo.int

Form PCT/IB/373 (January 2004)

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:
WINKLE ROBERT C.

WINKLE, PLLC C/O CPA GLOBAL P.O. BOX 52050
MINNEAPOLIS MN 55402 USA

PCT

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43bis.1)

Date of mailing *(day/month/year)*	**15 MAY 2012 (15.05.2012)**
Applicant's or agent's file reference P38946PCT	**FOR FURTHER ACTION** See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US2011/054294	**30 SEPTEMBER 2011 (30.09.2011)**	

International Patent Classification (IPC) or both national classification and IPC

H01L 29/78(2006.01)i, H01L 21/336(2006.01)i

Applicant

INTEL CORPORATION et al

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☐ Box No. VII Certain defects in the international application
- ☐ Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1bis(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.
For further options, see Form PCT/ISA/220.

Name and mailing address of the ISA/KR	Date of completion of this opinion	Authorized officer
Korean Intellectual Property Office Government Complex-Daejeon, 189 Cheongsa-ro, Seo-gu, Daejeon 302-701, Republic of Korea Facsimile No. 82-42-472-7140	15 MAY 2012 (15.05.2012)	Lee,Sang Ho Telephone No.82-42-481-8221

Form PCT/ISA/237 (cover sheet) (July 2011)

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2011/054294

Box No. I Basis of this opinion

1. With regard to the **language**, this opinion has been established on the basis of :

   ☒ the international application in the language in which it was filed

   ☐ a translation of the international application into _____ , which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(a))

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of:

   a. a sequence listing filed or furnished
      ☐ on paper
      ☐ in electronic form

   b. time of filing or furnishing
      ☐ contained in the international application as filed.
      ☐ filed together with the international application in electronic form.
      ☐ furnished subsequently to this Authority for the purposes of search.

4. ☐ In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additioanl copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2011/054294

Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Claims	1-25	YES
	Claims	NONE	NO
Inventive step (IS)	Claims	1-25	YES
	Claims	NONE	NO
Industrial applicability (IA)	Claims	1-25	YES
	Claims	NONE	NO

2. Citations and explanations :

Reference is made to the following documents:

D1: US 7528025 B2 (BRASK JUSTIN K. et al.) 05 May 2009
D2: KR 10-0585178 B1 (SAMSUNG ELECTRONICS CO., LTD.) 30 May 2006
D3: US 2011-0147831 A1 (STEIGERWALD JOSEPH M. et al.) 23 June 2011

1. Novelty and Inventive Step

1.1 claims 1-5
The subject matter of claim 1 differs from the disclosure of D1 in that the gate electrode includes a tungsten-containing gate fill material adjacent the gate fill barrier. As the subject matter of claim 1 is not shown in any other prior art documents cited in the ISR, claim 1 is not anticipated by any of the prior art documents including D1, nor obvious to the person skilled in the art.
Therefore, claim 1 is novel and involves an inventive step under PCT Article 33(2) and (3).

Claims 2-5 which are dependent on claim 1 also meet the requirements of PCT Article 33(2)-(3) with respect to novelty and inventive step.

1.2 claims 6-16
The method of claim 6 differs from the disclosure of D1 in that the second step in the method of claim 6 forms a gate electrode including the step of depositing a tungsten-containing gate fill material adjacent the gate fill barrier. As the subject matter of claim 6 is not shown in any other prior art documents cited in the ISR, claim 6 is not anticipated by any of the prior art documents including D1, nor obvious to the person skilled in the art.
Therefore, claim 6 is novel and involves an inventive step under PCT Article 33(2) and (3).

Claims 7-16 which are dependent on claim 6 also meet the requirements of PCT Article 33(2)-(3) with respect to novelty and inventive step.

1.3 claims 17-25
The method of claim 17 differs from the disclosure of D1 in that the seventh step in the method of claim 17 forms a gate electrode including the step of depositing a tungsten-containing gate fill material adjacent the gate fill barrier. As the subject matter of claim 17 is not shown in any other prior art documents cited in the ISR, claim 17 is not anticipated by any of the prior art documents including D1, nor obvious to the person skilled in the art.
Therefore, claim 17 is novel and involves an inventive step under PCT Article 33(2) and (3).

Claims 18-25 which are dependent on claim 17 also meet the requirements of PCT Article 33(2)-(3) with respect to novelty and inventive step.

2. Industrial Applicability
Claims 1-25 have industrial applicability (PCT Article 33(4)).

PATENT COOPERATION TREATY

From the INTERNATIONAL BUREAU

PCT

NOTIFICATION CONCERNING
TRANSMITTAL OF COPY OF INTERNATIONAL
PRELIMINARY REPORT ON PATENTABILITY
(CHAPTER I OF THE PATENT COOPERATION
TREATY)
(PCT Rule 44bis.1(c))

To:

BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP
1279 Oakmead Parkway
Sunnyvale, CA 94086
ETATS-UNIS D'AMERIQUE

Date of mailing *(day/month/year)* 10 April 2014 (10.04.2014)	
Applicant's or agent's file reference P38683PCT	**IMPORTANT NOTICE**

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US2011/054464	30 September 2011 (30.09.2011)	

Applicant
INTEL CORPORATION et al

The International Bureau transmits herewith a copy of the international preliminary report on patentability (Chapter I of the Patent Cooperation Treaty).

The International Bureau of WIPO
34, chemin des Colombettes
1211 Geneva 20, Switzerland

Facsimile No. +41 22 338 82 70

Authorized officer
Simin Baharlou

e-mail: pt09.pct@wipo.int

Form PCT/IB/326 (January 2004)

PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY
(Chapter I of the Patent Cooperation Treaty)

(PCT Rule 44*bis*)

Applicant's or agent's file reference P38683PCT	**FOR FURTHER ACTION**	See item 4 below
International application No. PCT/US2011/054464	International filing date *(day/month/year)* 30 September 2011 (30.09.2011)	Priority date *(day/month/year)*
International Patent Classification (8th edition unless older edition indicated) See relevant information in Form PCT/ISA/237		
Applicant INTEL CORPORATION		

1. This international preliminary report on patentability (Chapter I) is issued by the International Bureau on behalf of the International Searching Authority under Rule 44 *bis*.1(a).

2. This REPORT consists of a total of 5 sheets, including this cover sheet.

   In the attached sheets, any reference to the written opinion of the International Searching Authority should be read as a reference to the international preliminary report on patentability (Chapter I) instead.

3. This report contains indications relating to the following items:

☒	Box No. I	Basis of the report
☐	Box No. II	Priority
☐	Box No. III	Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
☐	Box No. IV	Lack of unity of invention
☒	Box No. V	Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
☐	Box No. VI	Certain documents cited
☐	Box No. VII	Certain defects in the international application
☐	Box No. VIII	Certain observations on the international application

4. The International Bureau will communicate this report to designated Offices in accordance with Rules 44*bis*.3(c) and 93*bis*.1 but not, except where the applicant makes an express request under Article 23(2), before the expiration of 30 months from the priority date (Rule 44*bis* .2).

	Date of issuance of this report 01 April 2014 (01.04.2014)
The International Bureau of WIPO 34, chemin des Colombettes 1211 Geneva 20, Switzerland Facsimile No. +41 22 338 82 70	Authorized officer Simin Baharlou e-mail: pt09.pct@wipo.int

Form PCT/IB/373 (January 2004)

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:
BLAKELY SOKOLOFF TAYLOR&AZFMAN LLP

1279 OAKMEAD PARKWAY SUNNYVALE, CA 94086
USA

PCT

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43bis.1)

Date of mailing *(day/month/year)*	**15 MAY 2012 (15.05.2012)**
Applicant's or agent's file reference P38683PCT	**FOR FURTHER ACTION** See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US2011/054464	**30 SEPTEMBER 2011 (30.09.2011)**	

International Patent Classification (IPC) or both national classification and IPC

H01L 29/78(2006.01)i, H01L 21/336(2006.01)i

Applicant

INTEL CORPORATION et al

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☐ Box No. VII Certain defects in the international application
- ☐ Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1bis(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.
For further options, see Form PCT/ISA/220.

Name and mailing address of the ISA/KR	Date of completion of this opinion	Authorized officer
Korean Intellectual Property Office Government Complex-Daejeon, 189 Cheongsa-ro, Seo-gu, Daejeon 302-701, Republic of Korea Facsimile No. 82-42-472-7140	15 MAY 2012 (15.05.2012)	Lee,Sang Ho Telephone No.82-42-481-8221

Form PCT/ISA/237 (cover sheet) (July 2011)

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2011/054464

Box No. I Basis of this opinion

1. With regard to the **language**, this opinion has been established on the basis of :

   ☒ the international application in the language in which it was filed

   ☐ a translation of the international application into _____ , which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(a))

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of:

   a. a sequence listing filed or furnished
      ☐ on paper
      ☐ in electronic form

   b. time of filing or furnishing
      ☐ contained in the international application as filed.
      ☐ filed together with the international application in electronic form.
      ☐ furnished subsequently to this Authority for the purposes of search.

4. ☐ In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additioanl copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2011/054464

Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Claims	1-25	YES
	Claims	NONE	NO
Inventive step (IS)	Claims	1-25	YES
	Claims	NONE	NO
Industrial applicability (IA)	Claims	1-25	YES
	Claims	NONE	NO

2. Citations and explanations :

Reference is made to the following documents:

D1: US 2008-0233699 A1 (BOOTH ROGER ALLEN et al.) 25 September 2008
D2: US 2010-0048007 A1 (LEE SHEN-NAN et al.) 25 February 2010
D3: KR 10-0653711 B1 (SAMSUNG ELECTRONICS CO., LTD.) 05 December 2006

1. Novelty and Inventive Step

1.1 claims 1-4
The subject matter of claim 1 differs from the disclosure of D1 in that the transistor gate comprises a substantially void free capping dielectric structure disposed adjacent the recessed gate electrode and between the pair of gate spacers. As the subject matter of claim 1 is not shown in any other prior art documents cited in the ISR, claim 1 is not anticipated by any of the prior art documents including D1, nor obvious to the person skilled in the art.
Therefore, claim 1 is novel and involves an inventive step under PCT Article 33(2) and (3).

Claims 2-4 which are dependent on claim 1 also meet the requirements of PCT Article 33(2)-(3) with respect to novelty and inventive step.

1.2 claims 5-9
The subject matter of claim 5 differs from the disclosure of D1 in that the microelectronic device comprises at least one dielectric material layer over the source/drain region, the non-planar transistor gate spacers, and the substantially void free capping dielectric structure. As the subject matter of claim 5 is not shown in any other prior art documents cited in the ISR, claim 5 is not anticipated by any of the prior art documents including D1, nor obvious to the person skilled in the art.
Therefore, claim 5 is novel and involves an inventive step under PCT Article 33(2) and (3).

Claims 6-9 which are dependent on claim 5 also meet the requirements of PCT Article 33(2)-(3) with respect to novelty and inventive step.

1.3 claims 10-14
The method of fabricating a transistor gate of claim 10 differs from the disclosure of D1 in that the third step in the method of claim 10 comprises high density plasma depositing a capping dielectric structure on a top surface of the recessed gate electrode and between the pair of gate spacers. As the subject matter of claim 10 is not shown in any other prior art documents cited in the ISR, claim 10 is not anticipated by any of the prior art documents including D1, nor obvious to the person skilled in the art.
Therefore, claim 10 is novel and involves an inventive step under PCT Article 33(2) and (3).

Claims 11-14 which are dependent on claim 10 also meet the requirements of PCT Article 33(2)-(3) with respect to novelty and inventive step.

(Continued on the Supplemental Box.)

Supplemental Box

In case **the space in any of the preceding boxes is not sufficient.**
Continuation of :

Box V.

1.4 claims 15-25
The method of claim 15 differs from the disclosure of D1 in that the ninth step in the method of claim 15 forms a capping dielectric structure within the recess by high density plasma depositing a dielectric material. As the subject matter of claim 15 is not shown in any other prior art documents cited in the ISR, claim 15 is not anticipated by any of the prior art documents including D1, nor obvious to the person skilled in the art.
Therefore, claim 15 is novel and involves an inventive step under PCT Article 33(2) and (3).

Claims 16-25 which are dependent on claim 15 also meet the requirements of PCT Article 33(2)-(3) with respect to novelty and inventive step.

2. Industrial Applicability
Claims 1-25 have industrial applicability (PCT Article 33(4)).

PATENT COOPERATION TREATY

ADVANCE E-MAIL

PCT

From the INTERNATIONAL BUREAU

NOTIFICATION CONCERNING TRANSMITTAL OF COPY OF INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY (CHAPTER I OF THE PATENT COOPERATION TREATY)
(PCT Rule 44bis.1(c))

To:

WINKLE, Robert
Winkle, PLLC
c/o CPA Global
P.O. Box 52050
Minneapolis, Minnesota 55402
ETATS-UNIS D'AMERIQUE

Date of mailing *(day/month/year)*
19 June 2014 (19.06.2014)

Applicant's or agent's file reference
P38684PCT

IMPORTANT NOTICE

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US2011/063433	06 December 2011 (06.12.2011)	

Applicant
INTEL CORPORATION et al

The International Bureau transmits herewith a copy of the international preliminary report on patentability (Chapter I of the Patent Cooperation Treaty).

The International Bureau of WIPO
34, chemin des Colombettes
1211 Geneva 20, Switzerland

Facsimile No. +41 22 338 82 70

Authorized officer
Agnès Wittmann-Regis

e-mail: pt06.pct@wipo.int

Form PCT/IB/326 (January 2004)

PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY
(Chapter I of the Patent Cooperation Treaty)

(PCT Rule 44*bis*)

Applicant's or agent's file reference P38684PCT	**FOR FURTHER ACTION**	See item 4 below
International application No. PCT/US2011/063433	International filing date *(day/month/year)* 06 December 2011 (06.12.2011)	Priority date *(day/month/year)*
International Patent Classification (8th edition unless older edition indicated) See relevant information in Form PCT/ISA/237		
Applicant INTEL CORPORATION		

1. This international preliminary report on patentability (Chapter I) is issued by the International Bureau on behalf of the International Searching Authority under Rule 44 *bis*.1(a).

2. This REPORT consists of a total of 5 sheets, including this cover sheet.

   In the attached sheets, any reference to the written opinion of the International Searching Authority should be read as a reference to the international preliminary report on patentability (Chapter I) instead.

3. This report contains indications relating to the following items:

☒	Box No. I	Basis of the report
☐	Box No. II	Priority
☐	Box No. III	Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
☐	Box No. IV	Lack of unity of invention
☒	Box No. V	Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
☐	Box No. VI	Certain documents cited
☐	Box No. VII	Certain defects in the international application
☐	Box No. VIII	Certain observations on the international application

4. The International Bureau will communicate this report to designated Offices in accordance with Rules 44*bis*.3(c) and 93*bis*.1 but not, except where the applicant makes an express request under Article 23(2), before the expiration of 30 months from the priority date (Rule 44*bis* .2).

	Date of issuance of this report 10 June 2014 (10.06.2014)
The International Bureau of WIPO 34, chemin des Colombettes 1211 Geneva 20, Switzerland Facsimile No. +41 22 338 82 70	Authorized officer Agnès Wittmann-Regis e-mail: pt06.pct@wipo.int

Form PCT/IB/373 (January 2004)

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:
WINKLE ROBERT

WINKLE, PLLC C/O CPA GLOBAL P.O. BOX 52050
MINNEAPOLIS MN 55402 USA

PCT

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43bis.1)

Date of mailing *(day/month/year)*	**20 JULY 2012 (20.07.2012)**
Applicant's or agent's file reference P38684PCT	**FOR FURTHER ACTION** See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US2011/063433	**06 DECEMBER 2011 (06.12.2011)**	

International Patent Classification (IPC) or both national classification and IPC

H01L 21/336(2006.01)i, H01L 29/78(2006.01)i, H01L 21/31(2006.01)i

Applicant

INTEL CORPORATION et al

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☐ Box No. VII Certain defects in the international application
- ☐ Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1bis(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.
For further options, see Form PCT/ISA/220.

Name and mailing address of the ISA/KR	Date of completion of this opinion	Authorized officer
Korean Intellectual Property Office 189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City, 302-701, Republic of Korea Facsimile No. 82-42-472-7140	19 JULY 2012 (19.07.2012)	KIM, Jung Jin Telephone No.82-42-481-5962

Form PCT/ISA/237 (cover sheet) (July 2011)

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2011/063433

Box No. I Basis of this opinion

1. With regard to the **language**, this opinion has been established on the basis of :

   ☒ the international application in the language in which it was filed

   ☐ a translation of the international application into _____ , which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(a))

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of:

   a. a sequence listing filed or furnished
      ☐ on paper
      ☐ in electronic form

   b. time of filing or furnishing
      ☐ contained in the international application as filed.
      ☐ filed together with the international application in electronic form.
      ☐ furnished subsequently to this Authority for the purposes of search.

4. ☐ In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additioanl copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2011/063433

Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Claims	1-20	YES
	Claims	NONE	NO
Inventive step (IS)	Claims	1-20	YES
	Claims	NONE	NO
Industrial applicability (IA)	Claims	1-20	YES
	Claims	NONE	NO

2. Citations and explanations :

Reference is made to the following documents:

D1: KR 10-2004-0050519 A (HYNIX SEMICONDUCTOR CO., LTD.) 16 June 2004
D2: US 2002-0130372 A1 (HYUNG-SHIN KWON et al.) 19 September 2002
D3: KR 10-2008-0021918 A (DONGBU ELECTRONICS CO., LTD.) 10 March 2008
D4: US 2006-0189058 A1 (JONG-WOOK LEE et al.) 24 August 2006

1. Novelty and Inventive Step

1.1 Independent Claim [1]

The subject matter of claim 1 differs from these prior art documents in that claim 1 discloses a method of fabricating a micro-electronic transistor, comprising: oxidizing the first interlayer dielectric material layer.

And it is not obvious to a skilled person in the art by the documents, taken alone or in combination. Therefore, claim 1 meets the requirements of PCT Article 33(2) and (3) with respect to novelty and inventive step.

1.2 Dependent Claims [2-7]

Claims 2-7 are dependant on claim 1 and therefore meet the requirements of PCT Article 33(2) and (3).

(Continued on the supplemental box)

Supplemental Box

In case **the space in any of the preceding boxes is not sufficient.**
Continuation of :

-BOX No. V-

1.3 Independent Claim [8]

The subject matter of claim 8 differs from these prior art documents in that claim 8 discloses a method comprising: forming a gate dielectric adjacent the non-planar transistor fin within the gate trench, removing a portion of the conductive gate material to form a recess between the non-planar transistor gate spacers, forming a capping dielectric structure within the recess and oxidizing the first interlayer dielectric material layer. And it is not obvious to a skilled person in the art by the documents, taken alone or in combination. Therefore, claim 8 meets the requirements of PCT Article 33(2) and (3) with respect to novelty and inventive step.

1.4 Dependent Claims [9-16]

Claims 9-16 are dependant on claim 8 and therefore meet the requirements of PCT Article 33(2) and (3).

1.5 Independent Claim [17]

The subject matter of claim 17 differs from these prior art documents in that claim 17 discloses a micro-electronic transistor, comprising: the first interlayer dielectric material layer includes a densified portion formed proximate a first surface of the first interlayer dielectric material layer.
And it is not obvious to a skilled person in the art by the documents, taken alone or in combination. Therefore, claim 17 meets the requirements of PCT Article 33(2) and (3) with respect to novelty and inventive step.

1.6 Dependent Claims [18-20]

Claims 18-20 are dependant on claim 17 and therefore meet the requirements of PCT Article 33(2) and (3).

2. Industrial Applicability:

Claims 1-20 of the present invention are considered to be industrially applicable under PCT Article 33(4).

Electronic Acknowledgement Receipt	
EFS ID:	19634723
Application Number:	13992598
International Application Number:	
Confirmation Number:	5215
Title of Invention:	CAPPING DIELECTRIC STRUCTURE FOR TRANSISTOR GATES
First Named Inventor/Applicant Name:	Aaron W. Rosenbaum
Customer Number:	92265
Filer:	Robert G. Winkle/Jodi Gandel-Klein
Filer Authorized By:	Robert G. Winkle
Attorney Docket Number:	P38683US
Receipt Date:	22-JUL-2014
Filing Date:	07-JUN-2013
Time Stamp:	09:34:25
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	P38683US_IDS.pdf	794027 d26ee2562d15a759e74461627bd9814d7294dab	no	4

Warnings:
Information:

This is not an USPTO supplied IDS fillable form					
2	Non Patent Literature	NPL1.pdf	222540 06589c63649bb957c73c9240344769944ba03e2d	no	6
Warnings:					
Information:					
3	Non Patent Literature	NPL2.pdf	197355 89f4899c4636852d801ff75931a2a811dd1c4e68	no	5
Warnings:					
Information:					
4	Non Patent Literature	NPL3.pdf	220245 0d4ba901af9f207f3070a4fdc398cf8f3b1f3c3a	no	6
Warnings:					
Information:					
5	Non Patent Literature	NPL4.pdf	214483 b402eca437ac38f88cf82fb18f875f20ade91c22	no	6
Warnings:					
Information:					
			Total Files Size (in bytes):	1648650	

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

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If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
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PTO/SB/08a (01-10)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	13992598
	Filing Date	2013-06-07
	First Named Inventor	Aaron W. Rosenbaum
	Art Unit	2817
	Examiner Name	Samuel L. Lair
	Attorney Docket Number	P38683US

U.S.PATENTS						
Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					
If you wish to add additional U.S. Patent citation information please click the Add button.						

U.S.PATENT APPLICATION PUBLICATIONS						
Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20050019993	A1	2005-01-27	Lee, et al.	
	2	20060046449	A1	2006-03-02	Liaw, Jhon-Jhy	
	3	20060088967	A1	2006-04-27	Hsiao, et al.	
	4	20060099783	A1	2006-05-11	Gluschenkov, et al.	
	5	20070111435	A1	2007-05-17	Kim, et al.	

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	Application Number	13992598
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	First Named Inventor	Aaron W. Rosenbaum
	Art Unit	2817
	Examiner Name	Samuel L. Lair
	Attorney Docket Number	P38683US

	6	20080001187	A1	2008-01-03	Booth, et al.	
	7	20080014710	A1	2008-01-17	Bian, et al.	
	8	20100105215	A1	2010-04-29	Sugawara, et al.	
	9	20100155842	A1	2010-06-24	Anderson, et al.	
	10	20110147812	A1	2011-06-23	Steigerwald, et al.	
	11	20110156107	A1	2011-06-30	Bohr, et al.	
	12	20110272739	A1	2011-11-10	Lee, et al.	

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FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] ¡	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
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	Application Number	13992598
	Filing Date	2013-06-07
	First Named Inventor	Aaron W. Rosenbaum
	Art Unit	2817
	Examiner Name	Samuel L. Lair
	Attorney Docket Number	P38683US

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	Office Action received for Taiwan Patent Application No. 101133821, mailed on August 6, 2014, 9 pages of English Translation and 9 pages of Taiwan Office Action.	☒

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	Application Number	13992598
	Filing Date	2013-06-07
	First Named Inventor	Aaron W. Rosenbaum
	Art Unit	2817
	Examiner Name	Samuel L. Lair
	Attorney Docket Number	P38683US

CERTIFICATION STATEMENT

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OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Robert G. Winkle/	Date (YYYY-MM-DD)	2014-10-16
Name/Print	Robert G. Winkle	Registration Number	37,474

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

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Electronic Acknowledgement Receipt	
EFS ID:	20431619
Application Number:	13992598
International Application Number:	
Confirmation Number:	5215
Title of Invention:	CAPPING DIELECTRIC STRUCTURE FOR TRANSISTOR GATES
First Named Inventor/Applicant Name:	Aaron W. Rosenbaum
Customer Number:	92265
Filer:	Robert G. Winkle/Jodi Gandel-Klein
Filer Authorized By:	Robert G. Winkle
Attorney Docket Number:	P38683US
Receipt Date:	16-OCT-2014
Filing Date:	07-JUN-2013
Time Stamp:	12:15:01
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	P38683US_IDS.pdf	817811 40427b7fab32e3e2e5e81c78366c4481d2dc27a8	no	5
Warnings:					
Information:					

This is not an USPTO supplied IDS fillable form					
2	Non Patent Literature	NPL1.pdf	2457476 eac1fc328c0358213357deddcbfea9ea1a60a645	no	18
Warnings:					
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			Total Files Size (in bytes):	3275287	

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PLUS Search Results for S/N 13992598, Searched Thu Feb 26 11:20:14 EST 2015

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6051920 99
4451324 98
4570332 98
4923473 98
5205543 98
5215439 98
5275066 98
5283392 98
5503491 98
5774939 98
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5013129 76
5214732 76
5273014 76
5293271 76
5332921 76
5564854 76

PTO/SB/08a (01-10)
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Filing Date	2013-06-07
First Named Inventor	Aaron W. Rosenbaum
Art Unit	2817
Examiner Name	Samuel L. Lair
Attorney Docket Number	P38683US

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20110147851	A1	2011-06-23	Thomas, et al.	
	2	20150041926	A1	2015-02-12	Pradhan, et al.	

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	2002-184981	JP	A	2002-06-28	Jang, et al.	English Abstract Submitted.	☐
	2	2004-128314	JP	A	2004-04-22	Kanemoto, Hiroshi	English Abstract Submitted.	☐

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
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	Filing Date	2013-06-07
	First Named Inventor	Aaron W. Rosenbaum
	Art Unit	2817
	Examiner Name	Samuel L. Lair
	Attorney Docket Number	P38683US

	3	2011/087571	WO	A1	2011-07-21	Cappellani, et al.		☐
	4	2011/090571	WO	A2	2011-07-28	Bohr, et al.		☐

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	Office Action received for Taiwan Patent Application No. 101133821, mailed on December 25, 2014, 7 pages of English Translation and 9 pages of Taiwan Office Action.	☒
	2	Office Action received for Japanese Patent Application No. 2014-533283, mailed on February 10, 2015, 2 pages of English Translation and 1 pages of Japanese Office Action.	☒

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☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Robert G. Winkle/	Date (YYYY-MM-DD)	2015-03-19
Name/Print	Robert G. Winkle	Registration Number	37,474

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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2002-184981
(43)Date of publication of application : 28.06.2002

(51)Int.Cl. H01L 29/78
H01L 21/28
H01L 21/336
H01L 21/768

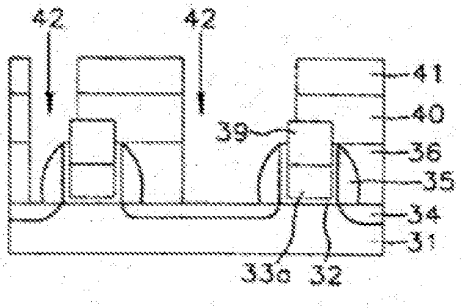
(21)Application number : 2001-315991
(22)Date of filing : 12.10.2001

(71)Applicant : HYNIX SEMICONDUCTOR INC
(72)Inventor : JANG SE AUG
TEI YUSEKI

(30)Priority
Priority number : 2000 200060416 Priority date : 13.10.2000 Priority country : KR

(54) MANUFACTURING METHOD OF SEMICONDUCTOR DEVICE USING DAMASCENE METAL GATE

(57)Abstract:
PROBLEM TO BE SOLVED: To provide the manufacturing method of a semiconductor device using a damascene metal gate for preventing an electrical short-circuiting phenomenon in a damascene gate electrode due to mismatching.
SOLUTION: This manufacturing method includes a step for forming a damascene gate oxide film 32 and the damascene gate electrode 33 on a semiconductor substrate 31, a step for selectively etching the damascene gate electrode by fixed thickness and for forming a recess 37 at the upper section of the damascene gate electrode, a step for forming an insulating film 39 in the recess at the upper section of the damascene gate electrode, a step for forming an interlayer insulating film 40 on the upper surface of the entire structure, and a step for selectively etching the interlayer insulating film 40 and for forming a contact hole 42 exposing one portion of the semiconductor substrate.



(19)日本国特許庁（ＪＰ）　(12)**公開特許公報**（Ａ）　(11)特許出願公開番号
特開2002－184981
（P2002－184981A）
(43)公開日　平成14年６月28日(2002.6.28)

(51)Int.Cl.'	識別記号	Ｆ Ｉ		テーマコード'(参考)
Ｈ０１Ｌ　29/78		Ｈ０１Ｌ　21/28	３０１Ｒ	４Ｍ１０４
21/28	３０１	29/78	３０１Ｃ	５Ｆ０３３
21/336		21/90	Ｃ	５Ｆ１４０
21/768		29/78	３０１Ｐ	

審査請求　未請求　請求項の数25　ＯＬ　（全 ９ 頁）

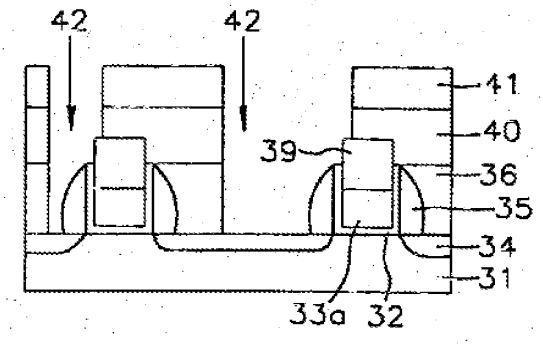
(21)出願番号　特願2001－315991(P2001－315991)
(22)出願日　平成13年10月12日(2001.10.12)
(31)優先権主張番号　２０００－０６０４１６
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(71)出願人　591024111
株式会社ハイニックスセミコンダクター
大韓民国京畿道利川市夫鉢邑牙美里山136－１
(72)発明者　張　世　億
大韓民国　京畿道　利川市　夫鉢邑　新河里　481－１　サムイクアパート　104－1210
(72)発明者　鄭　又　碩
大韓民国　京畿道　利川市　官廩洞　ドウサンアパート　101－1402
(74)代理人　110000051
特許業務法人共生国際特許事務所

最終頁に続く

(54)【発明の名称】　ダマシーン金属ゲートを用いた半導体装置の製造方法

(57)【要約】
【課題】　不整合によるダマシーンゲート電極の電気的ショート現象を防止することができるダマシーン金属ゲートを用いた半導体装置の製造方法を提供する。
【解決手段】　半導体基板３１上にダマシーンゲート酸化膜３２とダマシーンゲート電極３３とを形成するステップと、前記ダマシーンゲート電極を一定厚さだけ選択的にエッチングして前記ダマシーンゲート電極の上部に凹所３７を形成するステップと、前記ダマシーンゲート電極の上部の凹所内に絶縁膜３９を形成するステップと、前記全体構造の上面に層間絶縁膜４０を形成するステップと、前記層間絶縁膜を選択的にエッチングして前記半導体基板の一部分を露出させるコンタクトホール４２を形成するステップとを含んでなる。



【特許請求の範囲】

【請求項１】　半導体基板上にダマシーンゲート酸化膜とダマシーンゲート電極とを形成するステップと、
前記ダマシーンゲート電極を一定厚さだけ選択的にエッチングして前記ダマシーンゲート電極の上部に凹所を形成するステップと、
前記ダマシーンゲート電極の上部の凹所内に絶縁膜を形成するステップと、
前記全体構造の上面に層間絶縁膜を形成するステップと、
前記層間絶縁膜を選択的にエッチングして前記半導体基板の一部分を露出させるコンタクトホールを形成するステップとを含んでなることを特徴とするダマシーン金属ゲートを用いた半導体装置の製造方法。

【請求項２】　前記ダマシーンゲート電極用物質としてタングステン、窒化タングステン、チタニウム、モリブデン、タンタリウムもしくは窒化タンタリウムの内の一種もしくは複数種を使用することを特徴とする請求項１に記載のダマシーン金属ゲートを用いた半導体装置の製造方法。

【請求項３】　前記ダマシーンゲート電極は、２０００～２５００Åの厚さで形成することを特徴とする請求項１に記載のダマシーン金属ゲートを用いた半導体装置の製造方法。

【請求項４】　前記凹所は、前記ダマシーンゲート電極を５００～１０００Åだけウェットもしくはドライエッチング方法のいずれかを用いてリセスエッチングして形成することを特徴とする請求項１に記載のダマシーン金属ゲートを用いた半導体装置の製造方法。

【請求項５】　前記絶縁膜は、アルミニウム絶縁膜もしくはドーピングされていないポリシリコン絶縁膜を含むことを特徴とする請求項１に記載のダマシーン金属ゲートを用いた半導体装置の製造方法。

【請求項６】　前記アルミニウム絶縁膜を形成するステップは、前記凹所形成後、前記凹所内に選択性アルミニウム膜を形成するステップと、前記選択性アルミニウム膜を酸化もしくは窒化処理してアルミニウム絶縁膜を形成するステップとを含むことを特徴とする請求項５に記載のダマシーン金属ゲートを用いた半導体装置の製造方法。

【請求項７】　半導体基板上にダマシーンゲート酸化膜とダマシーンゲート電極とを形成するステップと、
前記ダマシーンゲート電極を一定厚さだけ選択的にエッチングして前記ダマシーンゲート電極の上部に凹所を形成するステップと、
前記ダマシーンゲート電極の上部の凹所内のみにアルミニウム膜を選択的に成長させるステップと、
前記アルミニウム膜をアルミニウム絶縁膜に変化させるステップと、
前記全体構造の上面に層間絶縁膜を形成するステップと、
前記層間絶縁膜を選択的にエッチングして前記半導体基板の一部分を露出させるコンタクトホール形成するステップとを含んでなることを特徴とするダマシーン金属ゲートを用いた半導体装置の製造方法。

【請求項８】　前記ダマシーンゲート電極は、タングステン、窒化タングステン、チタニウム、窒化チタニウム、モリブデン、タンタリウムもしくは窒化タンタリウムの内の一種もしくは複数種を使用することを特徴とする請求項７に記載のダマシーン金属ゲートを用いた半導体装置の製造方法。

【請求項９】　前記ダマシーンゲート電極は、２０００～２５００Åの厚さで形成することを特徴とする請求項７に記載のダマシーン金属ゲートを用いた半導体装置の製造方法。

【請求項１０】　前記凹所は、前記ダマシーンゲート電極を５００～１０００Åだけウェットもしくはドライエッチング方法のいずれかを用いてリセスエッチングして形成することを特徴とする請求項７に記載のダマシーン金属ゲートを用いた半導体装置の製造方法。

【請求項１１】　前記アルミニウム絶縁膜は、アルミニウム酸化膜もしくはアルミニウム窒化膜を含むことを特徴とする請求項７に記載のダマシーン金属ゲートを用いた半導体装置の製造方法。

【請求項１２】　前記選択性アルミニウム膜は、ＤＭＡＨ（Ｄｉｍｅｔｈｙｌａｌｕｍｉｎｕｍ，$(CH_3)_2AlH$）とH_2とを工程ガスとして使用し、ＤＭＡＨとH_2とのフロー量を各々０．０２～１ｓｌｍ（ｓｔａｎｄａｒｄ　ｌｉｔｅｒ／ｍｉｎ）と１～５０ｓｌｍで、工程温度は２５０～４５０℃で、圧力は１～１５０Ｔｏｒｒであることを特徴とする請求項７に記載のダマシーン金属ゲートを用いた半導体装置の製造方法。

【請求項１３】　前記凹所内にアルミニウム絶縁膜を形成するステップの前に洗浄工程を実行するステップを更に含むことを特徴とする請求項７に記載のダマシーン金属ゲートを用いた半導体装置の製造方法。

【請求項１４】　前記洗浄工程は、H_2SO_4とH_2O_2が（３０～５０）：１の比率で混合された混合溶液を用いて６０～１００℃の温度で５～２０分間の１次洗浄を行ない、５０～５００倍に希釈されたＨＦ溶液で２０～２００秒間の２次洗浄をすることを特徴とする請求項１３に記載のダマシーン金属ゲートを用いた半導体装置の製造方法。

【請求項１５】　前記アルミニウム膜を酸化させるステップは、酸素雰囲気で酸化させる方法、N_2Oプラズマ処理による酸化、または、ＵＶ・オゾン処理による酸化方法のいずれかを使用することを特徴とする請求項１１に記載のダマシーン金属ゲートを用いた半導体装置のゲート製造方法。

【請求項１６】　半導体基板上にダマシーンゲート酸化

膜とダマシーンゲート電極とを形成するステップと、
前記ダマシーンゲート電極を一定厚さだけエッチングして前記ダマシーンゲート電極の上部に凹所を形成するステップと、
前記ダマシーンゲート電極の上部の凹所内にドーピングされていないシリコン膜を形成するステップと、
前記シリコン膜を絶縁膜に変化させるステップと、
全体構造の上面に層間絶縁膜を形成するステップと、
前記層間絶縁膜をエッチングして半導体基板の一部分を露出させるコンタクトホールを形成するステップとを含むことを特徴とするダマシーン金属ゲートを用いた半導体装置の製造方法。

【請求項17】 前記シリコン膜は、LPCVDもしくはUHV-CVD法により選択的に凹所内のダマシーン金属ゲートの上部のみに成長させることを特徴とする請求項16に記載のダマシーン金属ゲートを用いた半導体装置の製造方法。

【請求項18】 前記シリコン膜の選択的成長工程は、SiH_4もしくはSi_2H_6のいずれかと、Clとを各々1～20sccm(standard cc/min)及び0.5～5sccm流し、圧力は1～10mTorr、温度は600～800℃で遂行されることを特徴とする請求項16に記載のダマシーン金属ゲートを用いた半導体装置の製造方法。

【請求項19】 前記シリコン膜の選択的成長の際、H_2を5～50sccmさらに付加することを特徴とする請求項18に記載のダマシーン金属ゲートを用いた半導体装置の製造方法。

【請求項20】 前記UHV-CVD法による選択的シリコン膜の成長工程前に初期圧力を7～10mTorrにしてポンピングし、0.5～5分程の真空洗浄工程を行なうことを特徴とする請求項17に記載のダマシーン金属ゲートを用いた半導体装置の製造方法。

【請求項21】 前記LPCVD法による選択的シリコン膜の成長工程は、DCS(dichlorosilane, $SiCl_2H_2$)、H_2及びHClのフロー量が各々0.1～2slm、10～150slmおよび0.1～3slmで、温度は750～850℃で、圧力は10～200Torrで進行されることを特徴とする請求項17に記載のダマシーン金属ゲートを用いた半導体装置の製造方法。

【請求項22】 前記LPCVD法による選択的シリコン膜の成長工程は、SiH_4、H_2及びHClのフロー量が各々0.1～2slm、10～150slmおよび0.2～4slmで、温度は750～850℃で、圧力は10～200Torrで進行されることを特徴とする請求項17に記載のダマシーン金属ゲートを用いた半導体装置の製造方法。

【請求項23】 前記LPCVD法による選択的シリコン膜の成長工程の前に、イン-シトウ(in-situ)洗浄を、温度850～950℃、水素雰囲気で1～5分間行なう方法、または、温度を瞬間的に950℃に上昇させてからシリコン成長温度に下降させる急速熱処理(Rapid Thermal Process)を用いた方法で行うことを特徴とする請求項17に記載のダマシーン金属ゲートを用いた半導体装置の製造方法。

【請求項24】 前記絶縁膜は、シリコン酸化膜もしくは窒化アルミニウム膜であることを特徴とする請求項16に記載のダマシーン金属ゲートを用いた半導体装置の製造方法。

【請求項25】 前記シリコン膜を酸化させる方法は、酸素雰囲気で酸化させる方法、N_2Oプラズマ処理による酸化、または、UV-オゾン処理による酸化方法のいずれかを用いることを特徴とする請求項24に記載のダマシーン金属ゲートを用いた半導体装置の製造方法。

【発明の詳細な説明】

【0001】

【発明が属する技術分野】本発明は、半導体装置の製造方法に関し、詳しくは、電気的ショートを防止することができるダマシーン金属ゲートを用いた半導体装置の製造方法に関する。

【0002】

【従来の技術】従来、この種半導体装置のゲート電極として、ポリシリコンゲート電極やポリサイドゲート電極等が使用されている。その中で、ポリシリコンゲート電極は、ゲート空乏化現象によるゲート絶縁膜の有効厚さの増加、p^+もしくはn^+ポリシリコンゲート電極から基板へのドーパント浸透現象及びドーパント分布変動によるしきい値電圧の変化等の問題がある。

【0003】また、従来のポリシリコンを用いたゲート電極は、微細線幅上でこれ以上の低抵抗値を達成することができないという問題がある。従って、従来のポリシリコンを用いるゲート電極に代替される新物質及び新構造のゲート電極に対する開発が求められている。

【0004】近年、このような要求により、金属ゲート電極に対する開発が積極的に推進されている。金属ゲート電極を使用する場合、ドーパントを使用しないので、既存のポリシリコンゲート電極から生じる問題が解決されるのみならず、金属ゲート電極としてワーク函数がシリコンのミッドバンドギャップに位置する金属を使用するので、NMOSトランジスタ及びPMOSトランジスタ領域で対称的にしきい値電圧を形成することができる単一ゲート電極を形成することができる。その際、金属ゲート電極の物質にはW、WN、Ti、TiN、MoおよびTa等が使用される。

【0005】一方、金属ゲート電極を用いる半導体装置を通常のポリシリコンゲート電極を用いた半導体装置の製造方法により製造する場合、金属ゲート電極をパターニングする困難さ、ソース/ドレインのためのイオン注入時におけるプラズマによる損傷及びイオン注入後にお

ける熱処理工程による熱的損傷が致命的な問題を招来する。

【０００６】上記のような金属ゲート電極の使用による工程上の問題を解決するため、金属ゲート電極を形成する新しいダマシーン金属ゲート工程が提示された。ダマシーン金属ゲート工程は、ポリシリコンゲートをダミーゲートとして形成した後、ソース／ドレイン領域を形成して、たとえばトランジスタを製造し、ダミーゲートとして形成されたポリシリコンゲートを除去した後、ダマシーン工程により金属ゲート電極を形成する工程である。

【０００７】このようなダマシーン金属ゲートを用いた従来の半導体装置の製造方法を図１乃至図７を参照して説明する。図１乃至図７は、従来のダマシーン金属ゲート電極を形成する製造工程を用いた半導体装置の製造方法を説明するための断面図である。

【０００８】従来のダマシーン金属ゲート形成工程を用いた半導体装置の製造方法は、図１に示すように、シリコン基板１１上に通常のポリシリコンゲート電極を形成する方法によりシリコン酸化膜とポリシリコン膜を形成した後、これらをパターニングしてダミーゲート絶縁膜１２とダミーゲート電極１３を形成する。続いて、ダミーゲート絶縁膜１２とダミーゲート電極１３の側壁にスペーサ１４を形成する。

【０００９】次に、図示しないが、スペーサ１４の両側の半導体基板１１にイオン注入工程を行なってソース／ドレイン領域（図示せず）を形成する。次に、図２、図３に示すように、層間絶縁膜１５を半導体基板１１の全面に形成した後、ＣＭＰ（ｃｈｅｍｉｃａｌ　ｍｅｃｈａｎｉｃａｌ　ｐｏｌｉｓｈｉｎｇ）工程を進行して層間絶縁膜１５を研磨してダミーゲート電極１３を露出させる。

【００１０】次に、図４に示すように、露出されたダミーゲート電極１３とその下部の露出されたダミーゲート絶縁膜１２とを選択的にエッチング方式により除去してダミーゲート電極１３とダミーゲート絶縁膜１２とが除去された部位に半導体基板１１を露出させる凹所１６を形成する。次に、図５に示すように絶縁膜１７と金属膜１８とを凹所１６を含む層間絶縁膜１５上に形成する。

【００１１】次に、図６に示すようにＣＭＰ工程を進行して絶縁膜１７と金属膜１８とを選択的に除去して層間絶縁膜１５を露出させる。その際、ダマシーンゲート絶縁膜１９とダマシーン金属ゲート電極２０が形成される。また、ダマシーンゲート絶縁膜１９で通常のシリコン酸化膜、Ta_2O_5 および Al_2O_3 等の通常のゲート絶縁物質を使用することが可能であり、ダマシーン金属ゲート電極２０の材質として前記タングステンを例に挙げたが、ＷＮ、Ｔｉ、ＴｉＮ、Ｍｏおよびタ等を選択的に使用することもできる。

【００１２】次に、図７に示すように、半導体基板１１を含む全体構造の全表面に層間絶縁膜２１が形成され、感光膜２２をマスクにして前記層間絶縁膜１５をエッチングしてソース／ドレイン領域が露出されるようにコンタクトホール２３、例えば、ビットラインコンタクトホールもしくはストレッジ電極用コンタクトホールを形成する。次に、図示しないが、金属配線もしくはメモリ装置の場合、ビットラインもしくはストレッジ電極ラインを形成し、コンタクトホール２３を通じてソース／ドレインと電気的に接続される。

【００１３】

【発明が解決しようとする課題】上記のような従来のダマシーン金属ゲート電極を用いた半導体装置の製造方法においては、次のような問題点がある。従来技術においては、ダマシーン金属ゲート電極がトランジスタのソース／ドレイン形成工程後に形成されるので、従来のダマシーン金属ゲート電極の形成工程から生じるソース／ドレイン用イオン注入時のプラズマ損傷及び後続熱処理工程による熱的損傷等の問題を解決することができた。しかし、従来の半導体装置の製造方法は、装置の高集積化に伴なってコンタクト露光工程から不整合が発生することにより、図７で示したように、ダマシーンゲート電極２０が露出されることになる。

【００１４】従って、図７のＡの部位で示すように、不整合によるダマシーンゲート電極２０の露出による後続工程で形成されるビットラインもしくはストレッジ電極ライン等と電気的ショートが発生するという深刻な問題点があった。

【００１５】そこで、本発明は、上記従来技術の問題点を解決するために案出されたもので、不整合によるダマシーンゲート電極の電気的ショート現象を防止することができるダマシーン金属ゲートを用いた半導体装置の製造方法を提供することを目的とする。

【００１６】

【課題を解決するための手段】上記目的を達成するためになされた、本発明によるダマシーン金属ゲートを用いた半導体装置の製造方法は、半導体基板上にダマシーンゲート酸化膜とダマシーンゲート電極とを形成するステップと、前記ダマシーンゲート電極を一定厚さだけ選択的にエッチングして前記ダマシーンゲート電極の上部に凹所を形成するステップと、前記ダマシーンゲート電極の上部の凹所内に絶縁膜を形成するステップと、前記全体構造の上面に層間絶縁膜を形成するステップと、前記層間絶縁膜を選択的にエッチングして前記半導体基板の一部分を露出させるコンタクトホールを形成するステップとを含んでなることを特徴とする。

【００１７】また、上記目的を達成するためになされた、本発明によるダマシーン金属ゲートを用いた半導体装置の製造方法は、半導体基板上にダマシーンゲート酸化膜とダマシーンゲート電極とを形成するステップと、前記ダマシーンゲート電極を一定厚さだけ選択的にエッ

チングして前記ダマシーンゲート電極の上部に凹所を形成するステップと、前記ダマシーンゲート電極の上部の凹所内のみにアルミニウム膜を選択的に成長させるステップと、前記アルミニウム膜をアルミニウム絶縁膜に変化させるステップと、前記全体構造の上面に層間絶縁膜を形成するステップと、前記層間絶縁膜を選択的にエッチングして前記半導体基板の一部分を露出させるコンタクトホール形成するステップとを含んでなることを特徴とする。

【００１８】また、上記目的を達成するためになされた、本発明によるダマシーン金属ゲートを用いた半導体装置の製造方法は、半導体基板上にダマシーンゲート酸化膜とダマシーンゲート電極とを形成するステップと、前記ダマシーンゲート電極を一定厚さだけエッチングして前記ダマシーンゲート電極の上部に凹所を形成するステップと、前記ダマシーンゲート電極の上部の凹所内にドーピングされていないシリコン膜を形成するステップと、前記シリコン膜を絶縁膜に変化させるステップと、全体構造の上面に層間絶縁膜を形成するステップと、前記層間絶縁膜をエッチングして半導体基板の一部分を露出させるコンタクトホールを形成するステップとを含むことを特徴とする。

【００１９】

【発明の実施の形態】次に、本発明にかかるダマシーン金属ゲートを用いた半導体装置の製造方法の実施の形態の具体例を図面を参照しながら説明する。図８乃至図１３は、本発明の第１の実施例によるダマシーン金属ゲートを用いた半導体装置の製造方法を説明するための断面図である。

【００２０】本発明の第１の実施例によるダマシーン金属ゲートを用いる半導体装置の製造方法は、図８に示すように、半導体基板３１上に通常のダマシーン金属ゲート工程を用いてダマシーンゲート酸化膜３２とダマシーンゲート電極３３とを形成する。その際、ダマシーンゲート電極３３用金属にはタングステン（Ｗ）、窒化タングステン（ＷＮ）、チタニウム（Ｔｉ）、窒化タンタニウム（ＴｉＮ）、モリブデン（Ｍｏ）、タンタリウム（Ｔａ）および窒化タンタリウム（ＴａＮ）等の電気伝導性を有する伝導体を使用する。また、ダマシーンゲート電極３３の厚さを２０００～２５００Åとする。

【００２１】次に、半導体基板３１の全面にダマシーンゲート電極３３が露出されるように、層間絶縁膜３６を形成した後、ＣＭＰ工程を遂行してダマシーンゲート電極３３が露出されるまで研磨する。その際、ダマシーン金属ゲートトランジスタは、ダマシーンゲート電極３３の両側の基板に通常のイオン注入工程によるソース／ドレイン領域３４が形成されており、ダマシーンゲート電極３３の側壁にはスペーサ３５が形成されている。

【００２２】次に、図９に示すように、露出されたダマシーンゲート電極３３を通常のドライエッチングもしくはウェットエッチング工程を通じてエッチングして、ダマシーンゲート電極３３の厚さの一部、例えば、５００～１０００Åをリセスエッチングしてダマシーンゲート電極３３ａの上部に凹所３７を形成する。

【００２３】次に、図１０に示すように、ＭＯＣＶＤ（ｍｅｔａｌ　ｏｒｇａｎｉｃ　ｃｈｅｍｉｃａｌ　ｖａｐｏｒ　ｄｅｐｏｓｉｔｉｏｎ）方法により、凹所３７の内部のゲート電極３３ａ上のみに選択的に導電体膜、例えば、アルミニウム膜３８を成長させる。その際、ＭＯＣＶＤ方法による選択的アルミニウム膜３８の成長は、必ず電荷伝達（ｃｈａｒｇｅ　ｔｒａｎｓｆｅｒ）を通じてなされるので、不導体である層間絶縁膜３６上にはアルミニウム膜の成長が抑制され、導体であるゲート電極３３ａ上のみで選択的にアルミニウム膜３８が成長される。

【００２４】前記アルミニウム膜３８の選択的成長に対し、より詳細に説明すると次の通りである。まず、アルミニウム膜３８が選択的に成長できるように成長前に洗浄工程を行なう。その際、洗浄工程はダマシーンゲート電極３３ａが露出された状態で有機物成分の不純物を除去することができるH_2SO_4とH_2O_2とを用いて行なう。

【００２５】まず、H_2SO_4とH_2O_2とが（３０～５０）：１の比率で混合された混合溶液に５～２０分間の１次洗浄を行なう。その際、温度は６０～１００℃である。次に、５０～５００倍に希釈されたＨＦ領域（ｄｉｌｕｔｅｄ　ＨＦ）で２０～２００秒間の２次洗浄工程を行なう。

【００２６】次に、洗浄工程後、アルミニウム膜３８を低圧ＭＯＣＶＤ法によりＤＭＡＨ（Ｄｉｍｅｔｈｙｌａｌｕｍｉｎｕｍ，$(CH_3)_2AlH$）とH_2を工程ガスとして用いて成長させる。その際、工程温度は、２５０～４５０℃で、圧力は１～１５０Ｔｏｒｒ、ＤＭＡＨとH_2とのフロー（ｆｌｏｗ）量は、各々０．０２～１ｓｌｍと１～５０ｓｌｍである。一方、選択的アルミニウム成長は、工程ガスであるH_2なしに成長させることができる。

【００２７】次に、図１１に示すように、アルミニウム膜３８を成長させた後、ダマシーンゲート電極３３ａの上部の凹所３７（図９）内に絶縁膜３９を形成する。その際、一例として、凹所３７内に形成されたアルミニウム膜３８を酸化させて凹所３７内に絶縁膜として酸化アルミニウム膜（Al_2O_3）を形成する。また、アルミニウム膜３８を酸化させる方法では、酸素雰囲気で酸化させる方法、N_2Oプラズマ処理による酸化方法、ＵＶ－オゾン（ＵＶ－O_3）処理による酸化方法等を選択的に用いることができる。

【００２８】また、凹所３７内に絶縁膜３９を形成する別の一例として、前記アルミニウム膜３８を通常の窒化処理（ｎｉｔｒｉｄａｔｉｏｎ）により窒化させて窒化

アルミニウム膜（ＡｌＮ）を形成する。このようにして、ダマシーン金属ゲート電極３３ａの上部に窒化アルミニウム膜もしくは酸化アルミニウム膜のような絶縁膜３９を形成することにより、ダマシーンゲート電極３３ａは露出されることなく絶縁膜３９により被覆されることになる。

【００２９】次に、図１２に示すようにダマシーンゲート電極３３ａを含んだ半導体基板３１の全面に層間絶縁膜４０を形成する。次に、図１３に示すように、感光膜４１をマスクにして、その下部の層間絶縁膜４０をソース／ドレイン領域３４が露出されるように選択的にエッチングしてコンタクトホール４２を形成する。その際、コンタクトホール４２は、本発明の半導体装置の製造方法がＤＲＡＭのようなメモリ装置に適用される場合はビットライン用コンタクトもしくはストレッジ電極用コンタクトに使用される。また、コンタクトホール４２の形成工程の際、不整合が発生してもダマシーンゲート電極３３ａの上部が絶縁膜３９により覆われているので、ダマシーンゲート電極３３ａは露出されない。

【００３０】従って、図示しないが、後続工程でビットラインもしくはストレッジ電極ラインを形成しても、不整合による電気的ショートを発生させることなく、ビットラインもしくはストレッジ電極ラインとソース領域とをコンタクトホール４２を通じて電気的に接続させることができる。

【００３１】次に、本発明の第２の実施例を図１４乃至図１９を参照して説明する。図１４乃至図１９は、本発明の第２の実施例によるダマシーン金属ゲートを用いた半導体装置の製造方法を説明するための断面図である。同図において、図８乃至図１３と同一もしくは相当部分には同一符号を付して、その詳しい説明を省略する。

【００３２】すなわち、図１４乃至図１９に示すように、ダマシーンゲート電極５３ａの上部の凹所にアルミニウム膜に代えて選択的にドーピングされなかったシリコン膜５８を成長させた後、酸化もしくは窒化処理して絶縁膜５９としてシリコン酸化膜もしくはシリコン窒化膜を形成する以外には同一である。

【００３３】まず、図１４及び図１５に示すように、図８および図９で説明したのとほぼ同様に、ダマシーンゲート酸化膜５２及びダマシーンゲート電極５３を形成した後、ダマシーンゲート電極５３の一部をエッチングして凹所５７を形成する。

【００３４】次に、図１６で示すシリコン膜５８をダマシーンゲート電極５３ａの上部の凹所５７内のみに選択的に成長させる方法について説明する。まず、シリコンが選択的に成長できるように成長前に洗浄工程を行なう。ダマシーンゲート電極５３ａが露出された状態で有機物成分の不純物を除去することができるH_2SO_4とH_2O_2とを用いて１次洗浄する。その際、H_2SO_4とH_2O_2とが（３０～５０）：１の比率で混合された混合溶液にて５～２０分間、１次洗浄を行なう。また、１次洗浄の際の温度は６０～１００℃である。次に、５０～５００倍に希釈されたＨＦ領域（ｄｉｌｕｔｅｄ ＨＦ）で２０～２００秒間に２次洗浄工程を行なう。

【００３５】次に、洗浄工程後、シリコン膜をＣＶＤ法により選択的に成長させる。その際、選択的シリコン成長（Ｓｅｌｅｃｔｉｖｅ Ｓｉｌｉｃｏｎ Ｇｒｏｗｔｈ）方法では、ＣＶＤ装備により２つの方法がある。１つは、ＬＰＣＶＤ（ｌｏｗ ｐｒｅｓｓｕｒｅ ｃｈｅｍｉｃａｌ ｖａｐｏｒ ｄｅｐｏｓｉｔｉｏｎ）法を用いた選択的シリコン成長方法で、気相内の化学的イオン化（ｃｈｅｍｉ－ｉｏｎｉｚａｔｉｏｎ）効果により電荷を含んでいる微小蒸着物等が形成され、これらは引力（ａｔｔｒａｃｔｉｖｅ ｆｏｒｃｅ）を受けることができる伝導体のみに成長が触発されてドーピングされていないシリコン膜５８が層間絶縁膜５６上では成長が抑制され、ダマシーン金属ゲート電極５３ａ上のみに選択的に成長される。

【００３６】その際、ＬＰＣＶＤ法によるシリコン膜５８の成長条件は、工程ガスとしてＤＣＳ（ｄｉｃｈｌｏｒｏｓｉｌａｎｅ，$SiCl_2H_2$）、ＨＣｌおよびH_2が使用され、その各々のフロー量は、ＤＣＳが０．１～２ｓｌｍ、ＨＣｌは０．１～３ｓｌｍ、H_2は１０～１５０ｓｌｍであり、工程温度は７５０～８５０℃で、圧力は１０～２００Ｔｏｒｒである。

【００３７】一方、シリコン膜５８の選択的成長の際、イン・シトウ洗浄工程（ｉｎ－ｓｉｔｕ ｃｌｅａｎｉｎｇ）を行なう。その際、イン・シトウ洗浄工程は、８５０～９５０℃の水素雰囲気で１～５分間行なうか、または、温度を瞬間的に９５０℃程度に上昇させてから、シリコン成長温度で加工させる急速熱処理（ＲＴＰ，ｒａｐｉｄ ｔｈｅｒｍａｌ ｐｒｏｃｅｓｓ）方法を用いて行なう。そして、シリコン膜５８の選択的成長のための工程ガスとしてＤＣＳに代わり、SiH_4を使用することもできるが、その際、圧力と温度はＤＣＳと同じ工程条件で遂行され，工程ガスのフロー量はSiH_4が０．１～２ｓｌｍで、ＨＣｌは０．２～４ｓｌｍ、H_2は１０～１５０ｓｌｍである。

【００３８】一方、選択的シリコン成長方法中、もう１つは、ＵＨＶ－ＣＶＤ方法により伝導体と非伝導体との間の初期核生成速度により純粋な選択的成長の幅が決定される。その際、工程ガスとしては、SiH_4もしくはSi_2H_6とＣｌを使用し、かつ、SiH_4もしくはSi_2H_6のフロー量は１～２０ｓｃｃｍを流し、Ｃｌは０．５～５ｓｃｃｍで、圧力は１～１０ｍＴｏｒｒ、温度は６００～８００℃である。また、必要に応じてH_2を５～５０ｓｃｃｍ程度入れることができる。また、ＵＨＶ－ＣＶＤ方法では、シリコン膜を成長させる前に初期圧力を７～１０Ｔｏｒｒでポンピングし、０．５～５分程の真空洗浄（ｖａｃｕｕｍ ｃｌｅａｎｉｎｇ）を

行なわなければならない。

【００３９】次に、図１７に示すように、図１１で説明したような方法で酸化もしくは窒化工程を行なって、シリコン膜５８を酸化もしくは窒化させて、ダマシーン金属ゲート電極５３ａの上部に酸化膜もしくは窒化膜のような絶縁膜５９を形成することにより、ダマシーンゲート電極５３ａは露出されることなく絶縁膜５９により被覆されることになる。

【００４０】次に、図１８に示すように、ダマシーンゲート電極５３ａを含んだ半導体基板３１の全面に層間絶縁膜６１を形成する。次に、図１９に示すように、感光膜６３をマスクにして、その下部の層間絶縁膜６１をソース／ドレイン領域５４が露出されるようにエッチングしてコンタクトホール６５を形成する。その際、コンタクトホール形成工程時に不整合が発生してもダマシーンゲート電極５３ａの上部が絶縁膜５９により覆われているので、ダマシーンゲート電極５３ａは露出されない。

【００４１】従って、図示しないが、後続工程でビットラインもしくはストレッジ電極ラインを形成しても不整合による電気的ショートの発生なしにビットラインもしくはストレッジ電極ラインとソース領域とをコンタクトホール６５を通じて電気的に接続させる。

【００４２】尚、本発明は、本実施例に限られるものではない。本発明の趣旨から逸脱しない範囲内で多様に変更実施することが可能である。

【００４３】

【発明の効果】上述のように、本発明によるダマシーン金属ゲートを用いた半導体装置の製造方法においては、ダマシーン金属ゲート電極の上部に絶縁膜を形成することにより、コンタクトホールの形成の際、不整合が発生してもダマシーンゲート電極と後続工程で形成される配線、例えば、ビットラインもしくはストレッジ電極ラインとの電気的ショートを防止することができる利点がある。従って、本発明のダマシーンゲートを用いた半導体装置の製造方法は、優れた特性を有する半導体装置を製造することができる。

【図面の簡単な説明】

【図１】従来のダマシーン金属ゲートを用いた半導体装置の製造方法を説明するための断面図である。

【図２】従来のダマシーン金属ゲートを用いた半導体装置の製造方法を説明するための断面図である。

【図３】従来のダマシーン金属ゲートを用いた半導体装置の製造方法を説明するための断面図である。

【図４】従来のダマシーン金属ゲートを用いた半導体装置の製造方法を説明するための断面図である。

【図５】従来のダマシーン金属ゲートを用いた半導体装置の製造方法を説明するための断面図である。

【図６】従来のダマシーン金属ゲートを用いた半導体装置の製造方法を説明するための断面図である。

【図７】従来のダマシーン金属ゲートを用いた半導体装置の製造方法を説明するための断面図である。

【図８】本発明の第１の実施例によるダマシーン金属ゲートを用いた半導体装置の製造方法を説明するための断面図である。

【図９】本発明の第１の実施例によるダマシーン金属ゲートを用いた半導体装置の製造方法を説明するための断面図である。

【図１０】本発明の第１の実施例によるダマシーン金属ゲートを用いた半導体装置の製造方法を説明するための断面図である。

【図１１】本発明の第１の実施例によるダマシーン金属ゲートを用いた半導体装置の製造方法を説明するための断面図である。

【図１２】本発明の第１の実施例によるダマシーン金属ゲートを用いた半導体装置の製造方法を説明するための断面図である。

【図１３】本発明の第１の実施例によるダマシーン金属ゲートを用いた半導体装置の製造方法を説明するための断面図である。

【図１４】本発明の第２の実施例によるダマシーン金属ゲートを用いた半導体装置の製造方法を説明するための断面図である。

【図１５】本発明の第２の実施例によるダマシーン金属ゲートを用いた半導体装置の製造方法を説明するための断面図である。

【図１６】本発明の第２の実施例によるダマシーン金属ゲートを用いた半導体装置の製造方法を説明するための断面図である。

【図１７】本発明の第２の実施例によるダマシーン金属ゲートを用いた半導体装置の製造方法を説明するための断面図である。

【図１８】本発明の第２の実施例によるダマシーン金属ゲートを用いた半導体装置の製造方法を説明するための断面図である。

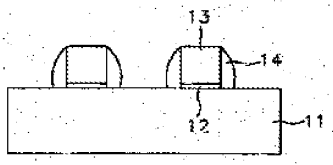
【図１９】本発明の第２の実施例によるダマシーン金属ゲートを用いた半導体装置の製造方法を説明するための断面図である。

【符号の説明】

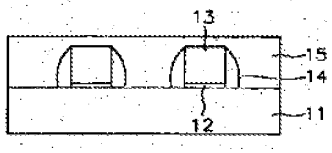
３１、５１　　半導体基板
３２、５２　　ダマシーンゲート酸化膜
３３、３３ａ、５３、５３ａ　ダマシーンゲート電極
３４、５４　　ソース／ドレイン領域
３５、５５　　スペーサ
３６、５６　　層間絶縁膜
３７、５７　　凹所
３８　　アルミニウム膜
３９　　絶縁膜（窒化（酸化）アルミニウム膜）
４０、６１　　層間絶縁膜
４１、６３　　感光膜
４２、６５　　コンタクトホール

58　　シリコン膜　　59　　絶縁膜（シリコン酸化（窒化）膜）

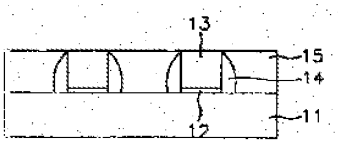
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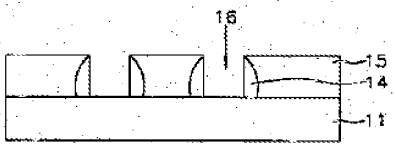
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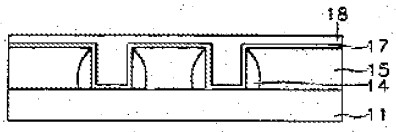
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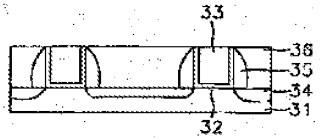
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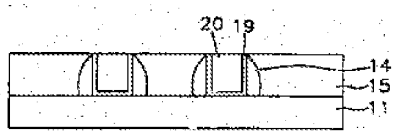
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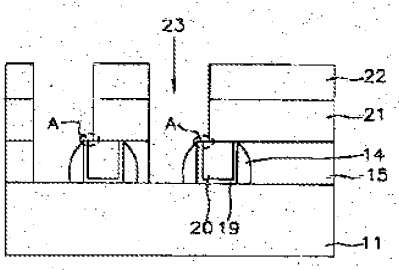
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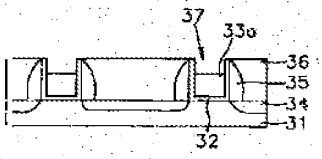
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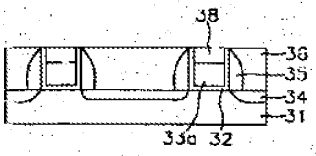
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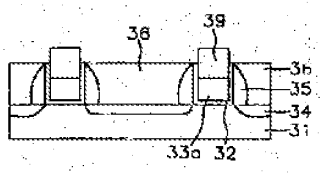
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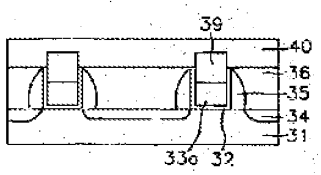
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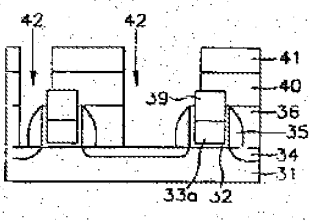
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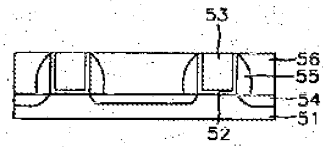
【図12】



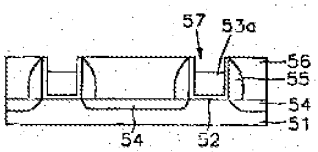
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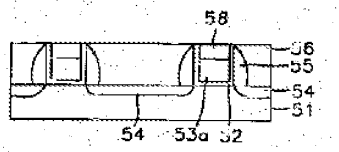
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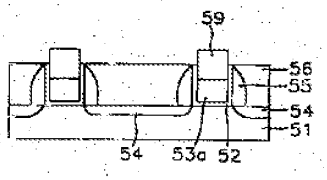
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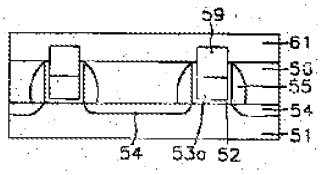
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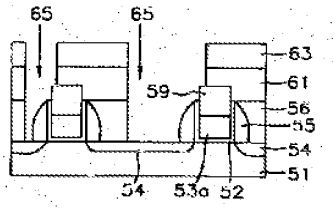
【図17】



【図18】



【図19】



フロントページの続き

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BB32 BB33 CC05 DD03 DD04
DD08 EE05 EE09 EE14 EE16
GG09 GG10 GG14 GG16 HH20
5F033 HH18 HH19 HH20 HH21 HH32
HH33 HH34 KK01 MM01 QQ89
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WW03 XX15 XX31
5F140 AA14 AC32 BF01 BF07 BF10
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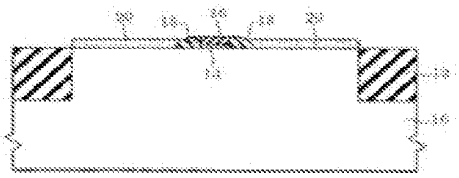
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(22)Date of filing : 04.10.2002

(71)Applicant : SEIKO EPSON CORP
(72)Inventor : KANEMOTO HIROSHI

(54) METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a method for manufacturing a semiconductor device capable of forming a highly precise impurity layer without being affected by the thermal treatment in an epitaxial growing process.
SOLUTION: In a method for manufacturing a semiconductor device, a dummy gate layer 16 is formed above a semiconductor substrate 10. A spacer layer 18 is formed so as to be made adjacent to the both side faces of the dummy gate layer 16 above the semiconductor substrate 10. A silicon layer 20 is selectively formed by epitaxial growth above the semiconductor substrate 10. A dummy gate 16 is removed, and a gate electrode 26 is formed. Impurity is introduced through the silicon layer 20 to the semiconductor substrate 10 so that a source/drain area 34 can be formed. Furthermore, the silicon layer 20 is silicided.



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H01L 29/423	H01L 29/50	M	
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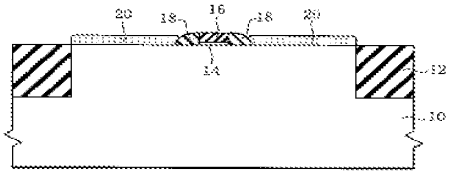
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(22)出願日　平成14年10月4日(2002.10.4)

(71)出願人　000002369
セイコーエプソン株式会社
東京都新宿区西新宿２丁目４番１号
(74)代理人　100090479
弁理士　井上　一
(74)代理人　100090387
弁理士　布施　行夫
(74)代理人　100090398
弁理士　大渕　美千栄
(72)発明者　金本　啓
長野県諏訪市大和３丁目３番５号　セイコーエプソン株式会社内

最終頁に続く

(54)【発明の名称】半導体装置の製造方法

(57)【要約】
【課題】エピタキシャル成長の工程での熱処理の影響を受けずに濃度の高い不純物層を形成できる、半導体装置の製造方法を提供する。
【解決手段】半導体装置の製造方法では、半導体基板１０の上方にダミーゲート層１６を形成する。半導体基板１０の上方に、ダミーゲート層１６の両側面に隣接してスペーサ層１８を形成する。半導体基板１０の上方にシリコン層２０をエピタキシャル成長によって選択的に形成する。ダミーゲート層１６を除去した後、ゲート電極２６を形成する。シリコン層２０を介して半導体基板１０に不純物を導入してソース／ドレイン領域３４を形成する。さらに、シリコン層２０をシリサイド化する。
【選択図】　図２



【特許請求の範囲】
【請求項１】
半導体基板の上方にダミーゲート層を形成し、
前記半導体基板の上方に、前記ダミーゲート層の両側面に隣接してスペーサ層を形成し、
前記半導体基板の上方にシリコン層をエピタキシャル成長によって選択的に形成し、
前記ダミーゲート層を除去した後、ゲート電極を形成し、
前記シリコン層を介して前記半導体基板に不純物を導入してソース／ドレイン領域を形成し、
前記シリコン層をシリサイド化すること、を含む、半導体装置の製造方法。
【請求項２】
半導体基板に素子分離絶縁層を形成し、
前記半導体基板の上方にダミーゲート層を形成し、
前記半導体基板の上方に、前記ダミーゲート層の両側面に隣接してスペーサ層を形成し、
前記半導体基板の上方にシリコン層をエピタキシャル成長によって選択的に形成し、
前記ダミーゲート層を除去した後、ゲート電極を形成し、
前記スペーサ層を除去した後、イオン注入によって、該スペーサが除去された領域の前記半導体基板に不純物を導入してエクステンション領域を形成し、
前記ゲート電極の両側面に隣接するサイドウォール絶縁層を形成し、
イオン注入によって、前記シリコン層を介して前記半導体基板に不純物を導入してソース／ドレイン領域を形成し、
前記シリコン層をシリサイド化すること、を含む、半導体装置の製造方法。
【請求項３】
請求項２において、
前記スペーサ層は、前記ダミーゲート層と異なる材料を前記半導体基板の上に堆積させた後、異方性エッチングを行うことにより形成される、半導体装置の製造方法。
【請求項４】
請求項２または３において、
前記シリコン層を形成した後、該シリコン層の表面に、熱酸化によって酸化シリコンからなるストッパ層を形成することを含む、半導体装置の製造方法。
【請求項５】
半導体基板に素子分離絶縁層を形成し、
前記半導体基板の上方に絶縁層を形成した後、所定領域に溝を形成し、
前記半導体基板の上方にダミーゲート層を形成し、該ダミーゲート層は、下部が前記溝内にあり、上部は前記溝より大きい幅を有し、該上部の側面は前記溝より外側に位置し、
前記ダミーゲート層をマスクとして前記絶縁層をパターニングし、前記半導体基板の上方に、前記ダミーゲート層の両側面に隣接するスペーサ層を形成し、
前記半導体基板の上方にシリコン層をエピタキシャル成長によって選択的に形成し、
前記ダミーゲート層を除去した後、ゲート電極を形成し、
前記スペーサ層を除去した後、イオン注入によって、該スペーサ層が除去された領域の前記半導体基板に不純物を導入してエクステンション領域を形成し、
前記ゲート電極の両側面に隣接するサイドウォール絶縁層を形成し、
イオン注入によって、前記シリコン層を介して前記半導体基板に不純物を導入してソース／ドレイン領域を形成し、
前記シリコン層をシリサイド化すること、を含む、半導体装置の製造方法。
【請求項６】
請求項５において、
前記シリコン層を形成した後、該シリコン層の表面に、熱酸化によって酸化シリコンからなるストッパ層を形成することを含む、半導体装置の製造方法。
【発明の詳細な説明】
【０００１】

【発明の属する技術分野】
本発明は、半導体装置の製造方法に関し、特に選択エピタキシャル成長によりソース／ドレイン領域の上にシリコン層を形成する、エレベーテッド・ソース／ドレイン（Ｅｌｅｖａｔｅｄ　Ｓｏｕｒｃｅ／Ｄｒａｉｎ）技術を用いる半導体装置の製造方法に関する。
【０００２】
【背景技術および発明が解決しようとする課題】
エレベーテッド・ソース／ドレイン技術では、半導体基板に形成されたソース／ドレイン領域の上に、エピタキシャル成長によって単結晶シリコン層を形成し、このシリコン層においてシリサイド化を行い、半導体基板の上にシリサイド層を形成する。このようにすることで、ソース／ドレイン領域の不純物層を浅くすることができ、素子の微細化に対応できる。
【０００３】
ところで、かかるエレベーテッド・ソース／ドレイン技術では、通常、シリコンをエピタキシャル成長で形成する工程で７００℃以上の熱処理を必要とする。そのため、あらかじめイオン注入などによって形成された、ソース／ドレイン領域などの不純物プロファイルが変化してしまい、設計通りの不純物層を形成することが困難な場合がある。
【０００４】
また、メタルゲートを用いる場合には、メタルゲートを形成した後に上述した７００℃以上の熱処理を行うと、界面反応によってメタルゲートの成分とゲート絶縁層の成分とが反応してゲート絶縁層の特性が劣化する問題を生じる。
【０００５】
本発明の目的は、上述したエピタキシャル成長の工程での熱処理の影響を受けずに精度の高い不純物層を形成できる、半導体装置の製造方法を提供することにある。
【０００６】
【課題を解決するための手段】
本発明にかかる製造方法は、半導体基板の上方にダミーゲート層を形成し、
前記半導体基板の上方に、前記ダミーゲート層の両側面に隣接してスペーサ層を形成し、
前記半導体基板の上方にシリコン層をエピタキシャル成長によって選択的に形成し、
前記ダミーゲート層を除去した後、ゲート電極を形成し、
前記シリコン層を介して前記半導体基板に不純物を導入してソース／ドレイン領域を形成し、
前記シリコン層をシリサイド化すること、を含む。
【０００７】
本発明によれば、エピタキシャル成長によってシリコン層を形成した後に、ゲート電極を形成し、さらにソース／ドレイン領域を形成する。したがって、エピタキシャル成長の工程で行われる高温のアニール処理の影響を受けずに不純物層を形成できるので、不純物の拡散を抑制でき、設計通りの不純物プロファイルを有する浅いソース／ドレイン領域を形成できる。また、エピタキシャル成長の工程で行われる高温のアニール処理の影響を受けずにゲート電極を形成できるので、ゲート電極の材料としてポリシリコンのみならずタンタルなどの金属を採用でき、ゲート電極の材料の選択性が広くなる。
【０００８】
本発明において、半導体基板の上方に特定の層を形成するとは、半導体基板上に直接特定の層を形成する場合と、半導体基板上の他の層を介して特定の層を形成する場合とを含む。本発明において、「シリコン層」とは、主成分がシリコン単体の場合のみならず、シリコンに他の物質、たとえばゲルマニウムが含まれていてもよい。また、「ソース／ドレイン領域」とは、ソース領域またはドレイン領域を意味する。
【０００９】
本発明の製造方法は、より具体的に以下の態様をとることができる。
【００１０】
第１の態様にかかる発明は、半導体基板に素子分離絶縁層を形成し、

前記半導体基板の上方にダミーゲート層を形成し、
前記半導体基板の上方に、前記ダミーゲート層の両側面に隣接してスペーサ層を形成し、
前記半導体基板の上方にシリコン層をエピタキシャル成長によって選択的に形成し、
前記ダミーゲート層を除去した後、ゲート電極を形成し、
前記スペーサ層を除去した後、イオン注入によって、該スペーサが除去された領域の前記半導体基板に不純物を導入してエクステンション領域を形成し、
前記ゲート電極の両側面に隣接するサイドウォール絶縁層を形成し、
イオン注入によって、前記シリコン層を介して前記半導体基板に不純物を導入してソース／ドレイン領域を形成し、
前記シリコン層をシリサイド化すること、を含むことができる。

【００１１】
この発明において、前記スペーサ層は、前記ダミーゲート層と異なる材料を前記半導体基板の上方に堆積させた後、異方性エッチングを行うことにより形成できる。

【００１２】
第２の態様にかかる発明は、
半導体基板に素子分離絶縁層を形成し、
前記半導体基板の上方に絶縁層を形成した後、所定領域に溝を形成し、
前記半導体基板の上方にダミーゲート層を形成し、該ダミーゲート層は、下部が前記溝内にあり、上部は前記溝より大きい幅を有し、該上部の側面は前記溝より外側に位置し、
前記ダミーゲート層をマスクとして前記絶縁層をパターニングし、前記半導体基板の上方に、前記ダミーゲート層の両側面に隣接するスペーサ層を形成し、
前記半導体基板の上方にシリコン層をエピタキシャル成長によって選択的に形成し、
前記ダミーゲート層を除去した後、ゲート電極を形成し、
前記スペーサ層を除去した後、イオン注入によって、前記スペーサ層が除去された領域の前記半導体基板に不純物を導入してエクステンション領域を形成し、
前記ゲート電極の両側面に隣接するサイドウォール絶縁層を形成し、
イオン注入によって、前記シリコン層を介して前記半導体基板に不純物を導入してソース／ドレイン領域を形成し、
前記シリコン層をシリサイド化すること、を含むことができる。

【００１３】
第１および第２の態様の発明において、前記シリコン層を形成した後、該シリコン層の表面に熱酸化によって酸化シリコンからなるストッパ層を形成することを含むことができる。この方法によれば、シリコン層をエッチングから保護するためのストッパ層を選択的に形成できる。

【００１４】
【発明の実施の形態】
以下、図面を参照しながら本発明の実施の形態を説明する。

【００１５】
［第１の実施の形態］
図１～図８は、第１の実施の形態に係る製造方法を示す断面図である。

【００１６】
（ａ）図１に示すように、シリコンなどの半導体基板１０に、素子分離絶縁層１２を形成する。素子分離絶縁層１２は、公知の方法によって形成することができる。素子分離絶縁層１２は、たとえば、シャロートレンチアイソレーション技術を用いて形成することができる。

【００１７】
ついで、熱酸化法によって半導体基板１０の表面に酸化シリコン層を形成する。ついで、この酸化シリコン層上にＣＶＤ法等を用いて窒化シリコン層を形成する。その後、酸化シリコン層および窒化シリコン層を公知のリソグラフィ（例えば光、Ｘ線あるいは電子ビームを用いたリソグラフィ）およびエッチング（例えば反応性イオンエッチング）によって

パターニングすることにより、保護層１４とダミーゲート層１６とを形成する。保護層１４の幅は、ゲート長に相当する。

【００１８】

この工程で形成される保護層１４は、後のダミーゲート層１６のエッチング工程（ｄ）において半導体基板１０を保護する機能を有する。保護層１４の膜厚は、この保護機能を有し、かつできるだけ容易に除去されるように設定される。これらのことを考慮すると、保護層１４は、数ｎｍ～１０ｎｍの膜厚を有することができる。なお、保護層１４が無くても問題のない場合には、これを設けなくともよい。また、ダミーゲート層１６の膜厚は、後のゲート電極の形成工程（ｅ）における電極材料の埋込み性などを考慮して設定される。ダミーゲート層１６は、例えば１０～１００ｎｍの膜厚を有することができる。

【００１９】

ついで、ダミーゲート層１６の両側面に接してスペーサ層１８を形成する。スペーサ層１８は、ＣＶＤ法などを用いて酸化シリコン層を基板上に堆積した後、反応性イオンエッチングなどの異方性エッチングを行うことにより形成することができる。したがって、スペーサ層１８は、エッチングにおいてダミーゲート層１６に対して充分に異なる選択比をとれるように、ダミーゲート層１６と異なる材料によって形成される。本実施の形態では、ダミーゲート層１６は窒化シリコン層から構成され、スペーサ層１８は酸化シリコン層から構成されている。

【００２０】

（ｂ）図２に示すように、半導体基板１０上に、エピタキシャル成長によってシリコン層２０を選択的に形成する。シリコン層２０は、半導体基板１０上においてシリサイド化されるのに必要な膜厚と、つぎの酸化シリコン層（ストッパ層）の形成工程（ｃ）での熱酸化に必要な膜厚とを考慮して決めることができる。シリコン層２０の膜厚は、このような点を考慮すると、５０～１００ｎｍとすることができる。

【００２１】

シリコン層２０は、公知のエピタキシャル成長によって形成できる。シリコン層２０は、例えば、以下のように形成される。まず、半導体基板１０の表面をＲＣＡ洗浄などの公知の方法で洗浄する。ＲＣＡ洗浄は、自然酸化膜を希フッ酸などを用いたライトエッチングで除去する工程を最後に含む。ついで、水素雰囲気中または真空中で半導体基板１０に熱処理を施すことにより、半導体基板１０の表面の酸化膜を完全に除去する。ついで、８００℃以上の温度で半導体基板１０を加熱した状態で、SiH_xCl_{4-x}（Ｘ＝０～４）、Si_2H_6、Si_3H_8、GeH_4、H_2、Cl_2などガスを成膜装置内に供給する。これにより、シリコンからなる半導体基板１０の露出部分にエピタキシャル成長によって選択的にシリコン層２０を形成することができる。

【００２２】

（ｃ）図３に示すように、熱酸化法によって、シリコン層２０の表面に酸化シリコン層からなるストッパ層２２を選択的に形成する。ストッパ層２２は、後の工程（ｅ）のエッチングにおいてシリコン層２０を保護する機能を有する。このような機能を考慮すると、ストッパ層２２は、３～２０ｎｍの膜厚を有することができる。

【００２３】

（ｄ）図４に示すように、窒化シリコン層からなるダミーゲート層１６を熱リン酸によってエッチングして除去する。この工程では、半導体基板１０は酸化シリコン層からなる保護層１４で覆われ、また、シリコン層２０は酸化シリコン層からなるストッパ層２２とスペーサ層１８とによって覆われているため、いずれも熱リン酸によるエッチングでダメージを受けることがない。ついで、保護層１４を希フッ酸によるライトエッチングで除去し、半導体基板１０を露出させる。

【００２４】

（ｅ）図５に示すように、ゲート絶縁層２４、ゲート電極２６およびキャップ層２８を形成する。ゲート絶縁層２４としては、酸化シリコン、酸化窒化シリコン、窒化シリコンの他、酸化タンタルなどの高誘電体を用いることができる。ゲート電極２６としては、ポリ

シリコンあるいはタングステン、タンタルなどの金属を用いることができる。キャップ層２８としては、酸化シリコン、窒化シリコンなどを用いることができる。ゲート電極２６としてタンタルなどの金属を用いた場合には、かかる金属の酸化を防止するために、キャップ層は酸素を含まない窒化シリコンなどを用いることが好ましい。キャップ層２８は、ゲート電極２６のエッチング後のプロセスでゲート電極２６の酸化を防止する機能を有する。

【００２５】

本実施の形態では、ダミーゲート層１６を除去した後の溝部にゲート電極２６を形成するので、この溝部が完全に埋め込まれるようにマスクのアライメントなどを考慮して、ゲート電極２６の幅（上部の幅）は溝部の幅より大きく設定されている。

【００２６】

ゲート電極２６としてタンタルを用いる場合には、ゲート絶縁層２４として窒化シリコン層を用い、ゲート電極２６として第１窒化タンタル層／タンタル層／第２窒化タンタル層の積層構造を用い、キャップ層２８として窒化シリコンを用いることができる。この場合、ゲート絶縁層２４、ゲート電極２６およびキャップ層２８は、たとえば、プラズマＣＶＤあるいは高密度プラズマ、アトミックレイヤーデポジション法、スパッタ法でゲート絶縁層を形成し、スパッタ法あるいはプラズマＣＶＤ、高密度プラズマでゲート電極およびキャップ層を形成した後、反応性イオンエッチングなどのドライエッチングによりパターニングを行うことで形成できる。ゲート電極２６において、第１窒化タンタル層は主に仕事関数制御層として機能し、第２窒化タンタル層は耐酸化機能を有する。かかる積層構造のタンタルゲート電極の例は、特開２００１－２９８１９３号公報に記載されている。

【００２７】

この工程では、シリコン層２０はストッパ層２２とスペーサ層１８とによって覆われているため、ゲート電極２６のエッチング時にダメージを受けることがない。

【００２８】

（ｆ）図６に示すように、酸化シリコンからなるスペーサ層１８を例えば希フッ酸によってエッチングする。このとき、シリコン層２０上のストッパ層２２も同時にエッチングされる。ついで、斜めイオン注入によって半導体基板１０の露出部（スペーサ層１８が除去された領域）に不純物を導入して、エクステンション領域３０を形成する。エクステンション領域３０は、つぎの工程（ｇ）で形成されるソース／ドレイン領域より浅く形成される。

【００２９】

（ｇ）図７に示すように、ゲート絶縁層２４、ゲート電極２６およびキャップ層２８の両側面にサイドウォール絶縁層３２を形成する。サイドウォール絶縁層３２は、酸化シリコン層、窒化シリコン層などの絶縁層をＣＶＤ法によって半導体基板１０上に全面的に形成した後、反応性イオンエッチングなどの異方性エッチングを行うことにより形成される。ゲート電極２６としてタンタルなどの金属を用いる場合には、かかる金属の酸化を防止するために、酸素を含まない窒化シリコン層を用いることが好ましい。

【００３０】

ついで、イオン注入（図示の例では斜めイオン注入）によって、シリコン層２０を介して半導体基板１０に不純物を導入し、ソース／ドレイン領域３４を形成する。そして、アニールを行うことによりソース／ドレイン領域の不純物を活性化させる。このときのアニール温度は、不純物の熱拡散を抑制し、ゲート電極に悪影響を与えない程度の温度で行われることが望ましい。特に、ゲート電極２６としてタンタルなどの金属を用いた場合には、低温アニール（４５０～６００℃）を行うことが望ましい。ゲート電極２６としてタンタルなどの金属を用いた場合には、約７００℃以上の高温に晒されると、この金属とゲート絶縁層とが反応して所望のゲート構造を得ることができないことがある。

【００３１】

（ｈ）図８に示すように、シリコン層２０にサリサイド技術によってシリサイド層３６を形成する。シリサイド層３６は、遷移金属、たとえばコバルト、ニッケル、チタンなどを

スパッタ法によって成膜した後、アニールによってシリコン層２０でシリサイドを自己整合的に形成する。このサリサイド工程においては、アニール温度は、不純物の熱拡散を抑制し、ゲート電極に悪影響を与えない程度の温度で行われることが望ましい。金属としてニッケルを用いることにより、５００℃程度の低温でシリサイド化を行うことができる。この場合、ゲート電極としてタンタルなどの金属を用いてもこれにダメージを与えることがなく、また、不純物層の熱による拡散を抑制できる。

【００３２】

この後は、通常のプロセス技術により層間絶縁層および配線層を形成し、半導体装置を完成することができる。

【００３３】

本実施の形態にかかる製造方法では、主に以下の作用効果を有する。

【００３４】

本実施の形態では、工程（ｂ）でエピタキシャル成長によってシリコン層２０を形成した後に、工程（ｅ）でゲート電極２６を形成し、工程（ｆ），（ｇ）でエクステンション領域３０およびソース／ドレイン領域３４を形成する。したがって、エクステンション領域３０およびソース／ドレイン領域３４は、工程（ｂ）で行われる高温のアニール処理の影響を受けずに形成できる。そのため、不純物の拡散を抑制でき、設計通りの不純物プロファイルを有する浅い不純物層を形成できる。このような浅い不純物層の形成は、デバイスの微細化にとって非常に重要である。

【００３５】

また、ゲート電極２６も、工程（ｂ）で行われる高温のアニール処理の影響を受けずに形成できるので、ゲート電極の材料としてポリシリコンのみならずタンタルなどの金属を採用できる。ゲート電極として金属を用いた場合には、一般的に、ゲート電極が例えば７００℃以上の高温に晒されると、ゲート電極とゲート絶縁層との間で化学反応（界面反応）を生じ、所望のゲート構造を形成できない。

【００３６】

このように、本実施の形態では、工程（ｂ）より後の工程のアニール処理、例えば工程（ｇ）、（ｈ）におけるアニールを４５０～６００℃で行うことにより、浅い不純物層を形成でき、また、ゲート電極に金属を用いることができる。

【００３７】

本実施の形態では、工程（ｃ）でシリコン層２０の表面に熱酸化法によって酸化シリコン層からなる保護層２２を選択的に形成することができる。この保護層２２はゲート電極のエッチング時にストッパとして機能する充分な膜厚を確保できるため、ゲート電極の材料として酸化シリコンに対する選択比が小さい金属などの材料を採用できる。

【００３８】

［第２の実施の形態］

図９～図１７は、第２の実施の形態に係る製造方法を示す断面図である。これらの図において図１～図８（第１の実施の形態）に示す部分と実質的に同じ部分には同一符号を付してその詳細な説明を一部省略する。第２の実施の形態は、ダミーゲート層およびスペーサ層の形成方法の点で、第１の実施の形態と異なる。

【００３９】

（ａ）図９に示すように、シリコンなどの半導体基板１０に、素子分離絶縁層１２を形成する。ついで、ＣＶＤ法によって半導体基板１０の表面に酸化シリコン層１８を形成する。その後、酸化シリコン層１８を公知のリソグラフィおよびエッチングによってパターニングすることにより溝部１８ａを形成する。溝部１８ａの幅はゲート長に相当する。ついで、溝部１８ａにおいて、熱酸化法によって半導体基板１０上に酸化シリコン層からなる保護層１４を形成する。保護層１４は、後のダミーゲート層のエッチング工程（ｄ）において半導体基板１０を保護する機能を有する。保護層１４の膜厚などは第１の実施の形態と同様である。

【００４０】

ついで、半導体基板１０の上方に溝部１３ａを埋めるように第１ダミーゲート層１６ａを形成する。第１ダミーゲート層１６ａは、ＣＶＤ法などを用いて窒化シリコン層を基板上に堆積した後、フォトリソグラフィおよび反応性イオンエッチングなどの異方性エッチングを行うことにより形成することができる。この第１ダミーゲート層１６ａは、下部が溝部１３ａ内にあり、溝部１３ａより上の上部は溝部１３ａより大きい幅を有し、かつ上部の両側面は溝部１３ａより所定距離外側に位置するように形成される。

【００４１】

ついで、図１０に示すように、第１ダミーゲート層１６ａの両側面に接してサイドウォール状の第２ダミーゲート層１６ｂを形成する。第２ダミーゲート層１６ｂは、ＣＶＤ法などを用いて窒化シリコン層を基板上に堆積した後、反応性イオンエッチングなどの異方性エッチングを行うことにより形成することができる。このようにして、第１ダミーゲート層１６ａとサイドウォール状の第２ダミーゲート層１６ｂとからなるダミーゲート層１６を形成できる。ダミーゲート層１６は、次のエッチング工程において酸化シリコン層１３に対して充分に異なる選択比をとれるように、酸化シリコン層１３と異なる材料によって形成される。本実施の形態では、第１の実施の形態と同様に、ダミーゲート層１６は窒化シリコン層から構成され、スペーサ層となる層は酸化シリコン層から構成されている。

【００４２】

（ｂ）図１１に示すように、ダミーゲート層１６をマスクとして酸化シリコン層１３をエッチングすることにより、スペーサ層１８を形成できる。

【００４３】

ついで、半導体基板１０上の露出面に、エピタキシャル成長によってシリコン層２０を選択的に形成する。シリコン層２０は、半導体基板１０上においてシリサイド化されるのに必要な膜厚と、つぎの酸化シリコン層（ストッパ層）の形成工程（ｃ）で熱酸化に必要な膜厚とを考慮して決めることができる。シリコン層２０の膜厚は、このような点を考慮すると、５０～１００ｎｍとすることができる。シリコン層２０は、第１の実施の形態と同様にして形成できる。

【００４４】

以下の工程（ｃ）～（ｋ）は、第１の実施の形態と同様であるので主要な点のみ記載する。

【００４５】

（ｃ）図１２に示すように、熱酸化法によって、シリコン層２０の表面に酸化シリコン層からなるストッパ層２２を選択的に形成する。ストッパ層２２は、後の工程（ｅ）のエッチングにおいてシリコン層２０を保護する機能を有する。

【００４６】

（ｄ）図１３に示すように、窒化シリコン層からなるダミーゲート層１６を熱リン酸によってエッチングして除去する。この工程では、半導体基板１０は酸化シリコン層からなる保護層１４で覆われ、また、シリコン層２０は酸化シリコン層からなるストッパ層２２とスペーサ層１８とによって覆われているため、いずれも熱リン酸によるエッチングでダメージを受けることがない。

【００４７】

ついで、保護層１４を希フッ酸によるライトエッチングで除去し、半導体基板１０を露出させる。

【００４８】

（ｅ）図１４に示すように、ゲート絶縁層２４、ゲート電極２６およびキャップ層２８を形成する。ゲート絶縁層２４、ゲート電極２６およびキャップ層２８などは、第１の実施の形態と同様の形成方法および材料を採用できる。また、この工程では、シリコン層２０はストッパ層２２とスペーサ層１８とによって覆われているため、ゲート電極２６のエッチング時にダメージを受けることがない。

【００４９】

（ｆ）図１５に示すように、第１の実施の形態と同様に、酸化シリコンからなるスペーサ

層１８を例えば希フッ酸によってエッチングする。ついで、斜めイオン注入によって半導体基板１０の露出部（スペーサ層１８が除去された領域）に不純物を導入して、エクステンション領域３０を形成する。

【００５０】

（ｇ）図１６に示すように、ゲート絶縁層２４、ゲート電極２６およびキャップ層２８の両側面にサイドウォール絶縁層３２を形成する。サイドウォール絶縁層３２は、第１の実施の形態と同様の形成方法および材料などを採用できる。

【００５１】

ついで、イオン注入（図示の例では斜めイオン注入）によって、シリコン層２０および半導体基板１０に不純物を導入し、半導体基板１０にソース／ドレイン領域３４を形成する。そして、アニールを行うことによりソース／ドレイン領域の不純物を活性化させる。このときのアニール温度は、第１の実施の形態と同様に、不純物の熱拡散を抑制し、ゲート電極に悪影響を与えない程度の温度で行われることが望ましい。特に、ゲート電極２６としてタンタルなどの金属を用いた場合には、低温アニール（５５０℃程度）を行うことが望ましい。

【００５２】

（ｈ）図１７に示すように、シリコン層２０にサリサイド技術によってシリサイド層３６を形成する。シリサイド層３６は、第１の実施の形態と同様の形成方法を採用できる。また、サリサイド工程においては、アニール温度は、不純物の熱拡散を抑制し、ゲート電極に悪影響を与えない程度の温度で行われることが望ましい。金属としてニッケルを用いることにより、５００℃程度の低温でシリサイド化を行うことができる。この場合、ゲート電極としてタンタルなどの金属を用いた場合でもこれにダメージを与えることがなく、また、不純物層の熱による拡散を抑制できる。

【００５３】

この後は、通常のプロセス技術により層間絶縁層および配線層を形成し、半導体装置を完成することができる。

【００５４】

第２の実施の形態では、ダミーゲート層１６を第１ダミーゲート層１６ａと第２ダミーゲート層１６ｂとで構成している。このようにダミーゲート層１６を２段階で形成することにより、第１ダミーゲート層１６ａとゲート電極２６、キャップ層２８とを同じマスクを用いてパターニングできる。もちろん、ダミーゲート層１６は、１回のパターニングで形成してもよい。

【００５５】

第２の実施の形態でも第１の実施の形態と同様な作用効果を得ることができる。すなわち、本実施の形態では、工程（ｂ）でエピタキシャル成長によってシリコン層２０を形成した後に、工程（ｅ）でゲート電極２６を形成し、工程（ｆ）、（ｇ）でエクステンション領域３０およびソース／ドレイン領域３４を形成する。したがって、エクステンション領域３０およびソース／ドレイン領域３４は、工程（ｂ）で行われる高温のアニール処理の影響を受けずに形成できる。そのため、不純物の拡散を抑制でき、設計通りの不純物プロファイルを有する浅い不純物層を形成できる。

【００５６】

また、ゲート電極２６も、工程（ｂ）で行われる高温のアニール処理の影響を受けずに形成できるので、ゲート電極の材料としてポリシリコンのみならずタンタルなどの金属を採用できる。

【００５７】

このように、本実施の形態では、工程（ｂ）より後の工程のアニール処理、例えば工程（ｇ）、（ｈ）におけるアニールを４５０～６００℃で行うことにより、浅い不純物層を形成でき、また、ゲート電極に金属を用いることができる。

【００５８】

本実施の形態では、工程（ｃ）でシリコン層２０の表面に熱酸化法によって酸化シリコン

層からなる保護層２２を選択的に形成することができる。この保護層２２はゲート電極のエッチング時にストッパとして機能する充分な膜厚を確保できるため、ゲート電極の材料として酸化シリコンに対する選択比が小さい金属などの材料を採用できる。

【００５９】

本発明は以上の実施の形態に限定されず、本発明の要旨の範囲内で各種の態様をとることができる。

【図面の簡単な説明】

【図１】第１の実施の形態にかかる製造方法の一工程を模式的に示す断面図である。

【図２】第１の実施の形態にかかる製造方法の一工程を模式的に示す断面図である。

【図３】第１の実施の形態にかかる製造方法の一工程を模式的に示す断面図である。

【図４】第１の実施の形態にかかる製造方法の一工程を模式的に示す断面図である。

【図５】第１の実施の形態にかかる製造方法の一工程を模式的に示す断面図である。

【図６】第１の実施の形態にかかる製造方法の一工程を模式的に示す断面図である。

【図７】第１の実施の形態にかかる製造方法の一工程を模式的に示す断面図である。

【図８】第１の実施の形態にかかる製造方法の一工程を模式的に示す断面図である。

【図９】第２の実施の形態にかかる製造方法の一工程を模式的に示す断面図である。

【図１０】第２の実施の形態にかかる製造方法の一工程を模式的に示す断面図である。

【図１１】第２の実施の形態にかかる製造方法の一工程を模式的に示す断面図である。

【図１２】第２の実施の形態にかかる製造方法の一工程を模式的に示す断面図である。

【図１３】第２の実施の形態にかかる製造方法の一工程を模式的に示す断面図である。

【図１４】第２の実施の形態にかかる製造方法の一工程を模式的に示す断面図である。

【図１５】第２の実施の形態にかかる製造方法の一工程を模式的に示す断面図である。

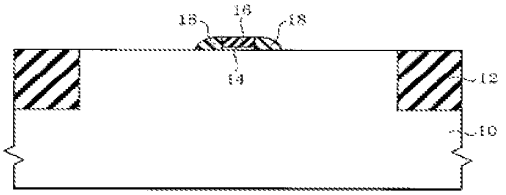
【図１６】第２の実施の形態にかかる製造方法の一工程を模式的に示す断面図である。

【図１７】第２の実施の形態にかかる製造方法の一工程を模式的に示す断面図である。

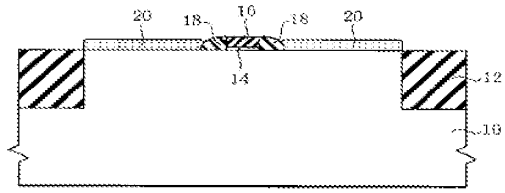
【符号の説明】

１０　半導体基板、１２　素子分離絶縁層、１４　保護層、１６　ダミーゲート層、１６ａ　第１ダミーゲート層、１６ｂ　第２ダミーゲート層、１８　スペーサ層、２０　シリコン層、２２　ストッパ層、２４　ゲート絶縁層、２６　ゲート電極、２８　キャップ層、３０　エクステンション領域、３２　サイドウォール絶縁層、３４　ソース／ドレイン領域、３６　シリサイド層

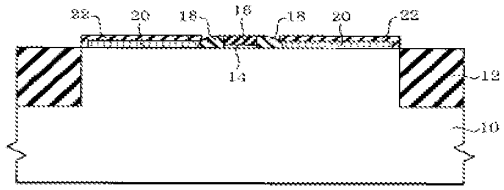
【図１】



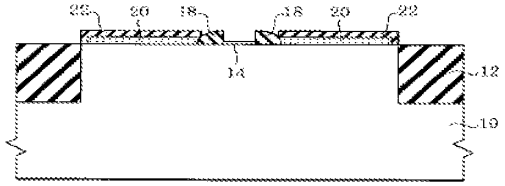
【図２】



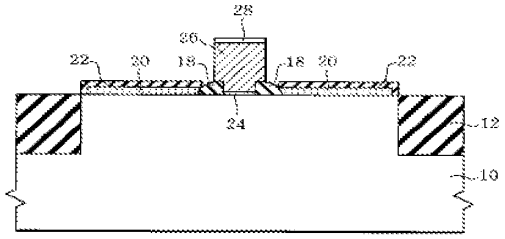
【図３】



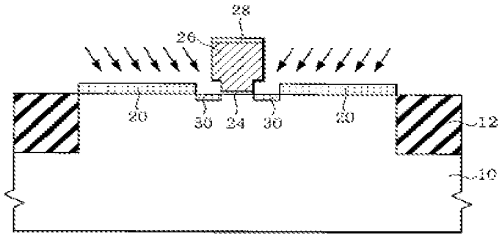
【図４】



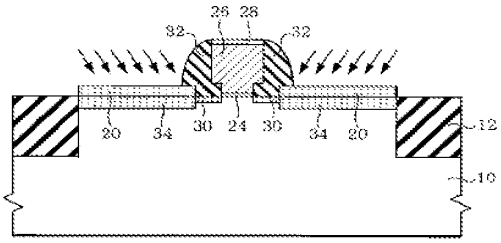
【図５】



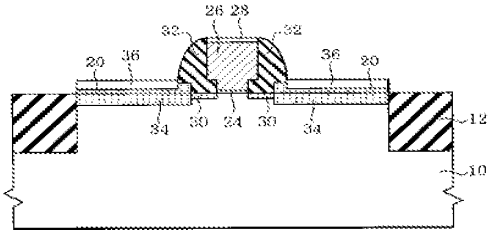
【図６】



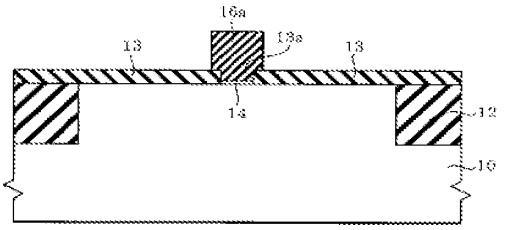
【図７】



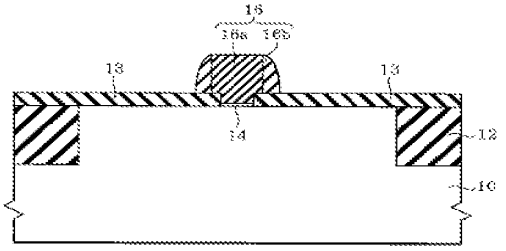
【図８】



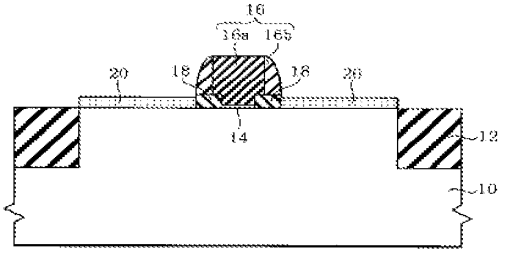
【図９】



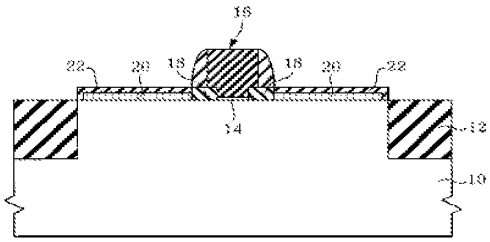
【図１０】



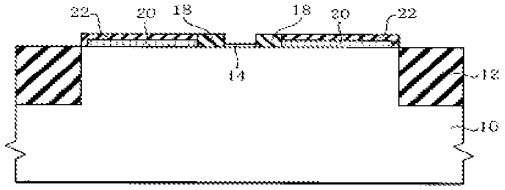
【図１１】



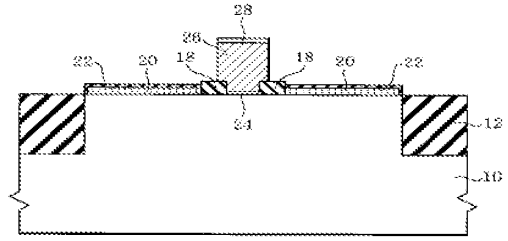
【図１２】



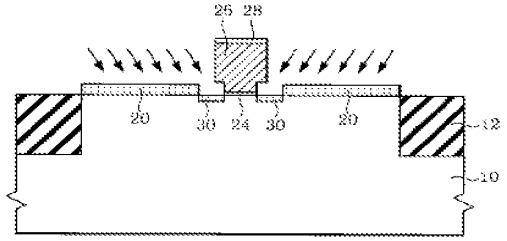
【図１３】



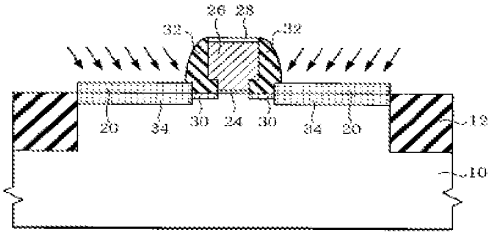
【図１４】



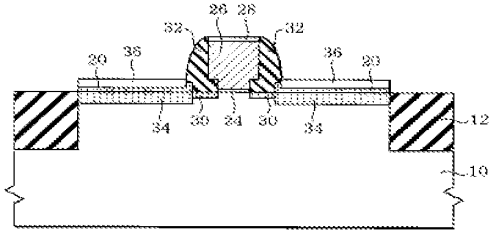
【図１５】



【図１６】



【図１７】



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本実施の形態では、工程（ｃ）でシリコン層２０の表面に熱酸化法によって酸化シリコン層からなるストッパ層２２を選択的に形成することができる。このストッパ層２２はゲート電極のエッチング時にストッパとして機能する充分な膜厚を確保できるため、ゲート電極の材料として酸化シリコンに対する選択比が小さい金属などの材料を採用できる。
【手続補正2】
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【補正の内容】
【００５８】
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(71) Applicant *(for all designated States except US)*: **INTEL CORPORATION** [US/US]; 2200 Mission College Boulevard, Santa Clara, California 95052 (US).

(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: **CAPPELLANI, Annalisa** [IT/US]; 4470 NW Kahneeta Drive, Portland, Oregon 97229 (US). **GHANI, Tahir** [US/US]; 15523 NW Andalusian Way, Portland, Oregon 97229 (US). **SHEN, Kuan-Yueh** [—/US]; 242 NE 62nd Place, Hillsboro, Oregon 97124 (US). **MURTHY, Anand S.** [US/US]; 10934 NW Lucerne Ct., Portland, Oregon 97229 (US). **GOMEZ, Harry** [US/US]; 7227 NE Rockridge P1, Hillsboro, Oregon 97124 (US).

(74) Agents: **VINCENT, Lester J.** et al.; Blakely Sokoloff Taylor & Zafman, 1279 Oakmead Parkway, Sunnyvale, California 94085 (US).

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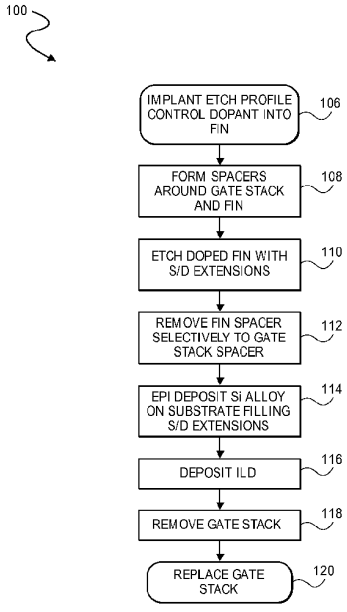


FIG. 1

(57) Abstract: A channel strained multi-gate transistor with low parasitic resistance and method of manufacturing the same. A gate stack may be formed over a semiconductor fin having a gate-coupled sidewall height (H_{si}), an etch rate controlling dopant may be implanted into a source/drain region of the semiconductor fin adjacent to the gate stack and into a source/drain extension region of the semiconductor fin. The doped fin region may be etched to remove a thickness of the semiconductor fin equal to at least H_{si} proximate a channel region and form a source/drain extension undercut. A material may be grown on the exposed semiconductor substrate to form a regrown source/drain fin region filling the source/drain extension undercut region.

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MULTI-GATE SEMICONDUCTOR DEVICE WITH SELF-ALIGNED EPITAXIAL SOURCE AND DRAIN

BACKGROUND

[0001] For increased performance, it is often desired to reduce transit time of electrons in N-type metal oxide semiconductor (NMOS) device channel regions and of positive charged holes in P-type MOS device (PMOS) channel regions used in a complementary metal oxide semiconductor (CMOS) devices on a substrate (e.g., integrated circuit (IC) transistor, etc. on a semiconductor substrate). Reduction in channel lengths is a favored way of reducing transit times however because such reductions induce short channel effects, multi-gate devices have been developed in which the channel regions are a portion of a non-planar semiconductor body, or "fin" covered by a gate stack. For such multi-gate devices, the transistor can be gated by the gate stack through a sidewall, as well as a top surface of the fin for better gate control.

[0002] With the improved gate control possible with multi-gate designs, the dimension of the fin may be scaled to such a point that the contact to the fin results in a parasitic resistance, $R_{external}$, which can severely limit the operational performance of the multi-gate device. One method of reducing the overall resistance is to dope the fin source/drain regions. For instance, a dopant may be implanted in the source/drain regions and an anneal may be carried out to activate and diffuse the dopant towards the channel region.

[0003] Where an implant and diffusion method is used, the ability to control the dopant concentration and location within the fin is limited. Furthermore, the size of other parts of a MOS device, such as the presence of a spacer around the fin, can also greatly hinder reductions in $R_{external}$.

[0004] Furthermore, because fin structures are free of a surrounding substrate, strain-inducing mobility enhancement techniques which have proved advantageous in the past for planar devices may not be readily adaptable to multi-gate devices. Without the ability to enhance channel mobility via strain (e.g., uniaxial or biaxial), the performance improvement in multi-gate devices resulting from the smaller channel lengths possible would be at least partially offset by a comparatively lower channel mobility. Accordingly, improved methods and structures are needed to overcome these limitations in the source/drain fin regions.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] Embodiments of the invention, both as to organization and method of operation, together with objects, features, and advantages thereof, may best be understood by reference to the following detailed description when read with the accompanying drawings in which:

[0006] Figure 1 is a flow diagram depicting a method of forming source and drain epitaxial extensions in a multi-gate device, in accordance with an embodiment of the invention;

[0007] Figure 2A is an isometric view of a stage in the fabrication of a multi-gate device corresponding to operation 106 in Figure 1, in accordance with an embodiment of the invention;

[0008] Figure 2B is a cross-sectional view of the device depicted in Figure 2A;

[0009] Figure 3A is an isometric view of a stage in the fabrication of a multi-gate device corresponding to operation 108 in Figure 1, in accordance with an embodiment of the invention;

[0010] Figure 3B is a cross-sectional view of the device depicted in Figure 3A;

[0011] Figure 4A is an isometric view of a stage in the fabrication of a multi-gate device corresponding to operation 110 in Figure 1, in accordance with an embodiment of the invention;

[0012] Figure 4B is a view of the cross-section along the B-B' plane of the device depicted in Figure 4A, in accordance with an embodiment of the invention;

[0013] Figure 4C is a view of the cross-section along the B-B' plane of the device depicted in Figure 4A, in accordance with an embodiment of the invention;

[0014] Figure 5A is a first cross-sectional view of a stage in the fabrication of a multi-gate device corresponding to operation 112 in Figure 1, in accordance with an embodiment of the invention;

[0015] Figure 5B is a second cross-sectional view, orthogonal to the view in Figure 5A, of a stage in the fabrication of a multi-gate device corresponding to operation 112 in Figure 1, in accordance with an embodiment of the invention;

[0016] Figure 6A is a first cross-sectional view of a stage in the fabrication of a multi-gate device corresponding to operation 114 in Figure 1, in accordance with an embodiment of the invention;

[0017] Figure 6B is a second cross-sectional view, orthogonal to the view in Figure 6A, of a stage in the fabrication of a multi-gate device corresponding to operation 114 in Figure 1, in accordance with an embodiment of the invention;

[0018] Figure 7 is a cross-sectional view of a stage in the fabrication of a multi-gate device corresponding to operation 116 in Figure 1, in accordance with an embodiment of the invention;

[0019] Figure 8 is a cross-sectional view of a stage in the fabrication of a multi-gate device corresponding to operation 118 in Figure 1, in accordance with an embodiment of the invention; and

[0020] Figure 9 is a cross-sectional view of a stage in the fabrication of a multi-gate device corresponding to operation 120 in Figure 1, in accordance with an embodiment of the invention.

[0021] It will be appreciated that for simplicity and clarity of illustration, elements illustrated in the figures have not necessarily been drawn to scale. For example, the dimensions of some of the elements may be exaggerated relative to other elements for clarity. Further, where considered appropriate, reference numerals have been repeated among the figures to indicate corresponding or analogous elements.

DETAILED DESCRIPTION

[0022] Described herein are systems and methods of forming epitaxial source and drain extensions in a multi-gate MOS device (e.g., "finfet"). In the following description, various aspects of the illustrative implementations will be described using terms commonly employed by those skilled in the art to convey the substance of their work to others skilled in the art. However, it will be apparent to those skilled in the art that the present invention may be practiced with only some of the described aspects. For purposes of explanation, specific numbers, materials and configurations are set forth in order to provide a thorough understanding of the illustrative embodiments. However, it will be apparent to one skilled in the art that the present invention may be practiced without the specific details. In other instances, well-known features are omitted or simplified in order not to obscure the illustrative embodiments.

[0023] Various operations will be described as multiple discrete operations, in turn, in a manner that is most helpful in understanding the illustrative embodiments of the present invention; however, the order of description should not be construed to imply that these

operations are necessarily order dependent. In particular, these operations need not be performed in the order of presentation.

[0024] Disclosed herein is a multi-gate device including epitaxial source and drain fin regions having a vertical thickness equal to approximately Hsi proximate the channel and which may further include a portion of the epitaxial source and drain fin regions regrown to be disposed under the gate dielectric layer of the transistor. Figure 1 is a flow diagram depicting a method 100 of forming such regrown source/drain regions, in accordance with an embodiment of the invention including source and drain epitaxial extensions. Figures 2-9 depict a multi-gate device after particular operations of the method 100 as it is performed.

[0025] Method 100 begins with an ion implantation operation 106 carried out to form doped regions of a semiconductor fin adjacent to a gate stack disposed on the semiconductor fin. The doped regions are to be removed in preparation for regrowing source and drain regions for the multi-gate MOS transistor being formed. When exposed to an appropriate etchant, the doped regions will have an etch rate that is higher than the etch rate of the surrounding substrate and channel semiconductor material which enables excellent control of the etch profile allowing shaping of the regrown source and drain regions for optimal sub-fin leakage characteristics and channel strain.

[0026] Figure 2A is an isometric view of a gate stack formed over a semiconductor fin as provided at operation 106 in Figure 1, in accordance with an illustrative embodiment of the invention. Figure 2B represents a cross-sectional view of the multi-gate transistor of Figure 2 taken along the A-A' reference line illustrated in Figure 2A. As shown in Figures 2A and 2B, a non-planar semiconductor body over a substrate 202 forms a fin with a parallelepiped shape having a sidewall 207 with a sidewall height, H_{si}, and a top surface 211 extending beyond an adjacent isolation region 210. The top surface 211 and sidewall 207 are apportioned into a non-planar source region 215 and non-planar drain region 216 with a channel region there between covered by a gate stack 217. For the multi-gate transistor, the channel is to be capacitively controllable at least through sidewall 207 such that the H_{si} represents the gate-coupled channel sidewall height. The top surface 211 may also be capacitively controllable by an overlying gate stack for greater sub-threshold control. In the exemplary embodiment, the gate stack 217 is sacrificial and subsequently removed for a replacement metal gate process. However, the methods described herein

may also be adapted to embodiments in which the gate stack 217 is not sacrificial but rather retained in the final multi-gate device.

[0027] In the exemplary embodiment, the substrate 202 is a bulk silicon or a silicon-on-insulator substructure. The semiconductor substrate 202 may, however, also be formed using alternate materials, which may or may not be combined with silicon, that include, but are not limited, to germanium, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, or gallium antimonide. Although a few examples of materials from which the substrate may be formed are described, any material known in the art that upon which a semiconductor device may be built falls within the spirit and scope of the present invention.

[0028] As shown, the gate stack 217 includes a gate dielectric 212, a gate electrode 213, and a gate cap 214. The gate dielectric 212 may be a silicon dioxide, silicon nitride, silicon oxynitride, or a dielectric material having a dielectric constant greater than 10 (i.e., "high-k"). Examples of high-k gate dielectric materials that may be used include, but are not limited to, hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate. The gate electrode 213 may be poly-silicon, poly-germanium, a metal, or a combination thereof. The gate cap 214 may be any conventional hard mask dielectric material such as, silicon oxide, silicon nitride, and the like.

[0029] Figure 2B illustrates how a first non-planar body 250 and a second non-planar body 225 may be formed on opposite side of the doped fin region 208. The second non-planar body 225 may either be the basis for another functional transistor or merely a dummy structure providing a means to control one or more aspects of the fabrication of the first non-planar body 250. As such, Figure 2B illustrates two different exemplary interfaces of the doped fin region 208: an interface with the isolation region 210 and an interface with a second non-planar semiconductor body. It should be appreciated that the doped fin region 208 may have an end distal from the first non-planar body 250 that abuts either one of these two interfaces.

[0030] The dopant used in the ion implantation operation 106 is chosen based on its ability to increase the etch rate of the semiconductor fin material in which it is implanted. The specific dopant may therefore vary based on the substrate material and the etchant

used in a subsequent etching of the doped fin. Exemplary dopants increase the etch rate of silicon, germanium, or indium antimonide. In particular embodiments, specific dopants include, but are not limited to, carbon, phosphorous, and arsenic. For instance, carbon may be used at a dosage that ranges from 1×10^{14} to 1×10^{16} atoms/cm^3. Phosphorous may be used at a dosage that ranges from 1×10^{14} to 5×10^{15} atoms/cm^3. Arsenic may be used at a dosage that ranges from 1×10^{14} to 5×10^{15} atoms/cm^3. The ion implantation may be performed in a substantially vertical direction (i.e., a direction perpendicular to substrate). However, in some embodiments, at least a portion of the ion implantation process may occur in an angled direction to implant ions below the gate stack 217. For non-replacement gate embodiments, the gate cap 214 may be formed of a sufficient thickness to prevent doping of the gate electrode 213. With the etch profile control dopants present in the semiconductor fin, an anneal may be carried out to complete operation 106. The anneal drives the dopants further into the semiconductor fin and reduces any damage sustained by the substrate during the ion implantation. The exemplary anneal is between 700°C and 1100°C for a duration of up to one minute, for instance, a duration of five seconds.

[0031] The size of the doped fin region 208, including the depth, may vary based on the requirements of the multi-gate MOS transistor being formed. As shown in Figures 2A and 2B, following the implant operation 106, the doped fin region 208 proximate to the channel region 205 extends to a depth of the semiconductor fin no greater than the height H_{si}. In the exemplary embodiment illustrated in Figure 2B, the doped fin region 208 forms a substantially perpendicular sidewall interface 209A with the channel region 205. The substantially perpendicular sidewall interface 209A extends through approximately the entire thickness of the semiconductor fin of height H_{si}. In one embodiment, the doped fin region 208 further forms a bottom interface 209B with the subjacent semiconductor substrate 202 that is substantially planar with a top surface of the isolation region 210. In another embodiment, the doped fin region 208 forms a bottom interface 209C with the subjacent semiconductor substrate 202 that is an amount D_R below a top surface of the isolation region 210. In either case, there may be a transitional interface 245 which slopes laterally away from the gate stack 217 with the transitional interface 245 preferably beginning a distance which is not more than H_{si} below the gate dielectric 212. As further shown in Figures 2A and 2B, portions of the doped fin region 208 are sited below, or subjacent to, the gate stack 217 by an amount, X_{IM}. In the exemplary embodiment, the

amount by which the doped fin region 208 overlap the gate stack 217 is substantially constant for the height H_{si} (along the interface 209A) with the amount of overlap decreasing at depths greater than H_{si} (forming the transitional interface 245).

[0032] Returning to Figure 1, at operation 108, spacers are formed on either side of the gate stack and the semiconductor fin. The spacers may be formed using conventional dielectric materials, including but not limited to silicon oxide or silicon nitride. The width of the spacers may be chosen based on design requirements for the multi-gate transistor being formed. Figures 3A and 3B illustrate a gate stack spacer 319 formed on sidewalls of the gate stack 217. Formation of the gate stack spacer 319 also forms a fin spacer 318 on the sidewalls of the semiconductor fin, in particular adjacent to the doped fin region 208, and disposed on the isolation region 210.

[0033] Returning to Figure 1, an etch process is performed at operation 110 to etch the doped fin region. In particular embodiments, this etch process may also form a cavity below the gate stack in which regrown source/drain regions may be subsequently formed. The etch operation 110 uses etchants that complements the dopant used in the ion implantation process to increase the etch rate of the doped regions. This enables the etching process to remove the doped fin region at a faster rate than the remainder of the undoped (or more lightly doped) substrate. As such, with an appropriate increase in etch rate, the etching process can selectively remove substantially the entire semiconductor fin (i.e., entire height H_{si} over the entire channel width W_{si}, as shown in Figure 3A) and retain only the channel region with good profile and depth control. This includes portions of the doped regions that undercut the gate stack spacer and the gate dielectric, thereby defining a self-aligned source/drain fin extensions of the multi-gate transistor.

[0034] In accordance with an exemplary embodiment of the invention, the etch operation 110 includes is a dry etch using a chlorinated chemistry in combination with at least one of NF_3, HBr, SF_6 and Ar or He used as a carrier gas. The flow rate for the active etchant species may vary between 50 and 200 standard cubic centimeters per minute (SCCM) while the flow rate of the carrier gas may vary between 150 and 400 SCCM. A high energy plasma may be employed at a power that ranges from 700W to 1100W with zero or an RF bias of less than 100W. The reactor pressure may range from around 1 pascal (Pa) to around 2 Pa. In further embodiments, the etch operation 110 further includes a wet etch to clean and further etch the semiconductor substrate 202 where the doped fin region 208 where removed. Conventional wet etch chemistries known in the art for cleaning silicon

and oxide material may be used. For instance, wet etch chemistries capable of removing silicon along its crystallographic planes may be used.

[0035] Figures 4A, 4B and 4C depict the multi-gate device after the etch operation 110 is performed. In the exemplary embodiment, the source/drain extension cavity 421 is etched with an undercut amount of X_{UC} that is controlled on the basis of the implant profile X_{IM} to be substantially constant over an etched depth that is approximately equal to H_{si}. In particular embodiments, X_{UC} can range from greater than 0 to 12 nm for a gate length range of 15 to 40nm while the gate stack length (dimension parallel to X_{UC}) over an entire gate coupled channel height H_{si} is, as an example, approximately 25nm. In an alternative embodiment where traditional tip implants are to be employed and the regrown source/drain is not to interface with the channel directly, X_{UC} is 0. Etching the source/drain fin regions and forming a source/drain extension undercut amount X_{UC} which is approximately constant over H_{si} enables a greater amount of stress to be applied to the channel region 205 than if the source/drain extension cavity 421 had a depth less than H_{si} or if the undercut amount X_{UC} was reduced (e.g., 0 for the tip implant embodiments). Application of greater stress has the effect of increasing $I_{d,sat}$ for the multi-gate transistor. Etching the source/drain fin regions down to H_{si} also maximizes the area of the channel region 205 available to be contacted by a subsequently regrown source/drain region for reduced $R_{external}$.

[0036] However, it has also been found that sub-fin leakage (source-to-drain leakage below channel region 205) is a function of the fin etch depth proximate to the channel region 205 with such leakage increasing significantly where the undercut amount X_{UC} is not reduced for depths greater than H_{si} (as measured from the interface of the gate dielectric 212). Thus, the depth and profile of the fin etch should be optimized between stress and channel leakage. As such, in one embodiment providing a substantially flat-bottomed etch profile, the thickness of the doped fin region 208 removed during the etch operation 110 should not be greater than H_{si} so that both the source/drain cavity 420 and the source/drain extension cavity 421 are substantially planar to, or flush with, an adjacent isolation region 210 disposed under the gate stack 217 (Figure 2A). In certain embodiments, the surface of the isolation region 210 not covered by the gate stack 217 is recessed as a result of the fabrication processes.

[0037] For embodiments where the implant and/or etch is engineered to provide for a tapered or sloped profile away from the channel region 205, the thickness of the doped fin

region 208 removed during the etch operation 110 may be greater than H_{si} at a point distal from the channel region 205. For such an embodiment, the source/drain cavity 420 is recessed (dashed line 422) an amount below the gate stack protected areas of the isolation region 210 while a portion of source/drain extension cavity 421 proximate to the channel region 205 is substantially planar to, or flush with, areas of the isolation region 210 disposed under the gate stack (corresponding to a source/drain recess depth approximately equal to H_{si}). For this embodiment, the undercut amount X_{UC} of the source/drain extension cavity 421 decreases as a function of etch depth greater than the threshold etch depth of H_{si} (as illustrated with the slope in 422).

[0038] At operation 112, the fin spacer 318 is removed. Depending on the embodiment, the spacer removal operation 112 is either performed prior to the doped fin etch operation 110, during the doped fin etch operation 110, or after the doped fin etch operation 110. In the embodiment shown in Figures 4A, 4B and 4C, the source/drain etch operation 110 is selective to dielectric materials (e.g., to maintain dielectric encapsulation of the gate electrode 213) and both the gate stack spacer 319 and the fin spacer 318 are retained after the etch operation 110. In such an embodiment, the fin spacer 318 remains as a dielectric veil surrounding the source/drain cavity 420. For an embodiment where the source/drain etch operation 110 is less selective to dielectric materials, the fin spacer 318 may be partially or completely removed during the doped fin etch operation 110 (in which case operations 110 and 112 of Figure 1 are performed simultaneously).

[0039] For embodiments where at least some portion of the fin spacer 318 remain after operation 110, the fin spacer 318 is removed preferentially to the semiconductor substrate 202 in a manner which retains the gate stack spacer 319 and the gate cap 214, as further depicted in Figures 5A and 5B. In one embodiment, an isotropic etch process (dry or wet) is utilized to etch the fin spacer 318. For such embodiments, the fin spacer 318 may be etched away from the surface of the isolation region 210 while the gate stack spacer 319 and the gate cap 214 are only partially thinned. With the gate electrode 213 remaining encapsulated following removal of the fin spacer 318 the gate electrode does not provide a seed surface during a subsequent source/drain regrowth.

[0040] Returning to Figure 1, at operation 114 the source/drain cavity 420, including the source/drain extension cavity 421, is filled with a material using a selective epitaxial deposition process to form regrown source/drain fin. In an embodiment, as depicted in Figures 6A and 6B, the material forming the source/drain fin 618 induces a strain on the

channel region 205. In accordance with particular embodiments, the material forming the regrown source/drain fin 618 contains silicon and follows the crystallinity of the substrate 202 but has a lattice spacing that is different than the lattice spacing of the substrate 202. The difference in lattice spacing induces a tensile or compressive stress in the channel region of the MOS transistor that is accentuated by depositing the silicon alloy in the source and drain extension cavity 421. As is known to those of skill in the art, deciding whether to induce a tensile stress or a compressive stress will depend on whether an NMOS or a PMOS transistor is being formed.

[0041] The epitaxial deposition operation 114 therefore regrows source/drain regions and source/drain extensions in one process. For embodiments in which the regrown source/drain regions fill an undercut having an X_{UC} that is greater than 0, the epitaxially regrown source/drain fin 618 may have a more abrupt interface 609A than embodiments which employ tip implants to place dopant at interface to the channel (e.g., X_{UC} is 0). In other words, the interface 609A between the epitaxial regrown source/drain fin 618 and the channel region 205 is well-defined by the regrowth process. On one side of the interface 609A is the epitaxially deposited doped silicon material and on the other side of the interface 609A is the substrate material that makes up the channel region 205. The dopants in the regrown source/drain fin 618 may diffuse into the channel region 205 but such diffusion is engineered by controlling the location of the X_{UC} dimension (i.e., location of the interface 209A with the channel region 205) and by optimizing the temperature of the EPI deposition and subsequent thermal treatments. This enables the regrown source/drain regions to bring the heavily doped source/drain material in very close proximity to the channel region 205 relative to conventional techniques (i.e., the undercut amount X_{UC} may overlap the gate stack extensively). As will be appreciated by those of skill in the art, this in turn enables the channel length to be scaled down without having to reduce the dimension of the gate stack.

[0042] In an embodiment, the source/drain regions are regrown to a thickness of at least H_{si}. In a further embodiment, the source/drain regions are regrown to a width of at least W_{si}, and preferably to a width greater than W_{si}, as depicted in Figure 6B. Forming the regrown source/drain fin 618 at the height H_{si} and in relatively close proximity to the channel region 205 imparts a large hydrostatic stress on the channel. As previously described, this stress increases the strain within the channel region 205, thereby increasing mobility in the channel and increasing drive current. In the exemplary embodiment with

the fin spacer 318 removed, the source/drain regions are regrown defect free or with significantly lower defects than possible with sidewall growth constraints. In the absence of fin spacer 318, the lateral epitaxial growth of the regrown source/drain fin 618 is unobstructed, thereby allowing the formation of {111} facets and continued growth on {111} planes to extend over a portion of isolation region 210, as further shown in Figure 6A. Of course, the epitaxial growth facets are dependent on the crystal orientation of the underlying substrate 202 such that different substrate orientations will result in different epitaxial facets. The width of the regrown source/drain fin 618 is therefore greater than the width of the doped fin region 208 which was removed. Thus, the channel region 205 has a width W_{si} that is smaller than the width of the regrown source/drain fin 618. For instance, the width of the regrown source/drain fin 618 may be between 10% and 100% wider than W_{si} to optimize performance. In one embodiment, the width of the regrown source/drain fin 618 is greater than W_{si} along at least half the height H_{si}. In other words, as the regrown source/drain fin 618 is formed, it reaches a width greater than W_{si} by the time the regrown source/drain thickness is approximately $1/2H_{si}$. The relatively wider regrown source/drain fin 618 provides for a larger surface area upon which a metallized contact may be made, thereby reducing $R_{external}$ relative to a source/drain region having a width equal to W_{si}. The greater width of the regrown source/drain fin 618 also increases the amount of strain placed on the channel region 205.

[0043] In certain embodiments, a silicon alloy is employed for the regrown source/drain fin 618. The alloy may impart strain on the channel region 205. Depending on the embodiment, the alloy may be in-situ Boron doped silicon germanium (e.g., for a PMOS multi-gate transistor with a compressively strained channel), in-situ Carbon and Phosphorus doped silicon (e.g., for a NMOS multi-gate transistor with a tensilely strained channel), or in-situ Phosphorus doped silicon. In alternate implementations, other silicon alloys may be used. For instance, alternate silicon alloy materials that may be used include, but are not limited to, nickel silicide, titanium silicide, cobalt silicide, and may be doped with one or more of boron and/or aluminum. In still other embodiments, non-silicon materials are employed (e.g., pure germanium, germanate, etc.).

[0044] For one NMOS transistor embodiment, the regrown source/drain fin 618 may be filled with carbon doped silicon. The carbon doped silicon may be epitaxially and selectively deposited. In further implementations, the carbon doped silicon may be further doped in situ with phosphorous. The carbon concentration may range from 0.5 atomic %

to 5.0 atomic %. The phosphorous concentration may range from $5\times10^{19}/c^{m3}$ to $3\times10^{21}/c^{m3}$. The thickness of the carbon doped silicon may range from 400Å to 1200Å. The carbon and phosphorous doped silicon may be denoted as $(C,P_{)y}S_{i(1-y)}$. The deposition of the doped $(C,P_{)y}S_{i(1-y)}$ source and drain regions may be carried out in chemical vapor deposition reactor using a co-flown or cyclically deposition and etch sequenced process. In one example, the film is formed by cyclical deposition and etch based on silane (Si_{H4}), diclholorosilane, disilane, PH_3, CH_3SiH_3, and chlorine (Cl_2) or HCl chemistry.

[0045] For one PMOS transistor embodiment, the regrown source/drain fin 618 may be filled with silicon germanium. The silicon germanium may be epitaxially deposited. The germanium concentration may range from 10 atomic % to 80 atomic %. In further implementations, the silicon germanium may be further doped in situ with boron. The boron concentration may range from $2\times10^{19}/cm^3$ to $2\times10^{21}/cm^3$. The thickness of the silicon germanium may range from 40Å to 1500Å. Deposition of the doped silicon germanium may be carried out in a CVD reactor, an LPCVD reactor, or an ultra high vacuum CVD (UHVCVD). The reactor temperature may fall between 600°C and 800°C and the reactor pressure may fall between 1 and 760 Torr. The carrier gas may consist of hydrogen or helium at a flow rate that ranges between 10 and 50 SLM.

[0046] As will be appreciated by those of skill in the art, the multi-gate MOS transistor may undergo further processing, such as replacement gate oxide processes, replacement metal gate processes, annealing, or salicidation processes, that may further modify the transistor and/or provide the necessary electrical interconnections. For instance, after the epitaxial deposition of the regrown source/drain fin 618, an interlayer dielectric (ILD) may be deposited and planarized over the multi-gate device at operation 116 (Figure 1), and as further shown in Figure 7. Because the fin spacer 318 was removed, the ILD 723 is deposited directly on sidewalls of the regrown source/drain fin 618, and as such, is in contact both with a sidewall of the gate stack spacer 319 and with a sidewall portion of the regrown source/drain fin 618 located within the height H_{si}. The ILD 723 may be formed using materials known for the applicability in dielectric layers for integrated circuit structures, such as low-k dielectric materials. Such dielectric materials include, but are not limited to, oxides such as silicon dioxide (SiO_2) and carbon doped oxide (CDO), silicon nitride, organic polymers such as perfluorocyclobutane or polytetrafluoroethylene, fluorosilicate glass (FSG), and organosilicates such as silsesquioxane, siloxane, or

organosilicate glass. The dielectric layer 723 may include pores or other voids to further reduce its dielectric constant.

[0047] Next, for embodiments of the invention in which a replacement metal gate process is used, the gate stack 217 is removed using an etching process at operation 118 to expose the regrown drain/source extension 618A which filled in the extension cavity 421. Methods for removing layers of the gate stack 217 are well known in the art. In alternate implementations, only the gate electrode 213 and gate cap 214 is removed to expose the gate dielectric 212. Figure 8 illustrates the trench opening that is formed when the gate stack is etched away.

[0048] Returning to Figure 1, if the gate dielectric layer is removed, a new gate dielectric layer may be deposited into the trench opening over the channel region 205 at operation 120. The high-k dielectric materials described above may be used here, such as hafnium oxide. The same deposition processes may also be used. Replacement of the gate dielectric layer may be used to address any damage that may have occurred to the original gate dielectric layer during application of the dry and wet etch processes. A metal gate electrode layer may then be deposited over the gate dielectric layer. Conventional metal deposition processes may be used to form the metal gate electrode layer, such as CVD, ALD, PVD, electroless plating, or electroplating. Figure 9 illustrates a high-k gate dielectric layer 924 and a gate electrode layer 926 that have been deposited into the trench opening such that the regrown drain/source extension 618A is disposed below the gate dielectric layer 924 (either subjacent to a portion of gate dielectric layer 924 in contact with a sidewall of the gate electrode layer 926 and the gate stack spacer 319, or below a portion of the gate dielectric layer 924 disposed subjacent to the gate electrode 926).

[0049] The gate electrode layer 926 may consist of a P-type workfunction metal or an N-type workfunction metal, depending on whether the transistor is to be a PMOS or an NMOS transistor. In some implementations, a PMOS transistor is being formed and materials that may be used to form a P-type workfunction metal layer include, but are not limited to, ruthenium, palladium, platinum, cobalt, nickel, and conductive metal oxides, e.g., ruthenium oxide. A P-type metal layer will enable the formation of a PMOS gate electrode with a workfunction that is between about 4.9 eV and about 5.2 eV. Alternately, in some implementations an NMOS transistor is being formed and materials that may be used to form an N-type workfunction metal layer include, but are not limited to, hafnium, zirconium, titanium, tantalum, aluminum, and their alloys, e.g., metal carbides that include

these elements, i.e., hafnium carbide, zirconium carbide, titanium carbide, tantalum carbide, and aluminum carbide. An N-type metal layer will enable the formation of an NMOS gate electrode with a workfunction that is between about 3.9 eV and about 4.2 eV. In some implementations, two or more metal gate electrode layers may be deposited. For instance, a workfunction metal may be deposited followed by a metal gate electrode fill metal such as aluminum metal. Of course, doped polysilicon, silicided silicon, etc., may also be employed in conformance with convention in the art.

[0050] Accordingly, a multi-gate transistor with self-aligned epitaxially regrown source/drain regions has been disclosed that reduce the overall resistance of the multi-gate transistor and increase channel strain due to increased doped silicon volume (e.g., boron doped silicon germanium volume) combined with reduced channel silicon volume. The epitaxial source and drain extensions extend approximately the entire fin height Hsi, form an abrupt boundary between the channel region and the source/drain regions, and have a doping concentration that is more easily controlled, yielding a more optimized source-drain profile.

[0051] The above description of illustrative embodiments of the invention, including what is described in the Abstract, is not intended to be exhaustive or to limit the invention to the precise forms disclosed. While specific implementations of, and examples for, the invention are described herein for illustrative purposes, various equivalent modifications are possible within the scope of the invention, as those skilled in the relevant art will recognize. The scope of the invention is to be determined entirely by the following claims, which are to be construed in accordance with established doctrines of claim interpretation.

CLAIMS

What is claimed is:

1. A method of forming a multi-gate transistor, comprising:

forming a gate stack over a channel region of semiconductor fin having a gate-coupled channel sidewall height (H_{si});

implanting an etch rate controlling dopant into a source/drain region of the semiconductor fin adjacent to the gate stack;

etching the doped fin region to remove a thickness of the semiconductor fin equal to approximately H_{si} and form a source/drain extension cavity exposing a semiconductor substrate portion subjacent to a portion of the gate stack; and

growing a material on the exposed semiconductor substrate to form a regrown source/drain fin region filling the source/drain extension cavity and extending a length away from the gate stack in a direction substantially parallel to a length of the channel.

2. The method of claim 1, wherein the regrown source/drain fin region is grown to a greatest width, along a dimension parallel to a transistor channel width (W_{si}), that is greater than W_{si}.

3. The method of claim 1, wherein an etch rate of the doped fin region is higher than an etch rate of the subjacent semiconductor substrate, and wherein the material regrown on the exposed semiconductor substrate contains silicon.

4. The method of claim 1, wherein the etching of the doped fin regions forms the source/drain extension cavity with an undercut length (X_{UC}) along a dimension perpendicular to a transistor channel width (W_{si}) that is substantially constant across the height H_{si}.

5. The method of claim 4, wherein the undercut length (X_{UC}) extends subjacent to a portion of the gate stack and decreases with etch depths greater than the height H_{si}.

6. The method of claim 4, wherein the undercut length X_{UC}, is constant across the transistor channel width W_{si}.

7. The method of claim 1, further comprising:

forming a first pair of spacers on laterally opposite sidewalls of the gate stack and a second pair of spacers on laterally opposite sidewalls of the semiconductor fin subsequent to implanting the dopant, wherein the first pair of spacers are disposed over the implanted

regions of the semiconductor fin and the second pair of spacers are disposed adjacent to the implanted regions of the semiconductor fin; and

removing the second pair of spacers prior to growing the silicon-containing material, the second pair of spacers removed without etching the first pair of spacers enough to expose a gate electrode layer of the gate stack.

8. The method of claim 7, wherein removing the second pair of spacers further comprises an etching performed subsequent to the etching of the doped fin regions.

9. The method of claim 7, wherein removing the second pair of spacers further comprises an etching performed during the etching of the doped fin regions.

10. The method of claim 1, wherein etching the doped fin region to remove a thickness of the semiconductor fin equal to at least Hsi further comprises etching a thickness approximately equal to H_{si} in a region of the semiconductor fin proximate to a channel region and etching a thickness greater than H_{si} in a region of the semiconductor fin distal from the channel region.

11. The method of claim 10, wherein the etching of a thickness greater than H_{si} in the region of the semiconductor fin distal from the channel region comprises recessing the semiconductor substrate below a top surface of an isolation top surface disposed below a portion of the gate stack adjacent to the semiconductor fin.

12. The method of claim 1, wherein the implanting of the dopant comprises implanting at least one of carbon, phosphorous, or arsenic; and wherein the etching etching the doped fin region comprises a dry etch including a mixture of Cl_2 and another compound selected from the group consisting of NF_3, HBr, SF_6, and Ar..

13. A multi-gate transistor comprising:

a gate stack including a gate dielectric and a gate electrode disposed over a channel region of a semiconductor fin extending from a semiconductor substrate, the channel region having a gate-coupled channel sidewall height of H_{si};

a regrown source/drain semiconductor fin disposed on the substrate, the regrown source/drain semiconductor fin including a source/drain extension region adjacent to the channel region, wherein the source/drain extension region and the channel region form an interface along a height that is approximately equal to H_{si}.

14. The multi-gate transistor of claim 13, wherein the source/drain extension region is subjacent to the gate stack by an amount, along a dimension perpendicular to a transistor channel width (W_{si}), that is constant across the height H_{si}.

15. The multi-gate transistor of claim 14, wherein the amount the source/drain extension region overlaps the gate stack decreases for heights greater than H_{si}, as measured from the gate dielectric interface.

16. The multi-gate transistor of claim 13, wherein the regrown source/drain fin height distal from the channel region is equal to at least H_{si} with a regrown source/drain fin width, along a dimension parallel to a transistor channel width (W_{si}), greater than W_{si}.

17. The multi-gate transistor of claim 16, wherein the regrown source/drain fin width is greater than W_{si} along at least half the height H_{si}.

18. The multi-gate transistor of claim 13, wherein laterally opposite sides of the gate stack are adjacent to a dielectric spacer, and wherein an interlayer dielectric (ILD) is in contact both with an outer sidewall of the dielectric spacer and with a sidewall portion of the regrown source/drain fin located within the height H_{si}.

19. The multi-gate transistor of claim 13, wherein the gate stack comprises a high-k gate dielectric layer and a metal gate electrode, wherein the regrown source/drain fin region comprises carbon and phosphorus doped silicon or boron doped silicon germanium to strain the channel region.

20. The transistor of claim 19, wherein the source/drain extension region is subjacent to the high-k gate dielectric layer by a distance greater than zero.

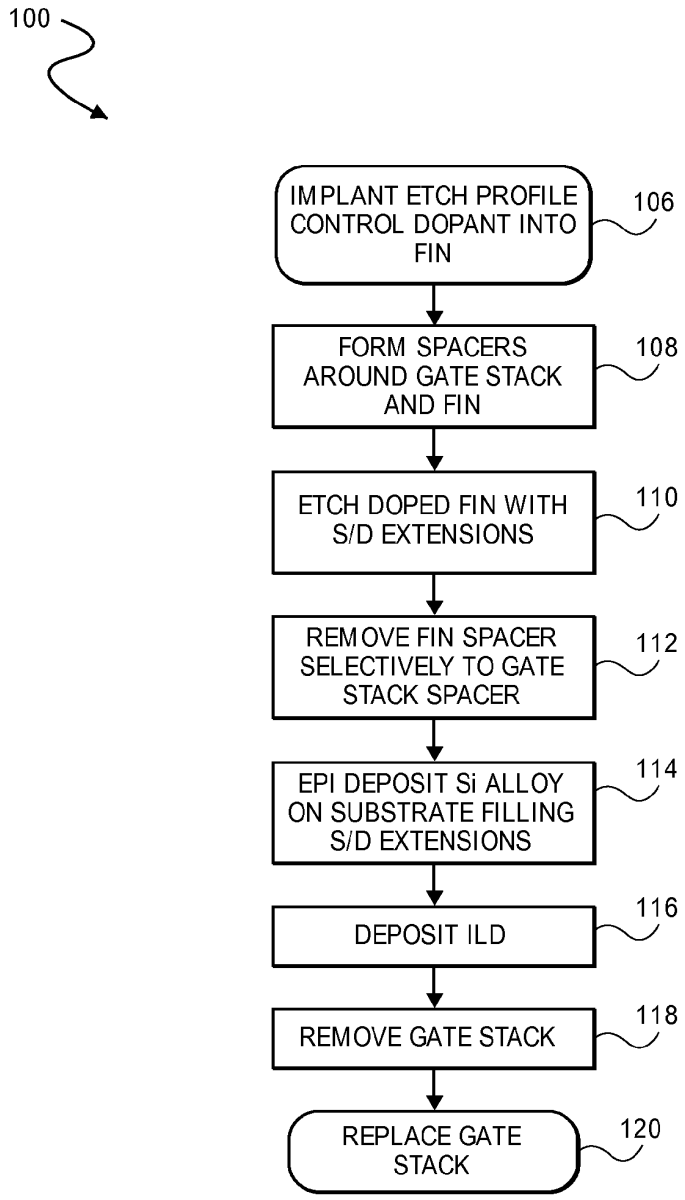

100
IMPLANT ETCH PROFILE CONTROL DOPANT INTO FIN
106
FORM SPACERS AROUND GATE STACK AND FIN
108
ETCH DOPED FIN WITH S/D EXTENSIONS
110
REMOVE FIN SPACER SELECTIVELY TO GATE STACK SPACER
112
EPI DEPOSIT Si ALLOY ON SUBSTRATE FILLING S/D EXTENSIONS
114
DEPOSIT ILD
116
REMOVE GATE STACK
118
REPLACE GATE STACK
120

FIG. 1

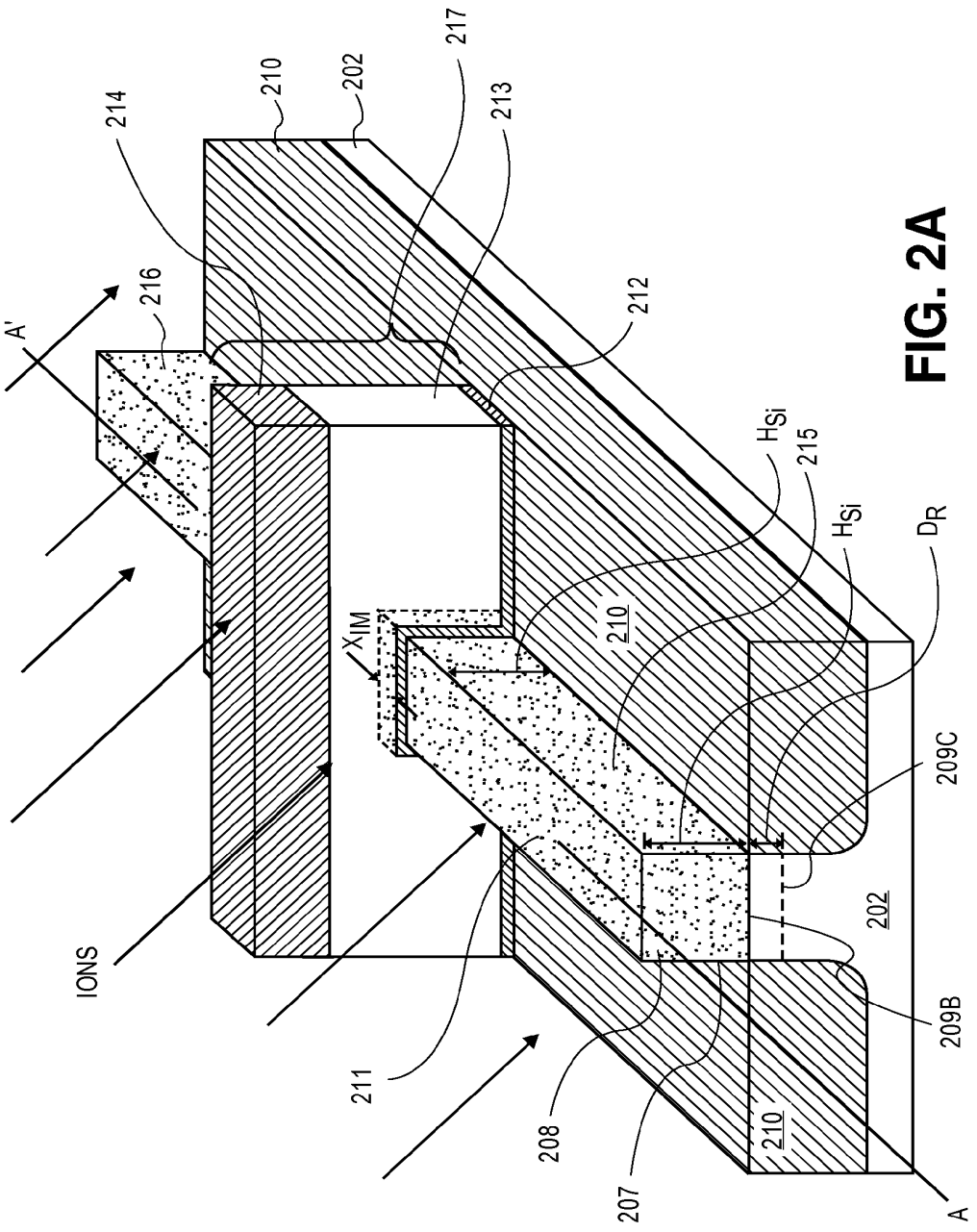

214
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202
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213
216
A'
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H_{Si}
215
H_{Si}
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209C
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IONS
209B
211
208
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207
A

FIG. 2A

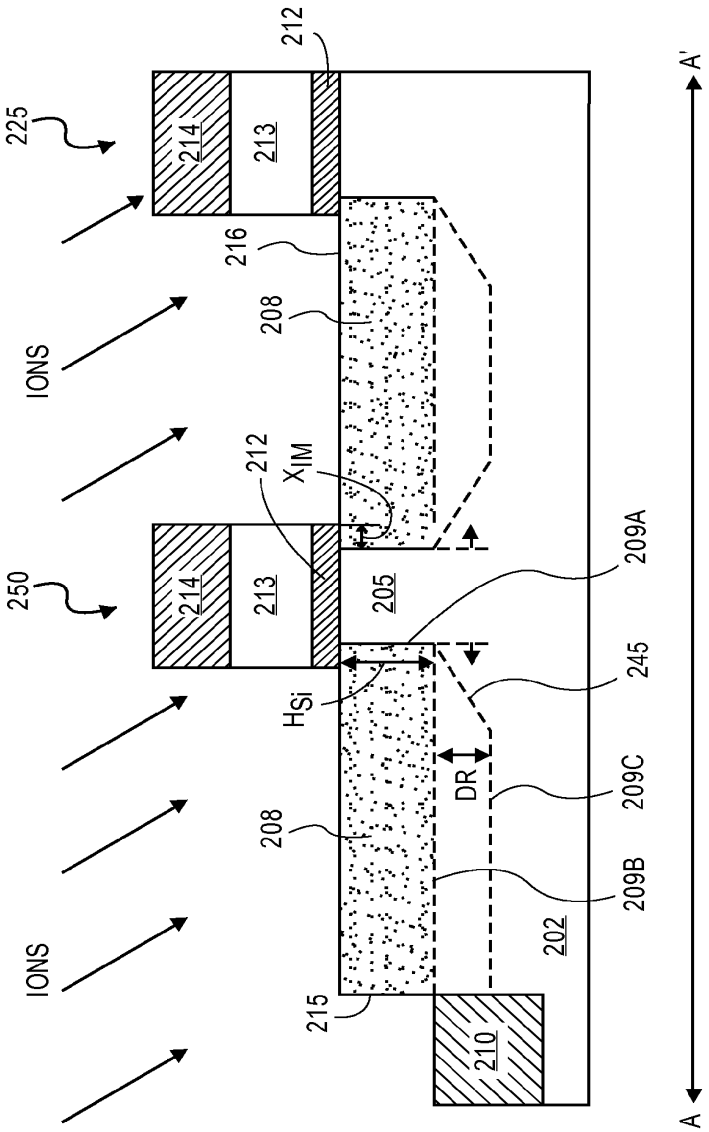

212
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IONS
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X_{IM}
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H_{Si}
DR
209C
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209B
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IONS
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A'
A

FIG. 2B

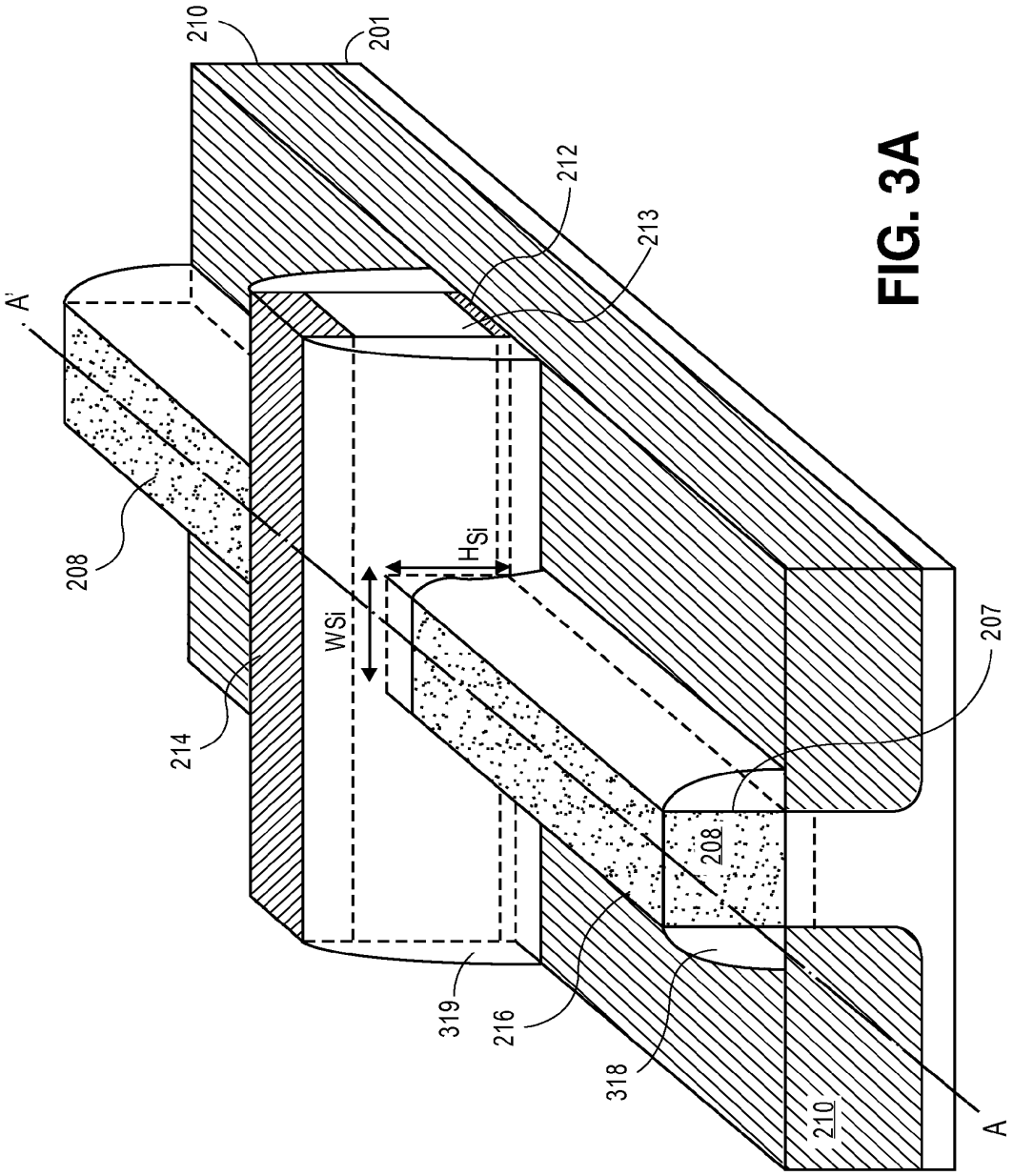


FIG. 3A

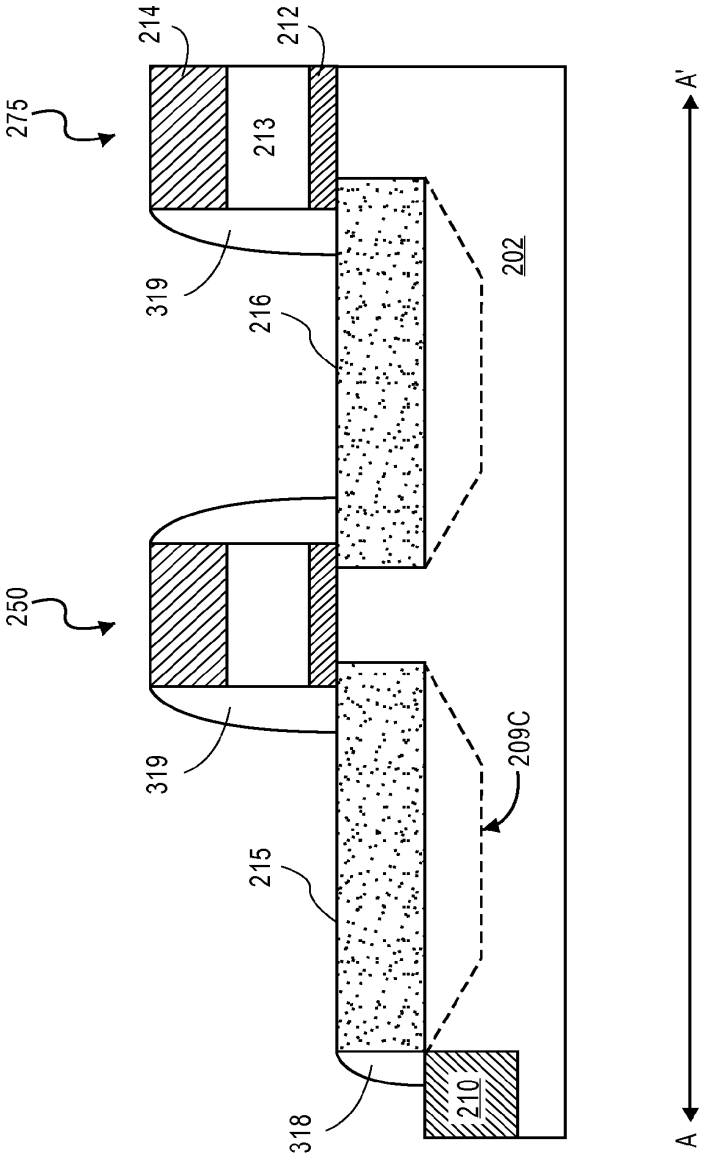


FIG. 3B

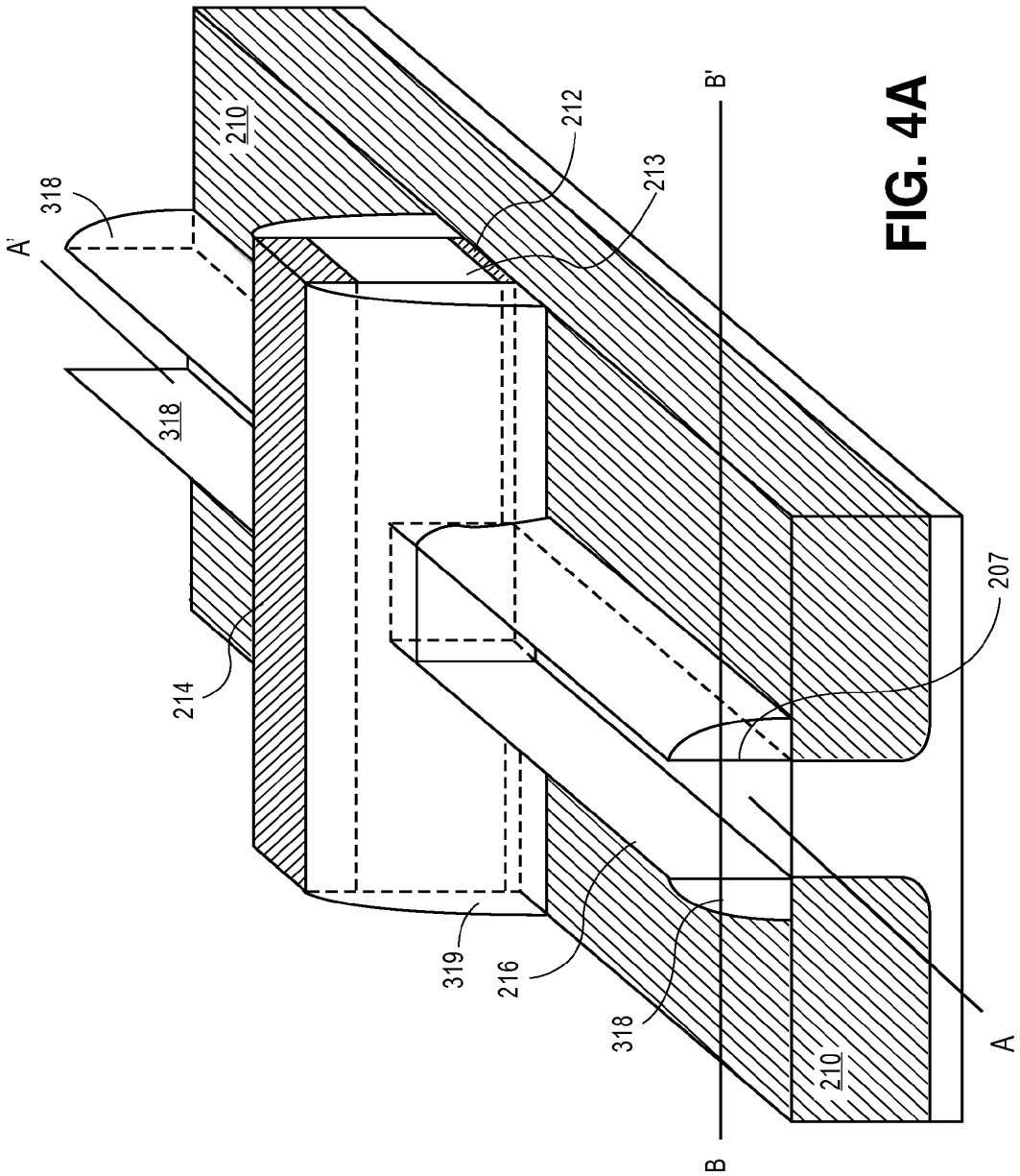


FIG. 4A

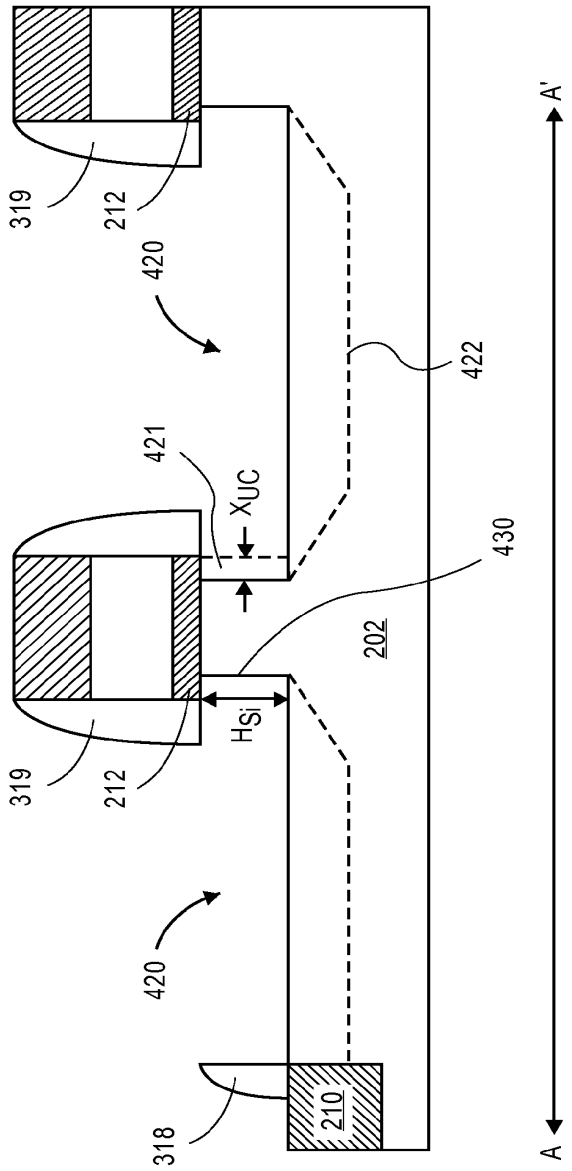


FIG. 4B

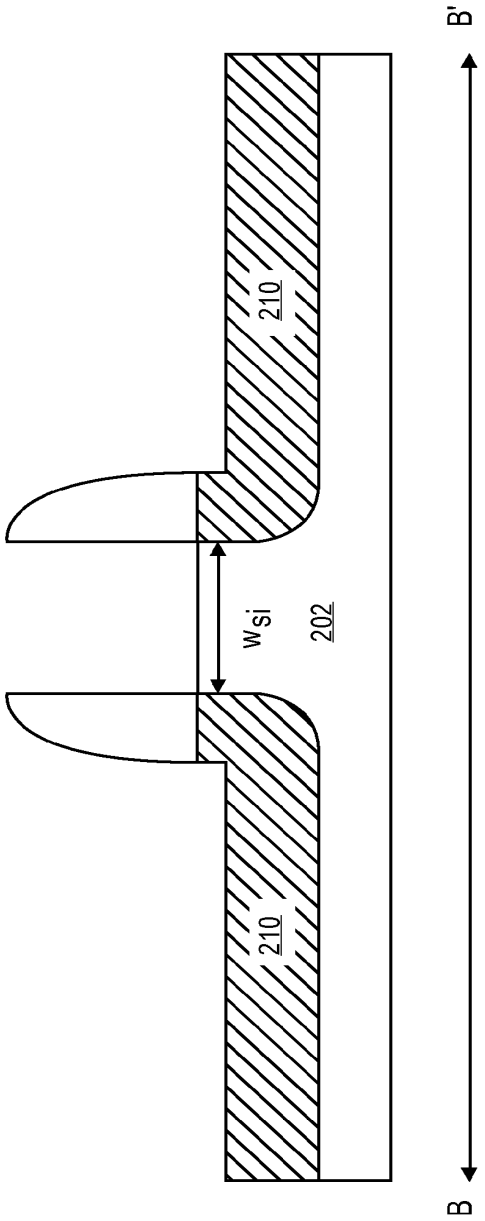


FIG. 4C

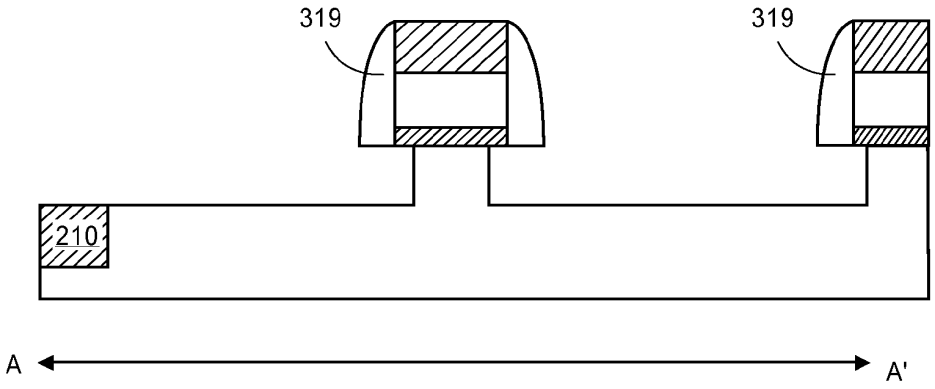


FIG. 5A

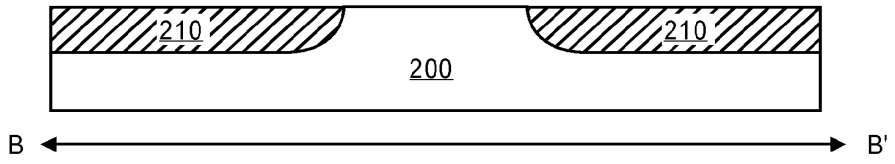


FIG. 5B

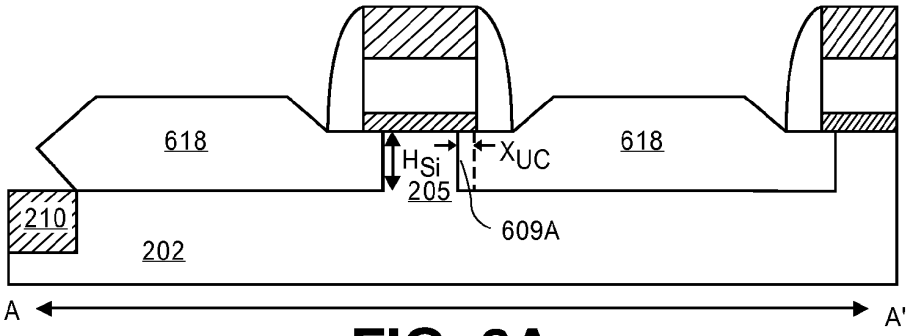


FIG. 6A

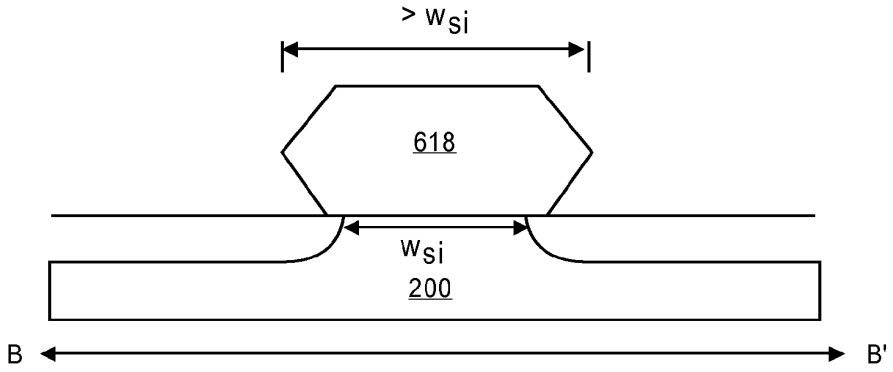


FIG. 6B

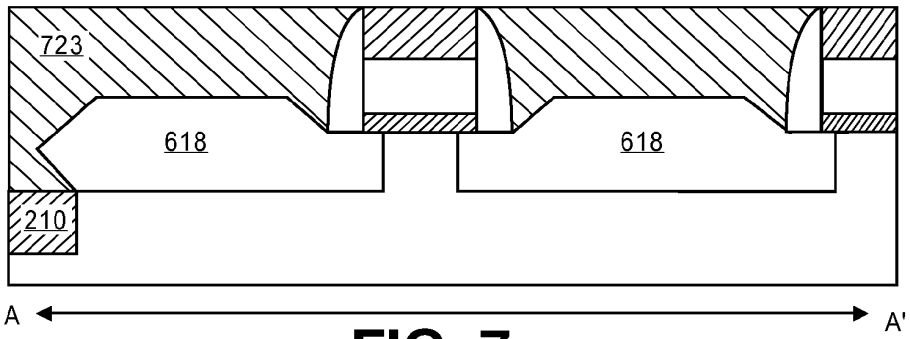


FIG. 7

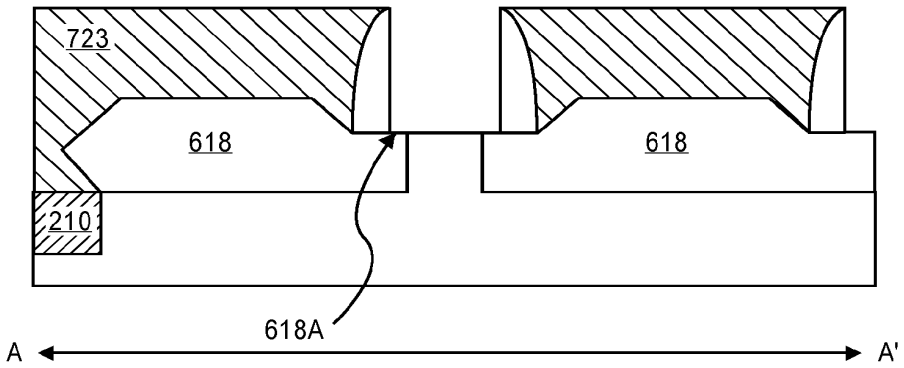


FIG. 8

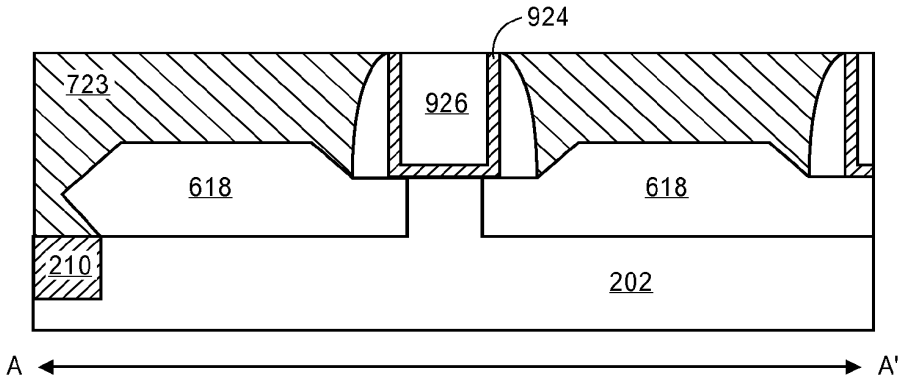


FIG. 9

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2010/057346

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/336(2006.01)i, H01L 29/78(2006.01)i, H01L 21/8238(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 21/336; H01L 29/78; H01L 31/119; H01L 21/8234

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: multi-gate transistor, etching, extension cavity, regrowing

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	US 2006-0286755 A1 (JUSTIN K. BRASK et al.) 21 December 2006 See paragraphs [0051]-[0060];claims 12-20;figures 15-22.	1-6,10-11,13-20 7-9,12
A	US 2006-0258072 A1 (JACK T. KAVALIEROS et al.) 16 November 2006 See paragraphs [0019]-[0032];figures 3A-3H.	1-20
A	US 2007-0231983 A1 (LUCIAN SHIFREN et al.) 04 October 2007 See paragraphs [0012]-[0020];figures 1-4.	1-20
A	JP 10-294457 A (NEC CORP.) 04 November 1998 See paragraphs [0019]-[0031];claims 1-3;figures 1,4.	1-20

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
24 JUNE 2011 (24.06.2011)	**24 JUNE 2011 (24.06.2011)**

Name and mailing address of the ISA/KR	Authorized officer
Korean Intellectual Property Office Government Complex-Daejeon, 189 Cheongsa-ro, Seo-gu, Daejeon 302-701, Republic of Korea Facsimile No. 82-42-472-7140	Lee, Byul Sup Telephone No. 82-42-481-8497

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2010/057346

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2006-0286755 A1	21.12.2006	US 7858481 B2	28.12.2010
US 2006-0258072 A1	16.11.2006	US 2008-318385 A1	25.12.2008
		US 7465976 B2	16.12.2008
US 2007-0231983 A1	04.10.2007	CN 101416297 A	22.04.2009
		DE 112007000662 B4	23.09.2010
		DE 112007000662 T5	30.04.2009
		GB 0812725 D0	20.08.2008
		GB 2448258 A	08.10.2008
		JP 2009-529803 A	20.08.2009
		JP 2009-529803 T	20.08.2009
		KR 10-1017477 B1	25.02.2011
		KR 10-2008-0108496 A	15.12.2008
		US 2009-230480 A1	17.09.2009
		US 7566605 B2	28.07.2009
		US 7851291 B2	14.12.2010
		WO 2007-126909 A1	08.11.2007
JP 10-294457 A	04.11.1998	JP 3033518 B2	17.04.2000

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(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
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H01L 21/28 (2006.01)

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7 December 2010 (07.12.2010)

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(30) **Priority Data**:
12/655,408 30 December 2009 (30.12.2009) US

(71) **Applicant** *(for all designated States except US)*: **INTEL CORPORATION** [US/US]; 2200 Mission College Boulevard, MS: RNB-4-150, Santa Clara, California 95052 (US).

(72) **Inventors; and**

(75) **Inventors/Applicants** *(for US only)*: **BOHR, Mark T.** [US/US]; 19475 SW Suncrest Lane, Aloha, Oregon 97007 (US). **GHANI, Tahir** [US/US]; 2501 NW 229th Avenue, Hillsboro, Oregon 97124 (US). **RAHHAL-ORABI, Nadia M.** [US/US]; 1894 NE Ashberry Dr., Hillsboro, Oregon 97124 (US). **JOSHI, Subhash** [IN/US]; 496 NE 61st Way, Hillsboro, Oregon 97124 (US). **STEIGERWALD, Joseph M.** [US/US]; 11893 NW Shearer Hill Road, Forest Grove, Oregon 97116 (US). **KLAUS, Jason W.** [US/US]; 11967 NW Coleman Dr, Portland, Oregon 97229 (US). **HWANG, Jack** [US/US]; 75 SW 68th Ave, Portland, Oregon 97225 (US). **MACKIEWICZ, Ryan** [US/US]; 15145 SW Trenton Ct, Beaverton, Oregon 97006 (US).

(74) **Agents**: **VINCENT, Lester J.** et al.; Blakely Sokoloff Taylor & Zafman, 1279 Oakmead Parkway, Sunnyvale, California 94085 (US).

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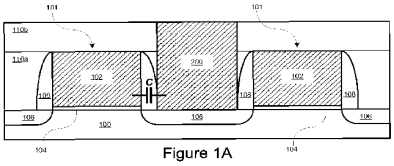


Figure 1A

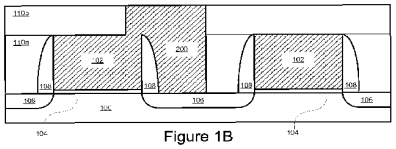


Figure 1B

(57) **Abstract**: A transistor comprises a substrate, a pair of spacers on the substrate, a gate dielectric layer on the substrate and between the pair of spacers, a gate electrode layer on the gate dielectric layer and between the pair of spacers, an insulating cap layer on the gate electrode layer and between the pair of spacers, and a pair of diffusion regions adjacent to the pair of spacers. The insulating cap layer forms an etch stop structure that is self aligned to the gate and prevents the contact etch from exposing the gate electrode, thereby preventing a short between the gate and contact. The insulator-cap layer enables self-aligned contacts, allowing initial patterning of wider contacts that are more robust to patterning limitations.

SELF-ALIGNED CONTACTS

Background

Metal-oxide-semiconductor (MOS) transistors, such as MOS field effect transistors (MOSFET), are used in the manufacture of integrated circuits. MOS transistors include several components, such as a gate electrode, gate dielectric layer, spacers, and diffusion regions such as source and drain regions. An interlayer dielectric (ILD) is typically formed over the MOS transistor and covers the diffusion regions.

Electrical connections are made to the MOS transistor by way of contact plugs that are typically formed of a metal such as tungsten. The contact plugs are fabricated by first patterning the ILD layer to form vias down to the diffusion regions. The patterning process is generally a photolithography process. Next, metal is deposited in the vias to form the contact plugs. A separate contact plug is formed down to the gate electrode using the same or a similar process.

One problem that can occur during the fabrication of a contact plug is the formation of a contact-to-gate short. A contact-to-gate short is a short circuit that occurs when the contact plug is misaligned and comes into electrical contact with the gate electrode. One conventional approach to preventing contact-to-gate shorts is by controlling registration and critical dimensions (CDs). Unfortunately, for transistors with gate pitches (gate length + space) at or below 100 nanometers (nm), CD control for gate and contact dimensions needs to be less than 10 nm and the registration control between gate and contact layers also needs to be less than 10 nm to deliver a manufacturable process window. Thus, the likelihood of a contact shorting to a gate is very high. This problem becomes more prevalent as transistor gate pitch dimensions are scaled down further because the critical dimensions become much smaller.

Brief Description of the Drawings

Figures 1A illustrates a substrate and two conventional MOS transistors with a correctly aligned trench contact.

Figure 1B illustrates a misaligned trench contact formed to a diffusion region of the MOS transistors, resulting in a contact-to-gate short.

Figures 2A illustrates a substrate and two MOS transistors having insulator-cap layers atop their respective metal gate electrodes in accordance with one implementation of the invention.

Figure 2B illustrates a correctly aligned trench contact formed between two MOS transistors of the invention having insulator-cap layers.

Figure 2C illustrates a misaligned trench contact formed between two MOS transistors of the invention having insulator-cap layers, where the misalignment does not result in a contact-to-gate short.

Figures 3A to 3C illustrate an insulator-cap layer formed after a replacement metal gate process, in accordance with an implementation of the invention.

Figures 4A to 4C illustrate an insulator-cap layer formed after a replacement metal gate process, in accordance with another implementation of the invention.

Figures 5A to 5I illustrate a fabrication process for an insulator-cap layer that extends over the spacers of a MOS transistor, in accordance with an implementation of the invention.

Figures 6A to 6F illustrate a fabrication process for a metal gate electrode having a stepped profile, in accordance with an implementation of the invention.

Figures 7A to 7C illustrate MOS transistors having both metal gate electrodes with stepped profiles and insulator-cap layers that extend over the spacers, in accordance with an implementation of the invention.

Figure 8A to 8F illustrate contact sidewall spacers in accordance with an implementation of the invention.

Figures 9A to 9D illustrate a fabrication process to form an insulating-cap atop a metal gate electrode in accordance with an implementation of the invention.

Figures 10A to 10G illustrate a fabrication process to form a metal stud and insulating spacers atop a trench contact in accordance with an implementation of the invention.

Detailed Description

Described herein are systems and methods of reducing the likelihood of contact-to-gate shorts during the fabrication of metal-oxide-semiconductor (MOS) transistors. In the following description, various aspects of the illustrative implementations will be described using terms commonly employed by those skilled in the art to convey the substance of their work to others skilled in the art. However, it will be apparent to those skilled in the art that the present invention may be practiced with only some of the described aspects. For purposes of explanation, specific numbers, materials and configurations are set forth in order to provide a thorough understanding of the illustrative implementations. However, it will be apparent to one skilled in the art that the present invention may be practiced without the specific details. In other instances, well-known features are omitted or simplified in order not to obscure the illustrative implementations.

Various operations will be described as multiple discrete operations, in turn, in a manner that is most helpful in understanding the present invention, however, the order of description should not be construed to imply that these operations are necessarily order dependent. In particular, these operations need not be performed in the order of presentation.

Figure 1A illustrates a substrate 100 and two MOS transistors 101. The MOS transistors 101 include gate electrodes 102, gate dielectric layers 104, and spacers 108. Diffusion regions 106 are formed in the substrate 100. Interlayer dielectrics (ILD), such as ILD layers 110a and 110b, are deposited in the regions between and around the two MOS transistors 101.

Figure 1A also illustrates a trench contact 200 that is formed through the ILD layers 110a/b down to the diffusion region 106. The trench contact 200 is typically formed using a photolithography patterning process followed by a metal deposition process. Photolithography patterning processes and metal deposition processes are well known in the art. The photolithography patterning process etches a trench opening through the ILD layers 110a/b down to the diffusion region 106. The metal deposition process, such as electroplating, electroless plating, chemical vapor deposition, physical vapor deposition, sputtering, or atomic layer deposition, fills the trench opening with a metal such as tungsten or copper. A metal liner is often deposited prior to the metal, such

as a tantalum or tantalum nitride liner. A planarization process, such as chemical-mechanical polishing (CMP), is used to remove any excess metal and complete the fabrication of the trench contact 200.

It should be noted that in alternate implementations of the invention, via contacts may be used instead of trench contacts. Thus, the contact opening may be either a trench shape or a via shape, depending on the patterning process used or the needs of a particular integrated circuit process. The implementations of the invention described herein will refer to contact trench openings and trench contacts, but it should be noted that via openings and via contacts (also known as contact plugs or via plugs) can be used instead of contact trench openings and trench contacts in any of these implementations.

As integrated circuit technology advances, transistor gate pitches progressively scale down. This gate pitch scaling has resulted in a number of new, problematic issues, one of which is increased parasitic capacitance (denoted by the "C" in Figure 1A) caused by relatively tight spacing between the trench contact 200 and the diffusion region 106 on one side and the gate electrode 102 on the other. The spacers 108 tend to provide the bulk of the separation between the trench contact 200/diffusion region 106 and the gate electrodes 102. Conventional spacer materials, such as silicon nitride, do little to reduce this parasitic capacitance. Unfortunately, parasitic capacitance degrades transistor performance and increases chip power.

Another problematic issue caused by gate pitch scaling is the formation of contact-to-gate (CTG) shorts. The fabrication process for the trench contact 200 is designed to prevent the trench contact 200 from coming into physical contact with the metal gate electrode 102. When such contact occurs, a CTG short is created that effectively ruins the MOS transistor. CTG shorts have become a major yield limiter as transistor gate pitches have scaled down below 100 nanometers (nm).

Current methods to reduce CTG shorts include controlling registration and patterning contacts with smaller critical dimensions. However, as gate pitch has scaled down, the registration requirements are becoming very difficult to meet with existing technology. For instance, transistors with gate pitches at or below 100 nm require CD control and layer registration control of less than 10 nm to deliver a manufacturable process window. Thus, the likelihood of a contact shorting to a gate is very high.

Figure 1B illustrates what happens when the trench contact 200 is misaligned. The same photolithography processes are used, but as shown, the trench contact 200 is formed at a location that is not completely within the area between the two spacers 108. The misalignment causes the trench contact 200 to be in physical contact with one of the gate electrodes 102, thereby creating a contact-to-gate short.

In accordance with implementations of the invention, an insulator-capped gate electrode may be used to minimize the likelihood of contact-to-gate shorts. In one implementation, the insulator-cap layer is formed atop the gate electrode 102 and within the spacers 108 of the MOS transistor 101. In some implementations of the invention, the insulator-cap can consume a significant portion of the volume that exists between the spacers. For instance, the insulator-cap can consume anywhere from 10% to 80% of the volume that exists between the spacers, but will generally consume between 20% and 50% of that volume. The gate electrode and gate dielectric layer consume the majority of the remaining volume. Materials that may be used to form the insulator-cap are described below.

Figure 2A illustrates an insulator-capped metal gate electrode in accordance with one implementation of the invention. A substrate 100 is shown in Figure 2A upon which MOS transistors 101 are formed. The substrate 100 may be a crystalline semiconductor substrate formed using a bulk silicon substrate or a silicon-on-insulator substructure. In other implementations, the semiconductor substrate may be formed using alternate materials, which may or may not be combined with silicon, that include but are not limited to germanium, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, gallium antimonide, or other Group III-V materials. Although a few examples of materials from which the substrate may be formed are described here, any material that may serve as a foundation upon which a semiconductor device may be built falls within the spirit and scope of the present invention.

Each MOS transistor 101 can be a planar transistor, as shown in Figure 2A, or can be a nonplanar transistor, such as a double-gate or trigate transistor. Although the implementations described herein illustrate planar transistors, the invention is not limited to planar transistors. Implementations of the invention may also be used on nonplanar transistors, including but not limited to FinFET or trigate transistors. Each MOS transistor

101 includes a gate stack formed of three layers: a gate dielectric layer 104, a gate electrode layer 102, and an insulator-cap layer 300. The gate dielectric layer 104 may be formed of a material such as silicon dioxide or a high-k material. Examples of high-k materials that may be used in the gate dielectric layer 104 include, but are not limited to, hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate. In some embodiments, the gate dielectric layer 104 may have a thickness between around 1 Angstrom (Å) and around 50 Å. In further embodiments, additional processing may be performed on the gate dielectric layer 104, such as an annealing process to improve its quality when a high-k material is used.

The gate electrode layer 102 is formed on the gate dielectric layer 104 and may consist of at least a P-type workfunction metal or an N-type workfunction metal, depending on whether the transistor is to be a PMOS or an NMOS transistor. In some implementations, the gate electrode layer 102 may consist of two or more metal layers, where at least one metal layer is a workfunction metal layer and at least one metal layer is a fill metal layer.

For a PMOS transistor, metals that may be used for the gate electrode include, but are not limited to, ruthenium, palladium, platinum, cobalt, nickel, and conductive metal oxides, e.g., ruthenium oxide. A P-type metal layer will enable the formation of a PMOS gate electrode with a workfunction that is between about 4.9 eV and about 5.2 eV. For an NMOS transistor, metals that may be used for the gate electrode include, but are not limited to, hafnium, zirconium, titanium, tantalum, aluminum, alloys of these metals, and carbides of these metals such as hafnium carbide, zirconium carbide, titanium carbide, tantalum carbide, and aluminum carbide. An N-type metal layer will enable the formation of an NMOS gate electrode with a workfunction that is between about 3.9 eV and about 4.2 eV.

The insulator-cap layer 300 is formed on the gate electrode layer 102 and may be formed of materials that include, but are not limited to, silicon nitride, silicon oxide, silicon carbide, silicon nitride doped with carbon, silicon oxynitride, other nitride

materials, other carbide materials, aluminum oxide, other oxide materials, other metal oxides, boron nitride, boron carbide, and other low-k dielectric materials or low-k dielectric materials doped with one or more of carbon, nitrogen, and hydrogen. The insulator-cap layer 300 is described in more detail below.

A pair of spacers 108 brackets the gate stack. The spacers 108 may be formed from a material such as silicon nitride, silicon oxide, silicon carbide, silicon nitride doped with carbon, and silicon oxynitride. Processes for forming spacers are well known in the art and generally include deposition and etching process steps.

Diffusion regions 106 are formed within the substrate 100 adjacent to the gate stacks of the MOS transistors 101. For each MOS transistor 101, one adjacent diffusion region 106 functions as a source region and the other adjacent diffusion region 106 functions as a drain region.

The diffusion region 106 may be formed using methods or processes that are well known in the art. In one implementation, dopants such as boron, aluminum, antimony, phosphorous, or arsenic may be implanted into the substrate 100 to form the diffusion regions 106. In another implementation, the substrate 100 may first be etched to form recesses at the locations of the diffusion regions 106. An epitaxial deposition process may then be carried out to fill the recesses with a silicon alloy such as silicon germanium or silicon carbide, thereby forming the diffusion regions 106. In some implementations the epitaxially deposited silicon alloy may be doped in situ with dopants such as boron, arsenic, or phosphorous. In further implementations, alternate materials may be deposited into the recesses to form the diffusion regions 106.

One or more ILD layers 110a/b are deposited over the MOS transistors 101. The ILD layers 110a/b may be formed using dielectric materials known for their applicability in integrated circuit structures, such as low-k dielectric materials. Examples of dielectric materials that may be used include, but are not limited to, silicon dioxide (SiO_2), carbon doped oxide (CDO), silicon nitride, organic polymers such as perfluorocyclobutane or polytetrafluoroethylene, fluorosilicate glass (FSG), and organosilicates such as silsesquioxane, siloxane, or organosilicate glass. The ILD layers 110a/b may include pores or other voids to further reduce their dielectric constant.

Fabrication of a trench contact 200, also referred to as contact patterning, involves at least a photolithography process and an etching process. The photolithography process forms a photoresist hard mask that defines the location of the trench contact 200. The process begins by depositing a photoresist material on the ILD layer 110b. The deposited photoresist layer is exposed to ultraviolet radiation through a patterned optical mask, wherein the pattern defines the trench contact 200. The photoresist layer is then developed to create a photoresist hard mask layer that includes an opening where the trench contact 200 is to be formed. It should be noted that photolithography processes are well known in the art and this description is simply a brief overview of a typical photolithography process. Many intermediate steps, such as baking and alignment steps, have been omitted.

Once the photoresist hard mask is in place defining the trench contact 200, an etching process is carried out. The etchant etches portions of the ILD layer 110a/b that are left exposed by openings in the photoresist hard mask, such as the opening for the trench contact 200. The etchant therefore etches a trench opening down to the diffusion region 106. The etching process used may be a conventional chemical wet etch process or a plasma dry etch process. The etching process is carried out for a duration of time, denoted as T_{ETCH}, that is sufficient to etch the ILD layer 110 all the way down to the diffusion region 106. The etched trench opening is then filled with one or more metals, as described above, to form the trench contact 200.

In accordance with implementations of the invention, the insulator-cap layer 300 has a thickness that is sufficient to protect the metal gate electrode 102 from being exposed during fabrication of the trench contact 200 should the contact trench opening be aligned over the insulator-cap layer. Furthermore, the insulator-cap layer 300 has a thickness that is sufficient to electrically isolate the metal gate electrode 102 from the trench contact 200 after the trench contact 200 is formed. In one implementation of the invention, this thickness can range from 5 nm to 50 nm. In another implementation, the height of the insulator-cap layer can account for 20% to 80% of the overall height of the gate stack. The etching process used to form the contact trench opening is selective to the insulator-cap layer 300. This means the wet or dry etch chemistry will etch the material of the ILD layer 110a/b but will selectively stop and self align to the insulator-cap layer 300 and the sidewall spacers 108.

In accordance with implementations of the invention, the insulator-cap layer 300 also has a thickness that is sufficient to withstand the etching process for the entirety of T_{ETCH} without exposing the underlying metal gate electrode 102. Stated differently, the insulator-cap layer 300 has an initial thickness sufficient to withstand the etching process for a duration of time needed to etch the ILD layer 110a/b all the way down to the diffusion region 106 without any portion of the insulator-cap layer 300 being reduced to a thickness that would permit electrical conductivity between the metal gate electrode 102 and the subsequently formed trench contact 200. After the etching process, the combination of the insulator-cap layer 300 and the spacers 108 electrically isolates the metal gate electrode 102 from the trench contact 200, thereby eliminating CTG shorts.

There are several different ways to form the insulator-cap layer 300 of the invention. In one implementation of the invention, where the gate electrode 102 is formed using a gate-first process, a blanket dielectric layer is initially deposited on a substrate. Next, a blanket electrode layer is deposited atop the dielectric layer. Finally, a blanket insulator layer is formed atop the electrode layer. The deposition processes that are used to deposit the dielectric layer, the electrode layer, and the insulator layer are well known in the art and may include, but are not limited to, processes such as electroplating, electroless plating, chemical vapor deposition, atomic layer deposition, physical vapor deposition, and sputtering. The three layers are then etched using conventional patterning processes, such as photolithography processes, to form a gate stack consisting of a gate dielectric layer 104, a gate electrode layer 102, and an insulator-cap layer 300. Spacers 108 and diffusion regions 106 are then formed on opposing sides of the gate stack. An ILD layer 110a is deposited over the gate stack, the spacers 108, and the diffusion region 110. A trench contact 200 may then be formed as described above.

In an alternate implementation of a gate-first process, a blanket dielectric layer and a blanket electrode layer may be deposited and patterned to form a gate stack that consists of the gate dielectric layer 104 and the gate electrode 102. A pair of spacers 108 and diffusion regions 106 may be formed on either side of the gate stack. Next, an etching process may be carried out to recess the metal gate electrode 102 within the spacers 108, thereby reducing the thickness of the metal gate electrode 102. The recessing of the metal gate electrode 102 results in the formation of a trench between the spacers 108 where the bottom surface of the trench corresponds to the top surface of the recessed metal gate

electrode 102. The metal etch process is followed by an insulator material deposition process that deposits a blanket layer of insulator material and fills the trench between the spacers 108. A polishing process, such as a chemical mechanical planarization process, is used to polish down the insulator material layer and substantially remove any insulator material that is outside of the spacers 108. The removal of this excess insulator material yields an insulator-cap layer 300 that is substantially contained within the spacers 108.

In another implementation of the invention, a gate-last process, such as a replacement metal gate process, is used to form the gate electrode. In this implementation, a blanket dielectric layer and a blanket dummy electrode layer may be initially deposited and patterned to form a gate stack that consists of the gate dielectric layer 104 and a dummy gate electrode (not shown). It should be noted that the term "dummy" is used to indicate that this layer is sacrificial in nature. The materials used in dummy layers may or may not be the same materials that are used in non-dummy layers. For instance, the dummy electrode layer may consist of polysilicon, which is used in real gate electrodes. A pair of spacers 108 and diffusion regions 106 may be formed on either side of the gate stack. Next, the dummy gate electrode may be etched out to form a trench between the spacers 108 and atop the gate dielectric layer 104. An electrode metal layer may then be deposited to fill the trench. The electrode metal layer may be polished down to remove metal outside of the spacers 108 and to confine the electrode metal to the trench between the spacers 108, thereby forming a metal gate electrode 102.

As described above, an etching process is carried out to recess the metal gate electrode 102 within the spacers 108. The recessing of the metal gate electrode 102 results in the formation of a trench between the spacers 108. An insulator material deposition process fills the trench and a polishing process is used to polish down the insulator material layer and substantially remove any insulator material that is outside of the spacers 108. This yields an insulator-cap layer 300 that is substantially contained within the spacers 108.

Figure 2B illustrates a trench contact 200 that is correctly aligned between two MOS transistors having insulator-cap layers 300. In this instance the insulator-cap 300 is not used.

Figure 2C illustrates a misaligned trench contact 200 formed between two MOS transistors having insulator-cap layers 300. As shown, a portion of the misaligned trench contact 200 is situated directly over the gate electrode 102. Unlike the prior art transistors shown in Figure 1B, however, a CTG short is avoided due to the use of the insulator-cap layer 300. The insulator-cap layer 300 electrically isolates the metal gate electrode 102 from the misaligned trench contact 200, allowing the trench contact 200 to be "self-aligned".

Figures 3A to 3C illustrate a slight variation on the transistors of Figure 2A. In Figure 3A, a different implementation of a replacement metal gate process is used to form the transistors. In this implementation, a blanket dummy dielectric layer and a blanket dummy electrode layer are deposited on a substrate. Here, the dummy electrode layer may consist of polysilicon and the dummy dielectric layer may consist of silicon dioxide, both of which are used in real gate electrodes and real gate dielectric layers. These two dummy layers are etched to form a gate stack that consists of a dummy gate dielectric layer and a dummy gate electrode layer. Spacers 108 and diffusion regions 106 are then formed on opposing sides of the gate stack. An ILD layer 110a is deposited over the gate stack, spacers 108, and diffusion regions 106. The ILD layer 110a is planarized to expose the dummy electrode layer.

Next, the dummy electrode layer and the dummy gate dielectric layer are removed using one or more etching processes. The removal of the dummy layers produces a trench between the spacers 108. The substrate 100 forms a bottom surface of the trench. A new high-k gate dielectric layer 104 is deposited into the trench using a chemical vapor deposition process or an atomic layer deposition process. The high-k gate dielectric layer 104 is deposited along the bottom and sidewalls of the trench, thereby forming a "U" shaped gate dielectric layer 104, as shown in Figure 3A. Next, a metal gate electrode layer 102 is deposited atop the high-k gate dielectric layer 104. Processes for forming the metal gate electrode 102 are well known in the art.

In accordance with implementations of the invention, the final metal gate electrode 102 does not fill the trench in its entirety. In one implementation, the metal gate electrode 102 may initially fill the trench in its entirety, but a subsequent etching process may be used to recess the metal gate electrode 102. In another implementation, the metal gate

electrode deposition process only partially fills the trench with the metal gate electrode 102. In both implementations, a trench remains above the final metal gate electrode 102 between the spacers 108.

Finally, an insulator material deposition process is used to deposit a blanket layer of insulator material that fills the trench between the spacers 108. A polishing process, such as a chemical mechanical planarization process, is then used to polish down the insulator material layer and remove substantially any insulator material that is outside of the spacers 108. The removal of this excess insulator yields an insulator-cap layer 300 that is substantially confined within the spacers 108. As shown in Figure 3A, the insulator-cap 300 is also confined within the sidewall portions of the gate dielectric layer 104.

Figure 3B illustrates a trench contact 200 that is correctly aligned between two MOS transistors having insulator-cap layers 300. Figure 3C illustrates a misaligned trench contact 200 formed between two MOS transistors having insulator-cap layers 300. Again, a portion of the misaligned trench contact 200 is situated directly over the gate electrode 102. A CTG short is avoided due to the use of the insulator-cap layer 300, which electrically isolates the metal gate electrode 102 from the misaligned trench contact 200.

Figures 4A to 4C illustrate a slight variation on the transistors of Figure 3A. In Figure 4A, a replacement gate process is used again to form transistors having a "U" shaped gate dielectric layer 104. The gate electrode layer 102 and the gate dielectric layer 104 are initially formed using the same processes detailed above for Figure 3A. Unlike Figure 3A, in this implementation, both the "U" shaped gate dielectric layer 104 and the metal gate electrode 102 are recessed prior to fabrication of the insulator-cap layer 300. One or more etching processes may be used to recess both structures. The insulator-cap 300 is then formed using the same process described above for Figure 3A and is situated atop both the gate electrode 102 and portions of the gate dielectric layer 104, as shown in Figure 4A. Figure 4B illustrates a trench contact 200 that is correctly aligned between two MOS transistors having insulator-cap layers 300. Figure 4C illustrates a misaligned trench contact 200 formed between two MOS transistors having insulator-cap layers 300. Again, a portion of the misaligned trench contact 200 is situated directly over the gate electrode

102. A CTG short is avoided due to the use of the insulator-cap layer 300, which electrically isolates the metal gate electrode 102 from the misaligned trench contact 200.

Figures 5A to 5F illustrate the fabrication of an alternate insulator-cap layer that may be used with a MOS transistor. Initially, Figure 5A illustrates two MOS transistors that include a dummy gate electrode 500 and a dummy gate dielectric layer 502. Also shown are a pair of spacers 108 that are generally formed of silicon nitride.

In accordance with implementations of the invention, one or multiple etching processes are carried out to partially recess both the dummy gate electrode layer 500 and the spacers 108. This dual recess is shown in Figure 5B. The etch chemistry used to recess the dummy gate electrode 500 may differ from the etch chemistry used to recess the spacers 108. The etching processes used may be wet etches, dry etches, or a combination. When the dummy gate electrode 500 and the spacers 108 have been recessed, a trench 503a is formed within the ILD layer 110a where the top surfaces of the dummy gate electrode 500 and the spacers 108 form the bottom of the trench.

Moving to Figure 5C, one or more etching processes are carried out to completely remove the dummy gate electrode 500 as well as the dummy gate dielectric 502. Etching processes to completely remove the dummy gate electrode 500 and dummy gate dielectric are well known in the art. Again, these etches may be wet, dry, or a combination. As shown in Figure 5C, the trench 503a is now much deeper and has a cross-section profile that is relatively wide at the top of the trench 503a and relatively narrow at the bottom of the trench 503a. The dummy gate electrode 500 and dummy gate dielectric 502 are removed in their entirety, thereby exposing the top of the substrate 100.

In Figure 5D, a gate dielectric layer 104 and a metal gate electrode layer 102 are deposited in the trench 503a. A conformal deposition process, such as a CVD or an ALD process, is generally used for the deposition of the gate dielectric layer 104, resulting in a conformal dielectric layer 104 that covers the sidewalls and bottom surface of the trench 503a. The metal gate electrode layer 102 fills the remainder of the trench 503a. In some implementations of the invention, the metal gate electrode layer 102 may consist of two or more layers of metal, for instance, a work function metal layer and a fill metal layer.

In a replacement metal gate process flow, it is very challenging to fill narrow gate trenches with metal gate materials, particularly with transistors having gate widths at or below 22 nm. The process flow described here in Figures 5A to 5D enhances the intrinsic fill characteristics by widening the trench openings at the top without affecting the narrow trench widths at the bottom. Thus, the cross-section profile of the trench 503a, with its relatively wide opening at the top, results in an improved metal gate electrode deposition with fewer voids or other defects.

Next, the metal gate electrode layer 102 and the gate dielectric layer 104 are recessed as shown in Figure 5E, forming a trench 503b. Again, one or more etching processes, either wet or dry, may be used to recess both the gate electrode layer 102 and the gate dielectric layer 104. The etch processes used must be selective to the ILD layer 110a. The metal gate electrode 102 is recessed until its top surface is even with or below the top surfaces of the spacers 108. Although portions of the metal gate electrode 102 are on top of the spacers 108 in Figure 5D, it is important that no portion of the metal gate electrode 102 remain above the top of the spacers 108 after the recessing of the metal gate 102 in Figure 5E. This is because any portion of the metal gate electrode 102 that remains atop the spacers 108 may end up forming a CTG short with a misaligned trench contact.

Moving to Figure 5F, an insulator material deposition process fills the trench 503b and a polishing process is used to polish down the insulator material layer and substantially remove any insulator material that is outside of the trench 503b. This yields an insulator-cap layer 504 that is substantially contained within the trench 503b. The insulator-cap layer 504 has the appearance of a mushroom top as it extends laterally above the spacers 108. The insulator-cap layer 504 improves contact-to-gate margin by extending over the gate spacer 108. The insulator-cap layer 504 may be formed of materials that include, but are not limited to, silicon nitride, silicon oxide, silicon carbide, silicon nitride doped with carbon, silicon oxynitride, other nitride materials, other carbide materials, aluminum oxide, other oxide materials, other metal oxides, and low-k dielectric materials.

Figure 5G illustrates the deposition of an additional ILD layer 110b that covers the insulator-cap layers 504 and sits atop the first ILD layer 110a. Figure 5H illustrates a trench contact 200 that has been fabricated down to the diffusion region 106 through the

ILD layers 110a and 110b. The trench contact 200 of Figure 5H has been correctly aligned between the spacers 108 of adjacent transistors.

Figure 5I illustrates a trench contact 200 that is misaligned. As shown, even though the trench contact 200 is situated on top of the metal gate electrode 102, the insulating-cap layer 504 protects the metal gate electrode 102 and prevents a CTG short from forming by electrically isolating the metal gate electrode 102 from the misaligned trench contact 200.

Another advantage provided by the insulating-cap layer 504 addresses the parasitic capacitance issue discussed above in relation to Figure 1A. Parasitic capacitance issues are caused by the relatively tight spacing between the trench contact 200 and the diffusion region 106 on one side and the gate electrode 102 on the other side. The spacers 108 tend to provide the bulk of the separation between the trench contact 200/diffusion region 106 and the gate electrodes 102, but conventional spacer materials, such as silicon nitride, do little to reduce this parasitic capacitance. Nevertheless, silicon nitride is still used because the etching process that creates a contact trench opening for the trench contact 200 is selective to silicon nitride.

In accordance with this implementation of the invention, materials other than silicon nitride may be used in the spacers 108. Here, the laterally extending insulating-cap layer 504 protects the underlying spacers 108 during etching processes used to fabricate the trench contact 200. These etching processes are generally anisotropic processes, therefore, the etch chemistry need only be selective to the insulating-cap layer 504. The insulating-cap layer 504 can then shield the underlying spacers 108. So with an anisotropic process, the use of the insulating-cap layer 504 means the etch chemistry does not necessarily need to be selective to the material used in the spacers 108. This removes any constraints on the choice of spacer material and enables the use of materials that are optimized for capacitance. For instance, materials such as silicon oxynitride (SiON), carbon-doped silicon oxynitride (SiOCN), or low-k dielectric materials may be used in the spacers 108 to reduce issues with parasitic capacitance.

Figures 6A to 6F illustrate the formation of a stepped metal gate electrode in conjunction with an insulating-cap layer in accordance with an implementation of the invention. Initially, Figure 6A illustrates two MOS transistors that include a dummy gate

electrode 500 and a dummy gate dielectric layer 502. Moving to Figure 6B, one or more etching processes are carried out to completely remove the dummy gate electrode 500 as well as the dummy gate dielectric 502. Etching processes to completely remove the dummy gate electrode 500 and dummy gate dielectric are well known in the art. The dummy gate electrode 500 and dummy gate dielectric 502 are removed in their entirety, thereby exposing the top of the substrate 100.

Figure 6C illustrates the deposition of dual metal gate electrode layers, a conformal metal gate electrode layer 102a and a second metal layer 102b that may or may not be conformal. The initial metal gate electrode layer 102a may be deposited using a conformal deposition process such as chemical vapor deposition or atomic layer deposition. Other processes, such as physical vapor deposition or sputtering, may also be used. The second metal gate electrode 102b is deposited using a conventional deposition process such as chemical vapor deposition, atomic layer deposition, physical vapor deposition, sputtering, or even processes such as electroplating or electroless plating since a conformal layer is not needed for layer 102b.

The initial metal gate electrode layer 102a is typically a workfunction metal layer and can be formed using any of the workfunction metals described above. The second metal gate electrode layer 102b may be a second workfunction metal layer or it may be a low resistance fill metal layer such as aluminum, tungsten, or copper. In accordance with implementations of the invention, the metal used in the metal gate electrode 102a has different etch properties than the metal used in the metal gate electrode 102b.

Moving to Figure 6D, the dual metal gate electrode layers 102a and 102b are etched and recessed to form trenches 600 in which insulating cap layers may be fabricated. In accordance with an implementation of the invention, the etching process removes a larger portion of metal layer 102a than metal layer 102b. This yields a stepped or bulleted profile for the metal gate electrode 102, as shown in Figure 6D. A middle portion of the overall metal gate electrode 102 is relatively thicker than the outer edge portions of the overall metal gate electrode 102. Stated differently, a middle portion of the metal gate electrode 102 has a relatively larger height than side portions of the metal gate electrode 102. This stepped profile for the metal gate electrode 102 provides advantages as explained below in Figure 6F.

In one implementation, a single etching process is used that etches the metal gate electrode layer 102a at a faster rate than the metal gate electrode layer 102b. In other words, the etch chemistry is more selective to the metal gate electrode 102b. In another implementation, two etching processes may be used, one for metal layer 102a and another for metal layer 102b. If two etching processes are used, a larger portion of metal layer 102a must be removed relative to metal layer 102b. Thus in one implementation, the first of the two etching processes may be selective to the metal layer 102b and the second of the two etching processes may be selective to the metal layer 102a. The etching processes used may be wet etch, dry etch, or a combination of both. It will be appreciated by those of ordinary skill in the art that for almost any arbitrary pair of metals used in metal layers 102a and 102b, it is possible to find a wet or dry chemical etch that will differentiate between the two metals.

As shown in Figure 6E, an insulator material deposition process fills the trenches 600 and a polishing process is used to polish down the insulator material layer and substantially remove any insulator material that is outside of the trench 600. This yields an insulator-cap layer 602 that is substantially contained within the trench 600. The insulator-cap layer 602 is relatively thick at its outer edges and relatively thin at its middle portion due to the stepped profile of the metal gate electrode 102. The insulator-cap layer 602 may be formed of materials that include, but are not limited to, silicon nitride, silicon oxide, silicon carbide, silicon nitride doped with carbon, silicon oxynitride, other nitride materials, other carbide materials, aluminum oxide, other oxide materials, other metal oxides, and low-k dielectric materials.

Figure 6F illustrates a trench contact 200 that is misaligned. As shown, even though the trench contact 200 is situated on top of the metal gate electrode 102, the insulating-cap layer 602 protects the metal gate electrode 102 and prevents a CTG short from forming by electrically isolating the metal gate electrode 102 from the misaligned trench contact 200. The stepped profile of the metal gate electrode 102 provides at least two advantages. First, the stepped profile causes the thick portion of the insulator-cap layer 602 to be positioned between the metal gate electrode 102 and the trench contact 200, thereby providing strong electrical isolation. Second, the stepped profile allows the middle portion of the metal gate electrode 102 to remain thick, thereby lowering the electrical resistance of the metal gate electrode 102 by increasing its metal content. In

various implementations of the invention, the stepped profile may be optimized by trying to maximize the volume or width of the middle portion of the metal gate electrode 102 while maintaining its electrical isolation from misaligned trench contact 200. In some implementations, this may be done by increasing the size or thickness of the metal gate electrode 102b. In further implementations, this may be done by using more than two metal gate electrode layers to more finely tailor the stepped profile.

In accordance with another implementation of the invention, Figures 7A to 7C illustrate the fabrication of a MOS transistor that combines the wide insulator-cap layer 504 of Figure 5F with the stepped profile metal gate electrode 102 of Figures 6D to 6F. Starting with the structure shown in Figure 5C, dual metal gate electrode layers are deposited as shown in Figure 7A. One layer is a conformal metal gate electrode layer 102a and the other layer is a second metal layer 102b that may or may not be conformal. The initial metal gate electrode layer 102a is typically a workfunction metal layer and the second metal gate electrode layer 102b may be a second workfunction metal layer or it may be a fill metal layer. In accordance with implementations of the invention, the metal used in the metal gate electrode 102a has different etch properties than the metal used in the metal gate electrode 102b.

Moving to Figure 7B, the dual metal gate electrode layers 102a and 102b, as well as the gate dielectric layer 104, are etched and recessed. The etch process is selective to the metal gate electrode 102b. This yields a stepped profile for the metal gate electrode 102, as shown in Figure 7B. A middle portion of the overall metal gate electrode 102 is relatively thicker than the outer edge portions of the overall metal gate electrode 102.

An insulating material is then deposited and planarized to form insulator-cap layers 700 atop each metal gate electrode 102. This is shown in Figure 7C. Also shown is a misaligned trench contact 200. The stepped profile of the metal gate electrode 102 allows the thick portion of the insulator-cap layer 700 to electrically isolate the metal gate electrode 102 from the trench contact 200. The stepped profile also allows a middle portion of the metal gate electrode 102 to remain thick, thereby reducing electrical resistance. In this implementation, the insulating-cap layer 700 extends over the recessed spacers 108, thereby protecting the spacers during the trench contact 200 etch process and

allowing a material to be used in the spacers 108 that is optimized for reducing parasitic capacitance between the trench contact 200 and the metal gate electrode 102.

Figures 8A to 8F illustrate another implementation of the invention in which contact sidewall spacers are used to reduce CTG shorts and to improve parasitic capacitance issues. Figure 8A illustrates a contact trench opening 800 that has been etched through ILD layers 110a and 110b down to the diffusion region 106. As explained above, photolithography patterning and etching processes are used to form the contact trench opening 800.

Also shown in Figure 8A is a silicide layer 802 that has been formed at the bottom of the contact trench opening 800. To fabricate the silicide layer 802, a conventional metal deposition process, such as a sputtering deposition process or an ALD process, may be used to form a conformal metal layer along at least the bottom of the contact trench opening 800. Often the metal will deposit on the sidewalls of the contact trench opening 800 as well. The metal may include one or more of nickel, cobalt, tantalum, titanium, tungsten, platinum, palladium, aluminum, yttrium, erbium, ytterbium, or any other metal that is a good candidate for a silicide. An annealing process may then be carried out to cause the metal to react with the diffusion region 106 and form a silicide layer 802. Any unreacted metal may be selectively removed using known processes. The silicide layer 802 reduces the electrical resistance between the later formed trench contact 200 and the diffusion region 106.

Figure 8B illustrates a pair of contact sidewall spacers 804 that are formed along the sidewalls of the contact trench opening 800, in accordance with an implementation of the invention. The contact sidewall spacers 804 may be formed using deposition and etching processes similar to the fabrication of gate spacers 108. For instance, a conformal layer of an insulating material may be deposited within the contact trench opening 800, resulting in the insulating material being deposited along the sidewalls and bottom surface of the contact trench opening 800. The insulating material may be silicon oxide, silicon nitride, silicon oxynitride (SiON), carbon-doped silicon oxynitride (SiOCN), any other oxide, any other nitride, or any low-k dielectric material. Next, an anisotropic etching process is used to remove the insulating material from the bottom of the contact trench

opening 800, as well as from other areas such as the surface of the ILD layer 110b. This yields the contact sidewall spacers 804 that are shown in Figure 8B.

As will be appreciated by those of skill in the art, a separate patterning process may be used to form vias down to the metal gate electrodes 102 in order to form gate contacts. This separate patterning process will typically involve coating the wafer with a sacrificial photo-definable resist layer, etching the gate contacts, and then removing the photoresist with a wet or dry cleaning process or some combination thereof. This separate patterning process is generally carried out after the contact trench opening 800 has been formed, which means first the resist coating and then the wet or dry clean chemistry enters the contact trench opening 800 and can degrade the silicide layer 802. Therefore, in accordance with an implementation of the invention, the conformal layer of insulating material used to form the spacers 804 is deposited before the patterning process for the gate contacts. The conformal layer remains in place to protect the silicide layer 802 until after the gate contacts have been patterned. Then the anisotropic etch described above may be carried out to etch the conformal layer and form the spacers 804.

It should be noted that the silicide layer 802 is formed prior to fabrication of the contact sidewall spacers 804, which is when the contact trench opening 800 is at its largest width. By forming the silicide layer 802 before forming the contact sidewall spacers 804, a relatively wider silicide layer 802 can be formed to provide better electrical resistance properties, such as lower intrinsic contact resistance. If the contact sidewall spacers 804 are formed first, then less of the diffusion region 106 would be exposed for the silicide fabrication process, yielding a relatively shorter silicide layer.

A metal deposition process is then carried out to fill the contact trench opening 800 and form the trench contact 200, as shown in Figure 8C. As noted above, the metal deposition process can be any metal deposition process, such as electroplating, electroless plating, chemical vapor deposition, physical vapor deposition, sputtering, or atomic layer deposition. The metal used may be any metal that provides suitable contact properties, such as tungsten or copper. A metal liner is often deposited prior to the metal, such as a tantalum or tantulum nitride liner. A CMP process is used to remove any excess metal and complete the fabrication of the trench contact 200.

The contact sidewall spacers 804 provide an additional layer of protection between the gate electrodes 102 and the trench contact 200. The final trench contact 200 has a relatively narrower width than trench contacts 200 formed using conventional processes, thereby reducing the likelihood of CTG shorts. And the additional layer of insulation between the gate electrodes 102 and the trench contact 200 reduces parasitic capacitance.

Figures 8D to 8F illustrate the fabrication of contact sidewall spacers 804 when the contact is misaligned. Figure 8D illustrates a misaligned contact trench opening 800 that has been etched through ILD layers 110a and 110b down to the diffusion region 106. The insulating-cap layer 300 protects the metal gate electrode 102 from being exposed during this etching process, in accordance with an implementation of the invention. Also shown in Figure 8D is a silicide layer 802 that has been formed at the bottom of the contact trench opening 800. Fabrication processes for the silicide layer 802 were provided above.

Figure 8E illustrates a pair of contact sidewall spacers 804 that are formed along the sidewalls of the contact trench opening 800, in accordance with an implementation of the invention. The contact sidewall spacers 804 may be formed by depositing and etching a conformal layer of an insulating material, as explained above.

A metal deposition process is then carried out to fill the contact trench opening 800 and form the trench contact 200, as shown in Figure 8F. Here again, the contact sidewall spacers 804 provide an additional layer of protection between the gate electrodes 102 and the trench contact 200. The contact sidewall spacers 804 provide more separation between the final trench contact 200 and the metal gate electrodes 102, thereby reducing the likelihood of CTG shorts. And the additional layer of insulation between the gate electrodes 102 and the trench contact 200 reduces parasitic capacitance.

Figures 9A to 9D illustrate another process for forming an insulating-cap layer in accordance with an implementation of the invention. Figure 9A illustrates two MOS transistors having metal gate electrodes 102 and gate dielectric layer 104. The gate electrode layer 102 may include two or more layers (not illustrated), such as a workfunction metal layer and a fill metal layer. Although the gate dielectric layer 104 shown corresponds to a replacement-metal gate process, the following process may also be used with transistors formed using a gate-first approach.

A metal-cap 900 is formed atop the metal gate electrode 102, as shown in Figure 9A. In accordance with implementations of the invention, the metal-cap 900 is formed using a selective deposition process. Some selective deposition processes include, but are not limited to, electroless plating and chemical vapor deposition. Metals that may be selectively deposited include, but are not limited to, cobalt, nickel, platinum, copper, polysilicon, tungsten, palladium, silver, gold, and other noble metals. As will be appreciated by those of skill in the art, the choice of whether an electroless process or a CVD process is used will depend on the composition of the metal gate electrode 102 and the specific metal that is used in the metal-cap 900. In one example, if the top portion of the metal gate electrode 102 consists of copper metal, then cobalt metal can be electrolessly deposited on the copper. In another example, tungsten or polysilicon can be deposited by CVD on almost any metal that is used in the metal gate electrode 102. In another example, if the top portion of the metal gate electrode 102 consists of a noble metal, then most metals may be deposited using an electroless process on the noble metal. As will be appreciated by those of ordinary skill in the art, in general, electroless processes require a noble metal for both the substrate metal and the metal to be deposited. Therefore combinations of metals such as cobalt, nickel, copper, platinum, palladium, gold, and silver are possible.

Moving to Figure 9B, an ILD layer 902 is blanket deposited over the ILD 110a and the metal-caps 900. A CMP process is then used to planaraize both the ILD layer 902 and the metal-caps 900 and cause their top surfaces to be substantially even. This is done to expose the top surface of the metal-caps 900 after the ILD deposition.

Next, as shown in Figure 9C, an etching process is used to remove the metal-caps 900 from within the ILD layer 902. In one implementation, a wet etch chemistry may be applied to remove the metal-caps 900. In accordance with implementations of the invention, the etch chemistry that is used must be selective to both the ILD layer 902 and the metal gate electrode 102. This enables the metal-caps 900 to be removed with minimal impact to the ILD layer 902 and the metal gate electrode 102. The removal of the metal-caps 900 yields voids 904 within the ILD layer 902.

Moving to Figure 9D, an insulating layer, such as a silicon nitride layer, may be deposited and planarized to fill in the voids 904, thereby forming self-aligned insulating-

cap layers 906. This insulating layer is generally deposited as a blanket layer that fills the voids 904 and covers the ILD layer 902. A planarization process is then used to remove any excess material that is outside of the voids 904. This confines the insulating material to the voids 904, thereby forming insulating-cap layers 906. The insulator-cap layers 906 may be formed of materials that include, but are not limited to, silicon nitride, silicon oxide, silicon carbide, silicon nitride doped with carbon, silicon oxynitride, other nitride materials, other carbide materials, aluminum oxide, other oxide materials, other metal oxides, and low-k dielectric materials. The only constraint is that the material used in the insulator-cap layers 906 be dissimilar to the material used in the ILD layer 902.

Figures 10A to 10G illustrate a process for forming a self-aligned metal stud atop the trench contact 200 and a pair of insulating spacers that further insulate the metal stud from the metal gate electrodes 102, in accordance with an implementation of the invention. Figure 10A illustrates two MOS transistors having metal gate electrodes 102 and gate dielectric layer 104. A trench contact 200 is formed between the two MOS transistors.

A metal-cap 900 is formed atop the trench contact 200, as shown in Figure 10A. In accordance with implementations of the invention, the metal-cap 900 is formed using a selective deposition process. As noted above, selective deposition processes include, but are not limited to, electroless plating and chemical vapor deposition. The same metals and processes described above for use with the metal gate electrode 102 may also be used here with the trench contact 200. The selective deposition process used and the metal used in the metal-cap 900 will depend on the metal that is used in the trench contact 200.

In accordance with implementations of the invention, a selective deposition process is chosen that will deposit metal on only the trench contact 200 and not on the metal gate electrode 102. This can be accomplished by using different types of metals in the trench contact 200 and the metal gate electrode 102. For example, if aluminum is used in the metal gate electrode 102 and a noble metal is used in the trench contact 200, then a selective deposition process can be used to deposit the metal-cap 900 on only the noble metal in the trench contact 200. The same combinations of noble metals described above will work here as well. In some implementations of the invention, when an active metal such as aluminum, tungsten, molybdenum, titanium, tantalum, titanium nitride, or

polysilicon is used in the metal gate electrode 102, then a noble metal such as cobalt, nickel, copper, platinum, palladium, gold, and silver may be used in the trench contact 200.

Moving to Figure 10B, an ILD layer 902 is blanket deposited over the ILD 110a and the metal-cap 900. A CMP process is then used to planaraize both the ILD layer 902 and the metal-cap 900 and cause their top surfaces to be substantially even. This is done to expose the top surface of the metal-cap 900 after the ILD deposition.

Next, as shown in Figure 10C, an etching process is used to remove just the metal-cap 900 from within the ILD layer 902. The etch chemistry that is used must be selective to both the ILD layer 902 and the trench contact 200. This enables the metal-cap 900 to be removed with minimal impact to the ILD layer 902 and the trench contact 200. The removal of the metal-cap 900 yields a void 904 within the ILD layer 902.

Moving to Figure 10D, an insulating layer 906 may be blanket deposited over the ILD layer 902 and within the void 904. The insulating layer 906 may be formed of materials that include, but are not limited to, silicon nitride, silicon oxide, silicon carbide, silicon nitride doped with carbon, silicon oxynitride, other nitride materials, other carbide materials, aluminum oxide, other oxide materials, other metal oxides, and low-k dielectric materials, including materials that are the same or similar to the material used in the ILD layer 902.

Next, an etching process, such as an anisotropic etching process is applied to etch down the insulating layer 906 and form spacers 1000. This is shown in Figure 10E. The etching process also creates a trench 1002 between the two spacers 1000.

Moving to Figure 10F, a metal deposition process is used to deposit a self-aligned metal stud 1004 in the trench 1002 between the spacers 1000 and atop the trench contact 200. In some implementations this metal deposition process may be another selective deposition process, while in other implementations this metal deposition process need not be a selective process. Finally, as shown in Figure 10G, an insulating layer may be deposited and planarized to form an ILD layer 1006. The top of the metal stud 1004 is also planarized to be even with the ILD layer 1006. In accordance with implementations

of the invention, the self aligned metal stud 1004 is prevented from shorting to the gate by the spacers 1000.

Thus, implementations of the invention are described here that form etch stop structures that are self aligned to the gate, preventing the contact etch from exposing the gate electrode to cause shorting between the gate and contact. A contact to gate short is prevented even in the case of the contact pattern overlaying the gate electrode. Implementations of the invention also address problems such as parasitic capacitance between trench contacts and gate electrodes, dielectric breakdown or direct shorts from contact to gate, and degradation of contact silicide during gate contact patterning.

Accordingly, the use of an insulator-cap layer enables self-aligned contacts, which offer a robust manufacturable process. The invention allows initial patterning of wider contacts which is more robust to patterning limitations. The wider contacts are also desirable for a silicide-through-contact process flow. Not only does this eliminate a major yield limiter in contact-to-gate shorts, but it also alleviates major constraints for contact patterning and allows for more variability. From a lithography perspective, the use of an insulator-cap layer increases the registration window and allows for more critical dimension variability. From an etch perspective, the use of an insulator-cap layer makes the fabrication process for MOS transistors more tolerant to different profiles, different critical dimensions, and over-etching of the ILD during trench contact formation.

The above description of illustrated implementations of the invention, including what is described in the Abstract, is not intended to be exhaustive or to limit the invention to the precise forms disclosed. While specific implementations of, and examples for, the invention are described herein for illustrative purposes, various equivalent modifications are possible within the scope of the invention, as those skilled in the relevant art will recognize.

These modifications may be made to the invention in light of the above detailed description. The terms used in the following claims should not be construed to limit the invention to the specific implementations disclosed in the specification and the claims. Rather, the scope of the invention is to be determined entirely by the following claims, which are to be construed in accordance with established doctrines of claim interpretation.

Claims

1. A transistor comprising:

a substrate;

a pair of spacers on the substrate;

a gate dielectric layer on the substrate and between the pair of spacers;

a gate electrode layer on the gate dielectric layer and between the pair of spacers;

an insulating cap layer on the gate electrode layer and between the pair of spacers; and

a pair of diffusion regions adjacent to the pair of spacers.

2. The transistor of claim 1, wherein a height of the combination of the gate dielectric layer, the gate electrode layer, and the insulating cap layer does not exceed a height of the pair of spacers.

3. The transistor of claim 1, wherein the gate dielectric layer is formed along the surface of the substrate and along sidewalls of the pair of spacers.

4. The transistor of claim 1, wherein the insulating cap layer comprises silicon nitride, silicon oxide, silicon carbide, silicon nitride doped with carbon, silicon oxynitride, or aluminum oxide.

5. The transistor of claim 1, wherein the insulating cap layer comprises a nitride material, a carbide material, an oxide material, a metal oxide material, or a low-k dielectric material.

6. The transistor of claim 1, wherein the insulating cap layer comprises boron nitride or boron carbide.

7. The transistor of claim 1, wherein the insulating cap layer comprises a low-k dielectric material doped with one or more of carbon, nitrogen, and hydrogen.

8. A method of forming a transistor comprising:

forming a gate dielectric layer on a substrate;

forming a gate electrode layer on the gate dielectric layer;

forming a pair of spacers on opposing sides of the gate dielectric layer and the gate

electrode layer;

forming a pair of diffusion regions adjacent to the pair of spacers;

recessing the gate electrode layer; and

forming an insulating cap layer on the recessed gate electrode layer within the pair of spacers.

9. The method of claim 8, wherein the forming of the insulating cap layer comprises:

depositing a blanket layer of an insulating material over the recessed gate electrode layer; and

planarizing the insulating material layer to form the insulating cap layer.

10. The method of claim 8, further comprising:

removing the gate electrode layer and the gate dielectric layer after the diffusion regions have been formed, thereby forming a trench between the pair of spacers;

depositing a conformal low-k gate dielectric layer along the sidewalls and bottom surface of the trench between the spacers; and

depositing a metal gate electrode layer on the low-k gate dielectric layer before recessing the metal gate electrode.

11. The method of claim 8, wherein the insulating cap layer comprises silicon nitride, silicon oxide, silicon carbide, silicon nitride doped with carbon, silicon oxynitride, or aluminum oxide.

12. The method of claim 8, wherein the insulating cap layer comprises a nitride material, a carbide material, an oxide material, a metal oxide material, or a low-k dielectric material.

13. The method of claim 8, wherein the insulating cap layer comprises boron nitride or boron carbide.

14. The method of claim 8, wherein the insulating cap layer comprises a low-k dielectric material doped with one or more of carbon, nitrogen, and hydrogen.

15. A method of forming a transistor comprising:

forming a gate stack on a substrate, the gate stack comprising a gate dielectric

layer, a gate electrode layer on the gate dielectric layer, and an insulating cap layer on the gate electrode layer;

forming a pair of spacers on opposing sides of the gate stack; and

forming a pair of diffusion regions adjacent to the pair of spacers;

16. The method of claim 15, wherein the insulating cap layer comprises silicon nitride, silicon oxide, silicon carbide, silicon nitride doped with carbon, silicon oxynitride, or aluminum oxide.

17. The method of claim 15, wherein the insulating cap layer comprises a nitride material, a carbide material, an oxide material, a metal oxide material, or a low-k dielectric material.

18. The method of claim 15, wherein the insulating cap layer comprises boron nitride or boron carbide.

19. The method of claim 15, wherein the insulating cap layer comprises a low-k dielectric material doped with one or more of carbon, nitrogen, and hydrogen.

20. A transistor comprising:

a substrate;

a pair of spacers on the substrate;

a gate dielectric layer on the substrate and between the pair of spacers;

a gate electrode layer on the gate dielectric layer and between the pair of spacers;

an insulating cap layer sited atop the gate electrode layer that extends laterally over the top surfaces of the pair of spacers; and

a pair of diffusion regions adjacent to the pair of spacers.

21. The transistor of claim 20, wherein the gate dielectric layer is formed along the surface of the substrate and along sidewalls of the pair of spacers.

22. The transistor of claim 20, wherein the insulating cap layer comprises silicon nitride, silicon oxide, silicon carbide, silicon nitride doped with carbon, silicon oxynitride, or aluminum oxide.

23. The transistor of claim 20, wherein the insulating cap layer comprises a nitride material, a carbide material, an oxide material, a metal oxide material, or a low-k dielectric material.

24. The transistor of claim 20, wherein the insulating cap layer comprises boron nitride or boron carbide.

25. The transistor of claim 20, wherein the insulating cap layer comprises a low-k dielectric material doped with one or more of carbon, nitrogen, and hydrogen.

26. The transistor of claim 20, wherein the pair of spacers comprises silicon oxynitride, carbon-doped silicon oxynitride, or a low-k dielectric material.

27. A method of forming a transistor comprising:

forming a gate dielectric layer on a substrate;

forming a gate electrode layer on the gate dielectric layer;

forming a pair of spacers on opposing sides of the gate dielectric layer and the gate electrode layer;

forming a pair of diffusion regions adjacent to the pair of spacers;

recessing the gate electrode layer;

recessing the pair of spacers; and

forming an insulating cap layer on the recessed gate electrode layer that extends laterally over the top surfaces of the recessed pair of spacers.

28. The method of claim 27, further comprising:

removing the recessed gate electrode layer and the gate dielectric layer after the spacers have been recessed, thereby forming a trench between the recessed pair of spacers;

depositing a conformal low-k gate dielectric layer along the sidewalls and bottom surface of the trench between the recessed pair of spacers;

depositing a metal gate electrode layer on the low-k gate dielectric layer; and

recessing the metal gate electrode so that a height of the recessed metal gate electrode is similar to a height of the recessed pair of spacers before the insulating cap layer is formed.

29. The method of claim 27, wherein the forming of the insulating cap layer comprises:

depositing a blanket layer of an insulating material over the recessed gate electrode layer and recessed pair of spacers; and

planarizing the insulating material layer to form the insulating cap layer.

30. The method of claim 27, wherein a height of the recessed pair of spacers is substantially the same as a height of the recessed gate electrode.

31. The method of claim 27, wherein the pair of spacers comprises silicon oxynitride (SiON), carbon-doped silicon oxynitride (SiOCN), or a low-k dielectric material.

32. A transistor comprising:

a substrate;

a pair of spacers on the substrate;

a gate dielectric layer on the substrate and between the pair of spacers;

a gate electrode layer having a stepped profile on the gate dielectric layer, wherein a middle portion of the gate electrode layer has a relatively larger height than side portions of the gate electrode layer;

an insulating cap layer on the gate electrode layer and between the pair of spacers; and

a pair of diffusion regions adjacent to the pair of spacers.

33. The transistor of claim 32, wherein the insulating cap layer comprises silicon nitride, silicon oxide, silicon carbide, silicon nitride doped with carbon, silicon oxynitride, or aluminum oxide.

34. The transistor of claim 32, wherein the insulating cap layer comprises a nitride material, a carbide material, an oxide material, a metal oxide material, or a low-k dielectric material.

35. The transistor of claim 32, wherein the insulating cap layer comprises boron nitride or boron carbide.

36. The transistor of claim 32, wherein the insulating cap layer comprises a low-k dielectric material doped with one or more of carbon, nitrogen, and hydrogen.

37. The transistor of claim 32, wherein the gate electrode comprises two metal layers, wherein a first metal layer comprises the middle portion of the gate electrode having the relatively larger height and a second metal layer comprises the side portions of the gate electrode.

38. A method of forming a transistor comprising:

forming a gate dielectric layer on a substrate;

forming a gate electrode layer on the gate dielectric layer;

forming a pair of spacers on opposing sides of the gate dielectric layer and the gate electrode layer;

forming a pair of diffusion regions adjacent to the pair of spacers;

removing the gate electrode layer and the gate dielectric layer, thereby forming a trench between the pair of spacers;

depositing a conformal first metal layer within the trench;

depositing a second metal layer on the first metal layer;

recessing the first and second metal layers, wherein the first metal layer is recessed to a larger extent than the second metal layer; and

forming an insulating cap layer on the recessed first and second metal layers.

39. The method of claim 38, wherein the recessing of the first and second metal layers comprises:

applying an etch chemistry to the first and second metal layers that is selective to the second metal layer.

40. The method of claim 38, wherein the recessing of the first and second metal layers comprises:

applying a first etch chemistry to recess the first metal layer; and

applying a second etch chemistry to recess the second metal layer,

wherein the first and second etch chemistries recess the first metal layer to a larger extent than the second metal layer.

41. The method of claim 40, wherein the second etch chemistry also recesses the first metal layer.

42. The method of claim 38, wherein the forming of the insulating cap layer comprises:

depositing a blanket layer of an insulating material over the recessed first and second metal layers; and

planarizing the insulating material layer to form the insulating cap layer.

43. The method of claim 38, wherein the insulating cap layer comprises silicon nitride, silicon oxide, silicon carbide, silicon nitride doped with carbon, silicon oxynitride, or aluminum oxide.

44. The method of claim 38, wherein the insulating cap layer comprises a nitride material, a carbide material, an oxide material, a metal oxide material, or a low-k dielectric material.

45. The method of claim 38, wherein the insulating cap layer comprises boron nitride or boron carbide.

46. The method of claim 38, wherein the insulating cap layer comprises a low-k dielectric material doped with one or more of carbon, nitrogen, and hydrogen.

47. A transistor comprising:

a substrate;

a pair of spacers on the substrate;

a gate dielectric layer on the substrate and between the pair of spacers;

a gate electrode layer having a stepped profile on the gate dielectric layer, wherein a middle portion of the gate electrode layer has a relatively larger height than side portions of the gate electrode layer;

an insulating cap layer sited atop the gate electrode layer that extends laterally over the top surfaces of the pair of spacers; and

a pair of diffusion regions adjacent to the pair of spacers.

48. The transistor of claim 47, wherein the insulating cap layer comprises silicon nitride, silicon oxide, silicon carbide, silicon nitride doped with carbon, silicon oxynitride, or aluminum oxide.

49. The transistor of claim 47, wherein the insulating cap layer comprises a nitride material, a carbide material, an oxide material, a metal oxide material, or a low-k dielectric material.

50. The transistor of claim 47, wherein the insulating cap layer comprises boron nitride or boron carbide.

51. The transistor of claim 47, wherein the insulating cap layer comprises a low-k dielectric material doped with one or more of carbon, nitrogen, and hydrogen.

52. The transistor of claim 47, wherein the gate electrode comprises two metal layers, wherein a first metal layer comprises the middle portion of the gate electrode having the relatively larger height and a second metal layer comprises the side portions of the gate electrode.

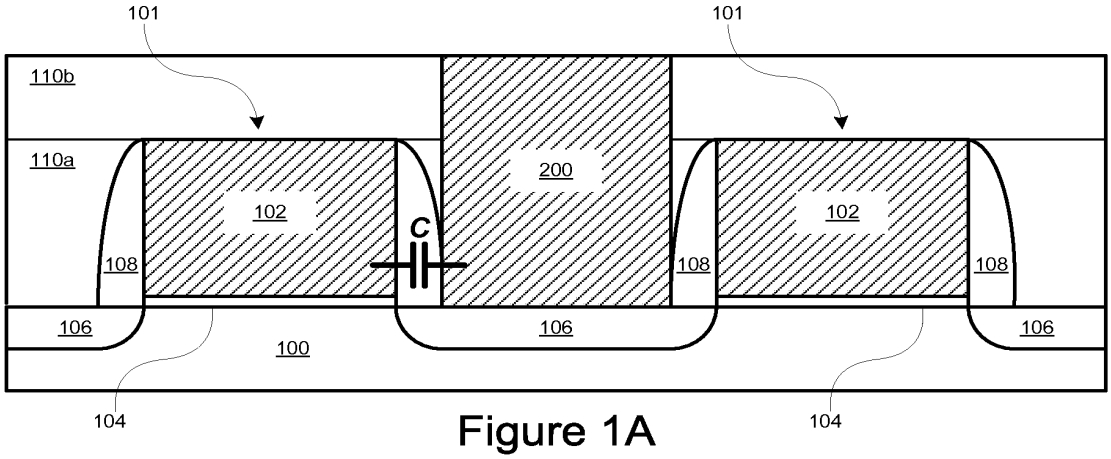


Figure 1A

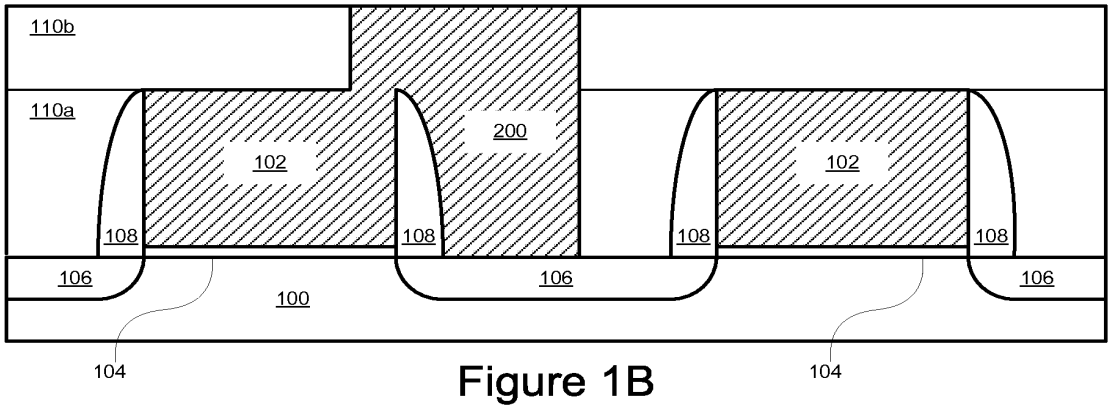


Figure 1B

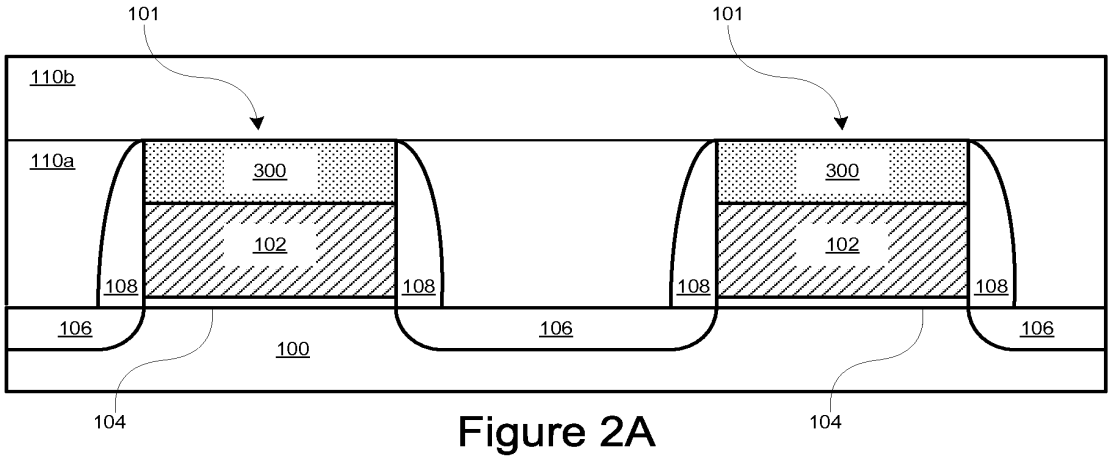


Figure 2A

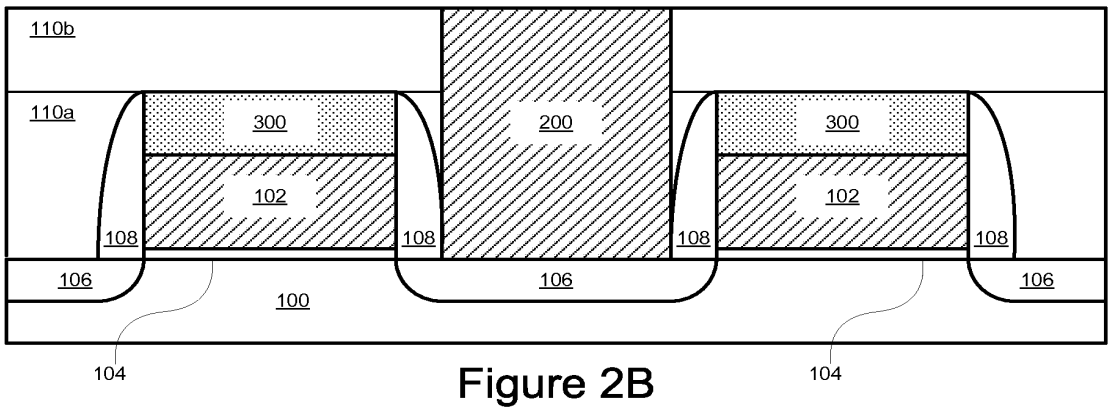


Figure 2B

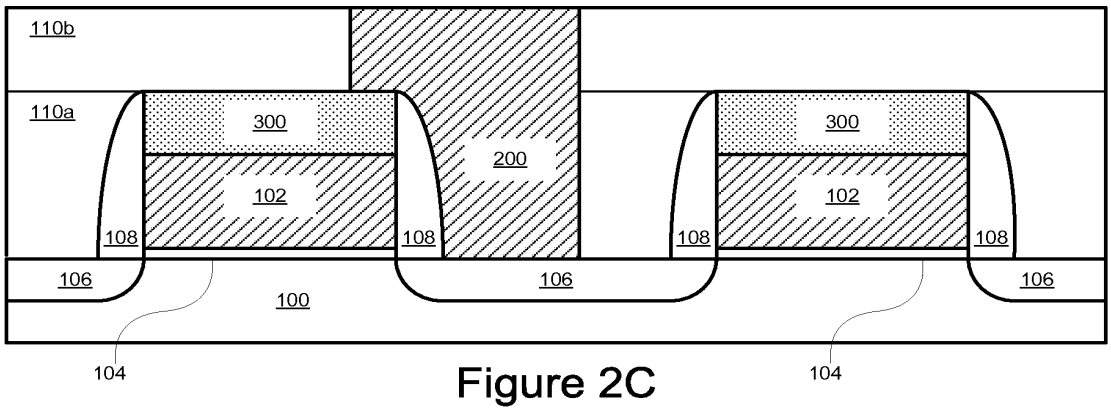


Figure 2C

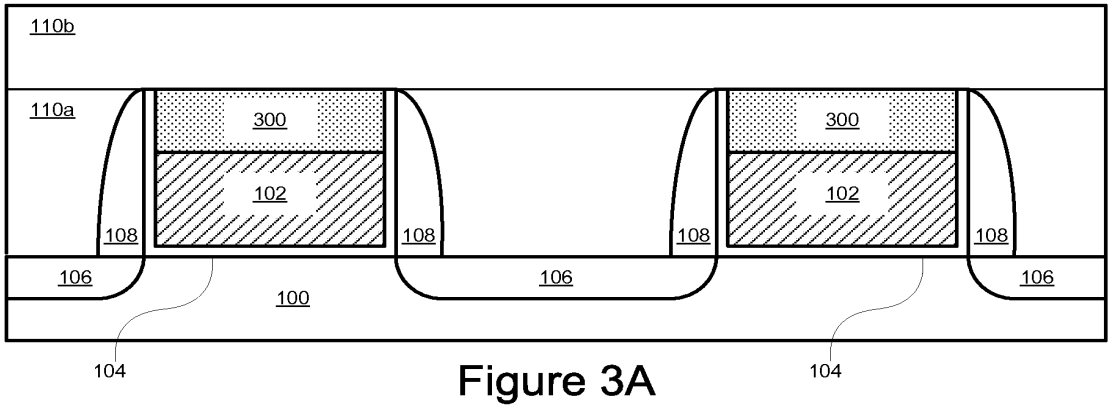


Figure 3A

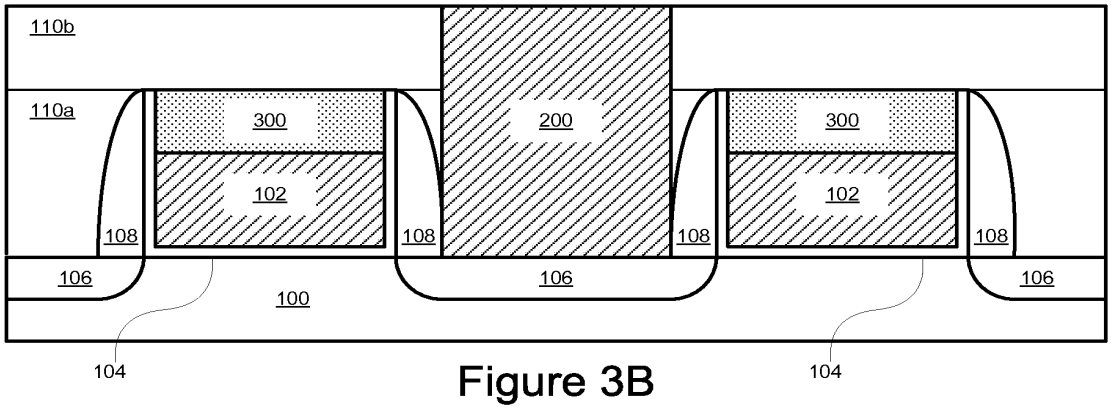


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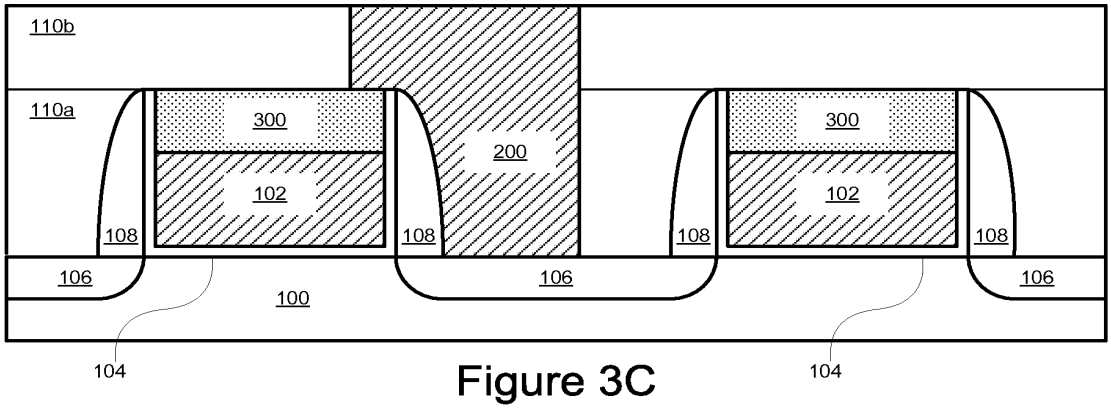


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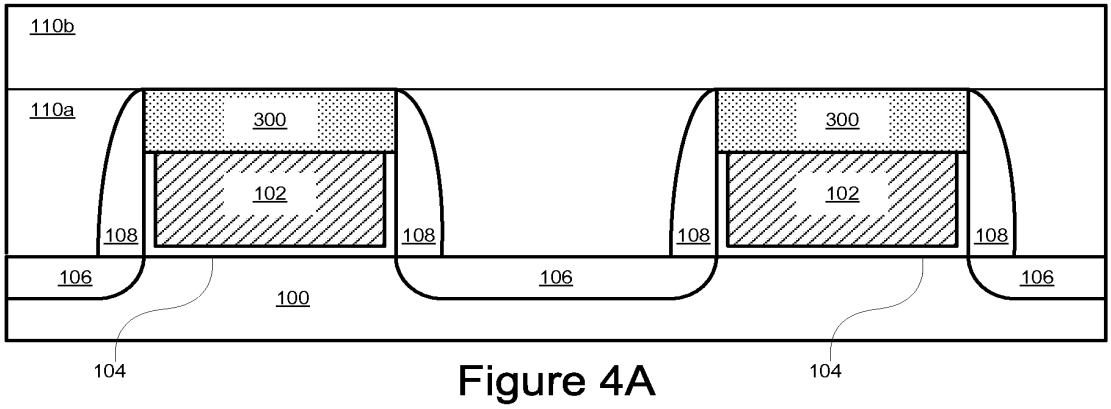


Figure 4A

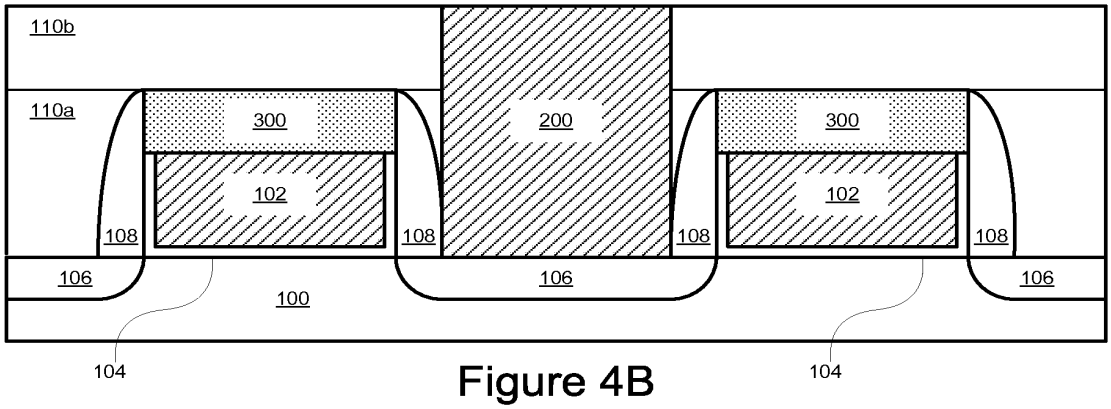


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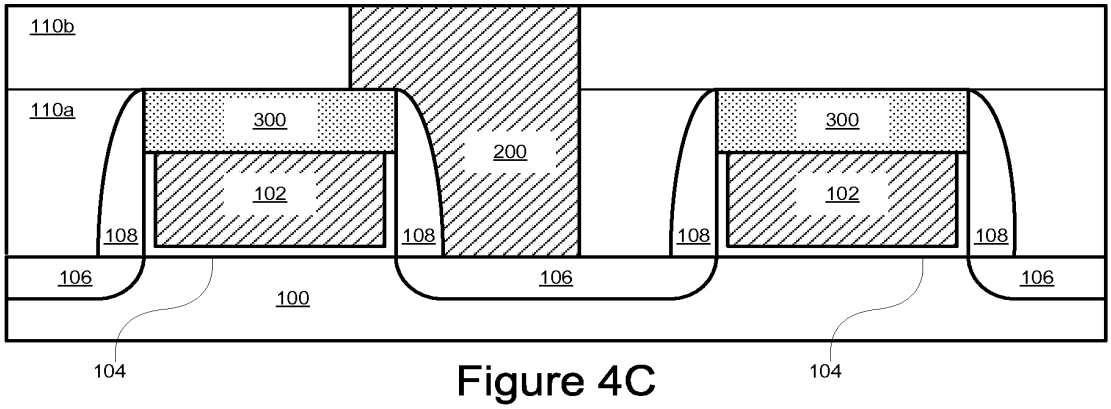


Figure 4C

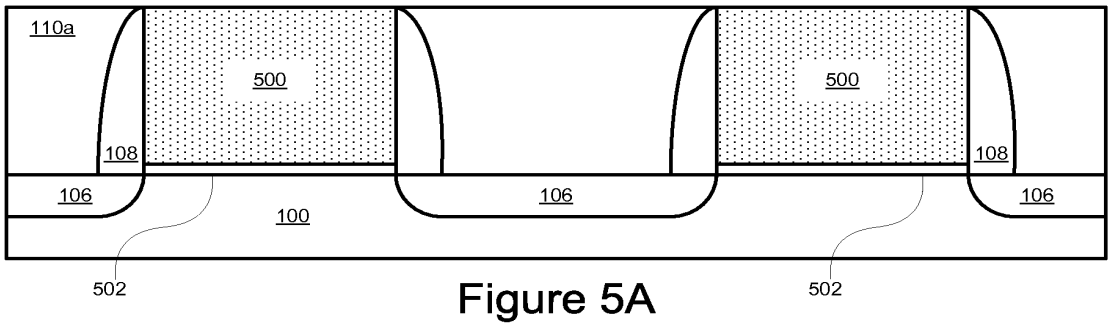


Figure 5A

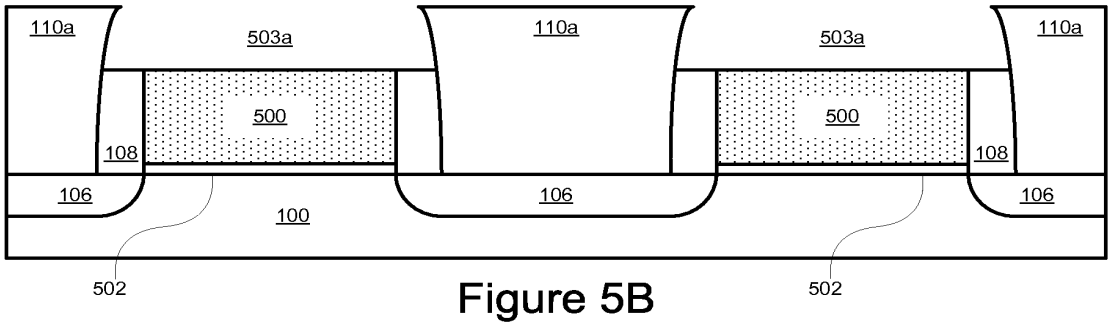


Figure 5B

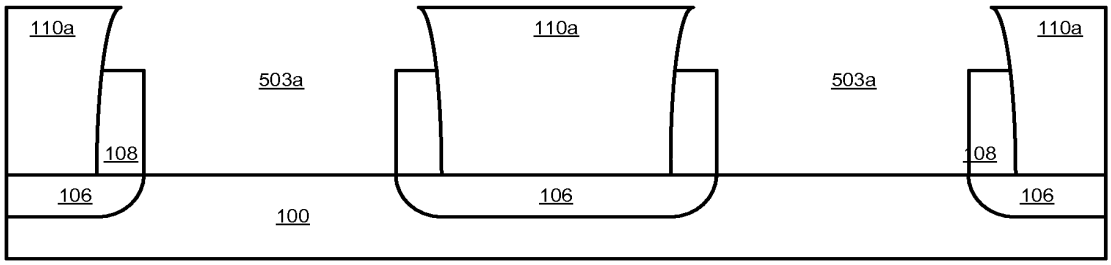


Figure 5C

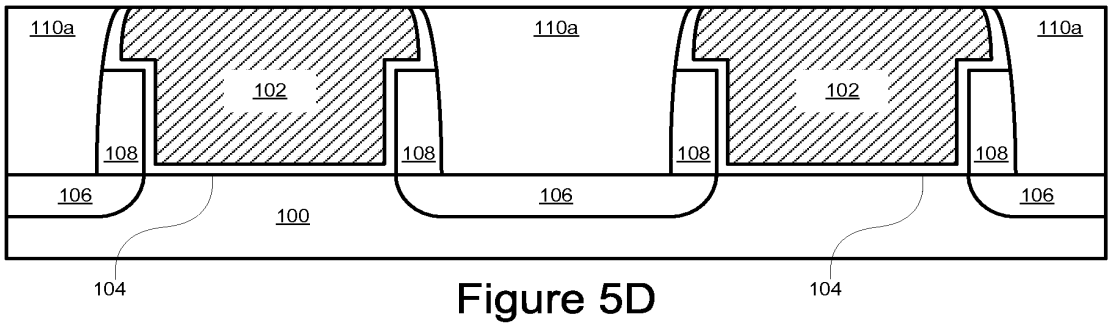


Figure 5D

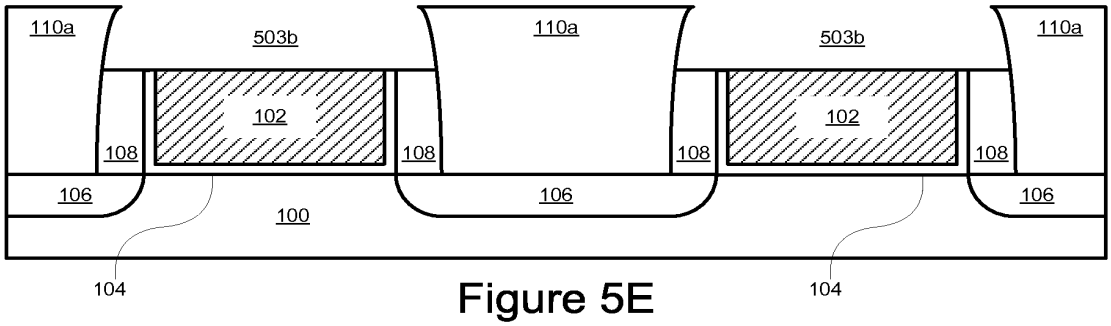


Figure 5E

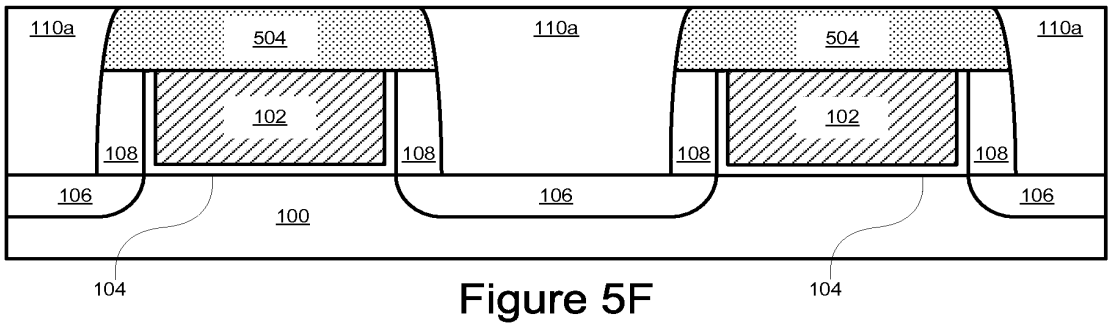


Figure 5F

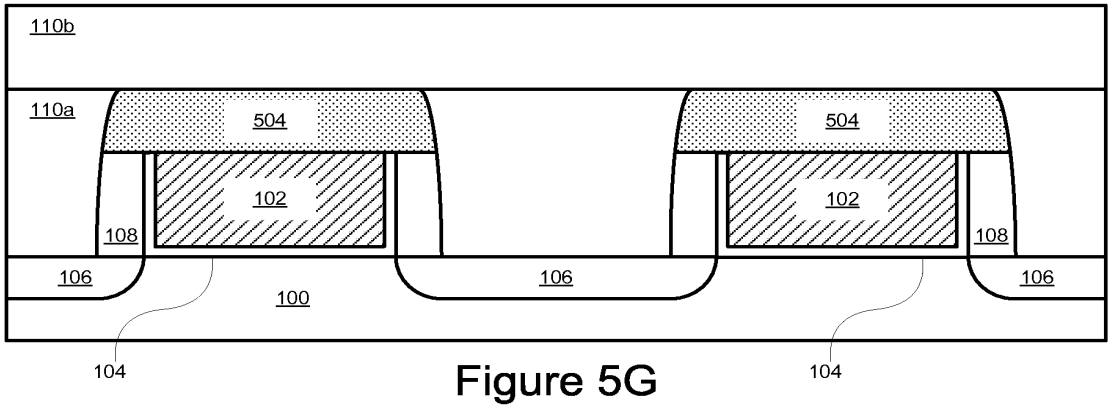


Figure 5G

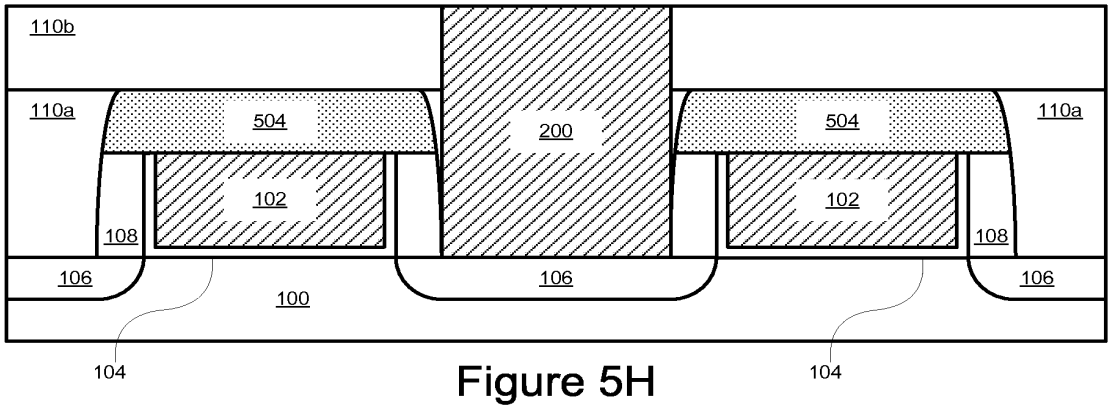


Figure 5H

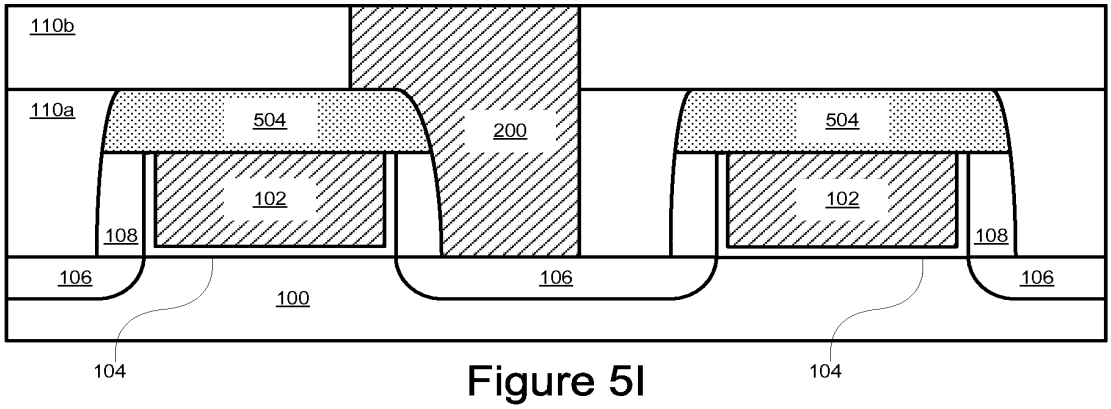


Figure 5I

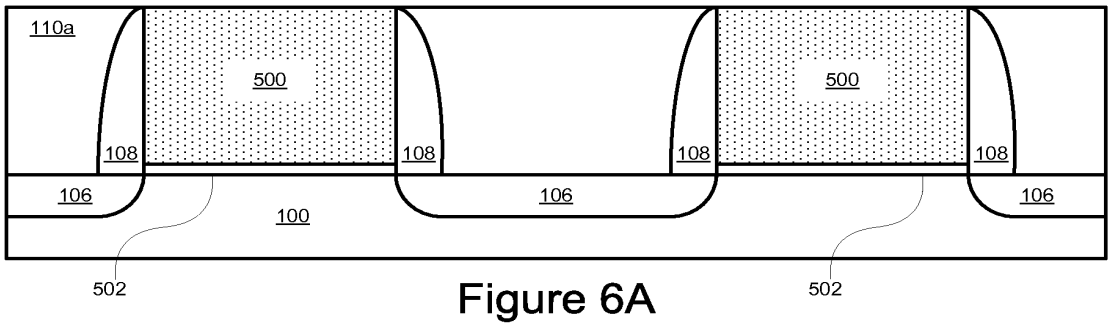


Figure 6A

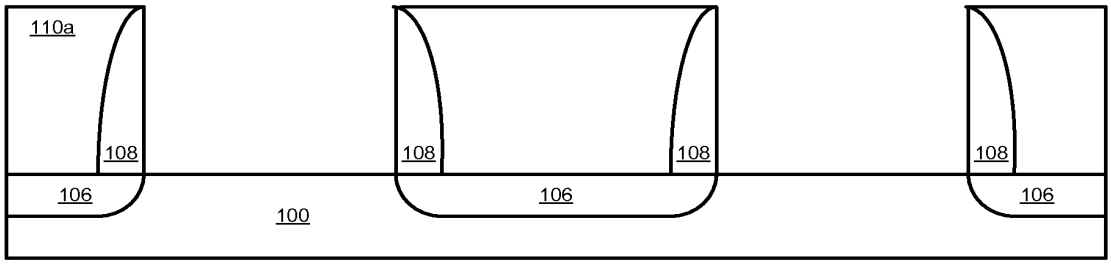


Figure 6B

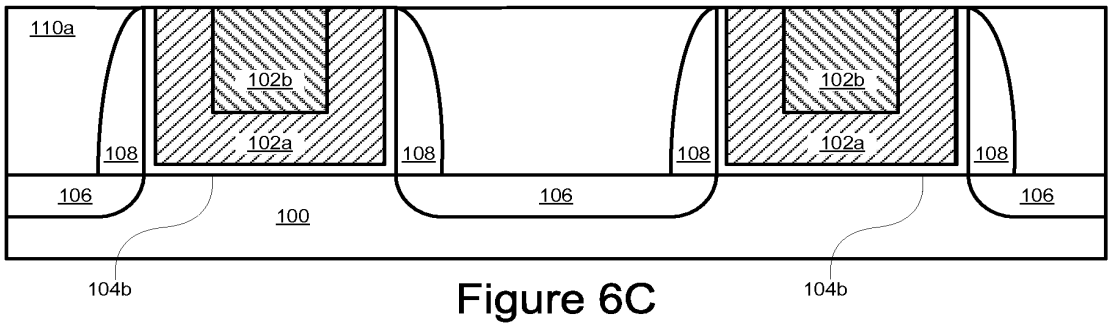


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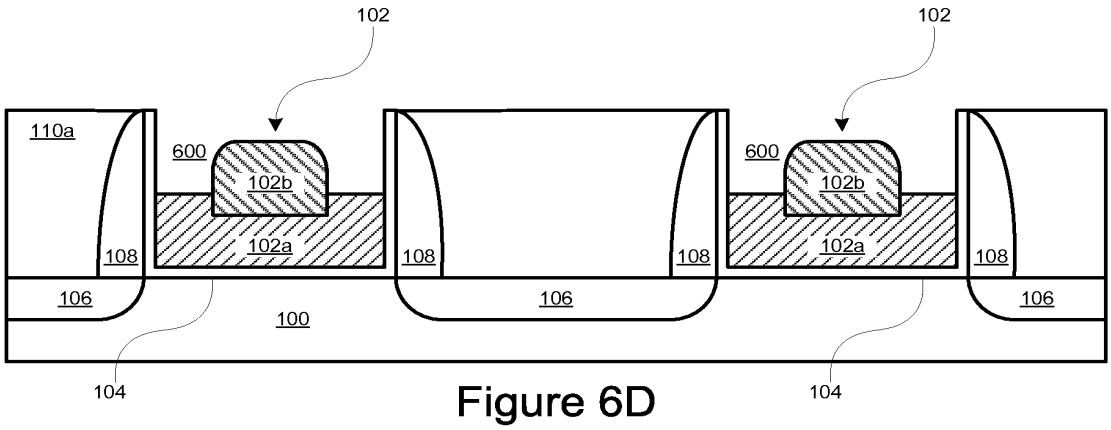


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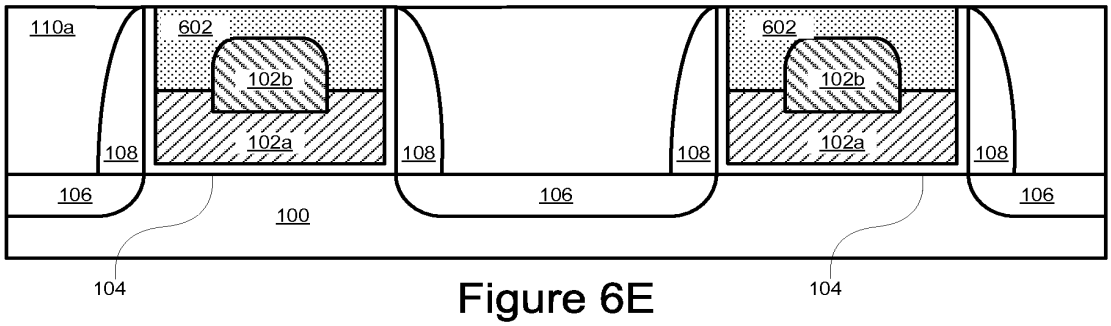


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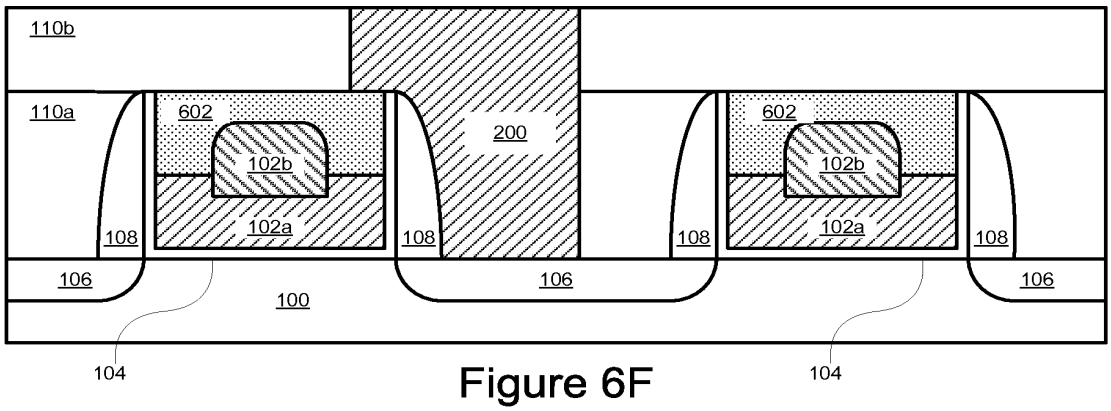


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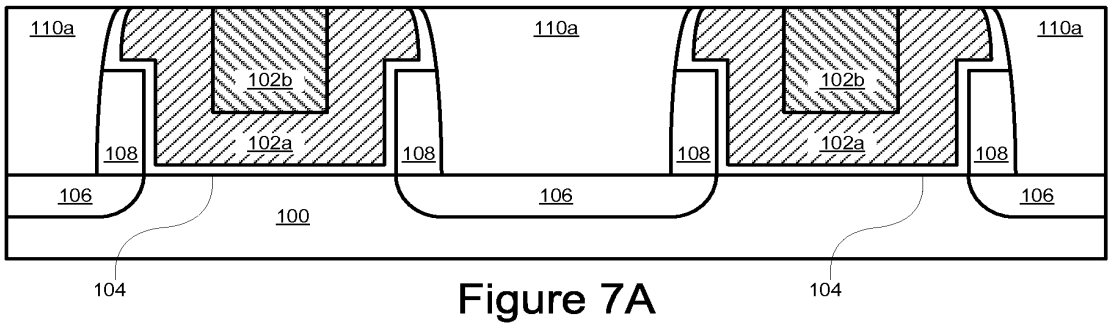


Figure 7A

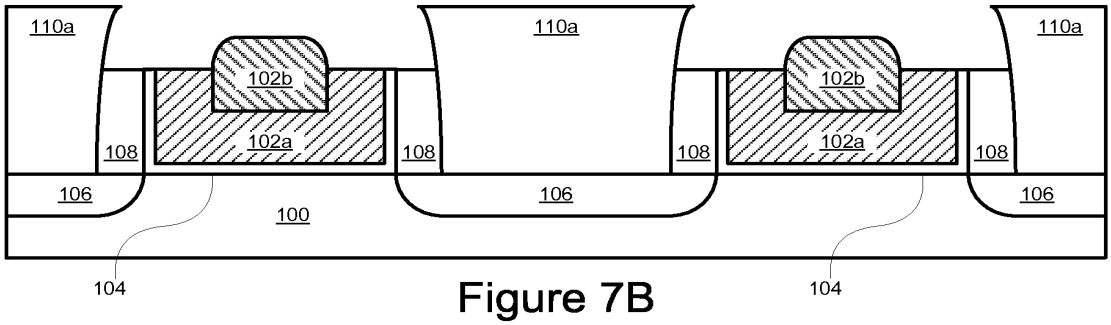


Figure 7B

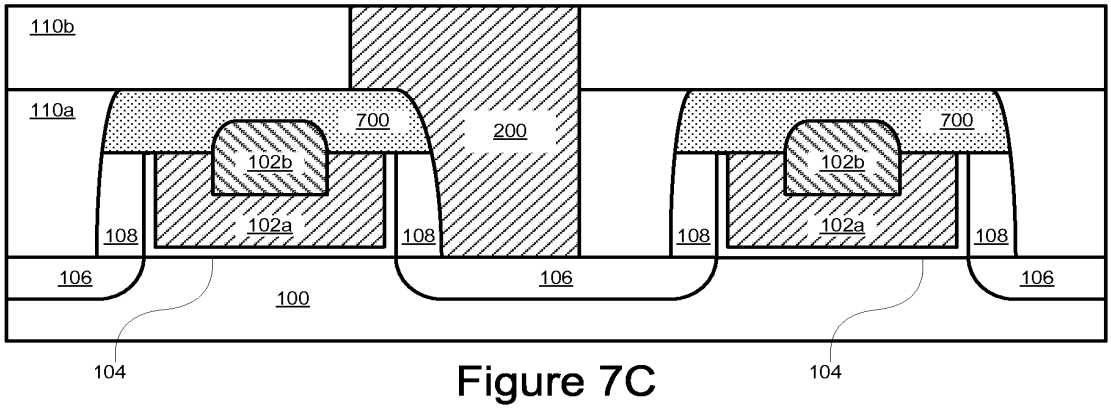


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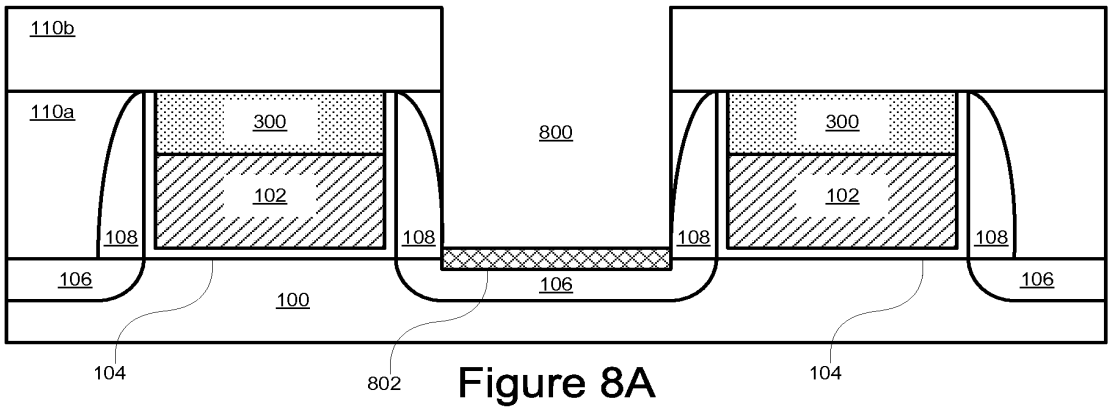


Figure 8A

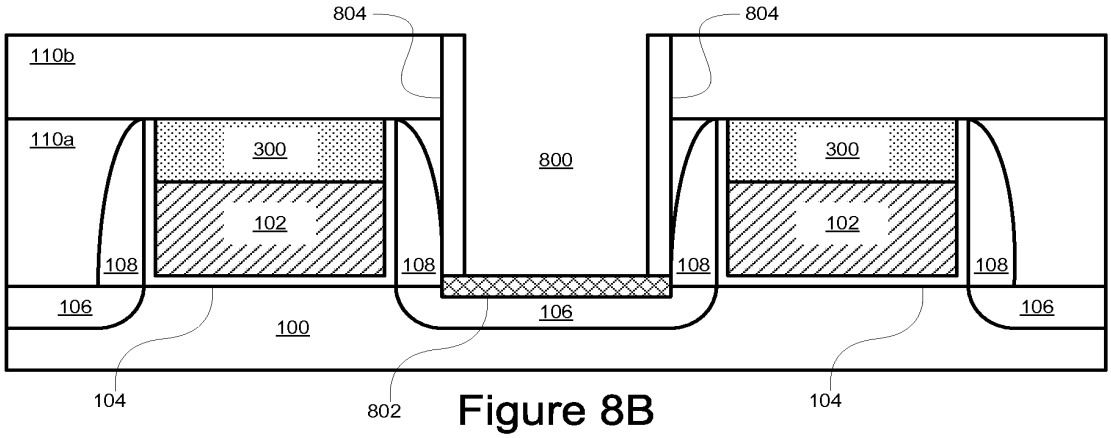


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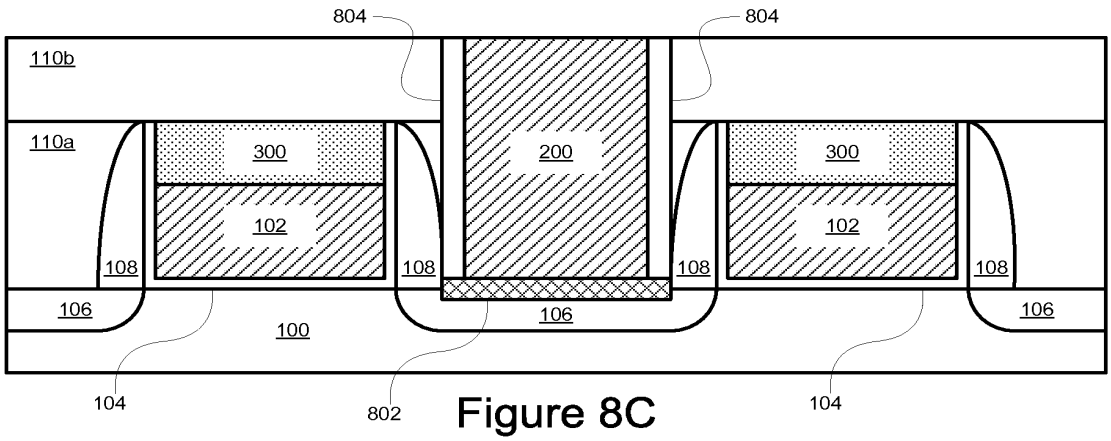


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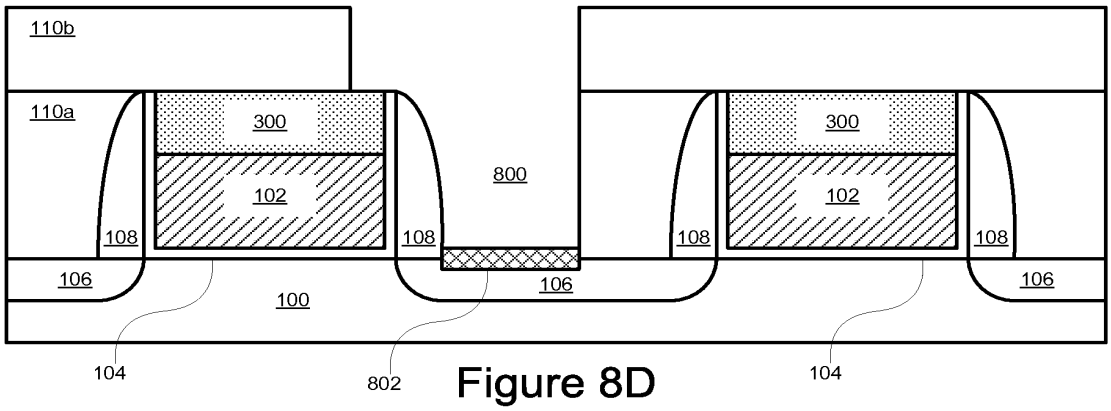


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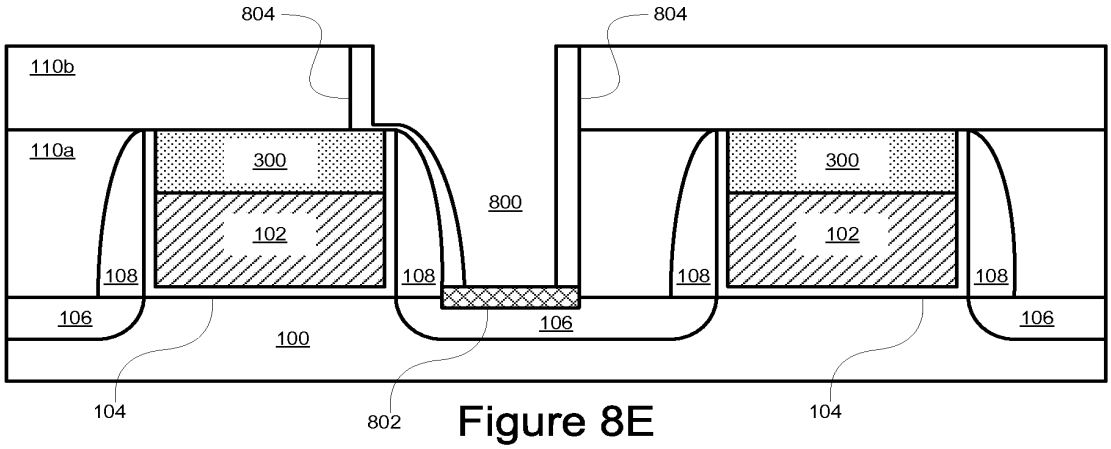


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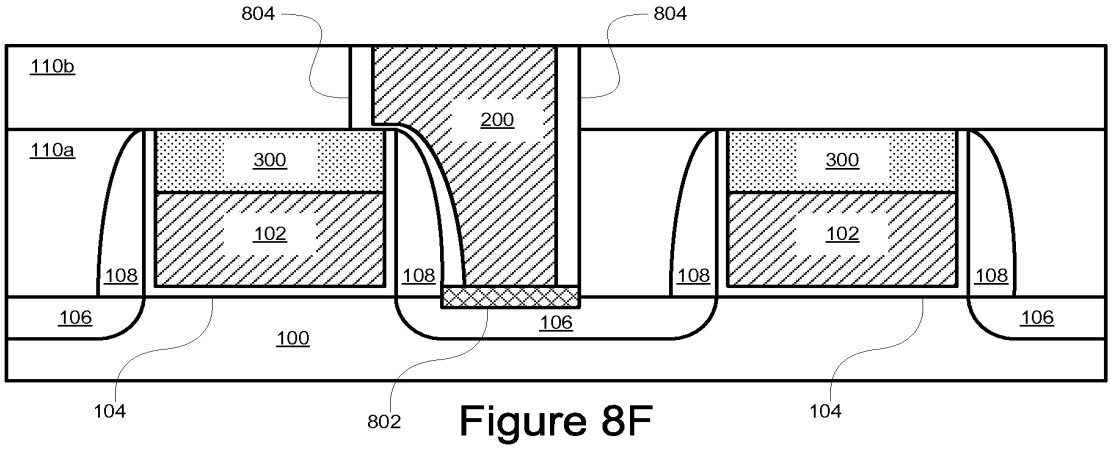


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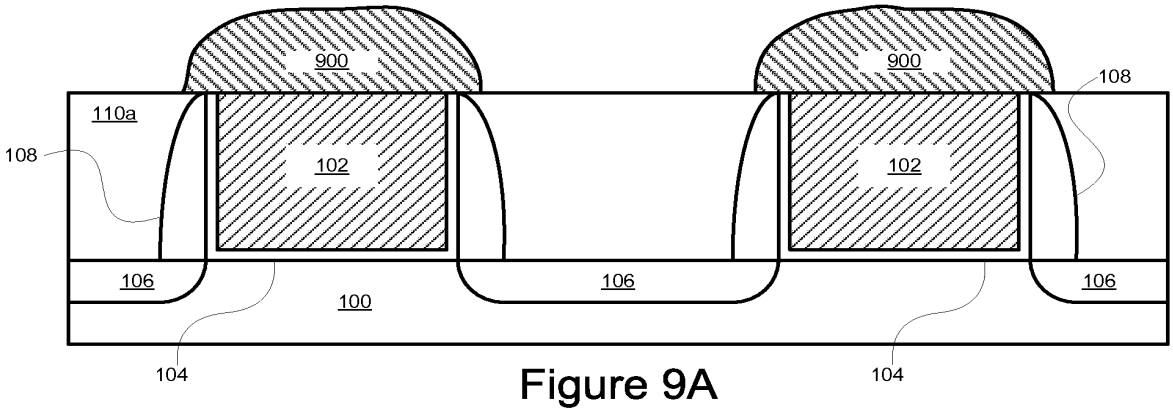


Figure 9A

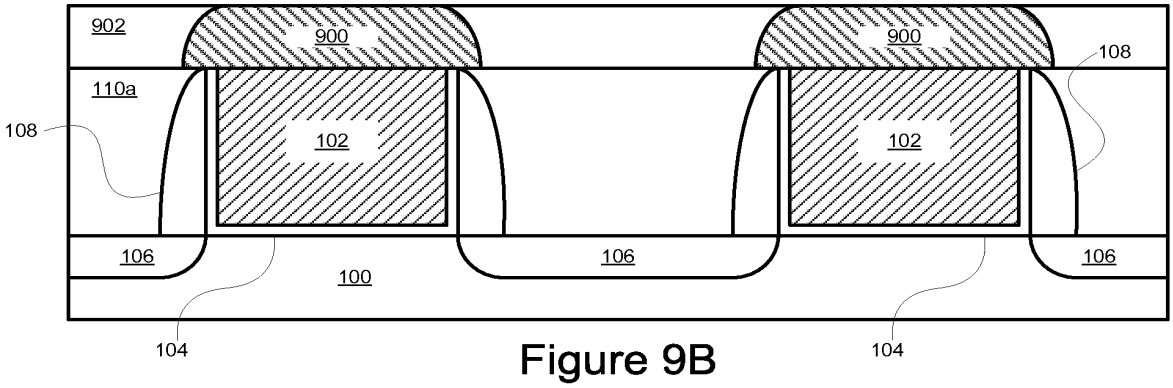


Figure 9B

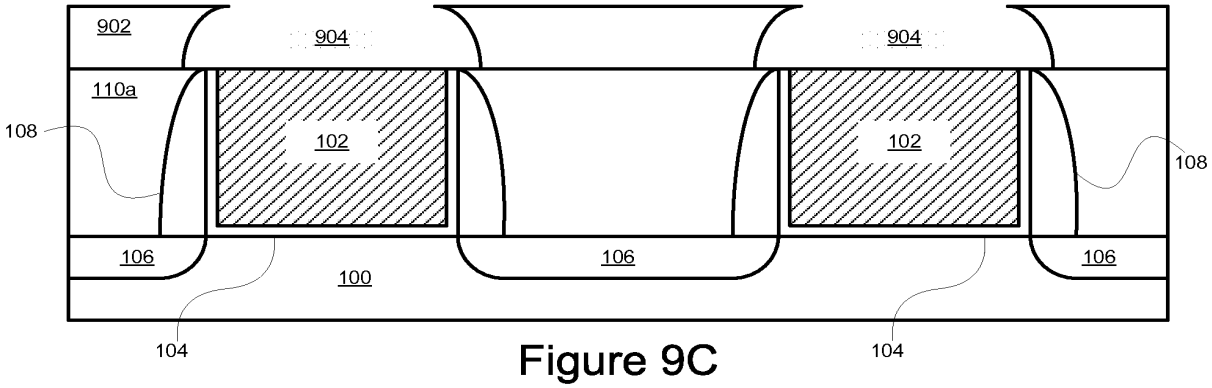


Figure 9C

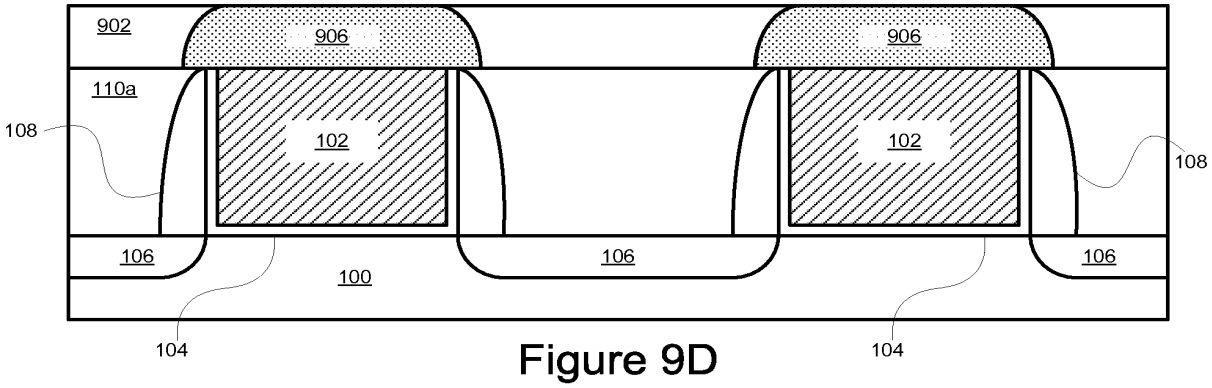


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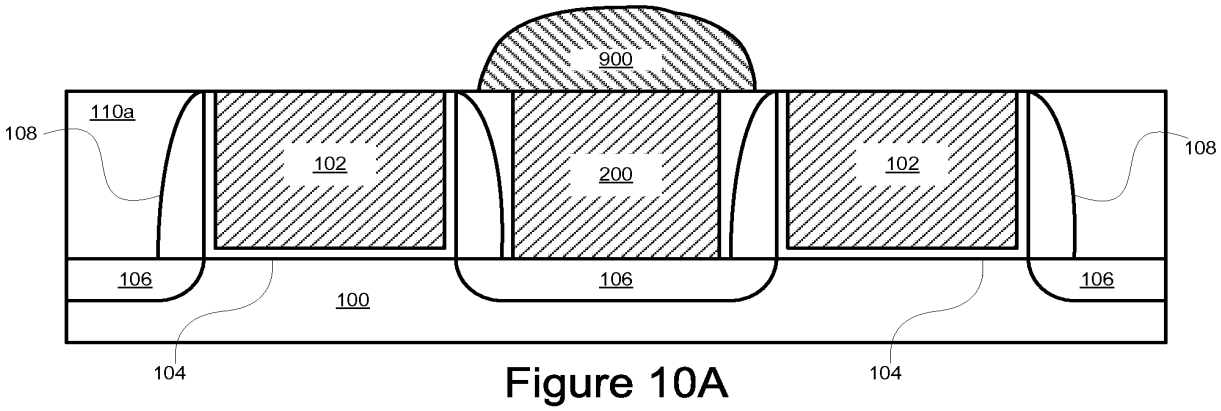


Figure 10A

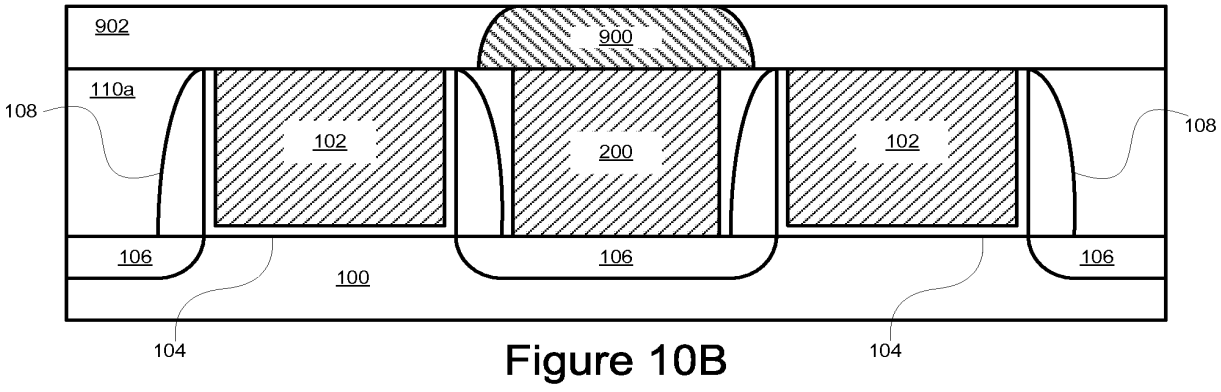


Figure 10B

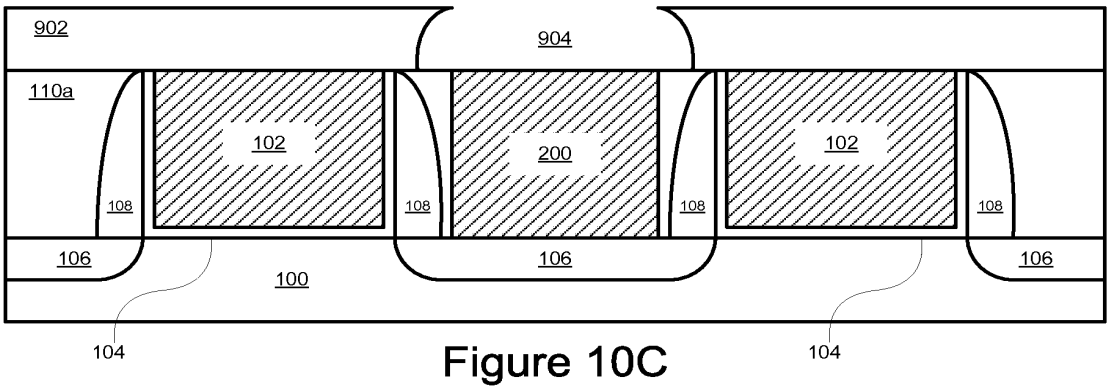


Figure 10C

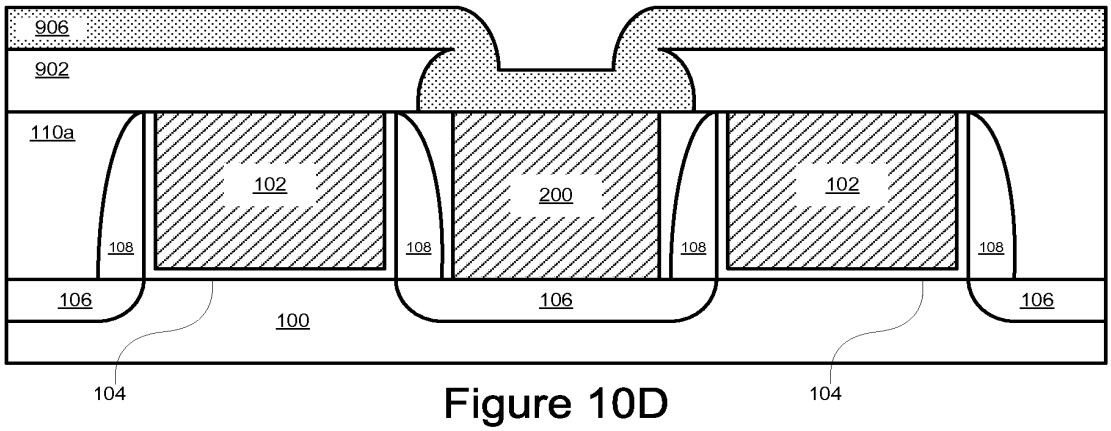


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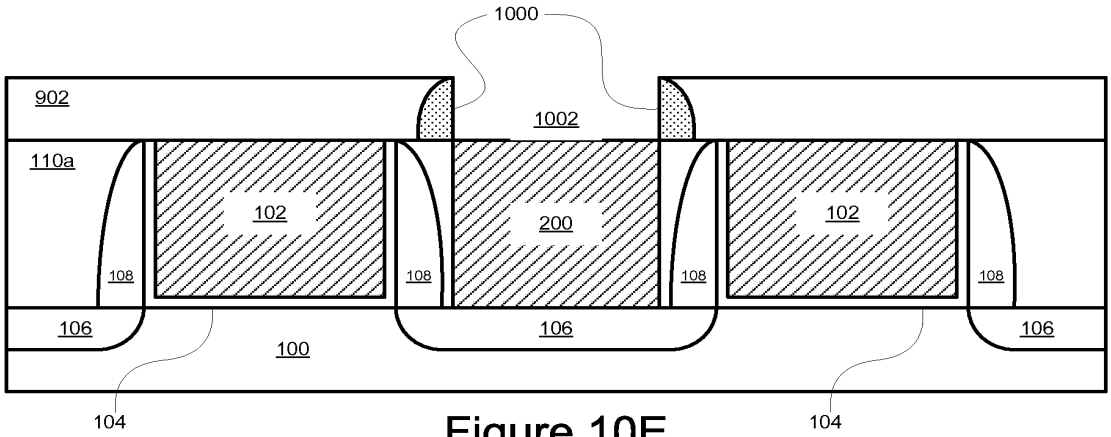


Figure 10E

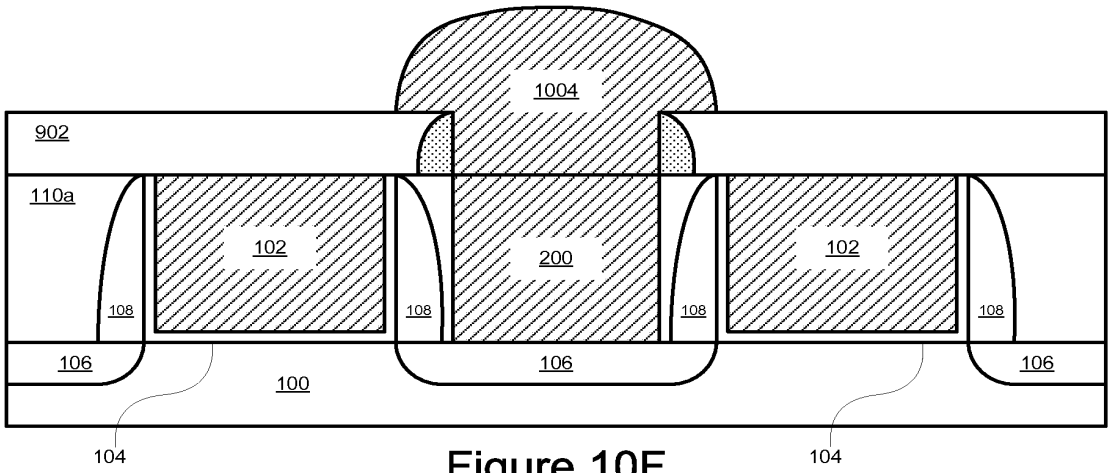


Figure 10F

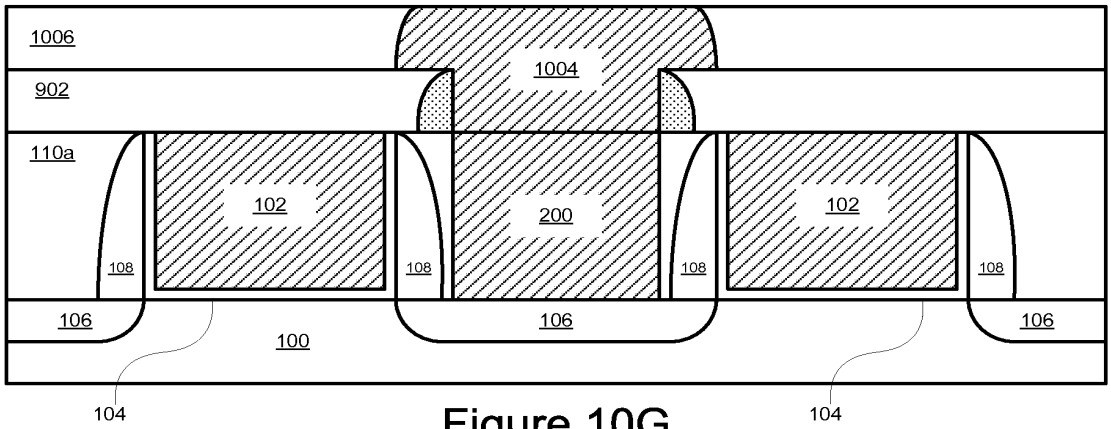


Figure 10G

Electronic Acknowledgement Receipt	
EFS ID:	21819320
Application Number:	13992598
International Application Number:	
Confirmation Number:	5215
Title of Invention:	CAPPING DIELECTRIC STRUCTURE FOR TRANSISTOR GATES
First Named Inventor/Applicant Name:	Aaron W. Rosenbaum
Customer Number:	92265
Filer:	Robert G. Winkle/Brittany McCloud
Filer Authorized By:	Robert G. Winkle
Attorney Docket Number:	P38683US
Receipt Date:	19-MAR-2015
Filing Date:	07-JUN-2013
Time Stamp:	14:52:38
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	P38683US_IDS.pdf	612523 ae81687b5b805166b378cfeb3f5541ba60a7f20a	no	4

Warnings:
Information:

2	Foreign Reference	FR1.pdf	1122220 ffedb29841efe14b18046457225e71669b8e83c9	no	10
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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/992,598	06/07/2013	Aaron W. Rosenbaum	P38683US	5215

92265 7590 04/21/2015

Winkle, PLLC
c/o CPA Global
P.O. Box 52050
Minneapolis, MN 55402

EXAMINER	
LAIR, SAMUEL L	

ART UNIT	PAPER NUMBER
2817	

NOTIFICATION DATE	DELIVERY MODE
04/21/2015	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

winkle@cableone.net
inteldocs@cpaglobal.com

Office Action Summary	Application No. 13/992,598	Applicant(s) ROSENBAUM ET AL.	
	Examiner SAMUEL LAIR	Art Unit 2817	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 March 2015*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☒ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-25* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☒ Claim(s) *15-25* is/are allowed.

7)☒ Claim(s) *1-14* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *7 June 2013* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date *See Continuation Sheet*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

Continuation of Attachment(s) 2). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :10/23/2013, 07/22/2014, 10/16/2014, 03/19/2015.

1. The present application is being examined under the pre-AIA first to invent provisions.

2. Claims 1-14 are rejected. Claims 15-25 are allowed.

DETAILED ACTION

Claim Rejections - 35 USC § 112

3. The following is a quotation of 35 U.S.C. 112(b):

> (b) CONCLUSION.—The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention.

The following is a quotation of 35 U.S.C. 112 (pre-AIA), second paragraph:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 10-14 are rejected under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor, or for pre-AIA the applicant regards as the invention.

5. Regarding claim 10, said claim is indefinite because “the recessed gate electrode” recited in lines 4 & 5 lack proper antecedent basis.

6. Regarding claim 11-14, said claims depend on claim 10 and, therefore, inherit the deficiencies of claim 10.

Claim Rejections - 35 USC § 102

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under

the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1, 2, 4-6, 8 and 9 are rejected under pre-AIA 35 U.S.C. 102(b) as being anticipated by Liaw, US 2006/0046449 A1.

8. Regarding claim 1, Liaw discloses a transistor gate, comprising:

a pair of gate spacers (FIG. 3B; ELMT. 314; PARA. 0020)

a recessed gate electrode disposed between the pair of gate spacers (FIG. 3B; ELMT. 308; PARA. 0020; Gate electrode 308 is recessed into the space between spacers 314.); and

a substantially void free capping dielectric structure disposed adjacent the recessed gate electrode and between the pair of gate spacers (FIG. 3B; ELMT. 312; PARA. 0020), as claimed.

9. Regarding claim 2, Liaw further discloses wherein the substantially void free capping dielectric structure comprises silicon nitride (PARA. 0019), as claimed.

10. Regarding claim 4, Liaw further discloses wherein the recessed gate electrode is a non-planar gate electrode (PARA. 0029 discloses that Liaw's device can be constructed as a finFET.), as claimed.

11. Regarding claim 5, Liaw discloses a microelectronic device, comprising:

a non-planar transistor gate over a non-planar transistor fin (PARA. 0029 discloses that Liaw's device can be constructed as a finFET.), wherein the non-planar transistor gate comprises a gate electrode (FIG. 3B; ELMT. 308; PARA. 0020) recessed between a pair of gate spacers (FIG. 3B;

ELMT. 314; PARA. 0020) and a substantially void free capping dielectric structure disposed on the recessed gate electrode between the gate spacers (FIG. 3B; ELMT. 312; PARA. 0020);

a source/drain region (FIG. 3B; ELMT. 318; PARA. 0021);

at least one dielectric material layer over the source/drain region, the non-planar transistor gate spacers, and the substantially void free capping dielectric structure (FIGS. 3A & 3B; ELMT. 320; PARA. 0021); and

a source/drain contact extending through a portion of the at least one dielectric material layer to contact the source/drain region (FIG. 3B; ELMT. 328; PARA. 0024), as claimed.

12. Regarding claim 6, Liaw further discloses wherein the substantially void free capping dielectric structure comprises silicon nitride (PARA. 0019), as claimed.

13. Regarding claim 8, Liaw further discloses wherein the source/drain contact abuts at least a portion of one non-planar transistor gate spacer (see FIG. 3B; ELMTS. 328 & 314), as claimed.

14. Regarding claim 9, Liaw further discloses wherein the source/drain contact abuts at least a portion of the capping dielectric structure (see FIG. 3B; ELMTS. 328 & 312), as claimed.

15. Claims 1, 3-5, 7-9 are rejected under pre-AIA 35 U.S.C. 102(e) as being anticipated by Bohr et al., US 2011/0156107 A1.

16. Regarding claim 1, Bohr discloses a transistor gate, comprising:

a pair of gate spacers (FIG. 2C; ELMT. 108; PARA. 0026)

a recessed gate electrode disposed between the pair of gate spacers (FIG. 2C; ELMT. 102; PARA. 0026; Gate electrode 102 is recessed into the space between spacers 108.); and

a substantially void free capping dielectric structure disposed adjacent the recessed gate electrode and between the pair of gate spacers (FIG. 2C; ELMT. 300; PARA. 0080), as claimed.

17. Regarding claim 3, Bohr further discloses wherein the substantially void free capping dielectric structure comprises silicon carbide (PARA. 0031), as claimed.

18. Regarding claim 4, Bohr further discloses wherein the recessed gate electrode is a non-planar gate electrode (PARA. 0028 discloses that Bohr's device can be constructed as a finFET.), as claimed.

19. Regarding claim 5, Bohr discloses a microelectronic device, comprising:

a non-planar transistor gate over a non-planar transistor fin (PARA. 0028 discloses that Bohr's device can be constructed as a finFET.), wherein the non-planar transistor gate comprises a gate electrode (FIG. 2C; ELMT. 102; PARA. 0026) recessed between a pair of gate spacers (FIG. 2C; ELMT. 108; PARA. 0026) and a substantially void free capping dielectric structure disposed on the recessed gate electrode between the gate spacers (FIG. 2C; ELMT. 300; PARA. 0080);

a source/drain region (FIG. 2C; ELMT. 106; PARA. 0033);

at least one dielectric material layer over the source/drain region, the non-planar transistor gate spacers, and the substantially void free capping dielectric structure (FIG. 2C; ELMTS. 110a & 110b; PARA. 0019); and

a source/drain contact extending through a portion of the at least one dielectric material layer to contact the source/drain region (FIG. 2C; ELMT. 200; PARA. 0020), as claimed.

20. Regarding claim 7, Bohr further discloses wherein the substantially void free capping dielectric structure comprises silicon carbide (PARA. 0031), as claimed.

21. Regarding claim 8, Bohr further discloses wherein the source/drain contact abuts at least a portion of one non-planar transistor gate spacer (see FIG. 2C; ELMTS. 200 & 108), as claimed.

22. Regarding claim 9, Bohr further discloses wherein the source/drain contact abuts at least a portion of the capping dielectric structure (see FIG. 2C; ELMTS. 200 & 300), as claimed.

Claim Rejections - 35 USC § 103

23. The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

24. Claims 10-14 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Bohr in view of Sunayama et al., US 2011/0034026 A1.

25. Regarding claim 10, Bohr discloses a method of fabricating a transistor gate, comprising:

forming a pair of gate spacers (Bohr; FIG. 2C; ELMT. 108; PARA. 0026);

forming a gate electrode disposed between the pair of gate spacers (Bohr; FIG. 2C; ELMT. 102; PARA. 0026;); and

forming a capping dielectric structure on a top surface of the recessed gate electrode and between the pair of gate spacers (Bohr; FIG. 2C; ELMT. 300; PARA. 0080; Gate electrode 102 is recessed into the space between spacers 108.), as claimed.

26. However, Bohr does not disclose wherein the capping dielectric structure is formed by high density plasma depositing, as claimed. However, Bohr discloses that his capping layer can be formed of silicon carbide or silicon nitride (Bohr; PARA. 0031). Sunayama teaches a method of fabricating a layer of silicon carbide or silicon nitride using PECVD (Sunayama PARA. 0059). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Bohr wherein the capping dielectric structure is formed by high density plasma depositing, as claimed, in order to form the capping layer of Bohr using a known method taught by Sunayama (see Bohr PARA. 0031 and Sunayama PARA. 0059).

27. Regarding claim 11, Bohr in the combination further discloses wherein high density plasma depositing the capping dielectric structure comprises high density plasma depositing a silicon nitride capping dielectric structure (see Bohr PARA. 0031), as claimed.

28. Regarding claim 12, Bohr in the combination further discloses wherein high density plasma depositing the capping dielectric structure comprises high density plasma depositing a silicon carbide capping dielectric structure (see Bohr PARA. 0031), as claimed.

29. Regarding claim 13, Sunayama in the combination further discloses wherein high density plasma depositing the capping dielectric structure comprises high density plasma depositing the capping dielectric structure at a temperature between about 300 ˚C and 600 ˚C.

30. Regarding claim 14, Bohr in the combination further discloses wherein forming the gate electrode comprises forming a non-planar gate electrode (PARA. 0028 discloses that Bohr's device can be constructed as a finFET.), as claimed.

Allowable Subject Matter

31. Claims 15-25 are allowed.

32. The following is an examiner's statement of reasons for allowance:

33. Claim 15 is allowable because the prior art of record fails to anticipate or render obvious all limitations of said claim. Liaw, US 2006/046449 A1, Bohr et al., US 2011/0156107 A1, and Lee et al., US 2005/0019993 A1, are the prior art references of record that most resemble the claimed invention. However, none of these references disclose all of the process steps recited in claim 15 and it is not obvious in light of the prior art of record to modify any prior art reference to include all of the process steps recited in claim 15.

34. Claims 16-25 depend on claim 15 and are, therefore, allowable as well.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

35. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

a. US 2009/0321841 A1

b. US 2012/0001266 A1

c. US 2012/0313170 A1

d. US 2013/0065371 A1

e. US 2013/0062669 A1

f. US Patent 5,399,415

g. US 6,331,481 B1

h. US 2010/0032728 A1

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SAMUEL LAIR whose telephone number is (571)272-5714. The examiner can normally be reached on Wednesday to Saturday, 11:00 AM - 9:30 PM EDT.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eva Montalvo can be reached on (571)270-3829. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/ANTHONY HO/
Primary Examiner, Art Unit 2817

/SAMUEL LAIR/
Examiner, Art Unit 2817

Notice of References Cited	Application/Control No. 13/992,598	Applicant(s)/Patent Under Reexamination ROSENBAUM ET AL.	
	Examiner SAMUEL LAIR	Art Unit 2817	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2011/0034026 A1	02-2011	Sunayama et al.	438/653
*	B	US-2009/0321841 A1	12-2009	Hoentschel et al.	257/369
*	C	US-2012/0001266 A1	01-2012	Lim et al.	257/369
*	D	US-2012/0313170 A1	12-2012	Chang et al.	257/347
*	E	US-2013/0065371 A1	03-2013	Wei et al.	438/294
*	F	US-2013/0062669 A1	03-2013	Chen et al.	257/288
*	G	US-5,399,415	03-1995	Chen et al.	428/209
*	H	US-6,331,481 B1	12-2001	Stamper et al.	438/626
*	I	US-2010/0032728 A1	02-2010	HAO et al.	257/262
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
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	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	13992598
Filing Date	2013-06-07
First Named Inventor	Aaron W. Rosenbaum
Art Unit	2817
Examiner Name	Samuel L. Lair
Attorney Docket Number	P38683US

U.S.PATENTS

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

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U.S.PATENT APPLICATION PUBLICATIONS

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20050019993	A1	2005-01-27	Lee, et al.	
	2	20060046449	A1	2006-03-02	Liaw, Jhon-Jhy	
	3	20060088967	A1	2006-04-27	Hsiao, et al.	
	4	20060099783	A1	2006-05-11	Gluschenkov, et al.	
	5	20070111435	A1	2007-05-17	Kim, et al.	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.L.L.

Receipt date: 10/16/2014	Application Number	13992598	13992598 - GAU: 2817
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Filing Date	2013-06-07	
	First Named Inventor	Aaron W. Rosenbaum	
	Art Unit	2817	
	Examiner Name	Samuel L. Lair	
	Attorney Docket Number	P38683US	

	6	20080001187	A1	2008-01-03	Booth, et al.	
	7	20080014710	A1	2008-01-17	Bian, et al.	
	8	20100105215	A1	2010-04-29	Sugawara, et al.	
	9	20100155842	A1	2010-06-24	Anderson, et al.	
	10	20110147812	A1	2011-06-23	Steigerwald, et al.	
	11	20110156107	A1	2011-06-30	Bohr, et al.	
	12	20110272739	A1	2011-11-10	Lee, et al.	

If you wish to add additional U.S. Published Application citation information please click the Add button.

FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2]	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							☐

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NON-PATENT LITERATURE DOCUMENTS

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.L.L.

Receipt date: 10/16/2014	Application Number	13992598 13992598 - GAU: 2817
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Filing Date	2013-06-07
	First Named Inventor	Aaron W. Rosenbaum
	Art Unit	2817
	Examiner Name	Samuel L. Lair
	Attorney Docket Number	P38683US

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	Office Action received for Taiwan Patent Application No. 101133821, mailed on August 6, 2014, 9 pages of English Translation and 9 pages of Taiwan Office Action.	☒

If you wish to add additional non-patent literature document citation information please click the Add button

EXAMINER SIGNATURE

Examiner Signature	/Samuel Lair/	Date Considered	04/14/2015

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.L.L.

Receipt date: 10/16/2014	Application Number	13992598	13992598 - GAU: 2817
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Filing Date	2013-06-07	
	First Named Inventor	Aaron W. Rosenbaum	
	Art Unit	2817	
	Examiner Name	Samuel L. Lair	
	Attorney Docket Number	P38683US	

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Robert G. Winkle/	Date (YYYY-MM-DD)	2014-10-16
Name/Print	Robert G. Winkle	Registration Number	37,474

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.L.L.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.L.L.

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L15	2	US-20110147812-$.did.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/14 16:58
L16	16	(aaron near2 rosenbaum).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/14 17:04
L17	6	(mei near3 din near3 how).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/14 17:04
L18	49	(pradhan near2 sameer).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/14 17:05
L19	61	L16 or L17 or L18	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/14 17:05
L20	27	L19 and (H01L21/$.cpc. \| H01L29/$.cpc. | "257"/$.ccls. \| "438"/$.ccls.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/14 17:06
L21	27	(jean near2 luce).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/14 17:08
L22	0	L21 and (H01L21/$.cpc. \| H01L29/$.cpc. | "257"/$.ccls. \| "438"/$.ccls.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/14 17:09
L23	9	(jeanne near2 luce).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/14 17:09

L24	5	L23 and (H01L21/$.cpc. \| H01L29/$.cpc. | "257"/$.ccls. \| "438"/$.ccls.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/14 17:09
L26	2	US-20060046449-$.did.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/14 17:27
L27	2	US-20110156107-$.did.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/14 17:30
L28	2	US-20050019993-$.did.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/14 18:42
L29	2	US-20060099783-$.did.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/14 18:46
L30	593	((high near5 density near5 plasma) or PECVD or HDP or (ionized near5 physical near5 vapor) or IPVD or (I near3 PVD) or (plasma near3 enhanc$5)) same (SiC or silicon near3 carbide) same cap$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/14 19:16
L33	304	L30 and (fin or finFET or CMOS or PMOS or NMOS or MOS)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/14 19:29
L36	9	(((high near5 density near5 plasma) or PECVD or HDP or (ionized near5 physical near5 vapor) or IPVD or (I near3 PVD) or (plasma near3 enhanc$5)) same (SiC or silicon near3 carbide) same cap$3 same (celsius or degree or degrees)) and (fin or finFET or CMOS or PMOS or NMOS or MOS)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/14 19:49
L37	2	US-20050019993-$.did.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/14 20:22
S1	2	(US-20060046449-$ | 20110156107-$ | 20050019993-$ | 20060099783-$).did.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/09 15:46
S2	8	(US-20060046449-$ | US-20110156107-$ | US-20050019993-$ | US-20060099783-$).did.	US-PGPUB; USPAT; USOCR; FPRS;	OR	ON	2015/04/09 15:48

			EPO; JPO; DERWENT; IBM_TDB			
S3	378	H01L2029/7858.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/09 17:15
S4	12844	H01L29/785,7851,7853,7854,7855,7856,7857,7858,66795,66803,6681,66818.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/09 17:16
S5	12850	S3 or S4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/09 17:16
S6	9371	H01L21/28247,76897.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/09 17:17
S7	378	H01L2029/7858.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/09 17:17
S8	9705	S6 or S7	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/09 17:17
S9	474	S8 and (fin or finFET)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/09 17:18
S10	12996	S9 or S5	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/09 17:18
S11	155502	(high near5 density near5 plasma) or PECVD or HDP or (ionized near5 physical near5 vapor) or IPVD or (I near3 PVD) or (plasma near3 enhanc$5)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/09 17:31
S15	197253	(sacrific$4 or remov$3 or etch$3) near7 gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/09 17:34

S16	1449	S10 and S11 and S15	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/09 17:36
S17	1255	S16 and ((@ad | @pd) <= "20130607")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/09 17:40
S18	1597	438/791,792.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/09 18:26
S19	6955	257/288.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/09 18:27
S20	8536	S18 or S19	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/09 18:27
S21	1087	S20 and (fin or finFET)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/09 18:27
S22	1502	257/E29.264,E21.421.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/09 18:30
S23	523	S22 and (fin or finFET)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/09 18:30
S24	1545	S23 or S21	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/09 18:30
S25	256	S24 and S11 and S15	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/09 18:31
S26	226	S25 and ((@ad | @pd) <= "20130607")	US-PGPUB; USPAT; USOCR; FPRS;	OR	ON	2015/04/09 18:31

			EPO; JPO; DERWENT; IBM_TDB			
S27	63	S26 not S17	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/04/09 18:31

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L38	200	H01L2029/7858.cpc.	US-PGPUB; USPAT; UPAD	OR	ON	2015/04/14 21:10
L39	6672	H01L29/785,7851,7853,7854,7855,7856,7857,7858,66795,66803,6681,66818.cpc.	US-PGPUB; USPAT; UPAD	OR	ON	2015/04/14 21:10
L40	4978	H01L21/28247,76897.cpc.	US-PGPUB; USPAT; UPAD	OR	ON	2015/04/14 21:10
L41	2001	((fin or finFET) and (etch$3 or remov$3 or sacrificial) and (trench or groove)).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2015/04/14 21:11
L42	871	(L38 or L39 or L40) and L41	US-PGPUB; USPAT; UPAD	OR	ON	2015/04/14 21:12

4/14/2015 9:20:55 PM
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Inductively Coupled Pulsed Plasmas in the Presence of Synchronous Pulsed Substrate Bias for Robust, Reliable, and Fine Conductor Etching
Banna, S. ; Agarwal, A. ; Tokashiki, K. ; Hong Cho ; Rauf, S. ; Todorow, V. ; Ramaswamy, K. ; Collins, K. ; Stout, P. ; Jeong-Yun Lee ; Junho Yoon ; Kyoungsub Shin ; Sang-Jun Choi ; Han-Soo Cho ; Hyun-Joong Kim ; Changhun Lee ; Lymberopoulos, D.
Plasma Science, IEEE Transactions on
Volume: 37 , Issue: 9 , Part: 1
DOI: 10.1109/TPS.2009.2028071
Publication Year: 2009 , Page(s): 1730 - 1746
Cited by: Papers (15) | Patents (1)
IEEE JOURNALS & MAGAZINES

Enhanced data retention of damascene-finFET DRAM with local channel implantation and <100> fin surface orientation engineering
Chul Lee ; Jae-Man Yoon ; Choong-Ho Lee ; Jong Chul Park ; Tae Yong Kim ; Hee Soo Kang ; Suk Kang Sung ; Eun Suk Cho ; Cho, Hye Jin ; Young Joon Ahn ; Donggun Park ; Kim, Kinam ; Byung-Il Ryu
Electron Devices Meeting, 2004. IEDM Technical Digest. IEEE International
DOI: 10.1109/IEDM.2004.1419065
Publication Year: 2004 , Page(s): 61 - 64
Cited by: Papers (7) | Patents (3)
IEEE CONFERENCE PUBLICATIONS

Improved post-cycling characteristic of FinFET NAND Flash
Se Hoon Lee ; Jong Jin Lee ; Jeong-Dong Choe , Eun Suk Cho ; Young Joon Ahn ; Won Hwang ; Taeyong Kim ; Woo-Jung Kim ; Young-Bae Yoon ; Donghoon Jang , Jongryeol Yoo ; Dongdae Kim , Kyucham Park , Donggun Park ; Byung-Il Ryu
Electron Devices Meeting, 2006. IEDM '06. International
DOI: 10.1109/IEDM.2006.346901
Publication Year: 2006 , Page(s): 1 - 4
Cited by: Papers (1) | Patents (1)
IEEE CONFERENCE PUBLICATIONS

Damage-Free Plasma Etching Processes for Future Nanoscale Devices
Samukawa, S.
Micro Electro Mechanical Systems, 2009. MEMS 2009. IEEE 22nd International Conference on
DOI: 10.1109/MEMSYS.2009.4805332
Publication Year: 2009 , Page(s): 112 - 119
Cited by: Papers (1)
IEEE CONFERENCE PUBLICATIONS

The ITFET: A Novel FinFET-Based Hybrid Device
Weimin Zhang ; Fossum, J.G. ; Mathew, L.
Electron Devices, IEEE Transactions on
Volume: 53 , Issue: 9
DOI: 10.1109/TED.2006.880813
Publication Year: 2006 , Page(s): 2335 - 2343
Cited by: Papers (1) | Patents (3)
IEEE JOURNALS & MAGAZINES

Epitaxially Defined FinFET: Variability Resistant and High-Performance Technology
Mittal, S. ; Gupta, S. ; Nainani, A. ; Abraham, M.C. ; Schuegraf, K. ; Lodha, S. ; Ganguly, U.
Electron Devices, IEEE Transactions on
Volume: 61 , Issue: 8

DOI: 10.1109/TED.2014.2329993
Publication Year: 2014 , Page(s): 2711 - 2718
Cited by: Papers (1)
IEEE JOURNALS & MAGAZINES

Dual Discharge Modes Operation of an Argon Plasma Generated by Commercial Electronic Ballast for Remote Plasma Removal Process

Cho, T.S. ; Yi-Heng Sen ; Bokka, R. ; Park, S. ; Lubomirsky, D. ; Venkataraman, S.
Plasma Science, IEEE Transactions on
Volume: 42 , Issue: 6 , Part: 2
DOI: 10.1109/TPS.2014.2321172
Publication Year: 2014 , Page(s): 1636 - 1639
IEEE JOURNALS & MAGAZINES

Reliability of sub 30NM BT(Body-Tied)-FinFET with HFSiON/Poly Silicon Gate Stack for symmetric Vth control

Eun Suk Cho ; Choong-Ho Lee ; Fayrushin, A. ; Park, Hong Bae ; Donggun Park
Reliability Physics Symposium Proceedings, 2006. 44th Annual., IEEE International
DOI: 10.1109/RELPHY.2006.251313
Publication Year: 2006 , Page(s): 663 - 664
Cited by: Papers (2) | Patents (1)
IEEE CONFERENCE PUBLICATIONS

Technology Breakthrough of Body-Tied FinFET for sub 50 nm NOR Flash Memory

Eun Suk Cho ; Tae-Yong Kim ; Byung Kyu Cho ; Choong-Ho Lee ; Jong Jin Lee ; Fayrushin, A. ; Chul Lee ; Donggun Park ; Byung-il Ryu
VLSI Technology, 2006. Digest of Technical Papers. 2006 Symposium on
DOI: 10.1109/VLSIT.2006.1705231
Publication Year: 2006 , Page(s): 90 - 91
Cited by: Papers (2) | Patents (2)
IEEE CONFERENCE PUBLICATIONS

Three-Dimensional FinFET Source/Drain and Contact Design Optimization Study

Vega, R.A. ; Tsu-Jae King Liu
Electron Devices, IEEE Transactions on
Volume: 56 , Issue: 7
DOI: 10.1109/TED.2009.2021439
Publication Year: 2009 , Page(s): 1483 - 1492
Cited by: Papers (10)
IEEE JOURNALS & MAGAZINES

Characterization and Optimization of Sub-32-nm FinFET Devices for ESD Applications

Thijs, S. ; Tremouilles, D. ; Russ, C. ; Griffoni, A. ; Collaert, N. ; Rooyackers, R. ; Linten, D. ; Scholz, M. ; Duvvury, C. ; Gossner, H. ; Jurczak, M. ; Groeseneken, G.
Electron Devices, IEEE Transactions on
Volume: 55 , Issue: 12
DOI: 10.1109/TED.2008.2006547
Publication Year: 2008 , Page(s): 3507 - 3516
Cited by: Papers (4)
IEEE JOURNALS & MAGAZINES

The application of BT-FinFET technology for sub 60nm DRAM integration

Choong-Ho Lee ; Jae-Man Yoon ; Chul Lee ; Keunnam Kim ; Seung Bae Park ; Young Joon Ahn ; Hee Soo Kang ; Donggun Park
Integrated Circuit Design and Technology, 2005. ICICDT 2005. 2005 International Conference on
DOI: 10.1109/ICICDT.2005.1502585
Publication Year: 2005 , Page(s): 37 - 41
IEEE CONFERENCE PUBLICATIONS

Nanoscale Roughness Effects at the Interface of Lithography and Plasma Etching: Modeling of Line-Edge-Roughness Transfer During Plasma Etching

Kokkoris, G. ; Constantoudis, V. ; Gogolides, Evangelos
Plasma Science, IEEE Transactions on
Volume: 37 , Issue: 9 , Part: 1
DOI: 10.1109/TPS.2009.2024117
Publication Year: 2009 , Page(s): 1705 - 1714
Cited by: Papers (3)
IEEE JOURNALS & MAGAZINES

Process integration technology and device characteristics of CMOS FinFET on bulk silicon substrate with sub-10 nm fin width and 20 nm gate length
Okano, K. ; Izumida, T. ; Kawasaki, H. ; Kaneko, A. ; Yagishita, A. ; Kanemura, T. ; Kondo, M. ; Ito, S. ; Aoki, N. ; Miyano, K. ; Ono, T. ; Yahashi, K. ; Iwade, K. ; Kubota, T. ; Matsushita, T. ; Mizushima, I. , Inaba, S. ; Ishimaru, K. ; Suguro, K. , Eguchi, K. ; Tsunashima, Y. ; Ishiuchi, H.
Electron Devices Meeting, 2005. IEDM Technical Digest. IEEE International
DOI: 10.1109/IEDM.2005.1609454
Publication Year: 2005 , Page(s): 721 - 724
Cited by: Papers (12) | Patents (16)
IEEE CONFERENCE PUBLICATIONS

FinFET scaling to 10 nm gate length
Bin Yu , Chang, L. ; Ahmed, S. , Haihong Wang ; Bell, S. ; Chih-Yuh Yang ; Tabery, C. ; Chau Ho ; Qi Xiang , Tsu-Jae King ; Bokor, J. , Chenming Hu ; Ming-Ren Lin ; Kyser, D.
Electron Devices Meeting, 2002. IEDM '02. International
DOI: 10.1109/IEDM.2002.1175825
Publication Year: 2002 , Page(s): 251 - 254
Cited by: Papers (137) | Patents (5)
IEEE CONFERENCE PUBLICATIONS

Nanometer-Scale Vertical-Sidewall Reactive Ion Etching of InGaAs for 3-D III-V MOSFETs
Xin Zhao ; del Alamo, J.A.
Electron Device Letters, IEEE
Volume: 35 , Issue: 5
DOI: 10.1109/LED.2014.2313332
Publication Year: 2014 , Page(s): 521 - 523
IEEE JOURNALS & MAGAZINES

A new aspect of plasma-induced physical damage in three-dimensional scaled structures — Sidewall damage by stochastic straggling and sputtering
Eriguchi, K. ; Takao, Y. ; Ono, K.
IC Design & Technology (ICICDT), 2014 IEEE International Conference on
DOI: 10.1109/ICICDT.2014.6838597
Publication Year: 2014 , Page(s): 1 - 5
IEEE CONFERENCE PUBLICATIONS

Four-Terminal FinFETs Fabricated Using an Etch-Back Gate Separation
Endo, K. ; Ishikawa, Y. ; Yongxun Liu ; Ishii, Kenichi ; Matsukawa, T. ; Ouchi, S. ; Masahara, M. ; Sugimata, E. ; Tsukada, J. ; Yamauchi, H. ; Suzuki, Eiichi
Nanotechnology, IEEE Transactions on
Volume: 6 , Issue: 2
DOI: 10.1109/TNANO.2007.891830
Publication Year: 2007 , Page(s): 201 - 205
Cited by: Papers (6)
IEEE JOURNALS & MAGAZINES

Challenges and solutions of FinFET integration in an SRAM cell and a logic circuit for 22 nm node and beyond
Kawasaki, H. ; Basker, V.S. ; Yamashita, T. ; Lin, C. ; Zhu, Y. ; Faltermeier, J. ; Schmitz, S. ; Cummings, J. ; Kanakasabapathy, S. ; Adhikari, H. ; Jagannathan, H. ; Kumar, A. ; Maitra, K. ; Wang, J. ; Yeh, C.-C. ; Wang, C. ; Khater, M. ; Guillorn, M. ; Fuller, N. ; Chang, J. ; Chang, L. ; Muralidhar, R. ; Yagishita, A. ; Miller, R. ; Ouyang, Q. ; Zhang, Y. ; Paruchuri, V.K. ; Bu, H. , Doris, B. ; Takayanagi, M. ; Haensch, W. , Mcherron, D. ; O'Neill, J. ; Ishimaru, K.
Electron Devices Meeting (IEDM), 2009 IEEE International
DOI: 10.1109/IEDM.2009.5424366
Publication Year: 2009 , Page(s): 1 - 4
Cited by: Papers (19) | Patents (4)
IEEE CONFERENCE PUBLICATIONS

Review of FINFET technology
Jurczak, M. ; Collaert, N. ; Veloso, A. ; Hoffmann, T. ; Biesemans, S.
SOI Conference, 2009 IEEE International
DOI: 10.1109/SOI.2009.5318794
Publication Year: 2009 , Page(s): 1 - 4
Cited by: Papers (14) | Patents (1)
IEEE CONFERENCE PUBLICATIONS

Ultimate top-down etching processes for future nanoscale devices
Samukawa, S. ; Kubota, Tomohiro
Solid-State and Integrated-Circuit Technology, 2008. ICSICT 2008. 9th International Conference on

DOI: 10.1109/ICSICT.2008.4734797
Publication Year: 2008 , Page(s): 1316 - 1319
IEEE CONFERENCE PUBLICATIONS

Atomistic simulations of plasma process-induced Si substrate damage - Effects of substrate bias-power frequency
Matsuda, A. ; Nakakubo, Y. ; Takao, Y. ; Eriguchi, K. ; Ono, K.
IC Design & Technology (ICICDT), 2013 International Conference on
DOI: 10.1109/ICICDT.2013.6563334
Publication Year: 2013 , Page(s): 191 - 194
Cited by: Papers (1)
IEEE CONFERENCE PUBLICATIONS

Fluctuations of electrical characteristics of FinFET devices
Tomaszewski, D. ; Malinowski, A. ; Zaborowski, M. ; Salek, P. ; Lukasiak, L. ; Jakubowski, A.
Mixed Design of Integrated Circuits & Systems, 2009. MIXDES '09. MIXDES- 16th International Conference
Publication Year: 2009 , Page(s): 61 - 66
IEEE CONFERENCE PUBLICATIONS

A High-Performance Body-Tied FinFET Bandgap Engineered SONOS (BE-SONOS) for nand-Type Flash Memory
Tzu-Hsuan Hsu ; Hang-Ting Lue ; Ya-Chin King ; Jung-Yu Hsieh ; Erh-Kun Lai ; Kuang-Yeu Hsieh ; Rich Liu ; Chih-Yuan Lu
Electron Device Letters, IEEE
Volume: 28 , Issue: 5
DOI: 10.1109/LED.2007.895421
Publication Year: 2007 , Page(s): 443 - 445
Cited by: Papers (4) | Patents (2)
IEEE JOURNALS & MAGAZINES

PLAD (Plasma Doping) on 22nm Technology Node and Beyond - Evolutionary and/or Revolutionary
Shu Qin ; Hu, Y.J. ; McTeer, A.
Junction Technology (IWJT), 2012 12th International Workshop on
DOI: 10.1109/IWJT.2012.6212600
Publication Year: 2012 , Page(s): 1 - 11
Cited by: Papers (2)
IEEE CONFERENCE PUBLICATIONS

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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13992598	ROSENBAUM ET AL.
	Examiner	Art Unit
	SAMUEL LAIR	2817

CPC- SEARCHED		
Symbol	Date	Examiner
H01L2029/7858	4/9/2015	SLL
H01L21/28247	4/9/2015	SLL
H01L21/76897	4/9/2015	SLL
H01L29/785	4/9/2015	SLL
H01L29/7851	4/9/2015	SLL
H01L29/7853	4/9/2015	SLL
H01L29/7854	4/9/2015	SLL
H01L29/7855	4/9/2015	SLL
H01L29/7856	4/9/2015	SLL
H01L29/7857	4/9/2015	SLL
H01L29/7858	4/9/2015	SLL
H01L29/66795	4/9/2015	SLL
H01L29/66803	4/9/2015	SLL
H01L29/6681	4/9/2015	SLL
H01L29/66818	4/9/2015	SLL

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
PLUS search	2/26/2015	SLL
Inventor name search (see search history)	4/14/2015	SLL
Pure text search (see search history)	4/14/2015	SLL
NPL search on IEEE Xplore (see search history)	4/14/2015	SLL

/SAMUEL LAIR/ Examiner.Art Unit 2817	

SEARCH NOTES		
Search Notes	**Date**	**Examiner**
STIC search (see search history)	3/24/2015	SLL
USPC search limited by text (see search history)	4/9/2015	SLL
CPC search limited by text (see search history)	4/9/2015	SLL

INTERFERENCE SEARCH			
US Class/ CPC Symbol	**US Subclass / CPC Group**	**Date**	**Examiner**
H01L2029	7858	4/14/2015	SLL
H01L21	2847	4/14/2015	SLL
H01L21	78697	4/14/2015	SLL
H01L29	785	4/14/2015	SLL
H01L29	7851	4/14/2015	SLL
H01L29	7853	4/14/2015	SLL
H01L29	7854	4/14/2015	SLL
H01L29	7855	4/14/2015	SLL
H01L29	7856	4/14/2015	SLL
H01L29	7857	4/14/2015	SLL
H01L29	7858	4/14/2015	SLL
H01L29	66795	4/14/2015	SLL
H01L29	66803	4/14/2015	SLL
H01L29	6681	4/14/2015	SLL
H01L29	66818	4/14/2015	SLL

/SAMUEL LAIR/ Examiner.Art Unit 2817	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	13992598
	Filing Date	2013-06-07
	First Named Inventor	Aaron W. Rosenbaum
	Art Unit	2896
	Examiner Name	Samuel L. Lair
	Attorney Docket Number	P38683US

U.S.PATENTS

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

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U.S.PATENT APPLICATION PUBLICATIONS

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20050023133	A1	2005-02-03	Lippitt et al.	
	2	20060157749	A1	2006-07-20	Okuno, Masaki	
	3	20140117425	A1	2014-05-01	Pradhan et al.	
	4	20130256767	A1	2013-10-03	Pradhan et al.	

If you wish to add additional U.S. Published Application citation information please click the Add button.

FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]

EFS Web 2.1.17

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.L.L.

Receipt date: 07/22/2014	Application Number	13992598 13992598 - GAU: 2817
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Filing Date	2013-06-07
	First Named Inventor	Aaron W. Rosenbaum
	Art Unit	2896
	Examiner Name	Samuel L. Lair
	Attorney Docket Number	P38683US

	1							☐

If you wish to add additional Foreign Patent Document citation information please click the Add button

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	International Preliminary Report on Patentability and Written Opinion received for PCT Patent Application No. PCT/US2011/054479, mailed on April 10, 2014, 6 pages.	☐
	2	International Preliminary Report on Patentability and Written Opinion received for PCT Patent Application No. PCT/US2011/054294, mailed on April 10, 2014, 5 pages.	☐
	3	International Preliminary Report on Patentability and Written Opinion received for PCT Patent Application No. PCT/US2011/054464, mailed on April 10, 2014, 6 pages.	☐
	4	International Preliminary Report on Patentability and Written Opinion received for PCT Patent Application No. PCT/US2011/063433, mailed on June 19, 2014, 6 pages.	☐

If you wish to add additional non-patent literature document citation information please click the Add button

EXAMINER SIGNATURE

Examiner Signature	/Samuel Lair/	Date Considered	04/14/2015

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.L.L.

Receipt date: 07/22/2014	Application Number	13992598	13992598 - GAU: 2817
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Filing Date	2013-06-07	
	First Named Inventor	Aaron W. Rosenbaum	
	Art Unit	2896	
	Examiner Name	Samuel L. Lair	
	Attorney Docket Number	P38683US	

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Robert G. Winkle/	Date (YYYY-MM-DD)	2014-07-21
Name/Print	Robert G. Winkle	Registration Number	37,474

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.L.L.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	13992598
Filing Date	2013-06-07
First Named Inventor	Aaron W. Rosenbaum
Art Unit	2817
Examiner Name	Samuel L. Lair
Attorney Docket Number	P38683US

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20110147851	A1	2011-06-23	Thomas, et al.	
	2	20150041926	A1	2015-02-12	Pradhan, et al.	

If you wish to add additional U.S. Published Application citation information please click the Add button. Add

FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	2002-184981	JP	A	2002-06-28	Jang, et al.	English Abstract Submitted.	☐
	2	2004-128314	JP	A	2004-04-22	Kanemoto, Hiroshi	English Abstract Submitted.	☐

EFS Web 2.1.17

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.L.L.

Receipt date: 03/19/2015	Application Number	13992598 13992598 - GAU: 2817
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Filing Date	2013-06-07
(Not for submission under 37 CFR 1.99)	First Named Inventor	Aaron W. Rosenbaum
	Art Unit	2817
	Examiner Name	Samuel L. Lair
	Attorney Docket Number	P38683US

	3	2011/087571	WO	A1	2011-07-21	Cappellani, et al.		☐
	4	2011/090571	WO	A2	2011-07-28	Bohr, et al.		☐

If you wish to add additional Foreign Patent Document citation information please click the Add button Add

NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	Office Action received for Taiwan Patent Application No. 101133821, mailed on December 25, 2014, 7 pages of English Translation and 9 pages of Taiwan Office Action.	☒
	2	Office Action received for Japanese Patent Application No. 2014-533283, mailed on February 10, 2015, 2 pages of English Translation and 1 pages of Japanese Office Action.	☒

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature	/Samuel Lair/	Date Considered	04/14/2015

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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Receipt date: 03/19/2015	Application Number	13992598	13992598 - GAU: 2817
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	First Named Inventor	Aaron W. Rosenbaum	
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☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

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A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Robert G. Winkle/	Date (YYYY-MM-DD)	2015-03-19
Name/Print	Robert G. Winkle	Registration Number	37,474

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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

BIB DATA SHEET

CONFIRMATION NO. 5215

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
13/992,598	06/07/2013	257	2817	P38683US

APPLICANTS
Intel Corporation, Santa Clara, CA, Assignee (with 37 CFR 1.172 Interest);

INVENTORS
Aaron W. Rosenbaum, Portland, OR;
Din-How Mei, Portland, OR;
Sameer S. Pradhan, Portland, OR;

**** CONTINUING DATA ***************************
This application is a 371 of PCT/US11/54464 09/30/2011

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****
06/15/2013

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /SAMUEL L LAIR/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		OR	13	25	4

ADDRESS
Winkle, PLLC
c/o CPA Global
P.O. Box 52050
Minneapolis, MN 55402
UNITED STATES

TITLE
CAPPING DIELECTRIC STRUCTURE FOR TRANSISTOR GATES

FILING FEE RECEIVED		
2300	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

BIB (Rev. 05/07).

Scientific and Technical Information Center

EIC 2800
SEARCH REPORT

STIC Database Tracking Number: 480867

To:	From:
Samuel Lair Location: JEF-6A40 Art Unit: 2817 Friday, March 27, 2015 Case Serial Number: 13/992,598	SCOTT SEGAL Location: EIC2800 JEF-4A58 Phone: (571)272-1314 scott.segal@uspto.gov

Search Notes

Re: Capping Dielectric Structure for Transistor Gate

Examiner Lair:

Attached are edited search results from the patent literature in Thomson Innovation and EAST.

While I am unsure I found documents with all the search limitations, I found some patents that appear to show many of the features of the notched or recessed gate/dense capping layer structure.

I highly recommend that you browse all the results.

If you would like more searching to be done on this case, or if you have questions or comments, please do not hesitate to contact me.

Respectfully,
Scott

Scott Segal
Searcher, STIC-EIC2800
JEF-4A58, 571-272-1314

STIC-EIC2800 MAR 24 2015 480867

From: STIC-EIC2800@uspto.gov
Sent: Saturday, March 21, 2015 3:05 PM
To: Lair, Samuel
Cc: STIC-EIC2800
Subject: Confirmation Receipt: 2800 Search Request - 13992598

Categories: Green Category

This is an automated email confirming that your 2800 Search Request has been received by STIC's EIC2800.

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Requester ----------

Name: **Lair Samuel L**
Organization: **TC 2800**
Art Unit: **2817**
Employee Number: **90024**
Office Location: **JEF-6A40**
PHP: **No**
Phone Number: **(571)272-5714**
Email: **SAMUEL.LAIR@USPTO.GOV**

Request Detail ----------

Attachment: **No**

Case/Application number: **13992598** PALM
Date to Limit Search Results By: **09/30/2011**
Format for Search Results: **EMAIL**
Board of Appeals Case?: **No**

Describe this invention in your own words.:
This invention is a FET whose main distinguishing feature appears to be a notched or recessed gate wherein the notch or recess is covered by a capping layer formed by a high density plasma process (guesses by examiner: PECVD or HDP CVD). See FIG. 24 ELMTS. 166 & 188.

Synonyms:

Additional Comments:

Search Histories

THOMSON INNOVATION

THOMSON REUTERS

SELECT LANGUAGE: ENGLISH | 日本語 | 简体中文

Queries in this Search History

#	Results	Collections	Search Query	Last Run
1	112	All	Specialized Search: Patent Citations - Forward, Backward pns=(WO2013048516 US20130248952 TW201330255 KR2014049075 CN103828057 EP2761664 JP2014531770 SG201400726 US8981435 WO2013048524 TW201320345 US20130256767 DE112011105702 CN103918083 WO2013048449 TW201320343 KR2014054358 CN103843143 EP2761662 SG201400724 US20150041926 WO2013085490 TW201338093 US20140117425 DE112011105925 CN103975424 WO2013048455 TW201330267 US20130264617 KR2014057626 EP2761647 CN103858215 JP2014528643 SG201400719 US20080079094 US7709312);	2015-03-26 12:45:14

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	419	"8981435" "20150041926" JP adj "2014531770" JP adj "2014528643" DE adj "112011105925" EP adj "2761662" EP adj "2761664" EP adj "2761647" CN adj "103975424" DE adj "112011105702" CN adj "103918083" CN adj "103858215" CN adj "103843143" CN adj "103828057" KR adj "2014057626" KR adj "2014054358" "20140117425" SG adj "201400719" KR adj "2014049075" SG adj "201400724" SG adj "201400726" "20130264617" "20130256767" "20130248952" TW adj "201338093" TW adj "201330267" TW adj "201330255" WO adj "2013085490" TW adj "201320345" TW adj "201320343" WO adj "2013048524" WO adj "2013048516" WO adj "2013048455" WO adj "2013048449" "7709312" "20080079094" "20130334713" WO adj "2013095527" "20110281509" "20110272739" "20110156107" "20110151250" "20110147812" "20110147831" "20100155842" "20100105215" "20100048007" "20090142991" "7528025" "7456471" "20080233699" KR adj "2008021918" "20080014710" "20080001187" "20070111435" "20070066184" KR adj "653711" "20060189058" "20060157749" KR adj "585178" "20060099783" "20060088967" "20060046449" "20050023133" "20050019993" KR adj "2004050519" "20020130372" "6136697" "6030692" WO adj "2011090571" WO adj "2011087571" JP adj "2004128314" JP adj "2002184981" "20110223735" JP adj "2011101002" JP adj "2011054718" JP adj "2007250665" "20070057325" "20050156171" "20140346607" "8823060" "20140167187" "20140187039" "7585734" "20080265321" "7384838" "7268024" "8872284" "8871584" "20130249019" "20130187207" "8338892" "20110101469" "20060057802" "6960781" "6869868" "20040173812" "20020086472" "8927373" "8872160" "8828818" "8703565" "8633470" "20130237026" "20130228862" "20130196478" "8440998" "20130092992" GB adj "491515" "8278687" "8129749"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/26 13:49
L2	85	1 and (gate) near4 (notch$3 or recess$4 or undercut$4 or (under adj cut$4) or nick$2 or nook$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/26 13:56
L3	90	1 and (gate) near4 (cut or cutting or groov$3 or incis$4 or indent$5 or microindent$5 or indenture$1 or mark$3 or corner$3 or slot or slotted)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/26 13:56
L4	103	1 and (gate) near6 (notch$3 or recess$4 or undercut$4 or (under adj cut$4) or nick$2 or nook$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/26 13:56
L5	49	1 and (gate) near4 (micronotch$3 or microrecess$4 or microcavit$3 or cavit$3 or opening or concavit$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/26 13:57
L6	72	1 and (gate) near5 (microtrench$3 or trench$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/26 13:57
L7	211	2 3 4 5 6	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/26 13:57
L8	96	7 and (cap or capped or capping)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/26 13:57
L9	81	7 and (cap or capped or capping) near3 (layer$3 or coat$3 or film or thinfilm or surface)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/26 13:57
L10	31	7 and (cap or capped or capping) near2 (dielectric$4 or insulat$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/26 13:58
L11	70	7 and (cap or capped or capping) same (SIN or SI3N4 or SiC or (silicon or SI) adj (carbide or nitride))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/26 13:58
L12	8	7 and (cap or capped or capping) same ("^SI.sub.3N.sub.4^" or "^SI.sub.xN.sub.y^")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/26 13:58
L13	91	9 10 11 12	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/26 13:59

EAST Search History (Prior Art)

L14	21	13 and (nonplanar or (non adj planar)) near3 (transistor or FET)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/26 13:59
L15	19	13 and (HDP or (high adj density adj plasma))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/26 13:59
L16	2	13 and (cap or capping or capped) same (voidless or (void adj less) or voidfree or (void) near1 (free))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/26 14:00
L17	0	13 and (cap or capping or capped) same (void) near1 (without)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/26 14:00
L18	16	13 and (cap or capping or capped) same (dense$5 or densit$3 or densified or densify$3 or densificat$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/26 14:00
L19	8	13 and (cap or capping or capped) same (nanovoid or microvoid or void or pore or porous or micropore or microporous or microporosit$4 or nanoporous or nanopore or porosit$3 or nanoporosit$3 or (nano) adj (pore or porous or porosit$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/26 14:00
L20	70	11 12	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/26 14:01
L21	31	15 16 18 19	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/26 14:01
L22	44	20 not 21	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/26 15:13

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	27826	(gate) near4 (notch$3 or recess$4 or undercut$4 or (under adj cut$4) or nick$2 or nook$3 or cutout or (cut) adj (out))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 06:33
L2	46043	(gate) near4 (cut or cutting or groov$3 or incis$4 or indent$5 or microindent$5 or indenture$1 or mark$3 or corner$3 or slot or slotted)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 06:34
L3	131832	(gate) near4 (micronotch$3 or microrecess$4 or microcavit$3 or cavit$3 or opening or concavit$3 or overhung or overhang$4 or overlap$4 or (over) adj (hung or hang$4) or lap or lapp$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 06:35
L4	1035	(gate) near4 (partial$4) adj (etch$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 06:35
L5	184239	1 2 3 4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 06:35
L6	8901	5 and (cap or capped or capping) near3 (layer$3 or coat$3 or film or thinfilm or surface) same gate	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 06:35
L7	3367	5 and (cap or capped or capping) near2 (dielectric$4 or insulat$4) same gate	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 06:36
L8	5594	5 and (cap or capped or capping) same (SiN or Si3N4 or SiC or (silicon or Si) adj (carbide or nitride))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 06:36
L9	477	5 and (cap or capped or capping) same ("Si.sub.3N.sub.4" or "Si.sub.xN.sub.y")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 06:36
L10	10500	6 7 8 9	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 06:36
L11	347	10 and (cap or capping or capped) same (HDP or (high adj density adj plasma) or HDCVD or (HD adj CVD) or (high adj density) adj (CVD) or (high adj density adj chemical))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 06:37
L12	22	10 and (cap or capping or capped) same (voidless or (void adj less) or voidfree or (void) near1 (free))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 06:37
L13	7	10 and (cap or capping or capped) same (void) near1 (without)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 06:37
L14	181	10 and (cap or capping or capped) near6 (dense$5 or densit$3 or densified or densify$3 or densificat$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 06:38
L15	2	10 and (cap or capping or capped) near6 (nonporous or (non) adj (porous) or (pore or nanopore or micropore) adj (free or less))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 06:39
L16	112	10 and (cap or capping or capped) near6 (nanovoid or microvoid or void or pore or porous or micropore or microporous or microporosit$4 or nanoporous or nanopore or porosit$3 or nanoporosit$3 or (nano) adj (pore or porous or porosit$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 06:40

EAST Search History (Prior Art)

L17	607	11 12 13 14 15 16	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 06:40
L18	132	5 and (cap or capped or capping) same (SIN or SI3N4 or SIC or (silicon or SI) adj (carbide or nitride)) same (HDP or (high adj density adj plasma) or HDCVD or (HD adj CVD) or (high adj density) adj (CVD) or (high adj density adj chemical))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 06:41
L19	12	5 and (cap or capped or capping) same ('"Si.sub.3N.sub.4"' or '"Si.sub.xN.sub.y"') same (HDP or (high adj density adj plasma) or HDCVD or (HD adj CVD) or (high adj density) adj (CVD) or (high adj density adj chemical))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 06:41
L20	304	5 and (cap or capped or capping) near3 (layer$3 or coat$3 or film or thinfilm or surface) same (HDP or (high adj density adj plasma) or HDCVD or (HD adj CVD) or (high adj density) adj (CVD) or (high adj density adj chemical))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 06:42
L21	64	5 and (cap or capped or capping) near2 (dielectric$4 or insulat$4) same gate same (HDP or (high adj density adj plasma) or HDCVD or (HD adj CVD) or (high adj density) adj (CVD) or (high adj density adj chemical))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 06:42
L22	1298	5 and (cap or capped or capping) near2 (dielectric$4 or insulat$4) same gate same (SIN or SI3N4 or SIC or (silicon or SI) adj (carbide or nitride))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 06:42
L23	29	5 and (cap or capped or capping) near2 (dielectric$4 or insulat$4) same gate same (SIN or SI3N4 or SIC or (silicon or SI) adj (carbide or nitride)) same (HDP or (high adj density adj plasma) or HDCVD or (HD adj CVD) or (high adj density) adj (CVD) or (high adj density adj chemical))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 06:43
L24	30	5 and (cap or capped or capping) near2 (dielectric$4 or insulat$4) near6 (dense$5 or densit$3 or densified or densify$3 or densificat$4) same gate	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 06:44
L25	347	18 19 20 21 23 24	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 06:44
L26	9	25 and (nonplanar or (non adj planar))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 06:44
L27	49	25 and (FinFET or (FIN adj FET) or (Fin or finned) near3 (FET or (field adj effect) or transistor))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 06:44
L28	0	25 and ((Multigate adj FET) or MugFET or MIGFET or (MUG adj FET) or (MIG adj FET) or (multiple adj independent) near2 (field adj effect))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 06:44
L29	8	25 and ((multigate adj FET) or (multi adj gate adj field adj effect) Or (trigate near2 transistor) or (tri adj gate near2 transistor))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 06:44
L30	106	25 and (H01L29/66795 or H01L21/823431 or H01L29/66818 or H01L21/845 or H01L29/785 or H01L2029/7858 or H01L29/66545 or H01L21/76897).cpc.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 06:45
L31	46	25 and (H01L29/78).ipc,ipcr.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 06:45
L32	0	25 and (U12-D02E).mc.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 06:45

EAST Search History (Prior Art)

L33	125	25 and (nMOSFET or pMOSFET or MOSFET or MISFET or IGFET or HMET or HEMT or OFET or LDMOS or PHEMT or MHEMT or (IG or MOS or MIS or MOD or CN or CHEM or MES or MUG or FIN or HJ) adj (FET))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 06:45
L34	172	25 and (FET or (field adj effect adj transistor))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 06:45
L35	246	26 27 29 30 31 33 34	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 06:46
L36	1282	(gate) near3 (partial$4 or corner$3) near1 (etch$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 07:38
L37	3736	(gate) near3 (etch$4) near1 (back)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 07:38
L38	9911	(gate) near3 (notch$3 or undercut or (under adj cut) or cutout or (cut adj out) or corner$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 07:39
L39	14557	36 37 38	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 07:39
L40	14506	39 not 35	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 07:39
L41	1511	40 and (cap or capped or capping) near3 (layer$3 or coat$3 or film or thinfilm or surface) same gate	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 07:40
L42	734	40 and (cap or capped or capping) near2 (dielectric$4 or insulat$4) same gate	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 07:40
L43	916	40 and (cap or capped or capping) same (SiN or Si3N4 or SiC or (silicon or Si) adj (carbide or nitride) or ""Si.sub.3N.sub.4"" or ""Si.sub.xN.sub.y"")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 07:41
L44	1724	41 42 43	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 07:41
L45	9	44 and (cap or capped or capping) same (SiN or Si3N4 or SiC or (silicon or Si) adj (carbide or nitride)) same (HDP or (high adj density adj plasma) or HDCVD or (HD adj CVD) or (high adj density) adj (CVD) or (high adj density adj chemical))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 07:41
L46	0	44 and (cap or capped or capping) same (""Si.sub.3N.sub.4"" or ""Si.sub.xN.sub.y"") same (HDP or (high adj density adj plasma) or HDCVD or (HD adj CVD) or (high adj density) adj (CVD) or (high adj density adj chemical))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 07:42
L47	264	40 and (cap or capped or capping) near2 (dielectric$4 or insulat$4) same gate same (SiN or Si3N4 or SiC or (silicon or Si) adj (carbide or nitride))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 07:42
L48	264	44 and (cap or capped or capping) near2 (dielectric$4 or insulat$4) same gate same (SiN or Si3N4 or SiC or (silicon or Si) adj (carbide or nitride))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 07:42

EAST Search History (Prior Art)

L49	5	44 and (cap or capping or capped) same (voidless or (void adj less) or voidfree or (void) near1 (free))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 07:43
L50	2	44 and (cap or capping or capped) same (void) near1 (without)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 07:43
L51	8	44 and (cap or capping or capped) near6 (dense$5 or densit$3 or densified or densify$3 or densificat$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 07:43
L52	0	44 and (cap or capping or capped) near6 (nonporous or (non) adj (porous) or (pore or nanopore or micropore) adj (free or less))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 07:43
L53	2	44 and (cap or capped or capping) near2 (dielectric$4 or insulat$4) near6 (dense$5 or densit$3 or densified or densify$3 or densificat$4) same gate	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 07:44
L54	5	44 and (cap or capped or capping) near6 (dense$5 or densit$3 or densified or densify$3 or densificat$4) same gate	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 07:44
L55	8	44 and (cap or capped or capping) near6 (dense$5 or densit$3 or densified or densify$3 or densificat$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 07:44
L56	121	44 and (gate) near3 (notch$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 07:45
L57	15	44 and (gate) near3 (notch$3) same (cap or capping or capped)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 07:45
L58	15	56 and 57	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 07:45
L59	5387	(gate) near3 (etchback$3 or backetch$4 or (etch$4) near1 (back or side) or sideetch$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 07:54
L60	1911	(gate) near3 (notch$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 07:55
L61	7239	59 60	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 07:55
L62	7224	61 not 58	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 07:55
L63	1121	62 and (gate) same (cap or capping or capped)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 07:55
L64	133	49 50 51 53 54 55 56	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 07:56

EAST Search History (Prior Art)

L65	105	63 and 64	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 07:56
L66	0	65 and (cap or capped or capping) same (SiN or Si3N4 or SiC or (silicon or Si) adj (carbide or nitride)) same (HDP or (high adj density adj plasma) or HDCVD or (HD adj CVD) or (high adj density) adj (CVD) or (high adj density adj chemical))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 07:57
L67	19	65 and (cap or capped or capping) near2 (dielectric$4 or insulat$4) same gate same (SiN or Si3N4 or SiC or (silicon or Si) adj (carbide or nitride))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 07:57
L68	3	65 and (cap or capped or capping) near6 (dense$5 or densit$3 or densified or densify$3 or densificat$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 07:57
L69	105	65 67 68	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/03/27 07:58

US 20130328111A1

(19) **United States**

(12) **Patent Application Publication**

Xie et al.

(10) **Pub. No.: US 2013/0328111 A1**

(43) **Pub. Date: Dec. 12, 2013**

Publication C See Attached Fig 6A

(54) **RECESSING AND CAPPING OF GATE STRUCTURES WITH VARYING METAL COMPOSITIONS**

(75) Inventors: **Ruilong Xie**, Albany, NY (US); **David V. Horak**, Essex Junction, VT (US); **Su Chen Fan**, Cohoes, NY (US); **Pranatharthiharan Haran Balasubramanian**, Watervliet, NY (US)

(73) Assignees: **International Business Machine Corporations**, Armonk, NY (US); **GLOBALFOUNDRIES Singapore Pte. Ltd.**, Singapore (SG)

(21) Appl. No.: **13/491,857**

(22) Filed: **Jun. 8, 2012**

* date too new?

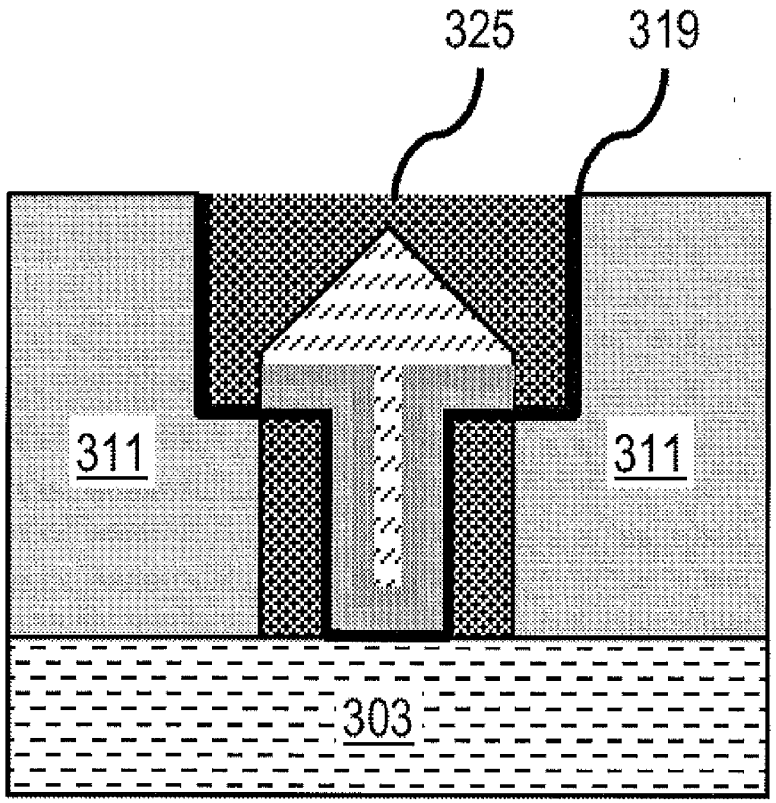
(51) **Int. Cl.**
H01L 21/28
H01L 29/78

(52) **U.S. Cl.**
USPC **257/288**; 438/592; 257/E29.255; 257/E21.19

(paragraph [0030]

(57) **ABSTRACT**

A method for recessing and capping metal gate structures is disclosed. Embodiments include: forming a dummy gate electrode on a substrate; forming a hard mask over the dummy gate electrode; forming spacers on opposite sides of the dummy gate electrode and the hard mask; forming an interlayer dielectric (ILD) over the substrate adjacent the spacers; forming a first trench in the ILD down to the dummy gate electrode; removing the dummy gate electrode to form a second trench below the first trench; forming a metal gate structure in the first and second trenches; and forming a gate cap over the metal gate structure.



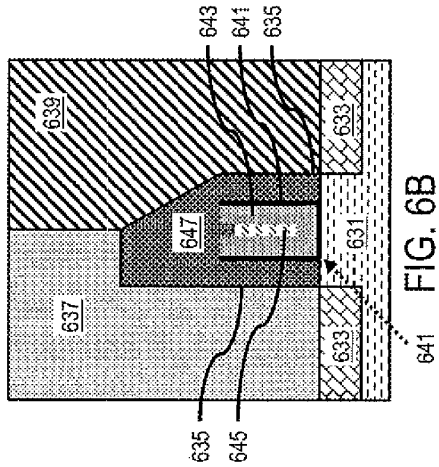

643
641
635
639
633
647
631
637
633
641
635
645

FIG. 6B

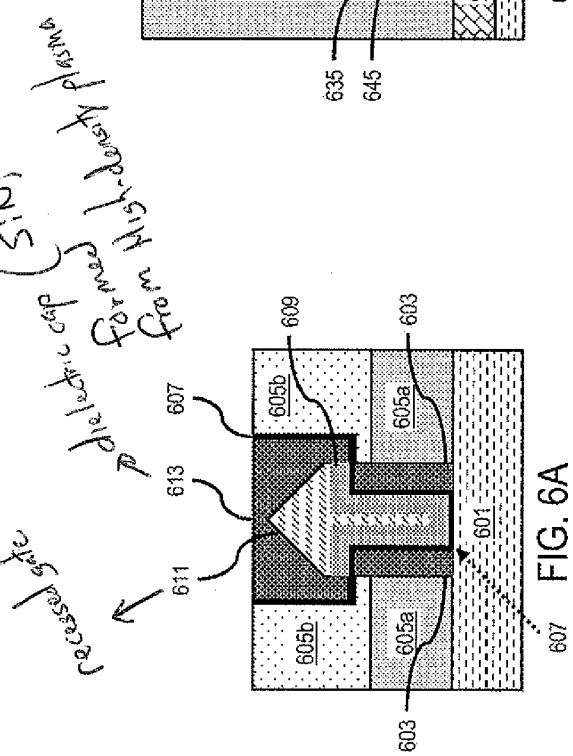

609
603
607
605b
605a
613
601
611
605b
605a
603
607

FIG. 6A

may be deposited and polished, followed by etching of dielectric material **429** and metallization to form self-aligned contact **431**.

[0029] FIGS. **5**A through **5**D schematically illustrate various shapes of metal gate structures that may be formed based on the process flow of FIGS. **3**A through **3**L, in accordance with embodiments of the present disclosure. The structures of FIGS. **5**A through **5**D may, for instance, include substrate **501**, spacers **503**, ILD **505**, high-k dielectric layer **507**, metal liners **509**, and dielectric cap **511**. However, the structures of FIGS. **5**A through **5**D may respectively be formed with metal gate structure **513***a* through **513***d* having the different shapes.

[0030] FIGS. **6**A and **6**B schematically illustrate additional options with respect to the process flows of FIGS. **3**A through **3**L and FIGS. **4**A through **4**Q, in accordance with embodiments of the present disclosure. For example, the structure in FIG. **6**A reflects a structure that may result from the process flow of FIGS. **3**A through **3**L, including substrate **601**, spacers **603**, and oxide **605***a* and **605***b*. In addition, the structure in FIG. **6**A includes high-k dielectric layer **607**, metal liners **609**, and metal gate structure **611**, along with the spacers **603** and dielectric cap **613** over metal liners **609** and metal gate structure **611**, all surrounded by oxide **605***a* and **605***b*. Adverting to FIGS. **3**A through **3**L, ILD **311** may be a flowable oxide to fill the gap between gates. However, since flowable oxide generally has poor CMP dishing performance as well as poor etch resistance against common etching solutions (e.g., a hydrofluoric acid solution), the flowable oxide may be etched and then re-filled with alternative materials having better CMP dishing performance and improved etch resistance (e.g., high-density plasma oxide). Thus, oxide **605***a* may be formed of flowable oxide, while oxide **605***b* may be formed of a different material (e.g., high-density plasma oxide). Moreover, as indicated, metal gate structure **611** may be formed of a number of materials, such as Al, silicide, W, or a combination thereof. Furthermore, the materials used to form spacers **603** (e.g., silicon nitride (SiN)) may be different from the materials used to form dielectric cap **613** (e.g. SiN, silicon carbide nitride (SiCN), silicoboron carbonitride (SiBCN), etc.). The materials used for dielectric cap **613** and spacer **603** may be formed of a material that would give high selectivity to high-density plasma oxide and flowable oxide.

[0031] The structure in FIG. **6**B reflects a structure that may result from the process flow of FIGS. **4**A through **4**Q, including substrate **631**, source/drain regions **633**, oxide **637**, and self-aligned contact **639**. Additionally, the structure in FIG. **6**B includes high-k dielectric layer **641**, metal liners **643**, and metal gate structure **645** between oxides **637** and self-aligned contact **639**, along with dielectric cap **647** over metal liners **643** and metal gate structure **645**. Moreover, the materials used to form spacers **635** may be different from the materials used to form dielectric cap **647**.

[0032] The embodiments of the present disclosure can achieve several technical effects, including controllable metal recess with improved uniformity for devices across a wafer, from wafer-to-wafer, and from lot-to-lot. Embodiments of the present disclosure enjoy utility in various industrial applications as, for example, microprocessors, smart phones, mobile phones, cellular handsets, set-top boxes, DVD recorders and players, automotive navigation, printers and peripherals, networking and telecom equipment, gaming systems, and digital cameras. The present disclosure therefore enjoys industrial applicability in any of various types of highly integrated semiconductor devices.

[0033] In the preceding description, the present disclosure is described with reference to specifically exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the present disclosure, as set forth in the claims. The specification and drawings are, accordingly, to be regarded as illustrative and not as restrictive. It is understood that the present disclosure is capable of using various other combinations and embodiments and is capable of any changes or modifications within the scope of the inventive concept as expressed herein.

1. A method comprising:
forming a dummy gate electrode on a substrate;
forming a hard mask over the dummy gate electrode;
forming spacers on opposite sides of the dummy gate electrode and the hard mask;
forming an interlayer dielectric (ILD) over the substrate adjacent the spacers;
forming a first trench in the ILD down to the dummy gate electrode;
removing the dummy gate electrode to form a second trench below the first trench;
forming a metal gate structure in the first and second trenches;
removing a portion of the metal gate structure from the first trench; and
forming a gate cap over the metal gate structure by filling a remainder of the first trench with dielectric cap material.

2. The method according to claim **1**, further comprising:
forming the first trench by removing the hard mask and a portion of the spacers adjacent the hard mask.

3. The method according to claim **2**, further comprising:
forming a high-k dielectric layer in the first and second trenches;
forming one or more metal liners, over the high-k dielectric layer, in the first and second trenches; and
forming the metal gate structure over the high-k dielectric layer and the metal liners.

4. The method according to claim **3**, further comprising:
recessing the metal liners proximate the ILD, with an etch stop on the spacers, the ILD, the high-k dielectric layer, or a combination thereof subsequent to forming the metal gate structure; and
removing the portion of the metal gate structure during the metal liners recess and removing a second portion of the metal gate structure by etching after the metal liners recess, prior to forming the gate cap.

5. The method according to claim **3**, further comprising:
removing the portion of the metal gate structure from the first trench with an etch stop at a top of the second trench; and
removing a portion of the metal liners and the high-k dielectric layer in the first trench adjacent an upper surface of remaining portions of the spacers, prior to forming the gate cap.

6. The method according to claim **5**, further comprising:
filling a remainder of the second trench with dielectric cap material in addition to the remainder of the first trench;
removing the ILD after the forming of the gate cap; and
removing the high-k dielectric layer and the metal liners around the gate cap after removing the ILD.

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LEE

(54) **SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME**

(75) Inventor: **Byung-Duk LEE**, Icheon-si (KR)

Correspondence Address:
LOWE HAUPTMAN HAM & BERNER, LLP
1700 DIAGONAL ROAD, SUITE 300
ALEXANDRIA, VA 22314 (US)

(73) Assignee: **HYNIX SEMICONDUCTOR INC.**, Icheon-si (KR)

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Publication Clas

(51) **Int. Cl.**
H01L 29/78 (200
H01L 21/28 (200

(52) **U.S. Cl.** **257/3**

See Attached fig 6c paragraphs [0079-0080]

(57) **ABSTRAC**

A semiconductor device with re between a substrate and a plug includes a gate electrode disposed over the substrate, the plug formed over the substrate at both sides of the gate electrode and having a sidewall with a positive slope, a capping layer disposed between the gate electrode and the plug, and a gate hard mask layer whose sidewall disposed over the gate electrode is extended to a top surface of the capping layer. By employing the capping layer having a sidewall with a negative slope, the plug having the sidewall with a positive slope can be formed regardless of a shape or profile of the sidewall of the gate electrode. As a result, the contact area between the substrate and the plug is increased.

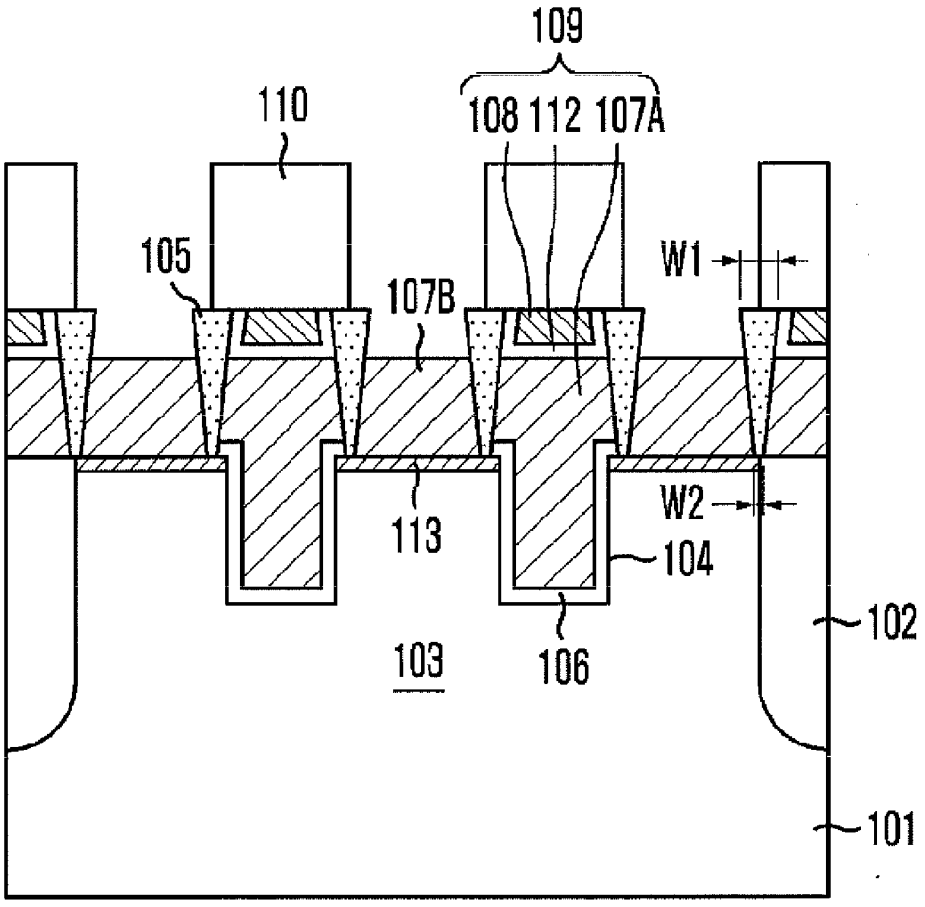


FIG. 6C

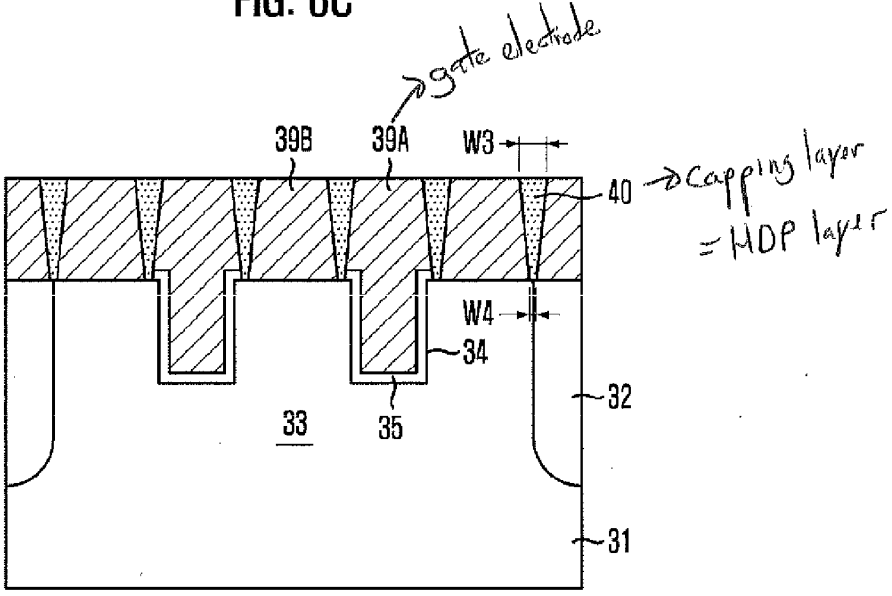
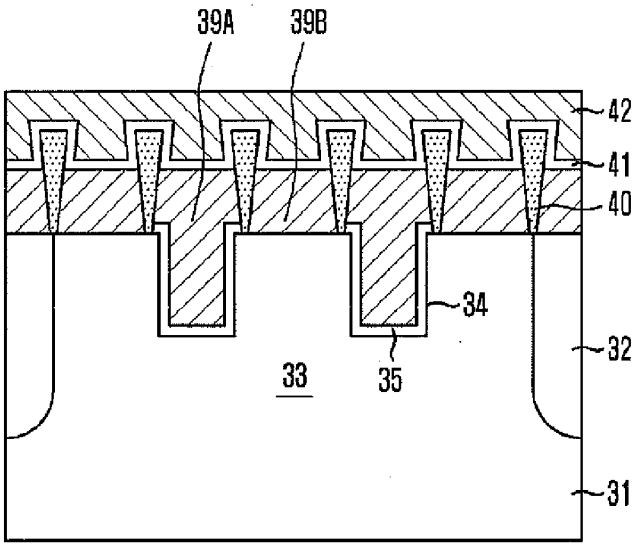

gate electrode
39B
39A
W3
40
capping layer
= HDP layer
W4
34
32
33
35
31

FIG. 6D


39A
39B
42
41
40
34
32
33
35
31

is to be formed. The gate insulation layer **35** may include an oxide layer such as a silicon dioxide (SiO_2) layer and the silicon dioxide layer may be formed through thermal oxidation.

[0069] A method for forming the gate insulation layer **35** on the portion of the substrate **31** where the gate is to be formed may be performed by forming an insulation layer over the entire surface of the substrate **31** and etching the insulation layer, leaving the insulation layer only on the region where the gate is to be formed.

[0070] Another method of selectively forming the gate insulation layer **35** on the portion of the substrate **31** where the gate is to be formed may be performed by forming a sacrificial pattern to expose the region where the gate is to be formed, depositing an insulation layer on a whole surface of the substrate **31**, and removing the insulation layer from portions of the substrate **31** where a gate is not to be formed as well as removing the sacrificial pattern.

[0071] A first conductive layer **36** is formed covering a top surface of the substrate **31** and filling the recess pattern **34**. The first conductive layer **36** may be formed of a silicon layer that has an excellent interfacial property to the substrate **31** and the gate insulation layer **35**. The silicon layer may include a polysilicon layer or a silicon germanium (SiGe) layer. Preferably, the first conductive layer **36** may be formed of a silicon layer that is doped with impurities to improve the conductivity thereof. At this time, the doped silicon layer may be formed by doping the impurities in-situ during the deposition process or doping the impurities ex-situ after the deposition process.

[0072] Referring to FIG. **6**B, a photoresist pattern **37** is formed on the first conductive layer **36**. The photoresist pattern **37** may be formed to cover the region where the gate is to be formed and a region where a landing plug is to be formed in subsequent processes. For instance, after coating photoresist on the first conductive layer **36**, a first exposure process is performed using a gate mask. Then, after performing a second exposure process using a landing plug contact mask, a developing process is performed to form the photoresist pattern **37**.

[0073] A trench **38** having a sidewall with a negative slope is formed by etching the first conductive layer **36** using the photoresist pattern **37** as an etch barrier. As a result, a plug **39**B having a sidewall with a positive slope may be formed at the same time of forming a first gate electrode **39**A. At this time, in the trench **38** having the sidewall with the negative slope, a line width reduces from an upper portion to a lower portion thereof (W1>W2). The trench **38** may be formed to expose the substrate **31** so as to electrically isolate the plug **39**B with the first gate electrode **39**A.

[0074] The first gate electrode **39**A may be formed to have a line shape crossing both of the active region **33** and the device isolation layer **32** at the same time. Since the trench **38** is formed to have the sidewall with the negative slope, the sidewall of the plug **39**B has the positive slope. Therefore, it is possible to increase a contact area between the plug **39**B and the substrate **31** and to reduce contact resistance between the plug **39**B and the substrate **31**, referring to FIGS. **4**A to **5**B.

[0075] The trench **38** having the sidewall with the negative slope provides a region to form a subsequent capping layer. Herein, the reason why the trench **38** is formed to have the sidewall with the negative slope, i.e., the trench **38** is formed to have an upper portion having a line width W1 greater than a line width W2 of a lower portion thereof, is to form a capping layer filling the trench **38** to have a sidewall with a negative slope in a subsequent process or the plug **39**B to have the sidewall with the positive slope.

[0076] The etching process of forming the trench **38** having the sidewall with the negative slope is performed using dry etching such as plasma etching. Herein, a plasma etch apparatus used to form the trench **38** having the sidewall with the negative slope may include an inductively coupled plasma (ICP), an electron cyclotron resonance (ECR), a microwave or a capacitively coupled plasma (CCP) apparatus. In order to adjust an etch profile, a ratio of etch gases, a source power, a bias power, a pressure, or temperatures of a top electrode and a bottom electrode can be adjusted.

[0077] For instance, in case that the first conductive layer **36** includes the polysilicon layer, a mixed gas of $CF_4/O_2/Ar$ is used as an etch gas. If applying a bias power in the range of approximately 10 W to approximately 100 W lower than a bias power required in forming a trench having a sidewall with a vertical profile, the trench **38** having the sidewall with the negative slope can be formed as the straightness of positive ions in plasma is reduced.

[0078] Referring to FIG. **6**C, after removing the photoresist pattern **37**, a capping layer **40** is formed by filling the trench **38** with an insulation material. Since the capping layer **40** is formed by filling the trench **38** with also the sidewall having a negative slope, a sidewall of the capping layer **40** has a negative slope.

[0079] The capping layer **40** protects a gate electrode during subsequent processes and electrically insulates the gate electrode from the plug **39**B. Therefore, the capping layer **40** may include one of an oxide layer, a nitride layer and an oxynitride layer, or a stack structure of the above layers. The oxide layer may include one of a silicon dioxide (SiO_2) layer, a boron phosphorus silicate glass (BPSG) layer, a phosphorus silicate glass (PSG) layer, a tetra ethyl ortho silicate (TEOS) layer, an un-doped silicate glass (USG) layer, a high density plasma (HDP) layer, a spin on glass (SOG) layer and a spin on dielectric (SOD) layer. The nitride layer may include a silicon nitride (Si_3N_4) layer. The oxynitride layer may include a silicon oxynitride (SiON) layer.

[0080] Through the above processes, it is possible to simultaneously form the first gate electrode **39**A and the plug **39**B that are electrically insulated from each other. As a result, a problem caused when forming the plug after forming the gate, e.g., the reduction of the contact area between the plug **39**B and the substrate **31** due to byproducts or residues generated in the etching process for the patterning of the gate electrode, can be prevented.

[0081] Referring to FIG. **6**D, the first gate electrode **39**A and the plug **39**B are recessed by a certain thickness using the capping layer **40** as an etch barrier. At this time, since the first gate electrode **39**A and the plug **39**B are formed of the same material, they can be recessed by the same thickness through one recess process.

[0082] The recess process is used to secure a space where a second gate electrode is to be formed and may be performed by an overall etching process, e.g., an etch-back process. Herein, the etch depth may be in the range of approximately 1,000 Å to approximately 1,500 Å.

[0083] Then, a barrier metal layer **41** and a second conductive layer **42** are sequentially formed on the entire surface of a resultant structure. The barrier metal layer **41** may include a heat resistant metal such as one selected from the group consisting of titanium (Ti), cobalt (Co), molybdenum (Mo),

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(19) **United States**

(12) **Patent Application Publication**

Surthi et al.

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(43) **Pub. Date: Oct. 11, 2012**

(54) **SINGLE-SIDED ACCESS DEVICE AND FABRICATION METHOD THEREOF**

(76) Inventors: **Shyam Surthi**, Boise, ID (US); **Sheng-Wei Yang**, Taoyuan County (TW)

(21) Appl. No.: **13/084,533**

(22) Filed: **Apr. 11, 2011**

Publication Classification

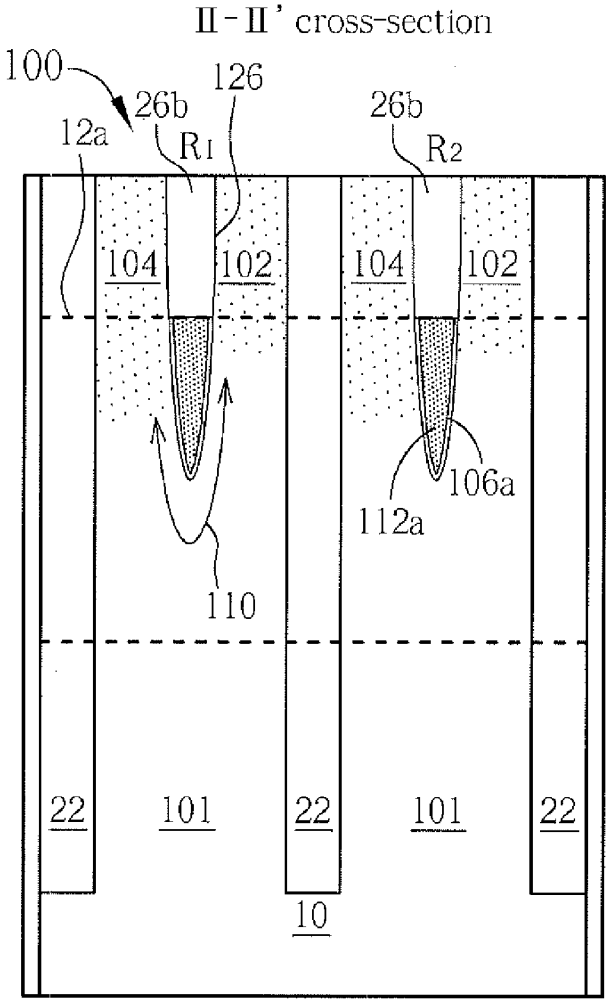
(51) **Int. Cl.**
H01L 29/78 (2006.01)

(52) **U.S. Cl.** .....

See Attached Fig 2C paragraph [0024]

(57) **ABSTRAC**

The present invention provides a si including an active fin structure co and a drain region; an insulating lay source region and the drain region; a disposed at one side of the active fi sidewall gate electrode disposed on fin structure opposite to the trench the active fin structure is sandwiched by trench isolation structure and the single-sided sidewall gate electrode; and a gate protrusion laterally and electrically extended from the single-sided sidewall gate electrode and embedded between the source region and the drain region under the insulating layer.



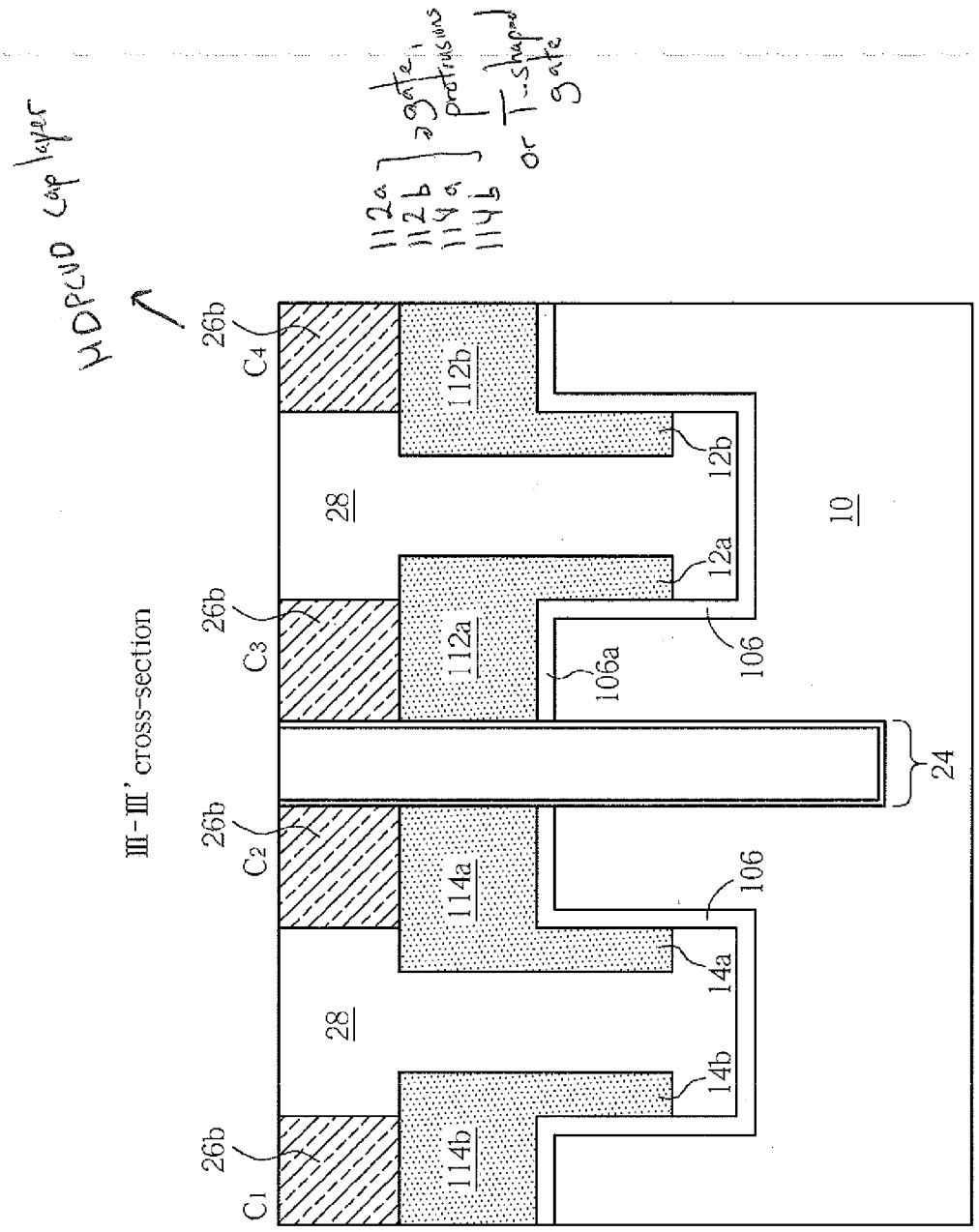

III-III' cross-section
26b
C4
C3
C2
C1
112b
112a
114a
114b
28
12b
12a
14a
14b
106
106a
24
10

FIG. 2C

illustration and description thereof, like or similar features will ordinarily be described with like reference numerals.

[0020] The term "horizontal" as used herein is defined as a plane parallel to the conventional major plane or primary surface of the semiconductor substrate, regardless of its orientation. The term "vertical" refers to a direction perpendicular to the horizontal as just defined. Terms, such as "on", "above", "below", "bottom", "top", "side" (as in "sidewall"), "higher", "lower", "over", and "under", are defined with respect to the horizontal plane.

[0021] Please refer to FIG. **1** and FIGS. **2**A-**2**C. FIG. **1** is a schematic layout diagram showing a portion of an exemplary DRAM array in accordance with one preferred embodiment of this invention. FIG. **2**A shows schematic, cross-sectional view of the single-gate FinFETs of the invention, which is taken along line I-I' (reference x-axis direction) of FIG. **1**. FIG. **2**B shows schematic, cross-sectional view of the single-gate FinFETs of the invention, which is taken along line II-II' (reference y-axis direction) of FIG. **1**. FIG. **2**C is a schematic, cross-sectional view of the single-gate FinFETs of the invention, which is taken along line III-III' (reference x-axis direction) of FIG. **1**. As shown in FIG. **1** and FIG. **2**A, the demonstrated portion of the DRAM array comprises eight single-gate FinFETs arranged in four columns (C1~C4) and two rows (R1 and R2), including single-gate FinFET **100** and single-gate FinFET **200**, for example, which are arranged in the same row (R1) and in two adjacent columns (C2 and C3 respectively).

[0022] The single-gate FinFETs **100** and **200**, which are formed in the active fin structures **101** and **201**, are indicated by the dotted line and are arranged in close proximity to each other. According to the embodiment of the invention, each single-gate FinFET and a corresponding capacitor element (not shown) can be configured as a DRAM cell with a device area of $4F^2$ or even smaller. Sidewall word lines **12***a*, **12***b*, **14***a* and **14***b*, which extend along the reference y-axis, are provided next to each column of transistors. The single-gate FinFET **100** and the single-gate FinFET **200** are mirror symmetrical to each other with respect to a central plane **150**. The single-gate FinFET **100** is electrically isolated from the single-gate FinFET **200** by a line-shaped trench isolation structure **24** that extends along the reference y-axis direction. The trench isolation structure **24** is disposed on a side of the active fin structure **101** or **201** opposite to the sidewall word line **12***a* or **14***a*. As can be seen in II-II' cross-section of FIG. **2**B, each of the active fin structures, e.g. the active fin structure **101**, is a tuning fork-shaped silicon island with an insulating layer **26***b* interposed between the two source/drain regions **102** and **104**.

[0023] The sidewall word lines **12***a* and **12***b* are embedded in a line-shaped trench **122** and are disposed on two opposite sidewalls of the line shaped trench **122**. The sidewall word lines **14***a* and **14***b* are embedded in a line-shaped trench **124** and are disposed on two opposite sidewalls of the line shaped trench **124**. The sidewall word line **12***a* that passes the active fin structure **101** acts as a single-sided sidewall gate electrode of the single-gate FinFET **100** and the sidewall word line **14***a* that passes the active fin structure **201** acts as a single-sided sidewall gate electrode of the single-gate FinFET **200**. The line-shaped trenches **122** and **124** may be filled with insulating layer **28** such as silicon oxide or the like.

[0024] As shown in FIG. **1** and FIG. **2**C, the sidewall word lines **12***a*, **12***b*, **14***a*, **14***b* further include a plurality of gate protrusions **112***a*, **112***b*, **114***a*, **114***b*, respectively, which laterally extend from a single side of each of the sidewall word lines **12***a*, **12***b*, **14***a*, **14***b*. The plurality of gate protrusions **112***a*, **112***b*, **114***a*, **114***b*, which are indicated with dotted lines in FIG. **1**, are formed integrally with the sidewall word lines **12***a*, **12***b*, **14***a*, **14***b* respectfully. Each of the gate protrusions **112***a*, **112***b*, **114***a*, **114***b* and the respective sidewall word lines **12***a*, **12***b*, **14***a*, **14***b* may function as a T-shaped gate of each of the single-gate FinFETs, which improves the access drive current and off state leakage of the single-gate FinFETs. It is one germane feature of this invention that each of the gate protrusions **112***a*, **112***b*, **114***a*, **114***b* is embedded in the lower part of a recessed trench **126** between the source region and the drain region of each single-gate FinFET and is capped with the insulating layer **26***b* such as high-density plasma chemical vapor deposition (HDPCVD) oxide, as shown in II-II' cross-section of FIG. **2**B.

[0025] For example, the single-gate FinFET **100**, which is fabricated in the active fin structure **101**, comprises two source/drain regions **102** and **104** spaced apart from each other, a recessed, U-shaped channel **110** under the two source/drain regions **102** and **104**, the word line **12***a* that acts as a gate electrode, a gate dielectric layer **106** between the U-shaped channel **110** and the word line **12***a*, the gate protrusion **112***a* of the word line **12***a*, and a gate dielectric layer **106***a* between the gate protrusion **112***a* and the U-shaped channel **110**. Likewise, the single-gate FinFET **200**, which is fabricated in the active fin structure **201**, comprises two source/drain regions **202** and **204** spaced apart from each other, a recessed, U-shaped channel **210** under the two source/drain regions **202** and **204**, the word line **14***a* that acts as a gate electrode, a gate dielectric layer **206** between the U-shaped channel **210** and the word line **14***a*, the gate protrusion **114***a* of the word line **14***a*, and a gate dielectric layer (not shown) between the gate protrusion **114***a* and the U-shaped channel **210**.

[0026] FIGS. **3**-**7** are schematic diagrams showing the process of fabricating the single-gate FinFET in accordance with one embodiment of the present invention, wherein like numeral numbers designate like layers, regions or elements.

[0027] As shown in FIG. **3**, a substrate **10** is provided. The substrate **10** may be a semiconductor substrate including but not limited to silicon substrate, silicon substrate with an epitaxial layer, SiGe substrate, silicon-on-insulator (SOI) substrate, gallium arsenide (GaAs) substrate, gallium arsenide-phosphide (GaAsP) substrate, indium phosphide (InP) substrate, gallium aluminum arsenic (GaAlAs) substrate, or indium gallium phosphide (InGaP) substrate. A pad oxide layer **302** and a pad nitride layer **304** may be formed over the primary surface of the substrate **10**. An STI process is then carried out to form line-shaped STI regions **22** embedded in the substrate **10**. The line-shaped STI regions **22** provide electrical isolation between two adjacent rows of devices. According to the embodiment of the invention, each of the line-shaped STI regions **22** extends along the reference x-axis direction. The line-shaped STI regions **22** may be formed by spin-on-dielectric (SOD) gap-fill methods. A lining layer **22***a* may be formed in the STI trench **21**. The lining layer **22***a* may comprise silicon oxide, silicon nitride or combination thereof. Preferably, the lining layer **22***a* comprises a silicon oxide layer (not explicitly shown) formed on interior surface of the STI trench **21** and a silicon nitride layer (not explicitly shown) on the silicon oxide layer. The lining layer **22***a* prevents SOD gap filling material from consuming the substrate **10**.

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Kronholz et al.

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(43) **Pub. Date: May 5, 2011**

(54) **STRAIN ENHANCEMENT IN TRANSISTORS COMPRISING AN EMBEDDED STRAIN-INDUCING SEMICONDUCTOR ALLOY BY CORNER ROUNDING AT THE TOP OF THE GATE ELECTRODE**

(76) Inventors: **Stephan Kronholz**, Dresden (DE); **Roman Boschke**, Dresden (DE); **Maciej Wiatr**, Dresden (DE); **Peter Javorka**, Radeburg (DE)

(21) Appl. No.: **12/893,808**

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Publication Clas

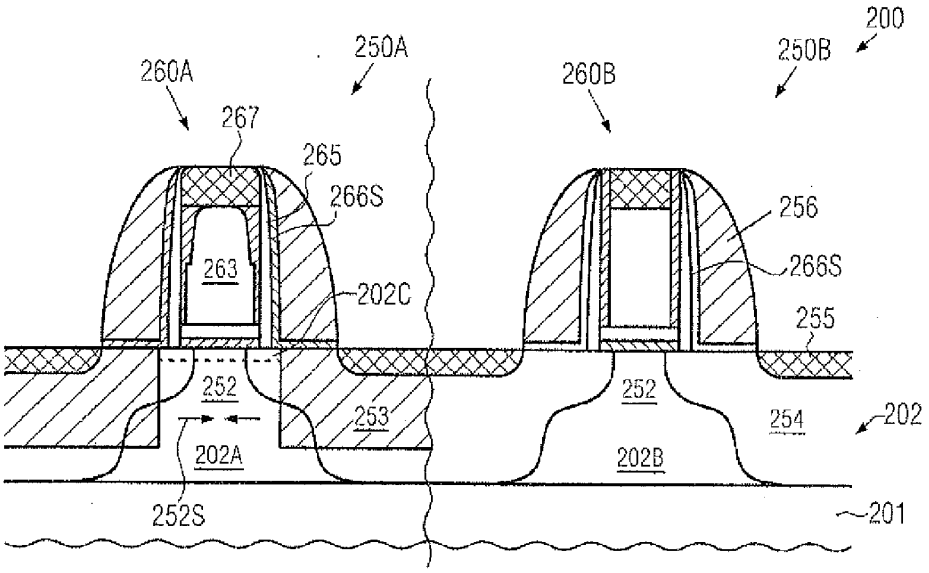
(51) **Int. Cl.**
H01L 27/088 (200
H01L 21/8234 (200
H01L 21/336 (200

(52) **U.S. Cl.** **257/410**; 438/2
2

See Attached Fig 2(b)

(57) **ABSTRA(**

In MOS transistor elements, a strai alloy may be embedded in the active region with a reduced offset from the channel region by applying a spacer structure of reduced width. In order to reduce the probability of creating semiconductor residues at the top area of the gate electrode structure, a certain degree of corner rounding of the semiconductor material may be introduced, which may be accomplished by ion implantation prior to epitaxially growing the strain-inducing semiconductor material. This concept may be advantageously combined with the provision of sophisticated high-k metal gate electrodes that are provided in an early manufacturing stage.



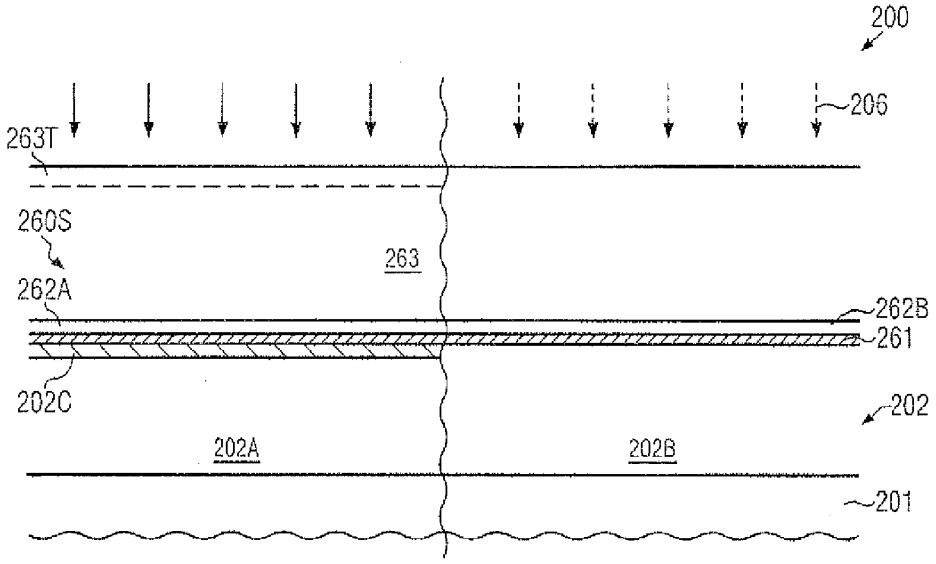

200
206
263T
260S
263
262A
262B
261
202C
202
202A
202B
201

FIG. 2a

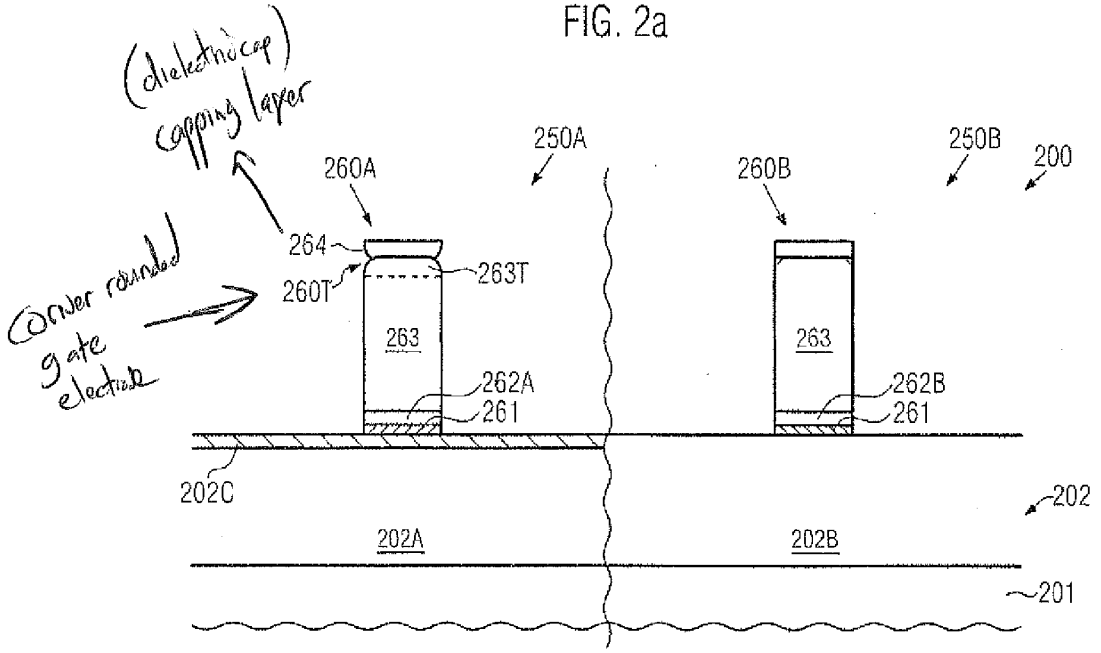

(dielectric cap) capping layer
250A
250B
200
260A
260B
264
263T
260T
corner rounded gate electrode
263
263
262A
262B
261
261
202C
202
202A
202B
201

FIG. 2b

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(12) **Patent Application Publication**

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(54) **SELF-ALIGNED CONTACTS**

(76) Inventors: **Mark T. Bohr**, Aloha, OR (US); **Tahir Ghani**, Portland, OR (US); **Nadia M. Rahhal-Orabi**, Hillsboro, OR (US); **Subhash M. Joshi**, Hillsboro, OR (US); **Joseph M. Steigerwald**, Forest Grove, OR (US); **Jason W. Klaus**, Portland, OR (US); **Jack Hwang**, Portland, OR (US); **Ryan Mackiewicz**, Beaverton, OR (US)

(21) Appl. No.: **12/655,408**

(22) Filed: **Dec. 30, 2009**

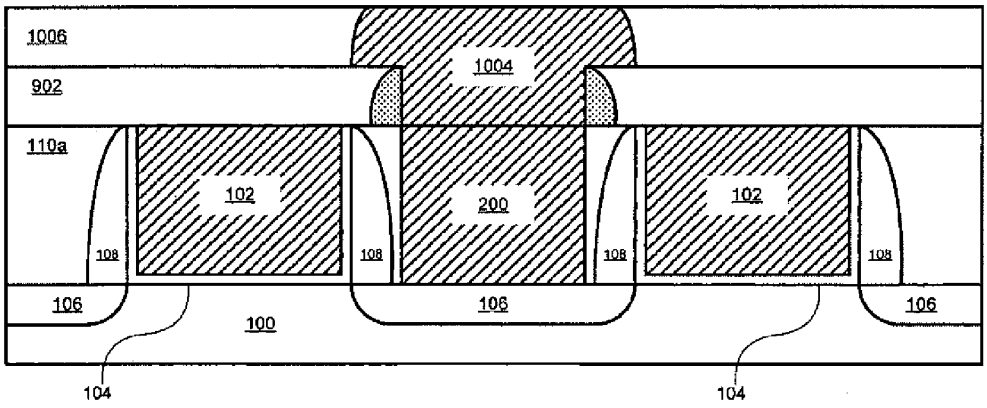
Publication Classi

(51) **Int. Cl.**
H01L 29/78 (200
H01L 21/336 (200

(52) **U.S. Cl.** **257/288**

(57) **ABSTRAC**

A transistor comprises a substrate, substrate, a gate dielectric layer on t... the pair of spacers, a gate electrode layer on the gate dielectric layer and between the pair of spacers, an insulating cap layer on the gate electrode layer and between the pair of spacers, and a pair of diffusion regions adjacent to the pair of spacers. The insulating cap layer forms an etch stop structure that is self aligned to the gate and prevents the contact etch from exposing the gate electrode, thereby preventing a short between the gate and contact. The insulator-cap layer enables self-aligned contacts, allowing initial patterning of wider contacts that are more robust to patterning limitations.



See Attached Figs 7b-c

paragraphs [0041], [0072], [0087]

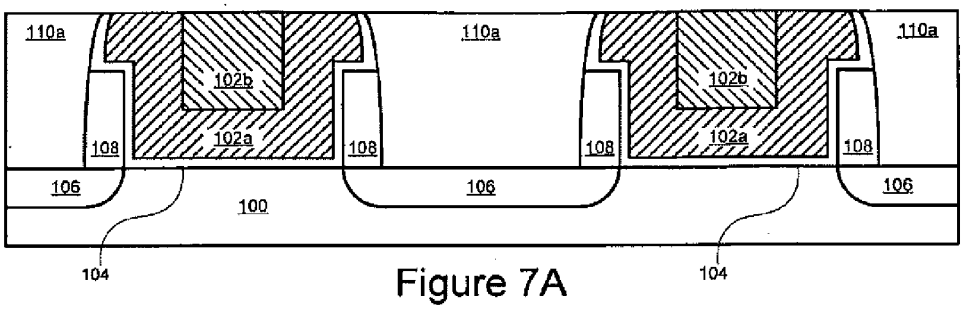


Figure 7A

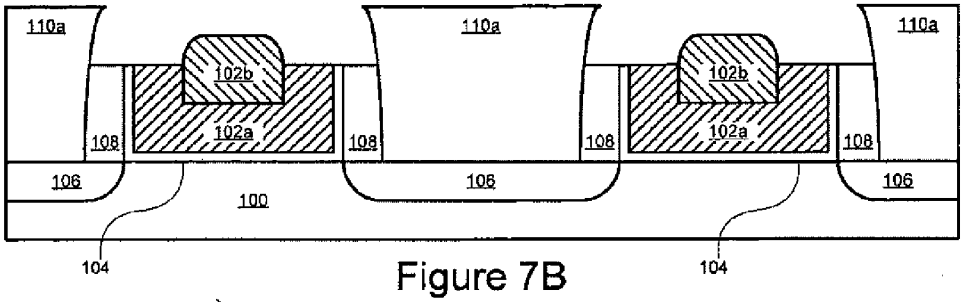


Figure 7B

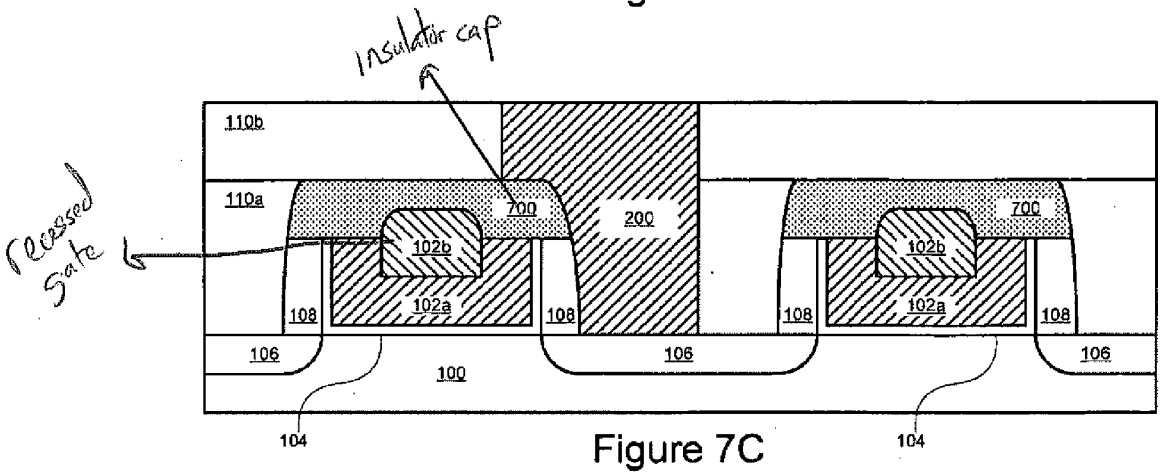


Figure 7C

[0041]

may be deposited and patterned to form a gate stack that consists of the gate dielectric layer **104** and the gate electrode **102**. A pair of spacers **108** and diffusion regions **106** may be formed on either side of the gate stack. Next, an etching process may be carried out to recess the metal gate electrode **102** within the spacers **108**, thereby reducing the thickness of the metal gate electrode **102**. The recessing of the metal gate electrode **102** results in the formation of a trench between the spacers **108** where the bottom surface of the trench corresponds to the top surface of the recessed metal gate electrode **102**. The metal etch process is followed by an insulator material deposition process that deposits a blanket layer of insulator material and fills the trench between the spacers **108**. A polishing process, such as a chemical mechanical planarization process, is used to polish down the insulator material layer and substantially remove any insulator material that is outside of the spacers **108**. The removal of this excess insulator material yields an insulator-cap layer **300** that is substantially contained within the spacers **108**.

[0042] In another implementation of the invention, a gate-last process, such as a replacement metal gate process, is used to form the gate electrode. In this implementation, a blanket dielectric layer and a blanket dummy electrode layer may be initially deposited and patterned to form a gate stack that consists of the gate dielectric layer **104** and a dummy gate electrode (not shown). It should be noted that the term "dummy" is used to indicate that this layer is sacrificial in nature. The materials used in dummy layers may or may not be the same materials that are used in non-dummy layers. For instance, the dummy electrode layer may consist of polysilicon, which is used in real gate electrodes. A pair of spacers **108** and diffusion regions **106** may be formed on either side of the gate stack. Next, the dummy gate electrode may be etched out to form a trench between the spacers **108** and atop the gate dielectric layer **104**. An electrode metal layer may then be deposited to fill the trench. The electrode metal layer may be polished down to remove metal outside of the spacers **108** and to confine the electrode metal to the trench between the spacers **108**, thereby forming a metal gate electrode **102**.

[0043] As described above, an etching process is carried out to recess the metal gate electrode **102** within the spacers **108**. The recessing of the metal gate electrode **102** results in the formation of a trench between the spacers **108**. An insulator material deposition process fills the trench and a polishing process is used to polish down the insulator material layer and substantially remove any insulator material that is outside of the spacers **108**. This yields an insulator-cap layer **300** that is substantially contained within the spacers **108**.

[0044] FIG. **2**B illustrates a trench contact **200** that is correctly aligned between two MOS transistors having insulator-cap layers **300**. In this instance the insulator-cap **300** is not used.

[0045] FIG. **2**C illustrates a misaligned trench contact **200** formed between two MOS transistors having insulator-cap layers **300**. As shown, a portion of the misaligned trench contact **200** is situated directly over the gate electrode **102**. Unlike the prior art transistors shown in FIG. **1**B, however, a CTG short is avoided due to the use of the insulator-cap layer **300**. The insulator-cap layer **300** electrically isolates the metal gate electrode **102** from the misaligned trench contact **200**, allowing the trench contact **200** to be "self-aligned".

[0046] FIGS. **3**A to **3**C illustrate a slight variation on the transistors of FIG. **2**A. In FIG. **3**A, a different implementation of a replacement metal gate process is used to form the transistors. In this implementation, a blanket dummy dielectric layer and a blanket dummy electrode layer are deposited on a substrate. Here, the dummy electrode layer may consist of polysilicon and the dummy dielectric layer may consist of silicon dioxide, both of which are used in real gate electrodes and real gate dielectric layers. These two dummy layers are etched to form a gate stack that consists of a dummy gate dielectric layer and a dummy gate electrode layer. Spacers **108** and diffusion regions **106** are then formed on opposing sides of the gate stack. An ILD layer **110***a* is deposited over the gate stack, spacers **108**, and diffusion regions **106**. The ILD layer **110***a* is planarized to expose the dummy electrode layer.

[0047] Next, the dummy electrode layer and the dummy gate dielectric layer are removed using one or more etching processes. The removal of the dummy layers produces a trench between the spacers **108**. The substrate **100** forms a bottom surface of the trench. A new high-k gate dielectric layer **104** is deposited into the trench using a chemical vapor deposition process or an atomic layer deposition process. The high-k gate dielectric layer **104** is deposited along the bottom and sidewalls of the trench, thereby forming a "U" shaped gate dielectric layer **104**, as shown in FIG. **3**A. Next, a metal gate electrode layer **102** is deposited atop the high-k gate dielectric layer **104**. Processes for forming the metal gate electrode **102** are well known in the art.

[0048] In accordance with implementations of the invention, the final metal gate electrode **102** does not fill the trench in its entirety. In one implementation, the metal gate electrode **102** may initially fill the trench in its entirety, but a subsequent etching process may be used to recess the metal gate electrode **102**. In another implementation, the metal gate electrode deposition process only partially fills the trench with the metal gate electrode **102**. In both implementations, a trench remains above the final metal gate electrode **102** between the spacers **108**.

[0049] Finally, an insulator material deposition process is used to deposit a blanket layer of insulator material that fills the trench between the spacers **108**. A polishing process, such as a chemical mechanical planarization process, is then used to polish down the insulator material layer and remove substantially any insulator material that is outside of the spacers **108**. The removal of this excess insulator yields an insulator-cap layer **300** that is substantially confined within the spacers **108**. As shown in FIG. **3**A, the insulator-cap **300** is also confined within the sidewall portions of the gate dielectric layer **104**.

[0050] FIG. **3**B illustrates a trench contact **200** that is correctly aligned between two MOS transistors having insulator-cap layers **300**. FIG. **3**C illustrates a misaligned trench contact **200** formed between two MOS transistors having insulator-cap layers **300**. Again, a portion of the misaligned trench contact **200** is situated directly over the gate electrode **102**. A CTG short is avoided due to the use of the insulator-cap layer **300**, which electrically isolates the metal gate electrode **102** from the misaligned trench contact **200**.

[0051] FIGS. **4**A to **4**C illustrate a slight variation on the transistors of FIG. **3**A. In FIG. **4**A, a replacement gate process is used again to form transistors having a "U" shaped gate dielectric layer **104**. The gate electrode layer **102** and the gate dielectric layer **104** are initially formed using the same processes detailed above for FIG. **3**A. Unlike FIG. **3**A, in this implementation, both the "U" shaped gate dielectric layer **104** and the metal gate electrode **102** are recessed prior to fabri-

layer **102***a* is typically a workfunction metal layer and the second metal gate electrode layer **102***b* may be a second workfunction metal layer or it may be a fill metal layer. In accordance with implementations of the invention, the metal used in the metal gate electrode **102***a* has different etch properties than the metal used in the metal gate electrode **102***b*.

[0071] Moving to FIG. **7**B, the dual metal gate electrode layers **102***a* and **102***b*, as well as the gate dielectric layer **104**, are etched and recessed. The etch process is selective to the metal gate electrode **102***b*. This yields a stepped profile for the metal gate electrode **102**, as shown in FIG. **7**B. A middle portion of the overall metal gate electrode **102** is relatively thicker than the outer edge portions of the overall metal gate electrode **102**.

[0072] An insulating material is then deposited and planarized to form insulator-cap layers **700** atop each metal gate electrode **102**. This is shown in FIG. **7**C. Also shown is a misaligned trench contact **200**. The stepped profile of the metal gate electrode **102** allows the thick portion of the insulator-cap layer **700** to electrically isolate the metal gate electrode **102** from the trench contact **200**. The stepped profile also allows a middle portion of the metal gate electrode **102** to remain thick, thereby reducing electrical resistance. In this implementation, the insulating-cap layer **700** extends over the recessed spacers **108**, thereby protecting the spacers during the trench contact **200** etch process and allowing a material to be used in the spacers **108** that is optimized for reducing parasitic capacitance between the trench contact **200** and the metal gate electrode **102**.

[0073] FIGS. **8**A to **8**F illustrate another implementation of the invention in which contact sidewall spacers are used to reduce CTG shorts and to improve parasitic capacitance issues. FIG. **8**A illustrates a contact trench opening **800** that has been etched through ILD layers **110***a* and **110***b* down to the diffusion region **106**. As explained above, photolithography patterning and etching processes are used to form the contact trench opening **800**.

[0074] Also shown in FIG. **8**A is a silicide layer **802** that has been formed at the bottom of the contact trench opening **800**. To fabricate the silicide layer **802**, a conventional metal deposition process, such as a sputtering deposition process or an ALD process, may be used to form a conformal metal layer along at least the bottom of the contact trench opening **800**. Often the metal will deposit on the sidewalls of the contact trench opening **800** as well. The metal may include one or more of nickel, cobalt, tantalum, titanium, tungsten, platinum, palladium, aluminum, yttrium, erbium, ytterbium, or any other metal that is a good candidate for a silicide. An annealing process may then be carried out to cause the metal to react with the diffusion region **106** and form a silicide layer **802**. Any unreacted metal may be selectively removed using known processes. The silicide layer **802** reduces the electrical resistance between the later formed trench contact **200** and the diffusion region **106**.

[0075] FIG. **8**B illustrates a pair of contact sidewall spacers **804** that are formed along the sidewalls of the contact trench opening **800**, in accordance with an implementation of the invention. The contact sidewall spacers **804** may be formed using deposition and etching processes similar to the fabrication of gate spacers **108**. For instance, a conformal layer of an insulating material may be deposited within the contact trench opening **800**, resulting in the insulating material being deposited along the sidewalls and bottom surface of the contact trench opening **800**. The insulating material may be silicon oxide, silicon nitride, silicon oxynitride (SiON), carbon-doped silicon oxynitride (SiOCN), any other oxide, any other nitride, or any low-k dielectric material. Next, an anisotropic etching process is used to remove the insulating material from the bottom of the contact trench opening **800**, as well as from other areas such as the surface of the ILD layer **110***b*. This yields the contact sidewall spacers **804** that are shown in FIG. **8**B.

[0076] As will be appreciated by those of skill in the art, a separate patterning process may be used to form vias down to the metal gate electrodes **102** in order to form gate contacts. This separate patterning process will typically involve coating the wafer with a sacrificial photo-definable resist layer, etching the gate contacts, and then removing the photoresist with a wet or dry cleaning process or some combination thereof. This separate patterning process is generally carried out after the contact trench opening **800** has been formed, which means first the resist coating and then the wet or dry clean chemistry enters the contact trench opening **800** and can degrade the silicide layer **802**. Therefore, in accordance with an implementation of the invention, the conformal layer of insulating material used to form the spacers **804** is deposited before the patterning process for the gate contacts. The conformal layer remains in place to protect the silicide layer **802** until after the gate contacts have been patterned. Then the anisotropic etch described above may be carried out to etch the conformal layer and form the spacers **804**.

[0077] It should be noted that the silicide layer **802** is formed prior to fabrication of the contact sidewall spacers **804**, which is when the contact trench opening **800** is at its largest width. By forming the silicide layer **802** before forming the contact sidewall spacers **804**, a relatively wider silicide layer **802** can be formed to provide better electrical resistance properties, such as lower intrinsic contact resistance. If the contact sidewall spacers **804** are formed first, then less of the diffusion region **106** would be exposed for the silicide fabrication process, yielding a relatively shorter silicide layer.

[0078] A metal deposition process is then carried out to fill the contact trench opening **800** and form the trench contact **200**, as shown in FIG. **8**C. As noted above, the metal deposition process can be any metal deposition process, such as electroplating, electroless plating, chemical vapor deposition, physical vapor deposition, sputtering, or atomic layer deposition. The metal used may be any metal that provides suitable contact properties, such as tungsten or copper. A metal liner is often deposited prior to the metal, such as a tantalum or tantulum nitride liner. A CMP process is used to remove any excess metal and complete the fabrication of the trench contact **200**.

[0079] The contact sidewall spacers **804** provide an additional layer of protection between the gate electrodes **102** and the trench contact **200**. The final trench contact **200** has a relatively narrower width than trench contacts **200** formed using conventional processes, thereby reducing the likelihood of CTG shorts. And the additional layer of insulation between the gate electrodes **102** and the trench contact **200** reduces parasitic capacitance.

[0080] FIGS. **8**D to **8**F illustrate the fabrication of contact sidewall spacers **804** when the contact is misaligned. FIG. **8**D illustrates a misaligned contact trench opening **800** that has been etched through ILD layers **110***a* and **110***b* down to the diffusion region **106**. The insulating-cap layer **300** protects the metal gate electrode **102** from being exposed during this

etching process, in accordance with an implementation of the invention. Also shown in FIG. **8**D is a silicide layer **802** that has been formed at the bottom of the contact trench opening **800**. Fabrication processes for the silicide layer **802** were provided above.

[0081] FIG. **8**E illustrates a pair of contact sidewall spacers **804** that are formed along the sidewalls of the contact trench opening **800**, in accordance with an implementation of the invention. The contact sidewall spacers **804** may be formed by depositing and etching a conformal layer of an insulating material, as explained above.

[0082] A metal deposition process is then carried out to fill the contact trench opening **800** and form the trench contact **200**, as shown in FIG. **8**F. Here again, the contact sidewall spacers **804** provide an additional layer of protection between the gate electrodes **102** and the trench contact **200**. The contact sidewall spacers **804** provide more separation between the final trench contact **200** and the metal gate electrodes **102**, thereby reducing the likelihood of CTG shorts. And the additional layer of insulation between the gate electrodes **102** and the trench contact **200** reduces parasitic capacitance.

[0083] FIGS. **9**A to **9**D illustrate another process for forming an insulating-cap layer in accordance with an implementation of the invention. FIG. **9**A illustrates two MOS transistors having metal gate electrodes **102** and gate dielectric layer **104**. The gate electrode layer **102** may include two or more layers (not illustrated), such as a workfunction metal layer and a fill metal layer. Although the gate dielectric layer **104** shown corresponds to a replacement-metal gate process, the following process may also be used with transistors formed using a gate-first approach.

[0084] A metal-cap **900** is formed atop the metal gate electrode **102**, as shown in FIG. **9**A. In accordance with implementations of the invention, the metal-cap **900** is formed using a selective deposition process. Some selective deposition processes include, but are not limited to, electroless plating and chemical vapor deposition. Metals that may be selectively deposited include, but are not limited to, cobalt, nickel, platinum, copper, polysilicon, tungsten, palladium, silver, gold, and other noble metals. As will be appreciated by those of skill in the art, the choice of whether an electroless process or a CVD process is used will depend on the composition of the metal gate electrode **102** and the specific metal that is used in the metal-cap **900**. In one example, if the top portion of the metal gate electrode **102** consists of copper metal, then cobalt metal can be electrolessly deposited on the copper. In another example, tungsten or polysilicon can be deposited by CVD on almost any metal that is used in the metal gate electrode **102**. In another example, if the top portion of the metal gate electrode **102** consists of a noble metal, then most metals may be deposited using an electroless process on the noble metal. As will be appreciated by those of ordinary skill in the art, in general, electroless processes require a noble metal for both the substrate metal and the metal to be deposited. Therefore combinations of metals such as cobalt, nickel, copper, platinum, palladium, gold, and silver are possible.

[0085] Moving to FIG. **9**B, an ILD layer **902** is blanket deposited over the ILD **110***a* and the metal-caps **900**. A CMP process is then used to plagiarize both the ILD layer **902** and the metal-caps **900** and cause their top surfaces to be substantially even. This is done to expose the top surface of the metal-caps **900** after the ILD deposition.

[0086] Next, as shown in FIG. **9**C, an etching process is used to remove the metal-caps **900** from within the ILD layer **902**. In one implementation, a wet etch chemistry may be applied to remove the metal-caps **900**. In accordance with implementations of the invention, the etch chemistry that is used must be selective to both the ILD layer **902** and the metal gate electrode **102**. This enables the metal-caps **900** to be removed with minimal impact to the ILD layer **902** and the metal gate electrode **102**. The removal of the metal-caps **900** yields voids **904** within the ILD layer **902**.

[0087] Moving to FIG. **9**D, an insulating layer, such as a silicon nitride layer, may be deposited and planarized to fill in the voids **904**, thereby forming self-aligned insulating-cap layers **906**. This insulating layer is generally deposited as a blanket layer that fills the voids **904** and covers the ILD layer **902**. A planarization process is then used to remove any excess material that is outside of the voids **904**. This confines the insulating material to the voids **904**, thereby forming insulating-cap layers **906**. The insulator-cap layers **906** may be formed of materials that include, but are not limited to, silicon nitride, silicon oxide, silicon carbide, silicon nitride doped with carbon, silicon oxynitride, other nitride materials, other carbide materials, aluminum oxide, other oxide materials, other metal oxides, and low-k dielectric materials. The only constraint is that the material used in the insulator-cap layers **906** be dissimilar to the material used in the ILD layer **902**.

[0088] FIGS. **10**A to **10**G illustrate a process for forming a self-aligned metal stud atop the trench contact **200** and a pair of insulating spacers that further insulate the metal stud from the metal gate electrodes **102**, in accordance with an implementation of the invention. FIG. **10**A illustrates two MOS transistors having metal gate electrodes **102** and gate dielectric layer **104**. A trench contact **200** is formed between the two MOS transistors.

[0089] A metal-cap **900** is formed atop the trench contact **200**, as shown in FIG. **10**A. In accordance with implementations of the invention, the metal-cap **900** is formed using a selective deposition process. As noted above, selective deposition processes include, but are not limited to, electroless plating and chemical vapor deposition. The same metals and processes described above for use with the metal gate electrode **102** may also be used here with the trench contact **200**. The selective deposition process used and the metal used in the metal-cap **900** will depend on the metal that is used in the trench contact **200**.

[0090] In accordance with implementations of the invention, a selective deposition process is chosen that will deposit metal on only the trench contact **200** and not on the metal gate electrode **102**. This can be accomplished by using different types of metals in the trench contact **200** and the metal gate electrode **102**. For example, if aluminum is used in the metal gate electrode **102** and a noble metal is used in the trench contact **200**, then a selective deposition process can be used to deposit the metal-cap **900** on only the noble metal in the trench contact **200**. The same combinations of noble metals described above will work here as well. In some implementations of the invention, when an active metal such as aluminum, tungsten, molybdenum, titanium, tantalum, titanium nitride, or polysilicon is used in the metal gate electrode **102**, then a noble metal such as cobalt, nickel, copper, platinum, palladium, gold, and silver may be used in the trench contact **200**.

Cap = SiN - SiC

US 20050019993A1

(19) United States

(12) Patent Application Publication (10) Pub. No.: US 2005/0019993 A1

Lee et al. (43) Pub. Date: Jan. 27, 2005

(54) METHODS FOR FABRICATING FIN FIELD EFFECT TRANSISTORS USING A PROTECTIVE LAYER TO REDUCE ETCHING DAMAGE

(76) Inventors: **Deok-Hyung Lee**, Gyeonggi-do (KR); **Si-Young Choi**, Gyeonggi-do (KR); **Byeong-Chan Lee**, Gyeonggi-do (KR); **Yong-Hoon Son**, Gyeonggi-do (KR); **In-Soo Jung**, Gyeonggi-do (KR)

Correspondence Address:
MYERS BIGEL SIBLEY & SAJOVEC
PO BOX 37428
RALEIGH, NC 27627 (US)

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(22) Filed: **Jun. 16, 2004**

(30) **Foreign Application Priority Data**

Jul. 24, 2003 (KR) 10-2003-51028

Publication Classi See Attached Figs 17a-d

(51) **Int. Cl.**[7] H0
H01L

(52) **U.S. Cl.** .....

paragraph [0057]

(57) **ABSTRACT**

A method of forming a fin field effect transistor on a semiconductor substrate includes forming a vertical fin protruding from the substrate. A buffer oxide liner is formed on a top surface and on sidewalls of the fin. A trench is then formed on the substrate, where at least a portion of the fin protrudes from a bottom surface of the trench. The trench may be formed by forming a dummy gate on at least a portion of the fin, forming an insulation layer on the fin surrounding the dummy gate, and then removing the dummy gate to expose the at least a portion of the fin, such that the trench is surrounded by the insulation layer. The buffer oxide liner is then removed from the protruding portion of the fin, and a gate is formed in the trench on the protruding portion of the fin.

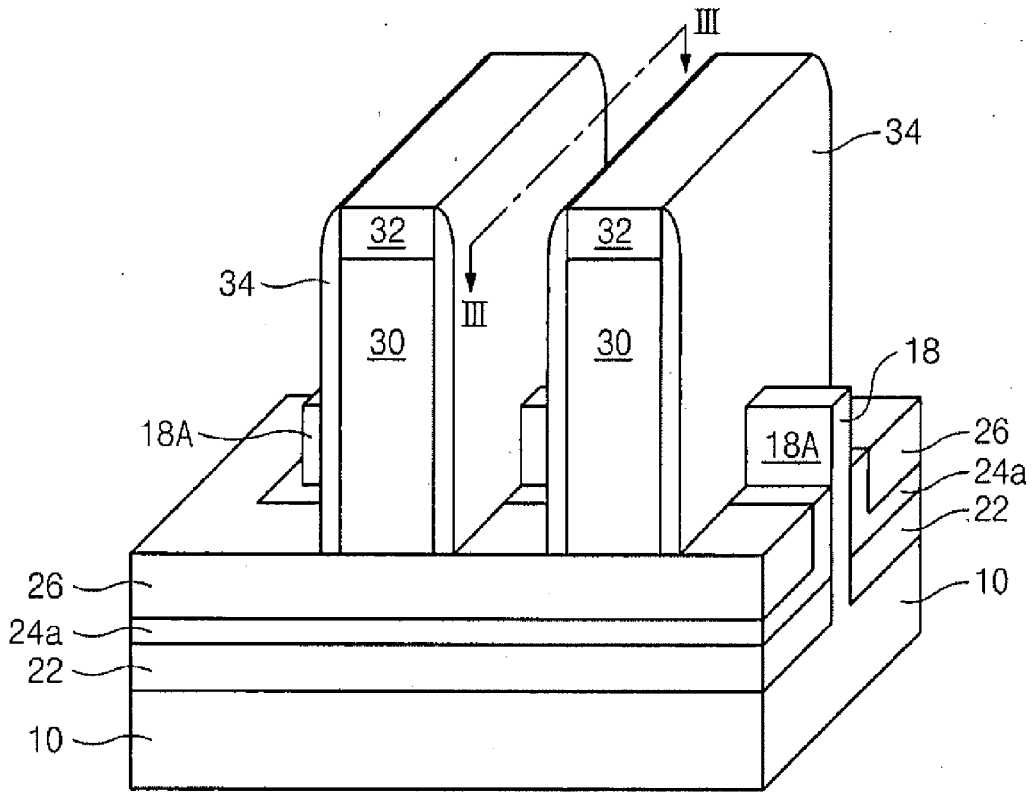


Fig. 17A

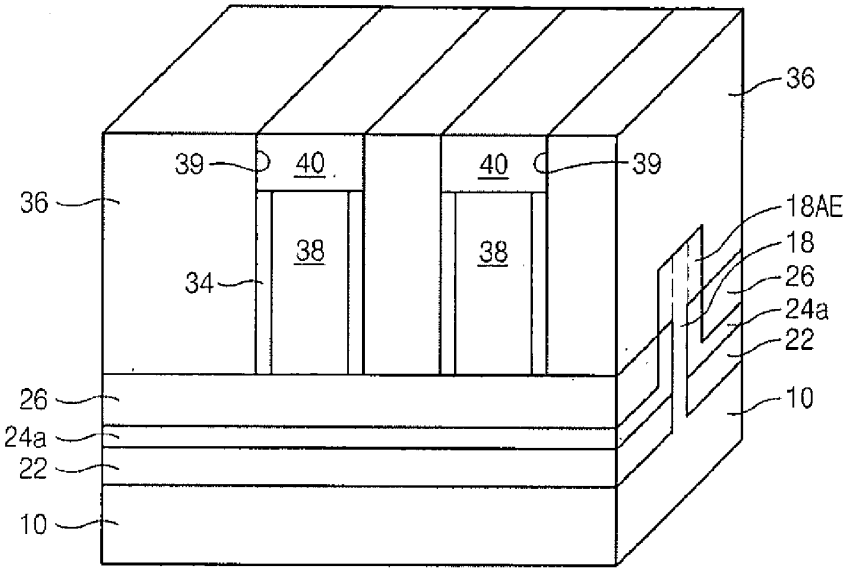


Fig. 17B

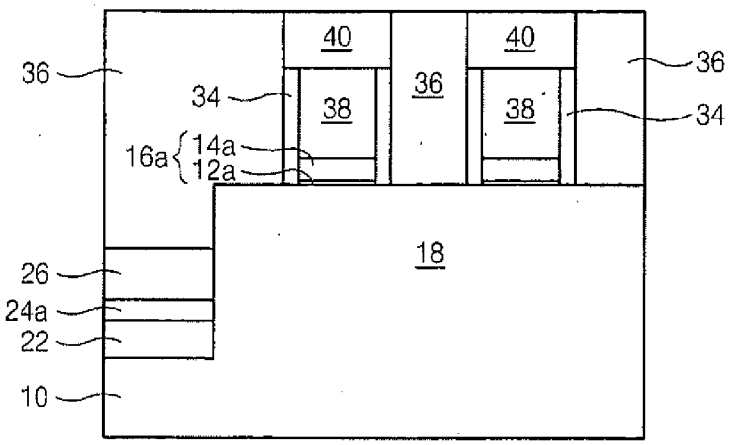


Fig. 17C

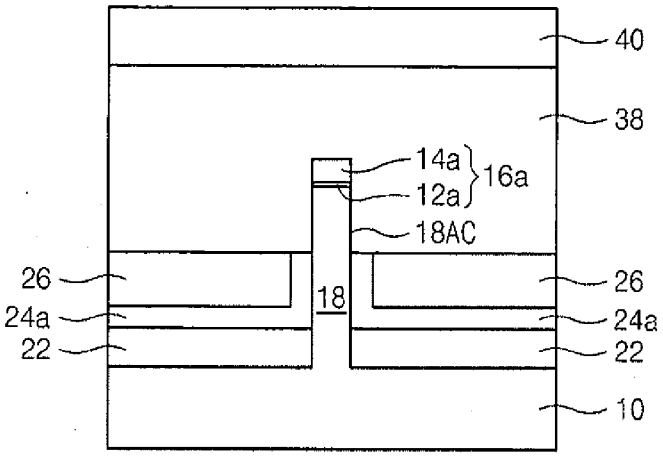
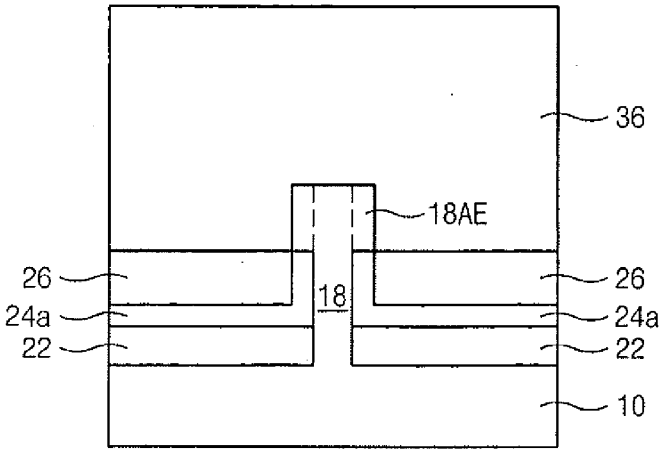


Fig. 17D



to a thickness of about 100 to about 300 Angstroms using a conventional thin-film deposition method, such as CVD. The buffer oxide liner **28** may protect the sidewalls of the silicon fin **18** in subsequent processing.

[0044] Next, referring to **FIG. 10A** to **FIG. 10C**, a sacrificial layer is formed which may fill the trench **20** and which may have a predetermined height (corresponding to the desired height of the transistor gate) from the fin capping layer. The sacrificial layer may be formed to the desired height of a gate electrode. An etching mask **32** is then formed on the sacrificial layer. The portion of the sacrificial layer exposed by the etching mask **32** is etched to form a dummy gate **30**. The dummy gate **30** may be formed of silicon. The etching mask **32** may be formed of a nitride layer.

[0045] Then, as shown in **FIG. 11A** to **FIG. 11C**, the exposed portions of the buffer oxide liner **28** are etched until the fin capping layer **16** (including nitride layer **14**) is exposed.

[0046] In some embodiments, the sacrificial layer and the buffer oxide liner **28** may be etched by a one-step etching process, using an etch gas which may have an etching selectivity with respect to the nitride layer **14**. In other words, to prevent electrical contact between neighboring dummy gates **30**, the sacrificial layer and the buffer oxide liner **28** may be over-etched until the fin capping layer **16** is exposed.

[0047] Alternatively, after the sacrificial layer is selectively etched with respect to the buffer oxide liner **28** and the nitride layer **14** (of the fin capping layer **16**), the buffer oxide liner **28** may be selectively etched with respect to the nitride layer **14**.

[0048] In either case, a buffer oxide layer **28***a* remains on the exposed sidewalls of the silicon fin **18** to protect the sidewalls **18**A of the silicon fin **18** from the etching process. In addition, because the fin capping layer **16** is formed on an upper portion of the silicon fin **18**, the silicon fin **18** is protected from etching damage during the etching process used in forming the dummy gates **30**. As such, over-etching may be performed to ensure that neighboring dummy gates **30** are electrically separated without concern as to etching damage to the silicon fin **18**.

[0049] Next, the exposed portions of the fin capping layer **16** are removed from the exposed portions of the silicon fin **18**, and the exposed buffer oxide layer **28***a* (which remains on sidewalls of the silicon fin **18**) is removed to expose sidewalls **18**A of the silicon fin **18**. At this time, as shown in **FIG. 12A** to **FIG. 12D**, after forming a spacer insulation layer, the spacer insulation layer is etched-back to form spacers **34** on the sidewalls of the dummy gates **30** and to simultaneously remove the fin capping layer **16**. In other words, etching is performed to form the spacers **34**, and the etching is continued (i.e. over-etching is performed) to remove the fin capping layer **16**. The exposed buffer oxide layer **28***a* is also removed.

[0050] After forming the dummy gates **30**, an optional oxidation process may be used to oxidize a part of the dummy gates **30** before forming the spacers **34**. The width of the dummy gates **30** (corresponding to the length of a gate) may then be reduced by removing the oxidized portion. In this case, the oxidized portions of the dummy gates **30** may be removed by wet etching or chemical dry etching. Source/drain regions are then formed by implanting impurity ions into opposite ends of the exposed silicon fin **18**.

[0051] Next, referring to **FIG. 13A** to **FIG. 13D**, an optional epitaxial process may be used to increase the width of the silicon fin to form an extended silicon fin **18**AE. The source/drain regions may be formed in the extended silicon fin **18**AE. Accordingly, because the size of the extended silicon fin is increased, margins may be increased in subsequent processes.

[0052] If an epitaxial silicon growth process is performed, impurity ion implantation for forming the source/drain regions may be performed after forming the extended silicon fin **18**AE. In other words, the source/drain regions may be formed by implanting impurity ions into the extended silicon fin **18**AE using the dummy gates **30** and the spacers **34** as an ion implantation mask. In some embodiments, it may be preferable to perform both the optional oxidation process and the optional epitaxial silicon growth.

[0053] Next, referring to **FIG. 14A** to **FIG. 14D**, an insulation layer **36** is formed to fill the space between the dummy gates **30** (thereby covering the exposed extended silicon fin **18**AE). More particularly, an insulation layer is formed on the substrate surface over the dummy gates **30**, filling the space between the dummy gates **30**. The insulation layer may be formed using a conventional thin film deposition method. A planarizing process may then be performed until the etching mask **32** on top of each dummy gate **30** is exposed.

[0054] Next, referring to **FIG. 15A** to **FIG. 15D**, after removing the etching mask **32**, the dummy gates **30** are removed. Accordingly, portions of the remaining buffer oxide liner **28***b* under the dummy gates **30** are exposed. The etching mask **32** may be removed by wet etching using phosphoric acid. Channel ion implantation may then be performed. In the channel ion implantation process, impurity ions may be implanted into the silicon fin through the exposed remaining buffer oxide liner **28***b* to create a channel region.

[0055] Then, referring to **FIG. 16A** to **FIG. 16D**, the exposed remaining buffer oxide liner **28***b* is removed. As a result, a residual fin capping layer **16***a* and sidewalls **18**AC of the silicon fin **18** (which will form the channel) are exposed, and trenches or "grooves"**37** for defining gate electrodes are formed.

[0056] Next, a conductive material is formed to fill the grooves **37**, so that transistor gate electrodes **38** are formed. More particularly, after forming the conductive material on the substrate surface over the insulation layer **36** to fill the grooves **37**, a planarizing process is performed until the insulation layer **36** is exposed, leaving the conductive material in the grooves **37** to form the gates **38**.

[0057] In this case, as shown in **FIG. 17A** to **FIG. 17D**, a gate capping layer **40** may be formed on an upper portion of the gates **38**. More particularly, after the planarizing process leaves the conductive material in the groove **37**, a portion of the conductive material in the groove **37** is removed to recess the conductive material relative to an upper portion of the insulation layer **36**. As a result, a recessed gate **38** is formed. Accordingly, a groove **39** for the gate capping layer **40** is defined on an upper portion of the recessed gate line **38**.

A gate capping material, such as a nitride layer, is formed on the insulation layer **36** to fill the groove **39**. The excess gate capping material is then removed by a planarizing process until the insulation layer **36** is exposed. The gate capping material that remains in the groove **39** forms the gate capping layer **40**. The gate capping layer **40** may be formed in cases where a self-aligned contact process may be subsequently applied.

[**0058**] According to various embodiments of the present invention, because the gate is formed using a dummy gate, damages to the silicon fin may be reduced. Therefore, more reliable devices may be formed.

[**0059**] In addition, when epitaxial silicon growth is used, process margins may be improved for source/drain contact formation. Also, when an oxidation process is applied to the sacrificial dummy gate, the length of the gate may be reduced.

[**0060**] Further, because a buffer oxide layer is formed on the silicon fin, the sidewalls of the silicon fin may be protected from etching damage during the formation of the dummy gates.

[**0061**] Moreover, because the device isolation layer may include both upper and lower insulation layers, a narrow and deep trench may be completely filled.

[**0062**] Many alterations and modifications may be made by those having ordinary skill in the art, given the benefit of present disclosure, without departing from the spirit and scope of the invention. Therefore, it must be understood that the illustrated embodiments have been set forth only for the purposes of example, and that it should not be taken as limiting the invention as defined by the following claims. The following claims are, therefore, to be read to include not only the combination of elements which are literally set forth but all equivalent elements for performing substantially the same function in substantially the same way to obtain substantially the same result. The claims are thus to be understood to include what is specifically illustrated and described above, what is conceptually equivalent, and also what incorporates the essential idea of the invention.

What is claimed is:

1. A method of forming a fin field effect transistor on a semiconductor substrate, comprising:

forming a vertical fin protruding from the substrate;

forming a buffer oxide liner on a top surface and on sidewalls of the fin;

forming a trench on the substrate, wherein at least a portion of the fin protrudes from a bottom surface of the trench;

removing the buffer oxide liner from the protruding portion of the fin; and

forming a gate in the trench on the protruding portion of the fin.

2. A method of forming a fin field effect transistor on a semiconductor substrate, comprising:

forming a vertical fin protruding from the substrate;

forming a buffer oxide liner on a top surface and on sidewalls of the fin;

forming a dummy gate on at least a portion of the fin;

forming an insulation layer on the fin surrounding the dummy gate;

removing the dummy gate to expose the at least a portion of the fin and to form a trench surrounded by the insulation layer;

removing the buffer oxide liner from the exposed portion of the fin; and

forming a gate in the trench.

3. The method of claim 2, further comprising forming a fin-capping layer on the top surface of the fin before forming the buffer oxide liner.

4. The method of claim 3, wherein the fin-capping layer comprises a nitride layer and an oxide layer.

5. The method of claim 2, further comprising forming a device isolation layer prior to forming the buffer oxide liner, wherein forming the device isolation layer comprises:

forming a nitride liner on the substrate and on the top surface and on the sidewalls of the fin;

forming an upper trench insulation layer on the substrate, wherein at least a portion of the fin protrudes above the upper trench insulation layer; and

removing the nitride liner from the at least a portion of the fin.

6. The method of claim 5, wherein forming the device isolation layer further comprises:

forming a lower trench insulation layer on the substrate before forming the nitride liner; and

removing the upper trench insulation layer after removing the nitride liner from the at least a portion of the fin.

7. The method of claim 5, wherein forming the device isolation layer further comprises:

forming an oxide liner on the fin before forming the nitride liner; and

removing the oxide liner from the at least a portion of the fin after removing the nitride liner.

8. The method of claim 3, wherein forming the insulation layer comprises:

removing the buffer oxide liner and the fin-capping layer from portions of the fin which are not covered by the dummy gate to expose other portions of the fin; and

forming an insulation layer surrounding the dummy gates on the exposed other portions of the fin.

9. The method claim 8, further comprising epitaxially growing silicon on the exposed portions of the fin before forming the insulation layer.

10. The method of claim 3, wherein forming the dummy gate comprises:

forming a sacrificial layer on the substrate; and

selectively etching the sacrificial layer with respect to the buffer oxide liner and the fin capping layer to form the dummy gate.

See Full Patent (Not Attached)

US 20110223735A1

(19) **United States**

(12) **Patent Application Publication**

(10) **Pub. No.: US 2011/0223735 A1**

(43) **Pub. Date: Sep. 15, 2011**

YU et al.

(54) **REDUCING RESISTANCE IN SOURCE AND DRAIN REGIONS OF FINFETS**

(75) Inventors: **CHEN-HUA YU**, HSIN-CHU (TW); **YU-RUNG HSU**, TAINAN (TW); **CHEN-NAN YEH**, HSI-CHIH (TW); **CHENG-HUNG CHANG**, HSIN-CHU (TW)

(73) Assignee: **TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.**, HSIN-CHU (TW)

(21) Appl. No.: **13/103,594**

(22) Filed: **May 9, 2011**

Related U.S. Application Data

(62) Division of application No. 11/873,156, filed on Oct. 16, 2007, now Pat. No. 7,939,889.

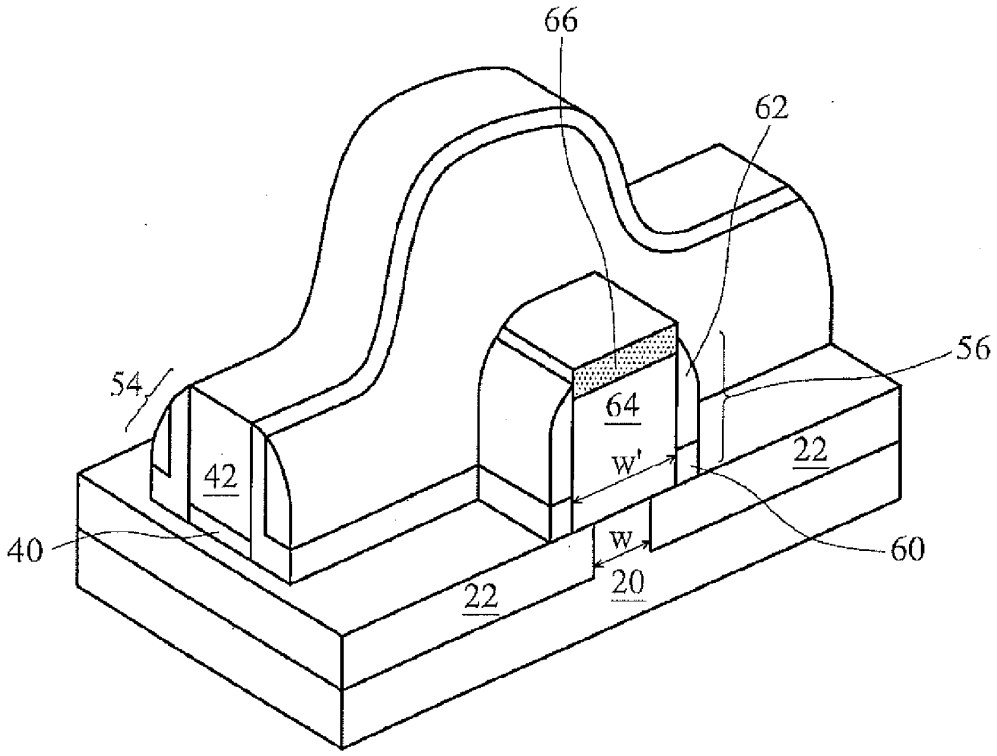
Publication Classification

(51) **Int. Cl.**
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H01L 21/20 (2006.01)

(52) **U.S. Cl.** **438/299**; 438/478; 257/E21.09; 257/E21.409

(57) **ABSTRACT**

A semiconductor structure includes a semiconductor fin on a top surface of a substrate, wherein the semiconductor fin includes a middle section having a first width; and a first and a second end section connected to opposite ends of the middle section, wherein the first and the second end sections each comprises at least a top portion having a second width greater than the first width. The semiconductor structure further includes a gate dielectric layer on a top surface and sidewalls of the middle section of the semiconductor fin; and a gate electrode on the gate dielectric layer.



INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99**)		
	Application Number	13992598
	Filing Date	2013-06-07
	First Named Inventor	Rosenbaum, Aaron W.
	Art Unit	2811
	Examiner Name	Unknown
	Attorney Docket Number	P38683US

U.S.PATENTS						
Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	6136697	A	2000-10-24	Wu	
	2	7456471	B2	2008-11-25	Anderson et al.	
	3	7528025	B2	2009-05-05	Brask et al.	
If you wish to add additional U.S. Patent citation information please click the Add button.						
U.S.PATENT APPLICATION PUBLICATIONS						
Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20020130372	A1	2002-09-19	Kwon et al.	
	2	20060189058	A1	2006-08-24	Lee et al.	
	3	20110147831	A1	2011-06-23	Steigerwald et al.	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.L.L.

Receipt date: 10/23/2013	Application Number	13992598	13992598 - GAU: 2817
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Filing Date	2013-06-07	
(Not for submission under 37 CFR 1.99)	First Named Inventor	Rosenbaum, Aaron W.	
	Art Unit	2811	
	Examiner Name	Unknown	
	Attorney Docket Number	P38683US	

	4	20080233699	A1	2008-09-25	Booth et al.	
	5	20100048007	A1	2010-02-25	Lee et al.	

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FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	100585178	KR	B1	2006-05-24	Kim et al.	English Abstract Submitted	☐
	2	10-0653711	KR	B1	2006-12-05	Kim et al.	English Abstract Submitted	☐
	3	10-2004-0050519	KR	A	2004-06-16	Lee	English Abstract Submitted	☐
	4	10-2008-0021918	KR	A	2008-03-10	Shin	English Abstract Submitted	☐
	5	2013/048449	WO	A1	2013-04-04	Pradhan et al.		☐
	6	2013/048516	WO	A1	2013-04-04	Rosenbaum et al.		☐
	7	2013/048524	WO	A1	2013-04-04	Pradhan et al.		☐

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Receipt date: 10/23/2013	Application Number	13992598 13992598 - GAU: 2817
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Filing Date	2013-06-07
(Not for submission under 37 CFR 1.99)	First Named Inventor	Rosenbaum, Aaron W.
	Art Unit	2811
	Examiner Name	Unknown
	Attorney Docket Number	P38683US

	8	2013/085490	WO	A1	2013-06-13	Pradhan et al.		☐

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NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	International Search Report and Written Opinion Received for PCT Patent Application No. PCT/US2011/054294, Mailed on May 15, 2012, 8 pages.	☐
	2	International Search Report and Written Opinion Received for PCT Patent Application No. PCT/US2011/054464, Mailed on May 15, 2012, 9 pages.	☐
	3	International Search Report and Written Opinion Received for PCT Patent Application No. PCT/US2011/054479, Mailed on May 16, 2012, 9 pages.	☐
	4	International Search Report and Written Opinion Received for PCT Patent Application No. PCT/US2011/063433, Mailed on July 20, 2012, 9 pages.	☐

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EXAMINER SIGNATURE

Examiner Signature	/Samuel Lair/	Date Considered	04/14/2015

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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Receipt date: 10/23/2013	Application Number	13992598	13992598 - GAU: 2817
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Filing Date	2013-06-07	
	First Named Inventor	Rosenbaum, Aaron W.	
	Art Unit	2811	
	Examiner Name	Unknown	
	Attorney Docket Number	P38683US	

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Robert G. Winkle/	Date (YYYY-MM-DD)	2013-10-23
Name/Print	Robert G. Winkle	Registration Number	37,474

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

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3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Aaron W. Rosenbaum et al.	Examiner: Samuel L. Lair
Serial No.:	13/992,598	Group Art Unit: 2817
Filed:	June 7, 2013	Docket No.: P38683US

Title: CAPPING DIELECTRIC STRUCTURE FOR TRANSISTOR GATES

AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Applicant has reviewed the Office Action mailed on April 21, 2015. Please amend the above-identified patent application as follows.

IN THE CLAIMS

Please amend the claims as follows:

1.-14. (Canceled)

15. (Original) A method comprising:

forming a sacrificial non-planar transistor gate over a non-planar transistor fin;

depositing a dielectric material layer over the sacrificial non-planar transistor gate and the non-planar transistor fin;

forming non-planar transistor gate spacers from a portion of the dielectric material layer adjacent the sacrificial non-planar transistor gate;

forming a source/drain region;

removing the sacrificial non-planar transistor gate to form a gate trench between the non-planar transistor gate spacers and expose a portion of the non-planar transistor fin;

forming a gate dielectric adjacent the non-planar transistor fin within the gate trench;

depositing conductive gate material within the gate trench;

removing a portion of the conductive gate material to form a recess between the non-planar transistor gate spacers;

forming a capping dielectric structure within the recess by high density plasma depositing a dielectric material;

forming at least one dielectric material over the source/drain region, the non-planar transistor gate spacers, and the capping dielectric structure; and

forming a contact opening through the at least one dielectric material to expose at least a portion of the source/drain region.

16. (Original) The method of claim 15, wherein high density plasma depositing the capping dielectric structure comprises high density plasma depositing a silicon nitride capping dielectric structure.

17. (Original) The method of claim 15, wherein high density plasma depositing the capping dielectric structure comprises high density plasma depositing a silicon carbide capping dielectric structure.

18. (Original) The method of claim 15, wherein high density plasma depositing the capping dielectric structure comprises high density plasma depositing the capping dielectric structure at a temperature between about 300 °C and 600°C.

19. (Original) The method of claim 15, wherein forming a capping dielectric structure comprises:

high density plasma depositing capping dielectric material within the recess; and

removing excess capping dielectric material.

20. (Original) The method of claim 15, wherein forming a contact opening through the dielectric material to expose at least a portion of the source/drain region further comprises forming a contact opening through the dielectric material which exposes at least a portion of the source/drain region and at least a portion of one non-planar transistor gate spacer.

21. (Original) The method of claim 20, further comprising forming a source/drain contact to abut the exposed portion of the source/drain region and exposed portion of the non-planar transistor gate spacer.

22. (Original) The method of claim 15, wherein forming a contact opening through the dielectric material to expose at least a portion of the source/drain region further comprises forming a contact opening through the dielectric material which exposes at least a portion of the source/drain region and at least a portion of the capping dielectric structure.

23. (Original) The method of claim 22, further comprising forming a source/drain contact abuts the exposed portion of the source/drain region and the exposed portion of the capping dielectric structure.

24. (Original) The method of claim 15, wherein forming a contact opening through the dielectric material to expose at least a portion of the source/drain region further comprises forming a contact opening through the dielectric material exposes at least a portion of the source/drain region, at least a portion of the non-planar transistor gate spacer, and at least a portion of the capping dielectric structure.

25. (Original) The method of claim 24, further comprising forming a source/drain contact to abut the exposed portion of the source/drain region, the exposed portion of non-planar gate spacer, and the exposed portion of the capping dielectric structure.

REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on April 21, 2015, and the references cited therewith.

Claims 1-14 are canceled without prejudice to be pursued in a continuation application.

Claims 15-25 are now pending in this application.

Allowable Subject Matter

Claims 15-25 are allowed.

35 USC § 112 Rejection of the Claims

Claims 10-14 are rejected under 35 USC 112(b) or 35 USC 112 (pre-AIA), second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor, or for pre-AIA the applicant regards as the invention.

Claims 10-14 have been canceled without prejudice to be pursued in a continuation application. Therefore, the current rejection is moot.

35 USC § 102 Rejection of the Claims

> A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Claims 1, 2, 4-6, 8, and 9 - Liaw

Claims 1, 2, 4-6, 8, and 9 were rejected under 35 U.S.C. § 102(b) as being anticipated by US 2006/0046449 by Liaw (hereinafter "the Liaw publication").

Claims 1, 2, 4-6, 8, and 9 have been canceled without prejudice to be pursued in a continuation application. Therefore, the current rejection is moot.

Claims 1, 3-5, and 7-9 - Bohr

Claims 1, 3-5, and 7-9 were rejected under 35 U.S.C. § 102(e) as being anticipated by US 2011/0156107 by Bohr et al. (hereinafter "the Bohr publication").

Claims 1, 3-5, and 7-9 have been canceled without prejudice to be pursued in a continuation application. Therefore, the current rejection is moot.

35 USC § 103 Rejection of the Claims

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Claims 10-14 - Bohr in view of Sunayama

Claims 10-14 was rejected under 35 USC § 103(a) as being unpatentable over the Bohr publication in view of U.S. Patent Publication US 2011/0034026 by Sunayama et al. (hereinafter "the Sunayama publication").

Claims 10-14 have been canceled without prejudice to be pursued in a continuation application. Therefore, the current rejection is moot.

RESERVATION OF RIGHTS

In the interest of clarity and brevity, Applicant may not have addressed every assertion made in the Office Action. Applicant's silence regarding any such assertion does not constitute any admission or acquiescence. Applicant reserves all rights not exercised in connection with this response, such as the right to challenge or rebut any tacit or explicit characterization of any

reference or of any of the present claims, the right to challenge or rebut any asserted factual or legal basis of any of the rejections, the right to swear behind any cited reference such as provided under 37 C.F.R. § 1.131 or otherwise, or the right to assert co-ownership of any cited reference. Applicant does not admit that any of the cited references or any other references of record are relevant to the present claims, or that they constitute prior art. To the extent that any rejection or assertion is based upon the Examiner's personal knowledge, rather than any objective evidence of record as manifested by a cited prior art reference, Applicant timely objects to such reliance on Official Notice, and reserves all rights to request that the Examiner provide a reference or affidavit in support of such assertion, as required by MPEP § 2144.03. Applicant reserves all rights to pursue any cancelled claims in a subsequent patent application claiming the benefit of priority of the present patent application, and to request rejoinder of any withdrawn claim, as required by MPEP § 821.04.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (208) 850-3104 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 50-4238.

Respectfully submitted,

REINHARD MAHNKOPF ET AL.

By their Representatives

CUSTOMER NUMBER: 92265
(208) 850-3104

Date July 14, 2015

By /Robert G. Winkle, Reg. No. 37,474/
Robert G. Winkle
Reg. No. 37,474

Electronic Acknowledgement Receipt	
EFS ID:	22911677
Application Number:	13992598
International Application Number:	
Confirmation Number:	5215
Title of Invention:	CAPPING DIELECTRIC STRUCTURE FOR TRANSISTOR GATES
First Named Inventor/Applicant Name:	Aaron W. Rosenbaum
Customer Number:	92265
Filer:	Robert G. Winkle
Filer Authorized By:	
Attorney Docket Number:	P38683US
Receipt Date:	14-JUL-2015
Filing Date:	07-JUN-2013
Time Stamp:	14:14:53
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		P38683US_NFOAR.pdf	135394 37892e82418ce8738190fe441453d69b92a719a7	yes	8

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Claims	2	4
	Applicant Arguments/Remarks Made in an Amendment	5	8
Warnings:			
Information:			
	Total Files Size (in bytes):	135394	

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/992,598	Filing Date 06/07/2013	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)		
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	07/14/2015	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 11	Minus	** 25	= 0	X $80 =	0
	Independent (37 CFR 1.16(h))	* 1	Minus	***4	= 0	X $420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/ALLYSON PURNELL/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/SB/08a (01-10)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	13992598
	Filing Date	2013-06-07
	First Named Inventor	Aaron W. Rosenbaum
	Art Unit	2817
	Examiner Name	Samuel L. Lair
	Attorney Docket Number	P38683US

U.S.PATENTS						Remove
Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	6030692	A	2000-02-29	Auger, Thomas J.	
	2	6617226	B1	2003-09-09	Suguro, et al.	
	3	6720261	B1	2004-04-13	Anderson, et al.	
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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20040203211	A1	2004-10-14	Yang, et al.	
	2	20070066184	A1	2007-03-22	Nagamoto, et al.	
	3	20080290380	A1	2008-11-27	Sheu, et al.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
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	Filing Date	2013-06-07
	First Named Inventor	Aaron W. Rosenbaum
	Art Unit	2817
	Examiner Name	Samuel L. Lair
	Attorney Docket Number	P38683US

	4	20090081836	A1	2009-03-26	Liu, et al.	
	5	20090142991	A1	2009-06-04	Moon, Do Min	
	6	20110108930	A1	2011-05-12	Cheng, et al.	
	7	20110151250	A1	2011-06-23	Yasuda, et al.	
	8	20110217541	A1	2011-09-08	Shimano, et al.	
	9	20110281509	A1	2011-11-17	Tanaka, et al.	
	10	20130334713	A1	2013-12-19	Xu, et al.	
	11	20150155385	A1	2015-06-04	Pradhan, et al.	

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	10-2007-0122319	KR	A	2007-12-31	Jeon, et al.	English Abstract Submitted.	☐

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	13992598
	Filing Date	2013-06-07
	First Named Inventor	Aaron W. Rosenbaum
	Art Unit	2817
	Examiner Name	Samuel L. Lair
	Attorney Docket Number	P38683US

	2	10-2009-0012793	KR	A	2009-02-04	Jang, et al.	English Abstract Submitted.	☐
	3	201110324	TW	A	2011-03-16	Xu, et al.	English Abstract Submitted.	☐
	4	201123448	TW	A	2011-07-01	Lim, et al.	English Abstract Submitted.	☐
	5	201208078	TW	A	2012-02-16	Chen, et al.	English Abstract Submitted.	☐
	6	201236153	TW	A	2012-09-01	Cai, et al.	English Abstract Submitted.	☐
	7	2013/095527	WO	A1	2013-06-27	Xu, et al.		☐

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T5
	1	Office Action received for Korean Patent Application No. 10-2014-7007165, mailed on April 14, 2015, 5 pages of Korean Office Action and 2 pages of English Translation.	☒
	2	Office Action received for Korean Patent Application No. 10-2014-7007872, mailed on April 28, 2015, 5 pages of Korean Office Action and 3 pages of English Translation.	☒
	3	Office Action received for Taiwan Patent Application No. 101134489, mailed on May 01, 2015, English summary of Office Action in a Reporting Letter, 3 pages of Taiwan Office Action including Search Report.	☐

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	13992598
	Filing Date	2013-06-07
	First Named Inventor	Aaron W. Rosenbaum
	Art Unit	2817
	Examiner Name	Samuel L. Lair
	Attorney Docket Number	P38683US

	4	Office Action received for Taiwan Patent Application No. 101135607, mailed on May 8, 2015, English summary of Office Action in a Reporting Letter, 5 pages of Taiwan Office Action and 1 page of English Search report.	☐
	5	Extended European Search Report received for European Patent Application No. 11873523.2, mailed on May 18, 2015, 8 pages.	☐
	6	International Preliminary Report on Patentability and Written Opinion received for PCT Patent Application No. PCT/US2011/066921, mailed on July 03, 2014, 14 pages.	☐
	7	International Search Report and Written Opinion received for PCT Patent Application No. PCT/US2011/066921, mailed on September 27, 2012, 11 pages.	☐

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EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	13992598
	Filing Date	2013-06-07
	First Named Inventor	Aaron W. Rosenbaum
	Art Unit	2817
	Examiner Name	Samuel L. Lair
	Attorney Docket Number	P38683US

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☐ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Robert G. Winkle/	Date (YYYY-MM-DD)	2015-07-16
Name/Print	Robert G. Winkle	Registration Number	37,474

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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

(19) KOREAN INTELLECTUAL PROPERTY OFFICE

KOREAN PATENT ABSTRACTS

(11) Publication number: 1020070122319 A
(43) Publication date: 31.12.2007

(21) Application number: 1020060057703
(22) Application date: 26.06.2006

(71) Applicant:
- SAMSUNG ELECTRONICS CO., LTD.

(72) Inventor:
- JEON, TAEK SOO
- CHO, HAG JU
- CHOI, SI YOUNG
- SHIN, YU GYUN
- KANG, SANG BOM

(51) Int. Cl:
H01L 21/336
H01L 29/78

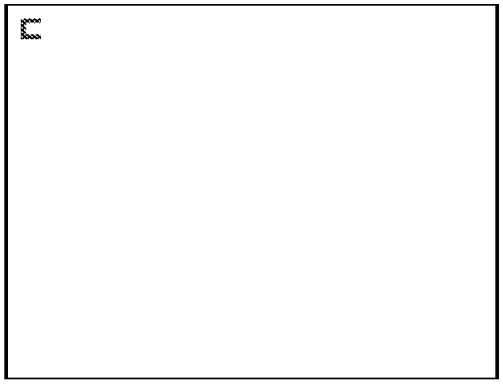
(54) SEMICONDUCTOR DEVICE AND A METHOD OF FABRICATING THE SAME BY INCREASING CONCENTRATION OF METAL ION OF A FIRST CONDUCTIVE LAYER AT A PORTION ADJACENT TO A GATE INSULATING LAYER

(57) Abstract:

PURPOSE: A semiconductor device and a fabricating method thereof are provided to minimize characteristic deterioration of a gate insulating layer and improve an operation efficiency of a gate electrode.

CONSTITUTION: A semiconductor substrate(410) has a first region (A) and a second region(B). Gate insulating layers are formed on the first region and the second region, and gate electrodes (422a,422b) are formed on the gate insulating layers, respectively. Each of the gate electrodes has a first conductive layer and a second conductive layer formed on the first conductive layer. The first conductive layer of the gate electrodes has an implanted metal ion, in which concentration of the metal ion is higher at a portion adjacent to the gate insulating layer.

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(19) 대한민국특허청(KR)
(12) 공개특허공보(A)

(11) 공개번호 10-2007-0122319
(43) 공개일자 2007년12월31일

(51) 국제특허분류(Int. Cl.)
H01L 21/336 (2006.01) *H01L 29/78* (2006.01)
(21) 출원번호 10-2006-0057703
(22) 출원일자 2006년06월26일
심사청구일자 없음

(71) 출원인
삼성전자주식회사
경기도 수원시 영통구 매탄동 416
(72) 발명자
전덕수
경기 용인시 수지구 풍덕천2동 태영 데시앙 2차 204동 802호
조학주
경기 용인시 죽전1동 현대홈타운4차1단지아파트 101동 803호
(총 2 명 생략)
(74) 대리인
권석수, 송윤호, 오세준

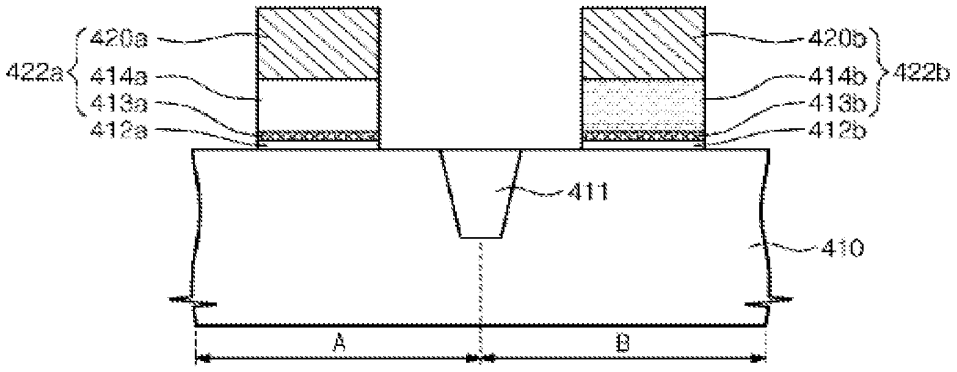
전체 청구항 수 : 총 31 항

(54) 발명의 명칭 반도체 소자 및 그 제조 방법

(57) 요 약

본 발명은 반도체 소자를 제공한다. 이 소자는 n모스 영역 및 p모스 영역을 갖는 반도체 기판, 및 n모스 영역 및 p모스 영역 상에 게이트 절연막을 상에 형성된 각각의 게이트 전극들을 포함하되, 게이트 전극들은 제 1 도전막 및 제 1 도전막 상의 제 2 도전막을 포함한다. n모스 영역 및 p모스 영역 중 적어도 하나의 영역의 게이트 전극들의 제 1 도전막은 주입된 금속 이온을 포함하되, 제 1 도전막은 게이트 절연막에 인접하는 부위에서 금속 이온의 농도가 높은 것을 특징으로 한다. 이에 따라, 게이트 절연막의 특성 저하를 최소화하는 동시에 게이트 전극의 동작 효율을 높임으로써, 적은 비용으로 품질이 우수한 반도체 소자를 제공할 수 있다.

대 표 도 : 도4d



(72) 발명자
최시영
경기 성남시 분당구 수내동 파크타운롯데아파트
137동 204호
신유균
경기 성남시 분당구 수내동 55번지 파크타운아파트
130-1401

강상범
서울특별시 서초구 반포동 1060번지 반포아파트 1
5동 202호

특허청구의 범위

청구항 1

제 1 영역 및 제 2 영역을 갖는 반도체 기판; 및

상기 제 1 영역 및 상기 제 2 영역 상의 게이트 절연막들 상에 형성된 각각의 게이트 전극들을 포함하되, 상기 게이트 전극들은 제 1 도전막 및 상기 제 1 도전막 상의 제 2 도전막을 포함하고, 상기 제 1 영역 및 상기 제 2 영역 중 적어도 하나의 영역의 상기 게이트 전극들의 상기 제 1 도전막은 주입된 금속 이온을 포함하며, 상기 제 1 도전막은 상기 게이트 절연막에 인접하는 부위에서 상기 금속 이온의 농도가 높은 것을 특징으로 하는 반도체 소자.

청구항 2

제 1항에 있어서,

상기 제 1 영역 및 상기 제 2 영역은 서로 반대되는 도전형인 것을 특징으로 하는 반도체 소자.

청구항 3

제 1항에 있어서,

상기 게이트 절연막은 실리콘 산화막 및 고유전막 중에서 선택된 적어도 하나의 막인 것을 특징으로 하는 반도체 소자.

청구항 4

제 1항에 있어서,

상기 제 1 도전막의 일함수는 상기 반도체 기판의 전도대와 가전자대 사이의 값을 갖는 것을 특징으로 하는 반도체 소자.

청구항 5

제 4항에 있어서,

상기 제 1 도전막은 도핑된 실리콘막, $Ta_xC_yN_z$막, $Ti_xC_yN_z$막 및 $W_xC_yN_z$막(x, y 및 z는 0 또는 양의 정수) 중에서 선택된 적어도 하나의 막 또는 이들이 조합된 막인 것을 특징으로 하는 반도체 소자.

청구항 6

제 1항에 있어서,

상기 제 1 도전막이 상기 도핑된 실리콘막이면,

상기 게이트 절연막 및 상기 제 1 도전막 사이에 개재되는 금속막을 더 포함하는 것을 특징으로 하는 반도체 소자.

청구항 7

제 6항에 있어서,

상기 금속막은 $Ta_xC_yN_z$막, $Ti_xC_yN_z$막 및 $W_xC_yN_z$막(x, y 및 z는 0 또는 양의 정수) 중에서 선택된 적어도 하나의 막 또는 이들이 조합된 막인 것을 특징으로 하는 반도체 소자.

청구항 8

제 6항에 있어서,

상기 금속막의 두께는 5~40Å인 것을 특징으로 하는 반도체 소자.

청구항 9

제 1항에 있어서,

상기 제 1 도전막에 주입된 상기 금속 이온은,

상기 제 1 영역 상의 상기 게이트 전극들의 상기 일함수를 낮추거나, 상기 제 2 영역 상의 상기 게이트 전극들의 상기 일함수를 높이는 것을 특징으로 하는 반도체 소자.

청구항 10

제 9항에 있어서,

상기 금속 이온은 상기 제 1 도전막의 성분과 다르되, 상기 제 1 도전막 내에서 이동 가능한 것을 특징으로 하는 반도체 소자.

청구항 11

제 10항에 있어서,

상기 금속 이온은 알루미늄, 하프늄, 지르코늄, 티타늄, 탄탈륨, 텅스텐, 프라세오디뮴, 란타늄, 란탄, 디로륨, 이테르븀, 디스프로슘, 가돌리늄, 플래티늄, 이리듐 및 루테늄 중에서 선택된 하나인 것을 특징으로 하는 반도체 소자.

청구항 12

제 1항에 있어서,

상기 제 2 도전막은 실리콘 또는 실리사이드를 포함하는 폴리막 및 금속 물질막 중에서 선택된 적어도 하나의 막 또는 이들이 조합된 막인 것을 특징으로 하는 반도체 소자.

청구항 13

제 1 영역 및 제 2 영역을 갖는 반도체 기판 상에 게이트 절연막 및 상기 게이트 절연막 상에 제 1 도전막을 형성하고;

상기 제 1 영역 및 상기 제 2 영역 중 선택된 하나의 영역 상의 상기 제 1 도전막을 노출하는 제 1 마스크 패턴을 형성하고;

상기 제 1 마스크 패턴을 마스크로 하는 제 1 이온 주입 공정으로 상기 선택된 영역 상의 상기 제 1 도전막에 금속 이온을 주입하고;

상기 제 1 마스크 패턴을 제거하고;

상기 제 1 도전막 상에 제 2 도전막을 형성하고; 그리고

상기 제 2 도전막, 상기 제 1 도전막 및 상기 게이트 절연막을 패터닝하여, 상기 제 1 영역 및 상기 제 2 영역 상에 각각의 게이트 전극들을 형성하는 것을 포함하되, 상기 선택된 영역의 상기 게이트 전극들의 상기 제 1 도전막은 상기 게이트 절연막에 인접하는 부위에서 상기 금속 이온의 농도가 높게 형성되는 것을 특징으로 하는 반도체 소자의 제조 방법.

청구항 14

제 13항에 있어서,

상기 제 1 영역 및 상기 제 2 영역은 서로 반대되는 도전형인 것을 특징으로 하는 반도체 소자의 제조 방법.

청구항 15

제 13항에 있어서,

상기 게이트 절연막은 실리콘 산화막 및 고유전막 중에서 선택된 적어도 하나의 막으로 형성되는 것을 특징으로 하는 반도체 소자의 제조 방법.

청구항 16

제 19항에 있어서,

상기 제 1 도전막의 일함수는 상기 반도체 기판의 전도대와 가전자대 사이의 값을 갖는 것을 특징으로 하는 반도체 소자의 제조 방법.

청구항 17

제 16항에 있어서,

상기 제 1 도전막은 도핑된 실리콘막, $Ta_xC_yN_z$막, $Ti_xC_yN_z$막 및 $W_xC_yN_z$막(x, y 및 z는 0 또는 양의 정수) 중에서 선택된 적어도 하나의 막 또는 이들이 조합된 막으로 형성되는 것을 특징으로 하는 반도체 소자의 제조 방법.

청구항 18

제 13항에 있어서,

상기 제 1 도전막이 상기 도핑된 실리콘막으로 형성되된,

상기 게이트 절연막 및 상기 제 1 도전막 사이에 금속막을 형성하는 것을 더 포함하는 것을 특징으로 하는 반도체 소자의 제조 방법.

청구항 19

제 18항에 있어서,

상기 금속막은 $Ta_xC_yN_z$막, $Ti_xC_yN_z$막 및 $W_xC_yN_z$막(x, y 및 z는 0 또는 양의 정수) 중에서 선택된 적어도 하나의 막 또는 이들이 조합된 막으로 형성되는 것을 특징으로 하는 반도체 소자의 제조 방법.

청구항 20

제 18항에 있어서,

상기 금속막의 두께는 5~40Å인 것을 특징으로 하는 반도체 소자의 제조 방법.

청구항 21

제 13항에 있어서,

상기 제 1 마스크 패턴을 형성하기 전에 상기 제 1 도전막 상에 희생막을 형성하는 것: 그리고

상기 희생막을 제거하는 것을 더 포함하는 것을 특징으로 하는 반도체 소자의 제조 방법.

청구항 22

제 21항에 있어서,

상기 희생막은 실리콘을 포함하는 물질막 및 금속 물질막 중에서 선택된 적어도 하나의 막 또는 이들이 조합된 막으로 형성되는 것을 특징으로 하는 반도체 소자의 제조 방법.

청구항 23

제 22항에 있어서,

상기 실리콘을 포함하는 물질막은 실리콘막, 실리콘 산화막 및 실리콘 질화막 중에서 선택된 적어도 하나의 막 또는 이들이 조합된 막으로 형성되는 것을 특징으로 하는 반도체 소자의 제조 방법.

청구항 24

제 22항에 있어서,

상기 금속 물질막은 실리콘 및 질소 중에서 선택된 적어도 하나의 성분을 포함하는 것을 특징으로 하는 반도체 소자의 제조 방법.

청구항 25

제 24항에 있어서,

상기 금속 물질막은 티타늄 질화막, 탄탈륨 질화막, 텅스텐 질화막, 티타늄 실리사이드막, 탄탈륨 실리사이드막, 텅스텐 실리사이드막, 티탄 실리콘 질화막, 탄탈 실리콘 질화막 및 텅스텐 실리콘 질화막 중에서 선택된 하나의 막 또는 이들이 조합된 막으로 형성되는 것을 특징으로 하는 반도체 소자의 제조 방법.

청구항 26

제 21항에 있어서,

상기 희생막을 처리하는 것은,

상기 희생막을 제거하는 공정, 열 처리하는 공정, 플라즈마 처리하는 공정 및 대기 중에 노출하는 공정 중에서 선택된 적어도 하나의 공정이 수행되는 것을 포함하는 것을 특징으로 하는 반도체 소자의 제조 방법.

청구항 27

제 13항에 있어서,

상기 제 1 마스크 패턴을 제거한 후,

상기 제 1 영역 및 상기 제 2 영역 중 선택되지 않은 영역 상의 상기 제 1 도전막을 노출하는 제 2 마스크 패턴을 형성하고;

상기 제 2 마스크 패턴을 마스크로 하는 제 2 이온 주입 공정으로 상기 선택되지 않은 영역 상의 상기 제 1 도전막에 상기 금속 이온을 주입하고; 그리고

상기 제 2 마스크 패턴을 제거하는 것을 더 포함하는 것을 특징으로 하는 반도체 소자의 제조 방법.

청구항 28

제 13항에 있어서,

상기 제 1 도전막에 상기 금속 이온을 주입함으로써,

상기 제 1 영역 상에 형성된 상기 게이트 전극들의 상기 일함수가 낮아지거나, 상기 제 2 영역 상에 형성된 상기 게이트 전극들의 상기 일함수가 높아지는 것을 특징으로 하는 반도체 소자의 제조 방법.

청구항 29

제 28항에 있어서,

상기 금속 이온은 상기 제 1 도전막의 성분과 다르되, 상기 제 1 도전막 내에서 이동 가능한 것을 특징으로 하는 반도체 소자의 제조 방법.

청구항 30

제 28항에 있어서,

상기 금속 이온은 알루미늄, 하프늄, 지르코늄, 티타늄, 탄탈륨, 텅스텐, 프라세오디뮴, 랜타늄, 란탄, 테르븀, 이테르븀, 디스프로슘, 가돌리늄, 플래티늄, 이리듐 및 루테늄 중에서 선택된 하나인 것을 특징으로 하는 반도체 소자의 제조 방법.

청구항 31

제 13항에 있어서,

상기 제 2 도전막은 실리콘 또는 실리사이드를 포함하는 물질막 및 금속 물질막 중에서 선택된 적어도 하나의 막 또는 이들이 조합된 막으로 형성되는 것을 특징으로 하는 반도체 소자의 제조 방법.

명 세 서

발명의 상세한 설명

발명의 목적

발명이 속하는 기술 및 그 분야의 종래기술

[0005] 본 발명은 반도체 소자 및 그 제조 방법에 관한 것으로, 더 구체적으로 게이트 전극을 포함하는 반도체 소자 및 그 제조 방법에 관한 것이다.

[0006] 최근 반도체 소자의 급격한 디자인 룰(design rule) 감소에 따라 모스펫(Metal-Oxide-Semiconductor Field Effect Transistor : MOSFET) 소자에 사용되는 게이트 절연막에 고유전율(high-k) 물질을 적용하고자 하는 연구가 급속도로 진행되고 있다. 고유전율 물질을 게이트 절연막으로 사용할 경우, 동일한 등가 산화막 두께(Equivalent Oxide Thickness : EOT)를 갖는 고유전율 물질은 실리콘 산화막(SiO2)에 비해 물리적으로 두께를 두껍게 증착할 수 있다. 이에 따라, 게이트 절연막으로 20Å 이하의 두께를 갖는 실리콘 산화막을 사용하는 경우, 전자의 터널링(tunneling)에 의해 발생하는 급격한 누설 전류(leakage current)의 증가를 줄일 수 있다. 이와 같이, 50nm 디자인 룰이 적용되는 반도체 소자는 등가 산화막 두께가 20Å 이하에서도 원하는 소자 특성을 확보할 수 있는 새로운 고유전율 물질이 필요하며, 이에 대한 방안으로 하프늄 베이스(Hf-based) 고유전율 물질에 대한 연구가 반도체 소자 제조사들에 의해 적극적으로 진행되고 있다.

[0007] 그러나 종래 실리콘(polysilicon)을 게이트 전극으로 사용하는 기존의 씨모스 제조 공정에 고유전율 물질을 게이트 절연막으로 사용하게 되면, 소위 페르미 레벨 피닝(Fermi level pinning)이라 불리는 현상에 의해 종래 실리콘에 주입되는 도펀트(dopant)에 의한 게이트 절연막의 플랫 밴드 전압(Vfb : flat band voltage)을 조절하는 것이 어려워지는 문제점이 있다. 이러한 문제점을 해결하기 위한 금속 물질을 이용한 게이트 전극의 개발 및 응용이 활발하다. 금속 물질을 게이트 전극으로 사용하면, 페르미 레벨 피닝 현상에 의한 문제점을 최소화하거나 없앨 수 있다. 또한, 금속 물질을 게이트 전극으로 사용하면, 종래 실리콘이 게이트 전극일 때 채널 반전(channel inversion) 영역에서 발생하는 게이트 공핍 효과(gate depletion effect)에 의한 등가 산화막 두께의 증가를 없앨 수 있다. 이에 따라, 게이트 절연막의 실질적인 두께를 감소시킬 수 있는 효과가 있다. 이에 더하여, 금속 물질의 낮은 저항 특성을 활용할 수 있으며, 소오스/드레인 영역을 형성하기 위한 불순물 주입 공정에서 불순물이 확산되는 것을 방지할 수 있다. 게다가, 전하 포획(charge trapping) 현상 및 원격 전하 산란(remote charge scattering) 효과를 감소시켜, 전하의 이동도(mobility)를 향상시킬 수 있다.

[0008] 금속 물질의 이러한 장점들에도 불구하고, 실제 게이트 전극으로 사용하기 위해서는 많은 문제점이 뒤따르고 있다. 예를 들면, n모스용 금속 물질의 특성(n모스용 게이트 전극에 적합한 일함수 값을 갖는 금속 물질은 반응성이 크기 때문에, 열적으로 불안정하다.)와 두 금속 물질을 반도체 소자에 동일하는 공정의 복잡성 때문에, n모스용 게이트 전극은 폴리 실리콘이, p모스용 게이트 전극은 금속 물질이 각각 사용된다. n모스용 게이트 전극에서 폴리 공핍이 발생하여 금속 전극의 장점인 등가 산화막 두께의 감소 효과를 얻을 수 없다.

[0009] 한편, n모스용 및 p모스용 금속 물질을 반도체 소자에 통합하는 경우, 통상적으로 n모스용 혹은 p모스용 금속 물질을 전면 증착한 후, 일부를 제거한다. 이때, 일부 제거된 금속 물질 하부의 게이트 절연막은 대기 중에 노출된다. 이어서, 다른 금속 물질을 증착한다. 이에 따라, 금속 물질의 제거와 다른 금속 물질의 증착 과정 중에, 게이트 절연막은 물리적 또는 화학적 손상을 입게 된다. 이러한 게이트 절연막의 손상으로 인해 게이트 절연막의 특성이 저하되는 문제점이 있다.

[0010] 폴리 실리콘에 의한 게이트 공핍 효과를 줄이기 위해서, 게이트 절연막과 폴리 실리콘 사이에 매우 얇은 금속막(20Å 이하)을 개재하는 금속막을 개재한 폴리 실리콘막 구조(Metal Inserted Polysilicon Structure : MIPS)가 사용될 수 있다. 이러한 금속막을 개재한 폴리 실리콘막 구조는 게이트 전극으로 금속 물질을 사용할 때 발생하는 건식 식각에 의한 문제점을 줄여 줄 수 있다. 또한, 게이트 전극으로 폴리 실리콘을 사용할 때 발생하는 등가 산화막 두께의 감소도 줄일 수 있다. 그러나 금속막을 개재한 폴리 실리콘막 구조도 앞서 언급한 페르미 레벨 피닝 현상을 막지는 못한다. 이에 따라, 금속막을 개재한 폴리 실리콘막 구조를 갖는 반도체 소자는 높은 임계 전압(Vth : threshold voltage)을 갖는 문제점이 있다.

발명이 이루고자 하는 기술적 과제

[0011] 본 발명이 이루고자 하는 기술적 과제는 게이트 절연막의 특성 저하를 최소화하는 동시에 게이트 전극의 동작

효율을 높일 수 있는 반도체 소자를 제공하는 데 있다.

[0012] 또한, 본 발명이 이루고자 하는 다른 기술적 과제는 제어된 절연막의 특성 저하를 최소화하는 동시에 게이트 전극의 동작 효율을 높일 수 있는 반도체 소자의 제조 방법을 제공하는 데 있다.

발명의 구성 및 작용

[0013] 상기한 기술적 과제를 달성하기 위하여, 본 발명은 반도체 소자를 제공한다. 이 소자는 n모스 영역 및 p모스 영역을 갖는 반도체 기판, 및 n모스 영역 및 p모스 영역 상의 제어된 절연막들 상에 형성된 각각의 게이트 전극들을 포함하되, 게이트 전극들은 제 1 도전막 및 제 1 도전막 상의 제 2 도전막을 포함한다. n모스 영역 및 p모스 영역 중 적어도 하나의 영역의 게이트 전극들의 제 1 도전막은 주입된 금속 이온을 포함하되, 제 1 도전막은 게이트 절연막에 인접하는 부위에서 금속 이온의 농도가 높은 것을 특징으로 한다.

[0014] n모스 영역 및 p모스 영역은 서로 분리되는 도전형일 수 있다.

[0015] 게이트 절연막은 실리콘 산화막 및 고유전막 중에서 선택된 적어도 하나의 막일 수 있다.

[0016] 제 1 도전막의 일함수는 반도체 기판의 전도대와 가전자대 사이의 값을 가질 수 있다. 제 1 도전막은 도핑된 실리콘막, $Ta_xC_yN_z$막, $Ti_xC_yN_z$막 및 $W_xC_yN_z$막(x, y 및 z는 0 또는 양의 정수) 중에서 선택된 적어도 하나의 막 또는 이들이 조합된 막일 수 있다.

[0017] 제 1 도전막이 도핑된 실리콘막이면, 게이트 절연막 및 제 1 도전막 사이에 개재되는 금속막을 더 포함할 수 있다.

[0018] 금속막은 $Ta_xC_yN_z$막, $Ti_xC_yN_z$막 및 $W_xC_yN_z$막(x, y 및 z는 0 또는 양의 정수) 중에서 선택된 적어도 하나의 막 또는 이들이 조합된 막일 수 있다. 금속막의 두께는 5~80Å일 수 있다.

[0019] 제 1 도전막에 주입된 금속 이온은 n모스 영역 상의 게이트 전극들의 일함수를 낮추거나, p모스 영역 상의 게이트 전극들의 일함수를 높일 수 있다.

[0020] 금속 이온은 제 1 도전막의 성분과 다르되, 제 1 도전막 내에서 이동 가능할 수 있다. 금속 이온은 알루미늄, 하프늄, 지르코늄, 티타늄, 탄탈륨, 텅스텐, 프라세오디뮴, 엘리븀, 란탄, 테르븀, 이테르븀, 디스프로슘, 가돌리늄, 플래티늄, 이리듐 및 루테늄 중에서 선택된 하나일 수 있다.

[0021] 제 2 도전막은 실리콘 또는 실리사이드를 포함하는 물질막 및 금속 물질막 중에서 선택된 적어도 하나의 막 또는 이들이 조합된 막일 수 있다.

[0022] 또한, 상기한 다른 기술적 과제를 달성하기 위하여, 본 발명은 반도체 소자의 제조 방법을 제공한다. 이 방법에 따르면, n모스 영역 및 p모스를 갖는 반도체 기판 상에 게이트 절연막 및 게이트 절연막 상에 제 1 도전막을 형성하는 것, n모스 영역 및 p모스 영역 중 선택된 하나의 영역 상의 제 1 도전막을 노출하는 제 1 마스크 패턴을 형성하는 것, 제 1 마스크 패턴을 마스크로 하는 제 1 이온 주입 공정으로 선택된 영역 상의 제 1 도전막에 금속 이온을 주입하는 것, 제 1 마스크 패턴을 제거하는 것, 제 1 도전막 상에 제 2 도전막을 형성하는 것, 그리고 제 2 도전막, 제 1 도전막 및 게이트 절연막을 패터닝하여 n모스 영역 및 p모스 영역 상에 각각의 게이트 전극들을 형성하는 것을 포함한다. 선택된 영역의 게이트 전극들의 제 1 도전막은 게이트 절연막에 인접하는 부위에서 금속 이온의 농도가 높게 형성되는 것을 특징으로 한다.

[0023] n모스 영역 및 p모스 영역은 서로 분리되는 도전형일 수 있다.

[0024] 게이트 절연막은 실리콘 산화막 및 고유전막 중에서 선택된 적어도 하나의 막으로 형성될 수 있다.

[0025] 제 1 도전막의 일함수는 반도체 기판의 전도대와 가전자대 사이의 값을 가질 수 있다. 제 1 도전막은 도핑된 실리콘막, $Ta_xC_yN_z$막, $Ti_xC_yN_z$막 및 $W_xC_yN_z$막(x, y 및 z는 0 또는 양의 정수) 중에서 선택된 적어도 하나의 막 또는 이들이 조합된 막으로 형성될 수 있다.

[0026] 제 1 도전막이 도핑된 실리콘막으로 형성되면, 게이트 절연막 및 제 1 도전막 사이에 금속막을 형성하는 것을 더 포함할 수 있다.

[0027] 금속막은 $Ta_xC_yN_z$막, $Ti_xC_yN_z$막 및 $W_xC_yN_z$막(x, y 및 z는 0 또는 양의 정수) 중에서 선택된 적어도 하나의 막 또는 이들이 조합된 막으로 형성될 수 있다. 금속막의 두께는 5~80Å일 수 있다.

[0028] 제 1 마스크 패턴을 형성하기 전에 제 1 도전막 상에 희생막을 형성하는 것, 그리고 희생막을 처리하는 것을 더 포함할 수 있다.

[0029] 희생막은 실리콘을 포함하는 물질막 및 금속 물질막 중에서 선택된 적어도 하나의 막 또는 이들이 조합된 막으로 형성될 수 있다.

[0030] 실리콘을 포함하는 물질막은 실리콘막, 실리콘 산화막 및 실리콘 질화막 중에서 선택된 적어도 하나의 막 또는 이들이 조합된 막으로 형성될 수 있다.

[0031] 금속 물질막은 실리콘 및 질소 중에서 선택된 적어도 하나의 성분을 포함할 수 있다.

[0032] 금속 물질막은 티타늄 질화막, 탄탈륨 질화막, 텅스텐 질화막, 티타늄 실리사이드막, 탄탈륨 실리사이드막, 텅스텐 실리사이드막, 티탄 실리콘 질화막, 탄탈 실리콘 질화막 및 텅스텐 실리콘 질화막 중에서 선택된 하나의 막 또는 이들이 조합된 막으로 형성될 수 있다.

[0033] 희생막을 처리하는 것은 희생막을 제거하는 공정, 열 처리하는 공정, 플라즈마 처리하는 공정 및 대기 중에 노출하는 공정 중에서 선택된 적어도 하나의 공정이 수행되는 것을 포함할 수 있다.

[0034] 제 1 마스크 패턴을 제거한 후, n모스 영역 및 p모스 영역 중 선택되지 않은 영역 상의 제 1 도전막을 노출하는 제 2 마스크 패턴을 형성하는 것, 제 2 마스크 패턴을 마스크로 하는 제 2 이온 주입 공정으로 선택되지 않은 영역 상의 제 1 도전막에 금속 이온을 주입하는 것, 그리고 제 2 마스크 패턴을 제거하는 것을 더 포함할 수 있다.

[0035] 제 1 도전막에 금속 이온을 주입함으로써, n모스 영역 상에 형성된 게이트 전극들의 일함수가 낮아지거나, p모스 영역 상에 형성된 게이트 전극들의 일함수가 높아질 수 있다.

[0036] 금속 이온은 제 1 도전막의 성분과 다르며, 제 1 도전막 내에서 이동 가능할 수 있다. 금속 이온은 알루미늄, 하프늄, 지르코늄, 티타늄, 탄탈륨, 텅스텐, 프라세오디뮴, 란탄, 테르븀, 이테르븀, 디스프로슘, 가돌리늄, 플래티늄, 이리듐 및 루테늄 중에서 선택된 하나일 수 있다.

[0037] 제 2 도전막은 실리콘 또는 실리사이드를 포함하는 물질막 및 금속 물질막 중에서 선택된 적어도 하나의 막 또는 이들이 조합된 막으로 형성될 수 있다.

[0038] 이하, 첨부된 도면들을 참조하여 본 발명의 바람직한 실시예를 상세히 설명하기로 한다. 그러나 본 발명은 여기서 설명되는 실시예에 한정되지 않고 다른 형태로 구체화될 수도 있다. 오히려, 여기서 소개되는 실시예는 제시된 내용이 철저하고 완전해질 수 있도록 그리고 당업자에게 본 발명의 사상이 충분히 전달될 수 있도록 하기 위해 제공되는 것이다. 또한, 바람직한 실시예에 따른 것이기 때문에, 설명의 순서에 따라 제시되는 참조 부호는 그 순서에 반드시 한정되지는 않는다. 도면들에 있어서, 막 및 영역들의 두께는 명확성을 기하기 위하여 과장된 것이다. 또한, 막이 다른 막 또는 기판 상에 있다고 언급되는 경우에 그것은 다른 막 또는 기판 상에 직접 형성될 수 있거나 또는 그들 사이에 제 3의 막이 개재될 수도 있다.

[0039] 도 1a 내지 도 1d는 본 발명의 일 실시예에 따른 반도체 소자의 게이트 전극을 제조하는 방법을 설명하기 위한 단면도들이다.

[0040] 도 1a를 참조하면, 제 1 영역(A) 및 제 2 영역(B)을 갖는 반도체 기판(110) 상에 게이트 절연막(112)을 형성한다. 제 1 영역(A) 및 제 2 영역(B)은 소자 분리막(111)에 의해 구분될 수 있으며, 서로 반대되는 도전형일 수 있다. 즉, 제 1 영역(A)이 n모스 영역이면, 제 2 영역(B)은 p모스 영역일 수 있다. 이와 반대로, 제 1 영역(A)이 p모스 영역이면, 제 2 영역(B)은 n모스 영역일 수 있다. 본 발명의 실시예에서는 제 1 영역(A) 및 제 2 영역(B)을 각각 n모스 영역 및 p모스 영역으로 설정하여 설명한다.

[0041] 게이트 절연막(112)은 실리콘 산화막 및 고유전막 중에서 선택된 적어도 하나의 막일 수 있다. 실리콘 산화막은 열 산화(thermal oxidation) 방식 또는 화학적 기상 증착(CVD : Chemical Vapor Deposition) 방식으로 형성될 수 있다. 고유전막은 고유전율 물질로써, 하프늄 산화막(HfO_2), 지르코늄 산화막(ZrO_2), 티타늄 산화막(TiO_2), 알루미늄 산화막(Al_2O_3), 탄탈륨 산화막(Ta_2O_5), 니오븀 산화막(Nb_2O_5), 프라세오디뮴 산화막(Pr_2O_3), 세륨 산화막(Ce_2O_3), 디스프로슘 산화막(Dy_2O_3), 에르븀 산화막(Er_2O_3), 이트륨 산화막(Y_2O_3), 지르코늄 실리콘 산화막($ZrSiO_4$), 지르코늄 실리콘 산화 질화막($ZrSiON$), 하프늄 실리콘 산화막($HfSiO$), 하프늄 실리콘 산화 질화막($HfSiON$), 하프늄 알루미늄 산화막($HfAlO$), 하프늄 알루미늄 산화 질화막($HfAlON$), 알루미늄 실리콘 산화 질화

막(Al$_2$O$_3$), 바륨 스트론튬 산화막(BaSrO$_3$), 바륨 스트론튬 산화막(BaSrO$_3$), BST막(Ba,Sr)TiO$_3$) 및 PZT막(Pb(Zr,Ti)O$_3$) 중에서 선택된 적어도 하나의 막일 수 있다.

[0042] 게이트 절연막(112) 상에 제 1 도전막(114)을 형성한다. 제 1 도전막(114)은 반도체 기판(110)의 전도대(conduction band)와 가전자대(valence band) 사이의 일함수(work function) 값을 가질 수 있다. 바람직하게는 제 1 도전막(114)은 3.8~5.2eV 범위의 일함수 값을 가질 수 있다. 제 1 도전막(114)은 도핑된 실리콘막(doped Si), $Ta_xC_yN_z$막, $Ti_xC_yN_z$막 및 $W_xC_yN_z$막(x, y 및 z는 0 또는 양의 정수) 중에서 선택된 적어도 하나의 막 또는 이들이 조합된 막일 수 있다. 본 발명의 실시예에서의 제 1 도전막(114)은 4.3eV 근처의 n모스형(nMOS dimension) 일함수 값을 가지는 탄탈륨 탄화막(TaC)일 수 있다.

[0043] 도핑된 실리콘은 주로 n형 도전성을 띄는 불순물인 인(P, phosphorous)을 주입하여 형성할 수 있다. 이는 앞서 종래기술에서 설명한 바와 같이, n모스용 게이트 전극에 적합한 일함수 값을 갖는 금속 물질은 반응성이 크기 때문이다. 이러한 큰 반응성으로 인해 n모스용 게이트 전극에 적합한 금속 물질이 거의 없는 상황이다.

[0044] $Ta_xC_yN_z$막, $Ti_xC_yN_z$막 및 $W_xC_yN_z$막(x, y 및 z는 0 또는 양의 정수)과 같은 금속 물질은 저밀화(densification) 및 탄소(C)와 질소(N)의 조성을 조절하기 위한 열 처리 또는 플라즈마 처리 공정이 추가적으로 수행될 수 있다.

[0045] 제 1 도전막(114) 상에 희생막(116)을 형성한다. 희생막(116)은 추후 공정인 금속 이온을 주입하는 공정(도 1b 참조)에서 제 1 도전막(114)이 받을 수 있는 물리적 및 화학적 손상을 최소화하기 위한 것일 수 있다.

[0046] 희생막(116)은 실리콘을 포함하는 물질막 및 금속 물질막 중에서 선택된 적어도 하나의 막 또는 이들이 조합된 막일 수 있다. 실리콘을 포함하는 물질막은 실리콘막, 실리콘 산화막 및 실리콘 질화막(Si_3N_4) 중에서 선택된 적어도 하나의 막 또는 이들이 조합된 막일 수 있다. 금속 물질막은 실리콘 및 탄소 중에서 선택된 적어도 하나의 성분을 포함하는 티타늄 질화막(TiN), 탄탈륨 질화막(TaN), 텅스텐 질화막(WN), 티타늄 실리사이드막(TiSi), 탄탈륨 실리사이드막(TaSi), 텅스텐 실리사이드막(WSi), 티탄 실리콘 질화막(TiSiN), 탄탈 실리콘 질화막(TaSiN) 및 텅스텐 실리콘 질화막(WSiN) 중에서 선택된 하나의 막 또는 이들이 조합된 막일 수 있다. 본 발명의 실시예에서의 희생막(116)은 티타늄 질화막일 수 있다.

[0047] 도 1b를 참조하면, 제 2 영역(B)을 노출하는 마스크 패턴(118)을 형성한다. 마스크 패턴(118)을 마스크로 하는 이온 주입 공정(화살표)으로 제 2 영역(B) 상의 제 1 도전막(114)에 금속 이온을 주입한다. 금속 이온은 제 1 도전막(114)의 성분과 다르며, 제 1 도전막(114) 내에서 이동 가능할 수 있다. 금속 이온은 알루미늄(Al), 하프늄(Hf), 지르코늄(Zr), 티타늄(Ti), 탄탈륨(Ta), 텅스텐(W), 프라세오디뮴(Pr), 팔라듐(Pd), 탄탈(Ta), 네오륨(Tb), 이테르븀(Yb), 디스프로슘(Dy), 가돌리늄(Gd), 플래티늄(Pt), 이리듐(Ir) 및 루테늄(Ru) 중에서 선택된 하나일 수 있다. 제 2 영역(B)이 p모스 영역일 경우, 금속 이온은 제 1 도전막(114)의 일함수 값을 높이는 알루미늄일 수 있다.

[0048] 이온 주입 공정에서 발생하는 제 1 도전막(114)에서의 손상을 줄이는 동시에, 주입된 금속 이온이 게이트 절연막(112) 쪽으로 확산하는 것을 촉진하기 위한 열 처리 공정을 수행한다. 바람직하게는 열 처리 공정은 700~850 ℃ 범위의 온도 및 질소(N_2) 분위기에서 1분 정도의 급속 열 처리(RTP : Rapid Thermal Process) 방식 또는 10분 정도의 가열로(furnace) 처리 방식으로 수행되는 것일 수 있다.

[0049] 도 1c를 참조하면, 이온 주입 공정으로 제 2 영역(B) 상의 금속 이온이 주입된 제 1 도전막(114md)은 제 1 영역(A) 상의 제 1 도전막(114)보다 높거나 낮은 일함수 값을 가질 수 있다. 제 2 영역(B)이 p모스 영역일 경우, 금속 이온이 주입된 제 1 도전막(114md)은 제 1 영역(A) 상의 제 1 도전막(114)보다 높은 일함수 값을 가질 수 있다. 반면에, 제 2 영역(B)이 n모스 영역일 경우, 금속 이온이 주입된 제 1 도전막(114md)은 제 1 영역(A) 상의 제 1 도전막(114)보다 낮은 일함수 값을 가질 수 있다.

[0050] 이온 주입 공정 및 열 처리 공정에 의해 제 2 영역(B) 상의 금속 이온이 주입된 제 1 도전막(114md)은 게이트 절연막(112)에 인접하는 부위에서 금속 이온의 농도가 높은 프로파일(수평 점선)을 가질 수 있다. 이러한 프로파일은 금속 이온이 주입된 제 1 도전막(114md)의 유효 일함수(effective work function)를 변화시킬 수 있다.

[0051] 마스크 패턴(118) 및 희생막(116)을 제거한 후, 제 1 도전막(114 및 114md) 상에 제 2 도전막(120)을 형성한다. 제 2 도전막(120)은 실리콘 또는 실리사이드를 포함하는 물질막 및 금속 물질막 중에서 선택된 적어도 하나의 막 또는 이들이 조합된 막일 수 있다. 본 발명의 실시예에서의 제 2 도전막(120)은 폴리 실리콘막일 수 있다. 여기서, 희생막(116)이 금속 물질막일 경우, 희생막(116)을 남겨놓을 수 있다. 남겨진 희생막(116)에 플라즈마

처리 공정 또는 대기 중에 노출하는 공정 중에서 적어도 하나의 공정이 수행될 수 있다. 이러한 공정은 희생막(118)을 게이트 전극에 포함되도록 한다.

[0052] 도 1e를 참조하면, 제 2 도전막(120), 제 1 도전막(114 및 114a~d) 및 게이트 절연막(112)을 패터닝(patterning)하여 제 1 영역(A) 및 제 2 영역(B) 상에 각각의 게이트 전극들(122a 및 122b)을 형성한다. 제 1 영역(A) 상의 게이트 전극들(122a)은 제 1 게이트 절연막 패턴(112a) 상에 형성된 제 1 도전막 패턴(114a) 및 제 2 도전막 패턴(120a)으로 이루어질 수 있다. 제 2 영역(B) 상의 게이트 전극들(122a)은 제 2 게이트 절연막 패턴(112b) 상에 형성된 금속 이온이 주입된 제 3 도전막 패턴(114b) 및 제 4 도전막 패턴(120b)으로 이루어질 수 있다.

[0053] 후속 공정으로 산소(O2)를 포함하는 산화 공정이 수행될 수 있다. 산소의 함량에 따라, 금속 이온이 주입된 제 3 도전막 패턴(114b)의 일함수 값이 변할 수 있다.

[0054] 도 2a 내지 도 2d는 본 발명의 다른 실시예에 따른 반도체 소자의 게이트 전극을 제조하는 방법을 설명하기 위한 단면도들이다.

[0055] 도 2a를 참조하면, 제 1 영역(A) 및 제 2 영역(B)을 갖는 반도체 기판(210) 상에 게이트 절연막(212)을 형성한다. 제 1 영역(A) 및 제 2 영역(B)은 소자 분리막(211)에 의해 구분될 수 있으며, 서로 반대되는 도전형일 수 있다. 제 1 영역(A) 및 제 2 영역(B)을 각각 n모스 영역 및 p모스 영역으로 설정하여 설명한다.

[0056] 게이트 절연막(212)은 실리콘 산화막 및 고유전막 중에서 선택된 적어도 하나의 막일 수 있다. 게이트 절연막(212) 상에 제 1 도전막(214)을 형성한다. 제 1 도전막(214)은 4.8~4.9eV 정도의 p모스함 (p-MOS dispositism) 일함수 값을 가지는 탄탈륨 탄소 질화막(TaCN)일 수 있다. 제 1 도전막(214) 상에 희생막(216)을 형성한다. 희생막(216)은 추후 공정인 금속 이온을 주입하는 공정(도 2b 참조)에서 제 1 도전막(214)이 받을 수 있는 물리적 및 화학적 손상을 최소화하기 위한 것일 수 있다. 희생막(216)은 티타늄 질화막일 수 있다.

[0057] 도 2b를 참조하면, n모스 영역인 제 1 영역(A)을 노출하는 마스크 패턴(218)을 형성한다. 마스크 패턴(218)을 마스크로 하는 이온 주입 공정(화살표)으로 제 1 영역(A) 상의 제 1 도전막(214)에 금속 이온을 주입한다. 금속 이온은 제 1 도전막(214)의 일함수 값을 낮추는 탄탈일 수 있다.

[0058] 이온 주입 공정에서 발생하는 제 1 도전막(214)에서의 손상을 줄이는 동시에, 주입된 탄탈 금속 이온이 게이트 절연막(212) 쪽으로 확산하는 것을 속진하기 위한 열 처리 공정을 수행한다.

[0059] 도 2c를 참조하면, 이온 주입 공정으로 제 1 영역(A) 상의 탄탈 금속 이온이 주입된 제 1 도전막(214a~d)은 제 2 영역(B) 상의 제 1 도전막(214)보다 낮은 일함수 값을 가질 수 있다.

[0060] 이온 주입 공정 및 열 처리 공정에 의해 제 1 영역(A) 상의 탄탈 금속 이온이 주입된 제 1 도전막(214a~d)은 게이트 절연막(212)에 인접하는 부위에서 금속 이온의 농도가 높은 프로파일(수평 점선)을 가질 수 있다. 이러한 프로파일은 탄탈 금속 이온이 주입된 제 1 도전막(214a~d)의 유효 일함수를 변화시킬 수 있다.

[0061] 마스크 패턴(218) 및 희생막(216)을 제거한 후, 제 1 도전막(214a~d 및 214) 상에 제 2 도전막(220)을 형성한다. 제 2 도전막(220)은 폴리 실리콘막일 수 있다.

[0062] 도 2d를 참조하면, 제 2 도전막(220), 제 1 도전막(214a~d 및 214) 및 게이트 절연막(212)을 패터닝하여 제 1 영역(A) 및 제 2 영역(B) 상에 각각의 게이트 전극들(222a 및 222b)을 형성한다. 제 1 영역(A) 상의 게이트 전극들(222a)은 제 1 게이트 절연막 패턴(212a) 상에 형성된 탄탈 금속 이온이 주입된 제 1 도전막 패턴(214a) 및 제 2 도전막 패턴(220a)으로 이루어질 수 있다. 제 2 영역(B) 상의 게이트 전극들(222b)은 제 2 게이트 절연막 패턴(212b) 상에 형성된 제 3 도전막 패턴(214b) 및 제 4 도전막 패턴(220b)으로 이루어질 수 있다.

[0063] 후속 공정으로 산소를 포함하는 산화 공정이 수행될 수 있다. 산소의 함량에 따라, 탄탈 금속 이온이 주입된 제 1 도전막 패턴(214a)의 일함수 값이 변할 수 있다.

[0064] 도 3a 내지 도 3e는 본 발명의 또 다른 실시예에 따른 반도체 소자의 게이트 전극을 제조하는 방법을 설명하기 위한 단면도들이다.

[0065] 도 3a를 참조하면, 제 1 영역(A) 및 제 2 영역(B)을 갖는 반도체 기판(310) 상에 게이트 절연막(312)을 형성한다. 제 1 영역(A) 및 제 2 영역(B)은 소자 분리막(311)에 의해 구분될 수 있으며, 서로 반대되는 도전형일 수 있다. 제 1 영역(A) 및 제 2 영역(B)을 각각 n모스 영역 및 p모스 영역으로 설정하여 설명한다.

[0066] 게이트 절연막(312)은 실리콘 산화막 및 고유전막 중에서 선택된 적어도 하나의 막일 수 있다. 게이트 절연막(312) 상에 제 1 도전막(314)을 형성한다. 제 1 도전막(314)은 4.5~4.7eV 정도의 일함수 값을 가지는 탄탈륨 질화막(TaN), 티타늄 질화막(TiN) 및 텅스텐 질화막(WN) 중에서 선택된 적어도 하나의 막 또는 이들이 조합된 막일 수 있다. 제 1 도전막(314) 상에 희생막(316)을 형성한다. 희생막(316)은 추후 공정인 금속 이온을 주입하는 공정(도 3b 및 도 3c 참조)에서 제 1 도전막(314)이 받을 수 있는 물리적 및 화학적 손상을 최소화하기 위한 것일 수 있다. 희생막(316)은 탄탈늄 질화막일 수 있다.

[0067] 도 3b 및 도 3c를 참조하면, p모스 영역인 제 2 영역(B)을 노출하는 제 1 마스크 패턴(318b)을 형성한다. 제 1 마스크 패턴(318b)을 마스크로 하는 제 1 이온 주입 공정(화살표)으로 제 2 영역(B) 상의 제 1 도전막(314)에 금속 이온을 주입한다. 금속 이온은 제 1 도전막(314)의 일함수 값을 높이는 알루미늄일 수 있다.

[0068] 제 1 마스크 패턴(318b)을 제거한 후, n모스 영역인 제 1 영역(A)을 노출하는 제 2 마스크 패턴(318a)을 형성한다. 제 2 마스크 패턴(318a)을 마스크로 하는 제 2 이온 주입 공정(도 3b의 화살표)으로 제 1 영역(A) 상의 제 1 도전막(314)에 금속 이온을 주입한다. 금속 이온은 제 1 도전막(314)의 일함수 값을 낮추는 란탄일 수 있다. 여기서, 도 3b 및 도 3c는 순서가 바뀌어 수행될 수 있다.

[0069] 이온 주입 공정에서 발생하는 제 1 도전막(314)에서의 손상을 줄이는 동시에, 제 1 영역(A) 및 제 2 영역(B)의 제 1 도전막(314)에 각각 주입된 금속 이온이 게이트 절연막(312) 쪽으로 확산하는 것을 촉진하기 위한 열 처리 공정을 수행한다.

[0070] 도 3d를 참조하면, 제 2 이온 주입 공정으로 제 1 영역(A) 상의 란탄 금속 이온이 주입된 제 1 도전막(314ada)은 이온 주입 공정 전의 반도체 기판(310) 상의 제 1 도전막(도 3a의 314)보다 낮은 일함수 값을 가질 수 있다. 또한, 제 1 이온 주입 공정으로 제 2 영역(B) 상의 알루미늄 금속 이온이 주입된 제 1 도전막(314adb)은 이온 주입 공정 전의 반도체 기판(310) 상의 제 1 도전막(도 3a의 314)보다 높은 일함수 값을 가질 수 있다.

[0071] 제 1 및 제 2 이온 주입 공정, 및 열 처리 공정에 의해 제 1 영역(A) 및 제 2 영역(B) 상의 각각 란탄 금속 이온이 주입된 제 1 도전막(314ada) 및 알루미늄 금속 이온이 주입된 제 1 도전막(314adb)은 게이트 절연막(312)에 인접하는 부위에서 각각의 금속 이온의 농도가 높은 프로파일(수평 절선)을 가질 수 있다. 이러한 프로파일은 각각의 금속 이온이 주입된 제 1 도전막(314ada 및 314adb)의 유효 일함수를 변화시킬 수 있다.

[0072] 제 2 마스크 패턴(318a) 및 희생막(316)을 제거한 후, 제 1 도전막(314ada 및 314adb) 상에 제 2 도전막(320)을 형성한다. 제 2 도전막(320)은 폴리 실리콘막일 수 있다.

[0073] 도 3e를 참조하면, 제 2 도전막(320), 제 1 도전막(314ada 및 314adb) 및 게이트 절연막(312)을 패터닝하여 제 1 영역(A) 및 제 2 영역(B) 상에 각각의 게이트 전극들(322a 및 322b)을 형성한다. 제 1 영역(A) 상의 게이트 전극들(322a)은 제 1 게이트 절연막 패턴(312a) 상에 형성된 란탄 금속 이온이 주입된 제 1 도전막 패턴(314a) 및 제 2 도전막 패턴(320a)으로 이루어질 수 있다. 제 2 영역(B) 상의 게이트 전극들(322b)은 제 2 게이트 절연막 패턴(312b) 상에 형성된 알루미늄 금속 이온이 주입된 제 3 도전막 패턴(314b) 및 제 4 도전막 패턴(320b)으로 이루어질 수 있다.

[0074] 후속 공정으로 산소를 포함하는 산화 공정이 수행될 수 있다. 산소의 함량에 따라, 란탄 금속 이온이 주입된 제 1 도전막 패턴(314a) 및 알루미늄 금속 이온이 주입된 제 1 도전막 패턴(314b)의 일함수 값이 변할 수 있다.

[0075] 도 4a 내지 도 4d는 본 발명의 또 다른 실시예에 따른 반도체 소자의 게이트 전극을 제조하는 방법을 설명하기 위한 단면도들이다.

[0076] 도 4a를 참조하면, 제 1 영역(A) 및 제 2 영역(B)을 갖는 반도체 기판(410) 상에 게이트 절연막(412)을 형성한다. 제 1 영역(A) 및 제 2 영역(B)은 소자 분리막(411)에 의해 구분될 수 있으며, 서로 반대되는 도전형일 수 있다. 제 1 영역(A) 및 제 2 영역(B)을 각각 n모스 영역 및 p모스 영역으로 설정하여 설명한다.

[0077] 게이트 절연막(412)은 실리콘 산화막 및 고유전막 중에서 선택된 적어도 하나의 막일 수 있다. 게이트 절연막(412) 상에 금속막(413)을 형성한다. 금속막(413)은 $Ta_xC_yN_z$막, $Ti_xC_yN_z$막 및 $W_xC_yN_z$막(x, y 및 z는 0 또는 양의 정수) 중에서 선택된 적어도 하나의 막 또는 이들이 조합된 막일 수 있다. 바람직하게는 금속막(413)은 5~40Å 정도인 탄탈륨 탄화 질화막일 수 있다.

[0078] 금속막(413) 상에 제 1 도전막(414)을 형성한다. 제 1 도전막(414)은 4.1eV 근처의 n모스향(nMOS disposition) 일함수 값을 가지는 n형 도핑 실리콘막(n-doped silicon)일 수 있다. 이에 따라, 금속막을 개재한 폴리 실리콘

막 구조(NBPS)의 기본 구조가 형성될 수 있다.

[0079] 제 1 도전막(414) 상에 희생막(416)을 형성한다. 희생막(416)은 추후 공정인 금속 이온을 주입하는 공정(도 4b 참조)에서 제 1 도전막(414)에 발생할 수 있는 물리적 및 화학적 손상을 최소화하기 위한 것일 수 있다. 희생막(416)은 더미늄 절화막일 수 있다.

[0080] 도 4b를 참조하면, p로스 영역인 제 2 영역(B)을 노출하는 마스크 패턴(418)을 형성한다. 마스크 패턴(418)을 마스크로 하는 이온 주입 공정(화살표)으로 제 2 영역(B) 상의 제 2 도전막(414)에 금속 이온을 주입한다. 금속 이온은 제 1 도전막(414)의 일함수 값을 높이는 알루미늄일 수 있다.

[0081] 이온 주입 공정에서 발생하는 제 1 도전막(414)에서의 손상을 줄이는 동시에, 주입된 알루미늄 금속 이온이 게이트 절연막(412) 쪽으로 확산하는 것을 촉진하기 위한 열 처리 공정을 수행한다.

[0082] 도 4c를 참조하면, 이온 주입 공정으로 제 2 영역(B) 상의 알루미늄 금속 이온이 주입된 제 1 도전막(414ma)은 제 1 영역(A) 상의 제 1 도전막(414)보다 높은 일함수 값을 가질 수 있다.

[0083] 이온 주입 공정 및 열 처리 공정에 의해 제 2 영역(A) 상의 알루미늄 금속 이온이 주입된 제 1 도전막(414ma)은 게이트 절연막(412)에 인접하는 부위에서 알루미늄 금속 이온의 농도가 높은 프로파일(수평 점선)을 가질 수 있다. 이러한 프로파일은 알루미늄 금속 이온이 주입된 제 1 도전막(414ma)의 유효 일함수를 변화시킬 수 있다.

[0084] 마스크 패턴(418) 및 희생막(416)을 제거한 후, 제 1 도전막(414 및 414ma) 상에 제 2 도전막(420)을 형성한다. 제 2 도전막(420)은 폴리 실리콘막일 수 있다.

[0085] 도 4d를 참조하면, 제 2 도전막(420), 제 1 도전막(414 및 414ma) 및 게이트 절연막(412)을 패터닝하여 제 1 영역(A) 및 제 2 영역(B) 상에 각각의 게이트 전극들(422a 및 422b)을 형성한다. 제 1 영역(A) 상의 게이트 전극들(422a)은 제 1 게이트 절연막 패턴(412a) 상에 형성된 제 1 도전막 패턴(414a) 및 제 2 도전막 패턴(420a)으로 이루어질 수 있다. 제 2 영역(B) 상의 게이트 전극들(422b)은 제 2 게이트 절연막 패턴(412b) 상에 형성된 알루미늄 금속 이온이 주입된 제 3 도전막 패턴(414b) 및 제 4 도전막 패턴(420b)으로 이루어질 수 있다.

[0086] 후속 공정으로 산소를 포함하는 산화 공정이 수행될 수 있다. 산소의 양에 따라, 알루미늄 금속 이온이 주입된 제 1 도전막 패턴(414b)의 일함수 값이 변할 수 있다.

[0087] 상기한 본 발명의 실시예들에 따른 방법으로 반도체 소자의 게이트 전극을 제조함으로써, 게이트 전극을 형성하는 공정에서 게이트 절연막이 노출되는 것을 방지할 수 있다. 이에 따라, 게이트 절연막의 특성이 저하되는 것을 최소화할 수 있다. 또한, 고유전율 물질을 게이트 절연막에 안정적으로 적용할 수 있다. 이에 따라, 게이트 전극의 동작 효율을 높일 수 있다. 이에 더하여, 단순한 이온 주입 공정으로 도전형에 맞는 게이트 전극을 형성할 수 있다. 이에 따라, 반도체 소자의 제조 비용을 절감할 수 있다.

발명의 효과

[0088] 상술한 바와 같이, 본 발명에 따르면 게이트 전극을 형성하는 공정에서 게이트 절연막이 노출되는 것을 방지하여 게이트 절연막의 특성이 저하되는 것을 최소화함으로써, 품질이 우수한 반도체 소자를 제공할 수 있다.

[0089] 또한, 고유전율 물질을 게이트 절연막에 안정적으로 적용하여 게이트 전극의 동작 효율을 높임으로써, 품질이 우수한 반도체 소자를 제공할 수 있다.

[0090] 이에 더하여, 단순한 이온 주입 공정으로 도전형에 맞는 게이트 전극을 형성함으로써, 제조 비용을 절감할 수 있는 반도체 소자의 제조 방법을 제공할 수 있다.

도면의 간단한 설명

[0091] 도 1a 내지 도 1d는 본 발명의 일 실시예에 따른 반도체 소자의 제조 방법을 설명하기 위한 단면도들;

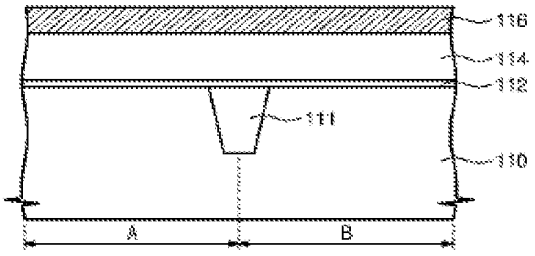
[0092] 도 2a 내지 도 2d는 본 발명의 다른 실시예에 따른 반도체 소자의 제조 방법을 설명하기 위한 단면도들;

[0093] 도 3a 내지 도 3e는 본 발명의 또 다른 실시예에 따른 반도체 소자의 제조 방법을 설명하기 위한 단면도들;

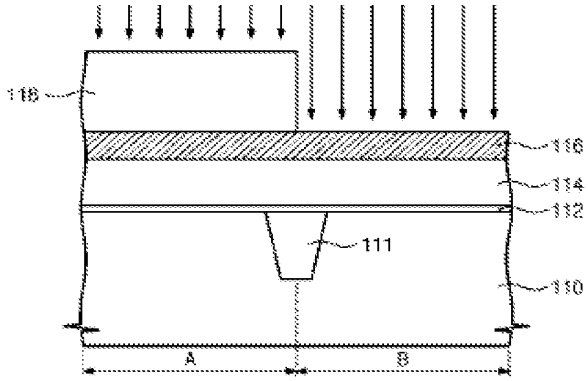
[0094] 도 4a 내지 도 4d는 본 발명의 또 다른 실시예에 따른 반도체 소자의 제조 방법을 설명하기 위한 단면도들.

도면

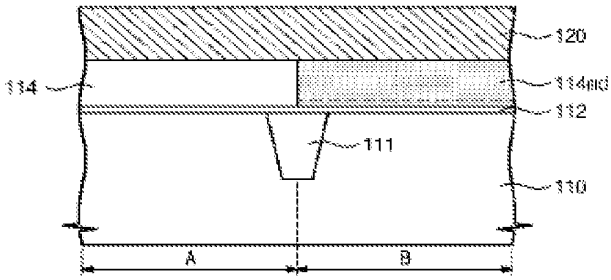
도면2a



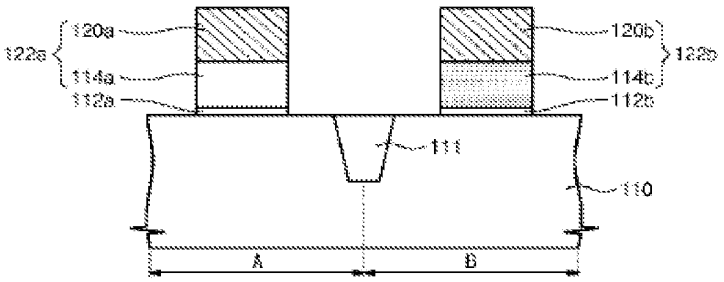
도면2b



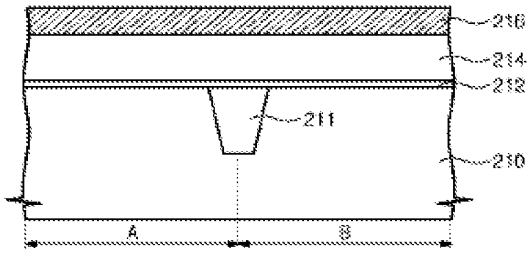
도면2c



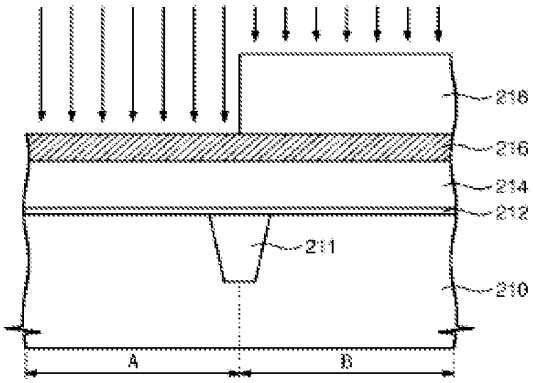
도면21



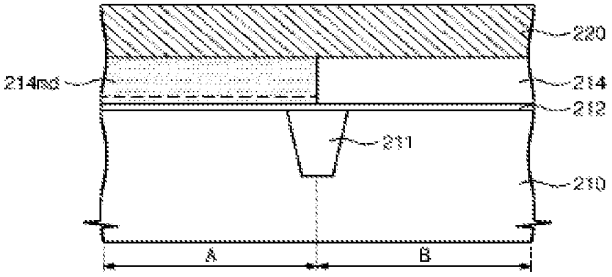
도면22a



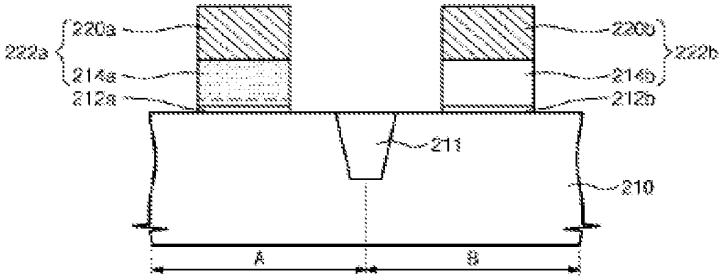
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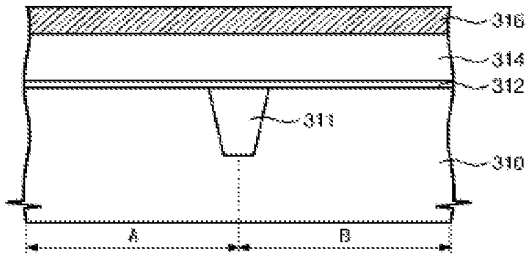
도면2c



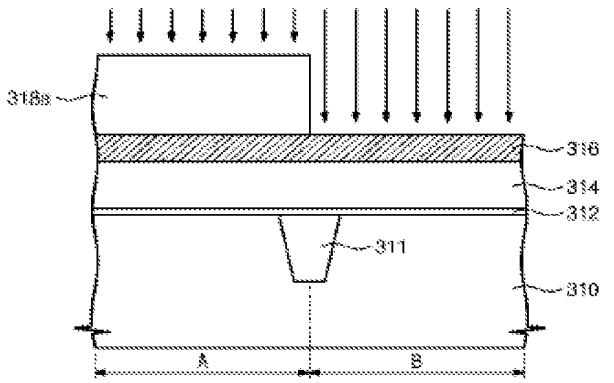
도면2d



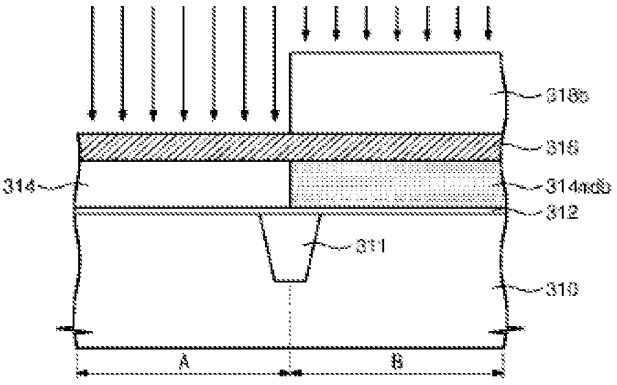
도면3a



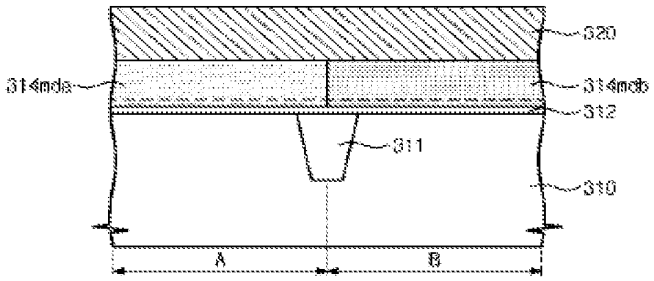
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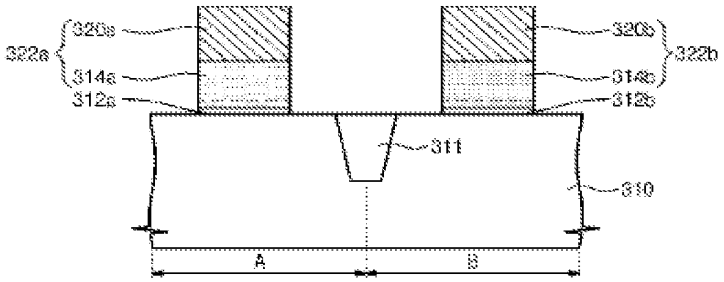
도면3c



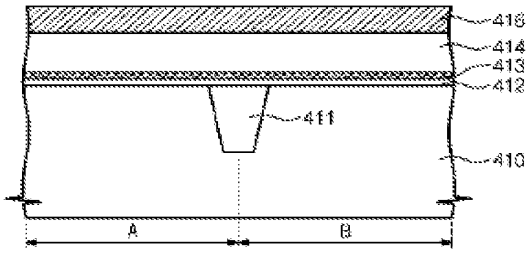
도면37



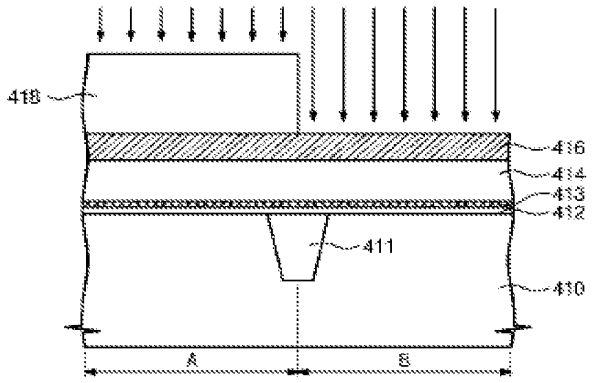
도면38a



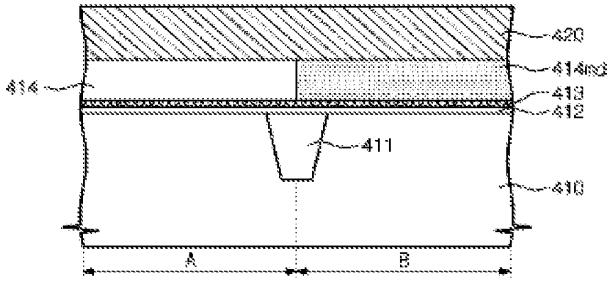
도면39a



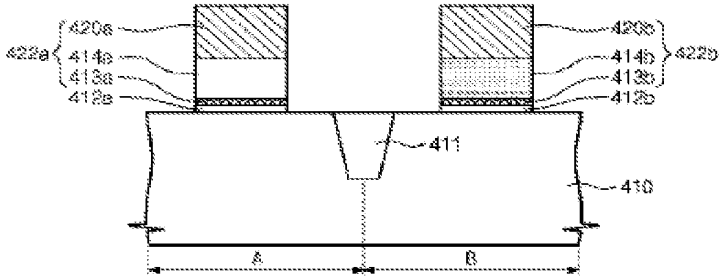
도면5b



도면5c



도면5d



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(71) Applicant:
- HYNIX SEMICONDUCTOR INC.

(72) Inventor:
- JANG, SE AUG
- YANG, HONG SEON
- CHO, HEUNG JAE

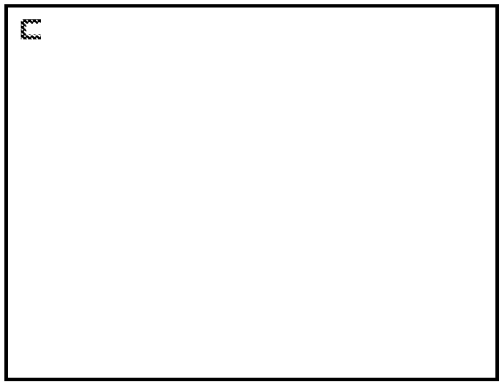
(54) TRANSISTOR HAVING A GATE ELECTRODE CAPABLE OF TUNING THE WORK FUNCTION BY INSERTING THE TITANIUM NITRIDE FILM BETWEEN THE N+ TYPE POLYSILICON LAYER AND GATE INSULATING LAYER AND A MEMORY DEVICE WITH THE SAME

(57) Abstract:

PURPOSE: A transistor having a gate electrode with tuning of work function and a memory device with the same are provided to adjust the gate induced leakage current and the threshold voltage using the N+ type poly silicon layer.

CONSTITUTION: A transistor comprises a gate insulating layer(54), a gate electrode(201), a source junction and a drain junction. The gate insulating layer is arranged on a substrate(51). The gate electrode comprises electrodes(55A, 57B) having different work functions. One among the electrodes is the metal nitride layer. The others are the doped poly silicon layer. The source junction and the drain junction are arranged on the substrate in order to overlap the gate electrode. The memory device comprises the substrate, the gate insulating layer, the first electrode(203) and the second electrode(202).

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(71) 출원인
주식회사 하이닉스반도체
경기 이천시 부발읍 아미리 산136-1
(72) 발명자
장세억
경기 이천시 부발읍 아미리 763 현대아파트 7차 707-1604
양홍선
경기 용인시 풍덕천2동 우성아파트 803-1905
조종제
경기 이천시 대월면 월대1-PART APT 105-804
(74) 대리인
특허법인 신성

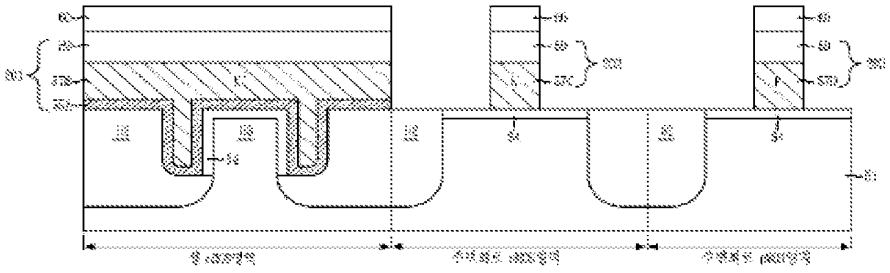
전체 청구항 수 : 총 34 항

(54) 발명의 명칭 일함수가 조절된 게이트전극을 구비한 트랜지스터 및 그를 구비하는 메모리소자

(57) 요 약

본 발명은 높은 전류구동능력과 낮은 게이트유도드레인누설을 가지면서도 문턱전압을 일정수준 이상으로 높일 수 있는 트랜지스터 및 그를 구비한 메모리소자를 제공하기 위한 것으로, 본 발명의 메모리 소자는 셀영역과 주변회로영역을 구비하는 기판; 상기 기판 상의 게이트절연막; 상기 셀영역의 게이트절연막에 형성된 제1게이트전극(서로 다른 일함수를 갖는 전극들로 이루어짐, 금속막과 폴리실리콘막의 적층구조); 및 상기 주변회로영역의 게이트절연막에 형성된 제2게이트전극을 포함하고, 상술한 본 발명은 상술한 본 발명은 셀영역에 형성되는 트랜지스터의 게이트전극에 P형 폴리실리콘막보다 일함수가 작은 금속막을 게이트절연막과 접촉하도록 하므로써 높은 문턱전압을 얻어 오프누설을 개선함과 동시에, 게이트절연막과 접합 계면에서의 밴드굽곡을 완화시켜 게이트유도드레인누설 특성을 개선시킬 수 있는 효과가 있다.

대 표 도 - 도3



특허청구의 범위

청구항 1

기판 상의 게이트절연막;

상기 게이트절연막 상에서 서로 다른 일함수를 갖는 전극물로 이루어진 게이트전극; 및

상기 게이트전극 양측의 기판 내에 형성된 소스접합 및 드레인접합

을 포함하는 트랜지스터.

청구항 2

제1항에 있어서,

상기 게이트전극을 이루는 전극물 중에서 상기 게이트절연막에 접촉하는 전극은,

N형 불순물이 도핑된 폴리실리콘막의 일함수보다는 크고 P형 불순물이 도핑된 폴리실리콘막의 일함수보다는 작은 일함수를 갖는 물질인 트랜지스터.

청구항 3

제1항에 있어서,

상기 게이트전극 중에서 상기 게이트절연막에 접촉하는 전극의 일함수는 4.4~4.8eV 범위인 트랜지스터.

청구항 4

제1항에 있어서,

상기 게이트전극은,

상기 게이트절연막에 접촉하는 금속막과, 상기 금속막 상의 폴리실리콘막을 포함하는 트랜지스터.

청구항 5

제4항에 있어서,

상기 금속막은 티타늄질화막(TiN)을 포함하는 트랜지스터.

청구항 6

제4항에 있어서,

상기 금속막은 30~150Å 두께인 트랜지스터.

청구항 7

제4항에 있어서,

상기 폴리실리콘막은 불순물이 도핑된 폴리실리콘막인 트랜지스터.

청구항 8

제7항에 있어서,

상기 불순물은 인(P) 또는 비소(As) 중에서 선택된 어느 하나를 포함하는 트랜지스터.

청구항 9

제4항에 있어서,

상기 폴리실리콘막의 저저항 금속막을 더 포함하는 트랜지스터.

청구항 10

제6항에 있어서,

상기 저저항 금속막은 텅스텐막 또는 텅스텐실리사이드막을 포함하는 트랜지스터.

청구항 11

제1항에 있어서,

상기 게이트전극 양측벽의 게이트측벽스페이서와, 상기 게이트측벽스페이서 아래의 기판 내에 형성된 LDD(Lightly Doped Drain) 구조를 더 포함하는 트랜지스터.

청구항 12

제1항에 있어서,

상기 게이트전극 아래의 기판에 형성된 다면채널 구조를 더 포함하는 트랜지스터.

청구항 13

제12항에 있어서,

상기 다면채널 구조는, 핀(Fin), 워제스, 멀티게이트 또는 새들형 구조 중 어느 하나인 트랜지스터.

청구항 14

제1항에 있어서,

상기 소스접합 및 드레인접합은 P형 불순물이 도핑된 소스 및 드레인 접합인 트랜지스터.

청구항 15

활성영역과 주변회로영역을 구비하는 기판;

상기 기판 상의 게이트절연막;

상기 활성영역의 게이트절연막에 형성된 제1게이트전극; 및

상기 주변회로영역의 게이트절연막에 형성된 제2게이트전극을 포함하고,

상기 제1게이트전극이 서로 다른 일함수를 갖는 전극들로 이루어진 메모리 소자.

청구항 16

제15항에 있어서,

상기 제1게이트전극을 이루는 전극들 중에서 상기 게이트절연막에 접촉하는 전극은,

N형 불순물이 도핑된 폴리실리콘막의 일함수보다는 크고 P형 불순물이 도핑된 폴리실리콘막의 일함수보다는 작은 일함수를 갖는 물질인 메모리소자.

청구항 17

제15항에 있어서,

상기 제1게이트전극 중에서 상기 게이트절연막에 접촉하는 전극의 일함수는 4.4~4.8eV 범위인 메모리소자.

청구항 18

제15항에 있어서,

상기 제1게이트전극은,

상기 게이트절연막에 접촉하는 금속막과, 상기 금속막 상의 폴리실리콘막을 포함하는 메모리소자.

청구항 19

제18항에 있어서,

상기 금속막은 티타늄질화막(TiN)을 포함하는 메모리소자.

청구항 20

제18항에 있어서,

상기 금속막은 30~150Å 두께인 메모리소자.

청구항 21

제18항에 있어서,

상기 폴리실리콘막은 불순물이 도핑된 폴리실리콘막인 메모리소자.

청구항 22

제21항에 있어서,

상기 불순물은 인(P) 또는 비소(As) 중에서 선택된 어느 하나를 포함하는 메모리소자.

청구항 23

제18항에 있어서,

상기 폴리실리콘막 위의 저저항 금속막을 더 포함하는 메모리소자.

청구항 24

제23항에 있어서,

상기 저저항 금속막은 텅스텐막 또는 텅스텐실리사이드막을 포함하는 메모리소자.

청구항 25

제15항 내지 제24항 중 어느 한 항에 있어서,

상기 제1게이트전극 아래의 기판에 형성된 다면채널 구조를 더 포함하는 메모리소자.

청구항 26

제25항에 있어서,

상기 다면채널 구조는, 핀(Fin), 리세스, 엘리베이티드 또는 새들핀 구조 중 어느 하나인 메모리소자.

청구항 27

제15항에 있어서,

상기 제1게이트전극 양측벽에 접하되어 상기 기판 내에 형성된 소스접합 및 드레인접합을 포함하는 메모리소자.

청구항 28

제27항에 있어서,

상기 제1게이트전극 양측의 게이트측벽스페이서와, 상기 게이트측벽스페이서 아래의 기판 내에 형성된 LDD(Lightly Doped Drain) 구조를 더 포함하는 메모리소자.

청구항 29

제28항에 있어서,

상기 소스접합 및 드레인접합은, N형 불순물이 도핑된 메모리 소자.

청구항 30

제15항에 있어서,

상기 제2게이트전극은, 폴리실리콘막과 저저항 금속막의 적층구조인 메모리 소자.

청구항 31

제30항에 있어서,

상기 폴리실리콘막은 N형 불순물 또는 P형 불순물이 도핑된 폴리실리콘막인 메모리 소자.

청구항 32

제15항에 있어서,

상기 제1게이트전극은 다면 채널(Multi-plane channel)을 갖는 트랜지스터의 게이트전극이고, 상기 제2게이트전극은 수평 채널을 갖는 트랜지스터의 게이트전극인 메모리 소자.

청구항 33

제15항에 있어서,

상기 제1게이트전극은 핀트랜지스터(Fin FET)의 게이트전극이고, 상기 제2게이트전극은 플래너트랜지스터(Planar FET)의 게이트전극인 메모리 소자.

청구항 34

제33항에 있어서,

상기 핀트랜지스터는 nMOS 트랜지스터이고, 상기 플래너트랜지스터는 nMOS 트랜지스터 또는 pMOS 트랜지스터를 포함하는 메모리 소자.

발 명 의

발명의 상세한 설명

기 술 분 야

[0001] 본 발명은 메모리 반도체 제조 공정에 관한 것이며, 특히 서로 다른 일함수(work function)를 갖는 전극들로 이루어진 게이트전극을 갖는 트랜지스터 및 그를 구비한 메모리소자에 관한 것이다.

배 경 기 술

[0002] 메모리소자의 집적도가 증가함에 따라 2차원적인 트랜지스터 구조(이를 '플래너 트랜지스터(Planar transistor)'라 일컬음)로는 여러가지 측면에서 한계에 다다르고 있다. 특히 고속소자(High Speed Device)의 경우, 2차원적인 트랜지스터 구조로는 요구되는 높은 전류 구동 성능(Current Drivability)을 만족시킬 수 없다. 이러한 문제점을 극복하기 위해 제안된 기술이 곧 전계효과트랜지스터(Fin FET, 이하 '핀트랜지스터'라 약칭함) 구조와 같은 3차원 트랜지스터이다.

[0003] 핀트랜지스터(FinFET)의 특징은 활성영역의 3면이 채널로 사용되며, 그 결과 전류구동능력(Current drivability)이 뛰어난 특징을 가지고 있다. 그러나 3면이 채널로 형성 되기 때문에 문턱전압(Threshold voltage, Vt)을 일정 수준 이상으로 높이기가 매우 힘든 단점을 가지고 있다.

[0004] DRAM 같은 메모리소자의 셀트랜지스터(Cell Transistor)는 통상적으로 NMOSFET를 사용하는데, 0.8V 이상의 높은 문턱전압이 요구되는 셀트랜지스터에 핀트랜지스터를 적용하기는 어렵다. DRAM에서는 문턱전압을 일정 수준 이상 올리지 못하면 GIDL(Gate Induced Drain Leakage)과 같은 오프누설(Off leakage)이 현저히 증가하는 문제점이 있다.

[0005] 최근에 메모리소자의 셀트랜지스터로서 핀트랜지스터를 적용하는 경우에 문턱전압을 쉽게 높이기 위해 제안된 방법이 핀트랜지스터의 게이트 전극을 인(P)과 같은 N형 불순물이 도핑된(In-Situ P+ doped) N형 폴리실리콘막(N^+ Poly Si)으로 사용하는 대신 붕소(B)와 같은 P형 불순물이 도핑된(In-Situ Boron Doped) P형 폴리실리콘막(P^+ Poly Si)을 형성하는 방법이 있다. 이론적으로 P형 폴리실리콘막(P^+ Poly Si)의 일함수(Work function)는

N형 폴리실리콘(N+ Poly Si)보다 1.1eV 정도 더 높기 때문에 nMOSFET에서 게이트전극의 교체만으로도 0.8~1.0V 정도의 수준으로 문턱전압을 높일 수 있다.

[0006] 도 1은 종래기술에 따른 풀트랜지스터(Fin FET)를 구비한 메모리소자의 구조단면도이다.

[0007] 도 1을 참조하면, 셀영역과 주변회로영역을 구비한 기판(11)에 소자분리막(12)이 형성되어 있고, 기판(11)의 셀 영역에는 nMOSFET가 형성되고, 주변회로영역에는 nMOSFET와 pMOSFET가 형성되어 있다. 셀영역은 '셀 nMOS 영역'이라 하고, 주변회로영역의 nMOS 영역은 '주변회로 nMOS 영역', 주변회로영역의 pMOS 영역은 '주변회로 pMOS 영역'이라 한다.

[0008] 먼저, 셀 nMOS 영역은 채널로 사용되는 핀 구조(Fin, 11A)가 형성되어 있고, 핀구조(11A) 상에 게이트절연막(13)이 형성되고, 게이트절연막(13) 상에 P형 폴리실리콘막(P+ Poly si)으로 이루어진 게이트전극(14A)이 형성된다.

[0009] 그리고, 주변회로 nMOS 영역은 기판(11) 상의 게이트절연막(13), 게이트절연막(13) 상의 N형 폴리실리콘막(N+ Poly si)으로 이루어진 게이트전극(14B)을 포함하여 풀리나 트랜지스터가 된다.

[0010] 그리고, 주변회로 pMOS 영역은 기판(11) 상의 게이트절연막(13), 게이트절연막(13) 상의 P형 폴리실리콘막(P+ Poly si)으로 이루어진 게이트전극(14A)을 포함하여 풀리나 트랜지스터가 된다.

[0011] 일반적으로 트랜지스터의 문턱전압(Vt)은 게이트전극으로 사용된 물질의 일함수(work function, Φ)와 비례 관계를 갖는다. 즉, 게이트전극의 일함수가 크면 문턱전압을 높일 수 있다.

[0012] 도 2는 셀 nMOS 영역에서 P형 폴리실리콘막을 게이트전극으로 사용할 때의 문제점을 설명하기 위한 도면이다. 도 2의 경우는, 일함수가 4eV(Φ_M)인 고농도 N형 폴리실리콘막(N+ Poly-si)을 게이트절연막(13) 위에 형성한 경우와 일함수가 5eV(Φ_M)인 고농도 P형 폴리실리콘막(P+ Poly-si)을 게이트절연막(13) 위에 형성한 경우의 밴드다이어그램(Band Diagram)을 비교한 도면이다. 소스영역 및 드레인영역은 모두 N형 불순물이 저농도(게이트전극용 폴리실리콘막에 도핑된 불순물의 농도보다 낮음)로 도핑된 소스 및 드레인영역(N- S/D)이라 가정하였다. 일반적으로, 고농도 N형 폴리실리콘막의 일함수는 저농도 N형 소스 및 드레인영역보다 약간 작고, P형 폴리실리콘막의 일함수는 저농도 N형 폴리실리콘막의 일함수보다 매우 크다. 그리고, 도면부호 'Ec', 'Ei', 'Ef', 'Ev'는 에너지 레벨(Energy Level)을 의미하고, Vl은 진공레벨(Vacuum Level)을 의미한다. 통상적으로 일함수라 함은 진공레벨(Vl)과 페르미레벨(Ef) 사이의 값을 의미한다.

[0013] 도 2에 도시된 결과를 살펴보면, N형 폴리실리콘막을 게이트전극으로 사용하는 경우에는 N형 폴리실리콘막과 N형 소스/드레인영역간 일함수 차이가 작기 때문에 밴드굴곡(Band bending, 도면부호 '20A')이 거의 발생하지 않으나, P형 폴리실리콘막을 게이트전극으로 사용하는 경우에는 P형 폴리실리콘막과 N형 소스/드레인영역간 일함수 차이가 매우 크기 때문에 게이트절연막과 접합 계면에서의 밴드굴곡(도면부호 '20B')이 격도하게 발생됨을 알 수 있다.

[0014] 결국, 셀 nMOS 영역에서 P형 폴리실리콘막을 게이트전극으로 사용하면 게이트유도드레인누설(Gate Induced Drain Leakage; GIDL) 특성이 N형 폴리실리콘막을 사용하는 경우보다 매우 취약해지지 DRAM에서 데이터유지(data retention) 특성이 급격히 열화된다.

[0015] P형 폴리실리콘막을 게이트전극으로 사용하는 경우에 게이트유도드레인누설(GIDL)이 증가하는 이유는, 게이트전극과 드레인영역의 중첩 영역에서 밴드굴곡이 과다하게 발생된 결과 전자(Electron)가 가전자대(valence band, Ev)로부터 전도대(conduction band, Ec)로 뛰고 나가는(tunneling)것에 기인한다. 게이트유도드레인누설은 밴드굴곡이 심하면 더욱 증가되는 것으로 알려져 있으며, 도 2에서 알 수 있듯이, P형 폴리실리콘막을 사용하는 경우에 밴드굴곡이 매우 과다하게 발생하고 있기 때문에 게이트유도드레인누설이 더욱 증가된다.

발명의 내용

해결 하고자하는 과제

[0016] 본 발명은 상기한 종래기술의 문제점을 해결하기 위해 안출한 것으로서, 높은 전류구동성능과 낮은 게이트유도드레인누설을 가지면서도 문턱전압을 일정수준 이상으로 높일 수 있는 게이트전극을 구비한 트랜지스터 및 그를 구비한 메모리소자를 제공하는데 그 목적이 있다.

구성 및 작용

[0017] 상기 목적을 달성하기 위한 본 발명의 트랜지스터는 기판 상의 게이트절연막; 상기 게이트절연막 상에서 서로 다른 일함수를 갖는 전극들로 이루어진 게이트전극; 및 상기 게이트전극 양측의 기판 내에 형성된 소스영역 및 드레인접합을 포함하는 것을 특징으로 하고, 상기 게이트전극을 이루는 전극들 중에서 상기 게이트절연막에 접촉하는 전극은 N형 불순물이 도핑된 폴리실리콘막의 일함수보다는 크고 P형 불순물이 도핑된 폴리실리콘막의 일함수보다는 작은 일함수를 갖는 물질인 것을 특징으로 하며, 상기 게이트전극 중에서 상기 게이트절연막에 접촉하는 전극의 일함수는 4.4~4.8eV 범위인 것을 특징으로 하며, 상기 게이트전극은 상기 게이트절연막에 접촉하는 금속막과, 상기 금속막 상의 폴리실리콘막을 포함하는 것을 특징으로 하며, 상기 금속막은 티타늄질화막을 포함하는 것을 특징으로 한다.

[0018] 그리고, 본 발명의 메모리 소자는 셀영역과 주변회로영역을 구비하는 기판; 상기 기판 상의 게이트절연막; 상기 셀영역의 게이트절연막에 형성된 제1게이트전극, 및 상기 주변회로영역의 게이트절연막에 형성된 제2게이트전극을 포함하고, 상기 제1게이트전극이 서로 다른 일함수를 갖는 전극들로 이루어진 것을 특징으로 한다. 상기 제1게이트전극 중에서 상기 게이트절연막에 접촉하는 전극은 N형 불순물이 도핑된 폴리실리콘막의 일함수보다는 크고 P형 불순물이 도핑된 폴리실리콘막의 일함수보다는 작은 일함수를 갖는 물질인 것을 특징으로 하며, 상기 제1게이트전극 중 이루는 전극들 중에서 상기 게이트절연막에 접촉하는 전극의 일함수는 4.4~4.8eV 범위인 것을 특징으로 하고, 상기 제1게이트전극은 상기 게이트절연막에 접촉하는 금속막과, 상기 금속막 상의 폴리실리콘막을 포함하는 것을 특징으로 하며, 상기 금속막은 티타늄질화막(TiN)을 포함하는 것을 특징으로 한다.

효 과

[0019] 상술한 본 발명은 셀영역에 형성되는 트랜지스터의 게이트전극에 P형 폴리실리콘막보다 일함수가 작은 금속막을 게이트절연막과 접촉하도록 하므로써 높은 문턱전압을 얻어 오프누설을 개선함과 동시에, 게이트절연막과 접합계면에서의 밴드굴곡을 완화시켜 게이트유도드레인누설 특성을 개선시킬 수 있는 효과가 있다.

[0020] 또한, 셀영역에 형성되는 트랜지스터에 핀구조와 같은 다면채널을 적용하므로써 채널길이를 증가시켜 전류구동능력을 향상시킬 수 있다.

발명의 실시를 위한 구체적인 내용

[0021] 이하, 본 발명이 속하는 기술분야에서 통상의 지식을 가진 자가 본 발명의 기술적 사상을 용이하게 실시할 수 있을 정도로 상세히 설명하기 위하여, 본 발명의 가장 바람직한 실시예를 첨부 도면을 참조하여 설명하기로 한다.

[0022] 도 3a는 본 발명의 제1실시예에 따른 트랜지스터의 구조 단면도이고, 도 3b는 도 3a의 A-A'선에 따른 단면도이다.

[0023] 도 3a에 도시된 바와 같이, 기판(31) 상에 게이트절연막(34)이 형성된다. 여기서, 기판(31)에는 소자분리막(32)이 형성되어 있고, 기판(31)에는 핀구조(Fin, 33)가 형성되어 있다. 여기서, 핀구조(33)는 채널길이 증가를 위한 다면채널의 일 예이며, 핀구조(33)는 소자분리막(32)을 일부 리세스시켜 형성한 것이다. 다면채널 형성을 위해 핀구조(33) 외에 리세스(Recess), 새들핀(Saddle fin), 벌브형리세스(Bulb type recess) 구조가 형성될 수도 있다. 이러한 다면채널 구조들에 의해 동일적인 플라나 구조에 비해 채널길이가 더 길어져 높은 전류구동능력의 트랜지스터를 얻을 수 있다.

[0024] 그리고, 게이트절연막(34) 상에 제1전극(35), 제2전극(36) 및 제3전극(37)의 순서로 적층된(Stack) 게이트전극(100)이 형성된다. 게이트전극(100)에서 제1전극(35)은 30~150Å 두께이고, 제2전극(36)은 500~1000Å 두께이

며, 제3전극(37)의 두께는 제1전극(35)보다는 두껍고 제2전극(36)보다는 얇은 두께이다.

[0025] 게이트전극(100)을 자세히 살펴보면 다음과 같다.

[0026] 제1전극(35)은 게이트절연막(34)에 접촉하고, 제2전극(36)은 제1전극(35) 위에 형성된다. 여기서, 게이트절연막(34)에 접촉하는 제1전극(35)의 일함수는 제2전극(36)의 일함수보다 더 큰 범위를 갖는다.

[0027] 예를 들어, 제2전극(36)이 폴리실리콘막인 경우 제1전극(35)은 폴리실리콘막보다 더 큰 일함수를 갖는 물질이고, 제1전극(35)이 금속막인 경우에는 제2전극(36)은 금속막보다 더 작은 일함수를 갖는 물질이다. 또한, 제1전극(35)은 P형 폴리실리콘막의 일함수보다는 작고 N형 폴리실리콘막의 일함수보다는 큰 일함수를 갖는 물질이다.

[0028] 특히, 제2전극(36)이 폴리실리콘막인 경우 제1전극(35)은 금속막일 수 있고, 이때, 제2전극(36)과 제1전극(35)은 각각 N형 폴리실리콘막과 티타늄질화막(TiN)이 바람직하다. N형 폴리실리콘막의 일함수는 4eV이고, 티타늄질화막(TiN)의 일함수는 4.4~4.8eV 범위이다. 4.4~4.8eV 범위의 일함수는 P형 폴리실리콘막의 일함수(5eV)보다는 작고 N형 폴리실리콘막의 일함수(4eV)보다는 큰 중간 일함수(Mid work function)라 볼 수 있다. 제2전극(36)으로 사용된 N형 폴리실리콘막은 인(P) 또는 비소(As)와 같은 N형 불순물이 도핑되어 있다.

[0029] 상술한 바와 같이, 금속막으로 된 제1전극(35)을 게이트절연막(34) 위에 직접 형성하면, 종래 P형 폴리실리콘막을 사용함에 따른 과도한 밴드굴곡을 최소화할 수 있다. 즉, 밴드굴곡이 제1전극(35)에 걸쳐 지속되고, 통상적으로 금속막과의 계면에서는 N형 폴리실리콘막을 사용하는 경우보다 밴드굴곡이 더 억제된다.

[0030] 마지막으로, 제3전극(37)은 저저항 금속막으로서 게이트전극(100)의 시트저항을 낮추기 위해 사용된다. 일예로, 제3전극(37)은 텅스텐막 또는 텅스텐실리사이드막이다. 시트저항이 낮아지면 고속 소자 동작을 얻을 수 있다.

[0031] 한편, 제2전극(36)과 제3전극(37) 사이에는 확산배리어막(Diffusion barrier)이 더 형성될 수 있으며, 제3전극(37) 위에는 게이트하드마스크(Gate hard mask)이 더 형성될 수 있다. 확산배리어막은 제2전극(36)과 제3전극(37) 사이의 상호확산을 방지하는 확산배리어막이면서 제2전극(36)과 제3전극(37)이 반응하는 것을 방지하는 반응방지막 역할도 한다. 예컨대, 확산배리어막은 티타늄막(Ti), 티타늄질화막과 텅스텐질화막의 적층구조(Ti/TiN/WN), 티타늄막, 티타늄질화막 및 텅스텐질화막의 적층구조(Ti/TiN/WN)을 포함할 수 있다. 그리고, 게이트하드마스크막은 게이트패터닝 공정의 용이 및 후속 콘택공정에서의 게이트전극 보호 역할을 하며, 질화막을 포함한다.

[0032] 그리고, 도 3b에 도시된 바와 같이, 게이트전극(100) 양측의 기판(31) 내에는 불순물이 도핑된 접합(Junction)이 형성되어 있을 수 있다. 예컨대, N형 불순물이 도핑된 N형 소스영역(38A) 및 N형 드레인영역(38B)이 형성된다. 접합은 P형 불순물이 도핑된 소스 영역 및 드레인영역이 될 수도 있다. 여기서, N형 소스영역(38A)과 N형 드레인영역(38B)의 불순물 농도는 고농도(N^+)이며, 또는 저농도(N^-) 일 수 있다.

[0033] 도 4a는 본 발명의 제2실시예에 따른 트랜지스터의 구조 단면도이고 도 4b는 도 4a의 A-A'선에 따른 단면도이다.

[0034] 도 4a 및 도 4b에 따르면, 제2실시예의 트랜지스터는 제1실시예의 구조에 게이트전극(100)의 양측벽에 게이트측벽스페이서(Gate sidewall spacer, 39)가 더 구비되어 LDD(Lightly Doped Drain, 40) 구조를 갖는 N형 소스영역(38A) 및 N형 드레인영역(38B)이 형성된 트랜지스터 구조이다. 여기서, LDD(40)는 저농도 N형 불순물이 도핑된 구조이며, N형 소스영역 및 N형 드레인영역에 비해 N형 불순물의 농도가 낮다. 통상적으로 'N^- LDD'로 표기된다.

[0035] 한편, LDD(40) 외에 SDE(Source Drain Extension) 구조를 갖는 N형 소스영역(38A) 및 N형 드레인영역(38B)이 형성된 트랜지스터 구조도 적용이 가능하다. 여기서, SDE는 고농도 N형 불순물이 도핑된 구조이며, N형 소스영역 및 N형 드레인영역과 동일한 농도의 N형 불순물이 도핑된 것이며, 깊합의 깊이가 N형 소스영역(38A) 및 N형 드레인영역(38B)보다 더 얕다.

[0036] 상술한 제1 및 제2실시예에 따르면, 게이트절연막(34) 위에 형성된 게이트전극(100)이 서로 다른 일함수를 갖는 제1전극(35)과 제2전극(36)을 포함한다.

[0037] 특히, 제1전극(35)은 금속막이고 제2전극(36)은 N형 폴리실리콘막이므로, 제1전극(35)과 제2전극(36)은 서로 다른 일함수를 갖되, 제1전극(35)의 일함수가 4.4~4.8eV 범위가 되고, 제2전극(36)의 일함수가 4eV가 된다. 즉

제1전극(35)의 일함수가 제2전극(36)보다 더 크다.

[0038] 위와 같이, 제어트랜지스터(300) 중 금속막으로 형성된 제1전극(35) 하에 N형 폴리실리콘막으로 형성된 제2전극(36)이 존재하지만, 제어트랜지연막(34) 위에는 금속막으로 형성된 제1전극(35)이 직접 접촉하고 있기 때문에 트랜지스터의 문턱전압은 제1전극(35)의 일함수에 의해 결정된다. 제1전극(35)의 일함수가 종래 P형 폴리실리콘막보다 작기 때문에 핀드 플곡이 과도하게 발생하지 않고, 이로써 게이트유도드레인누설이 감소한다. 이를러, 앞은 두께의 제1전극(35)의 일함수가 제2전극(36)으로 사용된 N형 폴리실리콘막보다는 크기 때문에 문턱전압을 일정 수준 이상으로 증가시킬 수 있다.

[0039] 결국, P형 폴리실리콘막보다 일함수가 작은 금속막을 제어트랜연막(34)과 접촉하도록 하여 게이트전극(100)에 포지티브로써 높은 문턱전압을 얻어 오프누설을 개선함과 동시에, 제어트랜연막(34)의 결함 계면에서의 핀드 플곡을 완화시킬 수 있다.

[0040] 또한, 핀구조(33)와 같은 다면채널을 적용함으로써 채널길이를 증가시켜 전류구동능능을 향상시킬 수 있다.

[0041] 도 5는 본 일형의 제3실시예에 따른 메모리소자의 구조 단면도이다.

[0042] 도 5에 도시된 바와 같이, 기판(51) 상에 제어트랜연막(54)이 형성된다. 여기서, 기판(51)은 소자분리막(52)에 의해 여러 영역이 구분된다. 크게, 기판(51)은셀영역(Cell regions)과 주변회로영역으로 구분되고, 주변회로영역은 nMOS 영역과 pMOS 영역으로 구분된다. 한편, 셀영역은 nMOS가 형성될 nMOS 영역이다. 이하, 셀영역은 '셀 nMOS 영역'이라 하고, 주변회로영역의 nMOS 영역은 '주변회로 nMOS 영역', 주변회로영역의 pMOS 영역은 '주변회로 pMOS 영역'이라 한다.

[0043] 그리고, 셀 nMOS 영역의 기판(51)은 핀 구조(fin, 53)를 갖고, 주변회로 nMOS 영역과 pMOS 영역의 기판(51)은 표면이 평탄한 플라나(Planar) 구조를 갖는다. 여기서, 플라나 구조는 수평채널을 위한 것이고, 핀 구조(53)는 플라나구조에 비해 채널길이가 증가효과를 얻는 다면채널(Multi-plane channel)을 위한 것이다. 도 5에서는 핀구조가 도시되었으나, 셀 nMOS 영역의 기판에는 핀구조(53) 외에 리세스(Recess), 새들핀(Saddle fin), 엠브형리세스(Bulb type recess) 구조가 형성될 수 있으며, 이들에 의해 셀 nMOS 영역에 형성되는 nMOSFET는 다면 채널을 가져 플라나구조에 비해 채널길이가 더 길다.

[0044] 그리고, 각 영역의 게이트절연막(54) 상에 서로 다른 일함수값을 갖는 제어트전극(201, 202, 203)이 형성된다.

[0045] 셀 nMOS 영역의 제어트전극(201)은 제1금속막(55A)과 N형 폴리실리콘막(57B)을 포함하고, 주변회로 nMOS 영역의 제어트전극(202)은 N형 폴리실리콘막(57C)을 포함하며, 주변회로 pMOS 영역의 제어트전극(203)은 P형 폴리실리콘막(57D)을 포함한다. 한편, 각 영역의 제어트전극은 모두 최상부층에 제2금속막(59)을 더 포함하고, 각 제어트전극 상부에는 게이트하드마스크막(60)이 더 형성될 수 있다. 제2금속막(59)은 저저항 금속막으로서 제어트전극의 시트저항을 낮추기 위해 사용된다. 예컨대, 제2금속막(59)은 텅스텐막 또는 텅스텐실리사이드막이다. 그리고, 게이트하드마스크막(60)은 절화막을 포함한다.

[0046] 한편, N형 폴리실리콘막(57B, 57C)은 인(P) 또는 비소(As)와 같은 N형 불순물이 도핑된 폴리실리콘막이며, P형 폴리실리콘막(57D)은 붕소(B)와 같은 P형 불순물이 도핑된 폴리실리콘막이다. 그리고, N형 및 P형 폴리실리콘막(57B, 57C, 57D)은 500~1000Å 두께이며, 후술하겠지만 P형 폴리실리콘막(57D)은 N형 불순물이 도핑된 폴리실리콘막에 P형 불순물을 카운터도핑(Counter doping)한 것이다.

[0047] 그리고, 제1금속막(55A)은 셀영역의 게이트전극(201)에만 존재하는데, 바람직하게 제1금속막(55A)은 티타늄질화막(TiN)을 포함한다. 제1금속막(55A)은 30~150Å의 얇은 두께이다.

[0048] 도시하지 않았지만, 각 트랜지스터의 기판에는 불순물이 도핑된 접합이 형성되어 있을 수 있다. 예컨대, 셀 nMOS 영역과 주변회로 nMOS 영역의 기판에는 N형 불순물이 도핑된 소스/드레인접합이 형성되고, 주변회로 pMOS 영역의 기판에는 P형 불순물이 도핑된 소스/드레인접합이 형성될 수 있다. 또한, 게이트측벽스페이서 및 LDD 구조가 더 형성될 수도 있다.

[0049] 상술한 바에 따르면, 셀 nMOS 영역에 형성되는 트랜지스터는 핀구조(53)에 의해 핀트랜지스터(FinFET)가 되고, 주변회로 nMOS 영역 및 pMOS 영역에 형성되는 트랜지스터는 플라나트랜지스터(Planar FET)가 된다.

[0050] 특히, 셀 nMOS 영역의 게이트전극(201)은 게이트절연막(54)에 직접 접촉하는 물질이 제1금속막(55A)이므로 셀 nMOS 영역에 형성되는 트랜지스터의 문턱전압은 제1금속막(55A)에 의해 지배된다. 예컨대, 제1금속막(55A)의 일

함수는 4.4~4.6eV 범위가 되는데, 이는 N형 폴리실리콘막(57B, 57C)의 일함수(4eV)보다는 크고 P형 폴리실리콘막(57D)의 일함수(5eV)보다는 작은 값이다. 즉, 제1금속막(55A)은 중간 일함수(Mid work function)를 갖는다.

[0051] 따라서, 제1금속막(55A)의 일함수가 P형 폴리실리콘막보다 적기 때문에 밴드 굽곡이 적도하게 발생하지 않고, 이로써 게이트유도드레인누설이 감소한다. 이외에, 얇은 두께의 제1금속막(55A)의 일함수가 N형 폴리실리콘막보다는 크기 때문에 문턱전압을 일정 수준 이상으로 증가시킬 수 있다.

[0052] 결국, 셀영역에 형성되는 트랜지스터(즉, 셀트랜지스터)는 P형 폴리실리콘막보다 일함수가 적은 제1금속막(55A)을 게이트절연막(54)과 접촉하도록 하여 게이트전극(20B)에 포함시키므로써 높은 문턱전압을 얻어 오프누설을 개선함과 동시에, 게이트절연막(54)과 접합 계면에서의 밴드굽곡을 완화시킬 수 있다.

[0053] 또한, 핀구조(53)와 같은 다면채널을 적용하므로써 채널길이를 증가시켜 전류구동성능을 향상시킬 수 있다.

[0054] 도 6a 내지 도 6f는 도 5에 도시된 메모리소자의 제조 방법을 도시한 공정 단면도이다.

[0055] 도 6a에 도시된 바와 같이, 기판(51)에 각 영역간 분리를 위한 소자분리막(52)을 형성한다. 이때, 기판(51)에는 셀영역과 주변회로영역이 구분되어 있고, 주변회로영역은 nMOS 영역과 pMOS 영역이 구분되어 있다. 한편, 셀영역은 nMOS가 형성될 영역이다. 이하, 셀영역은 '셀 nMOS 영역', 주변회로영역의 nMOS 영역은 '주변회로 nMOS 영역', 주변회로영역의 pMOS 영역은 '주변회로 pMOS 영역'이라 한다.

[0056] 다음으로, 셀 nMOS 영역의 기판(51)에 핀구조(53)를 형성한다. 이때, 핀구조(53)는 소자분리막(52)의 일부를 선택적으로 리세스(Recess)시켜 형성한다. 핀구조(53)는 채널길이 증가를 위한 다면채널의 일종이다.

[0057] 이어서, 전영역의 기판(51) 상에 게이트절연막(54)을 형성한다.

[0058] 도 6b에 도시된 바와 같이, 게이트절연막(54) 상에 제1금속막(55)을 형성한다. 이때, 제1금속막(55)은 게이트전극에 포함되는 물질로서, 티타늄질화막(TiN)을 포함할 수 있다. 그리고, 제1금속막(55)은 30~150Å의 얇은 두께로 형성하여, 전 영역에서 균일한 두께를 갖고 형성된다.

[0059] 도 6c에 도시된 바와 같이, 제1금속막(55) 상에 제1감광막패턴(56)을 형성한다. 이때, 제1감광막패턴(56)은 셀 nMOS 영역은 덮고 나머지 주변회로영역은 모두 오픈시키는 패턴이다.

[0060] 이어서, 제1감광막패턴(56)을 식각장벽으로 하여 제1금속막(55)을 식각한다. 이로써, 셀 nMOS 영역의 기판(51) 상부에만 제1금속막(55A)이 잔류한다.

[0061] 도 6d에 도시된 바와 같이, 제1감광막패턴(56)을 제거한 후에, 전면에 폴리실리콘막을 증착한다. 이때, 폴리실리콘막 내에는 N형 불순물 또는 P형 불순물이 인시튜로 도핑되어 있을 수 있다. 따라서, 폴리실리콘막은 N형 폴리실리콘막 또는 P형 폴리실리콘막이 된다. 이하, 고농도의 N형 불순물(N^+라 표기)이 도핑된 N형 폴리실리콘막(57)이라 한다.

[0062] 그리고, N형 폴리실리콘막(57)은 셀 nMOS 영역에 형성되어 있는 핀구조(53)에 의해 발생된 단차를 모두 매립하는 두께가 된다. 예컨대, N형 폴리실리콘막(57)은 500~1000Å 두께로 증착한다.

[0063] 도 6e에 도시된 바와 같이, N형 폴리실리콘막(57) 상에 제2감광막패턴(58)을 형성한다. 이때, 제2감광막패턴(58)은 셀 nMOS 영역과 주변회로 nMOS 영역의 상부는 덮고 나머지 주변회로 pMOS 영역 상부는 오픈시키는 형태이다.

[0064] 이어서, 제2감광막패턴(58)을 이온주입배리어로 이용한 이온주입을 진행한다. 이때, 이온주입은 고농도의 P형 불순물(P^+라 표기)의 이온주입으로 진행하는데, 이는 N형 폴리실리콘막(57)을 P형 도전형으로 카운터 도핑시키기 위함이다. 따라서, 이온주입에 의해 주변회로 pMOS 영역의 N형 폴리실리콘막은 P형 폴리실리콘막(57A)이 된다.

[0065] 도 6f에 도시된 바와 같이, 제2감광막패턴(58)을 제거한 후에, 게이트패터닝을 진행하여 각 영역 상부에 게이트구조를 완성한다.

[0066] 게이트패터닝 결과를 살펴보면, 셀 nMOS 영역의 게이트전극(20I)은 제1금속막(55A)과 N형 폴리실리콘막(57B)을 포함하고, 주변회로 nMOS 영역의 게이트전극(202I)은 N형 폴리실리콘막(57C)을 포함하며, 주변회로 pMOS 영역의 게이트전극(203I)은 P형 폴리실리콘막(57D)을 포함한다. 한편, 각 영역의 게이트전극은 모두 최상부층에 제2금속막(59)을 더 포함하고, 각 게이트전극 상부에는 게이트하드마스크막(60)이 더 형성될 수 있다. 제2금속막(59)은

저저항 금속막으로서 게이트전극의 시트저항을 낮추기 위해 사용된다. 예컨대, 제2금속막(55)은 텅스텐막 또는 텅스텐실리사이드막이다. 그리고, 게이트하드마스크막(60)은 절화막을 포함한다.

[0067] 도시하지 않았지만, 각 영역의 트랜지스터 특성에 맞도록 불순물의 이온주입을 진행하여 소스접합 및 드레인접합을 형성한다. nMOS 영역에는 N형 소스접합 및 N형 드레인접합이 형성되고, pMOS 영역에는 P형 소스접합 및 P형 드레인접합이 형성된다. 그리고, 게이트측벽스페이서를 이용하여 LDD 구조를 더 형성할 수도 있다.

[0068] 상술한 제조 방법에 따르면, 셀영역의 nMOS 영역은 게이트절연막(54) 위에 형성된 게이트전극(201)이 서로 다른 일함수를 갖는 제1금속막(55A)과 N형 폴리실리콘막(57B)을 포함한다.

[0069] 위와 같이, 셀 nMOS 영역의 게이트전극(201)에서 제1금속막(55) 위에 N형 폴리실리콘막(57B)이 존재하지만, 게이트절연막(54) 위에는 제1금속막(55)이 직접 접촉하고 있기 때문에 트랜지스터의 문턱전압은 제1금속막(55A)의 일함수에 의해 지배된다. 제1금속막(55A)의 일함수가 P형 폴리실리콘막보다 작기 때문에 밴드 굽곡이 과도하게 발생하지 않고, 이로써 게이트유도드레인누설이 감소한다. 이울러, 얇은 두께의 제1금속막(55A)의 일함수가 N형 폴리실리콘막보다는 크기 때문에 문턱전압을 일정 수준 이상으로 증가시킬 수 있다.

[0070] 결국, P형 폴리실리콘막보다 일함수가 작은 제1금속막(55A)을 게이트절연막(54)과 접촉하도록 하여 게이트전극(201)에 포함시키므로써 높은 문턱전압을 얻어 오프누설을 개선함과 동시에, 게이트절연막(54)과 접할 채널에서의 밴드굽곡을 완화시킬 수 있다.

[0071] 또한, 원구조(59)와 같은 다면채널을 적용하므로써 채널길이를 증가시켜 전류구동성능을 향상시킬 수 있다.

[0072] 본 발명의 기술 사상은 상기 바람직한 실시예에 따라 구체적으로 기술되었으나, 상기한 실시예는 그 설명을 위한 것이며 그 제한을 위한 것이 아님을 주의하여야 한다. 또한, 본 발명의 기술 분야의 통상의 전문가라면 본 발명의 기술 사상의 범위 내에서 다양한 실시예가 가능함을 이해할 수 있을 것이다.

도면의 간단한 설명

[0073] 도 1은 종래기술에 따른 핀트랜지스터(Fin FET)를 구비한 메모리소자의 구조단면도.

[0074] 도 2는 nMOSFET에서 P형 폴리실리콘막을 게이트전극으로 사용할 때의 문제점을 설명하기 위한 도면.

[0075] 도 3a는 본 발명의 제1실시예에 따른 트랜지스터의 구조 단면도.

[0076] 도 3b는 도 3a의 A-A'선에 따른 단면도.

[0077] 도 4a는 본 발명의 제2실시예에 따른 트랜지스터의 구조 단면도.

[0078] 도 4b는 도 4a의 A-A'선에 따른 단면도.

[0079] 도 5는 본 발명의 제3실시예에 따른 메모리소자의 구조 단면도.

[0080] 도 6a 내지 도 6i는 도 5에 도시된 메모리소자의 제조 방법을 도시한 공정 단면도.

[0081] * 도면의 주요 부분에 대한 부호의 설명

[0082] 51 : 기판 52 : 소자분리막

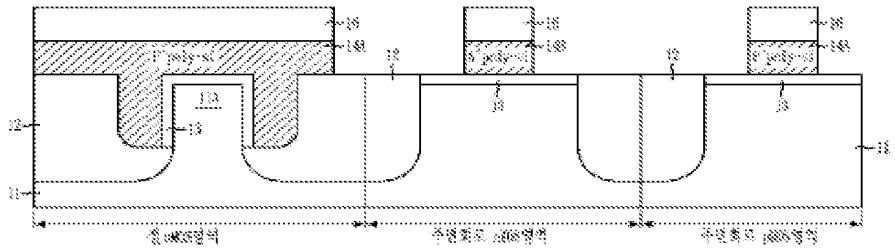
[0083] 53 : 원구조 54 : 게이트절연막

[0084] 55A : 제1금속막 57B, 57C : N형 폴리실리콘막

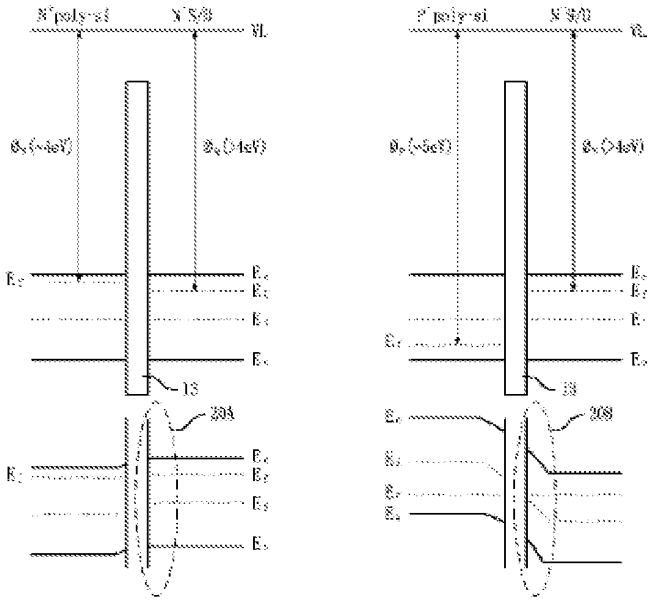
[0085] 57B : P형 폴리실리콘막 58 : 제2금속막

도면

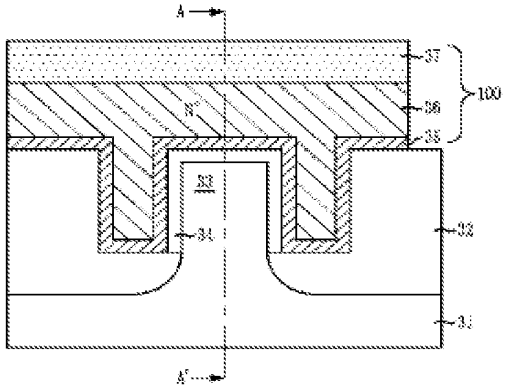
도면1



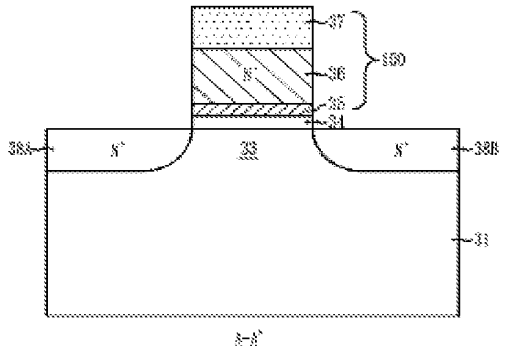
도면2



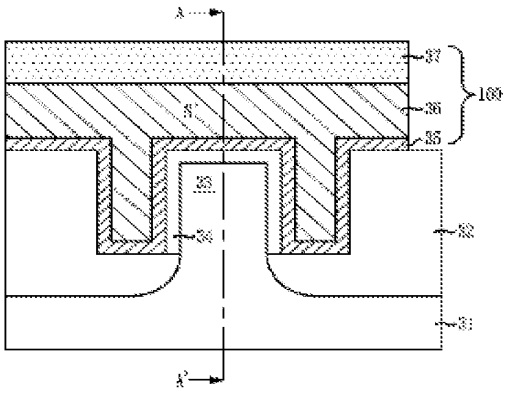
도면3a



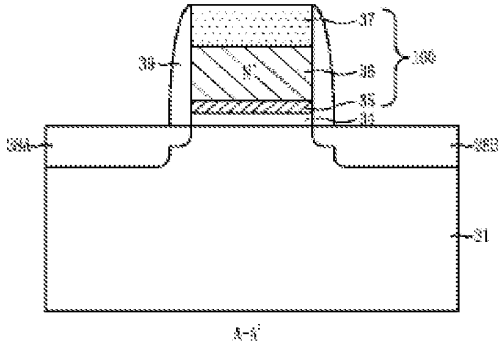
도면3b



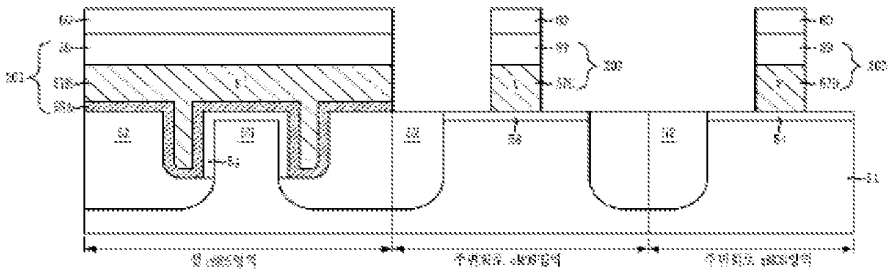
도면3a



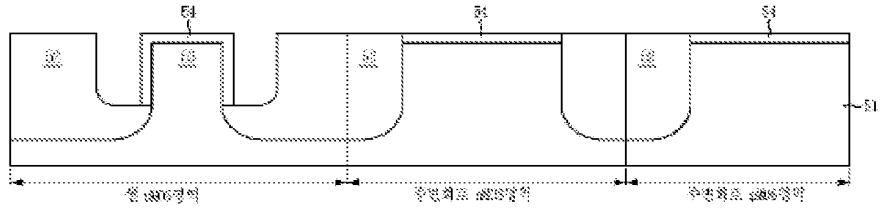
도면3b



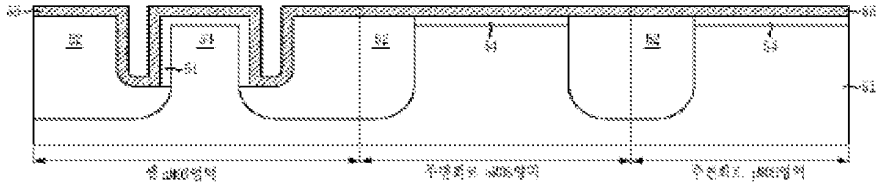
도면3c



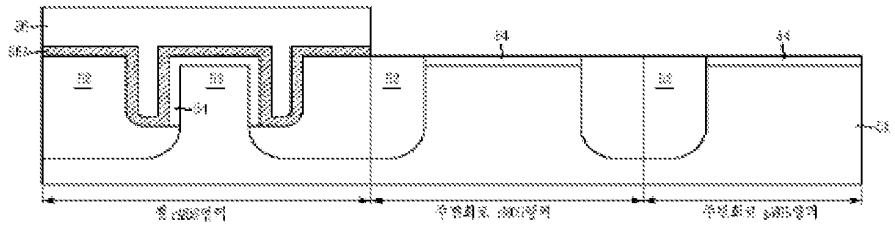
도면3c



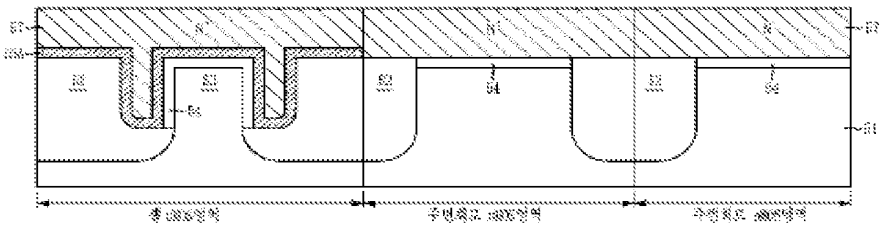
도면3d



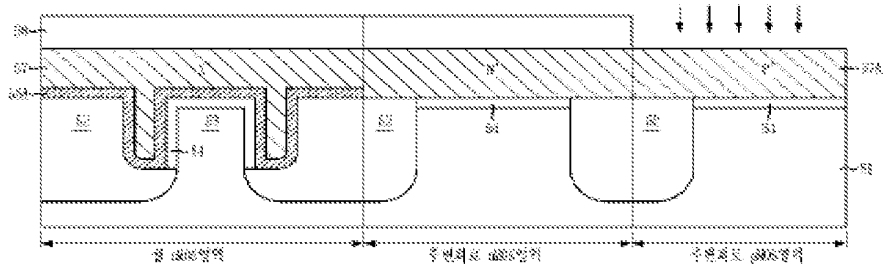
도면3e



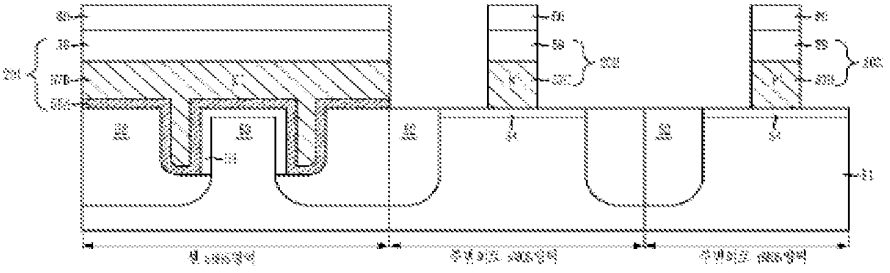
도 5f



도 5g



도 5h



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Bibliographic data: TW201110324 (A) — 2011-03-16

Semiconductor device and CMOS device and integrated circuit

Inventor(s): XU JEFF J [US]; LIN CHENG-TUNG [TW]; WANG HSIANG-YI [TW]; LEE WEN-CHIN [TW]; HSIEH BETTY [TW] ± (XU, JEFF J, ; LIN, CHENG-TUNG, ; WANG, HSIANG-YI, ; LEE, WEN-CHIN, ; HSIEH, BETTY, ; LIN, CHENG TUNG, ; WANG, HSIANG YI, ; LEE, WEN CHIN)

Applicant(s): TAIWAN SEMICONDUCTOR MFG [TW] ± (TAIWAN SEMICONDUCTOR MANUFACTURING CO., LTD)

Classification: - international: *H01L27/092; H01L29/40*
- cooperative: H01L21/823835; H01L21/823842; H01L27/092

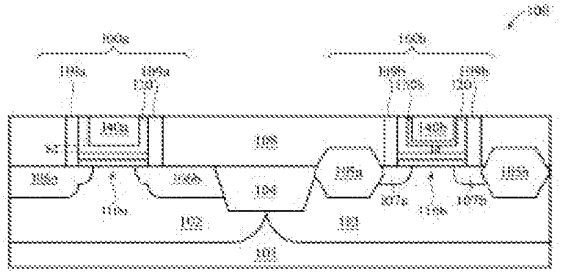
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Abstract of TW201110324 (A)

A semiconductor device is provided. The device includes a first MOS structure and a second MOS structure. The first MOS structure includes a first gate dielectric overlying a substrate, a first work function metallic layer overlying the first gate dielectric, and a first silicide overlying the first work function metallic layer. The second MOS structure includes a second gate dielectric overlying the substrate, a second work function metallic layer overlying the second gate dielectric, and a second silicide overlying the second work function metallic layer. The first silicide and the second silicide are different.



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(71)申請人：台灣積體電路製造股份有限公司 (中華民國) TAIWAN SEMICONDUCTOR MANUFACTURING CO., LTD. (TW)
新竹市新竹科學工業園區力行六路 8 號
(72)發明人：許俊豪 XU, JEFF J. (US) ；林正堂 LIN, CHENG TUNG (TW) ；王湘儀 WANG, HSIANG YI (TW) ；李文欽 LEE, WEN CHIN (TW) ；謝孟桂 HSIEH, BETTY (TW)
(74)代理人：洪澄文；顏錦順
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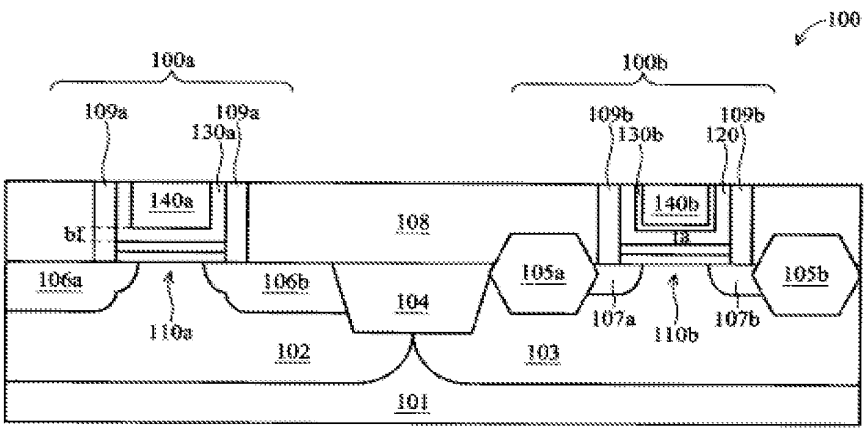
(54)名稱

半導體裝置、互補式金氧半裝置及積體電路

SEMICONDUCTOR DEVICE AND CMOS DEVICE AND INTEGRATED CIRCUIT

(57)摘要

本發明揭示一種半導體裝置，包括：一第一金氧半結構及一第二金氧半結構。第一金氧半結構，包括：一第一閘極介電層，位於一基底上；一第一功函數金屬層，位於第一閘極介電層上；以及一第一矽化物，位於第一功函數金屬層上。第二金氧半結構，包括：一第二閘極介電層，位於基底上；一第二功函數金屬層，位於第二閘極介電層上；以及一第二矽化物，位於第二功函數金屬層上。其中，第一矽化物不同於第二矽化物。



100：積體電路
100a：n 型電晶體
100b：p 型電晶體
101：基底
102：p 型井區
103：n 型井區
104：隔離結構
105a：鍺化矽結構
105b：鍺化矽結構
106a：n 型源極/汲極區
106b：n 型源極/汲極區
107a：p 型源極/汲極區

107b：p 型源極/汲極區
108：介電層
109a：間隙壁
109b：間隙壁
110a：閘極介電結構
110b：閘極介電結構
120：p 型功函數金屬層
130a：n 型功函數金屬層
130b：n 型功函數金屬層
140a：矽化物結構
140b：矽化物結構
a：底部厚度
b：底部厚度

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(71)申請人：台灣積體電路製造股份有限公司 (中華民國) TAIWAN SEMICONDUCTOR MANUFACTURING CO., LTD. (TW)
新竹市新竹科學工業園區力行六路 8 號
(72)發明人：許俊豪 XU, JEFF J. (US) ；林正堂 LIN, CHENG TUNG (TW) ；王湘儀 WANG, HSIANG YI (TW) ；李文欽 LEE, WEN CHIN (TW) ；謝孟桂 HSIEH, BETTY (TW)
(74)代理人：洪澄文；顏錦順
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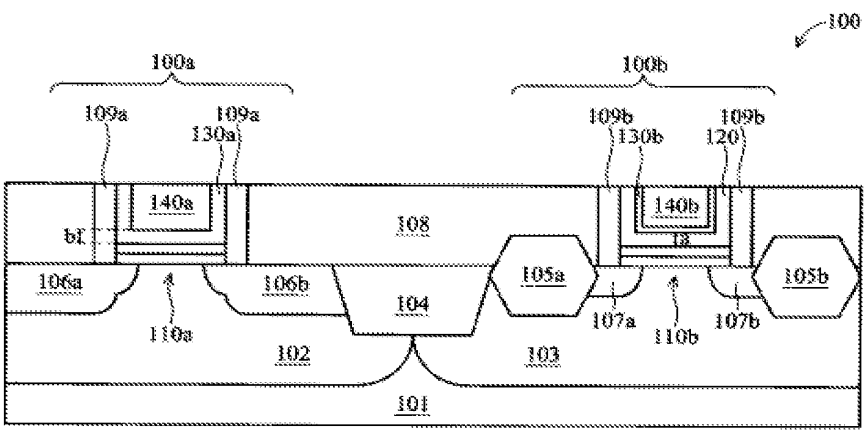
(54)名稱

半導體裝置、互補式金氧半裝置及積體電路

SEMICONDUCTOR DEVICE AND CMOS DEVICE AND INTEGRATED CIRCUIT

(57)摘要

本發明揭示一種半導體裝置，包括：一第一金氧半結構及一第二金氧半結構。第一金氧半結構，包括：一第一閘極介電層，位於一基底上；一第一功函數金屬層，位於第一閘極介電層上；以及一第一矽化物，位於第一功函數金屬層上。第二金氧半結構，包括：一第二閘極介電層，位於基底上；一第二功函數金屬層，位於第二閘極介電層上；以及一第二矽化物，位於第二功函數金屬層上。其中，第一矽化物不同於第二矽化物。



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105b：鍺化矽結構
106a：n 型源極/汲極區
106b：n 型源極/汲極區
107a：p 型源極/汲極區

六、發明說明：

【發明所屬之技術領域】

本發明係有關於一種半導體裝置，特別是有關於金屬閘極電晶體、積體電路、系統及其製造方法。

【先前技術】

半導體積體電路（integrated circuit, IC）工業歷經了快速的成長。IC材料與設計的技術進展造就了各個IC世代，每一世代的電路都比前世代來得更小更為複雜。然而，這些進展卻增加IC製造及加工的複雜度，而因應這些進展，IC製造及加工需要類似的演進。

在IC進展課題中，功能密度（即，單位晶片面積的內連裝置數量）普遍增加，而幾何尺寸（即，所使用的製程能形成的最小部件（或線））則下降。上述尺寸微縮製程因生產效率的增加及成本的降低而有所助益。而降低尺寸比例產生相對較高的功率消耗（power dissipation）值，其可藉由低功耗裝置的使用而獲得解決，例如互補式金氧半（complementary metal-oxide-semiconductor, CMOS）裝置。

在微型趨勢下，CMOS裝置中使用了各種材料作為閘極電極及閘極介電層。MOS裝置通常具有閘極氧化層及多晶矽閘極電極。而當特徵尺寸（feature size）持續下降時，這些裝置的製造希望能以高介電常數（high-k）材料取代閘極氧化層，且以金屬材料取代多晶矽閘極電極，以改善裝置效能。

【發明內容】

在本發明一實施例中，提供了一種半導體裝置，包括：一第一金氧半結構及一第二金氧半結構。第一金氧半結構，包括：一第一閘極介電層，位於一基底上；一第一功函數金屬層，位於第一閘極介電層上；以及一第一矽化物，位於第一功函數金屬層上。第二金氧半結構，包括：一第二閘極介電層，位於基底上；一第二功函數金屬層，位於第二閘極介電層上；以及一第二矽化物，位於第二功函數金屬層上。其中，第一矽化物不同於第二矽化物。

在本發明另一實施例中，提供了一種互補式金氧半裝置，包括：一 n 型金氧半結構及一 p 型金氧半結構。n 型金氧半結構，包括：一第一閘極介電結構，設置於一基底上；一第一功函數金屬層，設置於第一閘極介電結構上，第一功函數金屬層用以調整 n 型金氧半結構的一第一閘極電極的一第一功函數值；以及一第一矽化物結構，設置於第一功函數金屬層上，第一矽化物結構與第一閘極介電結構隔開，且沒有調整 n 型金氧半結構的第一閘極電極的第一功函數值。p 型金氧半結構，包括：一第二閘極介電結構，設置於基底上；一第二功函數金屬層，設置於第二閘極介電結構上，第二功函數金屬層用以調整 p 型金氧半結構的一第二閘極電極的一第二功函數值；以及一第二矽化物結構，設置於第二功函數金屬層上，第二矽化物結構與第二閘極介電結構隔開，且沒

有調整 p 型金氧半結構的第二閘極電極的第二功函數值。其中，第一矽化物結構不同於二矽化物結構。

在本發明又另一實施例中，提供了一種積體電路，包括：一 n 型電晶體及一 p 型電晶體。n 型電晶體，包括：一第一閘極介電結構，設置於一基底上；一第一 n 型功函數金屬層，設置於第一閘極介電結構上，第一 n 型功函數金屬層用以調整 n 型電晶體的一閘極電極的一功函數值；以及一第一矽化物結構，設置於第一 n 型功函數金屬層上，第一矽化物結構具有金屬對矽的一第一組成比。p 型電晶體，包括：一第二閘極介電結構，設置於基底上；一第二 p 型功函數金屬層，設置於第二閘極介電結構上，第二 p 型功函數金屬層用以調整 p 型電晶體的一閘極電極的一功函數值；以及一第二矽化物結構，設置於第二 p 型功函數金屬層上，第二矽化物結構具有金屬對矽的一第二組成比。其中，第一組成比大於第二組成比。

【實施方式】

傳統上，形成金屬閘極電極可分為先閘極（gate-first）法與後閘極（gate-last）法。對於先閘極法來說，金屬閘極係於形成電晶體的源極/汲極區之前形成。而後閘極法則在基底內形成源極/汲極區且在內層介電（interlayer dielectric, ILD）層內形成犧牲閘極（dummy gate）。去除犧牲閘極，以在內層介電層內形成一開口。接著在開口內填入金屬閘極電極。先閘極法與後閘極法可用於形

成金屬閘極 CMOS 電晶體。

習知金屬閘極 CMOS 電晶體包括一金屬閘極 PMOS 電晶體及一金屬閘極 NMOS 電晶體。金屬閘極 NMOS 電晶體及金屬閘極 PMOS 電晶體兩者具有 n 型及 p 型功函數材料。另外，金屬閘極 NMOS 電晶體包括一 n 型功函數材料設置於 p 型功函數材料上。CMOS 電晶體使用鋁作為導電材料。

在此發現了鋁（Al）可擴散及/或穿透進入 p 型及 n 型功函數材料、高介電（high-k）材料、及/或電晶體的通道區。為了防止鋁的擴散，會在功函數材料與鋁之間形成擴散阻障結構。習知擴散阻障材料由氮化鈦（TiN）層、鈦（Ti）層及/或氮化鉭（TaN）層所組成。習知擴散阻障層的厚度可約在 180Å，以防止鋁擴散進入 p 型及 n 型功函數材料及/或電晶體的通道區。

需注意的是習知後閘極法中去除了犧牲閘極，以形成製做金屬閘極電極的凹口。功函數材料、擴散阻障材料、及鋁依序地形成於凹口內。功函數材料及擴散阻障材料形成於凹口的側壁及底部。形成於側壁的功函數材料及擴散阻障材料縮減了用以填入鋁的凹口的開口寬度。若製程技術微縮至 25nm 或以下，則難以在狹窄的凹口內填入鋁。

另外，在此也發現了 PMOS 電晶體同樣使用 p 型功函數材料降低鋁的擴散。傳統上，p 型功函數材料層的厚度約在 150Å。位於凹口側壁上厚的 p 型功函數材料層進一步縮減了用以填入鋁的凹口的開口寬度而更加難以填

入鋁。

有鑑於此，有必要尋求新的金屬閘極電晶體、積體電路、系統及其製造方法。

要瞭解的是本說明書以下的揭露內容提供許多不同的實施例或範例，以實施本發明的不同特徵。而本說明書以下的揭露內容是敘述各個構件及其排列方式的特定範例，以求簡化發明的說明。當然，這些特定的範例並非用以限定本發明。另外，本發明的說明中不同範例可能使用重複的參考符號及/或用字。這些重複符號或用字係為了簡化與清晰的目的，並非用以限定各個實施例及/或所述外觀結構之間的關係。再者，本說明書以下的揭露內容敘述了將一特徵形成於另一特徵之上、連接至及或耦接至另一特徵，即表示其包含了所形成的上述特徵是直接接觸的實施例，亦包含了尚可將額外的特徵形成於這些特徵之間而使這些特徵並未直接接觸的實施例。另外，在空間上的相關用語，例如”下”、”上”、”水平”、”垂直”、”上方”、”下方”、”向上”、”向下”、”頂部”、”底部”等等及其派生詞（例如，”水平地”、”向下地”、”向上地”等等）係用以容易表達出本說明書中的特徵與額外特徵的關係。這些空間上的相關用語涵蓋了具有特些特徵的裝置的不同方位。

第 1 圖係繪示出具有 p 型電晶體與 n 型電晶體的積體電路剖面示意圖。請參照第 1 圖，積體電路 100 可包括設置於一基底 101 上的一 n 型電晶體（NMOS）100a

及一 p 型電晶體（PMOS）100b，。在一些實施例中，積體電路 100 可包括一 CMOS 電晶體、一記憶體陣列、一邏輯電路、一數位電路、一類比電路、其他電路及/或其組合。

基底 101 可包括一元素半導體，其包含結晶矽或鍺、多晶矽、或一非晶矽結構；一化合物半導體，其包含碳化矽、砷化鎵、磷化鎵、磷化銦、砷化銦及銻化銦；一合金半導體，其包含 SiGe、GaAsP、AlInAs、AlGaAs、GaInAs、GaInP 及 GaInAsP；任何適當材料及/或其組合。在一實施例中，合金半導體基底可具有漸變 SiGe 特徵，其中漸變 SiGe 特徵為 Si 及 Ge 的組成變化從漸變 SiGe 特徵位於一位置的一比率至位於另一位置的另一比率。在其他實施例中，合金 SiGe 形成於一矽基底上方。在另一實施例中，SiGe 基底為受應變的基底。再者，半導體基底可為絕緣層上覆半導體（例如，絕緣層上覆矽（silicon on insulator, SOI））或是薄膜電晶體（thin film transistor, TFT）。在其他範例中，半導體基底可包含一摻雜的磊晶（epi）層或一埋入層。在其他範例中，化合物半導體基底可具有一多層結構或包含一多層化合物半導體結構。

請參照第 1 圖，積體電路 100 可包括形成於基底 101 內的一 p 型井區 102 及一 n 型井區 103。p 型井區 102 及 n 型井區 103 可用於分別提供 n 型電晶體 100a 及 p 型電晶體 100b 的通道區。

積體電路 100 可包括設置於 n 型電晶體 100a 與 p 型電晶體 100b 之間的隔離結構 104。隔離結構 104 使 n 型

電晶體 100a 與 p 型電晶體 100b 絕緣。在一些實施例中，隔離結構 104 可為淺溝槽隔離（shallow trench isolation, STI）結構、局部矽氧化（local oxidation of silicon, LOCOS）結構或其他隔離結構。

在一些實施例中，p 型電晶體 100b 可包括鍺化矽（SiGe）結構 105a 及 105b，其分別相鄰於 p 型源極/汲極區 107a 及 107b。p 型源極/汲極區 107a 及 107b 可相鄰於 p 型電晶體 100b 的通道區。n 型電晶體 100a 可包括 n 型源極/汲極區 106a 及 106b，其相鄰於 n 型電晶體 100a 的通道區。

在一些實施例中，n 型源極/汲極區 106a 及 106b 可具有摻雜物，例如砷（As）、磷（P）、其他五族元素或其組合。p 型源極/汲極區 107a 及 107b 可具有摻雜物，例如硼（B）或其他三族元素。在其他實施例中，源極/汲極區可包括降低電阻值的矽化物。矽化物可包括：如，矽化鎳（NiSi）、矽化鎳鉑（NiPtSi）、矽化鎳鉑鍺（NiPtGeSi）、矽化鎳鍺（NiGeSi）、矽化鐿（YbSi）、矽化鉑（PtSi）、矽化銥（IrSi）、矽化鉺（ErSi）、矽化鈷（CoSi）、其他適合的材料及/或其組合。用以製作矽化物的材料可透過沉積技術來形成，例如物理氣相沉積（PVD）（如，濺鍍或蒸鍍）、電鍍、化學氣相沉積（CVD）（如，電漿輔助化學氣相沉積（plasma ehanced CVD, PECVD）、常壓化學氣相沉積（atmospheric pressure CVD, APCVD）、低壓化學氣相沉積（low pressure CVD, LPCVD）、高密度電漿化學氣相沉積（high density plasma

CVD, HDPCVD)、原子層化學氣相沉積(atomic layer CVD, ALCVD))、其他適當的沉積製程及/或其組合。在進行上述沉積之後，可進行矽化金屬沉積(salicidation)製程而使沉積的材料與摻雜區之間在高溫(elevated temperature)下發生反應，該溫度取決於材料。上述步驟也可稱為退火(annealing)，其包括快速熱製程(rapid thermal process, RTP)。發生反應的矽化物可透過單一步驟RTP或是多重步驟RTP而形成。

請再參照第1圖，至少一介電層108設置於基底101上。介電層108可包括：如，氧化物、氮化物、氮氧化物、低介電常數(low-k)材料、超低介電常數材料、極低介電常數材料、其他介電材料及/或其組合。介電層108可透過諸如CVD製程、HDPCVD製程、高縱深比填溝製程(high aspect ratio process, HARP)、旋塗(spin-coating)製程、其他適當的沉積製程及/或其組合。在一些實施例中，介電層108可稱為內層介電(interlayer dielectric, ILD)層。在其他實施例中，額外的介電層(未繪示)可形成於介電層108的下方或上方。

在一些實施例中，間隙壁109a及109b可分別相鄰於n型電晶體100a與p型電晶體100b。間隙壁109a及109b的材料可包括：如，氧化物、氮化物、氮氧化物及/或其他介電材料。

n型電晶體100a可包括設置於一基底101上的一閘極介電結構110a。一n型功函數金屬層130a可設置於閘極介電結構110a上。n型功函數金屬層130a係用以調整

n 型電晶體 100a 的閘極電極的功函數值。一矽化物結構 140a 可設置於 n 型功函數金屬層 130a 上。矽化物結構 140a 可與閘極介電結構 110a 隔開，且大體上不改變 n 型電晶體 100a 的閘極電極的功函數值。在一些使用 25-nm 技術的實施例中，矽化物結構 140a 與閘極介電結構 110a 隔開的距離可為 30Å 或以上。

p 型電晶體 100b 可包括設置於基底 101 上的一閘極介電結構 110b。一 p 型功函數金屬層 120 可設置於閘極介電結構 110b 上。p 型功函數金屬層 120 係用以調整 p 型電晶體 100b 的閘極電極的功函數值。一 n 型功函數金屬層 130b 可設置於 p 型功函數金屬層 120 上。一矽化物結構 140b 可設置於 n 型功函數金屬層 130b 上。矽化物結構 140b 可與閘極介電結構 110b 隔開，且大體上不改變 p 型電晶體 100b 的閘極電極的功函數值。在一些使用 25-nm 技術的實施例中，矽化物結構 140b 與閘極介電結構 110b 隔開的距離可為 30Å 或以上。

請再參照第 1 圖，每一閘極介電結構 110a 及 110b 可為一單層結構或多層結構。在一些實施例中，每一閘極介電結構 110a 及 110b 可包括：一界面層（如，氧化矽層）及一高介電常數材料層設置於界面層上。在一些實施例中，高介電常數材料層可包括：氧化鉿（HfO_2）、氧化矽鉿（HfSiO）、氮氧化矽鉿（HfSiON）、氧化鉭鉿（HfTaO）、氧化鈦鉿（HfTiO）、氧化鋯鉿（HfZrO）、其他適當的高介電常數材料及/或其組合。高介電常數材料可進一步擇自於金屬氧化物、金屬氮化物、金屬矽酸

鹽、過渡金屬氧化物、過渡金屬氮化物、過渡金屬矽酸鹽、金屬氮氧化物、金屬鋁酸鹽、鋯矽酸鹽、鋯鋁酸鹽、氧化矽、氮化矽、氮氧化矽、氧化鋯、氧化鈦、氧化鋁、氧化鉿-氧化鋁（HfO_2-Al_2O_3）合金、其他適當材料及/或其組合。高介電常數材料可透過適當製程而形成，如原子層沉積（atomic layer deposition, ALD）、化學氣相沉積（chemical vapor deposition, CVD）、物理氣相沉積（physical vapor deposition, PVD）、遙控電漿化學氣相沉積（remote plasma CVD, RPCVD）、PECVD、金屬有機化學氣相沉積（metal organic CVD, MOCVD）、濺鍍、電鍍、其他適當製程及/或其組合。

p型功函數金屬層120可包括：如，金屬、金屬碳化物、金屬氮化物、其他能夠提供電晶體所需功函數的材料。在一些實施例中，p型功函數金屬層120可包括：釘、鈀、鈷、鎳及導電的金屬氧化物（例如，氧化釕）、其他能夠調整p型電晶體100b的閘極電極的功函數值的p型金屬材料或其組合。在其他實施例中，p型功函數金屬層120可包括TiN。p型功函數金屬層120能夠提供p型電晶體100b的閘極電極的功函數值約為4.8 eV或以上。在一些實施例中，p型功函數金屬層120可具有約100Å或以上的一底部厚度"a"。在其他使用25-nm技術的實施例中，p型功函數金屬層120的底部厚度"a"約30Å。

n型功函數金屬層130a及130b可包括：如，金屬、金屬碳化物、金屬氮化物、其他能夠提供電晶體所需功函數的材料。在一些實施例中，n型功函數金屬層130a

及 130b 可包括：鉿、鋯、鈦、鉭、鋁、金屬碳化物、其他能夠調整 n 型電晶體 100a 的閘極電極的功函數值的 n 型金屬材料或其組合。在其他實施例中，n 型功函數金屬層 130a 及 130b 可包括 TiAl。n 型功函數金屬層 130a 及 130b 能夠提供 n 型電晶體 100a 的閘極電極的功函數值約為 4.5 eV 或以下。在一些實施例中，n 型功函數金屬層 130a 可具有約 30Å 的一底部厚度"b"。

請再參照第 1 圖，矽化物結構 140a 及 140b 可用於電性傳輸。矽化物結構 140a 及 140b 可包括：矽化物線、矽化物塊材、矽化物插塞（plug）及/或其他矽化物型式。在一些實施例中，每一矽化物結構 140a 及 140b 實質上本體部分為矽化物材料。需注意的是矽化物結構 140a 及 140b 最好是分別與閘極介電結構 110a 及 110b 隔開。n 型電晶體 100a 及 p 型電晶體 100b 的功函數實質上分別不受矽化物結構 140a 及 140b 影響及/或調整。

在一些實施例中，矽化物結構 140a 及 140b 可包括：如，矽化鎳（NiSi）、矽化鎳鉑（NiPtSi）、矽化鎳鉑鍺（NiPtGeSi）、矽化鎳鍺（NiGeSi）、矽化鐿（YbSi）、矽化鉑（PtSi）、矽化銥（IrSi）、矽化鉺（ErSi）、矽化鈷（CoSi）、矽化鈦（TiSi）、其他適合的材料及/或其組合。用以製作矽化物的材料可透過沉積技術來形成，例如 PVD（如，濺鍍或蒸鍍）、電鍍、CVD（如，PECVD、APCVD、LPCVD、HDPCVD、ALCVD）、其他適當的沉積製程及/或其組合。在進行上述沉積之後，可進行矽化金屬沉積製程而使沉積的材料與摻雜區之間在

高溫下發生反應，該溫度取決於材料。上述步驟也可稱為退火，其包括 RTP。發生反應的矽化物可透過單一步驟 RTP 或是多重步驟 RTP 而形成。

矽化物結構 140a 及 140b 可分別在 n 型電晶體 100a 及 p 型電晶體 100b 的通道區內提供應變。矽化物結構 140a 的應力可不同於矽化物結構 140b 的應力，以分別在 n 型電晶體 100a 及 p 型電晶體 100b 的通道區內提供不同的應變。舉例來說，矽化物結構 140a 具有壓縮應力，而矽化物結構 140b 具有中性或拉伸應力。矽化物結構 140a 的材料可不同於矽化物結構 140b 的材料，以分別在 n 型電晶體 100a 及 p 型電晶體 100b 的通道區內提供不同的應變。在一實施例中，矽化物結構 140a 及 140b 可由不同的矽化物所構成，例如，矽化鈷與矽化鎳。在另一實施例中，矽化物結構 140a 及 140b 可由相同的矽化物不同的組成比（金屬對矽的比率）所構成，例如，$Co_2Si/CoSi/CoSi_2$ 或 $Ni_2Si/NiSi/NiSi_2$。在一實施例中，在 n 型電晶體 100a 的通道區內施加一拉伸應變，而在 p 型電晶體 100b 的通道區內施加一中性應變。在另一實施例中，在 n 型電晶體 100a 的通道區內施加一拉伸應變，而在 p 型電晶體 100b 的通道區內施加一壓縮應變。

需注意的是第 1 圖的結構僅為示範說明。內連線結構（未繪示）可形成於介電層 108 上，用以作為電性連接。內連線結構可包括：各種介電材料、介層窗（via）結構、金屬線、單鑲嵌結構、雙鑲嵌結構、鈍化保護（passivation）層、其他所需的半導體結構及/或其組合。