

需注意的是習知金屬閘極 CMOS 電晶體使用 Al 作為電性傳輸的閘極電極塊材。Al 會擴散進入 p 型功函數材料、高介電常數材料及/或 CMOS 電晶體的通道區。習知金屬閘極 CMOS 電晶體使用擴散阻障層（例如，TiN、Ti 及/或 TaN）以防止 Al 擴散及/或穿透進入 n 型或 p 型功函數材料高介電常數材料及/或電晶體的通道區。

相較於習知金屬閘極 CMOS 電晶體，積體電路 100 使用矽化物結構 140a 及 140b 取代 Al 作為電性傳輸及/或應力源（stressor）的閘極電極塊材。透過不使用 Al 作為導電材料，可實質上排除 Al 擴散的問題。積體電路 100 的功函數金屬層 130a 與矽化物結構 140a 之間以及功函數金屬層 130b 與矽化物結構 140b 之間可不具有擴散阻障層，例如 TiN、Ti 及/或 TaN。

矽化物結構 140a 及 140b 可分別在 n 型電晶體 100a 及 p 型電晶體 100b 的通道區內提供不同的應變。矽化物結構 140a 可在 n 型電晶體 100a 的通道區內形成拉伸應變，以增加 n 型電晶體 100a 的通道區內的電子遷移率。矽化物結構 140b 可在 p 型電晶體 100b 的通道區內形成壓縮或中性應變，以增加或至少實質上不降低 p 型電晶體 100b 的通道區內的電洞遷移率。

第 2A 至 2L 圖係繪示出一實施例之利用後閘極法形成具有 CMOS 電晶體的積體電路的流程剖面示意圖。第 2A 至 2L 圖中相同於第 1 圖的部件係以相同的標號再加上 100 來表示。

請參照第 2A 圖，犧牲閘極 211a 及 211b 可分別形成

於閘極介電結構 210a 及 210b 上。犧牲閘極 211a 及 211b 的材料可包括：如，矽、多晶矽、非晶矽及相對於介電層 208 及間隙壁 209a 及 209b 具有所需蝕刻率的其他材料。犧牲閘極 211a 及 211b 可透過沉積製程、微影圖案化、蝕刻製程及/或其組合而形成。沉積製程可包括：CVD、ALD、其他適當方法及/或其組合。微影圖案化可包括：光阻塗佈（如，旋塗法）、軟烤、光罩對準、曝光、後曝烤、光組顯影、清洗、乾燥（如，硬烤）、其他適當製程及/或其組合。曝光製程可以其他適當的方法來實施或取代，如無光罩式（maskless）微影、電子束寫入、離子束寫入、分子拓印（molecular imprint）。蝕刻製程可包括：乾蝕刻、濕蝕刻及/或其他蝕刻方法（如，反應離子蝕刻（reactive ion etching, RIE））。蝕刻製程也可為純化學蝕刻（如，電漿蝕刻）、純物理蝕刻（如，離子研磨（ion milling））及/或其組合。

請參照第 2B 圖，犧牲閘極 211a 及 211b（如第 2A 圖所示）可去除以分別形成開口 212a 及 212b。可透過濕蝕刻、乾蝕刻、其他去除製程及/或其組合，以去除犧牲閘極 211a 及 211b。在一些實施例中，開口 212a 及 212b 可包括至少一上蓋層（未繪示）設置於高介電常數材料層上。上蓋層能夠保護高介電常數材料層而不因去除犧牲閘極 211a 及 211b 所進行的製程而損害。在一些實施例中，上蓋層的材料包括：如，TiN、TaN、其它能阻止去除製程的適當材料及/或其組合。

請參照第 2C 圖，一保護層（未繪示）及一 p 型功函

數層 220 可形成於第 2B 圖所示的結構上。保護層，例如 TaN，可在後續定義 p 型功函數金屬層 220a 的製程保護下方的結構。p 型功函數層 220 可提供 p 型電晶體 200b 的閘極電極所需的功函數值。保護層及 p 型功函數層 220 可透過任何適當的製程而形成，例如 ALD、CVD、PVD、RPCVD、PECVD、MOCVD、濺鍍、電鍍、其他適當製程及/或其組合。

請參照第 2D 圖，可形成一介電材料 221a，例如，旋塗玻璃 (spin-on glass, SOG)，以覆蓋 p 型電晶體 200b 區域並填入開口 212b (如第 2C 圖所示)。可在介電材料 221a 上定義形成一光阻 221b。介電材料 221a 及/或光阻 221b 可用於圖案化 p 型電晶體 200b 上的 p 型功函數層 220。可透過旋塗製程、微影製程及蝕刻製程來定義介電材料 221a 及光阻 221b。

請參照第 2E 圖，可去除未被介電材料 221a 及光阻 221b 所覆蓋的部分 p 型功函數層 220，以定義出 p 型功函數金屬層 220a。在定義出 p 型功函數金屬層 220a 之後，可透過濕蝕刻、乾蝕刻及/或其組合，以去除介電材料 221a 及光阻 221b 而露出 p 型功函數金屬層 220a。

請參照第 2F 圖，一 n 型功函數層 230 可形成於第 2E 圖所示的結構上。n 型功函數層 230 可提供 n 型電晶體 200a 的閘極電極所需的功函數值。n 型功函數層 230 可透過任何適當的製程而形成，例如 ALD、CVD、PVD、RPCVD、PECVD、MOCVD、濺鍍、電鍍、其他適當製程及/或其組合。

請參照第 2G，一矽層 235，例如多晶矽或非晶矽，可形成於 n 型功函數層 230 上並填入開口 212a 及 212b（如第 2F 圖所示）。係層 235 可透過 CVD 而形成，例如 HDPCVD、ALCVD 等等。

請參照第 2H 圖，進行的去除製程 250 可去除部分的矽層 235，使矽塊材 235a 及 235b 的上表面（未標示）實質上切齊於介電層 208 的上表面 208a。去除製程 250 包括：化學機械研磨（chemical-mechanical polishing, CMP）、乾蝕刻、濕蝕刻及/或其組合。

請參照第 2I 圖，進行的去除製程 260 可去除部分的矽塊材 235a，使矽塊材 235a 的上表面 236a 低於介電層 208 的上表面 208a 一既定距離。矽塊材 235b 被一光阻圖案層 236b 所覆蓋，以防止在進行去除製程 260 期間被去除，使凹陷的矽塊材 235a 薄於矽塊材 235b。凹陷的矽塊材 235a 的高度約為矽塊材 235b 高度的 1/6 至 1/2。去除製程 260 可包括乾蝕刻。

請參照第 2J 圖，在去除光阻圖案層 236b 之後，一金屬層 237 及一上蓋層 238 可依序形成於凹陷的矽塊材 235a、矽塊材 235b 及介電層 208 上。金屬層 237 的高度約為凹陷的矽塊材 235a 高度的 1/2 至 2 倍。金屬層 237 的材料可包括：如，鎳、鎳鉑、鎳鉑鍍、鎳鍍、鎳、鉑、鉍、鉕、鈷、鈦、其他適合的材料及/或其組合。金屬層 237 係用以形成一矽化物結構，其可透過沉積而形成，如使用濺鍍、蒸鍍、電鍍、PECVD、APCVD、LPCVD、HDPCVD、ALCVD、其他適當的沉積製程及/或其組合。

上蓋層 238 可包括：如，TiN、TaN、其他適當導電材料及/或其組合。上蓋層 238 可透過 CVD、PVD、ALD 及/或其他適當的製程而形成。

請參照第 2K 圖，進行一熱製程 270，其能夠使金屬層 237 與凹陷的矽塊材 235a 及矽塊材 235b 發生反應而形成矽化物結構 240a 及 240b。在一些實施例中，熱製程 270 可使矽塊材 235a 及矽塊材 235b 整體部分與金屬層 237 發生反應而形成矽化物結構 240a 及 240b。熱製程 270 可在高溫下進行，而溫度擇取決於金屬層 237 的材料。在一些實施例中，熱製程 270 也稱作退火，其可包括 RTP。可透過單一步驟 RTP 或多重步驟 RTP 來形成矽化物。

由於矽化物結構 240a 及 240b 的材料不同，因此可分別在 n 型電晶體 200a 及 p 型電晶體 200b 的通道區內提供不同的應變。在一實施例中，由於凹陷的矽塊材 235a 及矽塊材 235b 的高度不同，因此矽化物結構 240a 及 240b 內的金屬對矽的比率不同。在另一實施例中，由於使用不同的金屬來形成矽化物結構 240a 及 240b，因此矽化物結構 240a 及 240b 內的金屬不同。由於凹陷的矽塊材 235a 的高度低於矽塊材 235b 的高度，因此矽化物結構 240a 中金屬對矽的組成比可高於矽化物結構 240b 的組成比。舉例來說，透過使用鎳來作為金屬層 237，使矽化物結構 240a 及 240b 可分別為 Ni_2Si 及 NiSi_2 。 Ni_2Si 的初始體積大於由 n 型功函數金屬層 230a 所定義出的空間，使 Ni_2Si 具有壓縮應力而在 n 型電晶體 200a 的通道區內形成拉伸

應變並且增加 n 型電晶體 200a 的通道區內的電子遷移率。 NiSi_2 的初始體積小於或相似於由 p 型功函數金屬層 230b 所定義出的空間，使 NiSi_2 具有拉伸或中性應力而在 p 型電晶體 200b 的通道區內形成壓縮或中性應變並且增加或實質上不降低 p 型電晶體 200b 的通道區內的電洞遷移率。

矽化物結構 240a 可包括： Ni_2Si 、 Co_2Si 、 NiSi 、 CoSi 、 Ti_5Si_3 、 TiSi 或其組合。矽化物結構 240b 可包括： NiSi_2 、 NiSi 、 CoSi_2 、 CoSi 、 TiSi 、 TiSi_2 或其組合。

由於矽化物結構 240a 的初始體積大於矽化物結構 240b，因此上表面 241a 可高於上表面 241b。需注意的是金屬層 237 實質上不與介電層 208 發生交互作用。矽化物不會形成於介電層 208 與金屬層 237 之間。在一些實施例中，包括第 2H 至 2K 圖所述的製程的矽化金屬沉積製程也可稱為選擇性矽化金屬沉積製程。

請參照第 2L 圖，進行一去除製程 280，其可去除上蓋層 238 及金屬層 237 未反應的部分。去除製程 280 可包括濕蝕刻製程、乾蝕刻製程、CMP 及/或其組合。

需注意的是第 2A 至 2L 圖所示的方法可形成作為電性傳輸的矽化物結構 240a 及 240b。同樣需注意的是矽化物結構 240a 及 240b 可分別在 n 型電晶體 200a 及 p 型電晶體 200b 的通道區內提供不同的應變，以分別增加 n 型電晶體 200a 及 p 型電晶體 200b 的通道區內電子及電洞遷移率。

需注意的是第 2A 至 2L 圖所示的方法僅為範例說

明。所屬技術領域中具有通常知識者可更動方法流程以獲得所需的金屬閘極電晶體。舉例來說，若要單獨使用光阻 221b 來定義 p 型功函數金屬層 220a，可免去形成及定義介電材料 221a 的製程步驟。

在其他實施例中，p 型電晶體 200b 不包含 n 型功函數金屬層 230b。在一些實施例中，可使用額外的微影製程、蝕刻製程及/或清潔製程，而只在 n 型電晶體 200a 中形成 n 型功函數金屬層 230a。

在其他實施例中，可免去用以形成凹陷的矽塊材 235a 的去除製程 260。在一些實施例中，介電層 208 的上表面 208a 實質上切齊或高於矽化物結構 240a 及 240b 的上表面 241a 及 241b。

第 3 圖係繪示出具有設置於基材板上的積體電路的系統剖面示意圖。請參照第 3 圖，一系統 300 可包括設置於一基材板 (substrate board) 301 上的一積體電路 302 (未繪示)。基材板 301 可包括印刷電路板 (printed circuit board, PCB)、印刷線路板 (printed wiring board) 及/或其它能夠承載積體電路的載板。積體電路 302 可相似於第 1 圖所示的積體電路 100。積體電路 302 可電性耦接至基材板 301。在一些實施例中，積體電路 302 可透過凸塊 (bump) 305 而電性耦接至基材板 301。在其他實施例中，積體電路 302 可透過打線 (wire bonding) 而電性耦接至基材板 301。系統 300 可為電子系統 (如，電腦、無線通訊裝置、電腦相關週邊、娛樂裝置等等) 的一部分。

在一些實施例中，包括積體電路 302 的系統 300 可

在單一 IC 上提供整個系統，因而稱為晶片系統(system on a chip, SOC) 或是積體電路系統 (system on integrated circuit, SOIC) 裝置。這些 SOC 裝置可在單一積體電路中提供製造手機、個人數位助理 (personal data assistant, PDA)、數位 VCR、數位攝錄像機 (camcorder)、數位相機、或 MP3 播放器等等所需的所有電路。

以上敘述許多實施例的特徵，使所屬技術領域中具有通常知識者能夠清楚理解以下的說明。所屬技術領域中具有通常知識者能夠理解其可利用本發明揭示內容作為基礎，以設計或更動其他製程及結構而完成相同於上述實施例的目的及/或達到相同於上述實施例的優點。所屬技術領域中具有通常知識者亦能夠理解不脫離本發明之精神和範圍的等效構造可在不脫離本發明之精神和範圍內作任意之更動、替代與潤飾。

【圖式簡單說明】

第 1 圖係繪示出一實施例之具有 P 型及 N 型電晶體的積體電路剖面示意圖。

第 2A 至 2L 圖係繪示出一實施例之利用後閘極法形成具有 CMOS 電晶體的積體電路的流程剖面示意圖。

第 3 圖係繪示出具有設置於基材板上的積體電路的系統剖面示意圖。

【主要元件符號說明】

100、200~積體電路；

100a、200a~n 型電晶體；

100b、200b~p 型電晶體；

101、201~基底；

102、202~p 型井區；

103、203~n 型井區；

104、204~隔離結構；

105a、105b、205a、205b~鍺化矽結構；

106a、106b、206a、206b~n 型源極/汲極區；

107a、107b、207a、207b~p 型源極/汲極區；

108、208~介電層；

109a、109b、209a、209b~間隙壁；

110a、110b、210a、210b~閘極介電結構；

120、220a~p 型功函數金屬層；

130a、130b、230a、230b~n 型功函數金屬層；

140a、140b、240a、240b~矽化物結構；

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208a、236a、241a、241b~上表面；

211a、211b~犧牲閘極；

212a、212b~開口；

220~p型功函數層；

221a~介電材料；

221b~光阻；

230n~型功函數層；

235~矽層；

235a、235b~矽塊材；

236b~光阻圖案層；

237~金屬層；

238~上蓋層；

250、260、280~去除製程；

270~熱製程；

a、b~底部厚度。

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發明專利說明書

(本說明書格式、順序，請勿任意更動，※記號部分請勿填寫)

※申請案號：99/30663

※申請日：99.8.10

※IPC 分類：

H01L27/1092 (2006.01)

H01L29/40 (2006.01)

一、發明名稱：(中文/英文)

半導體裝置、互補式金氧半裝置及積體電路

SEMICONDUCTOR DEVICE AND CMOS DEVICE
AND INTEGRATED CIRCUIT

二、中文發明摘要：

本發明揭示一種半導體裝置，包括：一第一金氧半結構及一第二金氧半結構。第一金氧半結構，包括：一第一閘極介電層，位於一基底上；一第一功函數金屬層，位於第一閘極介電層上；以及一第一矽化物，位於第一功函數金屬層上。第二金氧半結構，包括：一第二閘極介電層，位於基底上；一第二功函數金屬層，位於第二閘極介電層上；以及一第二矽化物，位於第二功函數金屬層上。其中，第一矽化物不同於第二矽化物。

三、英文發明摘要：

A semiconductor device is provided. The device includes a first MOS structure and a second MOS structure. The first MOS structure includes a first gate dielectric overlying a substrate, a first work function metallic layer overlying the first gate dielectric, and a first silicide

overlying the first work function metallic layer. The second MOS structure includes a second gate dielectric overlying the substrate, a second work function metallic layer overlying the second gate dielectric, and a second silicide overlying the second work function metallic layer. The first silicide and the second silicide are different.

四、指定代表圖：

(一)本案指定代表圖為：第(1)圖。

(二)本代表圖之元件符號簡單說明：

- | | |
|---------------------|-------------|
| 100~積體電路； | 100a~n型電晶體； |
| 100b~p型電晶體； | 101~基底； |
| 102~p型井區； | 103~n型井區； |
| 104~隔離結構； | |
| 105a、105b~鍺化矽結構； | |
| 106a、106b~n型源極/汲極區； | |
| 107a、107b~p型源極/汲極區； | |
| 108~介電層； | |
| 109a、109b~間隙壁； | |
| 110a、110b~閘極介電結構； | |
| 120~p型功函數金屬層； | |
| 130a、130b~n型功函數金屬層； | |
| 140a、140b~矽化物結構； | |
| a、b~底部厚度。 | |

五、本案若有化學式時，請揭示最能顯示發明特徵的化學式：

七、申請專利範圍：

1.一種半導體裝置，包括：

一第一金氧半結構，包括：

一第一閘極介電層，位於一基底上；

一第一功函數金屬層，位於該第一閘極介電層上；

以及

一第一矽化物，位於該第一功函數金屬層上；以及

一第二金氧半結構，包括：

一第二閘極介電層，位於該基底上；

一第二功函數金屬層，位於該第二閘極介電層上；

以及

一第二矽化物，位於該第二功函數金屬層上；

其中該第一矽化物不同於該第二矽化物。

2.如申請專利範圍第 1 項所述之半導體裝置，其中該第一及該第二矽化物分別與該第一及該第二閘極介電層隔開，且不影響該第一及該第二金氧半結構的功函數值。

3.如申請專利範圍第 1 項所述之半導體裝置，其中該第一矽化物具有金屬對矽的一第一組成比，而該第二矽化物具有金屬對矽的一第二組成比，其中該第一組成比大於該第二組成比。

4.如申請專利範圍第 1 項所述之半導體裝置，其中該第一矽化物擇自於由 Ni_2Si 、 Co_2Si 、 NiSi 、 CoSi 、 Ti_5Si_3 、 TiSi 及其組合所組成的群族之一，且該第二矽化物擇自於由 NiSi_2 、 NiSi 、 CoSi_2 、 CoSi 、 TiSi 、 TiSi_2 及其組合所組成的群族之一。

5.如申請專利範圍第1項所述之半導體裝置，其中該第一矽化物具有一壓縮應力，而該第二矽化物具有一拉伸應力或中性應力。

6.如申請專利範圍第1項所述之半導體裝置，更包括一介電材料圍繞該第一及該第二矽化物，其中該介電材料的上表面切齊於或高於該第一及該第二矽化物的上表面。

7.一種互補式金氧半裝置，包括：

一 n 型金氧半結構，包括：

一第一閘極介電結構，設置於一基底上；

一第一功函數金屬層，設置於該第一閘極介電結構上，該第一功函數金屬層用以調整該 n 型金氧半結構的一第一閘極電極的一第一功函數值；以及

一第一矽化物結構，設置於該第一功函數金屬層上，該第一矽化物結構與該第一閘極介電結構隔開，且沒有調整該 n 型金氧半結構的該第一閘極電極的該第一功函數值；以及

一 p 型金氧半結構，包括：

一第二閘極介電結構，設置於該基底上；

一第二功函數金屬層，設置於該第二閘極介電結構上，該第二功函數金屬層用以調整該 p 型金氧半結構的一第二閘極電極的一第二功函數值；以及

一第二矽化物結構，設置於該第二功函數金屬層上，該第二矽化物結構與該第二閘極介電結構隔開，且沒有調整該 p 型金氧半結構的該第二閘極電極的該第二

功函數值，其中該第一矽化物結構不同於該二矽化物結構。

8.如申請專利範圍第 7 項所述之互補式金氧半裝置，其中該第一矽化物結構擇自於由 Ni_2Si 、 Co_2Si 、 NiSi 、 CoSi 、 Ti_5Si_3 、 TiSi 及其組合所組成的群族之一，且該第二矽化物擇自於由 NiSi_2 、 NiSi 、 CoSi_2 、 CoSi 、 TiSi 、 TiSi_2 、及其組合所組成的群族之一。

9.如申請專利範圍第 7 項所述之積體電路結構，更包括一介電材料圍繞該第一及該第二矽化物結構，其中該介電材料的上表面切齊或高於該第一及該第二矽化物結構的上表面。

10.一種積體電路，包括：

一 n 型電晶體，包括：

一第一開極介電結構，設置於一基底上；

一第一 n 型功函數金屬層，設置於該第一開極介電結構上，該第一 n 型功函數金屬層用以調整該 n 型電晶體的一開極電極的一功函數值；以及

一第一矽化物結構，設置於該第一 n 型功函數金屬層上，該第一矽化物結構具有金屬對矽的一第一組成比；以及

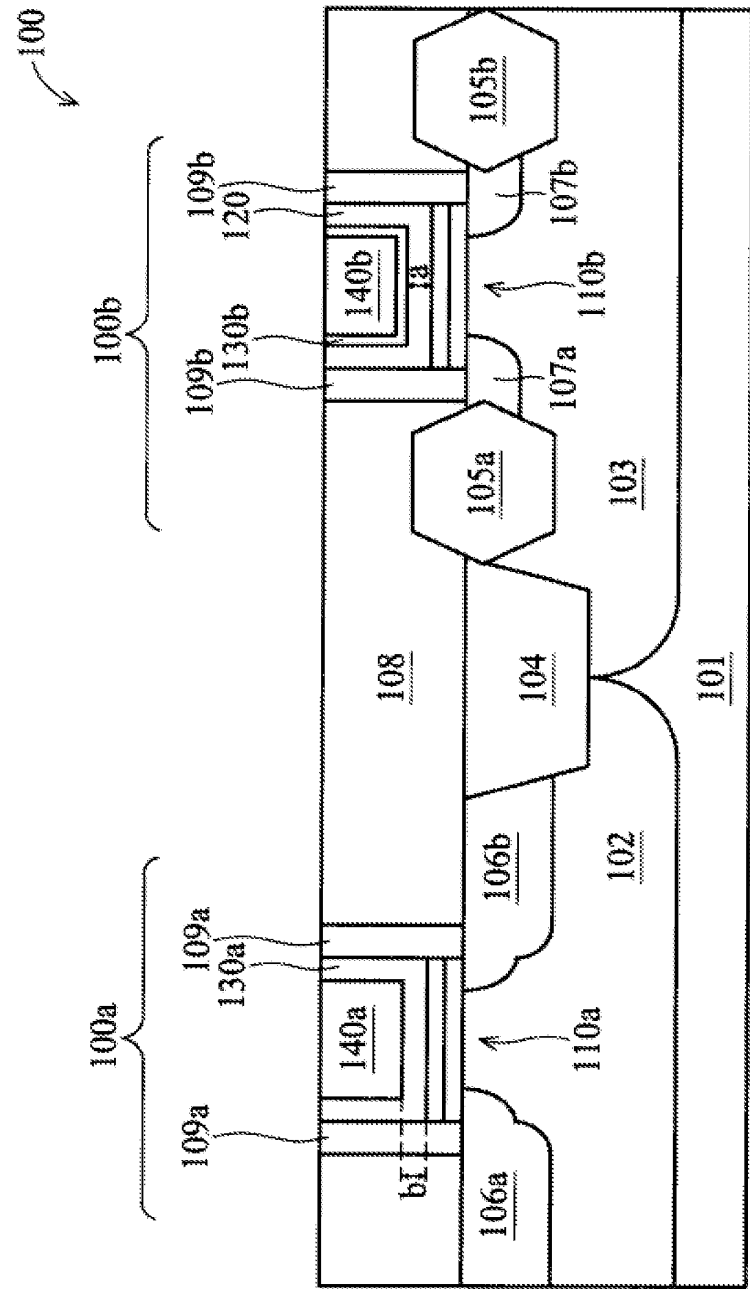
一 p 型電晶體，包括：

一第二開極介電結構，設置於該基底上；

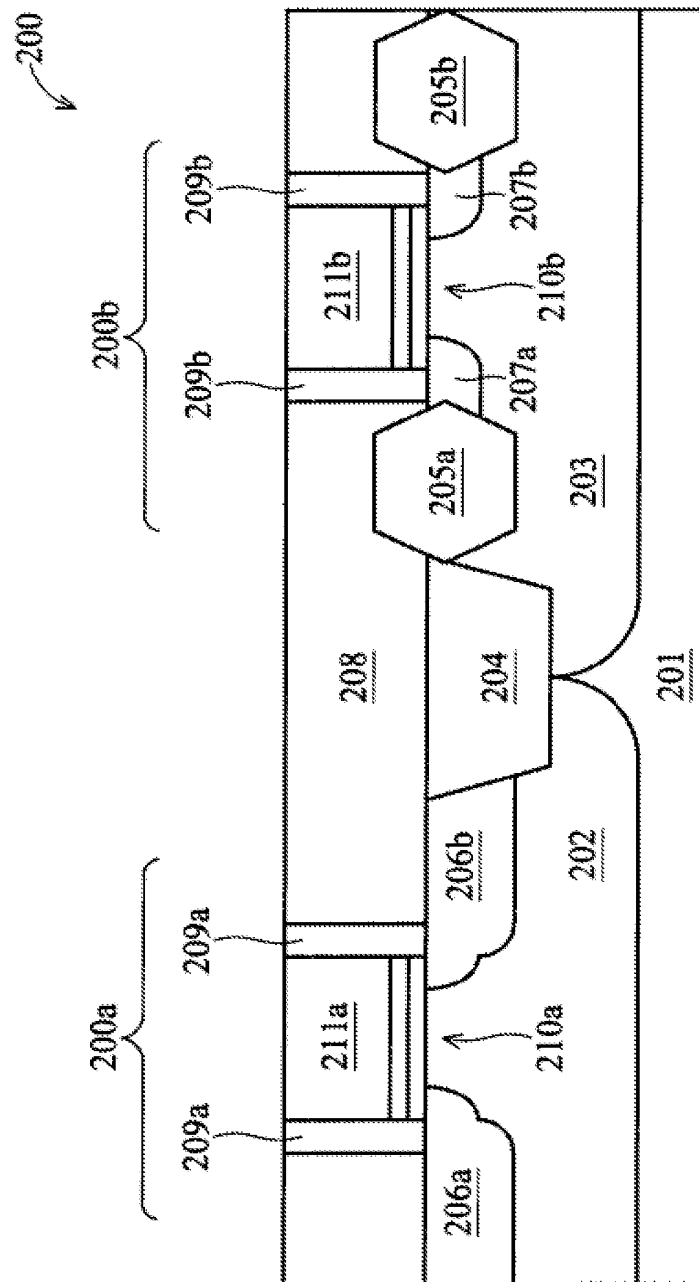
一第二 p 型功函數金屬層，設置於該第二開極介電結構上，該第二 p 型功函數金屬層用以調整該 p 型電晶體的一開極電極的一功函數值；以及

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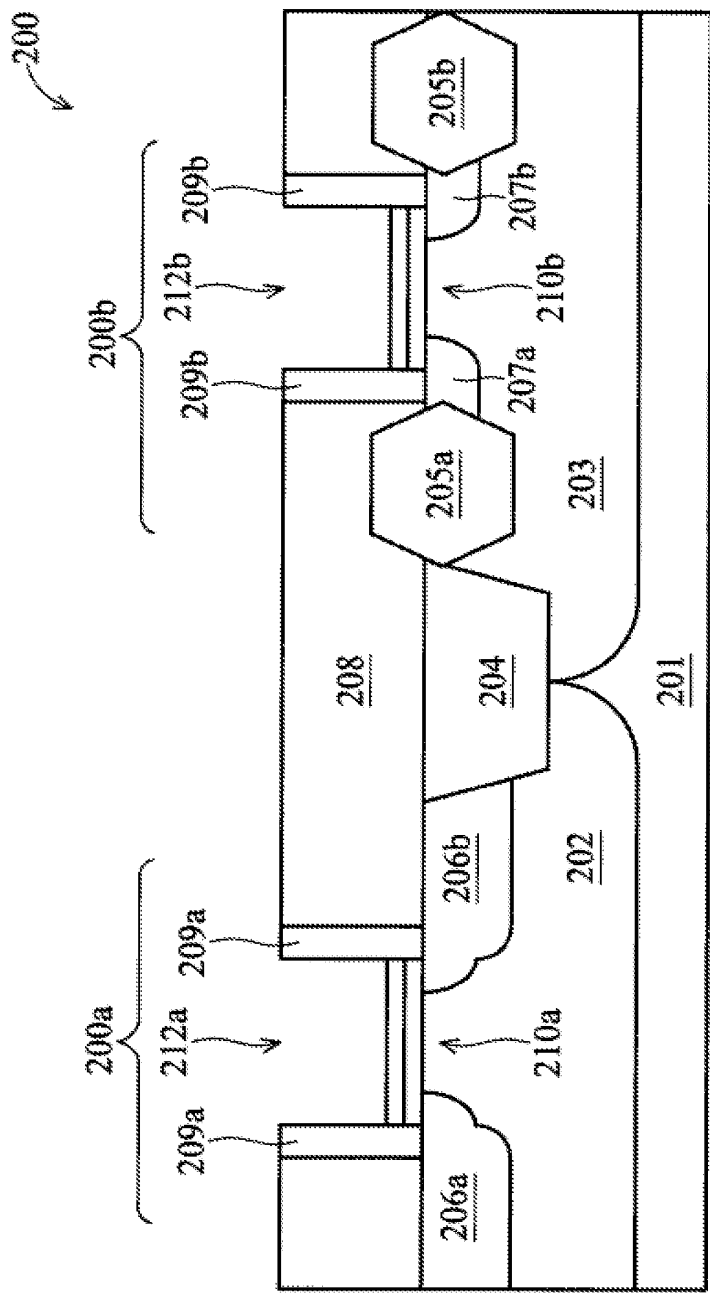
一第二矽化物結構，設置於該第二 p 型功函數金屬層上，該第二矽化物結構具有金屬對矽的一第二組成比，其中該第一組成比大於該第二組成比。



第 1 圖



第2A圖



第2B圖

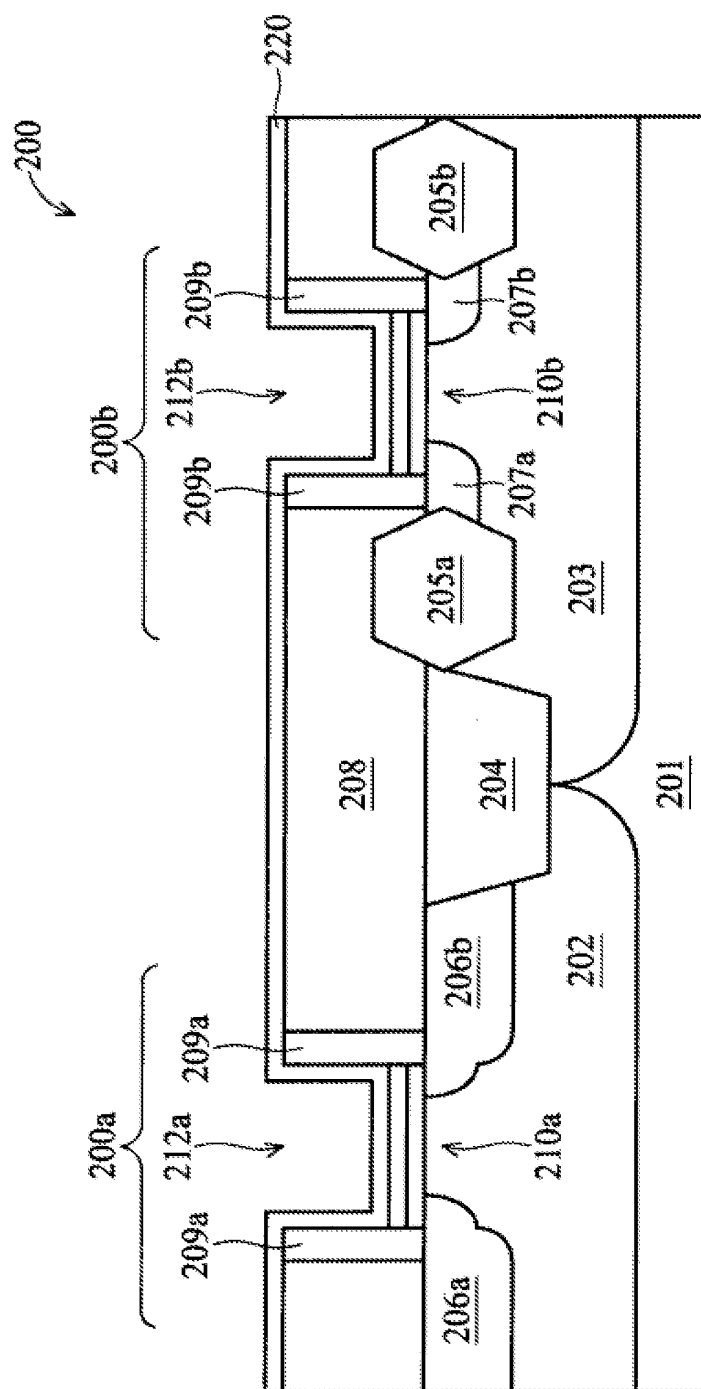
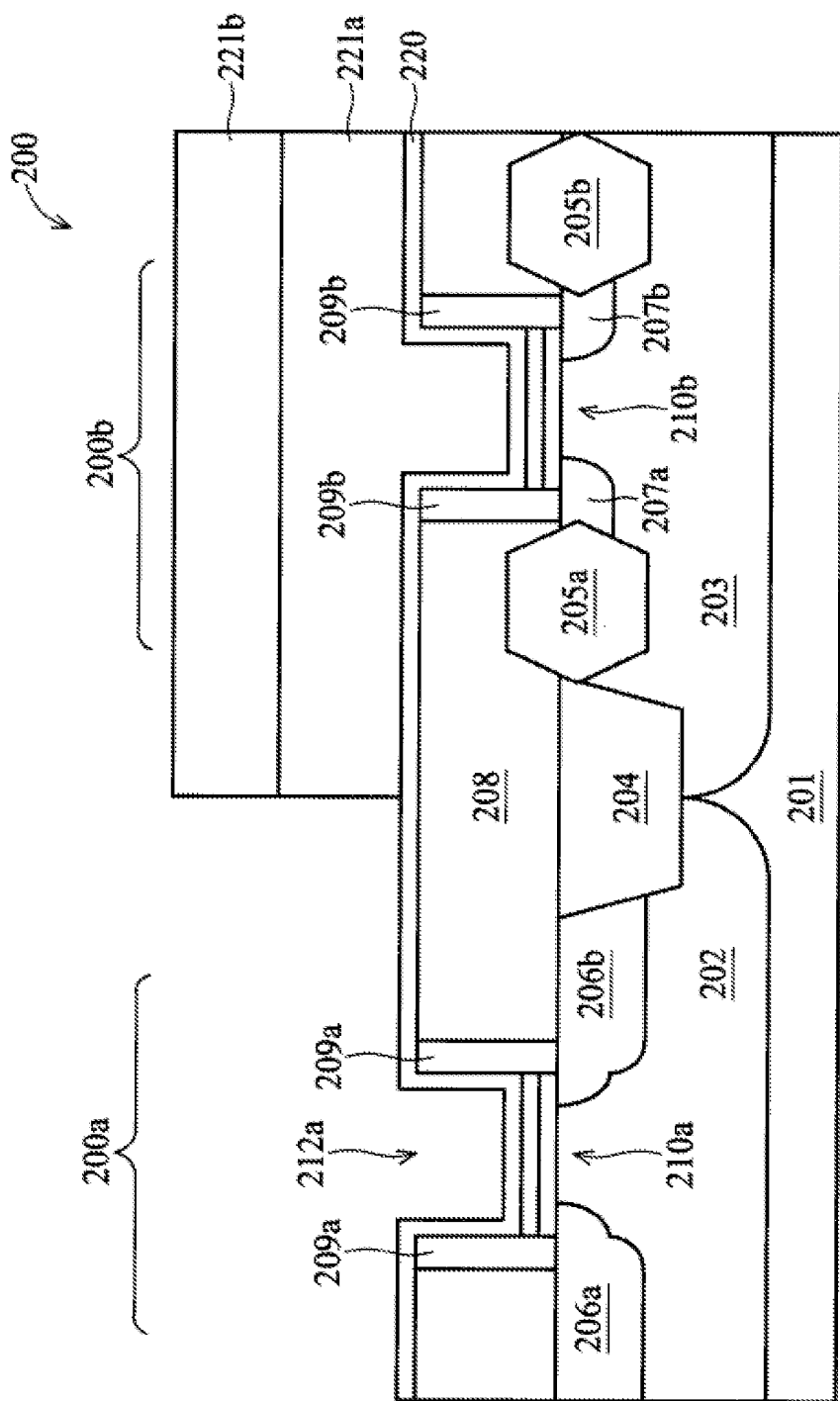


圖 20



第2D圖

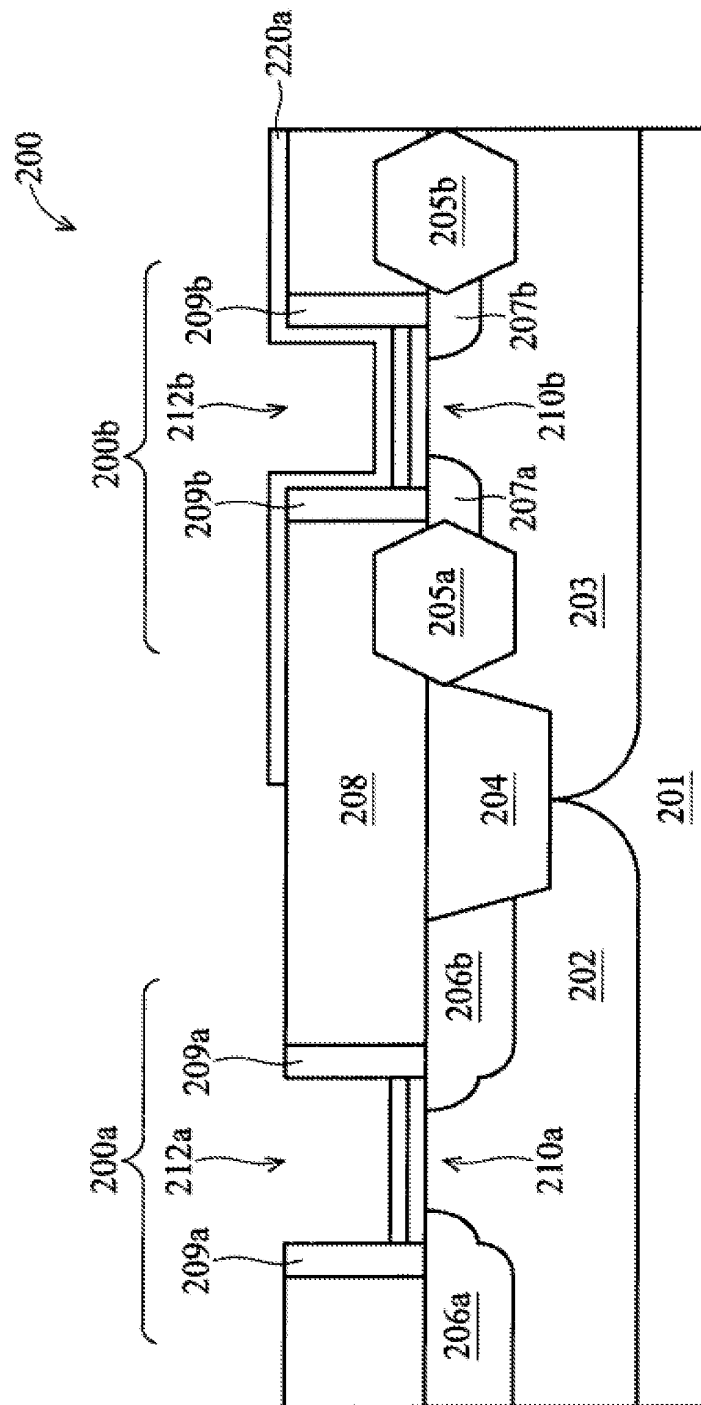
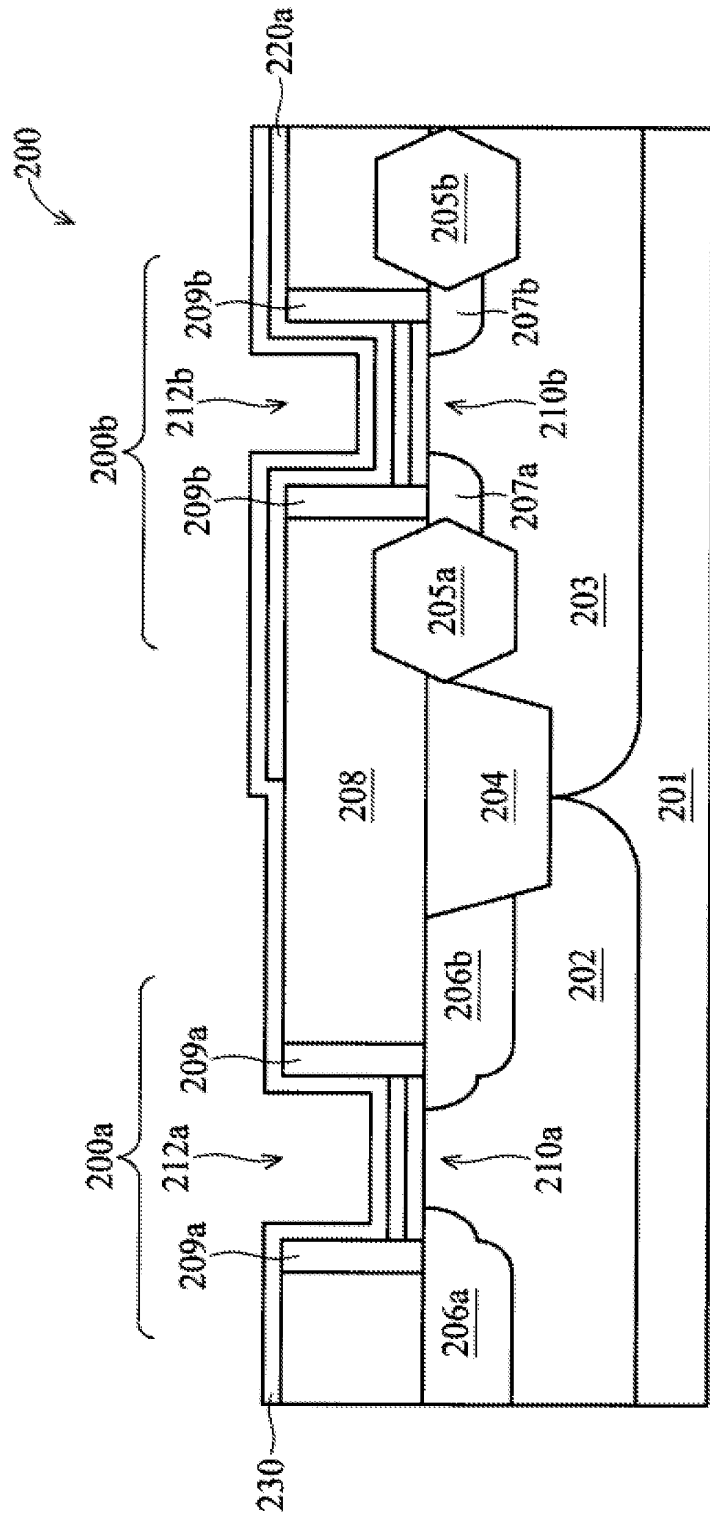


圖
第2E



第2F圖

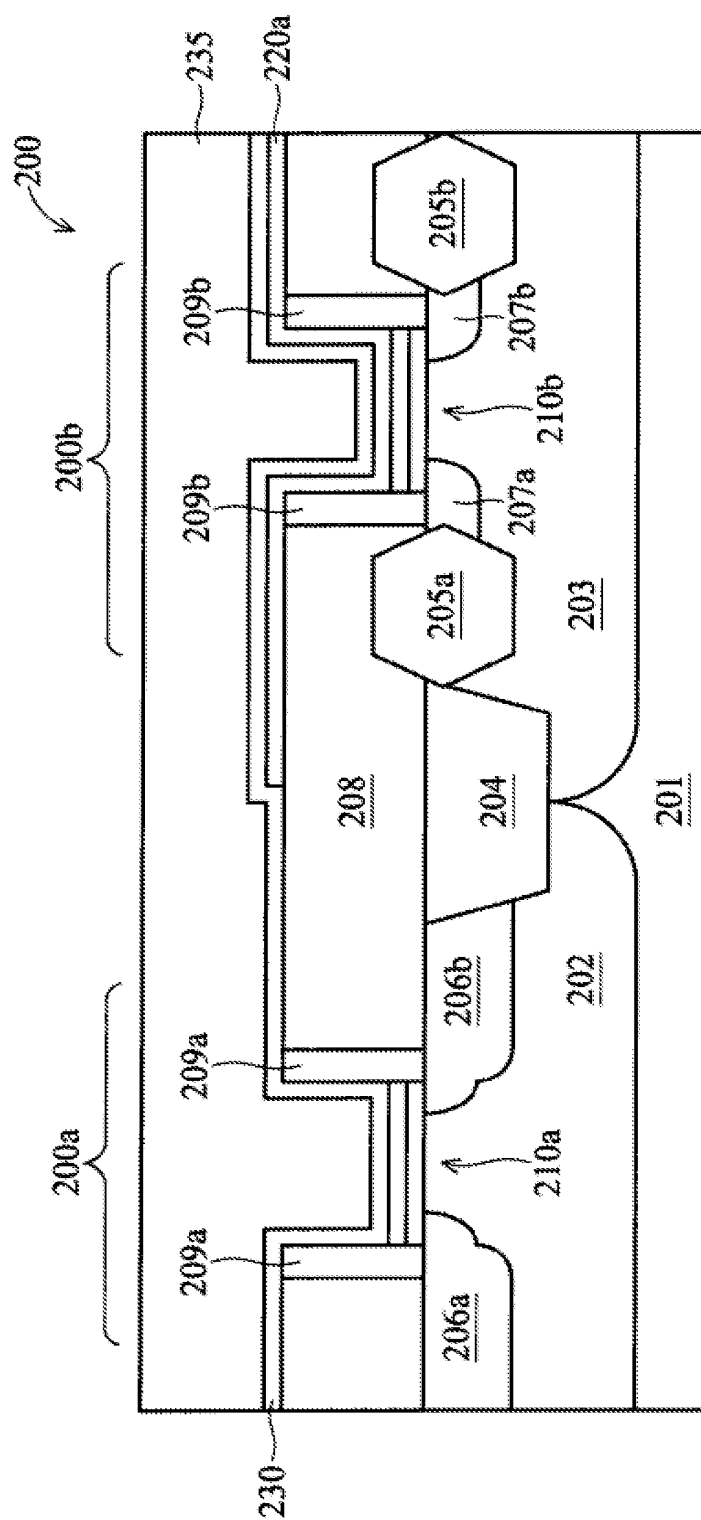
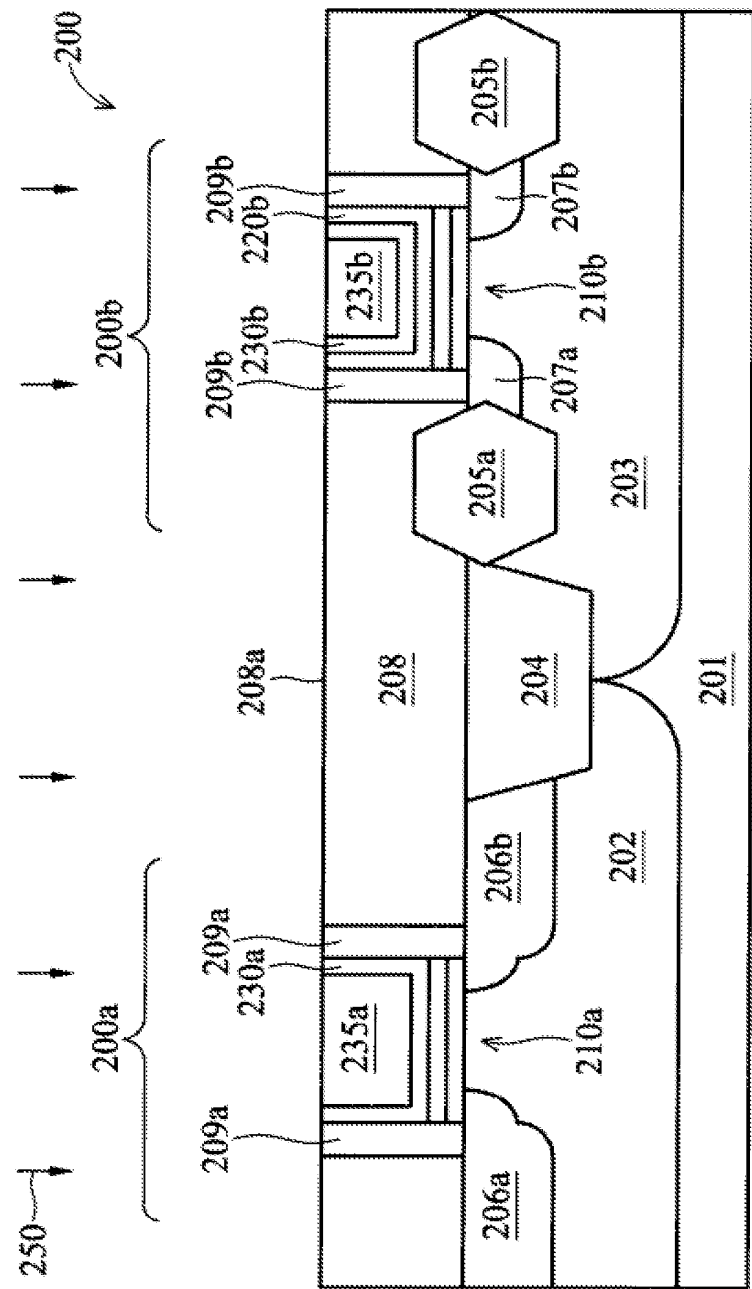
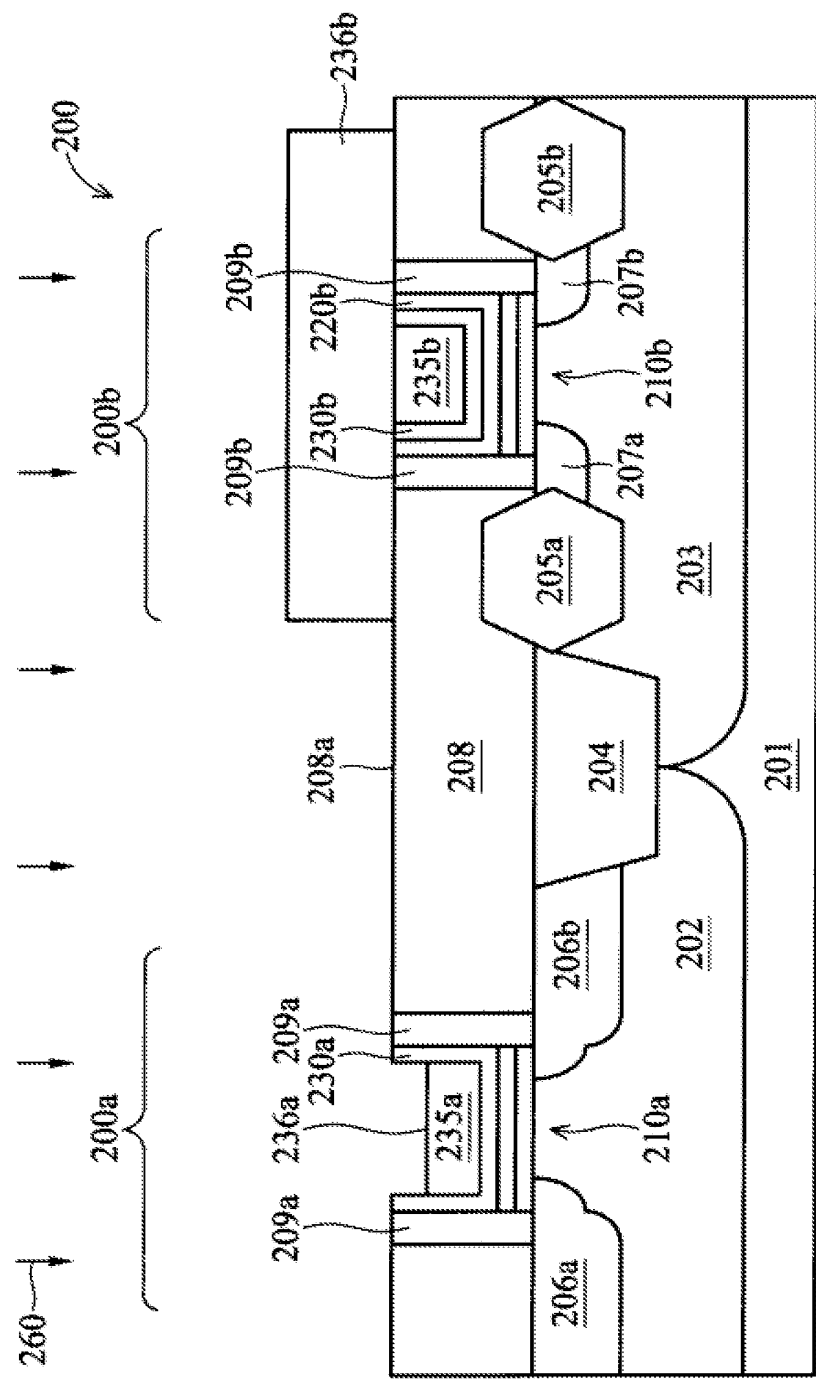


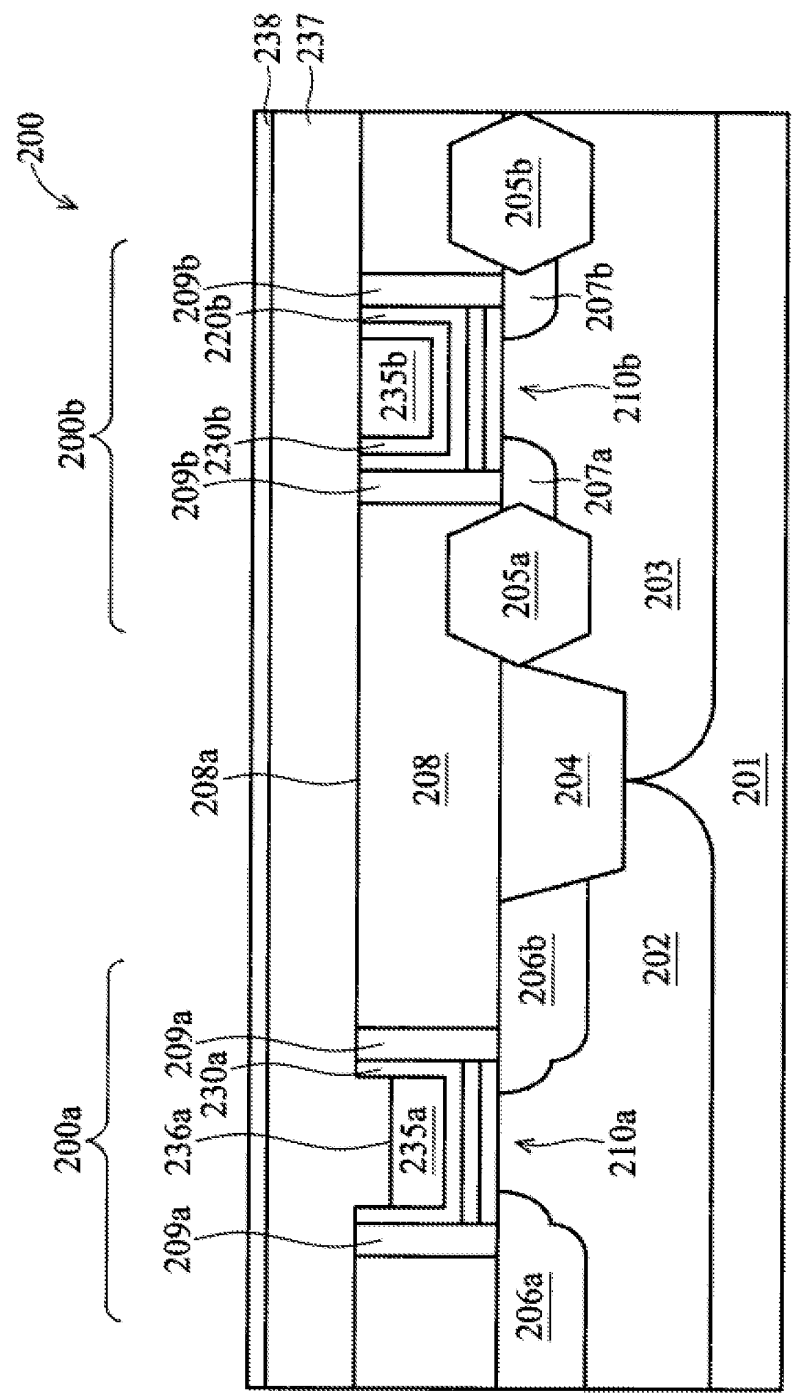
圖 2G



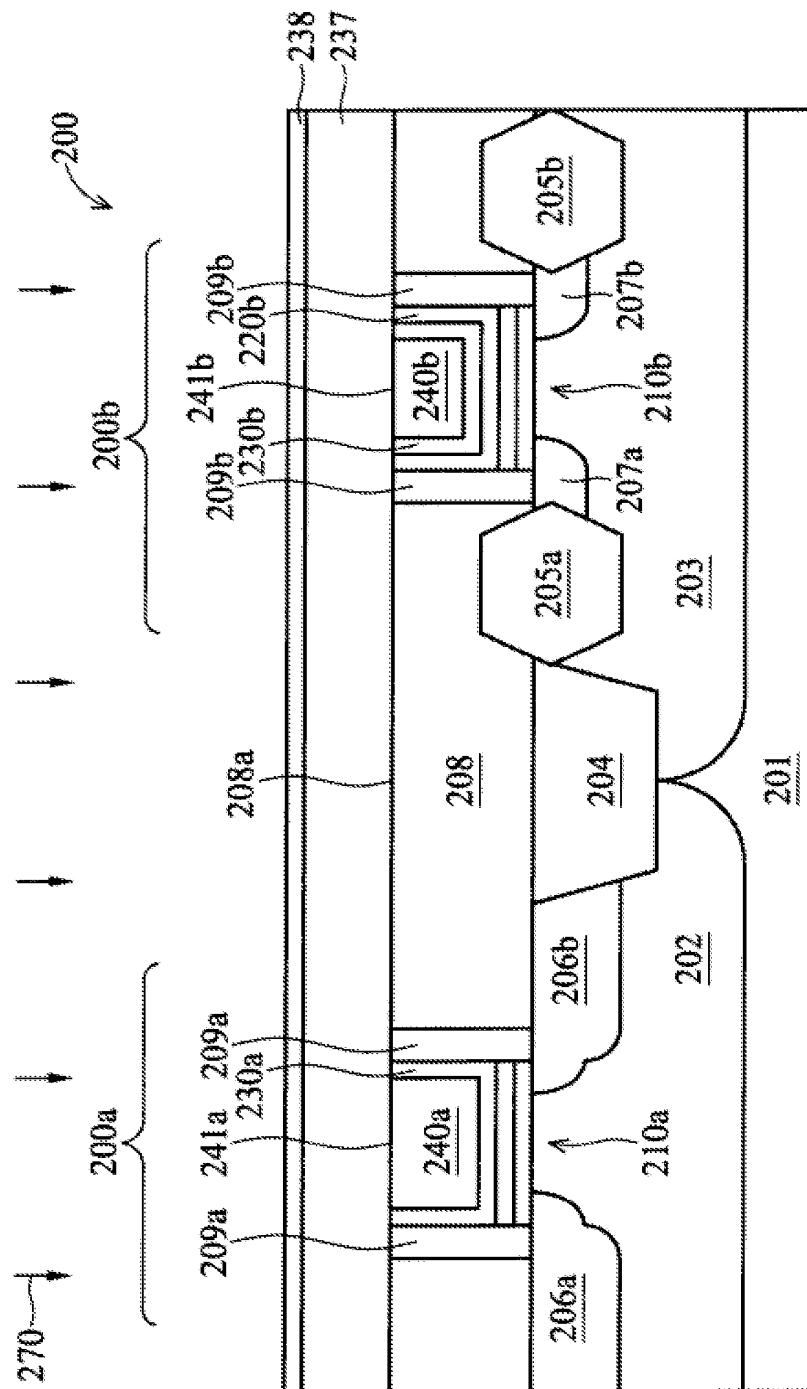
第2H圖



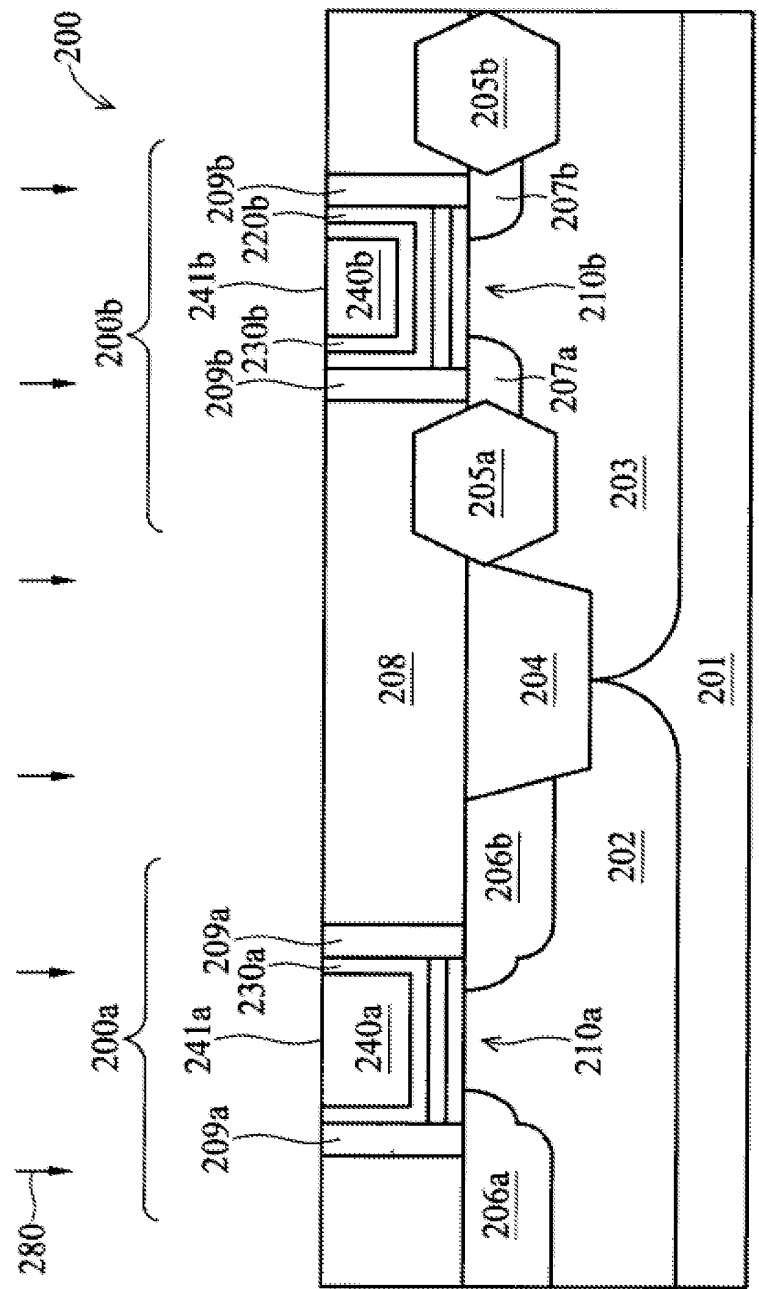
第 2I 圖



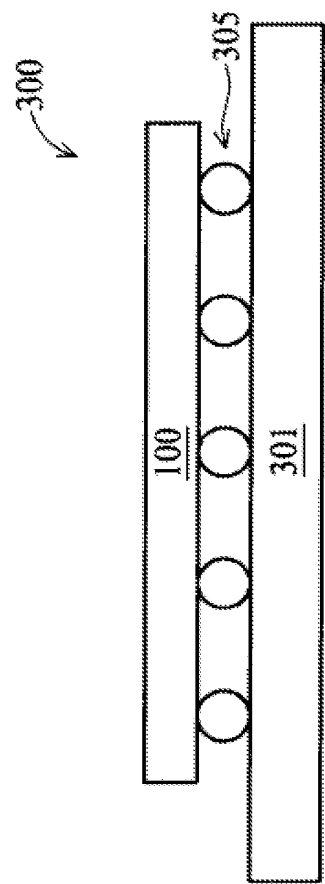
第 2J 圖



第2K圖



第2L圖



第 3 圖

overlying the first work function metallic layer. The second MOS structure includes a second gate dielectric overlying the substrate, a second work function metallic layer overlying the second gate dielectric, and a second silicide overlying the second work function metallic layer. The first silicide and the second silicide are different.

四、指定代表圖：

(一)本案指定代表圖為：第(1)圖。

(二)本代表圖之元件符號簡單說明：

- | | |
|---------------------|-------------|
| 100~積體電路； | 100a~n型電晶體； |
| 100b~p型電晶體； | 101~基底； |
| 102~p型井區； | 103~n型井區； |
| 104~隔離結構； | |
| 105a、105b~鍺化矽結構； | |
| 106a、106b~n型源極/汲極區； | |
| 107a、107b~p型源極/汲極區； | |
| 108~介電層； | |
| 109a、109b~間隙壁； | |
| 110a、110b~閘極介電結構； | |
| 120~p型功函數金屬層； | |
| 130a、130b~n型功函數金屬層； | |
| 140a、140b~矽化物結構； | |
| a、b~底部厚度。 | |

五、本案若有化學式時，請揭示最能顯示發明特徵的化學式：



Espacenet

Bibliographic data: TW201123448 (A) — 2011-07-01

Gate electrode for field effect transistor and field effect transistor

Inventor(s): LIM PENG-SOON [MY]; LEE DA-YUAN [TW]; HSU KUANG-YUAN [TW] ± (LIM, PENG-SOON, ; LEE, DA-YUAN, ; HSU, KUANG-YUAN, ; LEE, DA YUAN, ; HSU, KUANG YUAN)

Applicant(s): TAIWAN SEMICONDUCTOR MFG [TW] ± (TAIWAN SEMICONDUCTOR MANUFACTURING CO., LTD)

Classification: - international: H01L29/40; H01L29/78
 - cooperative: H01L29/4966; H01L29/4983; H01L29/512; H01L29/66545; H01L21/823842; H01L29/495; H01L29/513; H01L29/517

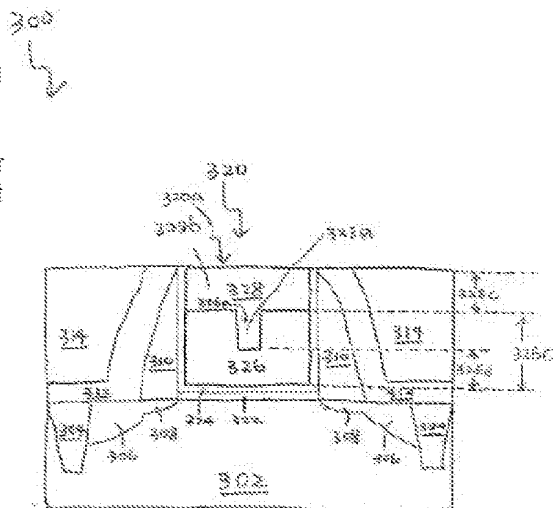
Application number: TW20100114020 20100503

Priority number (s): US20090643414 20091221

Also published as: TWI437708 (B) US2011147858 (A1) US8779530 (B2) US2014295659 (A1) KR20110073214 (A) more

Abstract of TW201123448 (A)

The invention relates to integrated circuit fabrication, and more particularly to a field effect transistor with a low resistance metal gate electrode. In one embodiment, a gate electrode for a field effect transistor comprises a lower portion formed of a first metal material having a recess and a first resistance; and an upper portion formed of a second metal material having a protrusion and a second resistance, wherein the protrusion extends into the recess, and the second resistance is lower than the first resistance.





(19)中華民國智慧財產局

(12)發明說明書公開本

(11)公開編號：TW 201123448 A1

(43)公開日：中華民國 100 (2011) 年 07 月 01 日

(21)申請案號：099114020

(22)申請日：中華民國 99 (2010) 年 05 月 03 日

(51)Int. Cl.:

H01L29/78 (2006.01)

H01L29/40 (2006.01)

(30)優先權：2009/12/21

美國

12/643,414

(71)申請人：台灣積體電路製造股份有限公司 (中華民國) TAIWAN SEMICONDUCTOR
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新竹市新竹科學工業園區力行六路 8 號

(72)發明人：林秉順 LIM, PENG-SOON (MY)；李達元 LEE, DA YUAN (TW)；許光源 HSU,
KUANG YUAN (TW)

(74)代理人：洪澄文；顏錦順

申請實體審查：有 申請專利範圍項數：20 項 圖式數：3 共 34 頁

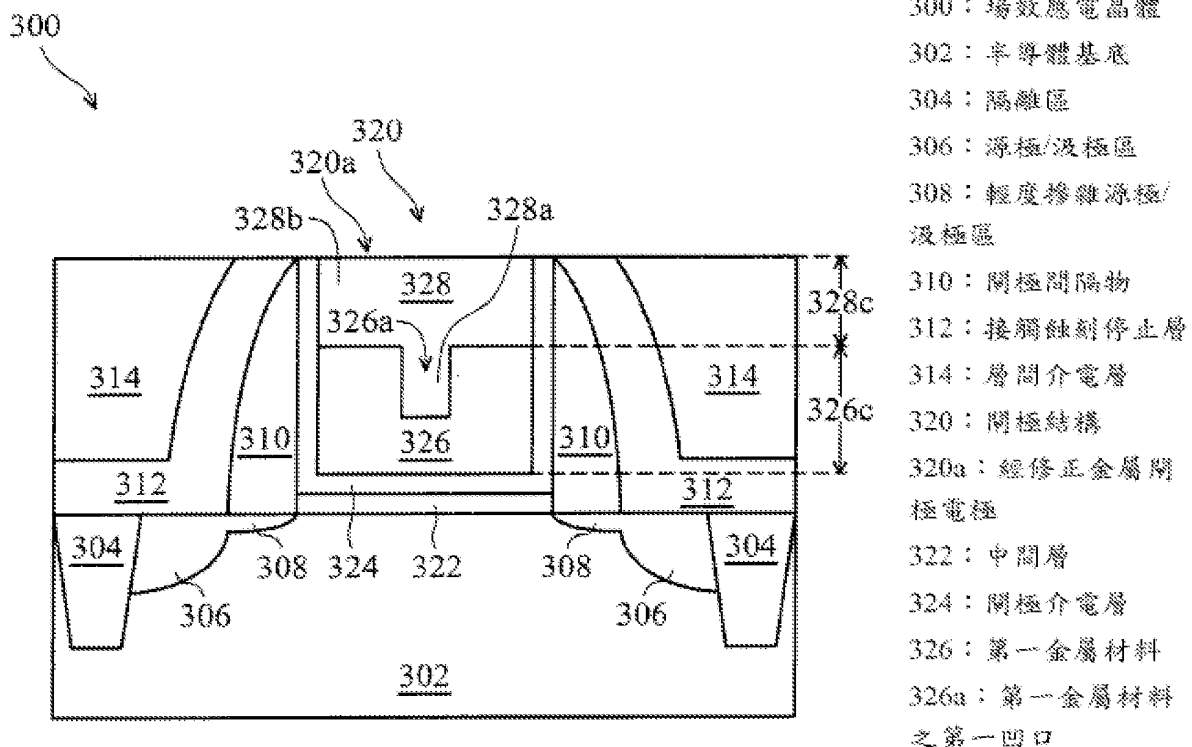
(54)名稱

用於場效應電晶體之閘極電極以及場效應電晶體

GATE ELECTRODE FOR FIELD EFFECT TRANSISTOR AND FIELD EFFECT TRANSISTOR

(57)摘要

本發明係關於積體電路製作，且特別是關於具有低電阻值金屬閘極電極之場效應電晶體。於一實施例中，一種用於場效應電晶體之閘極電極，包括：由第一金屬材料形成之一下方部，具有一凹口及一第一電阻值；以及由第二金屬材料形成之一上方部，具有一突出部以及一第二電阻值，其中該突出部延伸進入該凹口內，且該第二電阻值低於該第一電阻值。



326c：下方部之最大
高度

328：第二金屬材料

328a：第二金屬材料
之突出部

328b：金屬帶狀物

328c：上方部之最小
高度



(19)中華民國智慧財產局

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(11)公開編號：TW 201123448 A1

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(71)申請人：台灣積體電路製造股份有限公司 (中華民國) TAIWAN SEMICONDUCTOR
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(72)發明人：林秉順 LIM, PENG-SOON (MY)；李達元 LEE, DA YUAN (TW)；許光源 HSU,
KUANG YUAN (TW)

(74)代理人：洪澄文；顏錦順

申請實體審查：有 申請專利範圍項數：20 項 圖式數：3 共 34 頁

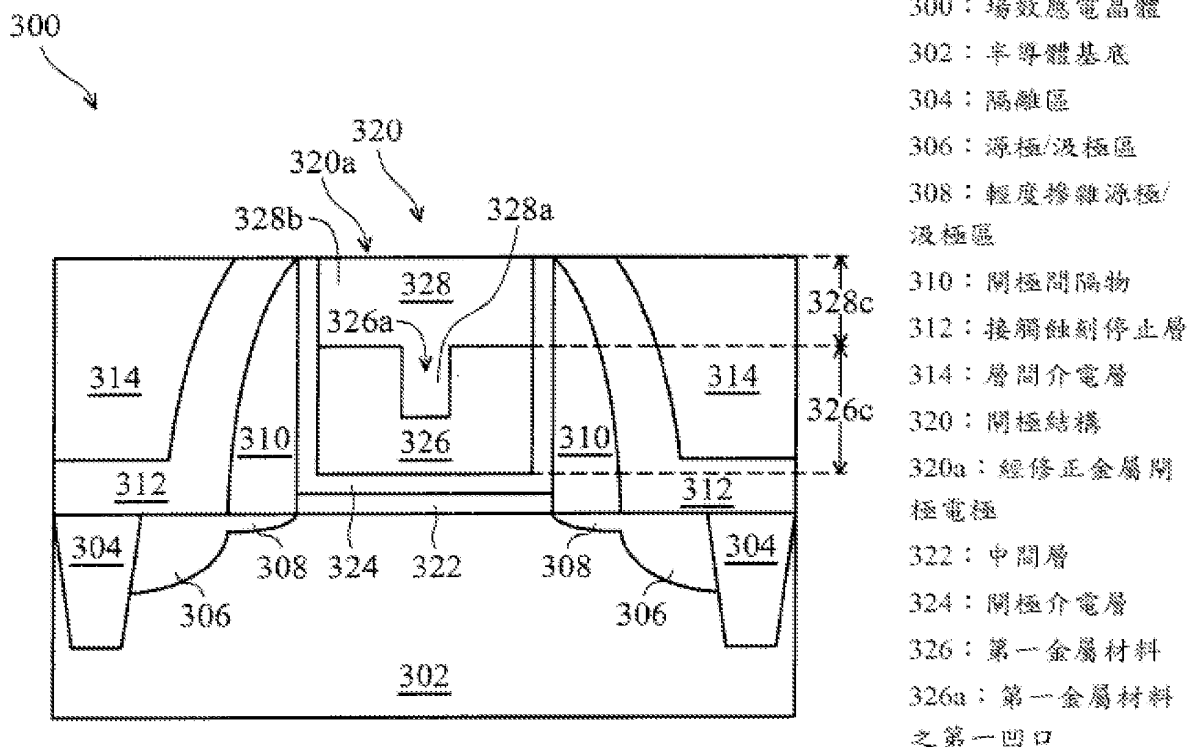
(54)名稱

用於場效應電晶體之閘極電極以及場效應電晶體

GATE ELECTRODE FOR FIELD EFFECT TRANSISTOR AND FIELD EFFECT TRANSISTOR

(57)摘要

本發明係關於積體電路製作，且特別是關於具有低電阻值金屬閘極電極之場效應電晶體。於一實施例中，一種用於場效應電晶體之閘極電極，包括：由第一金屬材料形成之一下方部，具有一凹口及一第一電阻值；以及由第二金屬材料形成之一上方部，具有一突出部以及一第二電阻值，其中該突出部延伸進入該凹口內，且該第二電阻值低於該第一電阻值。



六、發明說明：

【發明所屬之技術領域】

本發明係關於積體電路製作，且特別是關於具有金屬閘極電極(metal gate electrode)之一種場效應電晶體(field effect transistor, FET)。

【先前技術】

隨著電晶體尺寸的縮減，便需要降低閘極氧化物(gate oxide)厚度以維持具有經縮減閘極長度(gate length)之表現。然而，為了降低閘極漏電流(gate leakage)，因而採用了高介電常數(high-k)閘極介電膜層，於維持較大技術節點中所採用之習知閘極氧化物所具有之相同等效厚度時其可具有較高之物理厚度。

此外，隨著技術節點縮減，於部份積體電路設計中，便需要採用金屬閘極電極以取代習知多晶矽閘極電極，藉以改善具有縮減特徵尺寸之元件的表現。形成金屬閘極的製程之一係為”後閘極(gate last)”製程，其內金屬閘極係最後製備形成，因而允許了閘極電極免於受到某些高溫製程的影響，例如是受到源極/汲極回火程序的影響。

第 1 圖為一剖面圖，顯示了採用”後閘極”製程所製造得到之用於場效應電晶體 100 之一習知閘極結構(gate structure)120。在此，場效應電晶體 100 係形成於基底 102 內且鄰近於數個隔離區 104 之一主動區 103 之上。場效應電晶體 100 包括形成於基底 102 之主動區 103 內的數個源極/汲極區 106 與輕度摻雜區 108、包括依序形成於

基底 120 上之一中間層 122、一閘極介電層 124 與多膜層金屬閘極電極 120a 之一閘極結構 120、以及分別形成於閘極結構 120 之兩側側壁上之閘極間隔物 110。此外，於基底 102 之上亦可形成有一接觸蝕刻停止層 112 與一層間介電層 114。

此多膜層金屬閘極 120a 包括了依序形成於閘極介電層 124 上方之一下方部(lower portion)126 以及一上方部(upper portion)128。下方部 126 係由作為功函數金屬層(work-function metal layer)且具有第一電阻值之一第一金屬材料所構成。上方部 128 則由作為一內連金屬層(interconnection metal layer)且具有低於上述第一電阻值之一第二電阻值之一第二金屬材料所構成。由於具有較低電阻值之上方部 128 僅佔據了此多膜層金屬閘極 120a 區域之一小部份，可以觀察到的是此多膜層金屬閘極 120a 將表現出較高之閘極電阻值，如此將增加了電路之阻容延遲(RC delay)且劣化了裝置表現。

如此，便需要用於閘極結構之具有較低閘極電阻值之金屬閘極電極(metal gate electrode)。

【發明內容】

於一實施例中，本發明提供了一種用於場效應電晶體之閘極電極，包括：

由第一金屬材料形成之一下方部，具有一凹口及一第一電阻值；以及由第二金屬材料形成之一上方部，具有一突出部以及一第二電阻值，其中該突出部延伸進入

該凹口內，且該第二電阻值低於該第一電阻值。

於另一實施例中，本發明提供了一種場效應電晶體，包括：

一基底，包括一主動區；一閘極結構，設置於該基底之上，其中該閘極結構包括一閘極介電層與一閘極電極，其中該閘極電極包括由一第一金屬材料所構成且具有一凹口與第一電阻值之一下方部，以及由一第二金屬材料所構成且具有一突出部與一第二電阻值之一上方部，其中該突出部延伸進入該凹口且該第二電阻值係低於該第一電阻值；以及複數個源極/汲極區，位於該閘極結構之相對側之該主動區內。

為讓本發明之上述目的、特徵及優點能更明顯易懂，下文特舉一較佳實施例，並配合所附第圖式，作詳細說明如下：

【實施方式】

可以理解的是於下文中提供了用於解說本發明之不同特徵之數個不同實施例或範例。為了簡化本發明之描述，於下文中描述了構件與設置方式之特定範例。而此些範例僅作為範例之用而非用以限定本發明。舉例來說，於關於第一構件於一第二構件之上或上方的形成情形可能為第一構件與第二構件間之直接接觸，且亦可能包括於第一構件與第二構件之間形成有額外構件之情形，進而使得第一構件與第二構件之間可能不會產生直接接觸情形。基於簡單清楚之目的，不同構件可能採用

不同比例而任意地繪示表現。此外，本發明提供了“後開極(gate last)”之金屬開極製程之範例，然而熟悉此技藝者可將之應用於其他製程及或採用其他材料。

請參照第 2 圖至第 3H 圖並配合下文以解說一方法 200 以及一場效應電晶體 300。第 2 圖為一流程圖，顯示了依據本發明一實施例之製造開極結構 320 之方法 200。第 3A-3H 圖則為一系列示意圖，顯示了依據如第 2 圖所示之製造方法之一實施例中間極結構 320 於不同階段中之情形。可以理解的是，部分之場效應電晶體 300 係由互補型金氧半導體(CMOS)製造技術製成。如此，可以理解的是，於第 2 圖所示之方法 200 實施之前、之中與之後可更施行額外製程，且僅於此簡單描述了部分其他製程。此外，為了較易瞭解本發明之發明概念，第 2 圖至第 3H 圖亦經過簡化。舉例來說，雖然以下圖式僅繪示了用於場效應電晶體 300 之開極結構 320，可以理解到積體電路可包括如電阻、電容、電感或熔絲等許多其他裝置。

請參照第 2 圖與第 3A 圖，方法 200 啟始於步驟 202，首先提供包括開極結構 320 之一溝槽 325 之一半導體基底 302。半導體基底 302 可包括一矽基底。半導體基底 302 亦可包括矽鍺、砷化鎵或其他適當半導體材料。半導體基底 302 可更包括其他構件，例如多個摻雜區、埋入膜層及/或一磊晶層。再者，半導體基底 302 可為一絕緣層上覆半導體層之基底，例如絕緣層上覆矽(SOI)基底。於其他實施例中，半導體基底 302 可包括一經摻雜磊晶層、一梯度半導體層及/或更包括覆蓋具有不同性質之其

他半導體層之一半導體層，例如是位於一矽鍺層上之一矽層。於其他範例中，可採用包括一多重膜層矽結構之一化合物半導體基底或可能具有多重膜層半導體結構之一矽基底。

半導體基底 302 可包括一主動區 303 以及數個隔離區 304。依照習知技術之設計需求，主動區 303 可包括多個摻雜形態。於部份實施例中，主動區 303 可摻雜有 P 型或 N 型摻質。舉例來說，主動區 303 可能摻雜有 P 型摻質，例如 B 或 BF_2 ，或者是摻雜有 N 型摻質，例如磷或砷，及/或其組合。主動區 303 可用於 N 型金氧半導體電晶體(通稱為 NMOS)或用於 P 型金氧半導體電晶體(通稱為 PMOS)。

此些隔離區 304 可形成半導體基底 302 之上，以隔離多個主動區 303。此些隔離區 304 可利用如局部矽氧化物(LOCOS)或淺溝槽隔離(STI)之隔離技術而形成，以定義並電性絕緣多個主動區 303。於本實施例中，隔離區 304 包括一淺溝槽隔離物。此些隔離區 304 可包括氧化矽、氮化矽、氮氧化矽、氟摻雜矽玻璃(FSG)、低介電常數介電材料、其他適當材料及/或其組合。此些隔離區 304 以及本實施例中所採用之淺溝槽隔離物可藉由任何適當製程形成。舉例來說，淺溝槽隔離物的製作可包括藉由一習知微影程序圖案化半導體基底 302、蝕刻半導體基底 302 於其內形成一溝槽(例如採用一乾蝕刻、濕蝕刻及或電漿乾蝕刻)、以及於溝槽內填入一介電材料(例如藉由一化學氣相沈積程序)。於部份實施例中，經回填之溝槽可

具有一多層結構，例如為包括熱氧化物襯層且由氮化矽或氧化矽填滿之多層結構。

值得注意的是，場效應電晶體 300 可採用”後閘極 (gate last)”製程及其他 CMOS 技術製程以形成場效應電晶體 300 之多個構件。如此，在此僅簡短地描述其內之多個構件。場效應電晶體之此些多個構件係於閘極結構 320 形成之前採用一”前閘極 (gate first)”製程而先行形成。此些不同構件可包括位於主動區 303 內且位於閘極結構 320 相對側之數個源極/汲極區(以下簡稱為 N 型與 P 型 S/D)306 與輕度摻雜源極/汲極區(以下簡稱為 N 型或 P 型 LDD)308。N 型 S/D 306 以及 LDD 308 等區域內可摻雜有磷或砷，而 P 型 S/D 306 以及 LDD 308 等區域則可摻雜有硼或銦。上述不同構件可更包括位於閘極結構 320 之對稱側之閘間隔物 (gate spacer) 310、接觸蝕刻停止層 (contact etch stop layer, CESL) 312 以及層間介電層 314。閘極間隔物 310 可由氧化矽、氮化矽或其他適當材料形成。接觸蝕刻停止層 312 可由氮化矽、氮氧化矽、或其他適當材料所形成。層間介電層 314 則可包括由高深寬比製程所形成及/或高密度電漿沈積製程所形成之氧化物。

於一”後閘極”製程中，係先行形成如多晶矽材質假閘極之假閘極結構(未顯示)，且可接著採用 CMOS 製程技術直到完成層間介電層 314 的沈積。接著於層間介電層 314 上實施化學機械研磨 (CMP) 以露出此假閘極結構。可接著移除此假閘極結構，進而形成一開口。可以

理解的是上述例子並不用於限定用於形成假閘極結構之製程步驟。可以理解的是，上述假閘極結構可包括額外之介電層及/或導電層。舉例來說，假閘極結構可包括硬罩幕層、中間層、上蓋層、擴散/阻障層，其他適當膜層及/或其組合。

請繼續參照第 3A 圖，接著沈積一閘極介電層 324，部份填入於開口內以形成一溝槽 325。於部份實施例中，閘極介電層 324 可包括氧化矽、氮化矽、高介電常數介電層或其組合。高介電常數介電層可包括氧化鈣(HfO_2)、氧化鈣矽(HfSiO)、氮氧化鈣矽(HfSiON)、氧化鈣鈮(HfTaO)、氧化鈣鈦(HfTiO)、氧化鈣鋅(HfZrO)、金屬氧化物、金屬氮化物、金屬矽化物、過渡金屬氧化物、過渡金屬氮化物、過渡金屬矽化物、金屬之氮氧化物、金屬鋁酸鹽(metal aluminates)、矽酸鋯(zirconium silicate)、鋁酸鋯(zirconium aluminates)、氮化矽、氮氧化矽、氧化鋯(zirconium oxide)、氧化鈦、氧化鋁、二氧化鈣-氧化鋁($\text{HfO}_2\text{-Al}_2\text{O}_3$)合金、其他適當之高介電常數材料及/或其組合。於部份之實施例中，於開口內之高介電常數介電材料具有少於 2nm 之厚度。閘極介電層 324 可更包括一中間層 322，以降低閘極介電層 324 與半導體基底 302 間的毀損情形。中間層 322 可包括氮化矽、氮氧化矽、氮化矽、矽酸鈣(Hf silicate)或氧化鋁基介電材料(Al_2O_3 based dielectric)。

一般來說，溝槽 325 係接著為多個金屬層所填入，且可施行金屬圖案化程序以形成場效應電晶體 100 內之適當金屬膜層。可施行一化學機械研磨(CMP)以移除溝槽

325 外之多個金屬層，並形成場效應電晶體 100 之多膜層金屬閘極電極 120a。或者，亦可施行乾蝕刻或濕蝕刻製程。可以觀察到的是場效應電晶體 100 之多膜層金屬閘極電極 120a 內，由於具有較低電阻值之金屬層 128 僅佔據了多膜層金屬閘極電極 120a 區域之一小部份，因此使得多膜層金屬閘極電極 120a 具有高閘極電阻值。如此將增加積體電路之阻容延遲(RC delay)並劣化裝置表現。如此，於下文中透過第 2 圖與第 3B-3H 圖解說一經修改多膜層金屬閘極電極 120a 以形成一閘極結構 320，藉以降低其閘極電阻值至低於一個次方值。如此可降低積體電路之阻容延遲並提升元件表現。

請參照第 2 圖與第 3B 圖，方法 200 接著進行步驟 204，將具有第一凹口 326a 之第一金屬材料 326 沈積並部份填入溝槽 325 內。第一金屬材料 326 包括擇自由 Ti、Ta、W、TiAl、Co、其合金與其包括 C 及/或 N 之化合物金屬所組成族群之一材料。第一金屬材料 326 可由化學氣相沈積(CVD)、物理氣相沈積(PVD)或其他適當技術所形成。第一金屬材料 326 具有一第一電阻值。第一金屬材料 326 具有介於 30~150 埃之一厚度。第一金屬材料 326 可包括功函數金屬之一堆疊膜層。於一實施例中，用於一 NMOS 之第一金屬材料 326 可包括 Ti、Ta、TiAl、其合金或包括 C 及/或 N 等功函數金屬之化合物。於另一實施例中，用於一 PMOS 之第一金屬材料 326 可包括 Ti、Ta、Co、其合金或包括 C 及/或 N 等功函數金屬。於某些實施例中，上述堆疊膜層可包括一阻障金屬(barrier metal)

層、一襯墊金屬 (liner metal) 層或一增濕金屬 (wetting metal) 層。

請參照第 2 圖與第 3C 圖，方法 200 接著進行步驟 206，沈積一犧牲層 327 於第一金屬材料 326 之上以填滿第一凹口 326a 與溝槽 325。犧牲層 327 可包括多晶矽、光阻或旋轉塗佈介電層，但並限定於上述材料。犧牲層 327 可藉由化學氣相沈積 (CVD)、物理氣相沈積 (PVD)、原子層沈積 (ALD)、旋轉塗佈或其他適當技術所形成。犧牲層 327 之厚度則依照第一凹口 326a 與溝槽 325 之深度而決定。如此，犧牲層 327 係沈積直至大體填滿第一凹口 326a 與溝槽 325。

請參照第 2 圖與第 3D 圖，方法 200 接著進行步驟 208，施行一化學機械研磨 (CMP) 程序以移除溝槽 325 外之犧牲層 327、第一金屬材料 326 與閘極介電層 324 之一部份。如此，當抵達層間介電層 314 處此化學機械研磨程序將停止並因而提供了一大體平坦表面。或者，上述移除情形亦可由一乾蝕刻及/或濕蝕刻程序所達成。

請參照第 2 圖與第 3E 圖，方法 200 接著進行步驟 210，經由一蝕刻製程移除第一金屬材料 326 之一上方部以形成此第一金屬材料 326 之一第二凹口 326b。蝕刻製程可包括一乾蝕刻製程及或一濕蝕刻製程。舉例來說，濕蝕刻化學可包括 SC-1 或 SPM，且可能具有如 H_2O_2 之氧化劑，且於低於 $70^{\circ}C$ 之溫度施行以選擇性移除該第一金屬材料 326 之上方部。舉例來說，乾蝕刻所使用之蝕刻化學品可包括 BCl_3 以選擇性地移除該第一金屬材料

326 之上方部。蝕刻製程形成了位於溝槽 325 之第一金屬材料 326 內之第二凹口 326b。位於溝槽 325 內第一金屬材料 326 之第二凹口 326b 可具有介於約 50~2700 埃之深度。此深度可透過調整蝕刻製程之不同參數而達成，例如是時間與蝕刻化學品。

再者，犧牲層 327 於蝕刻製程中可能不作為保護層之用，除非其移除率不夠大。於一實施例中，蝕刻化學品對於第一金屬材料 326 以及犧牲層 327 之間之移除率比例較佳地高於 10。再者，當閘極介電層 324 經過蝕刻化學品的毀損後，於後續製程中其將成為一缺陷源(defect source)並進而增加了漏電流之可能性。於一實施例中，蝕刻化學品對於第一金屬材料 326 與閘極介電材料 324 之移除率比例較佳地高於 20。於本實施例中，位於溝槽 327 內第一金屬材料 326 之一剩餘部形成了經修正金屬閘極 320a 之一下方部。此下方部大體為 U 形。

請參照第 2 圖與第 3F 圖，方法 200 接著進行步驟 212，經由另一蝕刻製程以移除殘留於溝槽 325 內之犧牲層 327，以露出第一金屬材料 326 之第一凹口 326a。並上述蝕刻製程可包括一乾蝕刻製程及/或一濕蝕刻製程。舉例來說，用於選擇性地移除殘存於溝槽 325 內之犧牲層 327 之乾/濕蝕刻之蝕刻化學品可包括 F、Cl 及 Br 基化學品。當鄰近於第一凹口 326a 之第一金屬材料 326 為蝕刻化學品所侵蝕時，將改變金屬之功函數，並進而增加了裝置失敗之可能性。於一實施例中，蝕刻化學品對於犧牲層 327 及第一金屬材料 326 之移除率比例較佳地高

於 10。

請參照第 2 圖與第 3G 圖，方法 200 接著施行步驟 214，沈積第二金屬材料 328 於第一金屬材料 326 之上，以填入第一金屬材料 326 之第一凹口 326a 與第二凹口 326b 內。第一金屬材料之第一凹口 326a 與第二凹口 326b 於下文中通稱為溝槽 325 之上部。於一實施例中，可於第一金屬材料 326 上選擇性地形成阻障層，藉以於第二金屬材料 328 沈積之前部份填入於溝槽 325 之上部中。阻障層可包括擇自由 Ti、Ta、TiN、TaN 與 WN 所組成族群之一材料。阻障層之厚度約介於 5~50 埃。阻障層可藉由 CVD、PVD、ALD 或其他適當技術所形成。於部份實施例中，由於阻障層亦具有高電阻值，故不使用阻障層。

請繼續參照第 2 圖與第 3G 圖，於第一金屬材料 326 之上沈積第二金屬材料 328 以填滿溝槽 325 之上部。於本實施例中，第二金屬材料 328 可包括擇自由 Al、Cu、Co 與 W 所組成族群之一材料。第二金屬材料 328 可藉由 CVD、PVD、電鍍、旋轉塗佈、原子層沈積或其他適當製程所形成。第二金屬材料 328 具有第二電阻值。第二電阻值係低於第一電阻值。舉例來說，Al 的電阻值(約 $2.65\ \mu\Omega\text{-cm}$)係低於 TiN(約 $200\ \mu\Omega\text{-cm}$)之電阻值。第二金屬材料 328 之厚度可依照溝槽 325 之上部深度而訂。如此，第二金屬材料 328 係沈積直至大體填滿了溝槽 325 之上部。

請參照第 2 圖與第 3H 圖，方法 200 接著進行步驟

216，施行一化學機械研磨(CMP)程序以移除位於溝槽 325 外之第二金屬材料 328。如此，此 CMP 程序於抵達層間介電層 314 處將停止，因而提供大體平坦表面。於 CMP 程序施行之後，位於溝槽 325 內之第二金屬材料 328 之剩餘部份形成了經修正金屬閘極電極 320a 之上部。第二金屬材料 328 可包括延伸進入第一金屬材料 326 之第一凹口 326a 內之一突出部 328a。第二金屬材料 328 更包括延伸進入於第一金屬材料 326 之第二凹口 326b 之一金屬帶狀物 328b，且第二金屬材料 328 此時大體為 T 形。

經修正金屬閘極結構 320a 包括由具有第一凹口 326a 與第一電阻值之第一金屬材料 326 所構成之下方部。此下部大體為 U 形。可以理解的是本發明並非以上述實施例加以限定。下方部可為大體 L 形或其他形狀。此下方部具有介於 300~2900 埃之一最大高度 326c。經修正金屬閘極 320a 更包括由具有突出部 328a 延伸進入凹口 326a 內以及第二電阻值之第二金屬材料 328 所構成之上方部。此上方部可更包括金屬帶狀物 328b 且大體為 T 形。可以理解的是本發明並非為上述實施例而加以限定。上方部可大體為 L 形或其他形狀。上方部具有介於 50~2700 埃之一最小高度 328c。此外，突出部 328a 延伸進入凹口 326a。第二電阻值係低於第一電阻值。與如第 1 圖所示之習知金屬閘極電極 120a 相比較，此時於經修正金屬閘極電極 320a 內具有較低電阻值之上方部 328 具有較大區域比例。如此，經修正金屬閘極電極較習知金屬閘極電極 120a 具有較低之閘極電阻值。如此之較低閘極電阻值

可降低電路之阻容延遲以及提升裝置之表現。

可以理解的是場效應電晶體 300 可更藉由其他 CMOS 製造流程的實施，以形成如接觸物/介層物、內連金屬層、介電層、保護層等多個構件。可以觀察到的是採用經修正金屬閘極電極 320a 作為閘極接觸材料可降低了 NMOS 與 PMOS 之閘極電阻值。

雖然本發明已以較佳實施例揭露如上，然其並非用以限定本發明，任何熟習此項技藝者，在不脫離本發明之精神和範圍內，當可作更動與潤飾，因此本發明之保護範圍當視後附之申請專利範圍所界定者為準。

【圖式簡單說明】

第 1 圖為一剖面圖，顯示了用於場效應電晶體之一習知閘極結構；

第 2 圖為一流程圖，顯示了依據本發明之不同實施例之閘極結構之製造方法；以及

第 3A-3H 圖為一系列剖面圖，顯示了依據如第 2 圖所示方法中之一實施例中之閘極結構於不同製程階段中之情形。

【主要元件符號說明】

100~場效應電晶體；	102~基底；
103~主動區；	104~隔離區；
106~源極/汲極區；	108~輕度摻雜區；
110~閘極間隔物；	112~接觸蝕刻停止層；
114~層間介電層；	120~閘極結構；
120a~多膜層金屬閘極電極 120a；	
122~中間層；	124~閘極介電層；
126~下方部；	128~上方部；
200~方法；	
202、204、206、208、210、212、214、216~步驟；	
300~場效應電晶體；	302~半導體基底；
303~主動區；	304~隔離區；
306~源極/汲極區；	
308~輕度摻雜源極/汲極區；	
310~閘極間隔物；	312~接觸蝕刻停止層；

- 314~層間介電層；
- 320~閘極結構；
- 320a~經修正金屬閘極電極；
- 322~中間層；
- 324~閘極介電層；
- 325~溝槽；
- 326~第一金屬材料；
- 326a~第一金屬材料之第一凹口；
- 326b~第一金屬材料之第二凹口；
- 326c~下方部之最大高度；
- 327~犧牲層；
- 328~第二金屬材料；
- 328a~第二金屬材料之突出部；
- 328b~金屬帶狀物；
- 328c~上方部之最小高度。

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發明專利說明書

(本說明書格式、順序、請勿任意更動，※記號部分請勿填寫)

※申請案號：99104020

※申請日：99.5.3

IPC分類：H01L29/18
H01L29/40

一、發明名稱：(中文/英文)

用於場效應電晶體之閘極電極以及場效應電晶體

GATE ELECTRODE FOR FIELD EFFECT
TRANSISTOR AND FIELD EFFECT TRANSISTOR

二、中文發明摘要：

本發明係關於積體電路製作，且特別是關於具有低電阻值金屬閘極電極之場效應電晶體。於一實施例中，一種用於場效應電晶體之閘極電極，包括：由第一金屬材料形成之一下方部，具有一凹口及一第一電阻值；以及由第二金屬材料形成之一上方部，具有一突出部以及一第二電阻值，其中該突出部延伸進入該凹口內，且該第二電阻值低於該第一電阻值。

三、英文發明摘要：

The invention relates to integrated circuit fabrication, and more particularly to a field effect transistor with a low resistance metal gate electrode. In one embodiment, a gate electrode for a field effect transistor comprises a lower portion formed of a first metal material having a recess and a first resistance; and an upper portion formed

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of a second metal material having a protrusion and a second resistance, wherein the protrusion extends into the recess, and the second resistance is lower than the first resistance.

七、申請專利範圍：

1. 一種用於場效應電晶體之閘極電極，包括：

由第一金屬材料形成之一下方部，具有一凹口及一第一電阻值；以及

由第二金屬材料形成之一上方部，具有一突出部以及一第二電阻值，其中該突出部延伸進入該凹口內，且該第二電阻值低於該第一電阻值。

2. 如申請專利範圍第 1 項所述之用於場效應電晶體之閘極電極，其中該下方部為大體 U 形。

3. 如申請專利範圍第 1 項所述之用於場效應電晶體之閘極電極，其中該下方部具有介於 300~2900 埃之最大高度。

4. 如申請專利範圍第 1 項所述之用於場效應電晶體之閘極電極，其中該第一金屬材料包括擇自由 Ti、Ta、W、TiAl、Co、其合金與其包括 C 及/或 N 之化合物金屬所組成族群之一材料。

5. 如申請專利範圍第 1 項所述之用於場效應電晶體之閘極電極，其中該第一金屬材料為包括功函數金屬之一膜層。

6. 如申請專利範圍第 1 項所述之用於場效應電晶體之閘極電極，其中該上方部為大體 T 形。

7. 如申請專利範圍第 1 項所述之用於場效應電晶體之閘極電極，其中該上方部具有介於 50~2700 埃之一最小高度。

8. 如申請專利範圍第 1 項所述之用於場效應電晶體

之間極電極，其中該第二金屬材料包括擇自由 Al、Cu、Co 與 W 所組成族群之一材料。

9. 如申請專利範圍第 8 項所述之用於場效應電晶體之間極電極，其中該第二金屬材料更包括一阻障層，而該阻障層包括擇自由 Ti、Ta、TiN、TaN 與 WN 所組成族群之一材料。

10. 一種場效應電晶體，包括：

一基底，包括一主動區；

一閘極結構，設置於該基底之上，其中該閘極結構包括一閘極介電層與一閘極電極，其中該閘極電極包括由一第一金屬材料所構成且具有一凹口與第一電阻值之一下方部，以及由一第二金屬材料所構成且具有一突出部與一第二電阻值之一上方部，其中該突出部延伸進入該凹口且該第二電阻值係低於該第一電阻值；以及

複數個源極/汲極區，位於該閘極結構之相對側之該主動區內。

11. 如申請專利範圍第 10 項所述之場效應電晶體，其中該下方部為大體 U 形。

12. 如申請專利範圍第 10 項所述之場效應電晶體，其中該下方部具有介於 300~2900 埃之一最大高度。

13. 如申請專利範圍第 10 項所述之場效應電晶體，其中該第一金屬材料包括擇自由 Ti、Ta、W、TiAl、Co、其合金與其包括 C 及/或 N 之化合物金屬所組成族群之一材料。

14. 如申請專利範圍第 10 項所述之場效應電晶體，

其中該第一金屬材料為包括功函數金屬之一膜層。

15. 如申請專利範圍第 15 項所述之場效應電晶體，其中該膜層包括一上蓋層，而該上蓋層包括擇自由 TiN、Ta、TaN 與 WN 所組成族群之一材料。

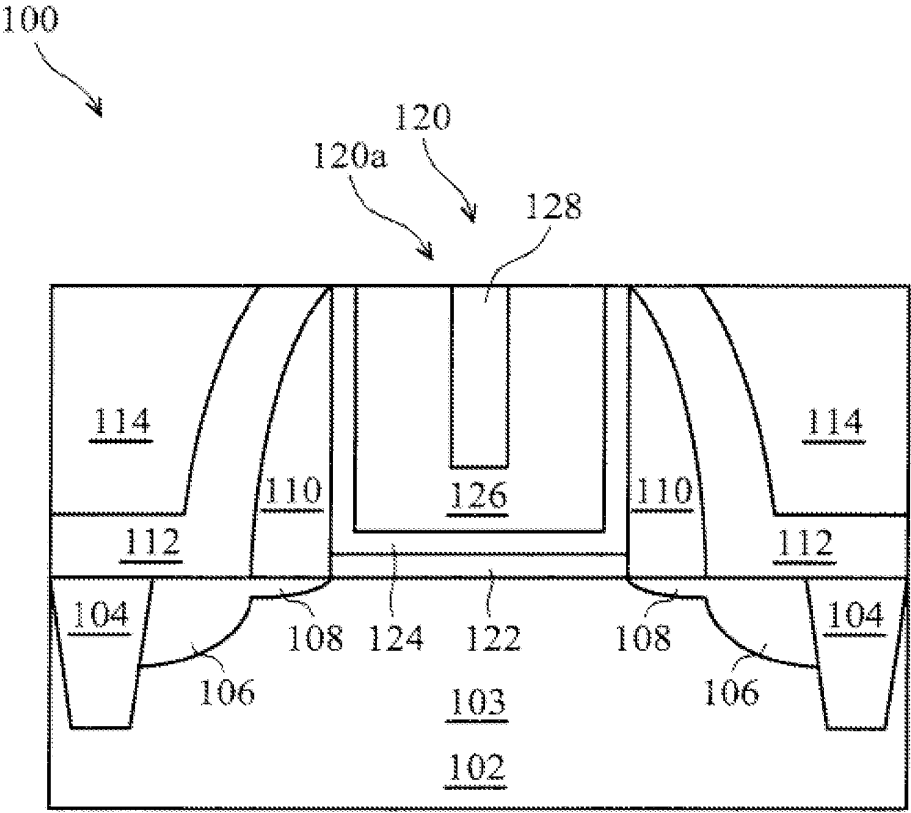
16. 如申請專利範圍第 10 項所述之場效應電晶體，其中該上方部為大體 T 形。

17. 如申請專利範圍第 10 項所述之場效應電晶體，其中該上方部具有介於 50~2700 埃之一最小高度。

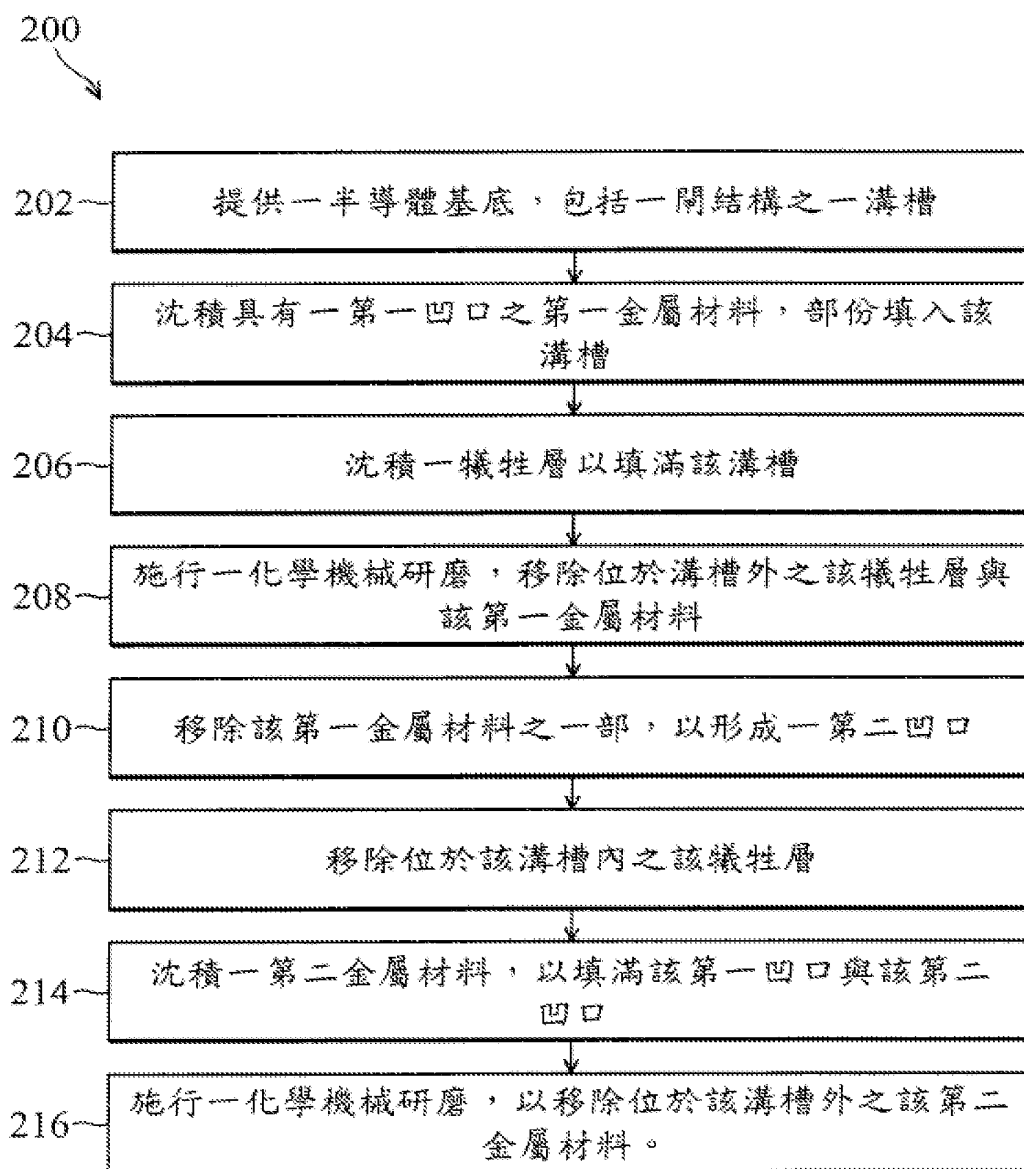
18. 如申請專利範圍第 10 項所述之場效應電晶體，其中該第二金屬材料包括擇自由 Al、Cu、Co 與 W 所組成族群之一材料。

19. 如申請專利範圍第 18 項所述之場效應電晶體，其中該第二金屬材料更包括一阻障層，而該阻障層包括擇自由 Ti、Ta、TiN、TaN 與 WN 所組成族群之一材料。

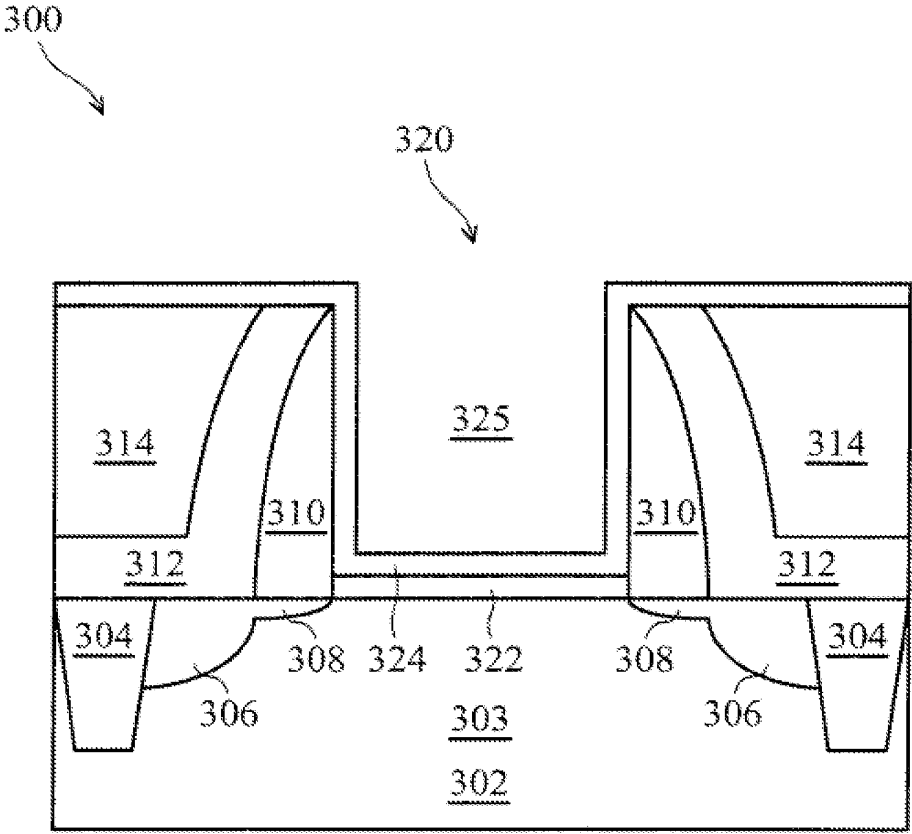
20. 如申請專利範圍第 10 項所述之場效應電晶體，其中該閘極介電層包括一高介電常數介電層。



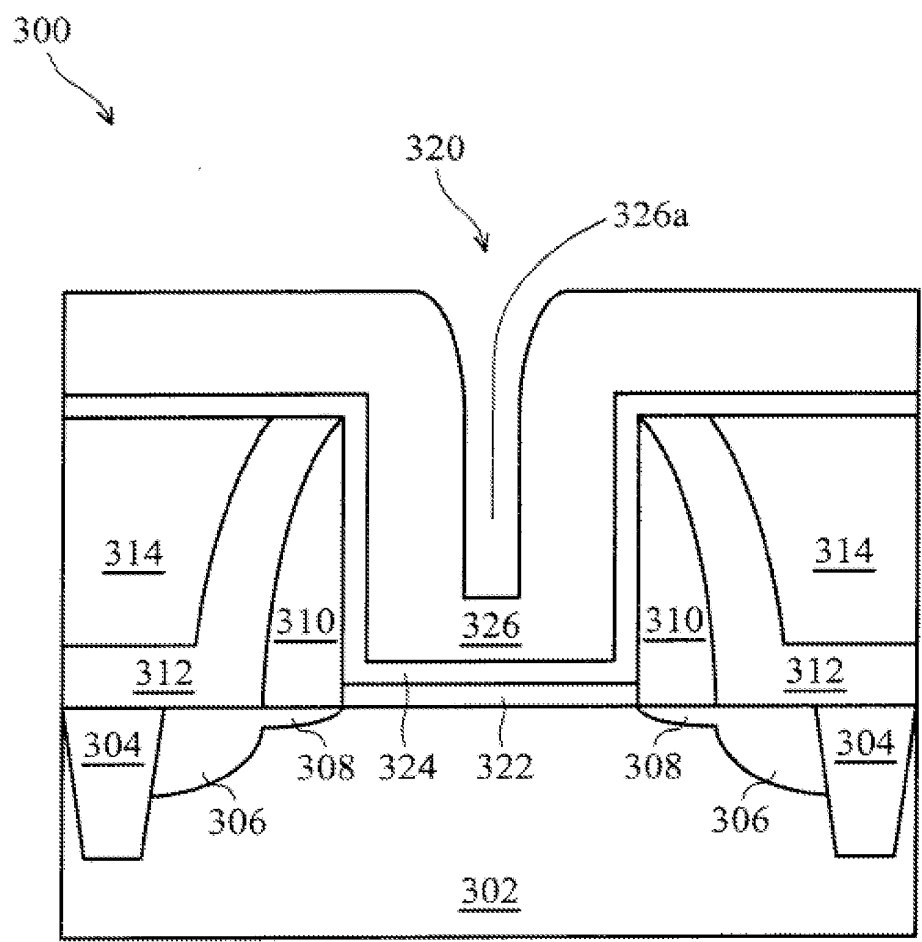
第 1 圖



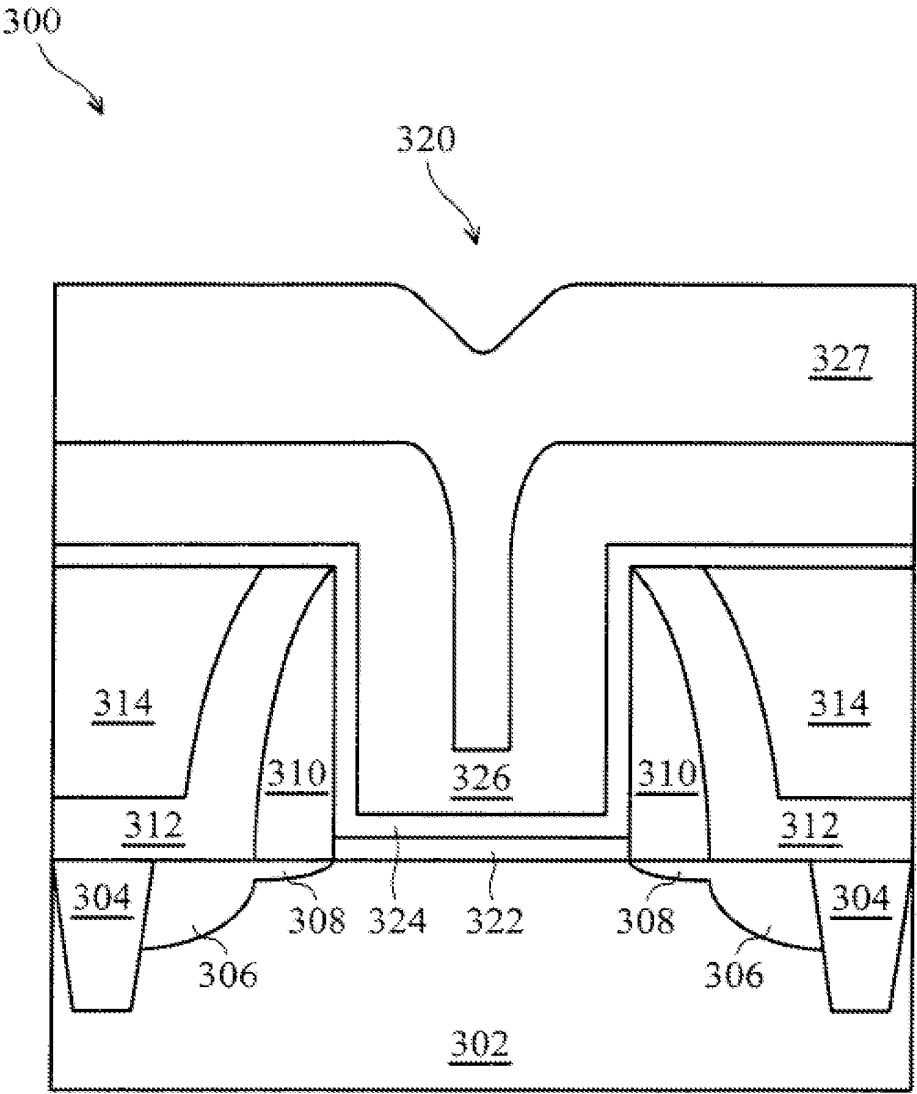
第 2 圖



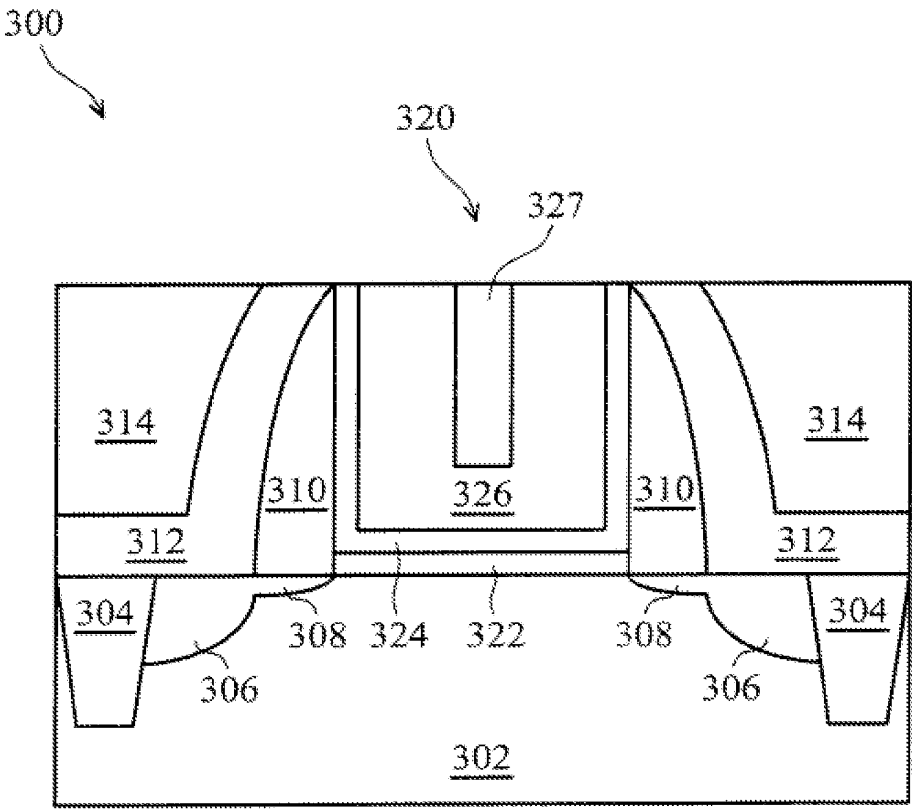
第 3A 圖



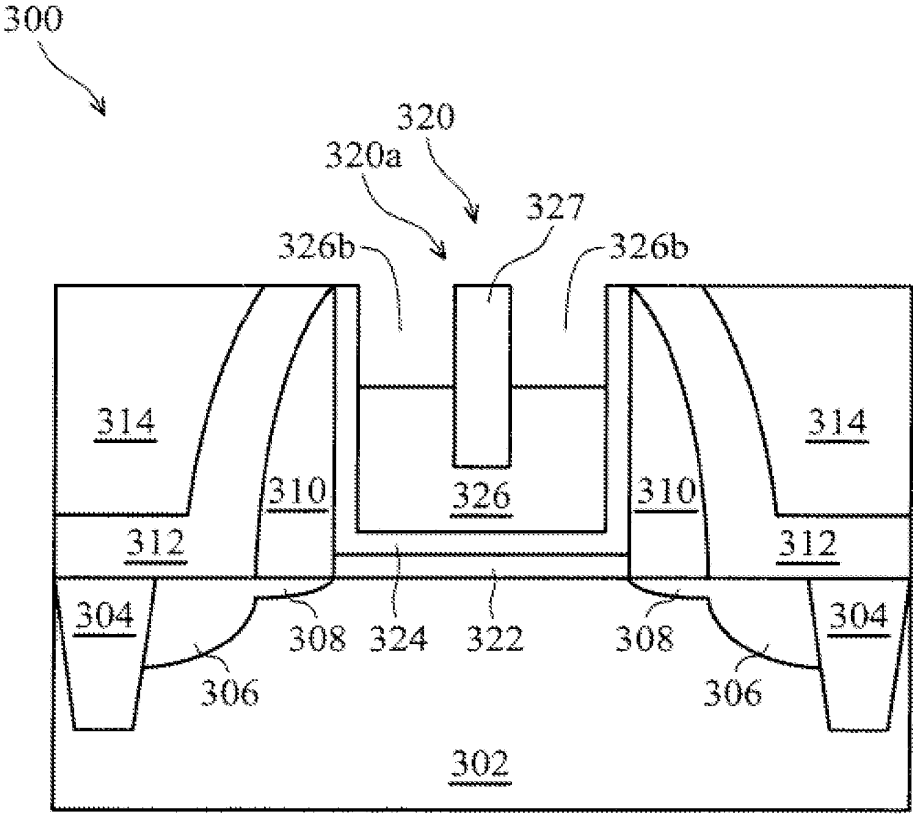
第 3B 圖



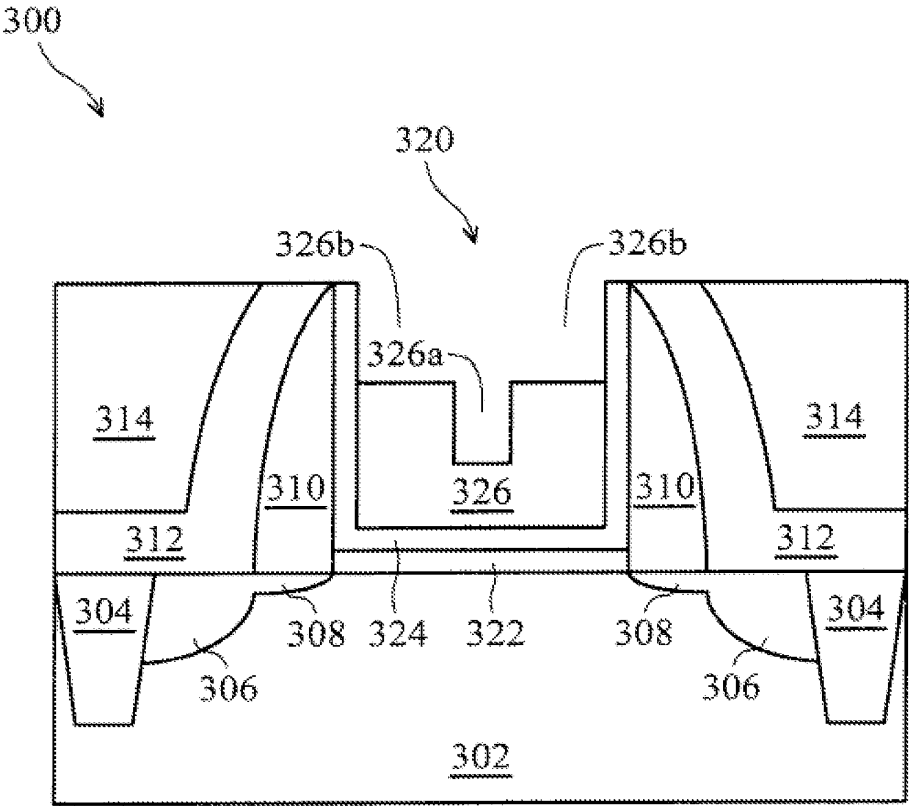
第 3C 圖



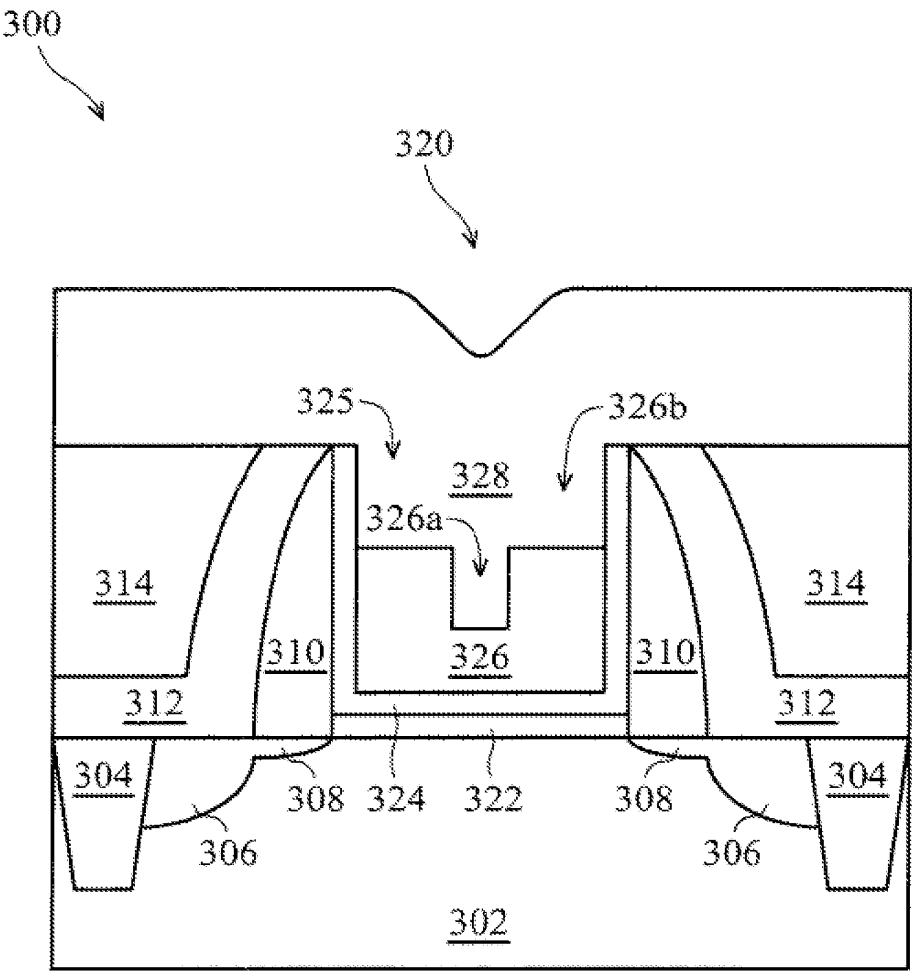
第 3D 圖



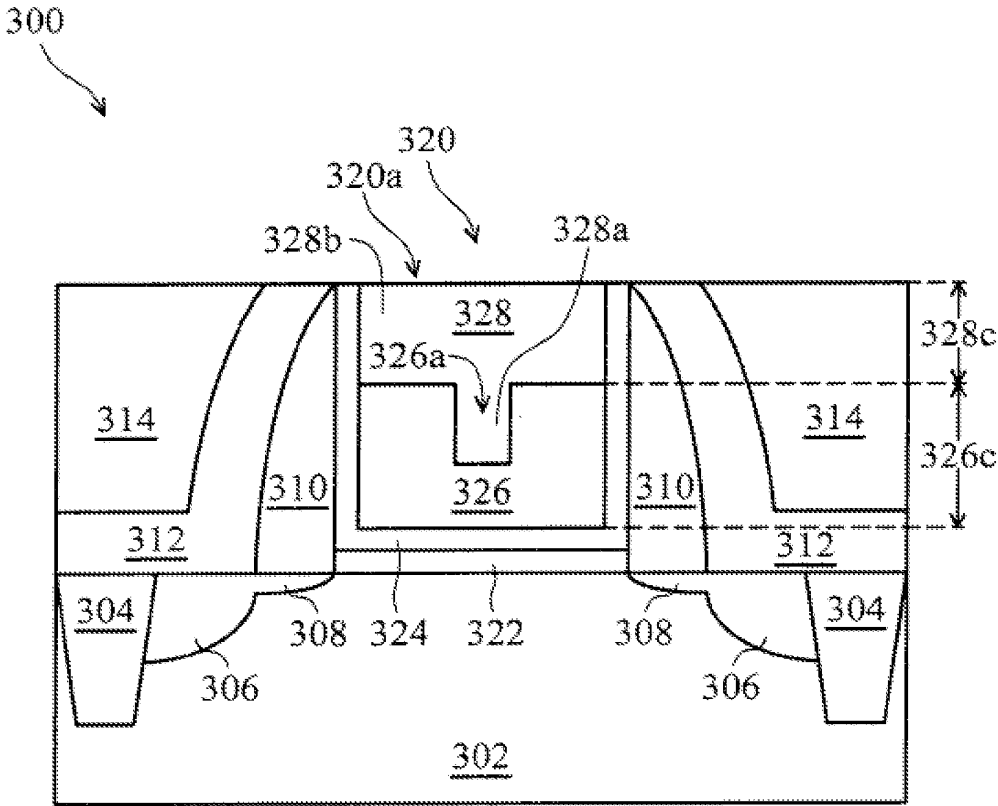
第 3E 圖



第 3F 圖



第 3G 圖



第 3H 圖

四、指定代表圖：

(一)本案指定代表圖為：第(3H)圖。

(二)本代表圖之元件符號簡單說明：

- 300~場效應電晶體；
- 302~半導體基底；
- 303~主動區；
- 304~隔離區；
- 306~源極/汲極區；
- 308~輕度摻雜源極/汲極區；
- 310~閘極間隔物；
- 312~接觸蝕刻停止層；
- 314~層間介電層；
- 320~閘極結構；
- 320a~經修正金屬閘極電極；
- 322~中間層；
- 324~閘極介電層；
- 326~第一金屬材料；
- 326a~第一金屬材料之第一凹口；
- 326c~下方部之最大高度；
- 328~第二金屬材料；
- 328a~第二金屬材料之突出部；
- 328b~金屬帶狀物；
- 328c~上方部之最小高度。

五、本案若有化學式時，請揭示最能顯示發明特徵的化學式：

六、發明說明：

【發明所屬之技術領域】

本發明係關於積體電路製作，且特別是關於具有金屬閘極電極(metal gate electrode)之一種場效應電晶體(field effect transistor, FET)。

【先前技術】

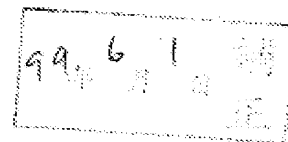
隨著電晶體尺寸的縮減，便需要降低閘極氧化物(gate oxide)厚度以維持具有經縮減閘極長度(gate length)之表現。然而，為了降低閘極漏電流(gate leakage)，因而採用了高介電常數(high-k)閘極介電膜層，於維持較大技術節點中所採用之習知閘極氧化物所具有之相同等效厚度時其可具有較高之物理厚度。

此外，隨著技術節點縮減，於部份積體電路設計中，便需要採用金屬閘極電極以取代習知多晶矽閘極電極，藉以改善具有縮減特徵尺寸之元件的表現。形成金屬閘極的製程之一係為“後閘極(gate last)”製程，其內金屬閘極係最後製備形成，因而允許了閘極電極免於受到某些高溫製程的影響，例如是受到源極/汲極回火程序的影響。

第 1 圖為一剖面圖，顯示了採用“後閘極”製程所製造得到之用於場效應電晶體 100 之一習知閘極結構(gate structure)120。在此，場效應電晶體 100 係形成於基底 102 內且鄰近於數個隔離區 104 之一主動區 103 之上。場效應電晶體 100 包括形成於基底 102 之主動區 103 內的數個源極/汲極區 106 與輕度摻雜區 108，包括依序形成於

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四、指定代表圖：

(一)本案指定代表圖為：第(3H)圖。

(二)本代表圖之元件符號簡單說明：

- 300~場效應電晶體；
- 302~半導體基底；
- 304~隔離區；
- 306~源極/汲極區；
- 308~輕度摻雜源極/汲極區；
- 310~閘極間隔物；
- 312~接觸蝕刻停止層；
- 314~層間介電層；
- 320~閘極結構；
- 320a~經修正金屬閘極電極；
- 322~中間層；
- 324~閘極介電層；
- 326~第一金屬材料；
- 326a~第一金屬材料之第一凹口；
- 326c~下方部之最大高度；
- 328~第二金屬材料；
- 328a~第二金屬材料之突出部；
- 328b~金屬帶狀物；
- 328c~上方部之最小高度。

五、本案若有化學式時，請揭示最能顯示發明特徵的化學式：



Espacenet

Bibliographic data: TW201208078 (A) — 2012-02-16

Interface structure for channel mobility improvement in high-k metal gate stack

Inventor(s): CHEN TZE-CHIANG [US]; GUO DE-CHAO [CN]; OLDIGES PHILIP J [US]; WANG YAN-FENG [CN] ± (CHEN, TZE-CHIANG, ; GUO, DE-CHAO, ; OLDIGES, PHILIP J, ; WANG, YAN-FENG)

Applicant(s): IBM [US] ± (INTERNATIONAL BUSINESS MACHINES CORPORATION)

Classification: - international: H01L21/28; H01L29/78
 - cooperative: H01L21/28176; H01L29/51; H01L29/513;
H01L29/517; H01L29/495; H01L29/4966;
H01L29/4975; H01L29/518

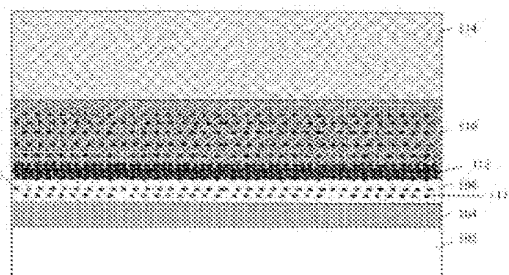
Application number: TW20110119394 20110602

Priority number (s): US20100792242 20100602

Also published as: US2011298060 (A1) US2011298060 (A1) US8492852 (B2) US8492852 (B2) GB2493463 (A) more

Abstract of TW201208078 (A)

A gate stack structure for field effect transistor (FET) devices includes a nitrogen rich first dielectric layer formed over a semiconductor substrate surface; a nitrogen deficient, oxygen rich second dielectric layer formed on the nitrogen rich first dielectric layer, the first and second dielectric layers forming, in combination, a bi-layer interfacial layer; a high-k dielectric layer formed over the bi-layer interfacial layer; a metal gate conductor layer formed over the high-k dielectric layer; and a work function adjusting dopant species diffused within the high-k dielectric layer and within the nitrogen deficient, oxygen rich second dielectric layer, and wherein the nitrogen rich first dielectric layer serves to separate the work function adjusting dopant species from the semiconductor substrate surface.





(19)中華民國智慧財產局

(12)發明說明書公開本

(11)公開編號：TW 201208078 A1

(43)公開日：中華民國 101 (2012) 年 02 月 16 日

(21)申請案號：100119394

(22)申請日：中華民國 100 (2011) 年 06 月 02 日

(51)Int. Cl.: H01L29/78 (2006.01)

H01L21/28 (2006.01)

(30)優先權：2010/06/02 美國

12/792,242

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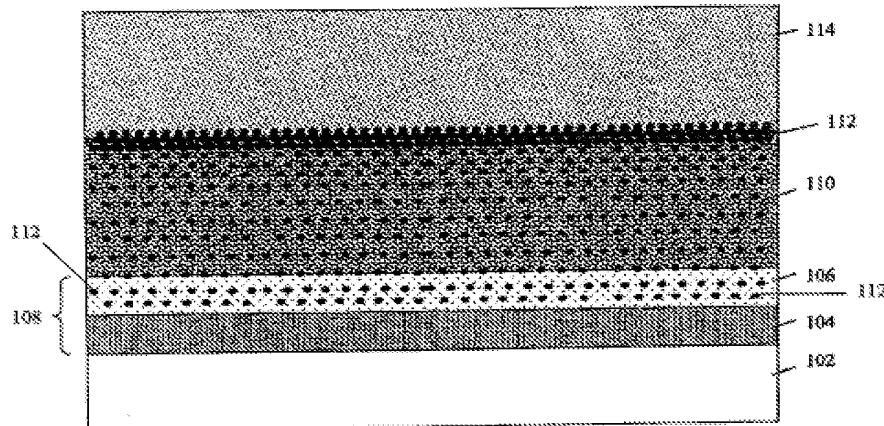
(54)名稱

於高介電常數金屬閘極堆疊中用以改善通道移動率的介面結構

INTERFACE STRUCTURE FOR CHANNEL MOBILITY IMPROVEMENT IN HIGH-K METAL GATE STACK

(57)摘要

本發明揭示一種用於場效電晶體(FET)裝置的閘極堆疊結構，其包括：一富氮第一介電層，其形成於一半導體基板表面之上；一缺氮、富氧第二介電層，其形成於該富氮第一介電層上，該第一介電層及該第二介電層共同形成一雙層介面層；一高介電常數介電層，其形成於該雙層介面層之上；一金屬閘極導體層，其形成於該高介電常數介電層之上；及一功函數調整摻雜物物種，其擴散於該高介電常數介電層及該缺氮、富氧第二介電層之內，及其中該富氮第一介電層用來隔開該功函數調整摻雜物物種與該半導體基板表面。



102：半導體基板

104：第一介電層

106：缺氮第二介電層

108：介面層

110：高介電常數閘極介電層

112：功函數調整摻雜物物種

114：金屬閘極導體層



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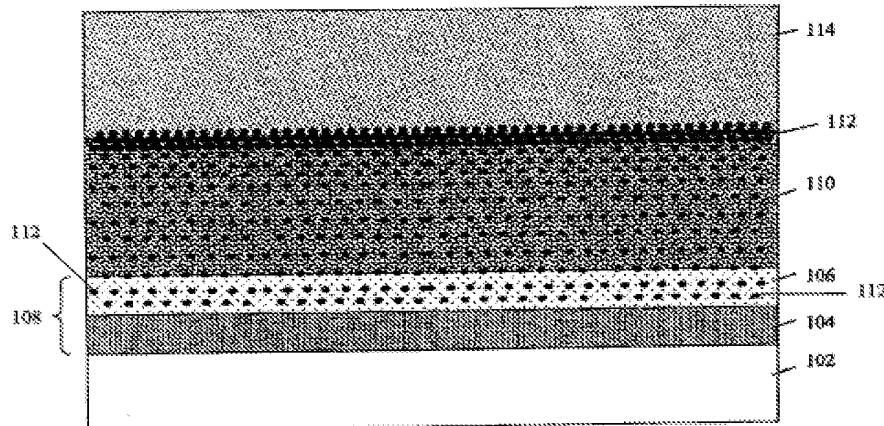
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102：半導體基板

104：第一介電層

106：缺氮第二介電層

108：介面層

110：高介電常數閘極介電層

112：功函數調整摻雜物物種

114：金屬閘極導體層

六、發明說明：

【發明所屬之技術領域】

本發明一般有關半導體裝置製造，尤其有關於高介電常數金屬閘極堆疊中用以改善通道移動率的介面結構。

【先前技術】

在標準的互補金屬氧化物半導體(CMOS)裝置中，通常使用多晶矽作為閘極材料。使用多晶矽閘極製造 CMOS 裝置的技術一直持續發展中，且現在廣泛使用於半導體工業中。使用多晶矽閘極的一個優點是其經得起高溫。然而，使用多晶矽閘極也會引起一些問題。例如，由於多晶矽空乏效應，CMOS 裝置中常用的多晶矽閘極變成通道長度 0.1 微米及以下之晶片性能的閘控因素。多晶矽閘極的另一問題是多晶矽閘極中的摻雜物材料(如，硼)可輕易擴散通過薄閘極介電質，進一步使裝置性能降級。因此，尤其隨著高介電常數閘極介電材料的出現，已提出一個改善次微米電晶體性能的方式是使用金屬閘極取代習用的多晶矽閘極。

儘管以金屬或金屬合金閘極電極取代傳統的多晶矽閘極解決了多晶矽空乏效應的問題，但使用金屬閘極及高介電常數閘極介電質還是有一些問題，包括例如因費米能階釘扎效應所造成的高臨限電壓(V_t)。臨限電壓是藉由在半導體通道表面形成反轉層使通道變成導電所需的閘極電壓值。對於增強模式(如，通常關閉)裝置， V_t 在 NFET 裝置中是正的及在 PFET 裝置中是負的。臨限電壓取決於平帶電壓，平帶電壓又取決於閘極及基板材料之間的功函數差，還有取決於表面電荷。

材料的功函數是將材料中電子從費米能階移出材料原子外所需能量的度量，且通常以電子伏特(eV)表示。在CMOS裝置中，需要對NFET及PFET提供穩定的臨限電壓。為了建立 V_t 值，獨立調諧或調整NFET及PFET閘極接觸及對應之通道材料的功函數。n通道電極及p通道電極的此類功函數值分別可以例如約4.1及5.2電子伏特(eV)。因此，採用閘極堆疊工程設計調整閘極接觸材料的功函數，其中針對NFET及PFET閘極建立不同的閘極功函數值。

【發明內容】

在一例示性具體實施例中，一種用於場效電晶體(FET)裝置的閘極堆疊結構包括：一富氮第一介電層，其形成於一半導體基板表面之上；一缺氮、富氧第二介電層，其形成於該富氮第一介電層上，該第一介電層及該第二介電層共同形成一雙層介面層；一高介電常數介電層，其形成於該雙層介面層之上；一金屬閘極導體層，其形成於該高介電常數介電層之上；及一功函數調整摻雜物物種，其擴散於該高介電常數介電層及該缺氮、富氧第二介電層之內，及其中該富氮第一介電層用來隔開該功函數調整摻雜物物種與該半導體基板表面。

在另一具體實施例中，一種用於場效電晶體(FET)裝置的高介電常數金屬閘極堆疊結構包括：一富氮第一介電層，其形成於一半導體基板表面之上；一缺氮、富氧第二介電層，其形成於該富氮第一介電層上，該第一介電層及該第二介電層共同形成一雙層介面層；一鉛基、高介電常數介電層，其形成於該雙層介面層之上；一金屬閘極導體層，其形

成於該高介電常數介電層之上；及一鏷摻雜物物種，其擴散於該高介電常數介電層及該缺氮、富氮第二介電層之內，在其中形成一高介電常數氧化鏷，及其中該富氮第一介電層用來隔開該高介電常數氧化鏷與該半導體基板表面。

在另一具體實施例中，一種形成用於場效電晶體(FET)裝置的閘極堆疊結構的方法包括：形成一富氮第一介電層於一半導體基板表面之上；形成一缺氮、富氮第二介電層於該富氮第一介電層上，該第一介電層及該第二介電層共同界定一雙層介面層；形成一高介電常數介電層於該雙層介面層之上；形成一金屬閘極導體層於該高介電常數介電層之上；及擴散一功函數調整摻雜物物種於該高介電常數介電層及該缺氮、富氮第二介電層之內，及其中該富氮第一介電層用來隔開該功函數調整摻雜物物種與該半導體基板表面。

【實施方式】

如上文指出，採用各種閘極堆疊工程設計技術以調整高介電常數金屬閘極(HKMG)結構的功函數。例如，在介面層及高介電常數層形成於半導體基板之上後，可沉積鏷系元素物種材料，諸如鏷(La)或鐳(Lu)。介面層通常是較低介電常數介電層，諸如氧化矽、氮化矽或氮氧化矽層(無論以特定步驟形成或作為高介電常數形成的副產品)，及用來隔開高介電常數層與在基板中形成的通道區。這麼做是需要的，因為高介電常數介電材料通常具有與氧化物有關的高缺陷密度。由於這些缺陷產生妨礙電荷載子移動率的電荷捕捉位置，存在介面層可隔開高介電常數層與通道區。

在沉積鍺系元素物種材料後，接著使用熱製程，諸如退火步驟，驅使鍺系元素物種向下朝向介面層。此擴散用來(1)降低 NFET 裝置的 V_t 及(2)藉由增加介面層介電常數，達成反轉厚度(T_{inv})微縮。另一方面，此擴散亦用來降低通道中的載子移動率，因為與以習用方式形成之介面層中之(例如) La_xO_y 相關聯的軟光學聲子效應接近(或甚至接觸)半導體表面。雖然使介面層變厚及降低高介電常數層的厚度以獲得 T_{inv} 微縮，可提高載子移動率，但這會造成高閘極穿隧電流。因此，為了維持得自高介電常數介電質的閘極漏電好處、維持得自如 La、Lu 之物種的 T_{inv} 微縮及 V_t 減少的好處且不會使載子移動率降級，需要新的解決方案。

因此，本文揭示一種用於高介電常數 FET 閘極堆疊的新穎介面層結構，其可維持 T_{inv} 微縮及 V_t 減少的好處，而且還可以降低或甚至消除載子移動率降級。簡而言之，介面層是一種雙層，其包括鄰接半導體表面的富氮第一層，及在富氮第一層上形成的缺氮、富氧第二層。以此方式形成，使得可供 T_{inv} 微縮及 V_t 減少的擴散鍺系元素物種與反轉通道保持足夠的距離，藉此提高載子移動率。

一開始先參考圖 1(a)至 1(f)，其中顯示一系列橫截面圖，其根據本發明之一具體實施例，圖解形成用於高介電常數 FET 閘極堆疊之介面層結構的例示性方法。從圖 1(a)開始，半導體基板 102 的通道表面具有直接在其上形成(諸如藉由生長或沉積)的薄富氮第一介電層 104，其例示性厚度約 10 至約 20 埃(Å)。基板 102 可包括任何合適的半導體材料，諸如但不限於：矽(Si)、鍺(Ge)、矽鍺(SiGe)、碳化矽(SiC)、碳化矽鍺(SiGeC)、砷化鎵(GaAs)、氮化鎵(GaN)、砷化鎵

(InAs)、磷化銦(InP)及所有其他 III/V 或 II/VI 化合物半導體。半導體基板 102 亦可包含有機半導體或分層半導體，如 Si/SiGe、絕緣體上矽(SOI)、絕緣體上矽鍺(SGOI)或絕緣體上鍺(GOI)。第一介電層 104 可包括例如氮化矽(SiN)或氮氧化矽(SiON)。

接著，如圖 1(b)所示，缺氮第二介電層 106 諸如藉由沉積，形成於富氮第一介電層 104 之上，其例示性厚度例如約 10Å。缺氮第二介電層 106 例如可以是臭氧層或氧化物層。以此方式形成，使得富氮第一介電層 104 及缺氮第二介電層 106 界定介面層 108。

接下來參考圖 1(c)，在一具體實施例中，在完成介面層 108 後，接著形成高介電常數閘極介電層 110。如本文中使用的術語「高介電常數」一般代表絕緣體具有介電常數大於約 4.0，及更明確地說，大於 7.0。高介電常數閘極介電層 110 例如可以是鈺(Hf)基層。合適的高介電常數介電層的更明確範例可包括但不限於：氧化鈺(HfO_2)、正矽酸鈺(HfSiO_4)、二氧化鋯(ZrO_2)、氧化鋁(Al_2O_3)、二氧化鈦(TiO_2)、氧化釷(La_2O_3)、鈦酸鋇(SrTiO_3)、鋁酸釷(LaAlO_3)、氧化鈾(CeO_2)、氧化釷(Y_2O_3)及其組合。高介電常數閘極介電層 110 的厚度可取決於有關閘極穿隧電流的特定需求。

接著，如圖 1(d)所示，功函數調整摻雜物物種 112(諸如釷系元素物種)沉積在高介電常數閘極介電層 110 上。物種 112 可包括例如釷系元素金屬，諸如釷(La)、鈾(Ce)、鐳(Pr)、鈳(Nd)、鉕(Pm)、釷(Sm)、鎔(Eu)、釷(Gd)、鈹(Tb)、鐳(Dy)、鈳(Ho)、鉕(Er)、鈳(Tm)、鐳(Yb)或鐳(Lu)。其他非釷系元

素材料，諸如鈐(Hf)，亦可用作功函數調整摻雜物物種 112。根據閘極優先程序流程，合適的一或多個金屬閘極導體層 114、及任何相關聯的帽蓋層(未顯示)接著形成於摻雜物物種 112 及高介電常數閘極介電層 110 之上，如圖 1(e)所示。金屬閘極導體層 114 可包括例如元素金屬，諸如鎢(W)、鉭(Ta)、鋁(Al)、鈦(Ru)、鉑(Pt)等，或任何導電化合物，包括但不限於：矽化鎳(NiSi)、矽化鎳鉑(NiPtSi)、氮化鈦(TiN)、氮化鉭(TaN)、碳化鈦(TiC)、碳化鉭(TaC)、氮氧碳化鉭(TaCNO)、氧化鈦(RuO_2)等、及其組合及多層。

在圖 1(e)中，對所形成的閘極堆疊結構進行熱製程，使物種 112 向下擴散至缺氮第二介電層 106，以達成 NFET 裝置的 T_{inv} 微縮及 V_t 減少。尤其，擴散的物種在第二介電層 106 的頂部及高介電常數介電層 110 之間建立電荷雙極，致使可調整低 V_t NFET 應用的有效功函數。然而，物種 112 係包含在缺氮第二介電層 106 之內，而非在富氮第一介電層 104 之內，藉此使物種 112 與基板 102 中形成的反轉通道保持足夠的距離。在一例示性具體實施例中，高介電常數介電層 110 為鈐基，摻雜物物種為鐳，及退火操作導致在缺氮、富氮第二介電層 106 之內形成高介電常數氧化鐳(La_2O_3)。因此， T_{inv} 微縮及 V_t 減少並未受到載子移動率減少的影響。

在上文描述的具體實施例中，將摻雜物物種 112 描繪為在形成高介電常數層 110 後沉積。然而，其他替代選項也是可行。例如，如圖 2(a)至 2(d)的程序流程順序所示，可在形成高介電常數層 110 之前，先形成摻雜物物種 112。在圖 2(a)中，摻雜物物種 112 在形成缺氮第二介電層 106 後沉積，接著形成高介電常數介電層 110，如圖 2(b)所示。接著，圖 2(c)

圖解在高介電常數層 110 之上形成一或多個金屬閘極導體層 114 及任何相關聯的帽蓋層(未顯示)。最後，在圖 2(d)中執行退火，以驅使摻雜物物種 112 進入缺氫第二介電層 106 但不在富氫第一介電層 104 之內。在又另外設想的具體實施例中，摻雜物物種 112 可在形成高介電常數層 110 的同時沉積。

雖然本發明已參考較佳具體實施例進行說明，但熟習本技術者應明白，在不脫離本發明的範疇下，可進行各種改變，並可以同等物取代其中元件。此外，在不脫離本發明的基本範疇下，可對本發明的說明內容進行許多修改以適應特別情況或材料。因此，預計本發明並不受限於揭露為執行本發明所設想之最佳模式的特定具體實施例；而是預計本發明將包括所有落在隨附申請專利範圍之範疇內的具體實施例。

【圖式簡單說明】

請參考例示性圖式，其中若干圖中的相同元件具有相同編號：

圖 1(a)至 1(f)是一系列橫截面圖，其根據本發明之一具體實施例，圖解形成用於高介電常數 FET 閘極堆疊之介面層結構的例示性方法；及

圖 2(a)至 2(d)是一系列橫截面圖，其根據本發明之一替代具體實施例，圖解形成用於高介電常數 FET 閘極堆疊之介面層結構的例示性方法。

【主要元件符號說明】

201208078

- 102 半導體基板
- 104 第一介電層
- 106 缺氮第二介電層
- 108 介面層
- 110 高介電常數閘極介電層
- 112 功函數調整摻雜物物種
- 114 金屬閘極導體層

發明專利說明書

(本說明書格式、順序，請勿任意更動，※記號部分請勿填寫)

※ 申請案號：100119394

※ 申請日：100 年 6 月 2 日

※IPC 分類：

H01L 29/78 (2006.01)

一、發明名稱：(中文/英文)

H01L 21/28 (2006.01)

於高介電常數金屬閘極堆疊中用以改善通道移動率的介面結構

INTERFACE STRUCTURE FOR CHANNEL MOBILITY IMPROVEMENT IN HIGH-K METAL GATE STACK

二、中文發明摘要：

本發明揭示一種用於場效電晶體(FET)裝置的閘極堆疊結構，其包括：一富氮第一介電層，其形成於一半導體基板表面之上；一缺氮、富氧第二介電層，其形成於該富氮第一介電層上，該第一介電層及該第二介電層共同形成一雙層介面層；一高介電常數介電層，其形成於該雙層介面層之上；一金屬閘極導體層，其形成於該高介電常數介電層之上；及一功函數調整摻雜物物種，其擴散於該高介電常數介電層及該缺氮、富氧第二介電層之內，及其中該富氮第一介電層用來隔開該功函數調整摻雜物物種與該半導體基板表面。

三、英文發明摘要：

A gate stack structure for field effect transistor (FET) devices includes a nitrogen rich first dielectric layer formed over a semiconductor substrate surface; a nitrogen deficient, oxygen rich second dielectric layer formed on the nitrogen

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rich first dielectric layer, the first and second dielectric layers forming, in combination, a bi-layer interfacial layer; a high-k dielectric layer formed over the bi-layer interfacial layer; a metal gate conductor layer formed over the high-k dielectric layer; and a work function adjusting dopant species diffused within the high-k dielectric layer and within the nitrogen deficient, oxygen rich second dielectric layer, and wherein the nitrogen rich first dielectric layer serves to separate the work function adjusting dopant species from the semiconductor substrate surface.

七、申請專利範圍：

1. 一種用於場效電晶體(FET)裝置的閘極堆疊結構，包含：
 - 一富氮第一介電層，其形成於一半導體基板表面之上；
 - 一缺氮、富氧第二介電層，其形成於該富氮第一介電層上，該第一介電層及該第二介電層共同形成一雙層介面層；
 - 一高介電常數介電層，其形成於該雙層介面層之上；
 - 一金屬閘極導體層，其形成於該高介電常數介電層之上；
 及
 - 一功函數調整摻雜物物種，其擴散於該高介電常數介電層及該缺氮、富氧第二介電層之內，及其中該富氮第一介電層用來隔開該功函數調整摻雜物物種與該半導體基板表面。
2. 如申請專利範圍第 1 項所述之結構，其中該功函數調整摻雜物物種包含一鐳系元素金屬；或其中該功函數調整摻雜物物種包含以下一或多者：鐳(La)、鈰(Ce)、鐮(Pr)、釹(Nd)、鉕(Pm)、釷(Sm)、鈾(Eu)、釷(Gd)、釷(Tb)、鐳(Dy)、釹(Ho)、鉕(Er)、銩(Tm)、鐳(Yb)、鐳(Lu)、及鈹(Hf)。
3. 如申請專利範圍第 1 項所述之結構，其中該富氮第一介電層包含氮化矽(SiN)及氮氧化矽(SiON)之一或多者；或其中該缺氮、富氧第二介電層包含一臭氧層及一氧化物層之一者。
4. 如申請專利範圍第 1 項所述之結構，其中該高介電常數介電層具有介電常數為約 4.0 或更高；或其中該高介電常數介電層具有介電常數為約 7.0 或更高；或其中該高介電常數介電層包含以下一或多者：氧化鈹(HfO₂)、正矽酸鈹(HfSiO₄)、二氧化鋯(ZrO₂)、氧化鋁(Al₂O₃)、二氧化鈦(TiO₂)、氧化鐳(La₂O₃)、

鈦酸鋇(SrTiO_3)、鋁酸鐳(LaAlO_3)、氧化鈣(CeO_2)、氧化釷(Y_2O_3)及其組合。

5. 如申請專利範圍第 1 項所述之結構，其中該金屬閘極導體層包含以下一或多者：鎢(W)、鉭(Ta)、鋁(Al)、鈳(Ru)、鉑(Pt)等，或任何導電化合物，包括但不限於矽化鎳(NiSi)、矽化鎳鉑(NiPtSi)、氮化鈦(TiN)、氮化鉭(TaN)、碳化鈦(TiC)、碳化鉭(TaC)、氮氧碳化鉭(TaCNO)、氧化鈳(RuO_2)、及其組合；或其中該基板包含以下一或多者：矽(Si)、鍺(Ge)、矽鍺(SiGe)、碳化矽(SiC)、碳化矽鍺(SiGeC)、砷化鎵(GaAs)、氮化鎵(GaN)、砷化銦(InAs)、及磷化銦(InP)。

6. 一種用於場效電晶體(PET)裝置的高介電常數金屬閘極堆疊結構，包含：

一富氮第一介電層，其形成於一半導體基板表面之上；

一缺氮、富氧第二介電層，其形成於該富氮第一介電層上，該第一介電層及該第二介電層共同形成一雙層介面層；

一鈣基、高介電常數介電層，其形成於該雙層介面層之上；

一金屬閘極導體層，其形成於該高介電常數介電層之上；

及

一鐳摻雜物物種，其擴散於該高介電常數介電層及該缺氮、富氧第二介電層之內，在其中形成一高介電常數氧化鐳，及其中該富氮第一介電層用來隔開該高介電常數氧化鐳與該半導體基板表面。

7. 如申請專利範圍第 6 項所述之結構，其中該富氮第一介電

層包含氮化矽(SiN)及氮氧化矽(SiON)之一或多者；或其中該缺氮、富氧第二介電層包含一臭氧層及一氧化物層之一者。

8. 如申請專利範圍第 6 項所述之結構，其中該高介電常數介電層具有介電常數為約 7.0 或更高；或其中該高介電常數介電層包含氧化鈺(HfO₂)及正矽酸鈺(HfSiO₄)之一或多者。

9. 如申請專利範圍第 6 項所述之結構，其中該金屬閘極導體層包含以下一或多者：鎢(W)、鉭(Ta)、鋁(Al)、鈦(Ru)、鉑(Pt)等，或任何導電化合物，包括但不限於矽化鎳(NiSi)、矽化鎳鉑(NiPtSi)、氮化鈦(TiN)、氮化鉭(TaN)、碳化鈦(TiC)、碳化鉭(TaC)、氮氧碳化鉭(TaCNO)、氧化鈦(RuO₂)、及其組合；或其中該基板包含以下一或多者：矽(Si)、鍺(Ge)、矽鍺(SiGe)、碳化矽(SiC)、碳化矽鍺(SiGeC)、砷化鎵(GaAs)、氮化鎵(GaN)、砷化銦(InAs)、及磷化銦(InP)。

10. 一種形成用於場效電晶體(FET)裝置之閘極堆疊結構的方法，該方法包含：

形成一富氮第一介電層於一半導體基板表面之上；

形成一缺氮、富氧第二介電層於該富氮第一介電層上，該第一介電層及該第二介電層共同界定一雙層介面層；

形成一高介電常數介電層於該雙層介面層之上；

形成一金屬閘極導體層於該高介電常數介電層之上；及

擴散一功函數調整摻雜物物種於該高介電常數介電層及該缺氮、富氧第二介電層之內，及其中該富氮第一介電層用來隔開該功函數調整摻雜物物種與該半導體基板表面。

11. 如申請專利範圍第 10 項所述之方法，其中該功函數調整摻雜物物種包含一鐳系元素金屬；或其中該功函數調整摻雜物物種包含以下一或多者：鐳(La)、鈰(Ce)、鐮(Pr)、釹(Nd)、鉕(Pm)、釷(Sm)、鈾(Eu)、釷(Gd)、錒(Tb)、鐿(Dy)、釹(Ho)、銲(Er)、鐿(Tm)、鐿(Yb)、鐳(Lu)、及鈪(Hf)；或其中該富氮第一介電層包含氮化矽(SiN)及氮氧化矽(SiON)之一或多者。

12. 如申請專利範圍第 10 項所述之方法，其中該缺氮、富氧第二介電層包含一臭氧層及一氧化物層之一；其中該高介電常數介電層具有介電常數為約 4.0 或更高；或其中該高介電常數介電層包含以下一或多者：氧化鈪(HfO_2)、正矽酸鈪(HfSiO_4)、二氧化鋯(ZrO_2)、氧化鋁(Al_2O_3)、二氧化鈦(TiO_2)、氧化鐳(La_2O_3)、鈦酸鋇(SrTiO_3)、鋁酸鐳(LaAlO_3)、氧化鈰(CeO_2)、氧化釹(Y_2O_3)及其組合。

13. 如申請專利範圍第 10 項所述之方法，其中該高介電常數介電層具有介電常數為約 7.0 或更高。

14. 如申請專利範圍第 10 項所述之方法，其中該金屬閘極導體層包含以下一或多者：鎢(W)、鉭(Ta)、鋁(Al)、鈱(Ru)、鉑(Pt)等，或任何導電化合物，包括但不限於矽化鎳(NiSi)、矽化鎳鉑(NiPtSi)、氮化鈦(TiN)、氮化鉭(TaN)、碳化鈦(TiC)、碳化鉭(TaC)、氮氣碳化鉭(TaCNO)、氧化鈱(RuO_2)、及其組合；或其中該基板包含以下一或多者：矽(Si)、鍺(Ge)、矽鍺(SiGe)、碳化矽(SiC)、碳化矽鍺(SiGeC)、砷化鎵(GaAs)、氮化鎵(GaN)、

砷化銦(InAs)、及磷化銦(InP)。

15. 如申請專利範圍第 10 項所述之方法，另外包含在形成該高介電常數介電層後，沉積該功函數調整摻雜物物種；或另外包含在形成該高介電常數介電層之前，沉積該功函數調整摻雜物物種；或另外包含在形成該高介電常數介電層的同時，沉積該功函數調整摻雜物物種。

八、圖式：

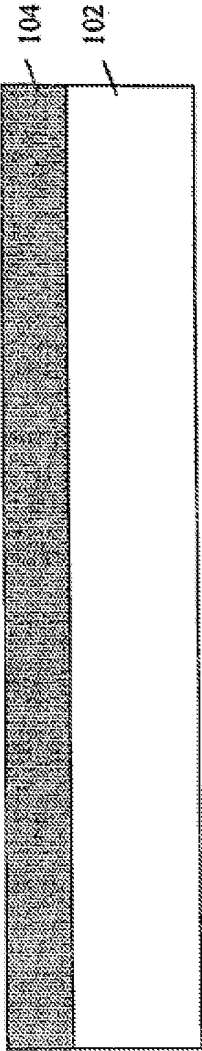


圖 1(a)

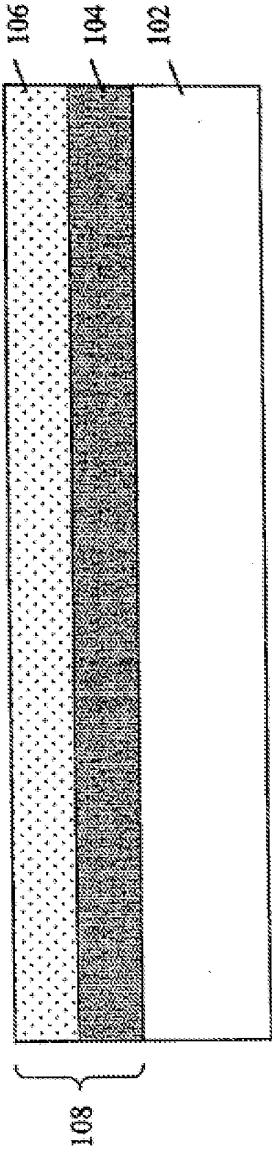


圖 1(b)

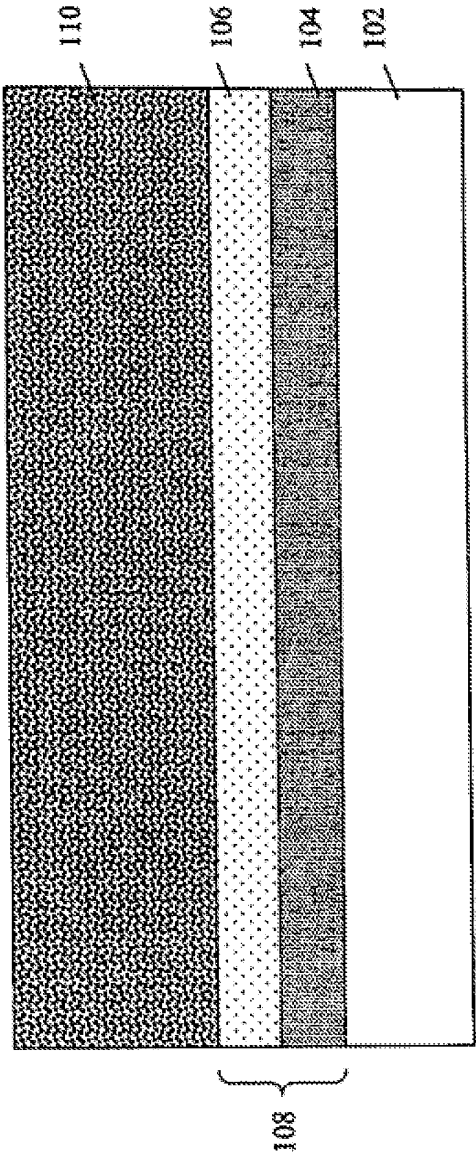


圖 1(c)

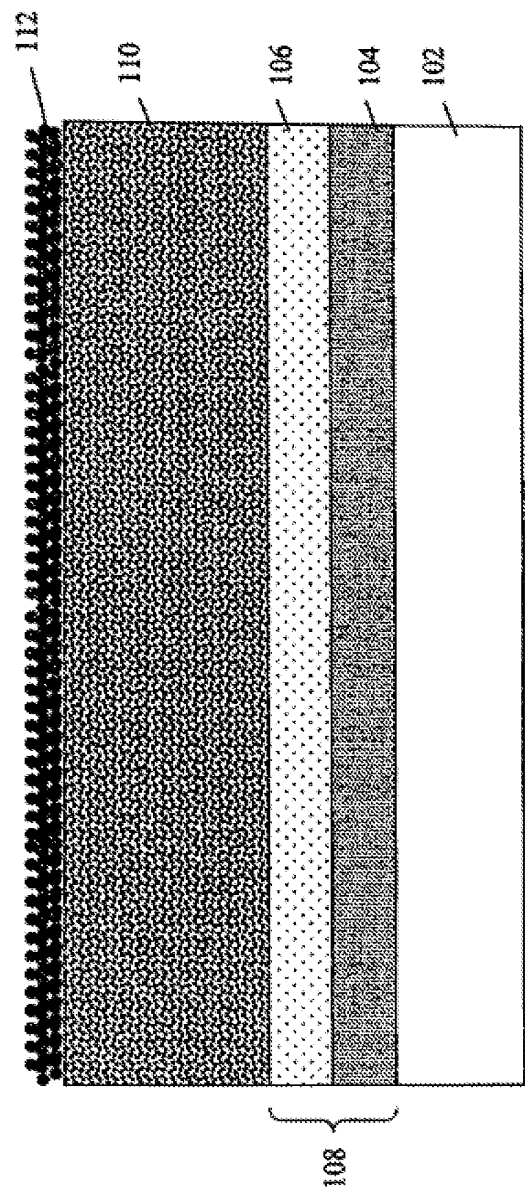


圖 1(d)

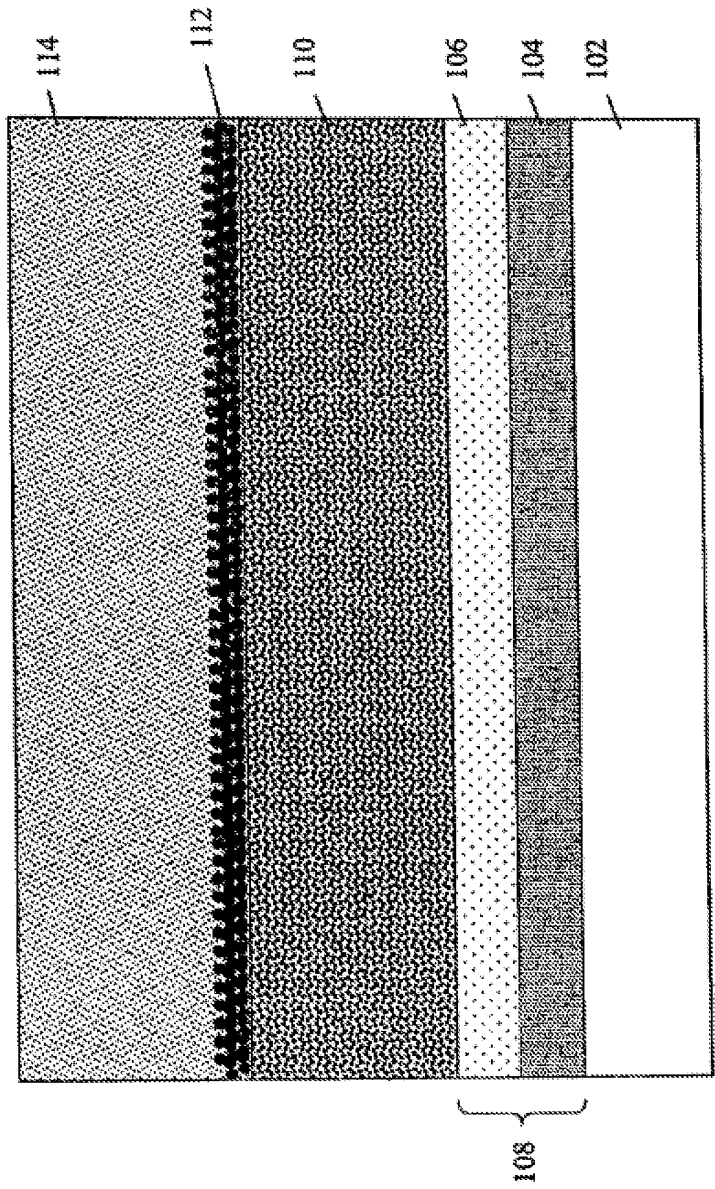


圖 1(e)

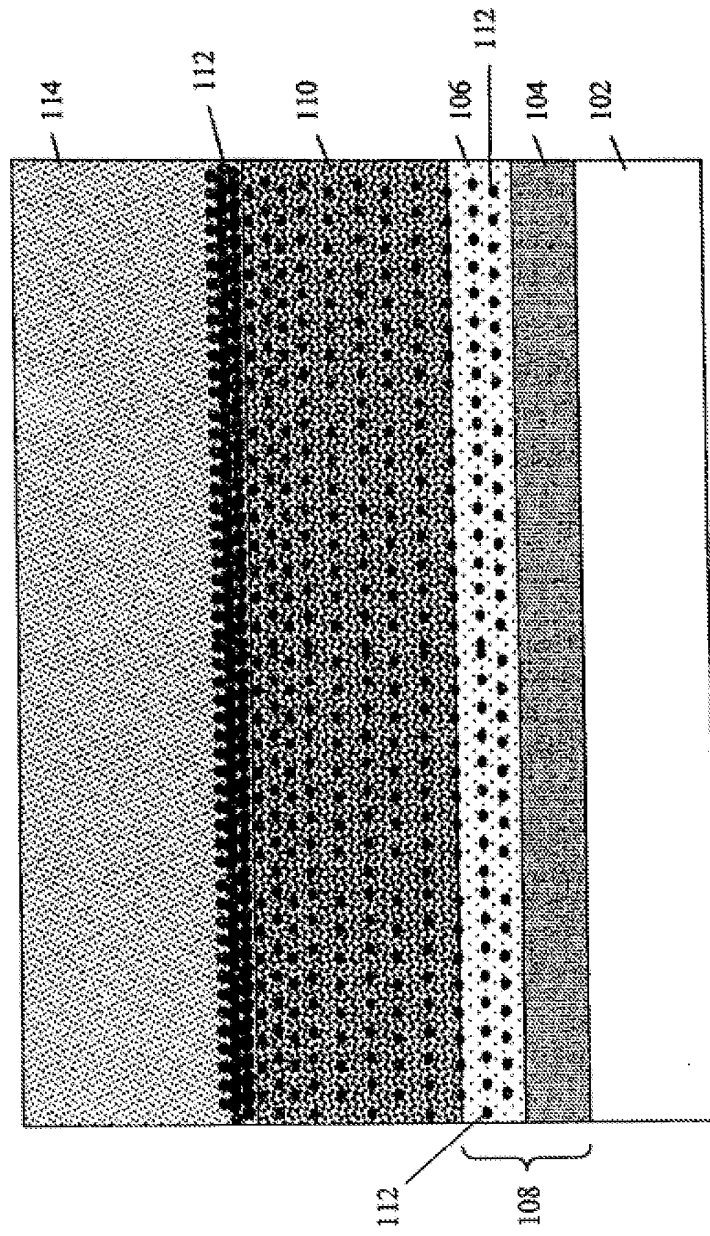


圖 1(f)

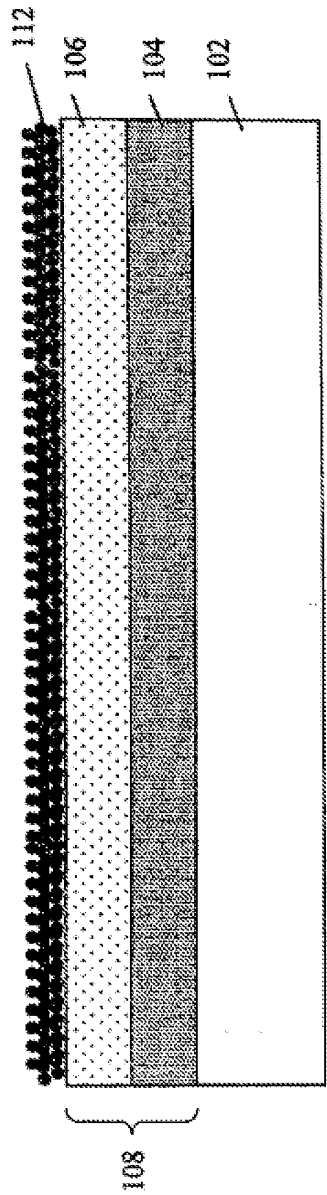


圖 2(a)

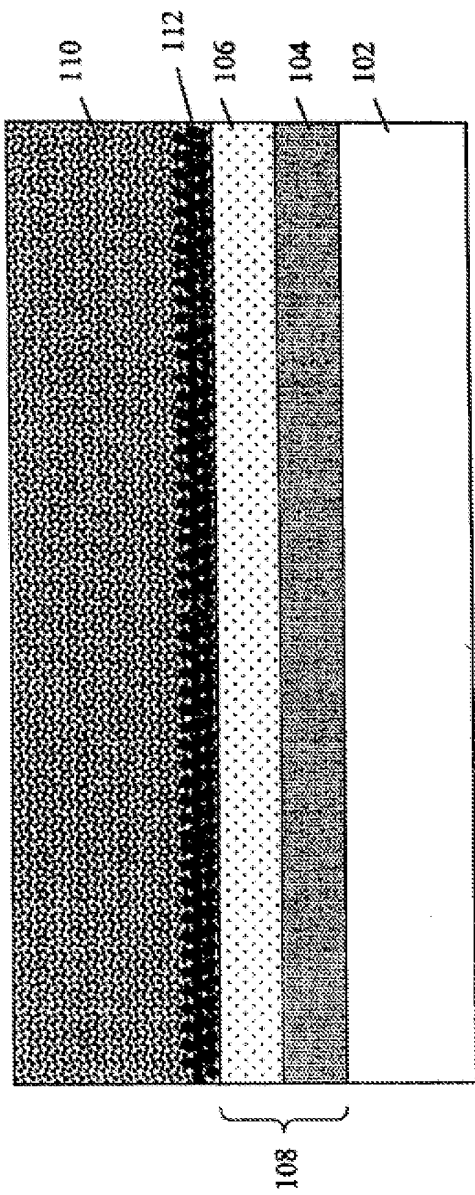


圖 2(b)

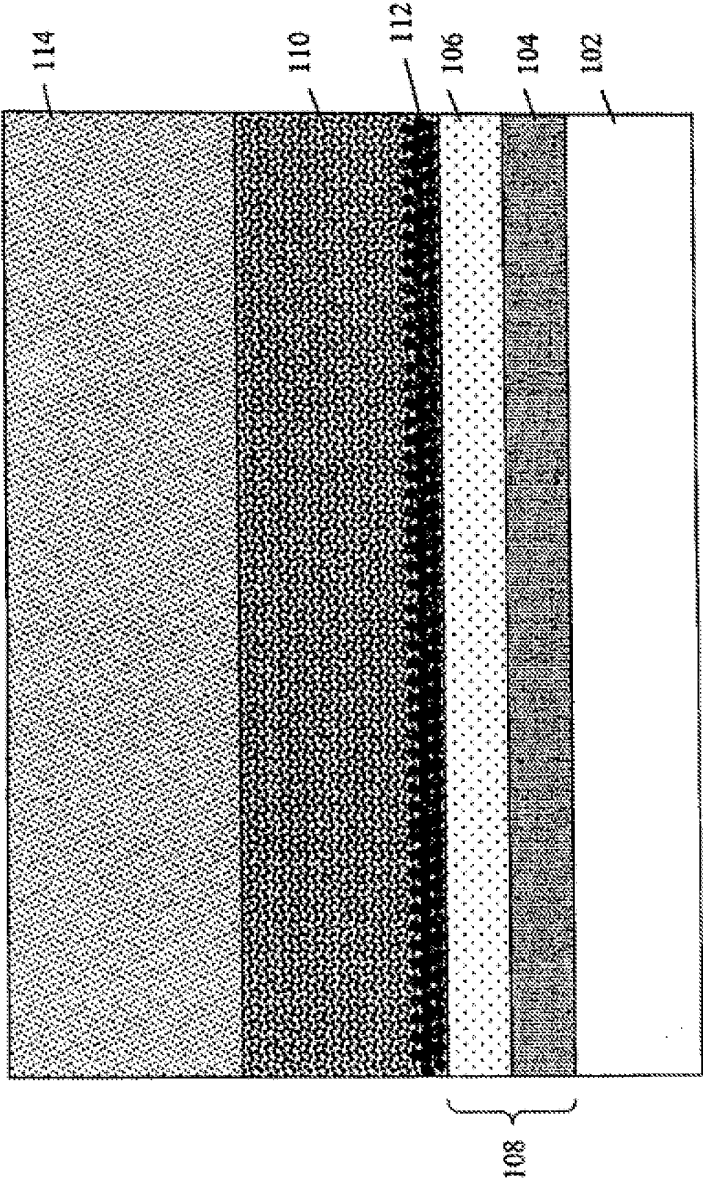


圖 2(c)

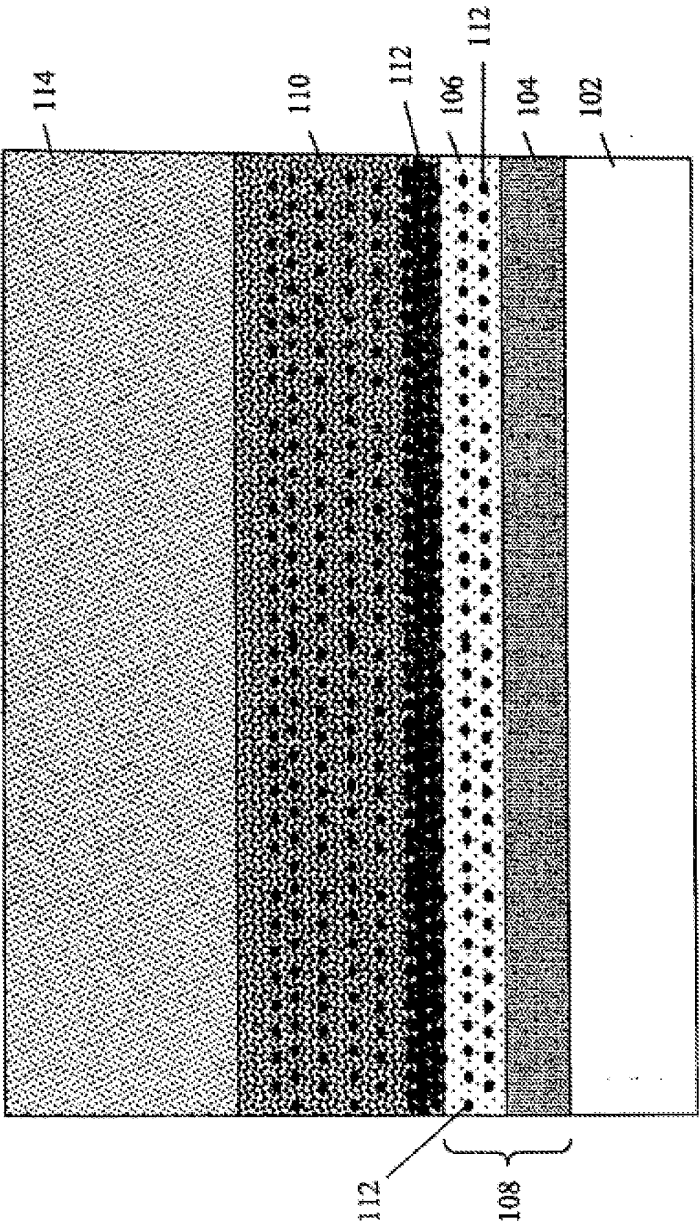


圖 2(d)

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四、指定代表圖：

(一)本案指定代表圖為：圖 1 (f)。

(二)本代表圖之元件符號簡單說明：

102 半導體基板

104 第一介電層

106 缺氮第二介電層

108 介面層

110 高介電常數閘極介電層

112 功函數調整摻雜物物種

114 金屬閘極導體層

五、本案若有化學式時，請揭示最能顯示發明特徵的化學式：無。



Espacenet

Bibliographic data: TW201236153 (A) — 2012-09-01

Structure and method for V_t tuning and short channel control with high k/metal gate MOSFETs

Inventor(s): CAI JIN [CN]; CHEN XIANG-DONG [CN]; WANG XIN-LIN [CN] ±
(CAI, JIN, ; CHEN, XIANG-DONG, ; WANG, XIN-LIN)

Applicant(s): IBM [US] ± (INTERNATIONAL BUSINESS MACHINES CORPORATION)

Classification: - international: H01L21/28; H01L29/78
- cooperative: H01L21/823807; H01L21/823892; H01L29/1041

Application number: TW20110140609 20111107

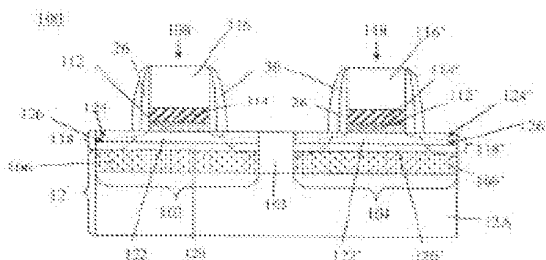
Priority number (s): US20100960589 20101206

Also published as: US2012138953 (A1) US8466473 (B2) WO2012078225 (A1)
JP2013545315 (A) JP2013545315 (A) more

Abstract of TW201236153 (A)

A semiconductor device is provided that includes a semiconductor substrate having a well region located within an upper region thereof. A semiconductor material stack is located on the well region. The semiconductor material stack includes, from bottom to top, a semiconductor-containing buffer layer and a non-doped semiconductor-containing

channel layer; the semiconductor-containing buffer layer of the semiconductor material stack is located directly on an upper surface of the well region. The structure also includes a gate material stack located directly on an upper surface of the non-doped semiconductor-containing channel layer. The gate material stack employed in the present disclosure includes, from bottom to top, a high k gate dielectric layer, a work function metal layer and a polysilicon layer.



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(30)優先權：2010/12/06 美國

12/960,589

(71)申請人：萬國商業機器公司(美國) INTERNATIONAL BUSINESS MACHINES CORPORATION (US)

 Springer

(72)發明人：蔡勁 CAI, JIN (CN)；陳夏冬 CHEN, XIANGDONG (CN)；王新琳 WANG, XINLIN (CN)

(74)代理人：蔡玉玲

每路線圖幅： 每路線比例尺圖幅： 15 張 圖式數： 7 共 36 頁

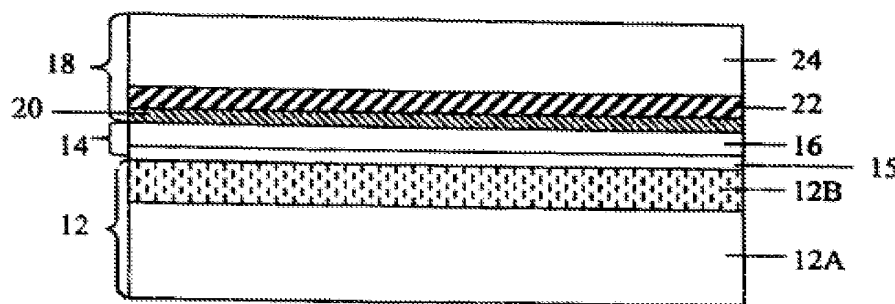
(54) 名 稱

具高介電常數／金屬閘極金氧半導體的 V_{th} 調整與短通道控制的結構與方法

STRUCTURE AND METHOD FOR VT TUNING AND SHORT CHANNEL CONTROL WITH HIGH K/METAL GATE MOSFETS

(57) 樂

提供一種半導體結構，其包含位於其上區域內具有井區之半導體基板。半導體材料堆疊位於井區上。半導體材料堆疊從下到上包括含半導體緩衝層及含無摻雜半導體通道層。半導體材料堆疊之含半導體緩衝層直接位於井區之上表面上。此結構亦包含閘極材料堆疊，直接位於含無摻雜半導體通道層之上表面上。本發明中所用之閘極材料堆疊從下到上包含高介電常數閘極介電層、功函數金屬層及多晶矽層。



12：半導體基板

12A：下區域

12B : 英國

14 : 學藝部部長

15: 含率與機器使用率

16: 含無接雜半導體
製造

18 : 關極材料堆疊

20：高介電常數閘極
介電層

22 : 功過數余履履

24: 4854

(19) 中華民國智慧財產局

(12)發明說明書公開本

(11)公開編號：TW 201236153 A1

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(30)優先權：2010/12/06 美國

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(71)申請人：萬國商業機器公司(美國) INTERNATIONAL BUSINESS MACHINES CORPORATION (US)

 Springer

(72)發明人：蔡勁 CAI, JIN (CN)；陳夏冬 CHEN, XIANGDONG (CN)；王新琳 WANG, XINLIN (CN)

(74)代理人：蔡玉玲

每種線型檢查：漁 每種線型範圍數：15項 圖式數：7 共36頁

(54) 名 稱

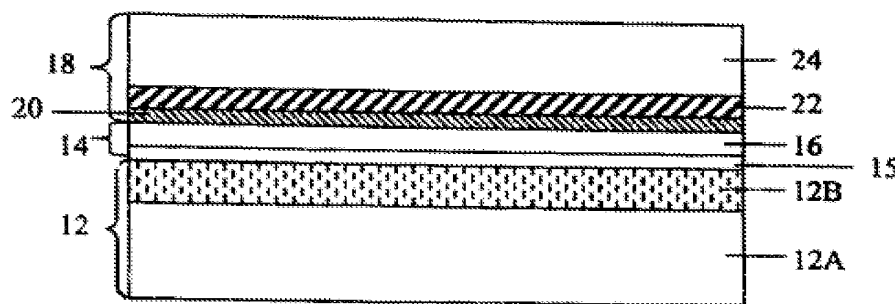
異質介電常數 / 金屬閘極金氧半導體電晶體的 V_t 調整與短通道控制的結構與方法

STRUCTURE AND METHOD FOR VT TUNING AND SHORT CHANNEL CONTROL WITH HIGH K/METAL GATE MOSFETS

(57) 衆

衆 (しゅ)

提供一種半導體結構，其包含位於其上區域內具有井區之半導體基板。半導體材料堆疊位於井區上。半導體材料堆疊從下到上包括含半導體緩衝層及含無摻雜半導體通道層。半導體材料堆疊之含半導體緩衝層直接位於井區之上表面上。此結構亦包含閘極材料堆疊，直接位於含無摻雜半導體通道層之上表面上。本發明中所用之閘極材料堆疊從下到上包含高介電常數閘極介電層、功函數金屬層及多晶矽層。



12: 半導體基板

12A：下區域

12B : 井區

14 : 4 5 6 7 8 9

15: 今年選舉後局

16: 含無接雜半導體
製造

18 : 關機材料検査

20：高介電常數閘極
介電層

22 : 功過數余履履

24: 4 4 4 4

六、發明說明：

【發明所屬之技術領域】

本發明係關於半導體結構以及製造此半導體結構之方法。具體而言，本發明係關於包含在半導體基板上具有高介電常數/金屬閘極堆疊之至少一場效電晶體(FET)的半導體結構，其中該至少一 FET 具有所欲臨界電壓值、改良的短通道控制、改良的反轉載子移動率以及降低的外部電阻。本發明亦提供形成此種半導體結構的方法。

【先前技術】

現代積體電路製造之一趨勢為產生儘可能小的半導體裝置，例如場效電晶體(FETs)。於典型場效電晶體中，藉由佈植 n 型或 p 型雜質於半導體材料中，形成源極與汲極於半導體基板的主動區域中。通道(或本體)區設置在源極與汲極之間。閘極電極設置在本體區上方。閘極電極與本體藉由閘極介電層隔開。

為了持續縮小半導體裝置，已使用高介電常數/金屬閘極堆疊降低有效閘極介電質厚度及閘極漏電流。然而，越高的臨界電壓 V_t (由於不利的金屬閘極功函數)及越高的電容為高效能互補金氧半導體(CMOS)應用的關切事項。上述關切事項在目前沒有可用的穩帶邊緣金屬閘極之 p 型 FETs 中尤其普遍。

【發明內容】

本發明提供一種半導體結構，其包含位在半導體基板上

具有高介電常數/金屬閘極堆疊之至少一場效電晶體。

於本發明中提供的場效電晶體具有所欲的臨界電壓值、改良的短通道控制、改良的反轉載子移動率以及降低的外部電阻。本發明亦提供一種形成此種半導體結構的方法。

舉例而言，於本發明之一實施例中，可利用中間帶隙功函數閘極堆疊、SiGe 通道以及超陡峭後退井(SSRW)達到所欲的 pFET 臨界電壓。具體而言，使用 SiGe 通道(V_t 偏移約 300mV)及 SSRW(V_t 偏移約 200mV，無劣化的短通道效應)，將中間帶隙金屬閘極高介電常數 pFET 之臨界電壓集中。在 SiGe 通道中使臨界電壓集中無需摻雜或逆摻雜，因此降低 V_t 的變異，強化反轉載子移動率以及降低外部電阻。申請人已確定使用中間帶隙功函數閘極堆疊、SiGe 通道以及 SSRW 之組合，可達到的 pFET 之所欲臨界電壓。申請人進一步確定在僅使用中間帶隙功函數閘極堆疊、SiGe 通道以及 SSRW 其中一者的案例中，難以達到 pFET 的所欲臨界電壓。申請人也確定在使用中間帶隙功函數閘極堆疊、SiGe 通道以及 SSRW 其中兩者的案例中，難以達到 pFET 的所欲臨界電壓。本發明中針對 nFET 也可達到類似的成就。

在本發明之一觀點中，半導體結構包含半導體基板，其具有井區位於其上區域內。半導體材料堆疊位於井區上。半導體材料堆疊從下到上包括含半導體緩衝層及含無摻雜半導體通道層，其中半導體材料堆疊之含半導體緩衝層直接位於井區之上表面上。本結構亦包含閘極材料堆疊，直接位於含無摻雜半導體通道層之上表面上。本發明中所用之閘極材

料堆疊從下到上包含高介電常數閘極介電層、功函數金屬層及多晶矽層。

於本發明中，緩衝層對 SiGe 通道 pFET 而言可為無摻雜矽層，或對 Si 通道 nFET 或 SiGe 通道 pFET 而言可為 SiC 層。於 SiC 緩衝層的案例中，其可為摻雜或無摻雜的。緩衝層之目的在於避免/降低雜質原子從井區擴散到含無摻雜半導體通道層。

於本發明之另一實施例中，提供一種半導體結構，其包含半導體基板，於其中具有至少一 pFET 裝置區及之至少一 nFET 裝置區。至少一 pFET 裝置區包含 n 井區位於半導體基板之上區域內、第一半導體材料堆疊從下到上包含第一含半導體緩衝層及第一含無摻雜半導體通道層，其中第一半導體材料堆疊之第一含半導體緩衝層直接位於 n 井區之上表面上、以及 pFET 閘極材料堆疊直接位於第一含無摻雜半導體通道層之上表面上，其中 pFET 閘極材料堆疊從下到上包含第一高介電常數閘極介電層、pFET 功函數金屬層及第一多晶矽層。至少一 nFET 裝置區包含 p 井區位於半導體基板之另一上區域內、第二半導體材料堆疊從下到上包含第二含半導體緩衝層及第二含無摻雜半導體通道層，其中第二半導體材料堆疊之第二含半導體緩衝層直接位於 p 井區之上表面上、以及 nFET 閘極材料堆疊直接位於第二含無摻雜半導體通道層之上表面上，其中 nFET 閘極材料堆疊從下到上包含第二高介電常數閘極介電層、nFET 功函數金屬層及第二多晶矽層。

除了上述結構，本案亦提供一種製造半導體結構之方法。於此所提供的方法包含提供半導體基板，其具有井區位於其上區域內。形成半導體材料堆疊於井區頂上。所形成的半導體材料堆疊從下到上包括含半導體緩衝層及含無摻雜半導體通道層，其中半導體材料堆疊之含半導體緩衝層直接位於井區之上表面上。形成閘極材料堆疊直接於含無摻雜半導體通道層之上表面上。閘極材料堆疊從下到上包含高介電常數閘極介電層、功函數金屬層及多晶矽層。

【實施方式】

現在參考以下討論及本案伴隨圖式詳細說明本發明，其提供一種包括在半導體基板上具有高介電常數/金屬閘極堆疊之至少一場效電晶體(FET)之半導體結構及其製造方法，其中至少一場效電晶體具有所欲的臨界電壓值、改良的短通道控制、改良的反轉載子移動率以及降低的外部電阻。應注意提供的圖式僅為說明目的並未依比例繪示。

於下文說明中，為了說明本發明提出許多特定細節，例如特定的結構、組件、材料、尺寸、製程步驟以及技術。然而，熟此技藝者應知本發明之各種實施例可不以這些特定細節施行或可以其他特定細節施行。於其他實例中，並未詳細說明熟知的結構或製程步驟，以免模糊本發明各種實施例。

應了解當元件為層、區(區域)、或基板且表示在另一元件「之上」或「上方」時，其可直接於另一元件上或可能有中介元件。相對地，當元件表示為「直接在上」或「直接在上方」即無中介元件。亦應了解當元件表示為與另一元件「連

接」或「耦接」，其可直接連接或耦接另一元件，或者可能有中介元件。相對地，當元件表示為與另一元件「直接連接」或「直接耦接」即無中介元件。

參考圖 1，顯示可用於本發明實施例之初始結構 10。圖 1 所示之初始結構 10 包含半導體基板 12，其具有井區 12B 係直接位於半導體基板 12 之上區域內。井區 12B 存在於由半導體材料所組成之半導體基板 12 的下區域 12A 頂上。

可用於本發明中之半導體基板 12(除了井區 12B 的部分)可包含塊體基板、絕緣層上覆半導體(SOI)基板或混合晶向半導體基板。

當使用塊體半導體基板做為半導體基板 12 時，塊體半導體基板由任何半導體材料所組成，其包含但不限於 Si、Ge、SiGe、SiC、SiGeC、InAs、GaAs、InP 或其他像 III/V 族化合物半導體。亦可使用這些半導體材料之多層做為塊體半導體之半導體材料。於一實施例中，塊體半導體基板由 Si 所組成。

當使用 SOI 基板做為半導體基板 12 時，SOI 基板包含處理基板、位在處理基板上表面的埋式絕緣層以及位在埋式絕緣層上表面的半導體層。SOI 基板之處理基板及半導體層可包含相同或不同的半導體材料。於此關於處理基板之半導體材料及半導體層所用的「半導體」一詞意指任何半導體材料，其包含例如 Si、Ge、SiGe、SiC、SiGeC、InAs、GaAs、InP 或其他像 III/V 族化合物半導體。這些半導體材料的多層

亦可用做為處理基板的半導體材料或半導體層。於一實施例中，處理基板及半導體層皆由 Si 所組成。

處理基板及半導體層可具有相同或不同的晶向。舉例而言，處理基板及/或半導體層的晶向可為{100}、{110}或{111}。除了上述具體指明的晶向，本發明也可使用其他晶向。SOI 基板之處理基板及/或半導體層可為單晶半導體材料、多晶材料或非晶材料。典型地，至少半導體層是單晶半導體材料。

SOI 基板之埋式絕緣層可為結晶或無結晶氧化物或氮化物。於一實施例，埋式絕緣層為氧化物。埋式絕緣層可為連續的或不連續的。當存在不連續的埋式絕緣區時，絕緣區為由半導體材料所包圍之孤島方式存在。

SOI 基板可利用標準製程形成，其包含例如 SIMOX (氧離子佈植分離)或層轉移。當使用層轉移製程時，選擇性薄化步驟可跟隨在兩個半導體晶圓接合之後。選擇性薄化步驟將半導體層的厚度降低到具有更希望得到之厚度的層。

SOI 基板之半導體層厚度典型從 100Å 至 1000Å，更典型為 500Å 至 700Å。若半導體層的厚度不在上述其中之一範圍內，可使用例如平坦化或蝕刻之薄化步驟以降低半導體層的厚度到在上述其中之一範圍內的值。

SOI 基板之埋式絕緣層典型具有從 10Å 至 2000Å 的厚度，更典型為從 1000Å 至 1500Å 的厚度。SOI 基板之處理

基板的厚度對本發明不重要。

在某些實施例中，使用不同表面區域具有不同晶向之混合半導體基板做為半導體基板 12。當使用混合基板時，nFET 典型形成在(100)晶面，而 pFET 典型形成在(110)晶面。混合基板可藉由本領域熟知的技術形成。例如參見美國專利 7,329,923 號、2005 年 6 月 2 日公開之美國專利申請案 2005/0116290 號以及美國專利 7,023,055 號，各整體內容併入於此做為參考。

在選擇要使用的基板類型後，形成井區 12B 於半導體基板 12 之上區域中。井區 12B 可藉由離子佈植、氣相摻雜以及從形成於基板上且於外擴散程序後移除之包含摻雜質的犧牲層進行外擴散其中之一方法所形成。於一實施例中，使用離子佈植形成井區。

本發明中所形成的井區 12B 可包含 n 型摻雜質(即元素週期表中 VA 族之元素，例如 P 及 As)或 p 型摻雜質(即元素週期表中 IIIA 族之元素，例如 B、Al 及 In)。存在於井區 12B 之摻雜質種類取決於其上要形成的裝置類型。舉例而言，當形成 pFET 裝置於井區 12B 上方時，n 型摻雜質併入於半導體基板 12 的上區域中。於另一實例中，當形成 nFET 裝置於井區 12B 上方時，p 型摻雜質併入於半導體基板 12 的上區域中。

形成於半導體基板 12 之上區域內的井區 12B 具有 1×10^{18} 原子/cm³ 或更高的摻雜濃度。更具體而言，形成於半導

體基板 12 之上區域內的井區 12B 具有 5×10^{18} 原子/cm³ 至 2×10^{19} 原子/cm³ 的摻雜濃度。在本發明某些實施例中，可在井區佈植後進行退火程序，以在成長含半導體緩衝層及含無摻雜半導體通道層之磊晶製程前修復晶格破損。

在本發明某些實施例中，可於此製程階段或在形成井區前，形成隔離區於半導體基板 12 中。於本發明另一實施例中，可在形成半導體材料堆疊於基板 12 頂上後形成隔離區於結構中。後者方案可得到較佳的半導體材料堆疊品質，因為半導體材料堆疊是磊晶成長在未受隔離區中斷的均勻井區上。為簡明之故，本發明之圖 1 至圖 6 中並未顯示至少一隔離區。

當形成隔離區時，至少一隔離區可為溝渠隔離區或場氧化隔離區。溝渠隔離區可利用熟此技藝者所熟知的傳統溝渠隔離製程所形成。舉例而言，微影、蝕刻以及利用例如氧化物之介電質填充溝渠，可用於形成溝渠隔離區。選擇性地，在填充溝渠前可形成襯層於溝渠中，在溝渠填充後可執行緻密化程序，也可在溝渠填充後進行平坦化程序。場氧化隔離區可利用所謂局部矽氧化製程所形成。應注意至少一隔離區提供相鄰閘極區之間的隔離，當相鄰閘極具有相反導電性（例如 nFET 及 pFET）時通常有此需要。如此一來，至少一隔離區將 nFET 裝置區及 pFET 裝置區分開。圖 7 顯示其中包含隔離區 103 的結構，於下文中之詳述。

參考圖 2，顯示圖 1 之結構在形成半導體材料堆疊 14 於半導體基板 12 之井區 12B 頂上後之圖式。半導體材料堆

疊 14 從下到上包括含半導體緩衝層 15 及含無摻雜半導體通道層 16。如圖所示，含半導體緩衝層 15 位於井區 12B 之上表面上且直接接觸井區 12B 之上表面，而含無摻雜半導體通道層 16 位於含半導體緩衝層 15 之上表面上且直接接觸含半導體緩衝層 15 之上表面。

由於半導體材料堆疊由含無摻雜半導體通道層 16 所組成且井區 12B 為重度摻雜，所以上述的井區 12B 可表示為超陡峭後退井(SSRW)，因為有著在井區 12B 中摻雜質濃度很高而在含無摻雜半導體通道層 16 中減少到低摻雜質濃度的摻雜質輪廓。再者，摻雜質濃的變化在薄含半導體緩衝層非常陡峭。就「陡峭」一詞係指陡峭度大於每十倍為 5nm 的摻雜質梯度。

所使用的含半導體緩衝層 15 係為任何阻礙摻雜質從井區 12B 擴散到含無摻雜半導體通道層 16 的半導體材料。如此一來，含半導體緩衝層 15 於此也可稱為摻雜質擴散阻障層，即含半導體阻障層。因此，所用的半導體材料種類隨著井區 12B 中存在的摻雜質種類(即 n 型摻雜質或 p 型摻雜質)改變。

於一實施例中，當要形成 pFET 裝置且井區 12B 包含 n 型摻雜質(例如砷)，可使用無摻雜矽(Si)做為含半導體緩衝層 15。於另一實施例中，當要形成 nFET 裝置且井區 12B 包含 p 型摻雜質(例如硼)，可使用碳化矽(SiC)做為含半導體緩衝層 15。SiC 緩衝層可以 p 型摻雜質摻雜或無摻雜。於一實施例中，p 型摻雜質可於磊晶成長程序期間原位導入緩衝

層。於另一實施例中，p 型摻雜質可在磊晶成長含半導體緩衝層 15 後利用熟此技藝者所熟知的技術(例如離子佈植及/或氣相摻雜)導入。SiC 緩衝層內的 p 型摻雜質濃度典型為 $5E18$ 原子/cm³ 至 $2E19$ 原子/cm³。

在使用 SiC 做為含半導體緩衝層 15 之實施例中，在碳化矽合金中的碳原子濃度可為在 0.1%及 5%之間的固定數值，典型為 0.5%及 2%之間。選替地，碳化矽合金中的碳原子濃度在垂直方向上可漸變。

含半導體緩衝層 15 係利用任何傳統磊晶成長程序所形成，其中可使用任何熟知的含半導體前驅劑。由於使用磊晶法形成含半導體緩衝層 15，所以層 15 為具有與下方基板 12 相同晶向的單晶半導體材料。含半導體緩衝層 15 的厚度典型為 2 nm 至 20 nm，更典型為 5 nm 至 10 nm 的厚度。只要含半導體緩衝層 15 保持阻礙摻雜質從井區 12B 擴散到含無摻雜半導體通道層 16 的能力，亦可使用其他厚度。

所用的含無摻雜半導體通道層 16 為任何可用做為裝置通道並有助於調整所要形成裝置之臨界電壓的半導體材料。因此，可變化含無摻雜半導體通道層 16 所用的半導體材料種類。於一實施例中，當要形成 pFET 裝置時，矽鍺(SiGe)合金可用做為含無摻雜半導體通道層 16。於另一實施例中，當要形成 nFET 裝置時，矽(Si)可用做為含無摻雜半導體通道層 16。

含無摻雜半導體通道層 16 係利用任何傳統磊晶成長程

序所形成，其中可使用任何熟知的含半導體前驅劑。由於使用磊晶法形成含無摻雜半導體通道層 16，所以層 16 為具有與下方基板 12 相同晶向的單晶半導體材料。含無摻雜半導體通道層 16 的厚度典型為 2 nm 至 20 nm，更典型為 5 nm 至 10 nm 的厚度。於本發明中亦可使用其他厚度。

在使用 SiGe 做為含無摻雜半導體通道層 16 的實施例中，在矽鍺合金中的鍺原子濃度可為在 20%及 50%之間的固定數值，典型為 30%及 40%之間。選替地，矽鍺合金中的鍺原子濃度在垂直方向上可漸變。舉例而言，矽鍺合金中的鍺原子濃度可隨著與含半導體緩衝層 15 及矽鍺合金間之界面的距離逐漸增加，達到可包含或不包含平高區之高峰，然後一旦距離增加到超過高峰及/或平高區就隨著與含半導體緩衝層 15 及矽鍺合金間之界面的距離而減少。選擇厚度及鍺原子濃度輪廓(不論鍺原子濃度輪廓為固定或漸變的)，使得含無摻雜半導體通道層 16 整體維持單晶，且應變鬆弛造成的缺陷密度是在可忽略的程度，即不夠明顯到足以對半導體材料堆疊 14 中(尤其是含無摻雜半導體通道層 16 中)之電荷載子移動率有不利的影響。

參考圖 3，顯示圖 2 之結構在形成閘極材料堆疊 18 於半導體材料堆疊 14 之上表面上(即含無摻雜半導體通道層 16 頂上)後之圖式。閘極材料堆疊 18 從下到上包含高介電常數閘極介電層 20、功函數金屬層 22 及多晶矽層 24。

閘極材料堆疊 18 之高介電常數閘極介電層 20 包含任何介電常數大於氧化矽之介電常數(例如 3.9)的介電材料。典型

地，高介電常數閘極介電層 20 具有大於 4.0 的介電常數，更典型為大於 8.0 的介電常數。可用做為高介電常數閘極介電層 20 之例示高介電常數材料包含但不限於 HfO_2 、 ZrO_2 、 La_2O_3 、 Al_2O_3 、 TiO_2 、 SrTiO_3 、 LaAlO_3 、 Y_2O_3 、 HfO_xN_y 、 ZrO_xN_y 、 $\text{La}_2\text{O}_x\text{N}_y$ 、 $\text{Al}_2\text{O}_x\text{N}_y$ 、 TiO_xN_y 、 SrTiO_xN_y 、 LaAlO_xN_y 、 $\text{Y}_2\text{O}_x\text{N}_y$ 、其矽酸鹽類及其合金。於一實施例中，使用含 Hf 的高介電材料(例如 HfO_2)做為高介電常數閘極介電層 20。亦可使用這些高介電常數材料之多層堆疊做為高介電常數閘極介電層 20。各 x 的值獨立為 0.5 至 3，且各 y 的值獨立為 0 至 2。

高介電常數閘極介電層 20 的厚度可依據所形成的技術改變。然而，高介電常數閘極介電層 20 典型具有 0.5 nm 至 10 nm 的厚度，更典型為 1.0 nm 至 5 nm 的厚度。所使用的高介電常數閘極介電層 20 可具有 1 nm 等級或更小的有效氧化物厚度。

高介電常數閘極介電層 20 可藉由本領域熟知的技術所形成，包含例如化學氣相沉積(CVD)、物理氣相沉積(PVD)、分子束沉積(MBD)、脈衝式雷射沉積(PLD)、液相源霧狀化學沉積(LSMCD)、原子層沉積(ALD)及其他類似的沉積製程。

功函數金屬層 22 包含具有功函數的金屬。選擇功函數金屬層 22 的金屬，以最佳化後續要形成之電晶體的效能。於一實施例中，功函數金屬層 22 包含矽價帶邊緣金屬，例如 Pt、Rh、Ir、Ru、Cu、Os、Be、Co、Pd、Te、Cr、Ni、TiN 及其合金。矽價帶邊緣金屬為具有功函數較接近對應矽

價帶邊緣之功函數(例如 5.10 eV)且較不接近對應矽導帶邊緣之功函數(例如 4.00 eV)之金屬。因此，矽價帶邊緣金屬具有大於 4.55 eV 之功函數。舉例而言，功函數金屬層 22 可為 TiN 層。此類功函數金屬典型適合用於 pFET 裝置。

於另一實施例中，功函數金屬層 22 包含矽導帶邊緣金屬，例如 Hf、Ti、Zr、Cd、La、Tl、Yb、Al、Ce、Eu、Li、Pb、Tb、Bi、In、Lu、Nb、Sm、V、Zr、Ga、Mg、Gd、Y、TiAl 及其合金。矽導帶邊緣金屬為具有功函數較接近對應矽導帶邊緣之功函數且較不接近對應矽價帶邊緣之功函數之金屬。因此，矽導帶邊緣金屬具有小於 4.55 eV 之功函數。舉例而言，功函數金屬層 22 可為 TiAl 層。此類功函數金屬典型適合用於 nFET 裝置。

功函數金屬層 22 可藉由例如物理氣相沉積、化學氣相沉積或原子層沉積(ALD)所形成。典型地，功函數金屬層 22 的厚度為 1 nm 至 30 nm，更典型為 2 nm 至 10 nm 的厚度。

多晶矽層 24 可利用任何傳統沉積製程所形成，包含如化學氣相沉積、電漿強化化學氣相沉積、化學溶液沉積以及蒸鍍。多晶矽層 24 於其沉積程序期間可進行原位摻雜。選替地，可在沉積多晶矽層後藉由離子佈植或氣相摻雜將摻雜質導入多晶矽層。多晶矽層 24 的厚度可依據其用於形成的技術變化。典型地，多晶矽層 24 具有 10 nm 至 100 nm 的厚度，更典型為 20 nm 至 50 nm 的厚度。

參考圖 4，顯示圖 3 之結構在圖案化閘極材料堆疊 18

以提供至少一圖案化閘極堆疊 18' (分別包含圖案化高介電常數閘極介電層 20', 圖案化功函數金屬層 22', 圖案化多晶矽層 24') 於半導體材料堆疊 14 後之圖式。雖然圖中顯示形成單一圖案化閘極堆疊, 但是形成複數圖案化閘極堆疊時亦可使用本發明。

閘極材料堆疊 18 的圖案化包含微影及蝕刻。微影步驟包含首先提供光阻於閘極材料堆疊 18 的頂上, 即多晶矽層 24 頂上。光阻可包含正型光阻材料、負型光阻材料或混合光阻材料, 其各為熟此技藝者所熟知的。光阻可利用任何傳統光阻沉積程序所形成, 例如旋轉塗佈、噴塗或蒸鍍。在塗佈光阻於閘極材料堆疊 18 的上表面上後, 光阻曝光於所需圖案的輻射, 之後利用傳統光阻顯影劑顯影曝光後的光阻。如此在閘極材料堆疊 18 上得到圖案化的光阻(未顯示)。圖案化的光阻保護某些下方部分的閘極材料堆疊 18, 同時暴露出其他下方部分的閘極材料堆疊 18。然後可利用乾蝕刻、濕蝕刻或其組合蝕刻下方閘極材料堆疊 18 之暴露部分。乾蝕刻包含反應式離子蝕刻、電漿蝕刻、離子束蝕刻或雷射消融。濕蝕刻包含選擇性移除閘極材料堆疊 18 之至少一層的化學蝕刻劑。在將圖案轉移到閘極材料堆疊 18 之一層後, 隨時可利用傳統光阻移除製程(例如灰化)移除圖案化光阻。還替地, 在移除閘極材料堆疊 18 之暴露部分時, 圖案化光阻可保持在閘極材料堆疊上, 且在完成移除閘極材料堆疊 18 之暴露部分後藉由傳統光阻移除製程(例如灰化)移除。蝕刻可包含單蝕刻或多蝕刻程序, 且停在半導體材料堆疊 14 的上表面。

參考圖 5，顯示圖 4 之結構在至少一閘極堆疊 18' 之側壁上形成內間隙壁 26 後以及在半導體材料堆疊 14 中形成延伸區 28 後之圖式。在某些實施例中，結構中省略了內間隙壁 26。當內間隙壁 26 存在時，內間隙壁 26 可由包含例如氧化物、氮化物、氮氧化物及其多層之介電材料所組成。於一實施例中，內間隙壁 26 由氧化物所組成，例如氧化矽。於另一實施例中，內間隙壁 26 由氮化物所組成，例如氮化矽。內間隙壁 26 可藉由沉積介電層然後蝕刻所形成。選替地，內間隙壁 26 可藉由熱製程所形成，例如氧化或氮化。在某些實施例中，可使用前述製程的組合形成內間隙壁 26。內間隙壁 26 具有由基部量測的寬度，其典型為 3 nm 至 20 nm，更典型為 5 nm 至 10 nm 的寬度。

延伸區 28 於此亦可稱為源極/汲極延伸區，其可以至少一圖案化閘極堆疊 18' 及選擇性的內間隙壁 26 做為離子佈植遮罩，利用任何已知的延伸離子佈植所形成。如此一來，延伸區 28 形成於各圖案化閘極堆疊 18' 的足印。在延伸離子佈植後，可使用退火活化植入的延伸離子。在某些實施例中，延伸區 28 的活化可延遲到源極/汲極區 32 形成後。延伸區 28 的深度可依據所使用的離子佈植及活化退火條件而異。典型地，形成於半導體材料堆疊 14 中之延伸區 28 從半導體材料堆疊 14 之上表面量起有 5 nm 至 20 nm 的深度。

參考圖 6，顯示圖 5 之結構在形成外間隙壁 30 後及在半導體材料堆疊 14 中形成源極區與汲極區(於此通稱源極/汲極區 32)後之圖式。

如圖 6 所示，在某些實施例中，外間隙壁 30 可形成鄰接內間隙壁 26。在其他實施例中，外間隙壁 30 可形成於各閘極堆疊 18' 之側壁上。外間隙壁 30 可由包含例如氧化物、氮化物、氮氧化物及其多層之介電材料所組成。於一實施例中，外間隙壁 30 由氧化物所組成，例如氧化矽。於另一實施例中，外間隙壁 30 由氮化物所組成，例如氮化矽。外間隙壁 30 典型由不同於內間隙壁 26 的材料所組成，但並非絕對。外間隙壁 30 可藉由沉積介電層然後蝕刻所形成。選替地，外間隙壁 30 可藉由熱製程所形成，例如氧化或氮化。在某些實施例中，可使用前述製程的組合形成外間隙壁 30。外間隙壁 30 典型由基部量測具有大於內間隙壁 26 之寬度的寬度。典型地，外間隙壁 30 具有 10 nm 至 50 nm 的寬度，更典型為 15 nm 至 30 nm 的寬度。

源極/汲極區 32 可以至少圖案化閘極堆疊 18'、選擇性的內間隙壁 26 及外間隙壁 30 作為離子佈植遮罩，利用任何已知的源極/汲極離子佈植程序所形成。如此一來，源極/汲極區 32 也形成於各圖案化閘極堆疊 18' 的足印。在源極/汲極離子佈植後，可使用退火活化植入的摻雜質離子。源極/汲極區 32 的深度比延伸區 28 還要深得多，且可依據所使用的離子佈植及活化退火條件而異。典型地，源極/汲極區 32 形成於半導體材料堆疊 14 且典型於井區 12B 之上部內。源極/汲極區 32 從半導體材料堆疊 14 之上表面量起有 20 nm 至 100 nm 的深度。

在某些實施例中，現在可利用任何能形成金屬半導體合金於半導體材料堆疊 14 頂上之製程形成金屬半導體合金接

觸。於一實施例中，金屬半導體合金接觸可利用矽化製程所形成。矽化製程可自行對準外間隙壁 30 的外緣。矽化製程包含形成與半導體材料反應時能形成金屬半導體合金的金屬。用於形成金屬半導體合金接觸的金屬包含但不限於鉭、鈦、鎢、鈹、鈷、鎳或這些材料的任何合適組合。在金屬頂上可形成例如氮化鈦或氮化鉭之擴散阻障層。執行退火，在金屬與下方半導體材料間造成反應，而形成金屬半導體合金區。典型地，在至少 250°C 或以上的溫度執行退火。可使用單退火步驟或多重退火步驟。在執行退火後，移除任何未反應的金屬及選擇性的擴散阻障層。在某些實施例中，於本發明此步驟期間，金屬半導體合金接觸可直接形成於圖案化閘極堆疊 18' 頂上。

在本發明的某些實施例中，可使用上述製程步驟以及傳統阻擋遮罩技術形成 CMOS 結構 100，例如圖 7 所示。圖 7 所示的結構 100 包含半導體基板 12，其具有藉由隔離區 103 分開的至少一 pFET 裝置區 102 及至少一 nFET 裝置區 104。半導體基板 12 包含由半導體材料組成的下區域 12A 以及上井區。在至少一 pFET 裝置區 102 內的井區標示為 106，而在至少一 nFET 裝置區 104 內的井區標示為 106'。井區 106、106' 利用上述井區 12B 之方法製造。應注意在至少一 pFET 裝置區 102 內的井區 106 包含 n 型摻雜質，而在至少一 nFET 裝置區 104 內的井區 106' 包含 p 型摻雜質。可利用阻擋遮罩在選擇性擋住其中一個裝置區時形成另一個裝置區的井區，而形成不同導電性的井區 106、106'。

圖 7 所示之結構 100 也包含位於至少一 pFET 裝置區 102

內的至少一 pFET 108 以及位於位於至少一 nFET 裝置區 104 內的至少一 nFET 110。

各 FET(即 pFET 108 及 nFET 110)包含高介電常數閘極介電層(標示為 112 及 112')、功函數金屬層(標示為 114 及 114') 以及多晶矽層(標示為 116 及 116')。至少一 pFET 108 之高介電常數閘極介電層 112 可與至少一 nFET 110 之高介電常數閘極介電層 112'相同或不同。可使用阻擋遮罩技術達到不同高介電常數閘極介電層。高介電常數閘極介電層 112、112'可包含上述高介電常數閘極介電層 20 其中之一高介電常數材料。再者，高介電常數閘極介電層 112、112'可由上述高介電常數閘極介電層 20 之方式製成並具有上述高介電常數閘極介電層 20 之厚度。

在至少一 pFET 108 中所含的功函數金屬層 114 包含上述適合用於 pFET 裝置之功函數金屬層 22 其中之一功函數金屬。類似地，在至少一 nFET 110 中所含的功函數金屬層 114'包含上述適合用於 nFET 裝置之功函數金屬層 22 其中之一功函數金屬。功函數金屬層 114 及 114'可使用上述形成功函數金屬層 22 其中之一製程所形成。再者，功函數金屬層 114、114'可具有在上述功函數金屬層 22 厚度範圍內的厚度。再者，可使用阻擋遮罩技術形成功函數金屬層 114、114'。

多晶矽層 116、116'可由上述多晶矽層 24 的方式製成，且具有上述多晶矽層 24 的厚度。多晶矽層 16 在所存在的摻雜質種類方面可與多晶矽層 16'相同或不同。舉例而言，多晶矽層 116 典型包含 p 型摻雜質，而多晶矽層 116'典型包含

n 型摻雜質。再者，可使用阻擋遮罩技術形成多晶矽層 116、116'。於其他實施例中，多晶矽層 116 及 116'皆可以 p 型摻雜質或 n 型摻雜質進行摻雜。

圖 7 所示之各 FET 亦包含內間隙壁 26 及外間隙壁 30，其係如上述方式製成且包含上述材料。

至少一 pFET 108 位在半導體材料堆疊 118 上，而至少一 nFET 110 位在半導體材料堆疊 118'上。半導體材料堆疊 118 從下到上包括含無摻雜半導體(典型為 Si)緩衝層 120 及含無摻雜半導體(典型為 SiGe 合金)通道層 122。半導體材料堆疊 118'從下到上包括含無摻雜或摻雜的半導體(典型為 SiC)緩衝層 120'及含無摻雜半導體(典型為 Si)通道層 122'。半導體材料堆疊 118、118'可使用上述關於半導體材料堆疊 14 之相同技術所製成。

圖 7 所示之結構亦包含源極/汲極延伸區 124、124'以及源極/汲極區 126/126'，其係使用上述形成源極/汲極延伸區 28 及源極/汲極區 32 相同的技術所形成。可針對要製造的裝置類型適當地摻雜源極/汲極延伸區 124/124'以及源極/汲極區 126/126'。

雖然本發明已特別顯示及說明各種實施例，但是熟此技藝者當知在不悖離本發明精神與範疇下在形式及細節上可有前述及其他變化。因此，本發明不限於所述或所示的確實形式及細節，而以落入所附申請專利範圍為準。

【圖式簡單說明】

圖 1 為顯示包含半導體基板之初始結構之截面示意圖，其中在半導體基板之上區域內具有井區。

圖 2 為顯示圖 1 之初始結構在形成半導體材料堆疊後之截面示意圖，其中半導體材料堆疊從下到上包括含半導體緩衝層及含無摻雜半導體通道層直接位於半導體基板之井區頂上。

圖 3 為顯示圖 2 之結構在形成閘極材料堆疊於半導體材料堆疊之上表面上後之截面示意圖。

圖 4 為顯示圖 3 之結構在圖案化閘極材料堆疊以提供至少一圖案化閘極堆疊於半導體材料堆疊上後之截面示意圖。

圖 5 為顯示圖 4 之結構在至少一圖案化閘極堆疊上形成內間隙壁後及在半導體材料堆疊中形成延伸區後之截面示意圖。

圖 6 為顯示圖 5 之結構在形成外間隙壁後及在半導體材料堆疊中與井區上部形成源極區及汲極區後之截面示意圖。

圖 7 為顯示可利用圖 1 至圖 6 所述之基本製程步驟及阻擋遮罩技術所形成的 CMOS 結構之截面示意圖。

【主要元件符號說明】

10 初始結構

12 半導體基板

12A 下區域

12B 井區

14 半導體材料堆疊

15 含半導體緩衝層

- 16 含無摻雜半導體通道層
- 18 閘極材料堆疊
- 18' 圖案化閘極堆疊
- 20、20' 高介電常數閘極介電層
- 22、22' 功函數金屬層
- 24、24' 多晶矽層
- 26 內間隙壁
- 28 延伸區
- 30 外間隙壁
- 32 源極/汲極區
- 100 CMOS 結構
- 102 pFET 裝置區
- 103 隔離區
- 104 nFET 裝置區
- 106 井區
- 106' 井區
- 108 pFET
- 110 nFET
- 112、112' 高介電常數閘極介電層
- 114、114' 功函數金屬層
- 116、116' 多晶矽層
- 118、118' 半導體材料堆疊
- 120 含無摻雜半導體緩衝層
- 120' 含無摻雜或摻雜的半導體緩衝層

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122 含無摻雜半導體通道層

122' 含無摻雜半導體通道層

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發明專利說明書

(本說明書格式、順序，請勿任意更動。※記號部分請勿填寫)

※申請案號：100140609

※申請日：100年11月07日

※IPC分類 H01L 29/78 (2006.01)

一、發明名稱：(中文/英文)

H01L 21/28 (2006.01)

具高介電常數/金屬閘極金氧半場效電晶體的 V_t 調整與短通道控制的結構與方法

STRUCTURE AND METHOD FOR V_t TUNING AND SHORT CHANNEL CONTROL WITH HIGH K/METAL GATE MOSFETs

二、中文發明摘要：

提供一種半導體結構，其包含位於其上區域內具有井區之半導體基板。半導體材料堆疊位於井區上。半導體材料堆疊從下到上包括含半導體緩衝層及含無摻雜半導體通道層。半導體材料堆疊之含半導體緩衝層直接位於井區之上表面上。此結構亦包含閘極材料堆疊，直接位於含無摻雜半導體通道層之上表面上。本發明中所用之閘極材料堆疊從下到上包含高介電常數閘極介電層、功函數金屬層及多晶矽層。

三、英文發明摘要：

A semiconductor device is provided that includes a semiconductor substrate having a well region located within an upper region thereof. A semiconductor material stack is located on the well region. The semiconductor material stack includes, from bottom to top, a semiconductor-containing buffer layer and a

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non-doped semiconductor-containing channel layer; the semiconductor-containing buffer layer of the semiconductor material stack is located directly on an upper surface of the well region. The structure also includes a gate material stack located directly on an upper surface of the non-doped semiconductor-containing channel layer. The gate material stack employed in the present disclosure includes, from bottom to top, a high k gate dielectric layer, a work function metal layer and a polysilicon layer.

七、申請專利範圍：

1. 一種半導體結構，包含：

一半導體基板，具有一井區位於其一上區域內；

一半導體材料堆疊，從下到上包含一含半導體緩衝層及一含無摻雜半導體通道層，其中該半導體材料堆疊之該含半導體緩衝層直接位於該井區之一上表面上；以及

一閘極材料堆疊，直接位於該含無摻雜半導體通道層之一上表面上，其中該閘極材料堆疊從下到上包含一高介電常數閘極介電層、一功函數金屬層及一多晶矽層。

2. 如申請專利範圍第 1 項所述之半導體結構，其中該井區包含 n 型摻雜質並具有 5×10^{18} 原子/cm³ 或更大的摻雜質濃度，且其中該含半導體緩衝層包含無摻雜 Si，且該含無摻雜半導體通道層包含 SiGe 合金。

3. 如申請專利範圍第 2 項所述之半導體結構，其中該功函數金屬層為包含一矽價帶邊緣金屬之一 pFET 功函數金屬層，且其中該矽價帶邊緣金屬包含 Pt、Rh、Ir、Ru、Cu、Os、Be、Co、Pd、Te、Cr、Ni、TiN 或其合金。

4. 如申請專利範圍第 1 項所述之半導體結構，

其中該井區包含 p 型摻雜質並具有 5×10^{18} 原子/cm³ 或更大的摻雜質濃度；

其中該含半導體緩衝層包含無摻雜或 p 型摻雜的 SiC，且該含無摻雜半導體通道層包含 Si；

其中該功函數金屬層為包含一矽導帶邊緣金屬之一 nFET 功函數金屬層，且其中該矽導帶邊緣金屬包含 Hf、Ti、Zr、Cd、La、Tl、Yb、Al、Ce、Eu、Li、Pb、Tb、Bi、In、Lu、Nb、Sm、V、Zr、Ga、Mg、Gd、TiAl 或其合金。

5. 一種半導體結構，包含：

一半導體基板，具有至少一 pFET 裝置區及至少一 nFET 裝置區位於其中；

其中該至少一 pFET 裝置區包含一 n 井區位於該半導體基板之一上區域內、一第一半導體材料堆疊，其從下到上包含一第一含無摻雜半導體緩衝層及一第一含無摻雜半導體通道層，其中該第一半導體材料堆疊之該第一含無摻雜半導體緩衝層直接位於該 n 井區之一上表面上、以及一 pFET 閘極材料堆疊直接位於該第一含無摻雜半導體通道層之一上表面上，其中該 pFET 閘極材料堆疊從下到上包含一第一高介電常數閘極介電層、一 pFET 功函數金屬層及一第一多晶矽層；以及

其中該至少一 nFET 裝置區包含一 p 井區位於該半導體基板之另一上區域內、一第二半導體材料堆疊，其從下到上包含一第二含半導體緩衝層及一第二含無摻雜半導體通道層，其中該第二半導體材料堆疊之該第二含半導體緩衝層直接位於該 p 井區之一上表面上、以及一 nFET 閘極材料堆疊直接位於該第二含無摻雜半導體通道層之一上表面上，其中該 nFET 閘極材料堆疊從下到上包含一第二高介電常數閘極介電層、一 nFET 功函數金屬層及一第二多晶矽層。

6. 如申請專利範圍第 5 項所述之半導體結構，其中該 n 井

區包含 n 型摻雜質並具有 5×10^{18} 原子/cm³ 或更大的摻雜質濃度，且該 p 井區包含 p 型摻雜質並具有 5×10^{18} 原子/cm³ 或更大的摻雜質濃度。

7. 如申請專利範圍第 5 項所述之半導體結構，其中該第一含無摻雜半導體緩衝層包含 Si，且該第一含無摻雜半導體通道層包含 SiGe 合金。

8. 如申請專利範圍第 5 項所述之半導體結構，

其中該 pFET 功函數金屬層包含一矽價帶邊緣金屬，以及

其中該矽價帶邊緣金屬包含 Pt、Rh、Ir、Ru、Cu、Os、Be、Co、Pd、Te、Cr、Ni、TiN 或其合金。

9. 如申請專利範圍第 5 項所述之半導體結構，其中該第二含半導體緩衝層包含無摻雜或 p 型摻雜的 SiC，且該第二含無摻雜半導體通道層包含 Si。

10. 如申請專利範圍第 5 項所述之半導體結構，

其中該 nFET 功函數金屬層包含一矽導帶邊緣金屬，以及

其中該矽導帶邊緣金屬包含 Hf、Ti、Zr、Cd、La、Tl、Yb、Al、Ce、Eu、Li、Pb、Tb、Bi、In、Lu、Nb、Sm、V、Zr、Ga、Mg、Gd、TiAl 或其合金。

11. 一種製造一半導體結構之方法，包含：

提供一半導體基板，具有一井區位於其一上區域內；

形成一半導體材料堆疊於該井區頂上，其中該半導體材料堆疊從下到上包含一含半導體緩衝層及一含無摻雜半導體通道層，其中該半導體材料堆疊之該含半導體緩衝層直接位於該井區之一上表面上；以及

形成一閘極材料堆疊直接於該含無摻雜半導體通道層之一上表面上，其中該閘極材料堆疊從下到上包含一高介電常數閘極介電層、一功函數金屬層及一多晶矽層。

12. 如申請專利範圍第 11 項所述之方法，其中該井區藉由導入濃度大於 5×10^{19} 原子/cm³ 的 n 型摻雜質於該基板之該上區域內而形成。

13. 如申請專利範圍第 12 項所述之方法，

其中形成該半導體材料堆疊之步驟包含磊晶成長一無摻雜 Si 層做為該含半導體緩衝層，以及磊晶成長一 SiGe 合金層做為該含無摻雜半導體通道層，以及

其中形成該閘極材料堆疊之步驟包含選擇並沉積一 pFET 功函數金屬層做為該功函數金屬層，其中該 pFET 功函數金屬層為一矽價帶邊緣金屬。

14. 如申請專利範圍第 11 項所述之方法，

其中該井區藉由導入濃度大於 5×10^{18} 原子/cm³ 的 p 型摻雜質於該基板之該上區域內而形成，

其中形成該半導體材料堆疊之步驟包含磊晶成長一無摻雜或 p 型摻雜 SiC 層做為該含半導體緩衝層，以及磊晶成

長一 Si 層做為該含無摻雜半導體通道層，以及

其中形成該閘極材料堆疊之步驟包含選擇並沉積一 nFET 功函數金屬層做為該功函數金屬層，其中該 nFET 功函數金屬層為一矽導帶邊緣金屬。

15. 如申請專利範圍第 12 項所述之方法，更包含：

提供另一井區位於該半導體基板之一上區域內；

形成另一半導體材料堆疊於該另一井區頂上，其中該另一半導體材料堆疊從下到上包含另一含半導體緩衝層及另一含無摻雜半導體通道層，其中該另一半導體材料堆疊之該另一含半導體緩衝層直接位於該另一井區之一上表面上；以及

形成另一閘極材料堆疊直接於該另一含無摻雜半導體通道層之一上表面上，其中該另一閘極材料堆疊從下到上包含另一高介電常數閘極介電層、另一功函數金屬層及另一多晶矽層。

八、圖式：

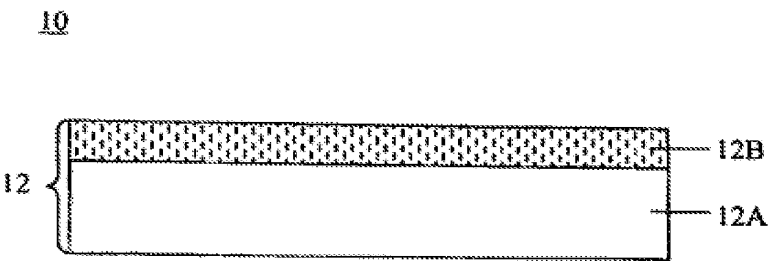


圖 1

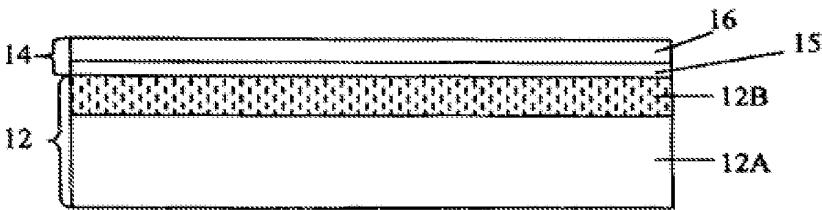


圖 2

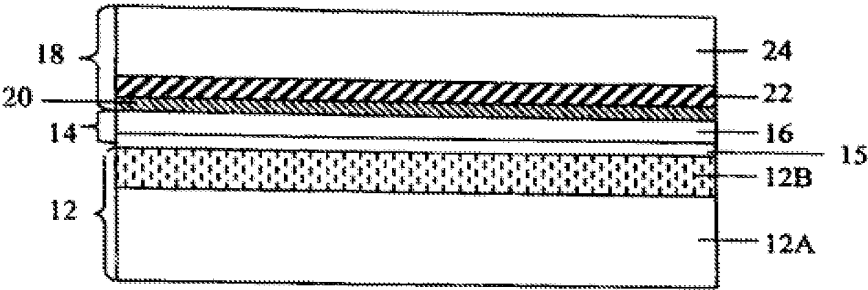


圖 3

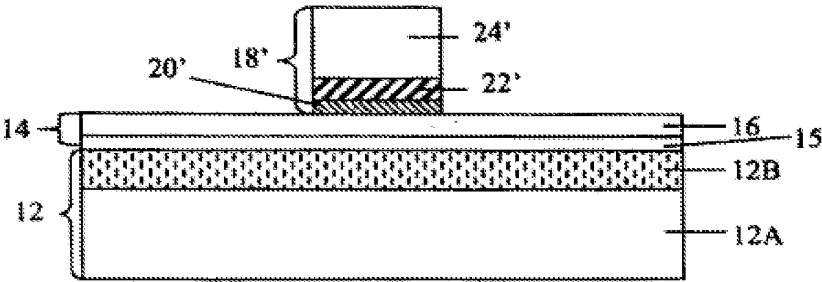


圖 4

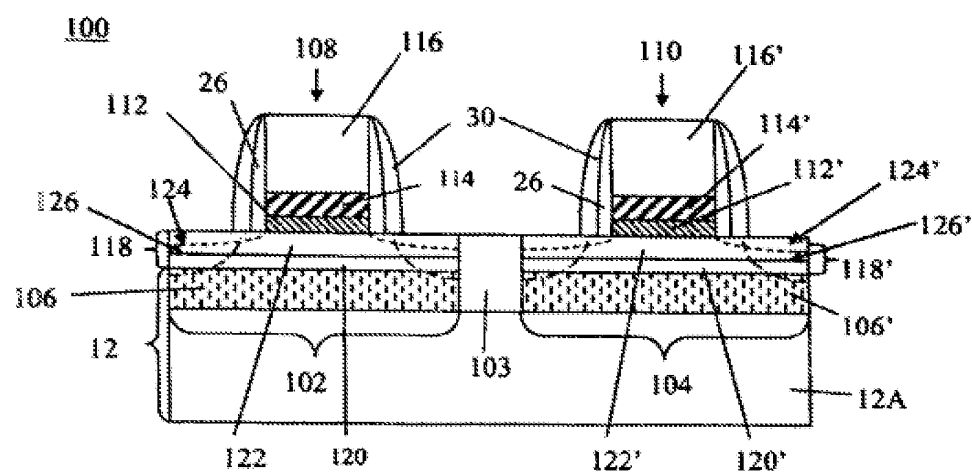


圖 7

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四、指定代表圖：

(一)本案指定代表圖為：圖 3。

(二)本代表圖之元件符號簡單說明：

12 半導體基板

12A 下區域

12B 井區

14 半導體材料堆疊

15 含半導體緩衝層

16 含無摻雜半導體通道層

18 閘極材料堆疊

20 高介電常數閘極介電層

22 功函數金屬層

24 多晶矽層

五、本案若有化學式時，請揭示最能顯示發明特徵的化學式：無。

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property
Organization
International Bureau



(10) International Publication Number
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[Continued on next page]

(54) Title: ELECTROSTATIC DISCHARGE COMPLIANT PATTERNED ADHESIVE TAPE

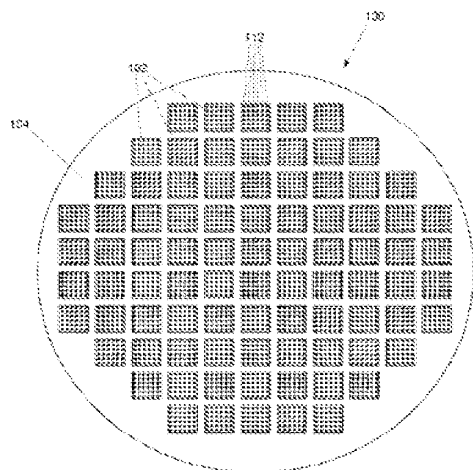


FIG. 1 (Prior Art)

(57) Abstract: The present disclosure relates to the field of fabricating microelectronic devices, wherein a microelectronic device substrate, such as a microelectronic wafer, may be thinned by a backgrinding process using a patterned adhesive tape that reduces slurry seepage and adhesive contamination while also reducing the potential of electrostatic discharge damage. The patterned adhesive tape may comprise a base film and adhesive material patterned on the base film such that an edge or periphery portion of the microelectronic device substrate may contact the adhesive material, but substantially no adhesive material contacts interconnectors formed on the microelectronic device substrate. The base film of the patterned adhesive tape may have an electrically conductive coating or layer, or may be electrically conductive itself to reduce the potential of electrostatic discharge damage during the backgrinding process.

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SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

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ELECTROSTATIC DISCHARGE COMPENSATION PATTERNED ADHESIVE TAPEBACKGROUND

Embodiments of the present description generally relate to the field of microelectronic
5 device fabrication and, more particularly, to thinning of microelectronic wafers with a
backgrinding process.

BRIEF DESCRIPTION OF THE DRAWINGS

The subject matter of the present disclosure is particularly pointed out and distinctly
claimed in the concluding portion of the specification. The foregoing and other features of the
10 present disclosure will become more fully apparent from the following description and appended
claims, taken in conjunction with the accompanying drawings. It is understood that the
accompanying drawings depict only several embodiments in accordance with the present
disclosure and are, therefore, not to be considered limiting of its scope. The disclosure will be
described with additional specificity and detail through use of the accompanying drawings, such
15 that the advantages of the present disclosure can be more readily ascertained, in which:

FIG. 1 illustrates a microelectronic device substrate having a plurality of microelectronic
dice on an active surface thereof, as known in the art.

FIG. 2 illustrates a side cross-sectional view of an adhesive tape applied over an active
surface of a microelectronic device substrate prior to a backgrinding process, wherein an
20 adhesive material of the adhesive tape substantially encapsulates interconnectors disposed on the
active surface of the microelectronic device substrate, as known in the art.

FIG. 3 illustrates a side cross-sectional view of the structure of FIG. 2 after the
backgrinding process, as known in the art.

FIG. 4 illustrates a side cross-sectional view of an adhesive tape applied over an active
25 surface of a microelectronic device substrate, wherein an adhesive material of the adhesive tape
substantially encapsulates an upper portion of interconnectors disposed on the active surface of
the microelectronic device substrate (illustrated after the backgrinding process), as known in the
art.

FIG. 5 illustrates a side cross-sectional view of an adhesive tape applied over an active
30 surface of a microelectronic device substrate, wherein an adhesive material of the adhesive tape
contacts a top portion of the interconnectors disposed on the active surface of the microelectronic
device substrate (illustrated after the backgrinding process), as known in the art.

FIG. 6 illustrates a film-side oblique view of a patterned adhesive tape according to an embodiment of the present description.

FIG. 7 illustrates an adhesive-side view of the patterned adhesive tape of FIG. 8, according to an embodiment of the present description.

5 FIG. 8 illustrates a side cross-sectional view of the patterned adhesive tape, according to an embodiment of the present description applied over an active surface of a microelectronic device substrate.

FIG. 9 illustrates a side cross-sectional view of the inset A of FIG. 8, according to an embodiment of the present description.

10 FIG. 10 illustrates a side cross-sectional view of the inset A of FIG. 8, according to another embodiment of the present description.

FIG. 11 illustrates a side cross-sectional view of the inset A of FIG. 8, according to a still another embodiment of the present description.

15 FIG. 12 illustrates a side cross-sectional view of the inset A of FIG. 8, according to a further embodiment of the present description.

FIG. 13 is flow diagram of a process of backgrinding a microelectronic device substrate utilizing a patterned adhesive tape according to an embodiment of the present description.

DETAILED DESCRIPTION

20 In the following detailed description, reference is made to the accompanying drawings that show, by way of illustration, specific embodiments in which the claimed subject matter may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the subject matter. It is to be understood that the various embodiments, although different, are not necessarily mutually exclusive. For example, a particular feature, structure, or characteristic described herein, in connection with one embodiment, may be implemented within
25 other embodiments without departing from the spirit and scope of the claimed subject matter. References within this specification to "one embodiment" or "an embodiment" mean that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one implementation encompassed within the present invention. Therefore,
30 the use of the phrase "one embodiment" or "in an embodiment" does not necessarily refer to the same embodiment. In addition, it is to be understood that the location or arrangement of individual elements within each disclosed embodiment may be modified without departing from the spirit and scope of the claimed subject matter. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the subject matter is defined only

by the appended claims, appropriately interpreted, along with the full range of equivalents to which the appended claims are entitled. In the drawings, like numerals refer to the same or similar elements or functionality throughout the several views, and that elements depicted therein are not necessarily to scale with one another, rather individual elements may be enlarged or
5 reduced in order to more easily comprehend the elements in the context of the present description.

Embodiments of the present description relate to the field of fabricating microelectronic devices, wherein a microelectronic device substrate, such as a microelectronic wafer, may be thinned by a backgrinding process using a patterned adhesive tape that reduces slurry seepage
10 and adhesive contamination while also reducing the potential of electrostatic discharge damage.

In the production of microelectronic devices, integrated circuitry may be formed in and/or on microelectronic device substrates. As shown in FIG. 1, a single microelectronic device substrate 100, such as a silicon or a silicon-germanium wafer, may contain a plurality of substantially identical integrated circuits (not shown) forming a plurality of microelectronic
15 dice 102, such as microprocessors, chipsets, graphics devices, wireless devices, memory devices, application specific integrated circuits, or the like, on an active surface 104 of the microelectronic device substrate 100. Each of the microelectronic dice 102 may include a plurality of interconnectors 112, such as solder bumps or pillars, which may be in electrical contact with the integrated circuits (not shown) of their respective microelectronic die 102. As
20 will be understood to those skilled in the art, the interconnectors 112 may be used in connect the microelectronic dice 102 to external device or components (not shown). The interconnectors 112 may be any appropriate electrically conductive material, including but not limited to lead/tin alloys, such as tin/lead solder, such as 63% tin / 37% lead solder, or lead-free solders, such a pure tin or high tin content alloys (e.g. 90% or more tin), such as tin/bismuth, eutectic tin/silver,
25 ternary tin/silver/copper, eutectic tin/copper, and similar alloys. The fabrication processes for the integrated circuits (not shown) and the interconnectors 112 are well known in the art and will not be discussed herein in the interest of brevity.

In a wafer backgrinding process (also known as 'wafer thinning' or 'backlapping'), a portion of a back surface 106 (see FIG. 2) of the microelectronic device substrate 100, which
30 opposes the microelectronic device substrate active surface 104, is removed to reduce its thickness (see thickness T_1 for FIG. 2 prior to wafer backgrinding and thickness T_2 in FIG. 3 after wafer backgrinding). Wafer backgrinding is not necessary in the fabrication of the microelectronic dice 102 themselves, but as the desire to make microelectronic devices thinner

for use in smart cards, memory sticks, smart phones, portable music players, and other compact electronic products, it has become an advantageous process.

As shown in FIGs. 2 and 3, in the backgrinding process, an adhesive tape 122 may be applied over the microelectronic device substrate active surface 104 prior to the backgrinding process to provide support thereof during the backgrinding process and to protect the microelectronic device substrate 100 from mechanical damage and contamination during the backgrinding process. The adhesive tape 122 may be comprised of a base film 124 and a layer of adhesive material 126. The backgrinding process may be conducted with a backgrinding tool comprising grinding wheels (bonded abrasive particle) and a cooling fluid. After the backgrinding process, the microelectronic device substrate 100 is removed from the adhesive tape 122 and sent for further processing.

As shown in FIGs. 2 and 3, the attachment of the adhesive tape 122 to the microelectronic device substrate active surface 104 may include the adhesive material layer 126 substantially encapsulating the interconnectors 112 and substantially covering the microelectronic device substrate active surface 104. This arrangement may be referred to as "full-bump encapsulation". However, residual adhesive may remain on the microelectronic device substrate active surface 104 and/or interconnectors 112 after the removal of the adhesive tape 122, particularly at a periphery or edge portion 108 proximate an edge 110 of the microelectronic device substrate 100 and in areas of a high density/tight pitch interconnector 112 pattern. Such, residual adhesive can result in defects in the microelectronic dice 102, as will be understood to those skilled in the art.

As shown in FIG. 4, in order to reduce residual adhesive contamination, the attachment of the adhesive tape 122 to the microelectronic device substrate active surface 104 may comprise a portion of the adhesive material layer 126 in contact with the microelectronic device substrate edge portion 108 and in contact with a top portion 114 of each interconnector 112 and an upper portion of each interconnector 112 proximate the top portion 114 thereof. This arrangement may be referred to as "partial bump lamination" and may be effectuated by reducing the thickness of the adhesive material layer 126 and/or reducing the adhesive properties of the adhesive material layer 126. Although with the adhesive tape 122 of FIG. 4, it may be possible to reduce or substantially eliminate adhesive residue on the microelectronic device substrate active surface 104, it may result in adhesive residue on the interconnector 112.

As shown in FIG. 5, in order to further reduce residual adhesive contamination, the attachment of the adhesive tape 122 to the microelectronic device substrate active surface 102 may comprise a portion of the adhesive material layer 126 in contact with the microelectronic device substrate edge portion 108 and in contact with the top portion 114 of each

interconnector 112. This arrangement is referred to as "bump top lamination" and maybe effectuated by further reducing the thickness of the adhesive material layer 126 and/or further reducing the adhesive properties of the adhesive material layer 126.

However, reducing the thickness of the adhesive material layer 126 and/or reducing the
5 adhesive properties of the adhesive material layer 126 may increase the risk of seepage
backgrinding slurry between the adhesive material layer 126 and the microelectronic device
substrate active surface 104. Backgrinding slurry is a combination of process cooling fluid and
particles from the grinding wheel due to wear. Such backgrinding slurry contamination can
result in defects in the microelectronic dice 102, as will be understood to those skilled in the art.
10 Moreover, with a desire to increase the number of microelectronic dice 102 (see FIG. 1) on each
microelectronic device substrate 100, the space around the microelectronic device substrate edge
portion 108 is reduced, which reduces the available contact area between the adhesive material
layer 126 and the microelectronic device substrate active surface 104. Thus, the reduction in
contact area and the reduction in the adhesive material thickness may significantly increase the
15 risk of seepage of the backgrinding slurry between the adhesive material layer 126 and the
microelectronic device substrate active surface 104.

Thus, the prevention of adhesive residue is at odds with the prevention of slurry seepage,
because to eliminate the adhesive residue on microelectronic device substrate active surface 102
and/or interconnectors 112, modulus properties of the adhesive material layer 126 have to be
20 increased and, to eliminate the occurrence of slurry seepage, the adhesion properties of the
adhesive material layer 126 have to be increased, which means the modulus properties of
adhesive material layer 126 have to be decreased. Therefore, the materials property of the
adhesive tape 122 cannot be optimally balanced.

Furthermore, the tape lamination process (e.g. attaching the microelectronic device
25 substrate 100 to the adhesive tape 122 prior the backgrinding process) and the de-tape process
(e.g. removing the wafer after the backgrinding process) may generate an electrostatic charge
within the adhesive tape 122. If this electrostatic charge discharges through the
interconnectors 112, the discharge can damage the integrated circuits, such as copper traces and
interlayer dielectric layers (not shown) of their respective microelectronic dice 102 (see FIG. 1),
30 as will be understood those skilled in the art.

In an embodiment of the present disclosure, a patterned adhesive tape 200 may be
comprised of a base film 202 and an adhesive material layer 204 disposed therein on, with at
least one opening 212 patterned through an adhesive material layer 204, as shown in FIGs. 6
and 7. As shown in FIG. 8, an intermediate structure 210 may be formed by attaching a

microelectronic device substrate 100 to the adhesive material layer 204. The adhesive material layer openings 212 may be patterned, such that the microelectronic device substrate edge portion 108 may contact the adhesive material layer 204, but substantially no portion of the adhesive material layer 204 contacts the interconnectors 112, as shown in FIG. 8. Such an arrangement may substantially reduce adhesive residue contamination and/or backgrinding slurry seepage. With regard to adhesive residue contamination reduction, having substantially no portion of the adhesive material layer 204 contacting the interconnectors 112, means that substantially no adhesive residue will result on the interconnectors 112. With regard to backgrinding slurry seepage reduction, having the adhesive material layer 204 only contacting the microelectronic device substrate edge portion 108 will allow for the use of the adhesive material layer 204 having of low modulus and high tackiness to achieve an effective seal, which may significantly reduce or prevent slurry seepage during the backgrinding process.

In one embodiment, the opening 212 through the adhesive material layer 204 may be substantially circular. In another embodiment, the opening 212 may be sized such that the microelectronic device substrate edge portion 108 which contacts the adhesive material layer 204 has a width of about equal to or less than about 3 mm. In still another embodiment, the opening 212 may be sized such that the microelectronic device substrate edge portion 108 which contacts the adhesive material layer 204 has a width of about equal to or less than about 2 mm. The adhesive material layer 204 may be an ultra-violet light curable adhesive. In one embodiment, the adhesive material layer 204 may have an adhesion greater than about 4500 mN / 25 mm.

Referring back to FIG. 6, at least one alignment mark 214 may be formed on the base film 202 of the patterned adhesive tape 200 to allow appropriate positioning of the microelectronic device substrate 100 (see FIG. 8) in relation to the openings 212 of the patterned adhesive tape 200.

In one embodiment of the present description, the base film 202 may include an electrically conductive element therein as a mechanism for electrostatic discharge. As will be understood to those skilled in the art, the electrically conductive element may be grounded such that any electrostatic charge that may be built-up during the attachment of the patterned adhesive tape 200 to the microelectronic device substrate 100 and/or during the removal of the microelectronic device substrate 100 from the patterned adhesive tape 200 may be discharged.

In one embodiment shown in the FIG. 8, the base film 202 itself may be the electrically conductive element. The electrically conductive base film 202 may comprise any electrically conductive material, including but not limited to, conducting polymers (such as polyphenylenes,

polypyrenes, polyazulenes, polynaphthalenes, polyacetylenes, poly p-phenylene vinylenes, polypyrroles, polycarbazoles, polyindoles, polyazepines, polyanilines, polythiophenes, poly(3,4-ethylenedioxythiophene)s, poly(p-phenylene sulfide)s, functionalized polyethylene oxides, ionomers, and ionic conductive polymers), or may contain conductive fillers, including but not limited to, metal coated glass, aluminum doped zinc oxide, nickel-coated graphite, fluorine-doped tin oxide, nickel graphite, indium tin oxide, silver particles, tin particles, and the like.

In another embodiment shown in FIG. 9, the base film 202 may comprise a support film 220 and an electrically conductive coating or film 230, as the electrically conductive element. The support film 220 may comprise any appropriate material, including but not limited to, polymer materials. The electrically conductive film 230 may comprise any electrically conductive material, including but not limited to, conducting polymers (such as polyphenylenes, polypyrenes, polyazulenes, polynaphthalenes, polyacetylenes, poly p-phenylene vinylenes, polypyrroles, polycarbazoles, polyindoles, polyazepines, polyanilines, polythiophenes, poly(3,4-ethylenedioxythiophene)s, poly(p-phenylene sulfide)s, functionalized polyethylene oxides, ionomers, and ionic conductive polymers), or may contain conductive fillers, including but not limited to, metal coated glass, aluminum doped zinc oxide, nickel-coated graphite, fluorine-doped tin oxide, nickel graphite, indium tin oxide, silver particles, tin particles, and the like. As shown in FIG. 9, the electrically conductive film 220 may be disposed between a first surface 222 of the support film 220 and the adhesive material layer 204. As shown in FIG. 10, the electrically conductive film 230 may be disposed proximate a second surface 224 of the support film 220 (opposing the support film first surface 222 and the adhesive material layer 204). It is understood that the base film 202 may comprise a plurality of layers of support film 220 and/or a plurality of layers of electrically conductive film 230. Such multiple layers within the base film 202 may allow for the tuning of the mechanical properties of the base film 202 for use in ultra-thin wafer thinning (e.g. thinning to less than about 200 μm)

In order to minimize stress and have sufficient support of the microelectronic device substrate 100 during the backgrinding process, a height H of the interconnector 112 may be approximately the same as a thickness T of the adhesive material layer 204, as shown in FIGs. 9 and 10.

In another embodiment of the present description, with ultra-thin substrate thinning, due to no adhesive in the bump area during thinning, there may not be sufficient support for microelectronic device substrate 100. Therefore, as shown in FIG. 11, a compliant layer 240 may be disposed proximate the support film first surface 222, such that the compliant layer 240 at least partially (e.g., either partially (shown) or fully) encapsulates the interconnectors 112, to

provide additional support. The use of the compliant layer 240 may result in lower shear stresses on the microelectronic device substrate edge portion 108 (see FIG. 8) with more uniform stress transferred across an entire contact surface between the patterned adhesive tape 200 and the microelectronic device substrate 100, as will be understood to those skilled in the art. The compliant layer 240 may include any appropriate material, including but not limited to a soft polymer layer, such as an ultraviolet light curable adhesive, pre-cured elastomer, and the like. It is understood that the compliant layer 240 should be selected such that it does not leave residual

As shown in FIG. 12, the compliant layer 240 may itself be the electrically conductive element or may contain the electrically conductive element, such as electrically conductive particles 250, dispersed therein, to act as an electrostatic discharge means. The electrically conductive particles 250 may include, but is not limited to, metal coated glass, aluminum doped zinc oxide, nickel-coated graphite, fluorine-doped tin oxide, nickel graphite, indium tin oxide, silver particles, tin particles, and the like. Furthermore, as also shown in FIG. 12, the electrically conductive particles 250 may also be contained within the support film 220 to have the support film 220 to act as an electrostatic discharge means in addition to or in lieu of the electrically conductive particles 250 in the compliant layer 240.

It is understood the subject matter of the present description can including combination of layer of support films 220, electrically conductive film 230, and compliant layers 240.

An embodiment of one process of thinning a microelectronic device substrate using the patterned adhesive tape of the present description is illustrated in a flow diagram 300 of FIG. 13. As defined in block 310, an adhesive tape may be formed with a base film and an adhesive material layer disposed thereon with at least one opening patterned through the adhesive material layer, wherein the base film includes an electrically conductive element. A microelectronic device substrate, having a plurality of interconnectors extending from an active surface thereof, may be attached to the patterned adhesive tape, such that an edge or periphery of the microelectronic device substrate active surface adheres to the adhesive material layer proximate the opening with the plurality interconnectors extending into the adhesive material layer opening, and wherein any electrostatic charge generated during the adhering of the microelectronic device substrate is discharged through the base film electrically conductive element, as defined in block 320. As defined in block 330, the microelectronic device substrate may be thinned by removing a portion of the microelectronic device substrate from a back surface thereof. The microelectronic device substrate may then be removed from the patterned adhesive tape while discharging any electrostatic charge generated during the removal through the base film electrically conductive element, as defined in block 340.

It is understood that the subject matter of the present description is not necessarily limited to specific applications illustrated in FIGs. 8-13. The subject matter may be applied to other microelectronic device fabrication applications, as will be understood to those skilled in the art. Furthermore, the subject matter may also be used in any appropriate application outside of the microelectronic device fabrication field.

Having thus described in detail embodiments of the present invention, it is understood that the invention defined by the appended claims is not to be limited by particular details set forth in the above description, as many apparent variations thereof are possible without departing from the spirit or scope thereof.

CLAIMS

What is claimed is:

1. A patterned adhesive tape comprising:
a base film including an electrically conductive element; and
5 an adhesive material layer disposed proximate a first surface of the base film with at least one opening patterned through the adhesive material layer, wherein the at least one opening is adapted to adhere to an edge portion of a microelectronic device substrate.
2. The patterned adhesive tape of claim 1, wherein the base film comprises a conductive
10 polymer.
3. The patterned adhesive tape of claim 1, wherein the electrically conductive element comprises electrically conductive particles dispersed within the base film.
- 15 4. The patterned adhesive tape of claim 1, wherein the base film comprises a support film and an electrically conductive film as the electrically conductive element.
5. The patterned adhesive tape of claim 4, wherein the support film comprises a polymer
film.
20
6. The patterned adhesive tape of claim 4, wherein the electrically conductive film comprises a conductive polymer.
7. The patterned adhesive tape of claim 4, wherein the electrically conductive film is
25 disposed on a first surface of the support film with at least a portion thereof between the support film and the adhesive material layer.
8. The patterned adhesive tape of claim 4, wherein the electrically conductive film is
disposed on a second surface of the support film opposing the adhesive material layer on a first
30 surface of the support film.

9. The patterned adhesive tape of claim 1, wherein the base film further includes a compliant layer disposed adjacent the adhesive material layer, wherein a portion of the compliant layer is exposed within the at least one opening.
- 5 10. The patterned adhesive tape of claim 9, wherein the electrically conductive element comprises electrically conductive particles dispersed within the compliant layer.
11. An intermediate structure comprising:
a base film including an electrically conductive element;
10 an adhesive material layer disposed on the base film having at least one opening patterned therethrough; and
a microelectronic device substrate having active surface, a edge portion proximate an edge of the microelectronic device substrate, and a plurality of interconnectors extending from the microelectronic device substrate active surface, wherein the microelectronic device edge
15 portion is adhered to the adhesive material layer and wherein the plurality of interconnectors extend into the at least one opening.
12. The intermediate structure of claim 11, wherein a height of the plurality of interconnectors is approximately the same as a thickness of the adhesive material layer.
- 20 13. The intermediate structure of claim 12, wherein the base film comprises conductive polymer.
14. The intermediate structure of claim 11, wherein the electrically conductive element
25 comprises electrically conductive particles dispersed within the base film.
15. The intermediate structure of claim 11, wherein the base film comprises a support film and an electrically conductive film as the electrically conductive element.
- 30 16. The intermediate structure of claim 15, wherein the support film comprises a polymer film.
17. The intermediate structure of claim 15, wherein the electrically conductive film comprises a conductive polymer.

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18. The intermediate structure of claim 15, wherein the electrically conductive film is disposed on a first surface of the support film with at least a portion thereof between the support film and the adhesive material layer.

5

19. The intermediate structure of claim 15, wherein the electrically conductive film is disposed on a second surface of the support film opposing the adhesive material layer on a first surface of the support film.

10 20. The intermediate structure of claim 11, wherein the base film further includes a compliant layer disposed adjacent the adhesive material layer, wherein a portion of the compliant layer is exposed within the at least one opening and wherein the compliant layer at least partially encapsulates the plurality of interconnectors.

15 21. The intermediate structure of claim 20, wherein the electrically conductive element comprises electrically conductive particles dispersed within the compliant layer.

22. The intermediate structure of claim 11, wherein the base film further includes an alignment mark.

20

23. A method of thinning a microelectronic device substrate comprising:

forming a patterned adhesive tape with a base film and an adhesive material layer disposed thereon with at least one opening patterned through the adhesive material layer, wherein the base film includes an electrically conductive element;

25 adhering an edge portion of an active surface of a microelectronic device substrate to the adhesive material layer proximate the adhesive material layer opening, wherein a plurality of interconnectors disposed on the microelectronic substrate active surface extend into the adhesive material layer opening, and wherein any electrostatic charge generated during the adhering of the microelectronic device substrate is discharged through the base film electrically conductive element;

30

removing a portion of the microelectronic device substrate from a back surface thereof; and

removing the microelectronic device substrate from the patterned adhesive tape while discharging any electrostatic charge generated during the removal through the base film electrically conductive element.

- 5 24. The method of claim 23, wherein removing the portion of the microelectronic device substrate comprises backgrinding the microelectronic device substrate back surface.
25. The method of claim 23, wherein forming the patterned adhesive tape with the base film and the adhesive material layer disposed thereon comprises forming a thickness of the adhesive
10 material layer that is approximately the same as a height of the plurality of interconnectors on the microelectronic device substrate.
26. The method of claim 23, wherein forming a pattern adhesive tape includes forming a compliant layer disposed adjacent the adhesive material layer, wherein a portion of the compliant
15 layer is exposed within the at least one opening and wherein adhering the microelectronic device substrate includes the compliant layer at least partially encapsulating the plurality of interconnectors.
27. The method of claim 23, wherein adhering the edge portion of the active surface of the
20 microelectronic device substrate to the adhesive material layer proximate the adhesive material layer opening further comprises aligning the microelectronic device substrate to the adhesive material layer opening with at least one alignment mark on the base film.

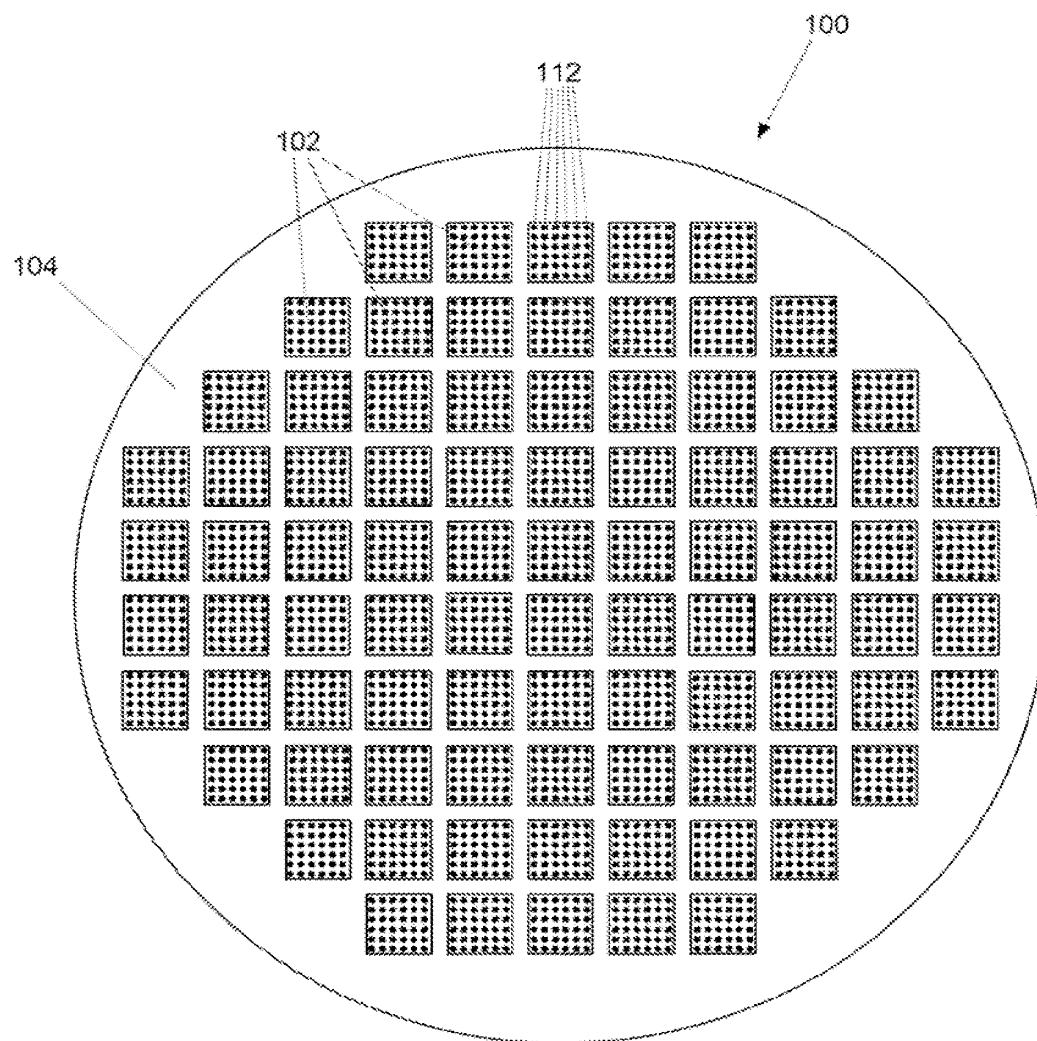


FIG. 1 (Prior Art)

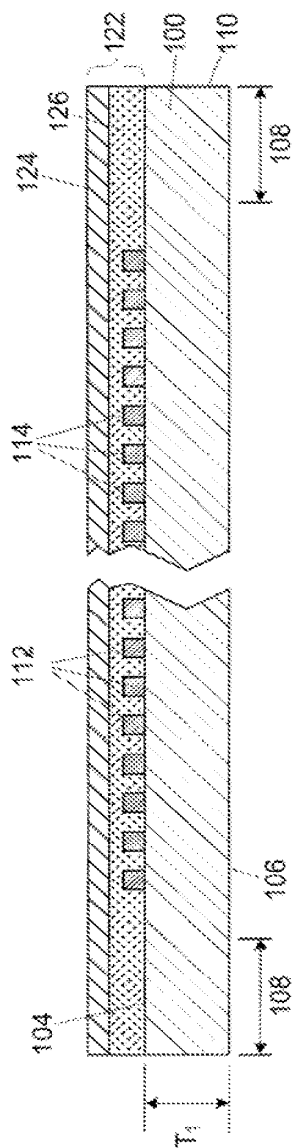


FIG. 2 (Prior Art)

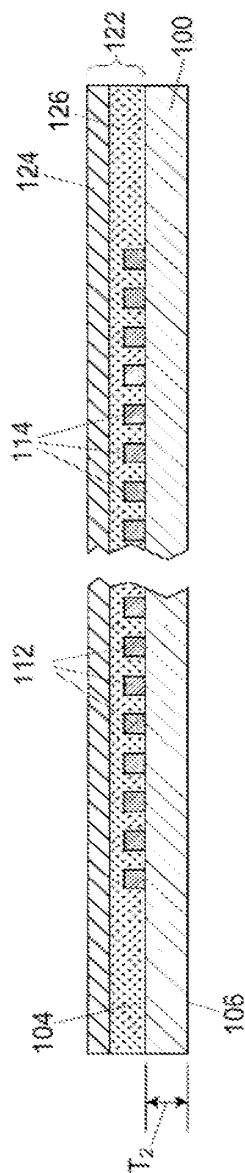


FIG. 3 (Prior Art)

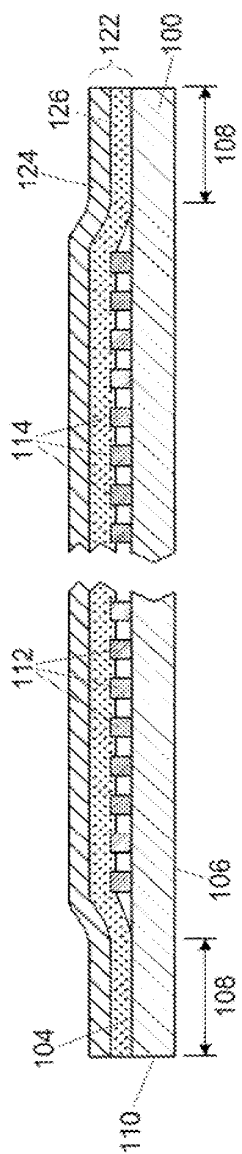


FIG. 4 (Prior Art)

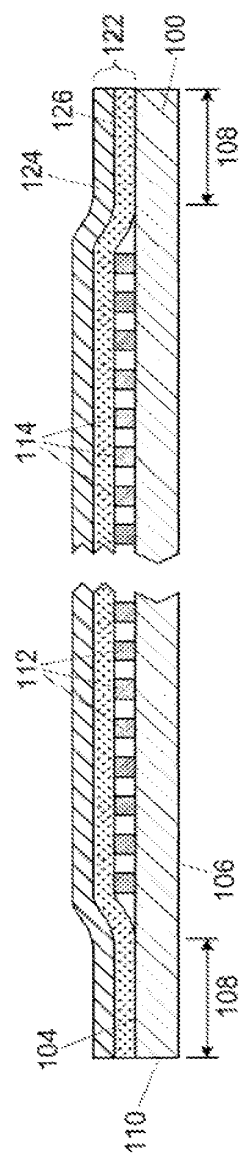


FIG. 5 (Prior Art)

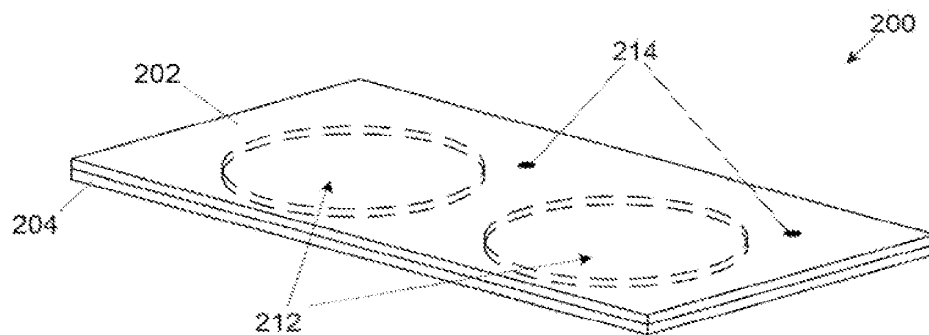


FIG. 6

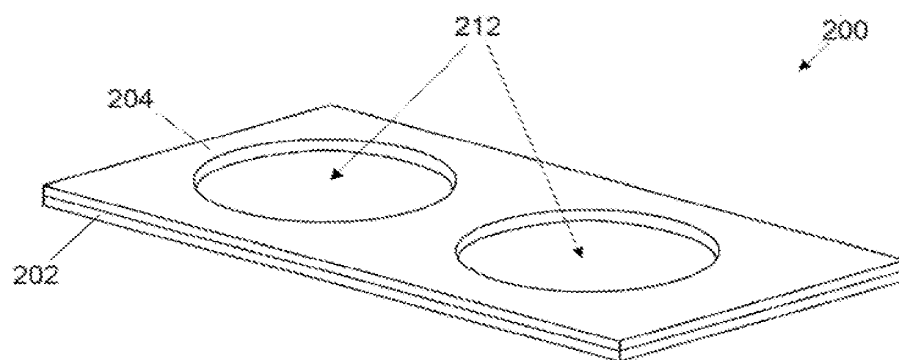


FIG. 7

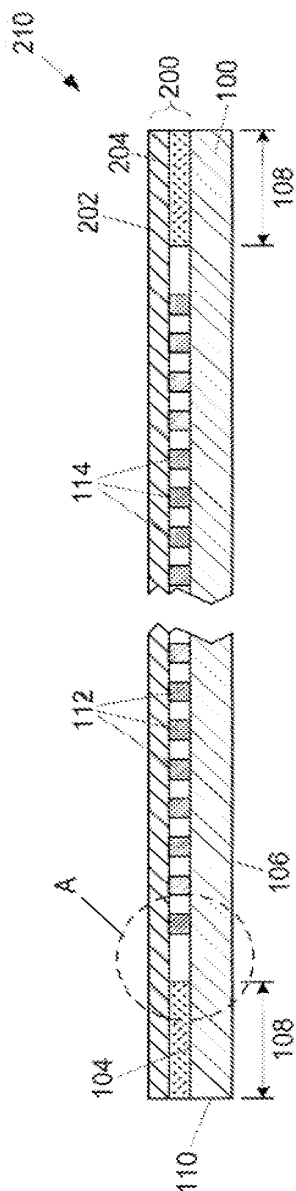


FIG. 8

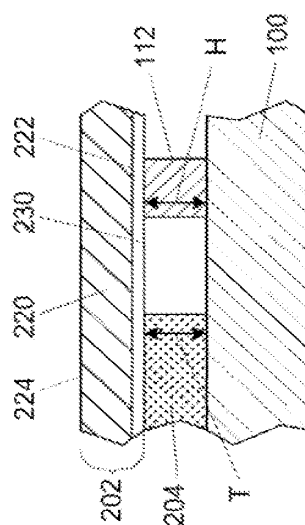


FIG. 9

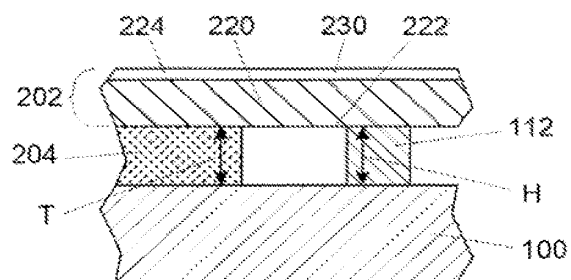


FIG. 10

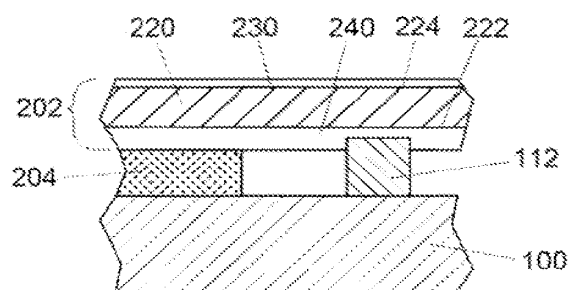


FIG. 11

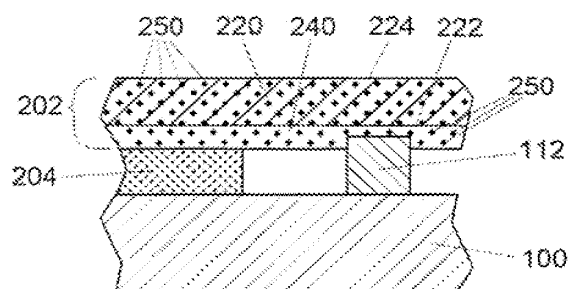


FIG. 12

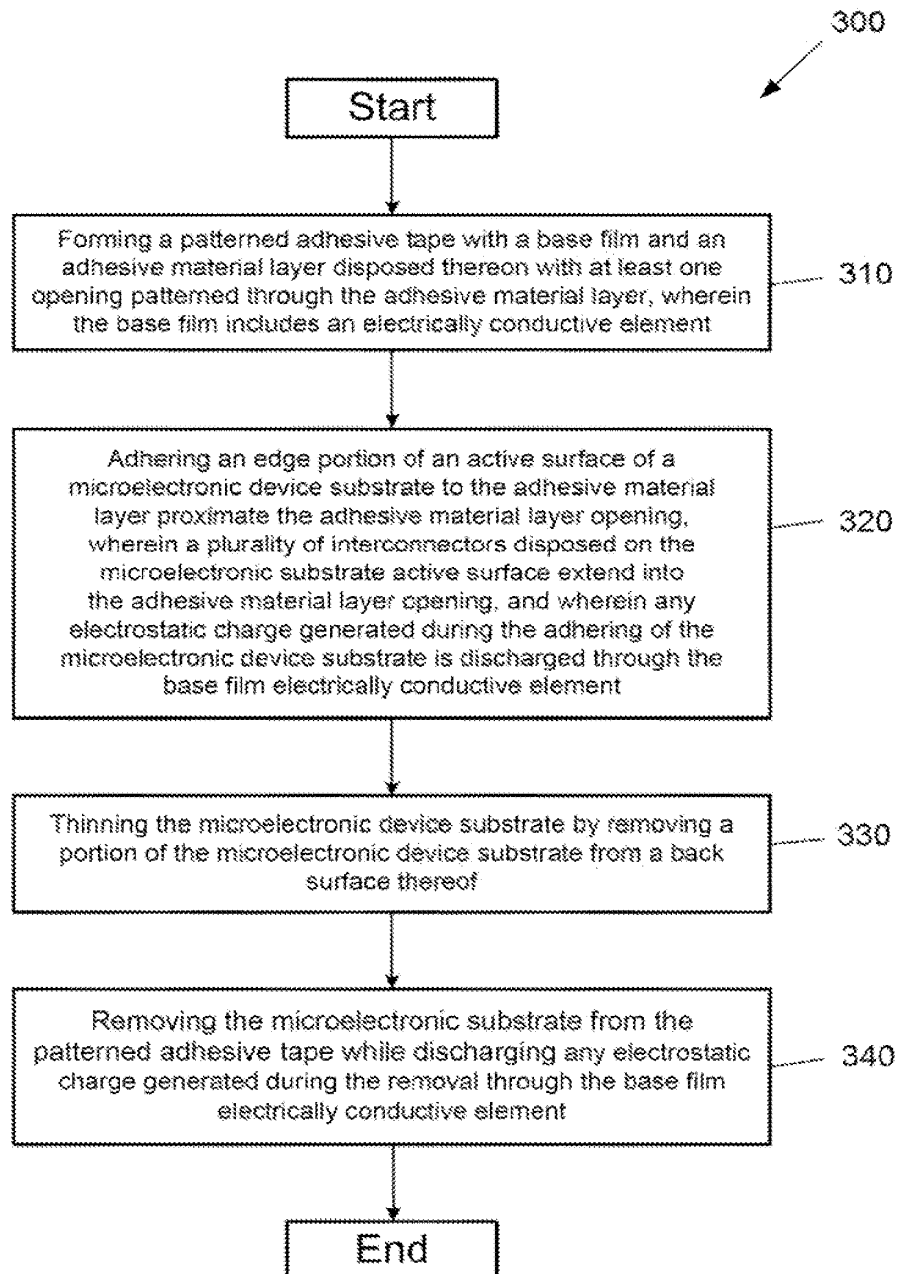


FIG. 13

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2011/066921**A. CLASSIFICATION OF SUBJECT MATTER****H01L 21/301(2006.01); H01L 21/304(2006.01);**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/301; B24B 7/30; C09J 7/02; B24B 1/09; B32B 7/12; B24B 49/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: backgrinding; adhesive tape; opening; conductive element; electrostatic charge

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2007-0666184 A1 (NAGAMOTO; KOICHI et al.) 22 March 2007 See paragraphs [0035]-[0051]; and figures 1-3.	1-27
Y	US 2011-0151250 A1 (YASUDA; TERUHIKO et al.) 23 June 2011 See paragraphs [0120], [0121], [0129], [0136].	1-27
Y	US 2009-0142991 A1 (KON; DO MIN) 04 June 2009 See paragraph [0112]; and figures 6A-6E.	22, 27



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

26 SEPTEMBER 2012 (26.09.2012)

Date of mailing of the international search report

27 SEPTEMBER 2012 (27.09.2012)

Name and mailing address of the ISA/KR

Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan
City, 302-701, Republic of Korea

Facsimile No. 82-42-472-7140

Authorized officer

Lee Seok Joo

Telephone No. 82-42-481-8681



INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/US2011/066921

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2007-0066184 A1	22.03.2007	CN 1868040 A	22.11.2006
		CN 1868040 C0	22.11.2006
		EP 1681713 A1	19.07.2006
		EP 1681713 A4	10.10.2007
		JP 04447280 B2	29.01.2010
		JP 2005-123382 A	12.05.2005
		JP 4447280 B2	07.04.2010
		KR 10-2006-0120113 A	24.11.2006
		US 7438631 B2	21.10.2008
		WO 2005-038894 A1	28.04.2005
US 2011-0151250 A1	23.06.2011	CN 102137909 A	27.07.2011
		EP 2322583 A1	18.05.2011
		KR 10-2011-0050444 A	13.05.2011
		TW 201016816 A	01.05.2010
		WO 2010-026995 A1	11.03.2010
US 2009-0142991 A1	04.06.2009	CN 1986154 A	27.06.2007
		CN 1986154 C0	27.06.2007
		JP 2007-173815 A	05.07.2007
		KR 10-0841094 B1	25.06.2008
		KR 10-2007-0065780A	25.06.2007
		US 2007-0141958 A1	21.06.2007
		US 2009-0149118 A1	11.06.2009

ADVANCE E-MAIL

From the INTERNATIONAL BUREAU

PCT

NOTIFICATION CONCERNING
TRANSMITTAL OF COPY OF INTERNATIONAL
PRELIMINARY REPORT ON PATENTABILITY
(CHAPTER I OF THE PATENT COOPERATION
TREATY)
(PCT Rule 44bis.1(c))

To:

WINKLE, Robert
Winkle, PLLC
C/O CPA Global
PO Box 52050
Minneapolis, Minnesota 55402
ETATS-UNIS D'AMERIQUE

Date of mailing (day/month/year) 03 July 2014 (03.07.2014)		
Applicant's or agent's file reference P40106PCT		IMPORTANT NOTICE
International application No. PCT/US2011/066921	International filing date (day/month/year) 22 December 2011 (22.12.2011)	Priority date (day/month/year)
Applicant INTEL CORPORATION et al		

The International Bureau transmits herewith a copy of the international preliminary report on patentability (Chapter I of the Patent Cooperation Treaty)

The International Bureau of WIPO 34, chemin des Colombettes 1211 Geneva 20, Switzerland Facsimile No. +41 22 338 92 70	Authorized officer Philippe Bécamel e-mail: pu03pct@wipo.int
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PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

(Chapter I of the Patent Cooperation Treaty)

(PCT Rule 44bis)

Applicant's or agent's file reference P40106PCT	FOR FURTHER ACTION		See item 4 below
International application No. PCT/US2011/066921	International filing date (<i>day/month/year</i>) 22 December 2011 (22.12.2011)	Priority date (<i>day/month/year</i>)	
International Patent Classification (8th edition unless older edition indicated) See relevant information in Form PCT/ISA/237			
Applicant INTEL CORPORATION			

1.	This international preliminary report on patentability (Chapter I) is issued by the International Bureau on behalf of the International Searching Authority under Rule 44 bis.1(a).																								
2.	This REPORT consists of a total of 7 sheets, including this cover sheet. In the attached sheets, any reference to the written opinion of the International Searching Authority should be read as a reference to the international preliminary report on patentability (Chapter I) instead.																								
3.	This report contains indications relating to the following items: <table style="width: 100%; border: none;"> <tr> <td style="width: 5%; text-align: center;">☒</td> <td style="width: 30%;">Box No. I</td> <td style="width: 65%;">Basis of the report</td> </tr> <tr> <td style="text-align: center;">☐</td> <td>Box No. II</td> <td>Priority</td> </tr> <tr> <td style="text-align: center;">☐</td> <td>Box No. III</td> <td>Non-establishment of opinion with regard to novelty, inventive step and industrial applicability</td> </tr> <tr> <td style="text-align: center;">☐</td> <td>Box No. IV</td> <td>Lack of unity of invention</td> </tr> <tr> <td style="text-align: center;">☒</td> <td>Box No. V</td> <td>Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement</td> </tr> <tr> <td style="text-align: center;">☐</td> <td>Box No. VI</td> <td>Certain documents cited</td> </tr> <tr> <td style="text-align: center;">☐</td> <td>Box No. VII</td> <td>Certain defects in the international application</td> </tr> <tr> <td style="text-align: center;">☒</td> <td>Box No. VIII</td> <td>Certain observations on the international application</td> </tr> </table>	☒	Box No. I	Basis of the report	☐	Box No. II	Priority	☐	Box No. III	Non-establishment of opinion with regard to novelty, inventive step and industrial applicability	☐	Box No. IV	Lack of unity of invention	☒	Box No. V	Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement	☐	Box No. VI	Certain documents cited	☐	Box No. VII	Certain defects in the international application	☒	Box No. VIII	Certain observations on the international application
☒	Box No. I	Basis of the report																							
☐	Box No. II	Priority																							
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☒	Box No. V	Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement																							
☐	Box No. VI	Certain documents cited																							
☐	Box No. VII	Certain defects in the international application																							
☒	Box No. VIII	Certain observations on the international application																							
4.	The International Bureau will communicate this report to designated Offices in accordance with Rules 44bis.3(c) and 93bis.1 but not, except where the applicant makes an express request under Article 25(2), before the expiration of 30 months from the priority date (Rule 44bis.2).																								

The International Bureau of WIPO 34, chemin des Colombettes 1211 Geneva 20, Switzerland Facsimile No. +41 22 338 82 70	Date of issuance of this report 24 June 2014 (24.06.2014) Authorized officer Philippe Bécamel e-mail: pt03.pcr@wipo.int
--	--

Form PCT/IB/373 (January 2004)

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:
WINKLE ROBERT

WINKLE, PLLC C/O CPA GLOBAL PO BOX 52050
MINNEAPOLIS MN 55402 USA

PCT

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43bis.1)

Date of mailing
(day/month/year) **27 SEPTEMBER 2012 (27.09.2012)**

Applicant's or agent's file reference
P40106PCT

FOR FURTHER ACTION

See paragraph 2 below

International application No.

PCT/US2011/066921

International filing date (day/month/year)

22 DECEMBER 2011 (22.12.2011)

Priority date(day/month/year)

International Patent Classification (IPC) or both national classification and IPC

H01L 21/301(2006.01); H01L 21/304(2006.01);

Applicant

INTEL CORPORATION et al

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☐ Box No. VII Certain defects in the international application
- ☒ Box No. VIII Certain observations on the international application

2. FURTHER ACTION

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1bis(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

Name and mailing address of the ISA/KR
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon
Metropolitan City, 302-701,
Republic of Korea
Facsimile No. 82-42-472-7140

Date of completion of this opinion

26 SEPTEMBER 2012 (26.09.2012)

Authorized officer

Lee Seok Joo

Telephone No. 82-42-481-8681



**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY**

International application No.

PCT/US2011/066921

Box No. 1 Basis of this opinion

1. With regard to the **language**, this opinion has been established on the basis of:
 - ☒ the international application in the language in which it was filed
 - ☐ a translation of the international application into _____, which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))
2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43bis.1(a))
3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of:
 - a. a sequence listing filed or furnished
 - ☐ on paper
 - ☐ in electronic form
 - b. time of filing or furnishing
 - ☐ contained in the international application as filed.
 - ☐ filed together with the international application in electronic form.
 - ☐ furnished subsequently to this Authority for the purposes of search.
4. ☐ In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.
5. Additional comments:

**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY**

International application No.

PCT/US2011/066921

Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Claims	1-27	YES
	Claims	NONE	NO
Inventive step (IS)	Claims	NONE	YES
	Claims	1-27	NO
Industrial applicability (IA)	Claims	1-27	YES
	Claims	NONE	NO

2. Citations and explanations :

Reference is made to the following documents:

D1: US 2007-0066184 A1 (NAGAMOTO; KOICHI et al.) 22 March 2007

D2: US 2011-0151250 A1 (YASUDA; TERUHIKO et al.) 20 June 2011

D3: US 2009-0142891 A1 (MOON; DO MIN) 04 June 2009

1. Novelty and Inventive Step

1.1. Independent claim [1]

D1 discloses a patterned adhesive tape(10) comprising: a base film(1); and an adhesive material layer(2) disposed proximate a first surface of the base film with at least one opening(3) patterned through the adhesive material layer, wherein the at least one opening is adapted to adhere to an edge position of a microelectronic device substrate(4)(see paragraphs [0035]-[0051]; and figures 1-3). Claim [1] differs from D1 in that a base film includes an electrically conductive element. However, D2 discloses an adhesive sheet which is useful as a back grinding tape and suppresses a peel electrostatic charge comprises a substrate including an electrically conductive material layer(see paragraphs [0120], [0121], [0129], [0136]). It would be obvious to a person skilled in the art to apply the feature of D2 to the base film in D1 in order to protect electric circuits from ESD. Therefore, claim [1] does not involve an inventive step under PCT Article 33(3).

1.2. Dependent claims [2-10]

The additional features of claims [2-8] are merely matters of design option with respect to a laminate in D2 comprising the substrate layer and the electrically conductive material layer which can be applied alone or in combination with a binder such as various resins(see paragraph [0120]). Therefore, claims [2-8] do not involve an inventive step under PCT Article 33(3).

The additional feature of claim [9] is identical to the feature of D2 in that a buffer layer is provided between the substrate and the adherence substance(see paragraph [0120]). Therefore, claim [9] does not involve an inventive step under PCT Article 33(3).

The additional feature of claim [10] is merely a matter of design option with respect to the electrically conductive material layer in D2 which can be applied in combination with a binder such as various resins(see paragraph [0120]). Therefore, claim [10] does not involve an inventive step under PCT Article 33(3).

1.3. Independent claim [11]

Continued on Sheet 2 of 2

**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY**

International application No.

PCT/US2011/066921

Box No. VIII Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

Claim [22] is dependent on claim [11]. However, the base file of claim [22] has not been worded in claim [11]. Therefore, claim [22] is not clear as required by PCT Article 6. To establish the opinion, the base file should be replaced by the base film.

**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY**

International application No.

PCT/US2011/066921

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.

Continuation of:

Box V

D1 discloses an intermediate structure comprising: a base film(1); an adhesive material layer(2) disposed on the base film having at least one opening(3) patterned therein; and a microelectronic device substrate(4) having active surface, a edge portion proximate an edge of the microelectronic device substrate, and a plurality of interconnectors(5) extending from the microelectronic device substrate active surface, wherein the microelectronic device edge portion is adhered to the adhesive material layer and wherein the plurality of interconnectors extend into the at least one opening(see paragraphs [0035]-[0051]; and figures 1-3). Claim [11] differs from D1 in that a base film includes an electrically conductive element. However, D2 discloses an adhesive sheet which is useful as a back grinding tape and suppresses a peel electrostatic charge comprises a substrate including an electrically conductive material layer(see paragraphs [0120], [0121], [0129], [0136]). It would be obvious to a person skilled in the art to apply the feature of D2 to the base film in D1 in order to protect electric circuits from ESD. Therefore, claim [11] does not involve an inventive step under PCT Article 33(3).

1.4. Dependent claims [12-22]

The additional feature of claim [12] is identical to the feature of D1 in that a height of the plurality of interconnectors is approximately the same as a thickness of the adhesive material layer(see figure 3). Therefore, claim [12] does not involve an inventive step under PCT Article 33(3).

The additional features of claims [13-19] are merely matters of design option with respect to a laminate in D2 comprising the substrate layer and the electrically conductive material layer which can be applied alone or in combination with a binder such as various resins(see paragraph [0120]). Therefore, claims [13-19] do not involve an inventive step under PCT Article 33(3).

The additional feature of claim [20] is identical to the feature of D2 in that a buffer layer is provided between the substrate and the adherence substance(see paragraph [0120]). Therefore, claim [20] does not involve an inventive step under PCT Article 33(3).

The additional feature of claim [21] is merely a matter of design option with respect to the electrically conductive material layer in D2 which can be applied in combination with a binder such as various resins(see paragraph [0120]). Therefore, claim [21] does not involve an inventive step under PCT Article 33(3).

The additional feature of claim [22] is not disclosed in D1. However, D3 discloses a backing film(24) includes an alignment mark(15) on a substrate layer(123)(see paragraph [0112]; and figures 6A-6B). It would be obvious to a person skilled in the art to apply the feature of D3 to the base film in D1 in order to align the microelectronic device substrate on the base film. Therefore, claim [22] does not involve an inventive step under PCT Article 33(3).

1.5. Independent claim [23]

D1 discloses a method of thinning a microelectronic device substrate comprising: forming a patterned adhesive tape(10) with a base film(1) and an adhesive material layer(2) disposed thereon with at least one opening(3) patterned through the adhesive material layer; adhering an edge portion of an active surface of a microelectronic device substrate(4) to the adhesive material layer proximate the adhesive material layer opening, wherein a plurality of interconnectors(5) disposed on the microelectronic device active surface extend into the adhesive material layer opening, removing a portion of the microelectronic device substrate from a back surface thereof; and removing the microelectronic device substrate from the patterned adhesive tape(see paragraphs [0035]-[0051]; and figures 1-3). Claim [23] differs from D1 in that a base film includes an electrically conductive element and any electrostatic
Continued on Supplemental Box

**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY**

International application No.

PCT/US2011/066921

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.

Continuation of:

Box V

charge generated during the adhering and the removal is discharged through the base film electrically conductive element. However, D2 discloses an adhesive sheet which is useful as a back grinding tape and suppresses a peel electrostatic charge comprises a substrate including an electrically conductive material layer(see paragraphs [0120], [0121], [0129], [0136]). It would be obvious to a person skilled in the art to apply the feature of D2 to the base film in D1 in order to protect electric circuits from ESD. Therefore, claim [23] does not involve an inventive step under PCT Article 33(3).

1.6. Dependent claims [24-27]

The additional feature of claim [24] is identical to the feature of D1 in that removing the portion of the microelectronic device substrate comprises backgrinding the microelectronic device substrate back surface(see paragraphs [0049]-[0051]). Therefore, claim [24] does not involve an inventive step under PCT Article 33(3).

The additional feature of claim [25] is identical to the feature of D1 in that a height of the plurality of interconnectors is approximately the same as a thickness of the adhesive material layer(see figure 3). Therefore, claim [25] does not involve an inventive step under PCT Article 33(3).

The additional feature of claim [26] is merely a matter of design option with respect to a buffer layer of D2 which is provided between the substrate and the adherence substance(see paragraph [0120]). Therefore, claim [26] does not involve an inventive step under PCT Article 33(3).

The additional feature of claim [27] is not disclosed in D1. However, D3 discloses a backing film(24) includes an alignment mark(15) on a substrate layer(133)(see paragraph [0132]; and figures 6A-6B). It would be obvious to a person skilled in the art to apply the feature of D3 to the base film in D1 in order to align the microelectronic device substrate on the base film. Therefore, claim [27] does not involve an inventive step under PCT Article 33(3).

2. Industrial Applicability

Claims [1-27] are industrially applicable under PCT Article 33(4).

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:
WINKLE ROBERT

WINKLE, PLLC C/O CPA GLOBAL PO BOX 52050
MINNEAPOLIS MN 55402 USA

PCT

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43bis.1)

Date of mailing
(day/month/year) **27 SEPTEMBER 2012 (27.09.2012)**

Applicant's or agent's file reference
P40106PCT

FOR FURTHER ACTION

See paragraph 2 below

International application No.

PCT/US2011/066921

International filing date (day/month/year)

22 DECEMBER 2011 (22.12.2011)

Priority date(day/month/year)

International Patent Classification (IPC) or both national classification and IPC

H01L 21/301(2006.01); H01L 21/304(2006.01);

Applicant

INTEL CORPORATION et al

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☐ Box No. VII Certain defects in the international application
- ☒ Box No. VIII Certain observations on the international application

2. FURTHER ACTION

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1bis(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.
For further options, see Form PCT/ISA/220.

Name and mailing address of the ISA/KR
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon
Metropolitan City, 302-701,
Republic of Korea
Facsimile No. 82-42-472-7140

Date of completion of this opinion

26 SEPTEMBER 2012 (26.09.2012)

Authorized officer

Lee Seok Joo

Telephone No. 82-42-481-8681



**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY**

International application No.

PCT/US2011/066921

Box No. 1 Basis of this opinion

1. With regard to the **language**, this opinion has been established on the basis of:
 - ☒ the international application in the language in which it was filed
 - ☐ a translation of the international application into _____, which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))
2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43bis.1(a))
3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of:
 - a. a sequence listing filed or furnished
 - ☐ on paper
 - ☐ in electronic form
 - b. time of filing or furnishing
 - ☐ contained in the international application as filed.
 - ☐ filed together with the international application in electronic form.
 - ☐ furnished subsequently to this Authority for the purposes of search.
4. ☐ In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.
5. Additional comments:

**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY**

International application No.

PCT/US2011/066921

Box No. V Reasoned statement under Rule 43bis.1(n)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Claims	1-27	YES
	Claims	NONE	NO
Inventive step (IS)	Claims	NONE	YES
	Claims	1-27	NO
Industrial applicability (IA)	Claims	1-27	YES
	Claims	NONE	NO

2. Citations and explanations :

Reference is made to the following documents:

D1: US 2007-0066184 A1 (NAGAMOTO; KOICHI et al.) 22 March 2007

D2: US 2011-0151250 A1 (YASUDA; TERUHIRO et al.) 20 June 2011

D3: US 2009-0142891 A1 (MOON; DO MIN) 04 June 2009

1. Novelty and Inventive Step

1.1. Independent claim [1]

D1 discloses a patterned adhesive tape(10) comprising: a base film(1); and an adhesive material layer(2) disposed proximate a first surface of the base film with at least one opening(3) patterned through the adhesive material layer, wherein the at least one opening is adapted to adhere to an edge position of a microelectronic device substrate(4)(see paragraphs [0035]-[0051]; and figures 1-3). Claim [1] differs from D1 in that a base film includes an electrically conductive element. However, D2 discloses an adhesive sheet which is useful as a back grinding tape and suppresses a peel electrostatic charge comprises a substrate including an electrically conductive material layer(see paragraphs [0120], [0121], [0129], [0136]). It would be obvious to a person skilled in the art to apply the feature of D2 to the base film in D1 in order to protect electric circuits from ESD. Therefore, claim [1] does not involve an inventive step under PCT Article 33(3).

1.2. Dependent claims [2-10]

The additional features of claims [2-8] are merely matters of design option with respect to a laminate in D2 comprising the substrate layer and the electrically conductive material layer which can be applied alone or in combination with a binder such as various resins(see paragraph [0120]). Therefore, claims [2-8] do not involve an inventive step under PCT Article 33(3).

The additional feature of claim [9] is identical to the feature of D2 in that a buffer layer is provided between the substrate and the adherence substance(see paragraph [0120]). Therefore, claim [9] does not involve an inventive step under PCT Article 33(3).

The additional feature of claim [10] is merely a matter of design option with respect to the electrically conductive material layer in D2 which can be applied in combination with a binder such as various resins(see paragraph [0120]). Therefore, claim [10] does not involve an inventive step under PCT Article 33(3).

1.3. Independent claim [11]

Continued on Sheet 2 of 2

**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY**

International application No.

PCT/US2011/066921

Box No. VIII Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

Claim [22] is dependent on claim [11]. However, the base file of claim [22] has not been worded in claim [11]. Therefore, claim [22] is not clear as required by PCT Article 6. To establish the opinion, the base file should be replaced by the base film.

**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY**

International application No.

PCT/US2011/066921

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.

Continuation of:

Box V

D1 discloses an intermediate structure comprising: a base film(1); an adhesive material layer(2) disposed on the base film having at least one opening(3) patterned therein; and a microelectronic device substrate(4) having active surface, a edge portion proximate an edge of the microelectronic device substrate, and a plurality of interconnectors(5) extending from the microelectronic device substrate active surface, wherein the microelectronic device edge portion is adhered to the adhesive material layer and wherein the plurality of interconnectors extend into the at least one opening(see paragraphs [0035]-[0051]; and figures 1-3). Claim [11] differs from D1 in that a base film includes an electrically conductive element. However, D2 discloses an adhesive sheet which is useful as a back grinding tape and suppresses a peel electrostatic charge comprises a substrate including an electrically conductive material layer(see paragraphs [0120], [0121], [0129], [0136]). It would be obvious to a person skilled in the art to apply the feature of D2 to the base film in D1 in order to protect electric circuits from ESD. Therefore, claim [11] does not involve an inventive step under PCT Article 33(3).

1.4. Dependent claims [12-22]

The additional feature of claim [12] is identical to the feature of D1 in that a height of the plurality of interconnectors is approximately the same as a thickness of the adhesive material layer(see figure 3). Therefore, claim [12] does not involve an inventive step under PCT Article 33(3).

The additional features of claims [13-19] are merely matters of design option with respect to a laminate in D2 comprising the substrate layer and the electrically conductive material layer which can be applied alone or in combination with a binder such as various resins(see paragraph [0120]). Therefore, claims [13-19] do not involve an inventive step under PCT Article 33(3).

The additional feature of claim [20] is identical to the feature of D2 in that a buffer layer is provided between the substrate and the adherence substance(see paragraph [0120]). Therefore, claim [20] does not involve an inventive step under PCT Article 33(3).

The additional feature of claim [21] is merely a matter of design option with respect to the electrically conductive material layer in D2 which can be applied in combination with a binder such as various resins(see paragraph [0120]). Therefore, claim [21] does not involve an inventive step under PCT Article 33(3).

The additional feature of claim [22] is not disclosed in D1. However, D3 discloses a backing film(24) includes an alignment mark(15) on a substrate layer(123)(see paragraph [0112]; and figures 6A-6B). It would be obvious to a person skilled in the art to apply the feature of D3 to the base film in D1 in order to align the microelectronic device substrate on the base film. Therefore, claim [22] does not involve an inventive step under PCT Article 33(3).

1.5. Independent claim [23]

D1 discloses a method of thinning a microelectronic device substrate comprising: forming a patterned adhesive tape(10) with a base film(1) and an adhesive material layer(2) disposed thereon with at least one opening(3) patterned through the adhesive material layer; adhering an edge portion of an active surface of a microelectronic device substrate(4) to the adhesive material layer proximate the adhesive material layer opening, wherein a plurality of interconnectors(5) disposed on the microelectronic device active surface extend into the adhesive material layer opening, removing a portion of the microelectronic device substrate from a back surface thereof; and removing the microelectronic device substrate from the patterned adhesive tape(see paragraphs [0035]-[0051]; and figures 1-3). Claim [23] differs from D1 in that a base film includes an electrically conductive element and any electrostatic
Continued on Supplemental Box

**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY**

International application No.

PCT/US2011/066921

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.

Continuation of:

Box V

charge generated during the adhering and the removal is discharged through the base film electrically conductive element. However, D2 discloses an adhesive sheet which is useful as a back grinding tape and suppresses a peel electrostatic charge comprises a substrate including an electrically conductive material layer(see paragraphs [0120], [0121], [0129], [0136]). It would be obvious to a person skilled in the art to apply the feature of D2 to the base film in D1 in order to protect electric circuits from ESD. Therefore, claim [23] does not involve an inventive step under PCT Article 33(3).

1.6. Dependent claims [24-27]

The additional feature of claim [24] is identical to the feature of D1 in that removing the portion of the microelectronic device substrate comprises backgrinding the microelectronic device substrate back surface(see paragraphs [0049]-[0051]). Therefore, claim [24] does not involve an inventive step under PCT Article 33(3).

The additional feature of claim [25] is identical to the feature of D1 in that a height of the plurality of interconnectors is approximately the same as a thickness of the adhesive material layer(see figure 3). Therefore, claim [25] does not involve an inventive step under PCT Article 33(3).

The additional feature of claim [26] is merely a matter of design option with respect to a buffer layer of D2 which is provided between the substrate and the adherence substance(see paragraph [0120]). Therefore, claim [26] does not involve an inventive step under PCT Article 33(3).

The additional feature of claim [27] is not disclosed in D1. However, D3 discloses a backing film(24) includes an alignment mark(15) on a substrate layer(133)(see paragraph [0132]; and figures 6A-6B). It would be obvious to a person skilled in the art to apply the feature of D3 to the base film in D1 in order to align the microelectronic device substrate on the base film. Therefore, claim [27] does not involve an inventive step under PCT Article 33(3).

2. Industrial Applicability

Claims [1-27] are industrially applicable under PCT Article 33(4).

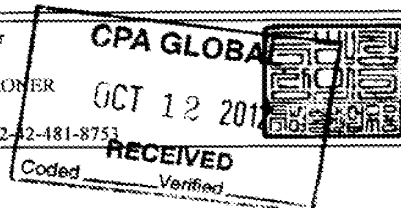
PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

To: WINKLE ROBERT WINKLE, PLLC C/O CPA GLOBAL PO BOX 52050 MINNEAPOLIS MN 55402 USA	PCT NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL SEARCH REPORT AND THE WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY, OR THE DECLARATION (PCT Rule 44.1)
Applicant's or agent's file reference P40106PCT	Date of mailing (day/month/year) 27 SEPTEMBER 2012 (27.09.2012)
International application No. PCT/US2011/066921	International filing date (day/month/year) 22 DECEMBER 2011 (22.12.2011)
Applicant INTEL CORPORATION et al	

1. ☒ The applicant is hereby notified that the international search report and the written opinion of the International Searching Authority have been established and are transmitted herewith.
- Filing of amendments and statement under Article 19:**
- The applicant is entitled, if he so wishes, to amend the claims of the international application (see Rule 46):
- When?** The time limit for filing such amendments is normally two months from the date of transmittal of the international search report.
- Where?** Directly to the International Bureau of WIPO, 34 chemin des Colombettes
1211 Geneva 20, Switzerland, Facsimile No.: +41 22 338 82 70
- For more detailed instructions, see *PCT Applicant's Guide*, International Phase, paragraphs 9.004 - 9.011.**
2. ☐ The applicant is hereby notified that no international search report will be established and that the declaration under Article 17(2)(a) to that effect and the written opinion of the International Searching Authority are transmitted herewith.
3. ☐ **With regard to any protest against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that:**
- ☐ the protest together with the decision thereon has been transmitted to the International Bureau together with any request to forward the texts of both the protest and the decision thereon to the designated Offices.
- ☐ no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.
4. **Reminders**
- The applicant may submit comments on an informal basis on the written opinion of the International Searching Authority to the International Bureau. The International Bureau will send a copy of such comments to all designated Offices unless an international preliminary examination report has been or is to be established. Following the expiration of 30 months from the priority date, these comments will also be made available to the public.
- Shortly after the expiration of **18 months** from the priority date, the international application will be published by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau before the completion of the technical preparations for international publication (Rules 90bis.1 and 90bis.3).
- Within **19 months** from the priority date, but only in respect of some designated Offices, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase **until 30 months** from the priority date (in some Offices even later); otherwise, the applicant must, **within 20 months** from the priority date, perform the prescribed acts for entry into the national phase before those designated Offices.
- In respect of other designated Offices, the time limit of **30 months** (or later) will apply even if no demand is filed within 19 months.
- For details about the applicable time limits, Office by Office, see www.wipo.int/pct/en/texts/time_limits.html and the PCT Applicant's Guide, National Chapters.

Name and mailing address of the ISA/KR  Korean Intellectual Property Office 189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City, 302-701, Republic of Korea Facsimile No. 82-42-472-7140	Authorized officer COMMISSIONER Telephone No. 82-42-481-8753
Form PCT/ISA/220 (July 2010)	



* Attention

Copies of the documents cited in the international search report can be searched in the following Korean Intellectual Property Office English website for three months from the date of mailing of the international search report.

<http://www.kipo.go.kr/en/> => PCT Services => PCT Services

ID : PCT international application number

PW : **QXA5TGHA**

Inquiries related to PCT International Search Report or Written Opinion prepared by KIPO as an International Searching Authority can be answered not only by KIPO but also through IPKC (Intellectual Property Korea Center), located in Vienna, VA, which functions as a PCT Help Desk for PCT applicants.

Homepage: <http://www.ipkcenter.com>

Email: ipkc@ipkcenter.com

Phone: +1 703 388 1066

Fax: +1 703 388 1084

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference P40106PCT	FOR FURTHER ACTION see Form PCT/ISA/220 as well as, where applicable, item 5 below.	
International application No. PCT/US2011/066921	International filing date (day/month/year) 22 DECEMBER 2011 (22.12.2011)	(Earliest) Priority Date (day/month/year)
Applicant INTEL CORPORATION et al		

This International search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 3 sheets.

☐ It is also accompanied by a copy of each prior art document cited in this report.

- Basis of the report**
 - With regard to the language, the international search was carried out on the basis of:
 - ☒ the international application in the language in which it was filed
 - ☐ a translation of the international application into _____, which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))
 - ☐ This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6bis(a)).
 - ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.
- ☐ Certain claims were found **unsearchable** (See Box No. II)
- ☐ **Unity of invention is lacking** (See Box No. III)
- With regard to the title,
 - ☒ the text is approved as submitted by the applicant.
 - ☐ the text has been established by this Authority to read as follows:
- With regard to the abstract,
 - ☒ the text is approved as submitted by the applicant.
 - ☐ the text has been established, according to Rule 38.2, by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.
- With regard to the drawings,
 - the figure of the drawings to be published with the abstract is Figure No. 1
 - ☒ as suggested by the applicant.
 - ☐ as selected by this Authority, because the applicant failed to suggest a figure.
 - ☐ as selected by this Authority, because this figure better characterizes the invention.
 - ☐ none of the figure is to be published with the abstract.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2011/066921**A. CLASSIFICATION OF SUBJECT MATTER***H01L 21/301(2006.01); H01L 21/304(2006.01);*

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/301; B24B 7/30; C09J 7/02; B24B 1/00; B32B 7/12; B24B 49/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: backgrinding; adhesive tape; opening; conductive element; electrostatic charge

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2007-0066184 A1 (NAGAMOTO; KOICHI et al.) 22 March 2007 See paragraphs [0035]-[0051]; and figures 1-3.	1-27
Y	US 2011-0151250 A1 (YASUDA; TERUHIRO et al.) 23 June 2011 See paragraphs [0120], [0121], [0129], [0136].	1-27
Y	ES 2009-0142991 A1 (MOON; DO MIN) 04 June 2009 See paragraph [0112]; and figures 6A-6B.	22, 27

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"I" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

26 SEPTEMBER 2012 (26.09.2012)

Date of mailing of the international search report

27 SEPTEMBER 2012 (27.09.2012)

Name and mailing address of the ISA/KR

Korean Intellectual Property Office
189 Cheongsu-ro, Seo-gu, Daejeon Metropolitan
City, 302-701, Republic of Korea

Facsimile No. 82-42-472-7140

Authorized officer

Lee Seok Joo

Telephone No. 82-42-481-8681



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2011/066921

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2007-0066184 A1	22.03.2007	CN 1868040 A	22.11.2006
		CN 1868040 C0	22.11.2006
		EP 1681713 A1	19.07.2006
		EP 1681713 A4	10.10.2007
		JP 04447280 B2	29.01.2010
		JP 2005-123382 A	12.05.2005
		JP 4447280 B2	07.04.2010
		KR 10-2006-0120113 A	24.11.2006
		US 7438631 B2	21.10.2008
		WO 2005-038894 A1	28.04.2005
US 2011-0151250 A1	23.06.2011	CN 102137909 A	27.07.2011
		EP 2322583 A1	18.05.2011
		KR 10-2011-0050444 A	13.05.2011
		TW 201016816 A	01.05.2010
		WO 2010-026895 A1	11.03.2010
US 2009-0142991 A1	04.06.2009	CN 1986154 A	27.06.2007
		CN 1986154 C0	27.06.2007
		JP 2007-173815 A	05.07.2007
		KR 10-0841094 B1	25.06.2008
		KR 10-2007-0065780A	25.06.2007
		US 2007-0141958 A1	21.06.2007
		US 2009-0149118 A1	11.06.2009

Form PCT/ISA/210 (patent family annex) (July 2009)

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:

WINKLE ROBERT

WINKLE, PLLC C/O CPA GLOBAL PO BOX 52050
MINNEAPOLIS MN 55402 USA

PCT

**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY**

(PCT Rule 43bis.1)

Date of mailing
(day/month/year) **27 SEPTEMBER 2012 (27.09.2012)**

Applicant's or agent's file reference
P40106PCT

FOR FURTHER ACTION

See paragraph 2 below

International application No.

PCT/US2011/066921

International filing date (day/month/year)

22 DECEMBER 2011 (22.12.2011)

Priority date(day/month/year)

International Patent Classification (IPC) or both national classification and IPC

H01L 21/301(2006.01); H01L 21/304(2006.01)

Applicant

INTEL CORPORATION et al

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☐ Box No. VII Certain defects in the international application
- ☒ Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1bis(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

Name and mailing address of the ISA/KR
Korean Intellectual Property Office
189 Cheongsu-ro, Seo-gu, Daejeon
Metropolitan City, 302-701,
Republic of Korea
Facsimile No. 82-42-472-7140

Date of completion of this opinion

26 SEPTEMBER 2012 (26.09.2012)

Authorized officer

Lee Seok Joo

Telephone No. 82-42-481-8681



WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

International application No.

PCT/US2011/066921

Box No. I Basis of this opinion

1. With regard to the **language**, this opinion has been established on the basis of:

- ☒ the international application in the language in which it was filed
- ☐ a translation of the international application into _____, which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(a))

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of:

a. a sequence listing filed or furnished

- ☐ on paper
- ☐ in electronic form

b. time of filing or furnishing

- ☐ contained in the international application as filed.
- ☐ filed together with the international application in electronic form.
- ☐ furnished subsequently to this Authority for the purposes of search.

4. ☐ In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY**

International application No.
PCT/US2011/066921

Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Claims	1-27	YES
	Claims	NONE	NO
Inventive step (IS)	Claims	NONE	YES
	Claims	1-27	NO
Industrial applicability (IA)	Claims	1-27	YES
	Claims	NONE	NO

2. Citations and explanations :

Reference is made to the following documents:

D1: US 2007-0066184 A1 (NAGAMOTO; KOICHI et al.) 22 March 2007
D2: US 2011-0151250 A1 (YASUDA; TERUHIKO et al.) 23 June 2011
D3: US 2009-0142391 A1 (MOON; DO MIN) 04 June 2009

1. Novelty and Inventive Step

1.1. Independent claim [1]

D1 discloses a patterned adhesive tape(10) comprising: a base film(1); and an adhesive material layer(3) disposed proximate a first surface of the base film with at least one opening(3) patterned through the adhesive material layer, wherein the at least one opening is adapted to adhere to an edge position of a microelectronic device substrate(4)(see paragraphs [0035]-[0051]; and figures 1-3). Claim [1] differs from D1 in that a base film includes an electrically conductive element. However, D2 discloses an adhesive sheet which is useful as a back grinding tape and suppresses a peel electrostatic charge comprises a substrate including an electrically conductive material layer(see paragraphs [0120], [0121], [0129], [0136]). It would be obvious to a person skilled in the art to apply the feature of D2 to the base film in D1 in order to protect electric circuits from ESD. Therefore, claim [1] does not involve an inventive step under PCT Article 33(3).

1.2. Dependent claims [2-10]

The additional features of claims [2-8] are merely matters of design option with respect to a laminate in D2 comprising the substrate layer and the electrically conductive material layer which can be applied alone or in combination with a binder such as various resins(see paragraph [0120]). Therefore, claims [2-8] do not involve an inventive step under PCT Article 33(3).

The additional feature of claim [9] is identical to the feature of D2 in that a buffer layer is provided between the substrate and the adherence substance(see paragraph [0120]). Therefore, claim [9] does not involve an inventive step under PCT Article 33(3).

The additional feature of claim [10] is merely a matter of design option with respect to the electrically conductive material layer in D2 which can be applied in combination with a binder such as various resins(see paragraph [0120]). Therefore, claim [10] does not involve an inventive step under PCT Article 33(3).

1.3. Independent claim [11]

Continued on Supplemental Box

**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY**

International application No.

PCT/US2011/066921

Box No. VIII Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

Claim [22] is dependent on claim [11]. However, the base file of claim [22] has not been worded in claim [11]. Therefore, claim [22] is not clear as required by PCT Article 6. To establish the opinion, the base file should be replaced by the base film.

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2011/066921

Supplemental Box

In case the space in any of the preceding boxes is not sufficient,
Continuation of:

Box V

D1 discloses an intermediate structure comprising: a base film(1); an adhesive material layer(2) disposed on the base film having at least one opening(3) patterned therethrough; and a microelectronic device substrate(4) having active surface, a edge portion proximate an edge of the microelectronic device substrate, and a plurality of interconnectors(5) extending from the microelectronic device substrate active surface, wherein the microelectronic device edge portion is adhered to the adhesive material layer and wherein the plurality of interconnectors extend into the at least one opening(see paragraphs [0035]-[0051]; and figures 1-3). Claim [11] differs from D1 in that a base film includes an electrically conductive element. However, D2 discloses an adhesive sheet which is useful as a back grinding tape and suppresses a peel electrostatic charge comprises a substrate including an electrically conductive material layer(see paragraphs [0120], [0121], [0129], [0135]). It would be obvious to a person skilled in the art to apply the feature of D2 to the base film in D1 in order to protect electric circuits from ESD. Therefore, claim [11] does not involve an inventive step under PCT Article 33(3).

1.4. Dependent claims [12-22]

The additional feature of claim [12] is identical to the feature of D1 in that a height of the plurality of interconnectors is approximately the same as a thickness of the adhesive material layer(see figure 3). Therefore, claim [12] does not involve an inventive step under PCT Article 33(3).

The additional features of claims [13-19] are merely matters of design option with respect to a laminate in D2 comprising the substrate layer and the electrically conductive material layer which can be applied alone or in combination with a binder such as various resins(see paragraph [0120]). Therefore, claims [13-19] do not involve an inventive step under PCT Article 33(3).

The additional feature of claim [20] is identical to the feature of D2 in that a buffer layer is provided between the substrate and the adherence substance(see paragraph [0120]). Therefore, claim [20] does not involve an inventive step under PCT Article 33(3).

The additional feature of claim [21] is merely a matter of design option with respect to the electrically conductive material layer in D2 which can be applied in combination with a binder such as various resins(see paragraph [0120]). Therefore, claim [21] does not involve an inventive step under PCT Article 33(3).

The additional feature of claim [22] is not disclosed in D1. However, D3 discloses a backing film(24) includes an alignment mark(15) on a substrate layer(123)(see paragraph [0112]; and figures 6A-6B). It would be obvious to a person skilled in the art to apply the feature of D3 to the base film in D1 in order to align the microelectronic device substrate on the base film. Therefore, claim [22] does not involve an inventive step under PCT Article 33(3).

1.5. Independent claim [23]

D1 discloses a method of thinning a microelectronic device substrate comprising: forming a patterned adhesive tape(10) with a base film(1) and an adhesive material layer(2) disposed thereon with at least one opening(3) patterned through the adhesive material layer; adhering an edge portion of an active surface of a microelectronic device substrate(4) to the adhesive material layer proximate the adhesive material layer opening, wherein a plurality of interconnectors(5) disposed on the microelectronic device substrate active surface extend into the adhesive material layer opening, removing a portion of the microelectronic device substrate from a back surface thereof; and removing the microelectronic device substrate from the patterned adhesive tape(see paragraphs [0035]-[0051]; and figures 1-3). Claim [23] differs from D1 in that a base film includes an electrically conductive element and any electrostatic
Continued on Supplemental Box

**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY**

International application No.

PCT/US2011/066921

Supplemental Box

In case the space in any of the preceding boxes is not sufficient,
Continuation of:

Box V

charge generated during the adhering and the removal is discharged through the base film electrically conductive element. However, D2 discloses an adhesive sheet which is useful as a back grinding tape and suppresses a peel electrostatic charge comprises a substrate including an electrically conductive material layer(see paragraphs [0120], [0121], [0129], [0136]). It would be obvious to a person skilled in the art to apply the feature of D2 to the base film in D1 in order to protect electric circuits from ESD. Therefore, claim [23] does not involve an inventive step under PCT Article 33(3).

1.6. Dependent claims [24-27]

The additional feature of claim [24] is identical to the feature of D1 in that removing the portion of the microelectronic device substrate comprises backgrinding the microelectronic device substrate back surface(see paragraphs [0049]-[0051]). Therefore, claim [24] does not involve an inventive step under PCT Article 33(3).

The additional feature of claim [25] is identical to the feature of D1 in that a height of the plurality of interconnectors is approximately the same as a thickness of the adhesive material layer(see figure 3). Therefore, claim [25] does not involve an inventive step under PCT Article 33(3).

The additional feature of claim [26] is merely a matter of design option with respect to a buffer layer of D2 which is provided between the substrate and the adherence substance(see paragraph [0120]). Therefore, claim [26] does not involve an inventive step under PCT Article 33(3).

The additional feature of claim [27] is not disclosed in D1. However, D3 discloses a backing film(24) includes an alignment mark(15) on a substrate layer(123)(see paragraph [0112]; and figures 6A-6B). It would be obvious to a person skilled in the art to apply the feature of D3 to the base film in D1 in order to align the microelectronic device substrate on the base film. Therefore, claim [27] does not involve an inventive step under PCT Article 33(3).

2. Industrial Applicability

Claims [1-27] are industrially applicable under PCT Article 33(4).

Electronic Patent Application Fee Transmittal				
Application Number:		13992598		
Filing Date:		07-Jun-2013		
Title of Invention:		CAPPING DIELECTRIC STRUCTURE FOR TRANSISTOR GATES		
First Named Inventor/Applicant Name:		Aaron W. Rosenbaum		
Filer:		Robert G. Winkle		
Attorney Docket Number:		P38683US		
Filed as Large Entity				
Filing Fees for U.S. National Stage under 35 USC 371				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Submission- Information Disclosure Stmt	1806	1	180	180
Total in USD (\$)				180

Electronic Acknowledgement Receipt

EFS ID:	22935862
Application Number:	13992598
International Application Number:	
Confirmation Number:	5215
Title of Invention:	CAPPING DIELECTRIC STRUCTURE FOR TRANSISTOR GATES
First Named Inventor/Applicant Name:	Aaron W. Rosenbaum
Customer Number:	92265
Filer:	Robert G. Winkle
Filer Authorized By:	
Attorney Docket Number:	P38683US
Receipt Date:	16-JUL-2015
Filing Date:	07-JUN-2013
Time Stamp:	12:50:38
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$ 180
RAM confirmation Number	11857
Deposit Account	504238
Authorized User	WINKLE, ROBERT G.
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. 1.492 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	P38683US_IDS.pdf	613337	no	6
			74c3b8d19b6283b9ce3174542ad9e816037a0842		
Warnings:					
Information:					
2	Foreign Reference	FR1.pdf	734351	no	20
			2e4eb9de33e5860062ea66de1911b358b5ab70aa		
Warnings:					
Information:					
3	Foreign Reference	FR2.pdf	635896	no	18
			fa6b423d632aa9e141c7584df232d1eb28abc6e9		
Warnings:					
Information:					
4	Foreign Reference	FR3.pdf	2318962	no	47
			957222d5372dd97a912245f712a2fc3aff984c77		
Warnings:					
Information:					
5	Foreign Reference	FR4.pdf	1806077	no	37
			83144e92c800c1fa08439add4d02758687269a7		
Warnings:					
Information:					
6	Foreign Reference	FR5.pdf	1826334	no	27
			962a2b2794feb4c7255e21e1b89f83954042935d		
Warnings:					
Information:					
7	Foreign Reference	FR6.pdf	2198293	no	37
			645ebba7dd76caf0fe6c660b8736e7d4d0bfa858		
Warnings:					
Information:					

8	Foreign Reference	FR7.pdf	3941518	no	24
			df8725a36316d8981238c0243422cdeb5c35d2e5		
Warnings:					
Information:					
9	Non Patent Literature	NPL1.pdf	1241316	no	7
			c073c7f49b0f64c36d509adebd5aa27f84e05ae3		
Warnings:					
Information:					
10	Non Patent Literature	NPL2.pdf	1535890	no	8
			cd9a768832f2d70ff829ecb70d5b7c4f26b81d79		
Warnings:					
Information:					
11	Non Patent Literature	NPL3.pdf	376975	no	5
			ec14085d4c7262d517c091fa515734a58ab1fdd2		
Warnings:					
Information:					
12	Non Patent Literature	NPL4.pdf	819841	no	7
			20b3dc10cd4a551b72eda31ce928c70843ecd80b		
Warnings:					
Information:					
13	Non Patent Literature	NPL5.pdf	497106	no	8
			9aaca747b0801de46731a24fbfb68e93ea1dfefb		
Warnings:					
Information:					
14	Non Patent Literature	NPL6.pdf	328150	no	14
			ad14249ff5ccd24de53664fddd3a5f21819e0e03		
Warnings:					
Information:					
15	Non Patent Literature	NPL7.pdf	1792376	no	11
			688448c22b7f36a5f0a8aa98a5ec1f9cc5a1177e		
Warnings:					
Information:					
16	Fee Worksheet (SB06)	fee-info.pdf	30520	no	2
			ac90a0ac351884a517c71b6837e0c605c88fb95e		
Warnings:					
Information:					

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

92265 7590 07/31/2015
Winkle, PLLC
c/o CPA Global
P.O. Box 52050
Minneapolis, MN 55402

EXAMINER

LAIR, SAMUEL L

ART UNIT

PAPER NUMBER

2817

DATE MAILED: 07/31/2015

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/992,598	06/07/2013	Aaron W. Rosenbaum	P38683US	5215

TITLE OF INVENTION: CAPPING DIELECTRIC STRUCTURE FOR TRANSISTOR GATES

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	11/02/2015

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

92265 7590 07/31/2015
Winkle, PLLC
c/o CPA Global
P.O. Box 52050
Minneapolis, MN 55402

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

13/992,598 06/07/2013 Aaron W. Rosenbaum P38683US 5215

TITLE OF INVENTION: CAPPING DIELECTRIC STRUCTURE FOR TRANSISTOR GATES

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
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nonprovisional UNDISCOUNTED \$960 \$0 \$0 \$960 11/02/2015

EXAMINER	ART UNIT	CLASS-SUBCLASS
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LAIR, SAMUEL L 2817 257-288000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
- 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/992,598	06/07/2013	Aaron W. Rosenbaum	P38683US	5215
92265	7590	07/31/2015	EXAMINER	
Winkle, PLLC c/o CPA Global P.O. Box 52050 Minneapolis, MN 55402			LAIR, SAMUEL L	
			ART UNIT	PAPER NUMBER
			2817	

DATE MAILED: 07/31/2015

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 13/992,598	Applicant(s) ROSENBAUM ET AL.	
	Examiner SAMUEL LAIR	Art Unit 2817	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to communications filed 16 July 2015.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 15-25. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:
a) ☐ All b) ☐ Some *c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)	5. ☐ Examiner's Amendment/Comment
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date <u>07/16/2015</u>	6. ☒ Examiner's Statement of Reasons for Allowance
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material	7. ☐ Other _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.	

/SAMUEL LAIR/ Examiner, Art Unit 2817	
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DETAILED ACTION

1. The present application is being examined under the pre-AIA first to invent provisions.
2. This office action is in response to an amendment filed 14 July 2015. Claims 15-25 are allowed.

Allowable Subject Matter

3. Claims 15-25 are allowed.
4. The following is an examiner's statement of reasons for allowance:
5. Claim 15 is allowable because the prior art of record fails to anticipate or render obvious all limitations of said claim. Liaw, US 2006/046449 A1, Bohr et al., US 2011/0156107 A1, and Lee et al., US 2005/0019993 A1, are the prior art references of record that most resemble the claimed invention. However, none of these references disclose all of the process steps recited in claim 15 and it is not obvious in light of the prior art of record to modify any prior art reference to include all of the process steps recited in claim 15.
6. Claims 16-25 depend on claim 15 and are, therefore, allowable as well.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SAMUEL LAIR whose telephone number is (571)272-5714. The examiner can normally be reached on Wednesday to Saturday, 11:00 AM - 9:30 PM EDT.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eva Montalvo can be reached on (571)270-3829. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/SAMUEL LAIR/
Examiner, Art Unit 2817

/ANTHONY HO/
Primary Examiner, Art Unit 2817

Notice of References Cited	Application/Control No. 13/992,598	Applicant(s)/Patent Under Reexamination ROSENBAUM ET AL.	
	Examiner SAMUEL LAIR	Art Unit 2817	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2005/0019993 A1	01-2005	Lee et al.	438/157
*	B	US-2011/0156107 A1	06-2011	Bohr et al.	257/288
*	C	US-2006/0046449 A1	03-2006	Liaw, Jhon-Jhy	438/585
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
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	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes 	Application/Control No. 13992598	Applicant(s)/Patent Under Reexamination ROSENBAUM ET AL.
	Examiner SAMUEL LAIR	Art Unit 2817

CPC- SEARCHED		
Symbol	Date	Examiner
H01L2029/7858 (limited by date and text)	4/9/2015	SLL
H01L21/28247 (limited by date and text)	4/9/2015	SLL
H01L21/76897 (limited by date and text)	4/9/2015	SLL
H01L29/785 (limited by date and text)	4/9/2015	SLL
H01L29/7851 (limited by date and text)	4/9/2015	SLL
H01L29/7853 (limited by date and text)	4/9/2015	SLL
H01L29/7854 (limited by date and text)	4/9/2015	SLL
H01L29/7855 (limited by date and text)	4/9/2015	SLL
H01L29/7856 (limited by date and text)	4/9/2015	SLL
H01L29/7857 (limited by date and text)	4/9/2015	SLL
H01L29/7858 (limited by date and text)	4/9/2015	SLL
H01L29/66795 (limited by date and text)	4/9/2015	SLL
H01L29/66803 (limited by date and text)	4/9/2015	SLL
H01L29/6681 (limited by date and text)	4/9/2015	SLL
H01L29/66818 (limited by date and text)	4/9/2015	SLL

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
PLUS search	2/26/2015	SLL
Inventor name search (see search history)	4/14/2015	SLL
Pure text search (see search history)	4/14/2015	SLL
NPL search on IEEE Xplore (see search history)	4/14/2015	SLL

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SEARCH NOTES		
Search Notes	Date	Examiner
STIC search (see search history)	3/24/2015	SLL
USPC search limited by text (see search history)	4/9/2015	SLL
CPC search limited by text (see search history)	4/9/2015	SLL
Updated CPC prior art searches to include potential prior art published after 04/09/2015 (see search history)	7/22/2015	SLL
Updated CPC interference searches to include potential prior art published after 04/14/2015 (see search history)	7/22/2015	SLL

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
H01L2029	7858	4/14/2015	SLL
H01L21	2847	4/14/2015	SLL
H01L21	78697	4/14/2015	SLL
H01L29	785	4/14/2015	SLL
H01L29	7851	4/14/2015	SLL
H01L29	7853	4/14/2015	SLL
H01L29	7854	4/14/2015	SLL
H01L29	7855	4/14/2015	SLL
H01L29	7856	4/14/2015	SLL
H01L29	7857	4/14/2015	SLL
H01L29	7858	4/14/2015	SLL
H01L29	66795	4/14/2015	SLL
H01L29	66803	4/14/2015	SLL
H01L29	6681	4/14/2015	SLL
H01L29	66818	4/14/2015	SLL

/SAMUEL LAIR/ Examiner.Art Unit 2817	
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Doc code: IDS

Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13992598	
	Filing Date		2013-06-07	
	First Named Inventor	Aaron W. Rosenbaum		
	Art Unit	2817		
	Examiner Name	Samuel L. Lair		
	Attorney Docket Number	P38683US		

U.S.PATENTS						Remove
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	6030692	A	2000-02-29	Auger, Thomas J.	
	2	6617226	B1	2003-09-09	Suguro, et al.	
	3	6720261	B1	2004-04-13	Anderson, et al.	

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	1	20040203211	A1	2004-10-14	Yang, et al.	
	2	20070066184	A1	2007-03-22	Nagamoto, et al.	
	3	20080290380	A1	2008-11-27	Sheu, et al.	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.L.L./

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	13992598
Filing Date	2013-06-07
First Named Inventor	Aaron W. Rosenbaum
Art Unit	2817
Examiner Name	Samuel L. Lair
Attorney Docket Number	P38683US

4	20090081836	A1	2009-03-26	Liu, et al.	
5	20090142991	A1	2009-06-04	Moon, Do Min	
6	20110108930	A1	2011-05-12	Cheng, et al.	
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10	20130334713	A1	2013-12-19	Xu, et al.	
11	20150155385	A1	2015-06-04	Pradhan, et al.	

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Examiner Initial*	Cite No	Foreign Document Number ³	Country Code ² j	Kind Code ⁴	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear	T ⁵
	1	10-2007-0122319	KR	A	2007-12-31	Jeon, et al.	English Abstract Submitted.	☐

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**INFORMATION DISCLOSURE
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(Not for submission under 37 CFR 1.99)

Application Number	13992598
Filing Date	2013-06-07
First Named Inventor	Aaron W. Rosenbaum
Art Unit	2817
Examiner Name	Samuel L. Lair
Attorney Docket Number	P38683US

2	10-2009-0012793	KR	A	2009-02-04	Jang, et al.	English Abstract Submitted.	☐
3	201110324	TW	A	2011-03-16	Xu, et al.	English Abstract Submitted.	☐
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5	201208078	TW	A	2012-02-16	Chen, et al.	English Abstract Submitted.	☐
6	201236153	TW	A	2012-09-01	Cai, et al.	English Abstract Submitted.	☐
7	2013/095527	WO	A1	2013-06-27	Xu, et al.		☐

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵
	1	Office Action received for Korean Patent Application No. 10-2014-7007165, mailed on April 14, 2015, 5 pages of Korean Office Action and 2 pages of English Translation.	☒
	2	Office Action received for Korean Patent Application No. 10-2014-7007872, mailed on April 28, 2015, 5 pages of Korean Office Action and 3 pages of English Translation.	☒
	3	Office Action received for Taiwan Patent Application No. 101134489, mailed on May 01, 2015, English summary of Office Action in a Reporting Letter, 3 pages of Taiwan Office Action including Search Report.	☐

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Filing Date	2013-06-07
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Art Unit	2817
Examiner Name	Samuel L. Lair
Attorney Docket Number	P38683US

4	Office Action received for Taiwan Patent Application No. 101135607, mailed on May 8, 2015, English summary of Office Action in a Reporting Letter, 5 pages of Taiwan Office Action and 1 page of English Search report.	☐
5	Extended European Search Report received for European Patent Application No. 11873523.2, mailed on May 18, 2015, 8 pages.	☐
6	International Preliminary Report on Patentability and Written Opinion received for PCT Patent Application No. PCT/US2011/066921, mailed on July 03, 2014, 14 pages.	☐
7	International Search Report and Written Opinion received for PCT Patent Application No. PCT/US2011/066921, mailed on September 27, 2012, 11 pages.	☐

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Examiner Signature	/Samuel Lair/	Date Considered	07/22/2015
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)

Application Number	13992598
Filing Date	2013-06-07
First Named Inventor	Aaron W. Rosenbaum
Art Unit	2817
Examiner Name	Samuel L. Lair
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Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

- ☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

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- ☐ See attached certification statement.
- ☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.
- ☐ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Robert G. Winkle/	Date (YYYY-MM-DD)	2015-07-16
Name/Print	Robert G. Winkle	Registration Number	37,474

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	420	H01L2029/7858.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/07/22 16:33
L2	14299	H01L29/785,7851,7853,7854,7855,7856,7857,7858,66795,66803,6681,66818.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/07/22 16:33
L3	14308	L1 or L2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/07/22 16:33
L4	9868	H01L21/28247,76897.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/07/22 16:33
L5	420	H01L2029/7858.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/07/22 16:33
L6	10236	L4 or L5	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/07/22 16:33
L7	536	L6 and (fin or finFET)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/07/22 16:33
L8	14479	L7 or L3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/07/22 16:33
L9	159225	(high near5 density near5 plasma) or PECVD or HDP or (ionized near5 physical near5 vapor) or IPVD or (I near3 PVD) or (plasma near3 enhanc\$5)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/07/22 16:33

L10	201045	(sacrific\$4 or remov\$3 or etch\$3) near7 gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/07/22 16:33
L11	1621	L8 and L9 and L10	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/07/22 16:33
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L14	7353	257/288.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/07/22 16:35
L15	9055	L13 or L14	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/07/22 16:35
L16	1164	L15 and (fin or finFET)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/07/22 16:35
L17	1548	257/E29.264,E21.421.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/07/22 16:35
L18	529	L17 and (fin or finFET)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/07/22 16:35
L19	1627	L18 or L16	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/07/22 16:35
L20	276	L19 and L9 and L10	US-PGPUB; USPAT; USOCR;	OR	ON	2015/07/22 16:35

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
L21	4	L20 and ((@ad <= "20130607") and (@pd >= "20150409"))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/07/22 16:35
L22	33	L21 or L12	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2015/07/22 16:35

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L23	212	H01L2029/7858.cpc.	US- PGPUB; USPAT; UPAD	OR	ON	2015/07/22 16:37
L24	7195	H01L29/785,7851,7853,7854,7855,7856,7857,7858,66795,66803,6681,66818.cpc.	US- PGPUB; USPAT; UPAD	OR	ON	2015/07/22 16:37
L25	5116	H01L21/28247,76897.cpc.	US- PGPUB; USPAT; UPAD	OR	ON	2015/07/22 16:37
L26	2118	((fin or finFET) and (etch\$3 or remov\$3 or sacrificial) and (trench or groove)).clm.	US- PGPUB; USPAT; UPAD	OR	ON	2015/07/22 16:37
L27	958	(L23 or L24 or L25) and L26	US- PGPUB; USPAT; UPAD	OR	ON	2015/07/22 16:37
L29	75	L27 and (@pd >= "20150414")	US- PGPUB; USPAT; UPAD	OR	ON	2015/07/22 16:38

7/ 22/ 2015 4:39:26 PM

C:\Users\slair\Documents\EAST\Workspaces\13992598.wsp

Issue Classification 	Application/Control No. 13992598	Applicant(s)/Patent Under Reexamination ROSENBAUM ET AL.
	Examiner SAMUEL LAIR	Art Unit 2817

CPC					
Symbol				Type	Version
H01L		21	28247	F	2013-01-01
H01L		29	66545	I	2013-01-01
H01L		29	66795	I	2013-01-01
H01L		2029	7858	A	2013-01-01
H01L		29	785	I	2013-01-01
H01L		21	76897	A	2013-01-01

CPC Combination Sets				
Symbol	Type	Set	Ranking	Version

/SAMUEL LAIR/ Examiner.Art Unit 2817 (Assistant Examiner)	07/22/2015 (Date)	Total Claims Allowed: 11	
(Primary Examiner)	(Date)	O.G. Print Claim(s) 1	O.G. Print Figure 25

Issue Classification 	Application/Control No. 13992598	Applicant(s)/Patent Under Reexamination ROSENBAUM ET AL.
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US ORIGINAL CLASSIFICATION						INTERNATIONAL CLASSIFICATION													
CLASS		SUBCLASS				CLAIMED					NON-CLAIMED								
						H	O	1	L	21 / 28 (2006.01.01)									
CROSS REFERENCE(S)																			
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)																		

/SAMUEL LAIR/ Examiner.Art Unit 2817 (Assistant Examiner)	07/22/2015 (Date)	Total Claims Allowed: 11	
(Primary Examiner)	(Date)	O.G. Print Claim(s) 1	O.G. Print Figure 25

Issue Classification 	Application/Control No. 13992598	Applicant(s)/Patent Under Reexamination ROSENBAUM ET AL.
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☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
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	2		18	11											
	3		19												
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	14	7													
	15	8													
	16	9													

/SAMUEL LAIR/ Examiner.Art Unit 2817 (Assistant Examiner)	07/22/2015 (Date)	Total Claims Allowed: 11	
(Primary Examiner)	(Date)	O.G. Print Claim(s) 1	O.G. Print Figure 25



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
13/992,598	06/07/2013	2817	2300	P38683US	25	4

CONFIRMATION NO. 5215

CORRECTED FILING RECEIPT



0000000076963174

92265
Winkle, PLLC
c/o CPA Global
P.O. Box 52050
Minneapolis, MN 55402

Date Mailed: 08/20/2015

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Aaron W. Rosenbaum, Portland, OR;
Din-How Mei, Portland, OR;
Sameer S. Pradhan, Portland, OR;

Applicant(s)

Aaron W. Rosenbaum, Portland, OR;
Din-How Mei, Portland, OR;
Sameer S. Pradhan, Portland, OR;

Assignment For Published Patent Application

Intel Corporation, Santa Clara, CA

Power of Attorney: The patent practitioners associated with Customer Number 92265

Domestic Priority data as claimed by applicant

This application is a 371 of PCT/US11/54464 09/30/2011

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.) - None.

Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access - A proper **Authorization to Permit Access to Application by Participating Offices** (PTO/SB/39 or its equivalent) has been received by the USPTO.

If Required, Foreign Filing License Granted: 06/15/2013

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/992,598**

Projected Publication Date: Not Applicable

Non-Publication Request: No

Early Publication Request: No
Title

CAPPING DIELECTRIC STRUCTURE FOR TRANSISTOR GATES

Preliminary Class

257

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER
Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit <http://www.SelectUSA.gov> or call +1-202-482-6800.

Issue Classification 	Application/Control No. 13992598	Applicant(s)/Patent Under Reexamination ROSENBAUM ET AL.	
	Examiner SAMUEL LAIR	Art Unit 2817	

CPC						
Symbol					Type	Version
H01L		21	/	28247	F	2013-01-01
H01L		29	/	66545	I	2013-01-01
H01L		29	/	66795	I	2013-01-01
H01L		2029	/	7858	A	2013-01-01
H01L		29	/	785	I	2013-01-01
H01L		21	/	76897	A	2013-01-01
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CPC Combination Sets				
Symbol	Type	Set	Ranking	Version

/SAMUEL LAIR/ Examiner.Art Unit 2817 (Assistant Examiner)	08/31/2015 (Date)	Total Claims Allowed: 11	
/ANTHONY HO/ Primary Examiner.Art Unit 2817 (Primary Examiner)	09/01/2015 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 25

Issue Classification 	Application/Control No. 13992598	Applicant(s)/Patent Under Reexamination ROSENBAUM ET AL.
	Examiner SAMUEL LAIR	Art Unit 2817

US ORIGINAL CLASSIFICATION						INTERNATIONAL CLASSIFICATION													
CLASS		SUBCLASS				CLAIMED					NON-CLAIMED								
						H	O	1	L	21 / 28 (2006.01.01)									
CROSS REFERENCE(S)																			
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)																		

/SAMUEL LAIR/ Examiner.Art Unit 2817 (Assistant Examiner)	08/31/2015 (Date)	Total Claims Allowed: 11	
/ANTHONY HO/ Primary Examiner.Art Unit 2817 (Primary Examiner)	09/01/2015 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 25

Issue Classification 	Application/Control No. 13992598	Applicant(s)/Patent Under Reexamination ROSENBAUM ET AL.
	Examiner SAMUEL LAIR	Art Unit 2817

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
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	2	4	18												
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/SAMUEL LAIR/ Examiner.Art Unit 2817 (Assistant Examiner)	08/31/2015 (Date)	Total Claims Allowed: 11	
/ANTHONY HO/ Primary Examiner.Art Unit 2817 (Primary Examiner)	09/01/2015 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 25



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/992,598	06/07/2013	Aaron W. Rosenbaum	P38683US	5215

92265	7590	09/08/2015
Winkle, PLLC c/o CPA Global P.O. Box 52050 Minneapolis, MN 55402		

EXAMINER	
LAIR, SAMUEL L	

ART UNIT	PAPER NUMBER
2817	

NOTIFICATION DATE	DELIVERY MODE
09/08/2015	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

winkle@cableone.net
inteldocs_docketing@cpaglobal.com

Corrected Notice of Allowability	Application No. 13/992,598	Applicant(s) ROSENBAUM ET AL.	
	Examiner SAMUEL LAIR	Art Unit 2817	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to communications filed 16 July 2015.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 15-25. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a) ☐ All b) ☐ Some *c) ☐ None of the:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. _____.

3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892) 2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____ 3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material 4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____	5. ☐ Examiner's Amendment/Comment 6. ☐ Examiner's Statement of Reasons for Allowance 7. ☐ Other _____
--	--

/ANTHONY HO/ Primary Examiner, Art Unit 2817	/SAMUEL LAIR/ Examiner, Art Unit 2817
---	--

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

92265 7590 07/31/2015
Winkle, PLLC
c/o CPA Global
P.O. Box 52050
Minneapolis, MN 55402

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

13/992,598 06/07/2013 Aaron W. Rosenbaum P38683US 5215

TITLE OF INVENTION: CAPPING DIELECTRIC STRUCTURE FOR TRANSISTOR GATES

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
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nonprovisional UNDISCOUNTED \$960 \$0 \$0 \$960 11/02/2015

EXAMINER	ART UNIT	CLASS-SUBCLASS
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LAIR, SAMUEL L 2817 257-288000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☒ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively, 1 Winkle, PLLC
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
- 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Intel Corporation

Santa Clara, CA

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☒ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number 50-4238 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Robert G. Winkle/

Date October 28, 2015

Typed or printed name Robert G. Winkle

Registration No. 37,474

"FEE ADDRESS" INDICATION FORM

Address to:
Mail Stop M Correspondence
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Fax to:
571-273-6500

- OR -

INSTRUCTIONS: The issue fee must have been paid for application(s) listed on this form. In addition, only an address represented by a Customer Number can be established as the fee address for maintenance fee purposes (hereafter, fee address). A fee address should be established when correspondence related to maintenance fees should be mailed to a different address than the correspondence address for the application. **When to check the first box below:** If you have a Customer Number to represent the fee address. **When to check the second box below:** If you have no Customer Number representing the desired fee address, in which case a completed Request for Customer Number (PTO/SB/125) must be attached to this form. For more information on Customer Numbers, see the Manual of Patent Examining Procedure (MPEP) § 403.

For the following listed application(s), please recognize as the "Fee Address" under the provisions of 37 CFR 1.363 the address associated with:



Customer Number:

000197

OR



The attached Request for Customer Number (PTO/SB/125) form.

PATENT NUMBER (if known)	APPLICATION NUMBER
	13/992,598

Completed by (check one):



Applicant/Inventor

/Robert G. Winkle/

Signature



Attorney or Agent of record 37,474

(Reg. No.)

Robert G. Winkle

Typed or printed name



Assignee of record of the entire interest. See 37 CFR 3.71.
Statement under 37 CFR 3.73(b) is enclosed.
(Form PTO/SB/96)

208-850-3104

Requester's telephone number



Assignee recorded at Reel _____ Frame _____

October 28, 2015

Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.



* Total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.363. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 5 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND COMPLETE D FORMS TO THIS ADDRESS. **SEND TO: Mail Stop M Correspondence, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal				
Application Number:		13992598		
Filing Date:		07-Jun-2013		
Title of Invention:		CAPPING DIELECTRIC STRUCTURE FOR TRANSISTOR GATES		
First Named Inventor/Applicant Name:		Aaron W. Rosenbaum		
Filer:		Robert G. Winkle		
Attorney Docket Number:		P38683US		
Filed as Large Entity				
Filing Fees for U.S. National Stage under 35 USC 371				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl Issue Fee	1501	1	960	960

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				960

Electronic Acknowledgement Receipt

EFS ID:	23923547
Application Number:	13992598
International Application Number:	
Confirmation Number:	5215
Title of Invention:	CAPPING DIELECTRIC STRUCTURE FOR TRANSISTOR GATES
First Named Inventor/Applicant Name:	Aaron W. Rosenbaum
Customer Number:	92265
Filer:	Robert G. Winkle
Filer Authorized By:	
Attorney Docket Number:	P38683US
Receipt Date:	28-OCT-2015
Filing Date:	07-JUN-2013
Time Stamp:	20:02:28
Application Type:	U.S. National Stage under 35 USC 371

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$ 960
RAM confirmation Number	7197
Deposit Account	504238
Authorized User	WINKLE, ROBERT G.
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. 1.492 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	P38683US_Issue_Fee_Transmit tal.pdf	88100	no	1
			e3f72057a8522032c3803447a6b8d5dac9a d5a9e		
Warnings:					
Information:					
2	Maintenance Fee Address Change	P38683US_FAC.pdf	312568	no	2
			3b04eb8a5c454e083a8007059618f1db217 d6058		
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	30575	no	2
			2e3082cbc343684d0c7c3fe864e769be40d 9feed		
Warnings:					
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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/992,598	12/01/2015	9202699	P38683US	5215
92265	7590	11/11/2015		
Winkle, PLLC c/o CPA Global P.O. Box 52050 Minneapolis, MN 55402				

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 255 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Aaron W. Rosenbaum, Portland, OR;
Din-How Mei, Portland, OR;
Sameer S. Pradhan, Portland, OR;

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AO 120 (Rev. 08/10)

TO: Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
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In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been
filed in the U.S. District Court Eastern District of Texas on the following

☐ Trademarks or ☐ Patents. (☐ the patent action involves 35 U.S.C. § 292.);

DOCKET NO. 2:22cv353	DATE FILED 9/12/2022	U.S. DISTRICT COURT Eastern District of Texas
PLAINTIFF Daedalus Prime LLC		DEFENDANT Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., Samsung Semiconductor, Inc., and Samsung Austin Semiconductor, LLC
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 10,541,334	1/21/2020	Daedalus Prime LLC
2 9,202,699	12/1/2015	Daedalus Prime LLC
3 10,727,183	7/28/2020	Daedalus Prime LLC
4 9,627,321	4/18/2017	Daedalus Prime LLC
5		

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE
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Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy