

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.
Petitioner

v.

DAEDALUS PRIME LLC
Patent Owner

Patent No. 9,202,699

**PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 9,202,699**

TABLE OF CONTENTS

I.	INTRODUCTION	1
II.	MANDATORY NOTICES UNDER 37 C.F.R. § 42.8.....	1
	Real Parties-in-Interest	1
	Related Matters	1
	Counsel and Service Information	1
III.	PAYMENT OF FEES UNDER 37 C.F.R. § 42.15(a)	2
IV.	GROUND FOR STANDING.....	2
V.	PRECISE RELIEF REQUESTED AND GROUNDS RAISED.....	2
VI.	LEVEL OF ORDINARY SKILL IN THE ART	4
VII.	OVERVIEW OF THE '699 PATENT	5
VIII.	CLAIM CONSTRUCTION	7
IX.	Detailed Explanation of Unpatentability	8
A.	Ground 1 – Cappellani in View of Siddiqui Renders Claims 1, 2, and 5-11 Obvious	8
1.	Claim 1	8
2.	Claim 2	37
3.	Claim 5	37
4.	Claim 6	38
5.	Claim 7	41
6.	Claim 8	44
7.	Claim 9	45
8.	Claim 10	47

9.	Claim 11	48
B.	Ground 2 – Cappellani in View of Siddiqui and Park Renders Claims 1, 2, and 4-11 Obvious	48
1.	Claims 1, 2, and 5-11	48
2.	Claim 4	51
C.	Ground 3 – Brask in View of Cheng Renders Claims 1, 2, and 5-11 Obvious	52
1.	Claim 1	52
2.	Claim 2	69
3.	Claim 5	70
4.	Claim 6	70
5.	Claim 7	72
6.	Claim 8	73
7.	Claim 9	74
8.	Claim 10	75
9.	Claim 11	76
D.	Ground 4 – Brask in View of Cheng and Park Renders Claims 1, 2, and 4-11 Obvious	76
1.	Claims 1, 2, and 5-11	76
2.	Claim 4	78
E.	Ground 5 – Brask in View of Siddiqui Renders Claims 1, 2, and 5-11 Obvious	79
1.	Claim 1	79
2.	Claim 2	84

3.	Claim 5	84
4.	Claim 6	84
5.	Claim 7	85
6.	Claim 8	85
7.	Claim 9	85
8.	Claim 10	85
9.	Claim 11	86
F.	Ground 6 – Brask in View of Siddiqui and Park Renders Claims 1, 2, and 4-11 Obvious	86
1.	Claims 1, 2, and 5-11	86
2.	Claim 4	88
X.	Discretionary Denial is not Appropriate.....	89
A.	The Board Should Not Deny Institution Under <i>Fintiv</i>	89
XI.	Conclusion	91

LIST OF EXHIBITS

Ex. 1001	U.S. Patent No. 9,202,699
Ex. 1002	Declaration of Dr. Stanley Shanfield
Ex. 1003	Curriculum Vitae of Dr. Stanley Shanfield
Ex. 1004	File History of U.S. Patent No. 9,202,699
Ex. 1005	U.S. Patent Publication No. 2011/0147842 to Cappellani <i>et al.</i> (“Cappellani”)
Ex. 1006	U.S. Patent Publication No. 2011/0298061 to Siddiqui <i>et al.</i> (“Siddiqui”)
Ex. 1007	U.S. Patent Publication No. 2011/0108930 to Cheng <i>et al.</i> (“Cheng”)
Ex. 1008	U.S. Patent Publication No. 2005/0148137 to Brask <i>et al.</i> (“Brask”)
Ex. 1009	Hisamoto <i>et al.</i> , <u>FinFET—A Self-Aligned Double-Gate MOSFET Scalable to 20 nm</u> , IEEE Transactions on Electron Devices, Vol. 47, No. 12, Dec. 2000 (“Hisamoto”)
Ex. 1010	U.S. Patent No. 8,951,853 to Park <i>et al.</i> (“Park”)
Ex. 1011	U.S. Patent No. 7,858,421 to Chen <i>et al.</i> (“Chen”)
Ex. 1012	U.S. Patent No. 8,558,336 to Su <i>et al.</i> (“Su”)
Ex. 1013	U.S. Patent No. to Kikuchi <i>et al.</i> (“Kikuchi”)
Ex. 1014	U.S. Patent Publication No. 2010/0173479 to Joo (“Joo”)
Ex. 1015	U.S. Patent 6,802,944 to Ahmad <i>et al.</i> (“Ahmad”)
Ex. 1016	U.S. Patent 6,500,771 to Vassiliev <i>et al.</i> (“Vassiliev”)
Ex. 1017	Plummer <i>et al.</i> , <u>Silicon VLSI Technology, Fundamentals, Practice and Modeling</u> , 2000 (“Plummer”)

Ex. 1018	Leobandung <i>et al.</i> , <u>Wire-Channel and Wrap-Around-Gate Metal-Oxide-Semiconductor Field-Effect Transistors with a Significant Reduction of Short Chanel Effects</u> , J. Vac. Sci. Technol. B 15(6), Nov/Dec 1997 (“Leobandung”)
Ex. 1019	Tang <i>et al.</i> , <u>FinFET – A Quasi-Planar Double-Gate MOSFET</u> , 2001 IEEE International Solid-State Circuits Conference, 2001 (“Tang”)
Ex. 1020	U.S. Patent Publication No. 2010/0038715 to Babich <i>et al.</i> (“Babich”)
Ex. 1021	U.S. Patent Publication No. 2009/0065877 to Tshchiaki (“Tshchiaki-877”)
Ex. 1022	U.S. Patent Publication No. 2004/0256645 to Tshchiaki <i>et al.</i> (“Tshchiaki-645”)
Ex. 1023	U.S. Patent Publication No. 2009/0057730 to Furukawa <i>et al.</i> (“Furukawa”)
Ex. 1024	U.S. Patent Publication No. 2008/0203440 to Tshchiaki (“Tshchiaki-440”)
Ex. 1025	Wolf, <u>Silicon Processing for the VLSI Era, Vol. 3: The Submicron MOSFET</u> , 1995 (“Wolf”)
Ex. 1026	Neaman, <u>Semiconductor Physics and Devices (Third Edition)</u> , 2003 (“Neaman”)
Ex. 1027	RESERVED
Ex. 1028	Docket Control Order (dated Dec. 12, 2022)

I. INTRODUCTION

Samsung Electronics Co., Ltd. (“Petitioner” or “Samsung”) requests *inter partes* review of claims 1, 2, and 4-11 (“the challenged claims”) of U.S. Patent No. 9,202,699 (“the ’699 patent”) (Ex. 1001), which, according to PTO records, is assigned to Daedalus Prime LLC (“Patent Owner” or “PO”). For the reasons discussed below, the challenged claims should be found unpatentable and canceled.

II. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8

Real Parties-in-Interest

Petitioner identifies the following as the real parties-in-interest: Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., Samsung Semiconductor, Inc., and Samsung Austin Semiconductor, LLC.

Related Matters

The ’699 patent is at issue in *Daedalus Prime LLC v. Samsung Electronics Co., Ltd. et al*, Case No. 2:22-CV-00353.

Counsel and Service Information

Lead counsel is Naveen Modi (Reg. No. 46,224), and Backup counsel are (1) Joseph E. Palys (Reg. No. 46,508), (2) Paul M. Anderson (Reg. No. 39,896), and (3) Howard Herr (*pro hac vice* to be filed). Service information is Paul Hastings LLP, 2050 M St., Washington, D.C., 20005, Tel.: 202.551.1700, Fax: 202.551.1705,

email: PH-Samsung-Daedalus-IPR@paulhastings.com. Petitioner consents to electronic service.

III. PAYMENT OF FEES UNDER 37 C.F.R. § 42.15(a)

The PTO is authorized to charge any fees due during this proceeding to Deposit Account No. 50-2613.

IV. GROUNDS FOR STANDING

Petitioner certifies that the '699 patent is available for review and Petitioner is not barred/estopped from requesting review on the grounds identified herein.

V. PRECISE RELIEF REQUESTED AND GROUNDS RAISED

Claims 1, 2, and 4-11 should be canceled as unpatentable based on the following grounds:

Ground 1: Claims 1, 2, and 5-11 are obvious under Pre-AIA 35 U.S.C. § 103 based on Cappellani (Ex. 1005) in view of Siddiqui (Ex. 1006);

Ground 2: Claims 1, 2, and 4-11 are obvious are obvious under Pre-AIA 35 U.S.C. § 103 based on Cappellani in view Siddiqui and Park (Ex. 1010);

Ground 3: Claims 1, 2, and 5-11 are obvious under Pre-AIA 35 U.S.C. § 103 based on Brask (Ex. 1008) in view of Cheng (Ex. 1007);

Ground 4: Claims 1, 2, and 4-11 are obvious are obvious under Pre-AIA 35 U.S.C. § 103 based on Brask in view Cheng and Park;

Ground 5: Claims 1, 2, and 5-11 are obvious under Pre-AIA 35 U.S.C. § 103 based on Brask in view of Siddiqui; and

Ground 6: Claims 1, 2, and 4-11 are obvious are obvious under Pre-AIA 35 U.S.C. § 103 based on Brask in view Siddiqui and Park.¹

The '699 patent issued December 1, 2015, from U.S. App. No. 13/992,598 (“the '598 application”) and claims priority back to International Application PCT/US2011/054464 (“the '464 PCT application”) filed September 30, 2011.

Cappellani published June 23, 2011. Siddiqui was filed June 8, 2010 and published December 8, 2011. Cheng published May 12, 2011 from an application filed November 12, 2009. Brask published July 7, 2005. Park issued February 10, 2015 from an application filed March 10, 2010. Therefore, Cappellani is prior art under at least pre-AIA 35 U.S.C. § 102(a), Brask is prior art under at least pre-AIA 35 U.S.C. § 102(b), Siddiqui and Park are prior art under at least pre-AIA 35 U.S.C. § 102(e), and Cheng is prior art under at least pre-AIA 35 U.S.C. § 102(a) and § 102(e).

¹ Other references discussed herein are provided to show the state of the art at the time of the alleged invention of the '699 patent.

Cheng was cited in an IDS submitted during prosecution of the '598 application (Ex. 1004, 586, 843), but was never applied by the Examiner, much less in combination with Brask. None of the remaining references or the obviousness combinations relied upon in this Petition were before, or applied by, the examiner during prosecution. The combinations presented in this Petition have the support of expert testimony (Ex. 1002), which the Examiner did not have the benefit of during prosecution. Accordingly, the prior art combinations and arguments presented in this Petition were never previously presented to the Office.

VI. LEVEL OF ORDINARY SKILL IN THE ART

A person of ordinary skill in the art (“POSITA”) at the time of the alleged invention of the '699 patent would have had a bachelor’s degree in a field relating to the semiconductor manufacturing process like materials science, physics, electrical engineering, or other related subjects, and at least two to three years of experience with fabrication of integrated circuits. (Ex. 1002, ¶¶16-17.)² More education can supplement practical experience and vice versa. (*Id.*)

² Petitioner submits the declaration of Dr. Stanley Shanfield (Ex. 1002), an expert in the field of the '699 patent. (*Id.*, ¶¶3-15; Ex. 1003.)

VII. OVERVIEW OF THE '699 PATENT

The '699 patent is entitled “Capping Dielectric Structure for Transistor Gates” and describes the formation of a self-aligned contact for a non-planar FinFET transistor, where the transistor is fabricated using a sacrificial gate. (Ex. 1001, Title, 3:52-4:11, 5:8-11, 7:52; Ex. 1002, ¶¶32-39.) As shown in annotated figures 16 and 19 below, forming the self-aligned contact includes recessing the conductive gate material for the gate and forming a capping dielectric material 166 in the recessed area. (*Id.*, 6:4-29, 7:21-26.)

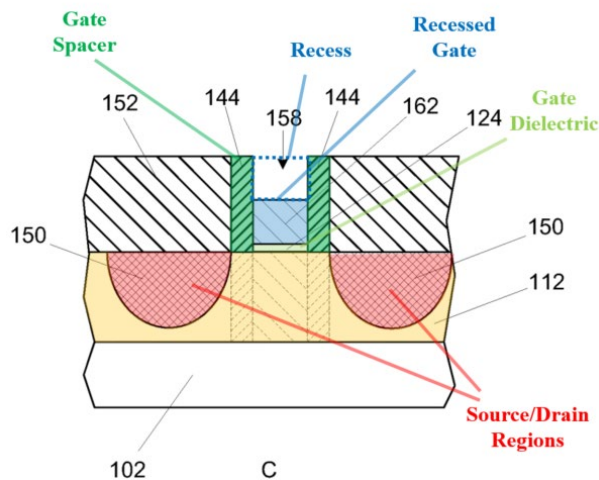


FIG. 16

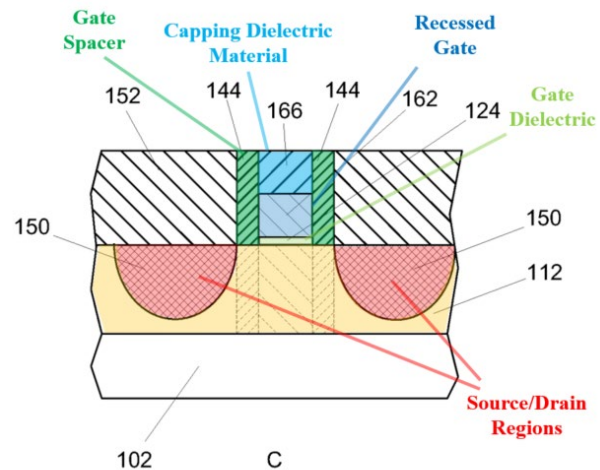


FIG. 19

(Ex. 1001, FIGs. 16, 19 (annotated); Ex. 1002, ¶¶35-36.)

As shown in annotated figure 22 below, after depositing additional dielectric material layer 168, selective etching is used to form the contact opening 182 to the source/drain region, where the selective etching removes dielectric material 152 and

168 faster than the dielectric material of the gate spacer 144 and cap 166. (Ex. 1001, 7:30-51.)

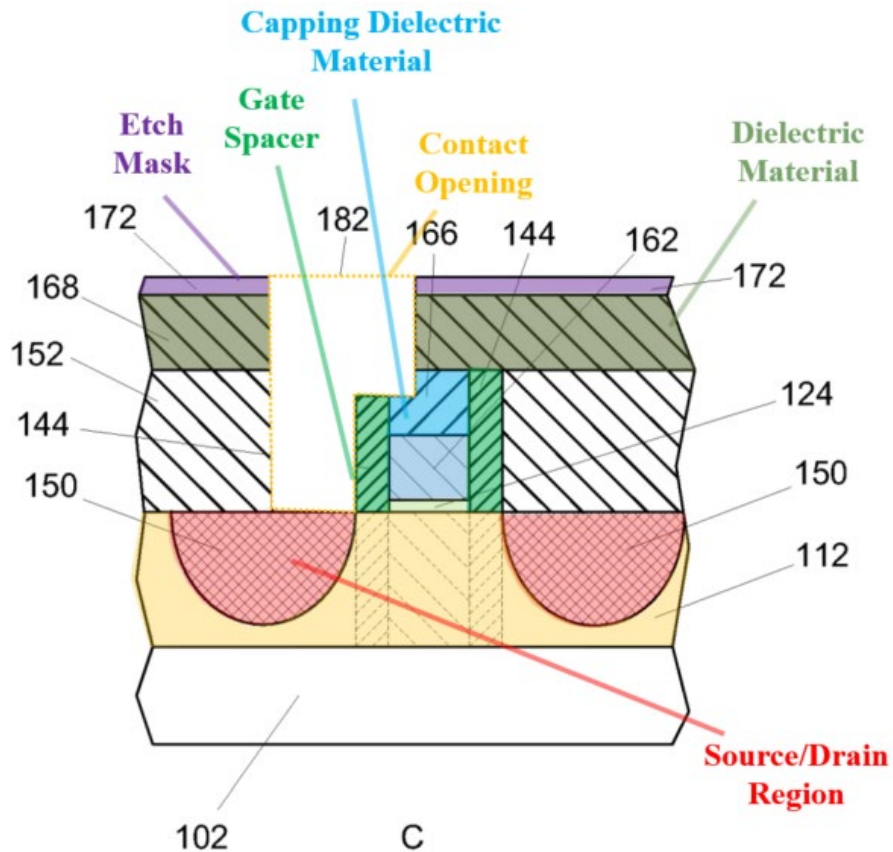


FIG. 22

(*Id.*, FIG. 22 (annotated); Ex. 1002, ¶38.)

As shown in figure 25 below, conductive contact material 188 is deposited in the contact opening 182 to form the self-aligned source/drain contact 190. (Ex. 1001, 7:53-54, 7:65-8:1.)

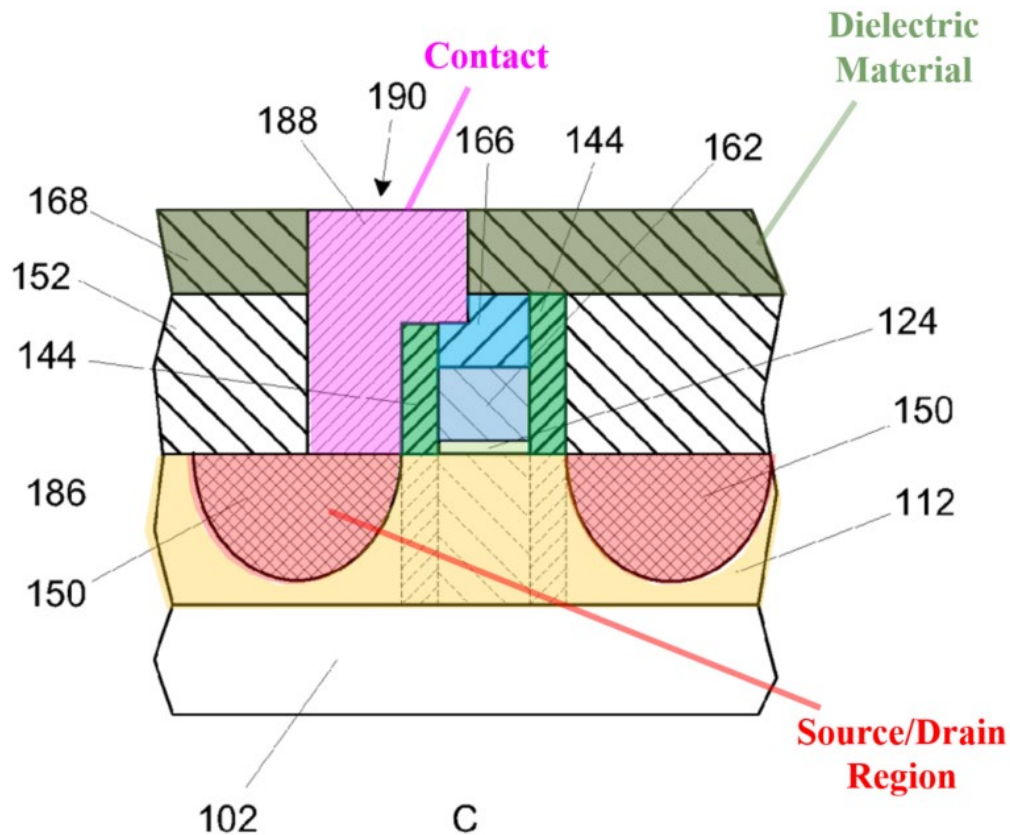


FIG. 25

(*Id.*, FIG. 25 (annotated); Ex. 1002, ¶39.)

VIII. CLAIM CONSTRUCTION

For IPR proceedings, the Board applies the claim construction standard according to *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). See 83 Fed. Reg. 51,340-59 (Oct. 11, 2018). Under *Phillips*, claim terms are typically given their ordinary and customary meanings, as would have been understood by a POSITA at the time of the invention. *Phillips*, 415 F.3d at 1313; see also *id.*, 1312-

16. The Board, however, only construes the claims when necessary to resolve the underlying controversy. *Toyota Motor Corp. v. Cellport Systems, Inc.*, IPR2015-00633, Paper No. 11 at 16 (Aug. 14, 2015) (citing *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)). (Ex. 1002, ¶40.)

IX. Detailed Explanation of Unpatentability

A. Ground 1 – Cappellani in View of Siddiqui Renders Claims 1, 2, and 5-11 Obvious

1. Claim 1

a) “A method comprising:”

To the extent the preamble is limiting, Cappellani discloses a “method.” (Ex. 1002, ¶¶41-45, 60-61.) Cappellani discloses a method for “forming epitaxial source and drain extensions in a multi-gate MOS device (e.g., ‘finfet’),” where a sacrificial gate stack is removed before forming a replacement metal gate. (Ex. 1005, ¶[0022] (“Described herein are systems and methods of forming epitaxial source and drain extensions in a multi-gate MOS device (e.g., ‘finfet’).”), ¶[0026] (“In the exemplary embodiment, the gate stack 217 is sacrificial and subsequently removed for a replacement metal gate process.”).) Such a method is further discussed below for claim elements 1[b]-1[l]. (Sections IX.A.1(b)-(l).) Figure 2A of Cappellani shows the multi-gate finfet MOS device at an early stage of formation. (Ex. 1005, ¶¶[0007], [0026]; Ex. 1002, ¶61.)

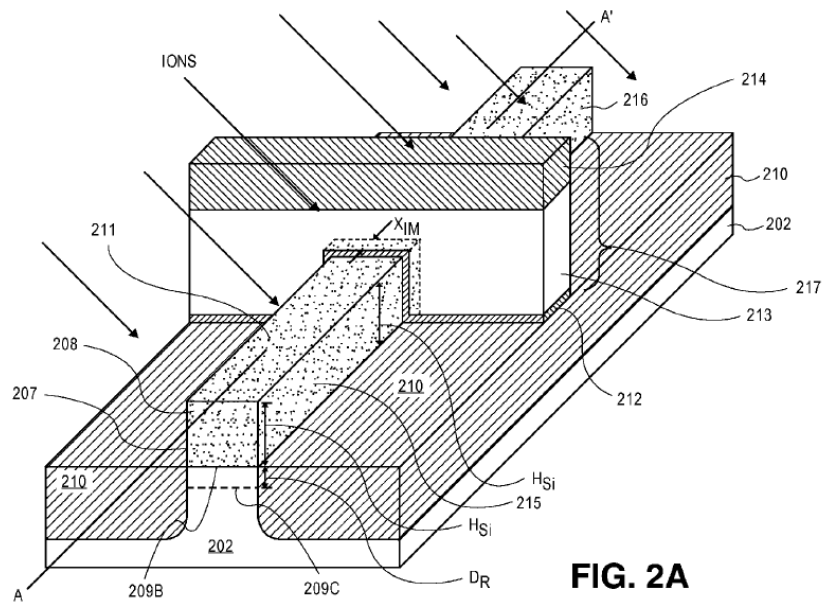
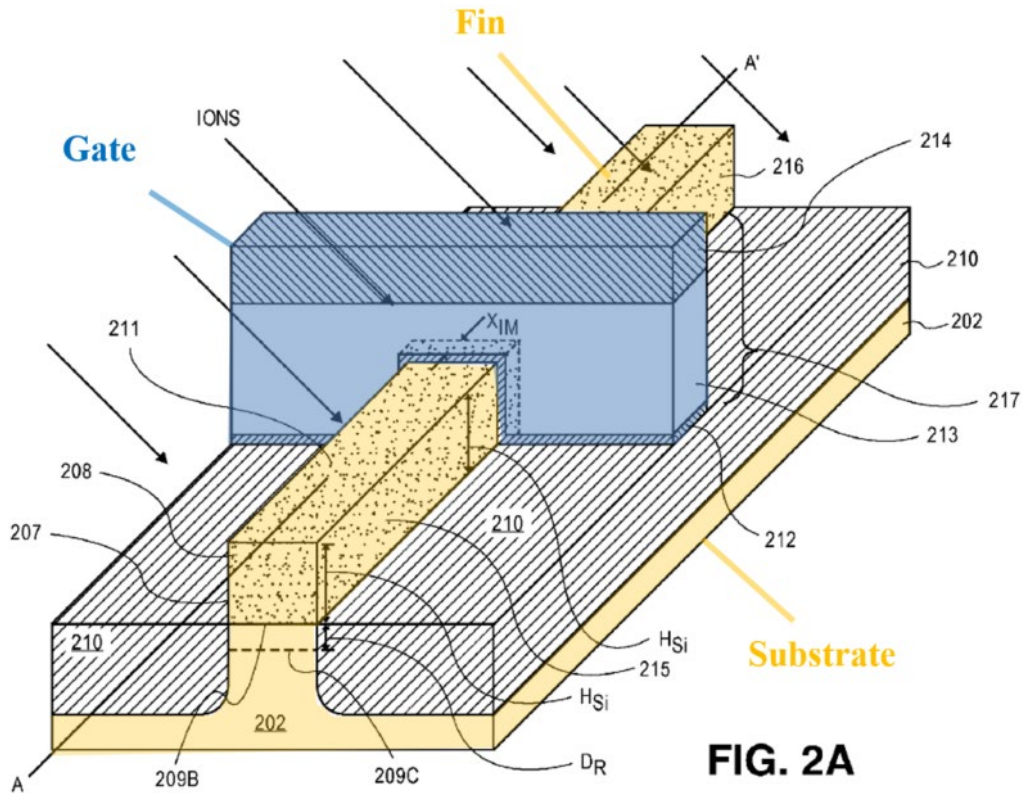


FIG. 2A

(Ex. 1005, FIG. 2A.)

b) “forming a sacrificial non-planar transistor gate over a non-planar transistor fin;”

Cappellani discloses this claim feature. (Ex. 1002, ¶¶62-63.) As shown in annotated figure 2A below, Cappellani discloses forming a sacrificial gate stack 217 (“sacrificial non-planar transistor gate”), which includes a gate dielectric 212, a gate electrode 213, and a gate cap 214, over the semiconductor non-planar fin for the multi-gate transistor. (Ex. 1005, ¶[0026] (“FIG. 2A is an isometric view of a gate stack formed over a semiconductor fin”), ¶[0007], ¶[0026] (“gate stack 217 is sacrificial and subsequently removed for replacement gate process.”), ¶[0028]; Ex. 1002, ¶¶62-63.)



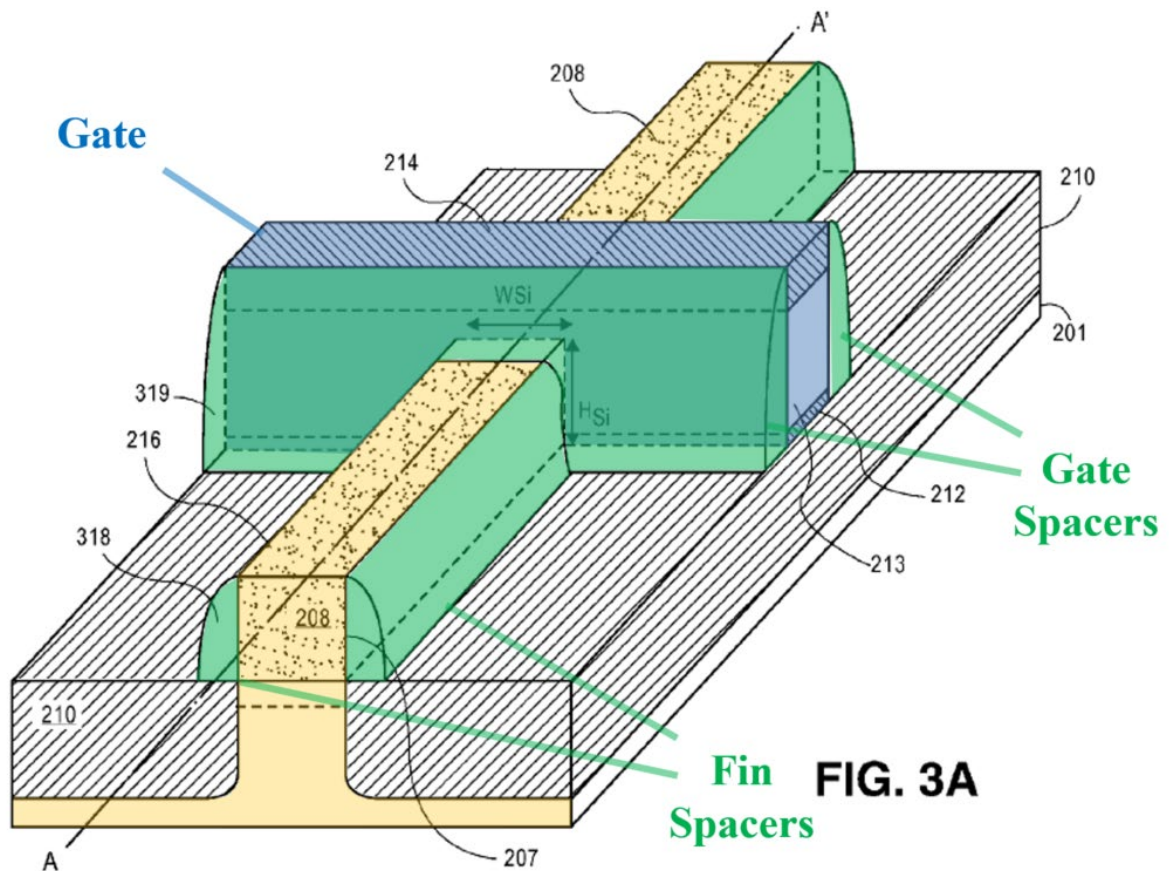
(Ex. 1005, FIG 2A (annotated); Ex. 1002, ¶62.)

c) “depositing a dielectric material layer over the sacrificial non-planar transistor gate and the non-planar transistor fin;”

d) “forming non-planar transistor gate spacers from a portion of the dielectric material layer adjacent the sacrificial non-planar transistor gate;”

Cappellani in view of Siddiqui discloses or suggests these limitations. (Ex. 1002, ¶¶64-75.) As shown in annotated figures 3A and 3B below, Cappellani discloses forming dielectric material gate stack spacers 319 (“non-planar transistor gate spacers”) adjacent to the sacrificial gate. (Ex. 1005, ¶[0032] (“spacers are

formed on either side of the gate stack and the semiconductor fin. The spacers may be formed using conventional dielectric materials, including but not limited to silicon oxide or silicon nitride. ... gate stack spacer 319 formed on sidewalls of the gate stack 217"); Ex. 1002, ¶64.)



(Ex. 1005, FIG. 3A; Ex. 1002, ¶64.)

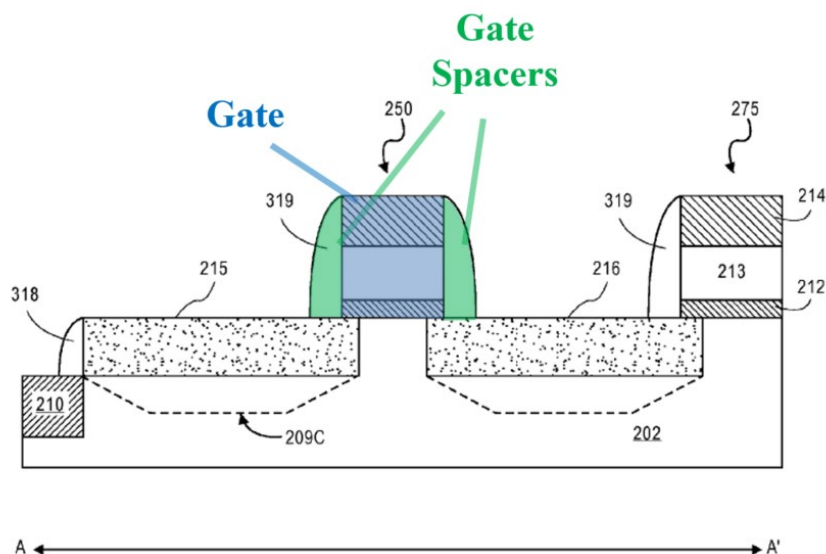


FIG. 3B

(Ex. 1005, FIG. 3B; Ex. 1002, ¶64.)

Cappellani does not explicitly disclose forming the gate spacers by first depositing the dielectric material for the spacers over the sacrificial gate and fin and then forming the spacers from that dielectric material. (Ex. 1002, ¶65.) However, formation of gate spacers using blanket deposition of the dielectric material followed by etching was a well-known and widely-used technique for gate spacer formation, and a POSITA would have found it obvious to form Cappellani's gate spacers in such a manner. (Ex. 1008, ¶[0065] ("sidewall spacers 612 can be formed along opposite sidewalls of the sacrificial gate electrodes 604 and 606 ... by any **well**

known techniques,³ such as by blanket depositing the conformal sidewall spacer dielectric over the substrate including the top surface and sidewalls of the sacrificial gate electrodes 604 and 606 as well as on the top surface and sidewalls of semiconductor bodies 510 and 512 as well as onto the exposed surface of the insulating substrate. ... The dielectric spacer material is then anisotropically etched back to remove the dielectric spacer material from a horizontal surface (e.g., top surface) of the sacrificial gate electrodes 604 and 606 and the top surface of the semiconductor bodies 510 and 512 and insulating substrate 602, while leaving spacer material on the vertical surfaces (e.g., sidewalls) of sacrificial gate electrodes 604 and 606 to form sidewall spacers 612”), ¶[0053] (“Spacers 540 can be formed by **blanket depositing** a conformal dielectric film, such as but not limited to silicon nitride, silicon oxide, silicon oxynitride or combination thereof over the substrate include the gate electrodes 526 and 528 and semiconductor bodies 510 and 512. ... Next, the dielectric film is anisotropically **etched** by, for example, plasma etching or reactive ion etching to form the sidewall spacers 540.”); Ex. 1023, ¶[0016] (“Nitride spacers 122 are formed by depositing conformal silicon nitride layer

³ Emphasis added unless otherwise noted.

followed by directional RIE of nitride to etch off the nitride on the horizontal surface leaving the nitride spacer on the vertical surfaces of gate stack.”); Ex. 1007, ¶[0039]; Ex. 1022, ¶[0075]; Ex. 1021, ¶[0106]; Ex. 1024 ¶[0072]; Ex. 1011, 4:28-34; Ex. 1013, 5:40-43; Ex. 1002, ¶65.) Indeed, forming gate spacers using conformal deposition followed by anisotropic etching was well-known long before the alleged invention date. (Ex. 1025, 595-596 (“A conformal deposition process produces a thicker film at the edge of the gate-to-active area step than on flat areas. Thus, an anisotropic dry-etch process will clear the oxide in the flat areas while leaving spacers at the sidewalls of the poly gate.”), FIG. 9-31; Ex. 1002, ¶66.)

Blanket depositing the dielectric material over both the gate and the fin and then etching to form the spacers is consistent with Cappellani’s disclosure that the gate spacers and source/drain spacers are formed simultaneously. (Ex. 1005, ¶[0032] (“Formation of the gate stack spacer 319 also forms a fin spacer 318 on the sidewalls of the semiconductor fin”); Ex. 1002, ¶67.) As a POSITA would have appreciated, performing a blanket deposition over the entirety of the transistor structure and then using the same etching operation to produce the gate and fin spacers would have been an efficient method for forming both sets of spacers simultaneously. (Ex. 1002, ¶67.) Therefore, a POSITA would have been motivated to use such a well-known technique for forming the gate spacers. (*Id.*)

As a POSITA would have appreciated, using a blanket deposition and etching process for forming the spacers in a transistor like that disclosed by Cappellani would have been nothing more than the application of a known technique (forming spacers by blanket deposition and etching) to a similar structure (the transistor structure including the sacrificial gate stack and fin) to achieve a predictable result (gate spacers for the transistor). (Ex. 1002, ¶67.) *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007).

Moreover, to the extent PO argues that Cappellani alone does not disclose or suggest these claim features, they would have been obvious in view of Siddiqui. (Ex. 1002, ¶¶68-75.) Siddiqui discloses forming spacers on sidewalls of a gate structure in a transistor using a deposition and etch process, and, in view of Siddiqui and their knowledge of the state of the art, a POSITA would have found it obvious to form the spacers in a transistor like that disclosed by Cappellani by first blanket depositing dielectric material and then etching the dielectric material to form the spacers. (Ex. 1002, ¶68.)

Siddiqui, like Cappellani, discloses a transistor structure where a sacrificial gate is first formed, and then later removed and replaced with a functional gate structure. (Ex. 1006, Abstract, ¶[0022]; Ex. 1002, ¶69.) As shown in annotated figure 1 of Siddiqui below, protective dielectric layers 18 (i.e., spacers) are formed

on the sides of the replacement gate structure 4 of the transistor. (Ex. 1006, ¶[0018], ¶[0032] (“FIG. 1 further depicts forming a protective dielectric layer 18 on the sidewall of the replacement gate structure 4. ... In one embodiment, the protective dielectric layer 18 is provided by at least one spacer.”); Ex. 1002, ¶70.)

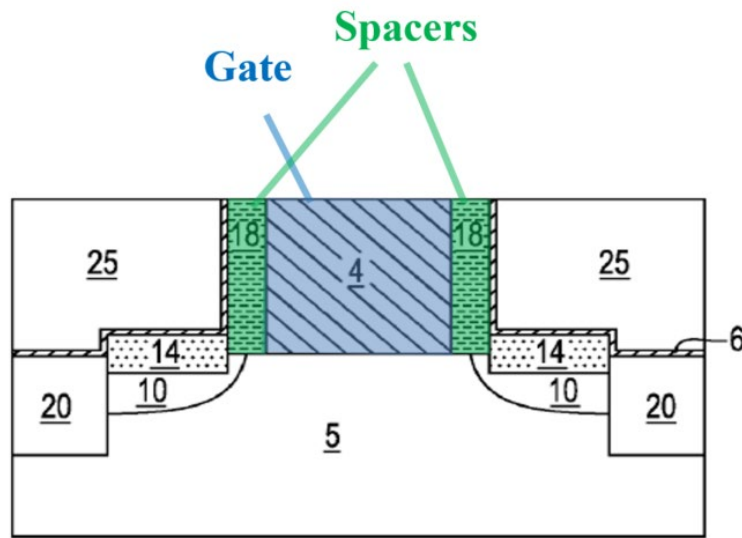


FIG. 1

(Ex. 1006, FIG. 1 (annotated); Ex. 1002, ¶70.)

Siddiqui further discloses that the spacers can be formed of silicon nitride using a deposition and etch process. (Ex. 1006, ¶[0033] (“The protective dielectric layer may be comprised of a dielectric material, such as a nitride, e.g., silicon nitride.”), ¶[0034], ¶[0032] (“The at least one spacer may be formed on the sidewall of the replacement gate structure 4 using **deposition and etch process**.”); Ex. 1002, ¶71.)

While Siddiqui does not expressly state that the deposition performed is a “blanket deposition” that covers the sacrificial gate and other structures of the transistor, a POSITA would have found it obvious to use such a blanket deposition in forming the gate spacers in a transistor like that of Cappellani. (Ex. 1002, ¶72.) As an initial matter, Siddiqui forms the spacers based on a deposition followed by an etch, which a POSITA would have understood to disclose or suggest using a blanket deposition because, as discussed above, using a blanket deposition followed by etching to form spacers was well-known and widely used. (*Id.*) Moreover, such an operation is simple and straightforward as opposed to other more complex options that might exist. (*Id.*) Furthermore, a POSITA would have been motivated to use a blanket deposition, which covers the sacrificial gate structure and the fins, followed by etching in order to be able to produce the gate and fin spacers in the same step as is disclosed by Cappellani. (*Id.*; Ex. 1005, ¶[0032].)

A POSITA implementing a transistor device like that disclosed by Cappellani would have looked to Siddiqui, particularly because Cappellani and Siddiqui are references in the same field and disclose transistor devices that utilize replacement gate structures with gate spacers on the sidewalls of the replacement gate structure. (Ex. 1002, ¶73.) Having looked to Siddiqui, such a POSITA would have found it obvious to form the gate spacers in a transistor like that disclosed by Cappellani

using a deposition and etch process like that disclosed by Siddiqui, where the deposition of the dielectric material (e.g., silicon nitride) deposits material over the sacrificial non-planar transistor gate and the non-planar transistor fin. (*Id.*)

Cappellani discloses that the spacers are formed of “conventional dielectric materials” including, for example, silicon nitride (Ex. 1005, ¶[0032]), but Cappellani does not disclose the details as to how the silicon nitride spacers are formed. (Ex. 1002, ¶74.) Therefore, having looked to Siddiqui, a POSITA would have found it obvious to use a deposition and etch technique as disclosed by Siddiqui to form the spacers in a transistor like that disclosed by Cappellani, where, in view of their knowledge of the state of the art, such a POSITA would have performed a blanket deposition as was common in spacer formation and would support Cappellani’s simultaneous formation of gate and fin spacers. (*Id.*)

Based on their knowledge of such well-known spacer formation techniques and Siddiqui’s disclosure of using deposition and etching to form the gate spacers, a POSITA would have had a reasonable likelihood of success. (*Id.*, ¶75.) To the extent PO argues that Siddiqui’s disclosure is limited to a planar MOS device and would not be applicable to a FinFET like that disclosed by Cappellani, such a position is contrary to what a POSITA would have understood at the time of the alleged invention. (*Id.*, ¶¶18-26, 75) While FinFET’s have more complex gate and

channel structures, it was well understood that they could be fabricated using conventional process technologies. (*Id.*; Ex. 1009, Abstract (“a novel self-aligned double-gate MOSFET, FinFET is proposed... the vertical double-gate MOSFETs can be fabricated relatively easily using the conventional planar MOSFET process technologies.”), 2324 (“In spite of its double-gate structure, FinFET is close to its root, the conventional MOSFET in terms of layout and fabrication.”); Ex. 1026, 449.) Indeed, the ’699 patent states that “[a]lthough embodiments herein are described in terms of non-planar transistors and replacement gate techniques, the subject matter is not so limited, as the subject matter may be used in planar transistors and in non-replacement gate applications” without any further explanation. (Ex. 1001, 3:47-51.) Such a statement supports the understanding that a POSITA would have understood that techniques for forming aspects of planar transistors are applicable to non-planar transistors and vice-versa. (Ex. 1002, ¶75.)

Therefore, the Cappellani-Siddiqui combination discloses or suggests claim elements 1[c] and 1[d].

e) “forming a source/drain region;”

The Cappellani-Siddiqui combination discloses or suggests this feature. (Ex. 1002, ¶76.) As shown in annotated figure 6A below, which is a cross-sectional view of a stage of fabrication of Cappellani’s multi-gate device, source/drain regions are

regrown (“formed”) using epitaxial deposition. (Ex. 1005, ¶[0040] (“the material forming the source/drain fin 618”), ¶[0041] (“The epitaxial deposition operation 114 therefore **regrows source/drain regions.**”); Ex. 1002, ¶76.)

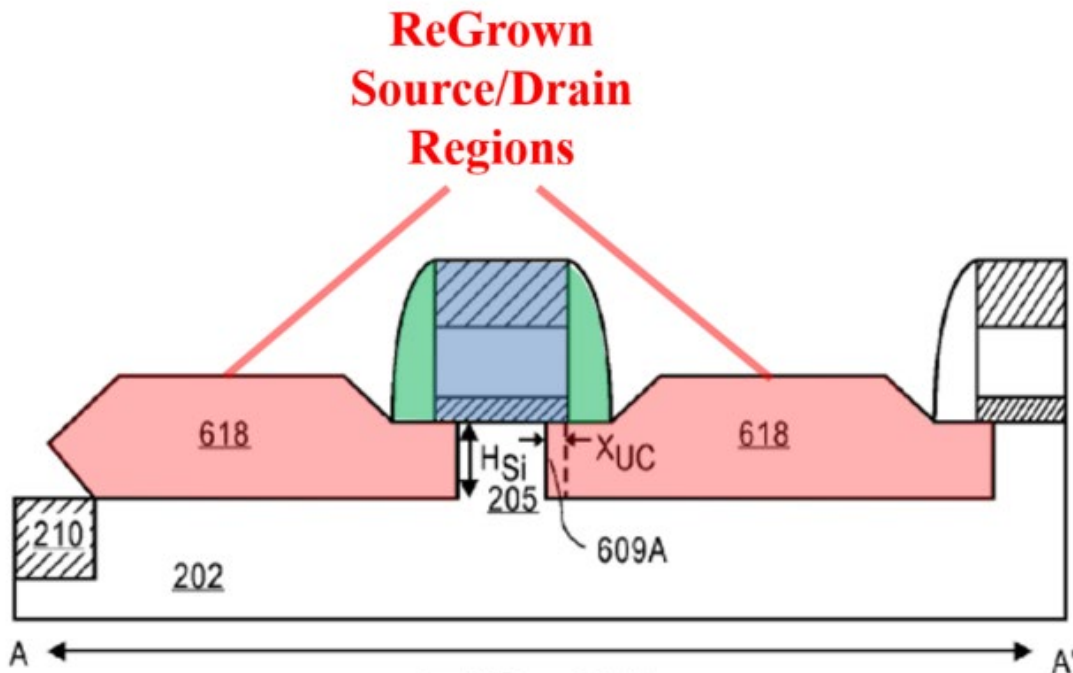


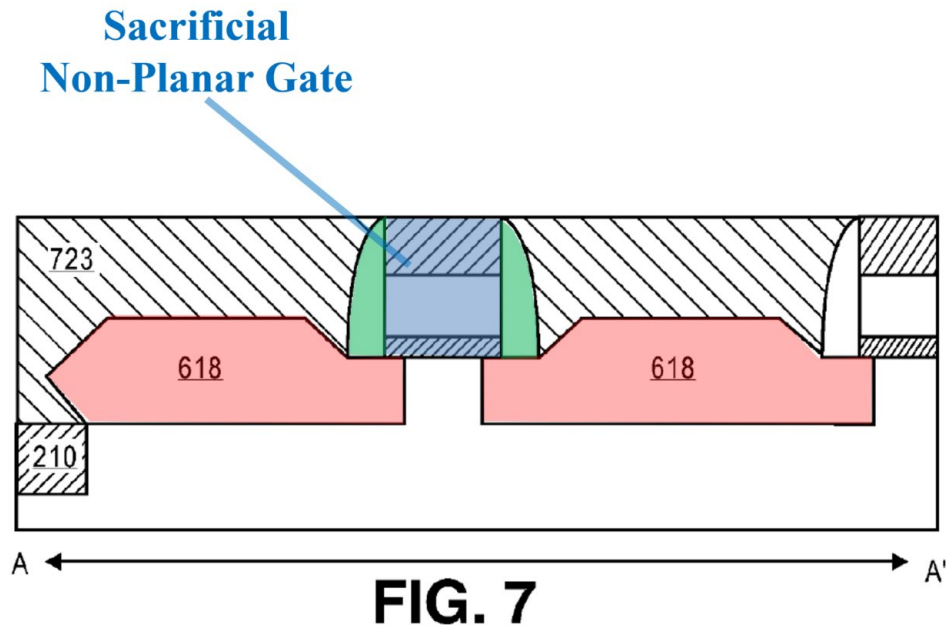
FIG. 6A

(Ex. 1005, FIG. 6A (annotated); Ex. 1002, ¶76.)

f) “removing the sacrificial non-planar transistor gate to form a gate trench between the non-planar transistor gate spacers and expose a portion of the non-planar transistor fin;”

The Cappellani-Siddiqui combination discloses or suggests these features. (Ex. 1002, ¶77.) Cappellani discloses removing the sacrificial gate structure (“sacrificial non-planar transistor gate”) shown in figure 7 to form a trench opening

(“gate trench between the non-planar gate spacers”) shown in figure 8, where the removal of the gate structure exposes the channel region 205 (“a portion of the non-planar transistor fin”). (Ex. 1005, ¶¶[0047], [0048]; Ex. 1002, ¶77.)



(Ex. 1005, FIG. 7 (annotated); Ex. 1002, ¶77.)

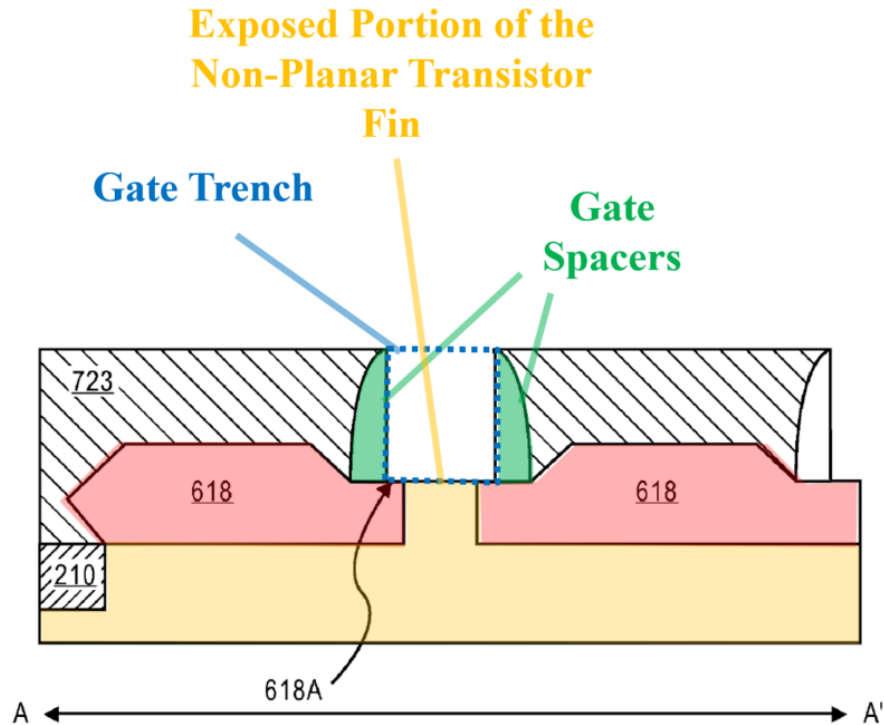


FIG. 8

(Ex. 1005, FIG. 8 (annotated); Ex. 1002, ¶77.)

- g) “forming a gate dielectric adjacent the non-planar transistor fin within the gate trench;”
- h) “depositing conductive gate material within the gate trench;”

The Cappellani-Siddiqui combination discloses or suggests these features. (Ex. 1002, ¶78.) As shown in annotated figure 9 below, Cappellani discloses forming a gate dielectric layer 924 in the gate trench on the channel region 205 of the fin (“adjacent the non-planar transistor fin within the gate trench”) and then depositing a metal gate electrode layer 926 (“conductive gate material”) within the

gate trench overlying the gate dielectric layer 924. (Ex. 1005, ¶[0048] (“Returning to FIG. 1, if the gate dielectric layer is removed, a new gate dielectric layer may be deposited into the trench opening over the channel region 205 at operation 120. ... A metal gate electrode layer may then be deposited over the gate dielectric layer.”), ¶[0049]; Ex. 1002, ¶78.)

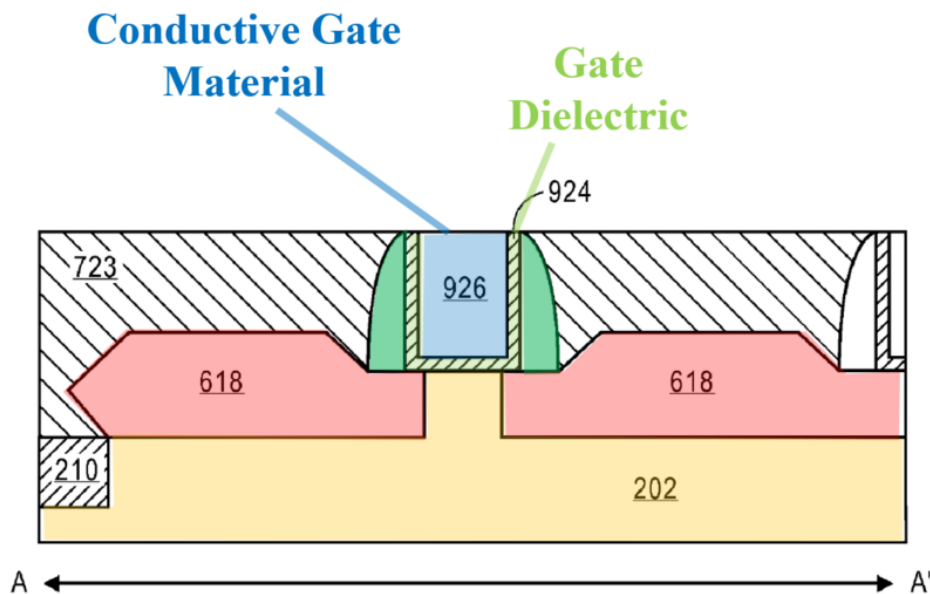


FIG. 9

(Ex. 1005, FIG. 9 (annotated); Ex. 1002, ¶78.)

- i) **“removing a portion of the conductive gate material to form a recess between the non-planar transistor gate spacers;”**
- j) **“forming a capping dielectric structure within the recess by high density plasma depositing a dielectric material;”**

The Cappellani-Siddiqui combination discloses or suggests these features. (Ex. 1002, ¶¶79-89.) As discussed above for claim elements 1[a]-1[h], the Cappellani-Siddiqui combination discloses or suggests the formation of a non-planar transistor that includes a replacement gate structure. (Sections IX.A.1[a]-[h].) While Cappellani specifically contemplates the need for electrical connections to the transistor, Cappellani does not explicitly disclose the additional steps that are taken after formation of the transistor to provide the needed connections. (Ex. 1005, ¶[0046] (“As will be appreciated by those of skill in the art, the multi-gate MOS transistor may undergo further processing, ... that may further modify the transistor and/or **provide the necessary electrical interconnections.**”); Ex. 1002, ¶79.)

Siddiqui discloses additional steps that enable the interconnection of a transistor to surrounding circuitry using a self-aligned source/drain contact, and a POSITA would have found it obvious, based on Siddiqui’s teachings, to implement such a self-aligned source/drain contact in conjunction with the Cappellani-Siddiqui transistor discussed above with respect to claim features 1[a]-[h]. (Ex. 1006, ¶[0017]

(“The present disclosure relates to structures and methods for forming semiconductor devices ... in which the contacts to the source and drain regions are formed using a self aligning process.”); Ex. 1002, ¶80.) As discussed above for claim element 1[c], Siddiqui, like Cappellani, is related to transistors that utilize sacrificial gate structures, and a POSITA implementing a transistor like that disclosed by Cappellani would have had reason to look to Siddiqui. (Section IX.A.1(c); Ex. 1002, ¶80.)

Siddiqui discloses that by forming dielectric spacers on the sidewalls of the sacrificial gate structure using silicon nitride, the spacers can be used together with a silicon nitride protective capping layer over a functional gate structure to provide the ability to control later etching of the opening in which the self-aligned source/drain contacts are formed. (Section IX.A.1(c); Ex. 1006, ¶[0032]-[0034]; Ex. 1002, ¶81.)

As shown in figure 3 below, Siddiqui discloses that after removing the sacrificial gate, a functional gate structure, which includes metal layer 35 and metal fill material 40 (“conductive gate material”) overlying gate dielectric layer 30, is formed. (Ex. 1006, ¶¶[0040], [0043], [0056]-[0057]; Ex. 1002, ¶82.)

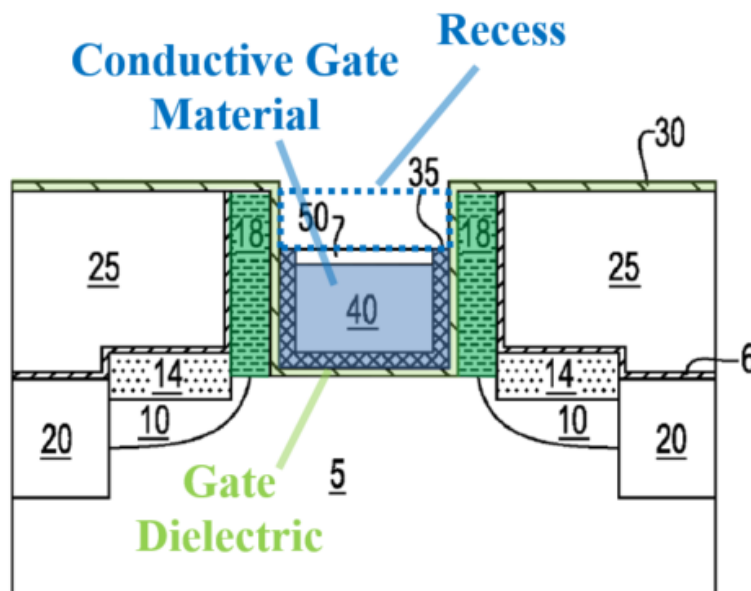


FIG. 3

(Ex. 1006, FIG. 3 (annotated); Ex. 1002, ¶82.)

Siddiqui further discloses that the conductive gate material shown in annotated figure 3 above has been recessed to form a recess using, for example, an anisotropic reactive ion etch (RIE) or an isotropic wet etch. (Ex. 1006, ¶[0058] (“metal fill material 40 may be recessed using an etch process”); *see also id.*, ¶¶[0059]-[0061]; Ex. 1002, ¶83.)

Following recessing of the metal fill material, a dielectric protective cap structure, which is shown in annotated figure 4 below, is formed over the functional gate structure, where the cap structure protects the gate during the etching to form the opening for the self-aligned contact. (Ex. 1006, ¶[0062] (“FIG. 4 depicts forming

a protective cap structure 60 over the functional gate structure. ... The protective cap structure 60 may be composed of any dielectric material that can protect the functional gate from being damaged during the etch process that provides the opening to the source regions 10 and the drain regions 15.”); Ex. 1002, ¶84.)

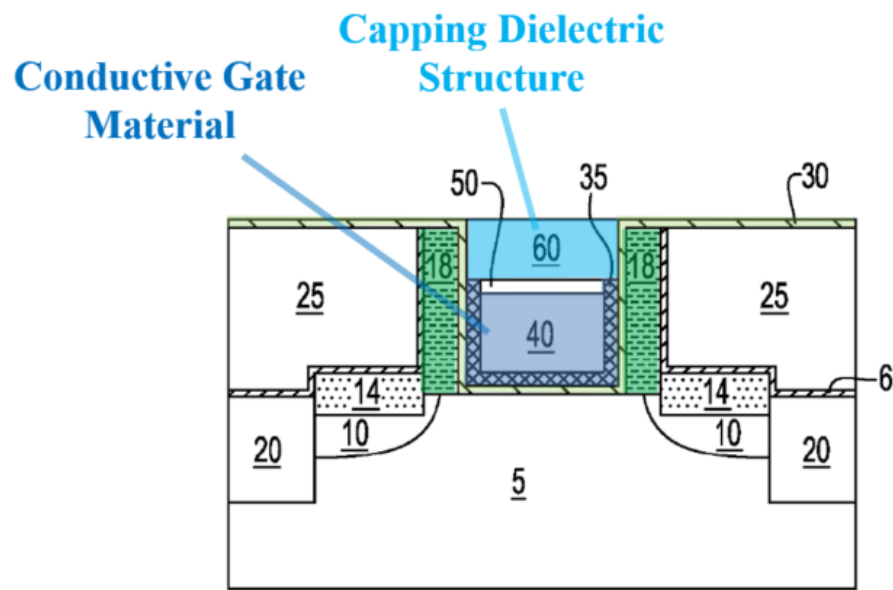
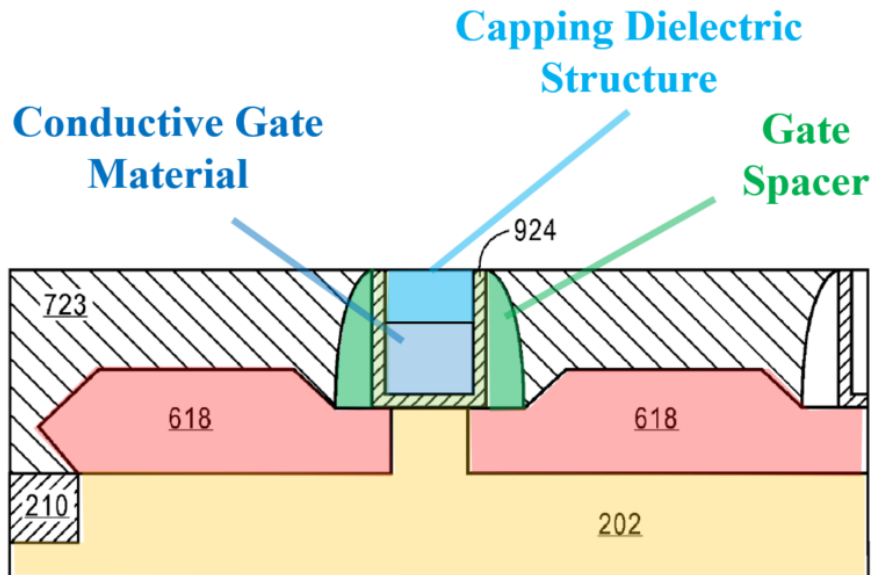


FIG. 4

(Ex. 1006, FIG. 4 (annotated); Ex. 1002, ¶84.)

Therefore, Siddiqui discloses that, in order to form a self-aligned source/drain contact, a capping dielectric structure like that shown in figure 4 above is used to act as an etch stop and protect the gate structure during subsequent etching to form the openings for the contacts. (Ex. 1002, ¶85.) In view of Siddiqui's disclosure, a

POSITA would have found it obvious to recess the conductive material of the gate in a transistor like that disclosed by Cappellani to form a recess between the transistor gate spacers, where a capping dielectric structure is then formed in the recess. (*Id.*) As disclosed by Siddiqui, these steps are part of the process for forming self-aligned source/drain contacts. (Ex. 1006, ¶[0070] (“The contacts 90 are self-aligned to the diffusion regions, i.e., source regions 10 and drain regions 15, because the functional gate is protected from being damaged by the etch process that forms the vias 75 for the contacts 90 by the protective cap structure 60 that is present over the functional gate, and the protective dielectric layer 18 that is present on the sidewall of the functional gate.”); Ex. 1002, ¶85.) The non-limiting demonstrative below, which is based on figure 9 of Cappellani, shows the transistor structure of the Cappellani-Siddiqui combination where the conductive gate material has been recessed and a capping dielectric structure has been formed in the recess. (Ex. 1002, ¶85.)

 $(Id.)$

Cappellani expressly contemplates the need for electrical connections to the transistor, but does not disclose the steps to form source/drain contacts. Siddiqui, however, provides such disclosure, and a POSITA would have found it obvious to use Siddiqui's contact-formation method in conjunction with a transistor as disclosed by Cappellani. (*Id.*, ¶86.) Formation of the source/drain contacts in a transistor as disclosed by Cappellani using the methodology disclosed by Siddiqui would have been nothing more than the application of a known technique (Siddiqui's self-aligned contact formation) to a known device (Cappellani's transistor) ready for improvement (adding electrical connections acknowledged as necessary by

Cappellani) to yield predictable results (a transistor having connectivity to other circuit elements). (*Id.*) See *KSR* at 417.

A POSITA would have been motivated to use Siddiqui's contact formation technique both because Cappellani does not provide any description as to how to form such contacts and because the self-aligned contact formation technique of Siddiqui provides advantages applicable to FinFET devices. (Ex. 1002, ¶87.) As a POSITA would have known, self-aligned contacts, which are sometimes referred to as "borderless contacts," are useful in devices having small critical dimensions (e.g. gate length) such as FinFETs. (Ex. 1007, ¶¶[0008]-[0009]; Ex. 1020, ¶¶[0002]-[0003]; Ex. 1002, ¶¶27-31, 87.) Such contacts, which are self-aligned to the gate electrode, allow the contact to be formed closer to the gate structure than non-self-aligned contacts while reducing the risk of shorting the electrodes, thereby reducing the area needed to form the transistor and associated interconnect. (Ex. 1020, ¶¶[0002]-[0003]; Ex. 1007, ¶[0009]; Ex. 1002, ¶¶27-31, 87.) A POSITA would also have known that such self-aligned contacts allow for increased tolerance with respect to possible lithographic misalignment in the formation of the different structures of the transistor. (Ex. 1020, ¶[0008]; Ex. 1002, ¶¶27-31, 87.) Therefore, a POSITA would have been motivated to form self-aligned contacts to provide the needed connections to the transistor of the Cappellani-Siddiqui combination. (Ex.

1002, ¶87.) As discussed above for claim elements 1[c]-[d], a POSITA would have understood that techniques applicable to planar MOSFETs, like that disclosed by Siddiqui, are also applicable to non-planar FETs, like Cappellani's FinFET, and therefore a POSITA implementing contacts in a FinFET like Cappellani's would have had good reason to look to Siddiqui. (*Id.*; Ex. 1009, Abstract, 2324; Ex. 1001, 3:47-51.)

Siddiqui further discloses that protective cap structure 60 may be a dielectric material formed using high-density chemical vapor deposition (HDCVD). (Ex. 1006, ¶[0062], ¶[0063] (“The protective cap structure 60 may be formed by a deposition process including...chemical vapor deposition (CVD),” including “high-density chemical vapor deposition (HDCVD)”); Ex. 1002, ¶88.) A POSITA would have understood that HDCVD is “high density plasma deposition” as recited in claim element 1[j]. (Ex. 1002, ¶88; Ex. 1011, 5:56-57 (“high-density plasma chemical vapor deposition (HDCVD) process”); Ex. 1012, 3:62-63; Ex. 1013, 10:9-10; Ex. 1014, ¶[0039].)

Therefore, the Cappellani-Siddiqui combination discloses or suggests claim elements 1[i] and 1[j], as these steps are included in the self-aligned contact formation process disclosed by Siddiqui that a POSITA would have found it obvious to use in conjunction with a transistor as disclosed or suggested by the Cappellani-

Siddiqui combination discussed above for claim elements 1[a]-1[h]. (Ex. 1002, ¶89.)

k) “forming at least one dielectric material over the source/drain region, the non-planar transistor gate spacers, and the capping dielectric structure; and”

The Cappellani-Siddiqui combination discloses or suggests this feature. (Ex. 1002, ¶¶90-91.) As discussed above for claim elements 1[i]-1[j], the Cappellani-Siddiqui combination discloses or suggests the formation self-aligned contacts for the transistor of the Cappellani-Siddiqui combination. (Sections IX.A.1[i]-[j].) Siddiqui discloses that, before etching to form via 75 as a part of the contact formation process, an interlayer dielectric layer 85 is blanket deposited over the protective cap structure, gate spacers, and source/drain regions. (Ex. 1006, ¶[0065] (“prior to etching to form the via 75, an interlevel dielectric layer 85 is blanket deposited atop the structure depicted in FIG. 5”); *see also id.*, ¶¶[0066]-[0067]; Ex. 1002, ¶90.)

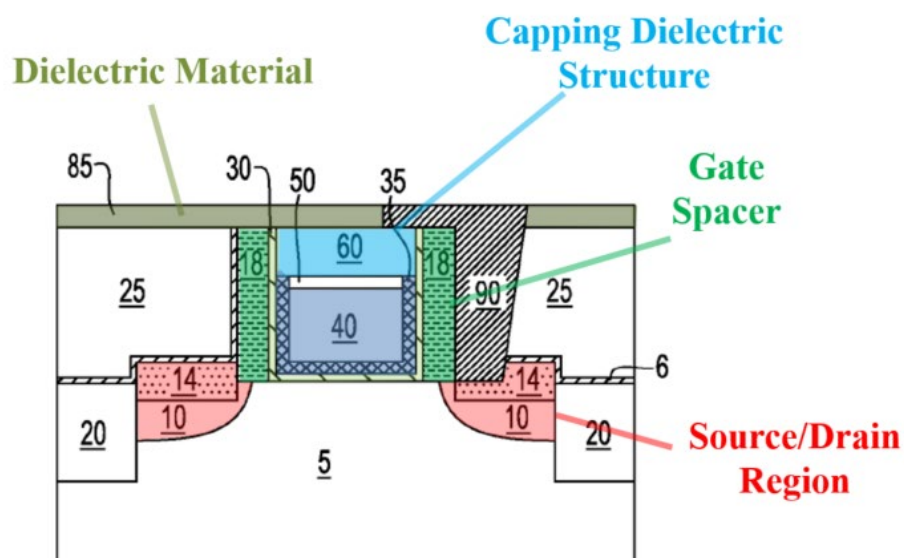


FIG. 6

(Ex. 1006, FIG. 6 (annotated); Ex. 1002, ¶90.)

A POSITA would have understood that the interlevel dielectric layer is used to separate different layers within the integrated circuit structure and isolate different contact structures (e.g., source/drain contacts) that are on the same layer. (Ex. 1002, ¶91.) As such, a POSITA would have found it obvious to form such a dielectric layer as a part of the contact formation process as disclosed or suggested by Siddiqui, where the dielectric layer is formed over the source/drain region, the non-planar transistor gate spacers, and the capping dielectric structure. (*Id.*) The non-limiting demonstrative below shows the transistor of the Cappellani-Siddiqui combination

discussed above for claim elements 1[i]-[j] with the addition of such an interlevel dielectric layer in a manner consistent with Siddiqui's disclosure.

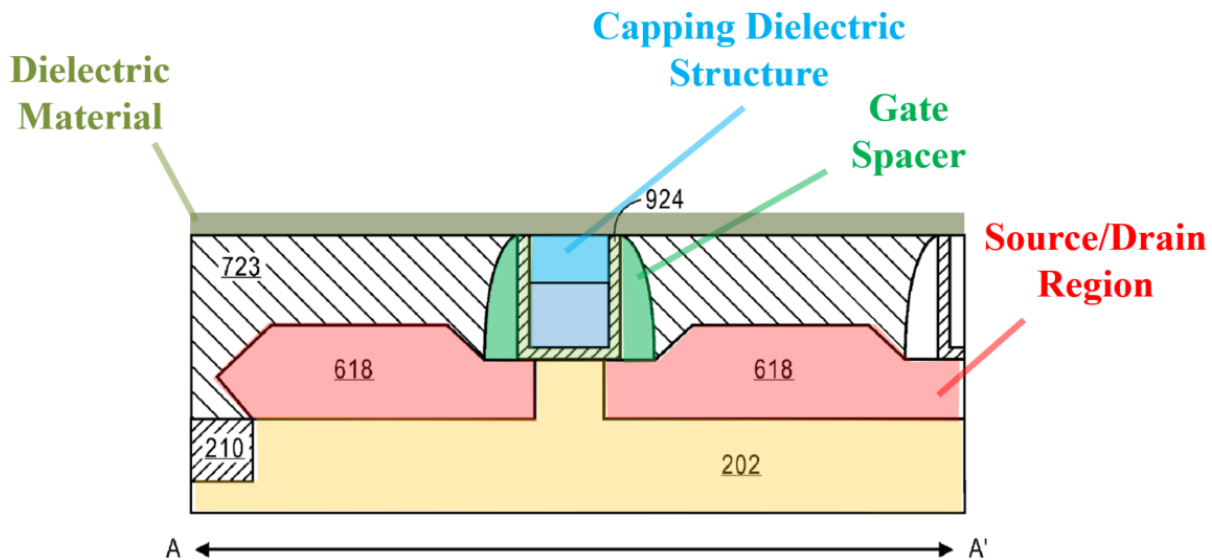


FIG. 9

(*Id.*)

l) “forming a contact opening through the at least one dielectric material to expose at least a portion of the source/drain region.”

The Cappellani-Siddiqui combination discloses or suggests this feature. (Ex. 1002, ¶¶92-95.) As discussed above for claim elements 1[i]-1[j], the Cappellani-Siddiqui combination discloses or suggests the formation self-aligned contacts as disclosed by Siddiqui. (Sections IX.A.1[i]-[j].) As a part of the contact formation process, Siddiqui discloses etching to form via 75 (“contact opening”) through the interlevel dielectric layer 85 (“the at least one dielectric material”) and the mandrel

dielectric layer 25 to expose the underlying source/drain region. (Ex. 1006, ¶[0068] (“The interlevel dielectric layer 85 and the mandrel dielectric layer 25 are then patterned and etched to form vias 75 to the source regions 10 and the drain regions 15 using patterning and selective etch process.”); Ex. 1002, ¶92.)

Annotated figure 6 of Siddiqui shows the via (“contact opening”) after conductive metal has been deposited in the opening to form the contact 90. (Ex. 1006, ¶[0070].)

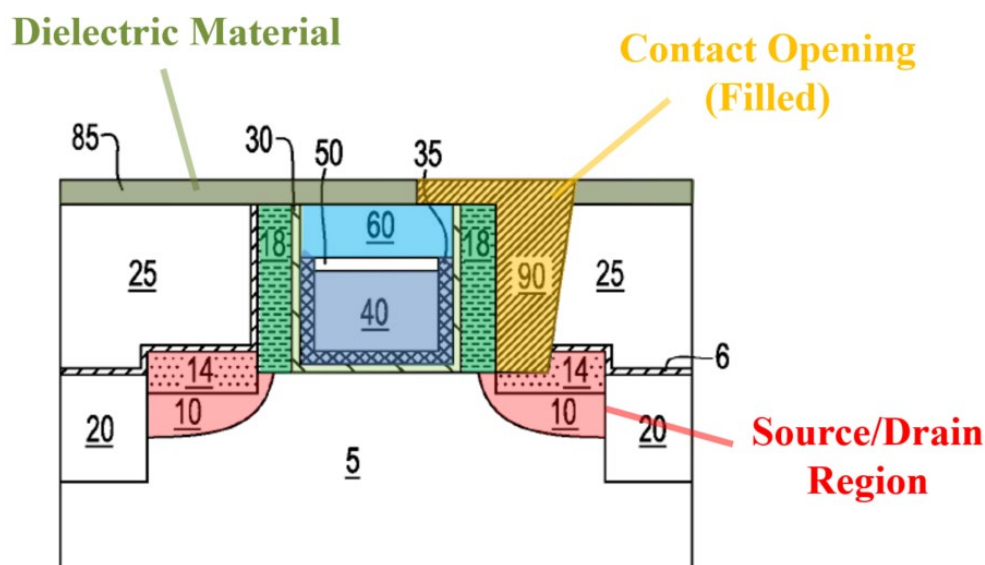
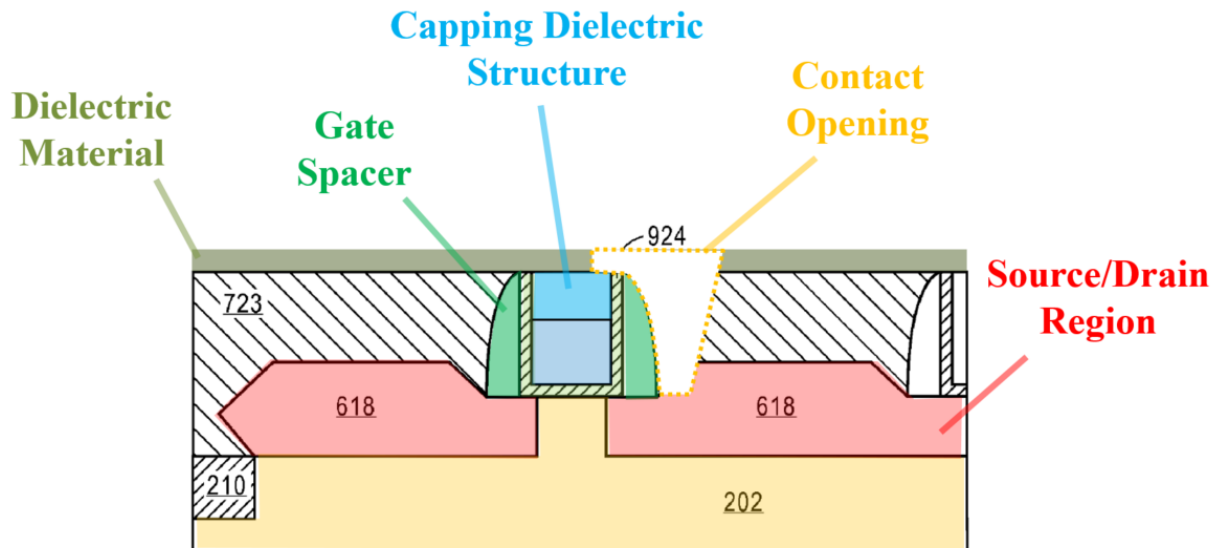


FIG. 6

(Ex. 1006, FIG. 6 (annotated); Ex. 1002, ¶93.)

The non-limiting demonstrative below shows the “contact opening” formed “through the at least one dielectric material to expose at least a portion of the

source/drain region” according to the Cappellani-Siddiqui combination. (Ex. 1002, ¶94.)



(*Id.*)

Consistent with the disclosure of Siddiqui, a POSITA would have understood that such an opening allows for the subsequent deposition of conductive material to provide electrical contact to the source/drain region. (Ex. 1006, ¶[0070]; Ex. 1002, ¶95.) Therefore, the Cappellani-Siddiqui combination discloses or suggests claim element 1[1].

2. Claim 2

“The method of claim 1, wherein high density plasma depositing the capping dielectric structure comprises high density plasma depositing a silicon nitride capping dielectric structure.”

The Cappellani-Siddiqui combination discloses or suggests this feature. (Ex. 1002, ¶96.) As discussed above for claim element 1[j], the Cappellani-Siddiqui combination discloses or suggests forming protective cap structure (“capping dielectric structure”) using high density plasma depositing as disclosed by Siddiqui. (Section IX.A.1(j).) Siddiqui further discloses that, in order to provide the desired protection for the gate structure during the subsequent selective etch used to form the via, the dielectric material is silicon nitride. (Ex. 1006, ¶[0062] (“the protective cap structure 60 is composed of a nitride, such as **silicon nitride.**”); Ex., 1002, ¶96.)

3. Claim 5

“The method of claim 1, wherein forming a capping dielectric structure comprises: high density plasma depositing capping dielectric material within the recess; and removing excess capping dielectric material.”

The Cappellani-Siddiqui combination discloses or suggests this feature. (Ex. 1002, ¶¶97-98.) As discussed above for claim element 1[j], the Cappellani-Siddiqui combination discloses or suggests forming protective cap structure (“capping dielectric structure”) over the conductive material of the gate structure using high

density plasma depositing as disclosed by Siddiqui. (Section IX.A.1(j).) Siddiqui further discloses that, after deposition of the capping dielectric material in the recess, chemical mechanical planarization (CMP) is used to planarize the cap structure, which removes excess capping dielectric material. (Ex. 1006, ¶[0064] (“Following deposition, the dielectric material that provides the protective cap structure 60 may be planarized...by chemical mechanical planarization (CMP).”); Ex. 1002, ¶97.)

A POSITA would have been motivated to include such a step in the self-aligned contact formation process to promote formation of subsequent overlying layers. (Ex. 1002, ¶98.)

4. Claim 6

“The method of claim 1, wherein forming a contact opening through the dielectric material to expose at least a portion of the source/drain region further comprises forming a contact opening through the dielectric material which exposes at least a portion of the source/drain region and at least a portion of one non-planar transistor gate spacer.”

The Cappellani-Siddiqui combination discloses or suggests this feature. (Ex. 1002, ¶¶99-100.) As discussed above for claim element 1[1], the Cappellani-Siddiqui combination discloses or suggests etching a contact opening to expose a portion of the source/drain region. (Section IX.A.1(l).) Siddiqui further discloses that the etching is a selective and etches the protective cap structure and gate spacers

at a slower rate than the interlevel dielectric layer 85 and the mandrel dielectric layer 25. (Ex. 1006, ¶¶[0068]-[0070]; Ex. 1002, ¶99.)

Therefore, Siddiqui discloses that the selective etch removes interlevel dielectric and the mandrel dielectric, while the protective cap and spacers act as an etch stop and protect the functional gate structure. In other words, the etching operation stops or slows the rate of removal of material when it reaches (and hence exposes) the protective cap and spacers. (Ex. 1002, ¶100.) Therefore, as shown in annotated figure 6 of Siddiqui and the non-limiting demonstrative below corresponding to the Cappellani-Siddiqui combination, the etch (“forming a contact opening through the dielectric material which exposes at least a portion of the source/drain region”) also exposes a portion of a gate spacer (“at least a portion of one non-planar transistor gate spacer”) and a portion of the protective cap. (*Id.*)

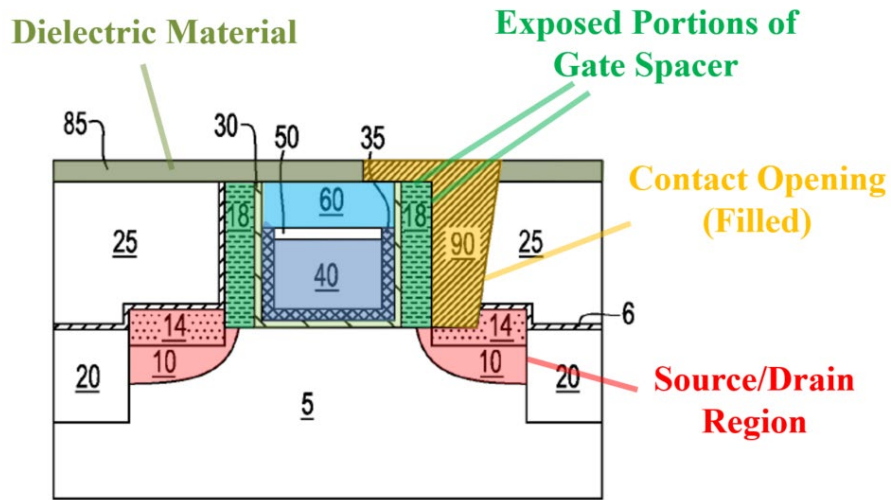
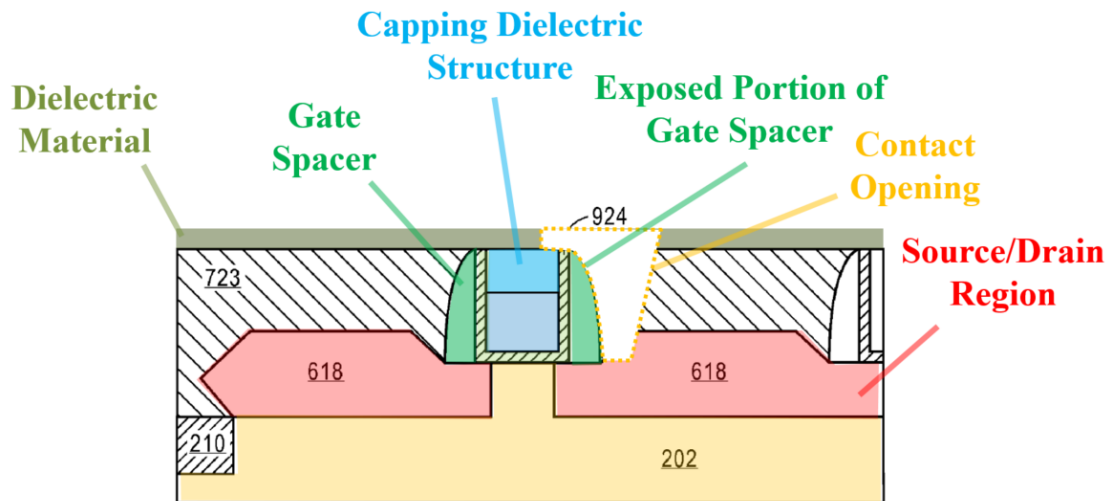


FIG. 6

(Ex. 1006, FIG. 6 (annotated); Ex. 1002, ¶100.)



(Ex. 1002, ¶100.)

5. Claim 7

“The method of claim 6, further comprising forming a source/drain contact to abut the exposed portion of the source/drain region and exposed portion of the non-planar transistor gate spacer.”

The Cappellani-Siddiqui combination discloses or suggests this feature. (Ex. 1002, ¶¶101-103.) As discussed above for claim element 1[1] and claim 6, the Cappellani-Siddiqui combination discloses or suggests forming a contact opening to expose a portion of the source/drain region and a portion of the gate spacer. (Sections IX.A.1(l), IX.A.4.) Siddiqui further discloses that the contact opening is filled with conductive metal to form the contact for the transistor. (Ex. 1006, ¶[0070]; Ex. 1002, ¶101.) Therefore, the self-aligned contact formation of the Cappellani-Siddiqui combination fills the contact hole with conductive material to form a source/drain contact, where, because it fills the contact hole, the contact abuts the exposed portions of the source/drain region and the gate spacer. (Ex. 1002, ¶101.) Annotated figure 6 of Siddiqui and the non-limiting demonstrative for the

Cappellani-Siddiqui combination show the filled contact abutting the exposed portions of the source/drain region and gate spacer.⁴ (Ex. 1002, ¶103.)

⁴ While Siddiqui discloses that “metal semiconductor alloy regions 14 may be formed atop the source regions 10 and the drain regions,” a POSITA would have understood that such alloy regions are meant to provide improved contact to the source/drain regions and are optional based on Siddiqui’s disclosure. (Ex. 1002, ¶102; Ex. 1006, ¶[0035].) Indeed, Siddiqui’s disclosure regarding formation of the via 75 indicates that the via exposes the source/drain region (Ex. 1006, ¶[0065] (“etching a via 75 ... to expose at least one of the source region 10 and the drain region 15”), thereby confirming that regions 14 are optional and/or can be considered as a part of the source/drain region. (Ex. 1002, ¶102.) A POSITA would have understood that such alloy regions need not be included in the Cappellani-Siddiqui transistor. (*Id.*)

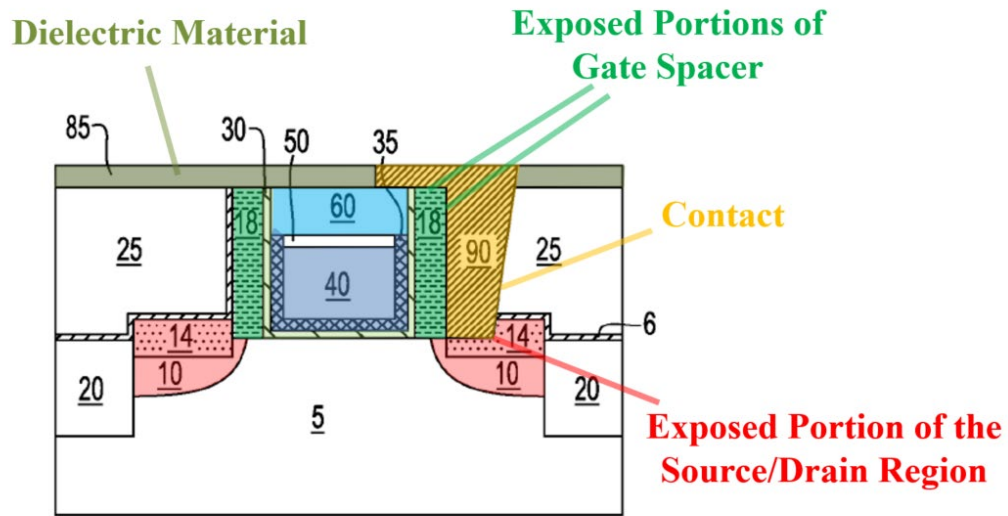
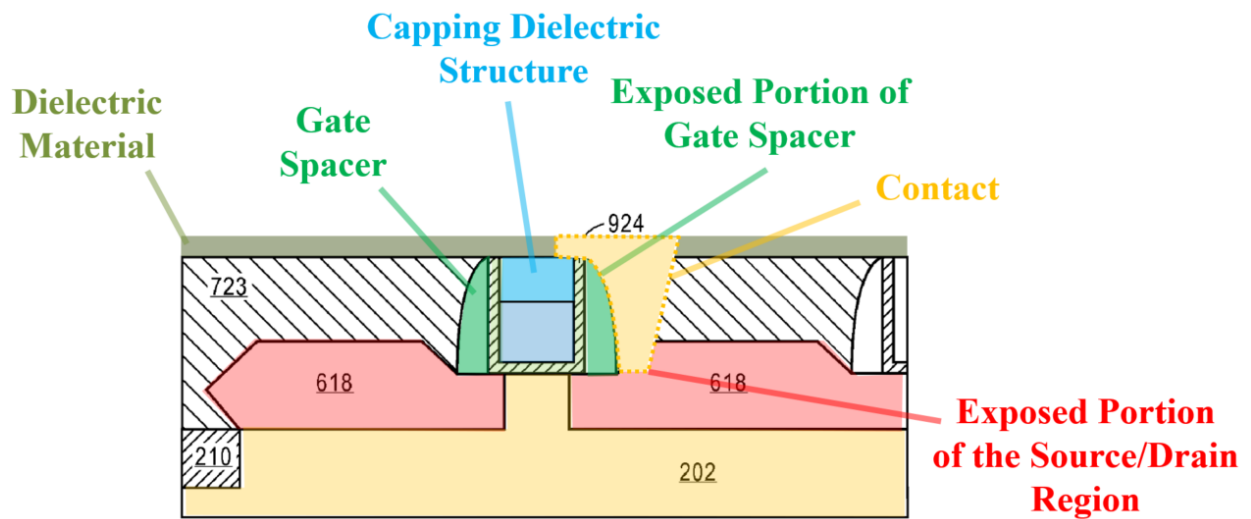


FIG. 6

(Ex. 1006, FIG. 6 (annotated); Ex. 1002, ¶103.)



(Ex. 1002, ¶103.)

6. Claim 8

“The method of claim 1, wherein forming a contact opening through the dielectric material to expose at least a portion of the source/drain region further comprises forming a contact opening through the dielectric material which exposes at least a portion of the source/drain region and at least a portion of the capping dielectric structure.”

The Cappellani-Siddiqui combination discloses or suggests this feature for the same reasons discussed above for claim 6, where, as shown in annotated figure 6 of Siddiqui and the non-limiting demonstrative below corresponding to the Cappellani-Siddiqui combination, the selective etching of the Cappellani-Siddiqui combination exposes a portion of the source/drain region and a portion of the protective cap (“capping dielectric structure”). (Section IX.A.4; Ex. 1002, ¶¶104-105.)

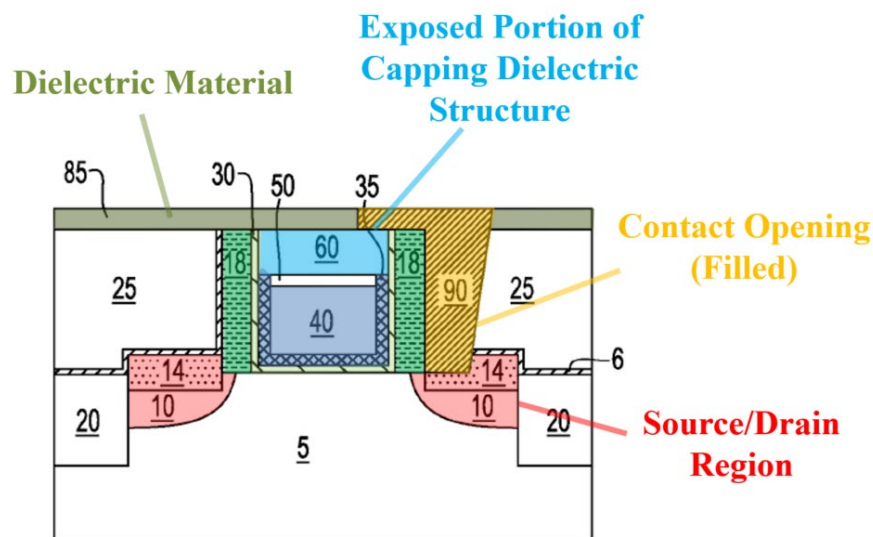
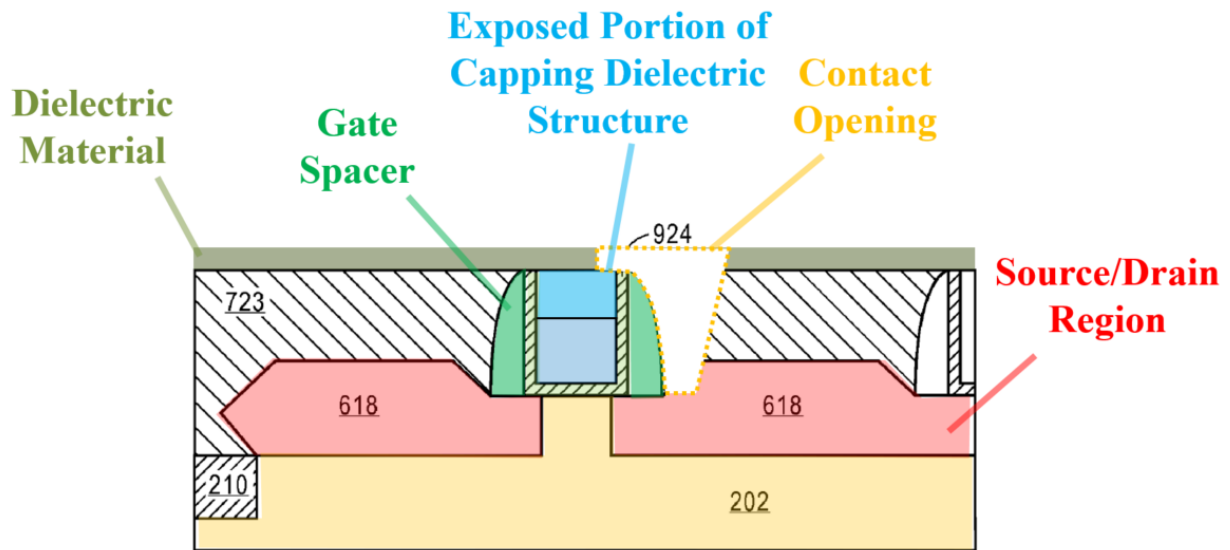


FIG. 6

(Ex. 1006, FIG. 6 (annotated); Ex. 1002, ¶105.)



(Ex. 1002, ¶105.)

7. Claim 9

“The method of claim 8, further comprising forming a source/drain contact abuts the exposed portion of the source/drain region and the exposed portion of the capping dielectric structure.”

The Cappellani-Siddiqui combination discloses or suggests this feature to the extent it can be understood⁵ for the same reasons discussed above for claim 7, where, as shown in annotated figure 6 of Siddiqui and the non-limiting demonstrative below

⁵ For purposes of this proceeding Petitioner assumes that claim 9 should read “forming a source/drain contact [abuts] to abut the exposed portion” Petitioner, however, does not concede that claim 9 is not indefinite.

corresponding to the Cappellani-Siddiqui combination, the contact abuts the exposed portions of the source/drain region and the protective cap (“capping dielectric structure”). (Section IX.A.5; Ex. 1002, ¶¶106-107.)

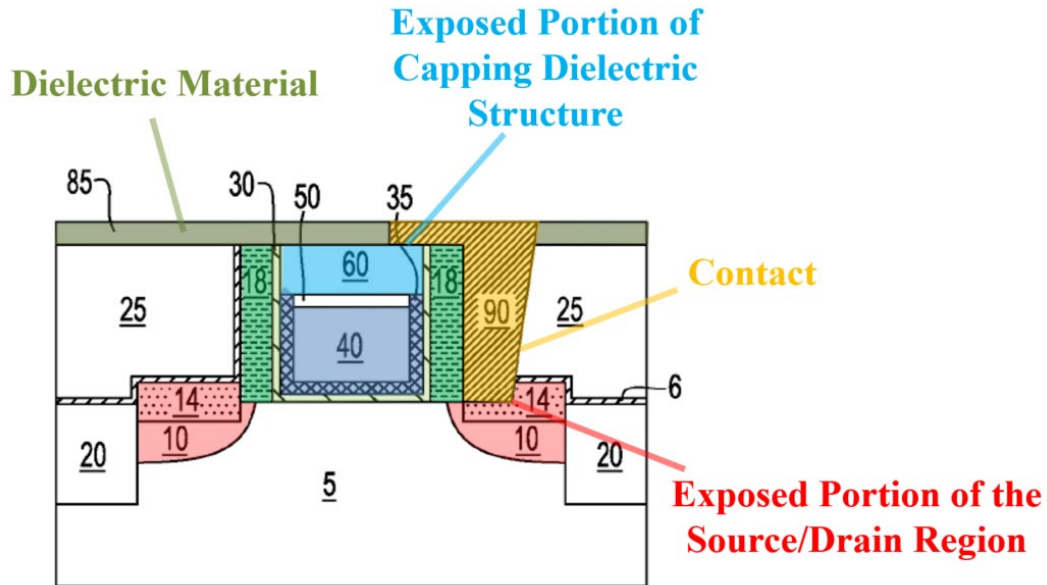
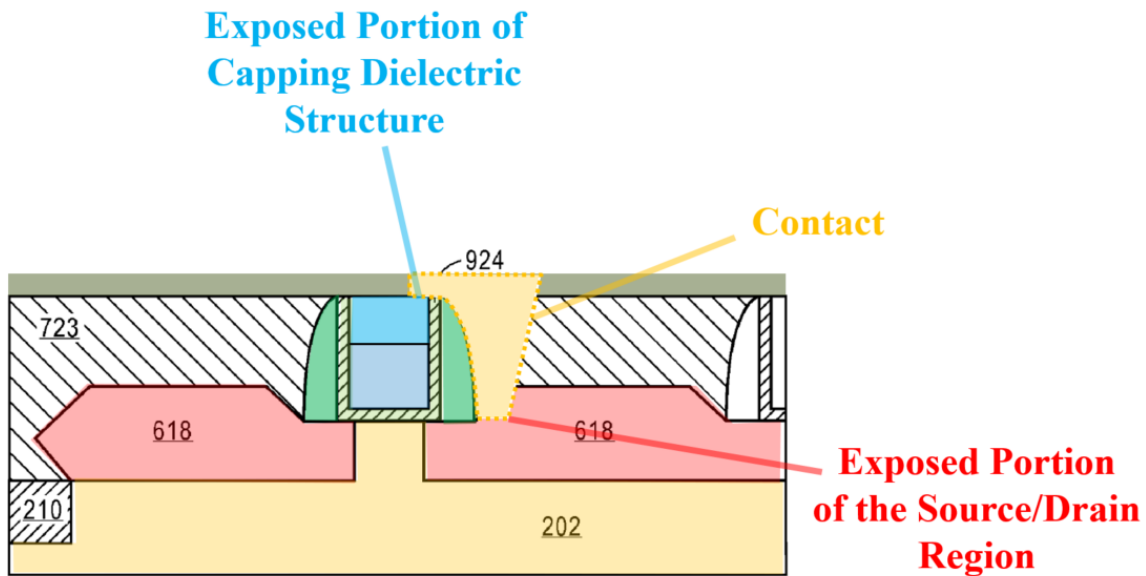


FIG. 6

(Ex. 1006, FIG. 6 (annotated); Ex. 1002, ¶107.)



(Ex. 1002, ¶107.)

8. Claim 10

“The method of claim 1, wherein forming a contact opening through the dielectric material to expose at least a portion of the source/drain region further comprises forming a contact opening through the dielectric material exposes at least a portion of the source/drain region, at least a portion of the non-planar transistor gate spacer, and at least a portion of the capping dielectric structure.”

The Cappellani-Siddiqui combination discloses or suggests this feature for the reasons presented above for claims 6 and 8. (Sections IX.A.4, 6; Ex. 1002, ¶108.)

9. Claim 11

“The method of claim 10, further comprising forming a source/drain contact to abut the exposed portion of the source/drain region, the exposed portion of non-planar gate spacer, and the exposed portion of the capping dielectric structure.”

The Cappellani-Siddiqui combination discloses or suggests this feature for the reasons presented above for claims 7 and 9. (Sections IX.A.5, 7; Ex. 1002, ¶109.)

B. Ground 2 – Cappellani in View of Siddiqui and Park Renders Claims 1, 2, and 4-11 Obvious

1. Claims 1, 2, and 5-11

As discussed above in Section IX.A, the Cappellani-Siddiqui combination discloses or suggests the features of claims 1, 2, and 5-11, including claim element 1[j], which requires “forming a capping dielectric structure within the recess by high density plasma depositing a dielectric material.” (Section IX.A.) To the extent PO argues that the Cappellani-Siddiqui combination does not disclose or suggest forming the capping dielectric by “high density plasma deposition,” a POSITA would have found it obvious to form the capping layer using high density plasma chemical vapor deposition (HDPCVD) in view of Park and their knowledge of the state of the art. (Ex. 1002, ¶¶110-113.)

Park, like Cappellani and Siddiqui, is directed to forming transistors with improved performance, where, like Siddiqui, Park discloses a nitride capping layer overlying the transistor structure. (Ex. 1010, Abstract, 1:14-17; Ex. 1002, ¶111.) Park further discloses that the nitride capping layer can be formed using high density plasma chemical vapor deposition (HDPCVD). (Ex. 1010, 6:32-37 (“The capping nitride layer 37 may be formed at a temperature of about 350° C. to about 500° C. using, e.g., low pressure chemical vapor deposition (LPCVD), plasma enhanced chemical vapor deposition (PECVD), high density plasma chemical vapor deposition (HDPCVD), or a combination thereof.”); Ex. 1002, ¶111.)

In view of Park, a POSITA would have found it obvious to form the silicon nitride capping layer in a transistor of the Cappellani-Siddiqui combination discussed above in section IX.A using HDPCVD. (Ex. 1002, ¶112.) Such a POSITA would have understood that Park discloses HDPCVD is one of a finite number of identified and predictable options for depositing silicon nitride capping layers, and would have found it obvious to try using HDPCVD to form the silicon nitride capping layer with a reasonable expectation of success. (*Id.*) *See KSR* at 416-18. Moreover, doing so would have been nothing more than the application of a known technique (HDPCVD deposition of silicon nitride) to a known device ready for improvement (the transistor of the Cappellani-Siddiqui combination) to yield

predictable results (a functional transistor with a silicon nitride capping layer). (Ex. 1002, ¶112.) *See KSR* at 416-18.

A POSITA would also have understood that using HDPCVD to form the silicon nitride cap provides certain advantages, including improved gap-fill capability, which such a skilled person would have recognized is particularly relevant to formation of the capping dielectric structure in the recessed gate region in the Cappellani-Siddiqui combination. (Ex. 1015, 1:65-2:2 (“HDP-CVD processes generally have superior gapfill capabilities as compared to these other types of CVD processes because HDP-CVD deposition process provide[s] for a sputtering component to the deposition process simultaneous with film growth.”); Ex. 1016, 1:65-2:6; Ex. 1002, ¶114.) Therefore a POSITA would have been motivated to use HDPCVD for forming the capping dielectric structure in order to avoid voids in the dielectric that could result in unwanted short circuits, or damage to the gate structure the dielectric is protecting. (Ex. 1002, ¶114.) Based on their knowledge of the state of the art and Park’s disclosure, a POSITA would have had a high likelihood of success. (*Id.*) Therefore, the Cappellani-Siddiqui-Park combination discloses or suggests claim element 1[j], whereas the remaining features of claims 1, 2, and 5-11 are disclosed or suggested for the reasons provided above in section IX.A. (*Id.*; Sections IX.A.1-9.)

2. Claim 4

“The method of claim 1, wherein high density plasma depositing the capping dielectric structure comprises high density plasma depositing the capping dielectric structure at a temperature between about 300° C. and 600° C.”

The Cappellani-Siddiqui-Park combination discloses or suggests this feature. (Ex. 1002, ¶114.) As discussed above in section IX.B.1, the Cappellani-Siddiqui-Park combination discloses or suggests forming protective cap structure (“capping dielectric structure”) over the conductive material of the gate structure using high density plasma depositing. (Section IX.B.1.) Park further discloses that the nitride capping layer can be formed using high density plasma chemical vapor deposition (HDPCVD) at a temperature of 350-500° C., which is within the claimed range of 300-600° C. (Ex. 1010, 6:32-37 (“The capping nitride layer 37 may be formed at a temperature of about 350° C. to about 500° C. using ... high density plasma chemical vapor deposition (HDPCVD)”); Ex. 1002, ¶114.) Therefore, the Cappellani-Siddiqui-Park combination discloses or suggests claim 4.

C. Ground 3 – Brask in View of Cheng Renders Claims 1, 2, and 5-11 Obvious

1. Claim 1

a) Element 1[a]⁶

To the extent the preamble is limiting, Brask discloses a “method.” (Ex. 1002, ¶¶115-116.) Brask discloses a method for forming p-type and n-type non-planar transistors with metal gate electrodes “utilizing a replacement gate technique.” (Ex. 1008, ¶[0058]; Ex. 1002, ¶116.) Such a method is further discussed below for claim elements 1[b]-1[l]. (Sections IX.C.1(b)-(l); Ex. 1002, ¶116.)

b) Element 1[b]

Brask discloses this claim feature. (Ex. 1002, ¶117.) As shown in annotated figure 6A below, Brask discloses forming a sacrificial gate dielectric layer 602 and a sacrificial gate electrode layer 604 (together “a sacrificial non-planar transistor gate”) over a semiconductor body 510 (“non-planar transistor fin”). (Ex. 1008, ¶¶[0046], [0059]; Ex. 1002, ¶117.)

⁶ The claim language is not repeated.

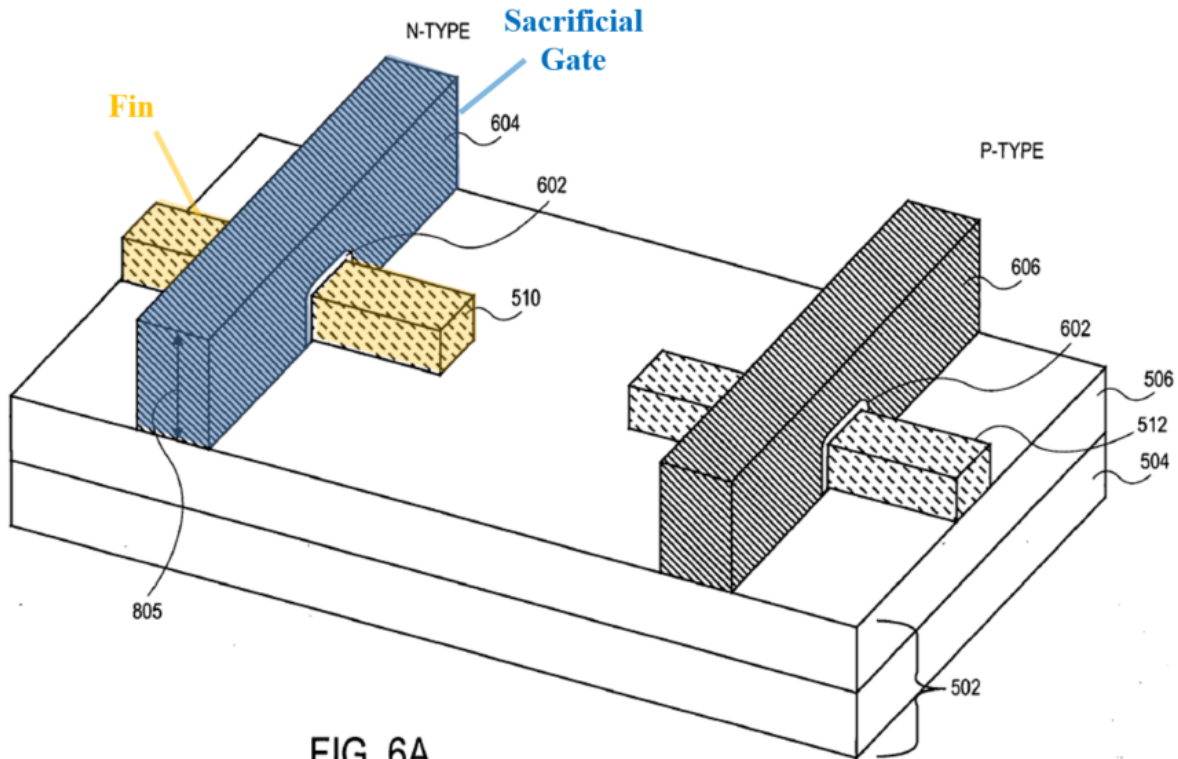


FIG. 6A

(Ex. 1008, FIG 6A (annotated); Ex. 1002, ¶117.)

c) Element 1[c]

d) Element 1[d]

Brask discloses these limitations. (Ex. 1002, ¶¶118-119.) As shown in annotated figure 6D below, Brask discloses forming dielectric sidewall spacers 612 (“non-planar transistor gate spacers”) adjacent to the sacrificial gate. (Ex. 1008, ¶[0065]; Ex. 1002, ¶118.)

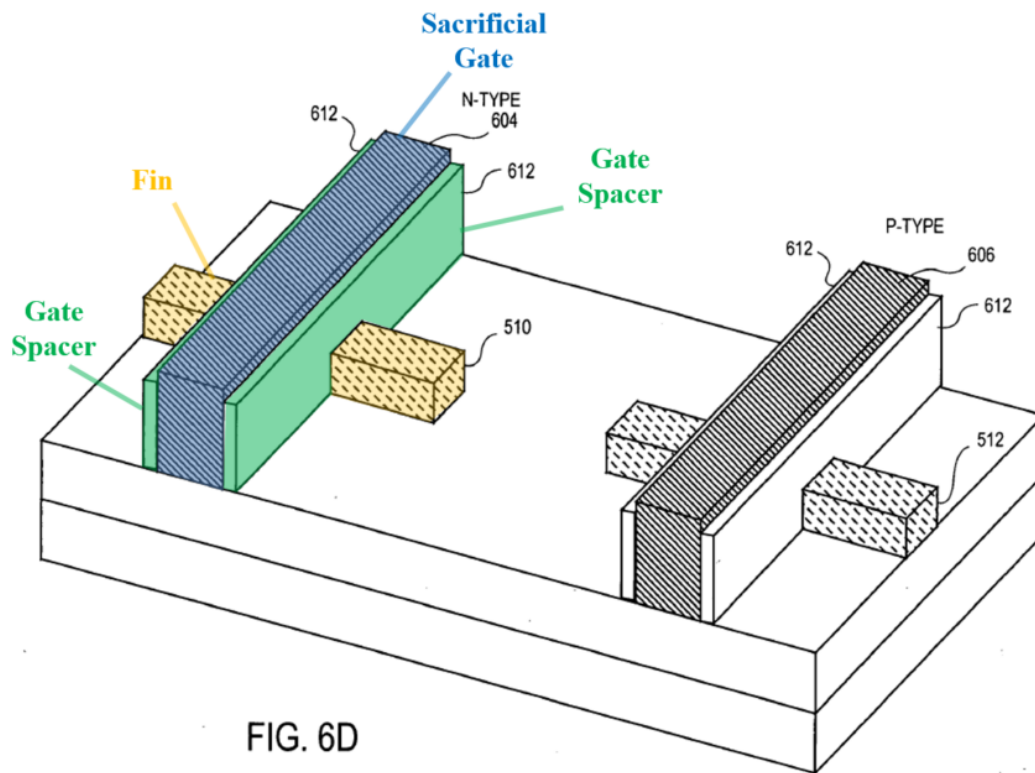


FIG. 6D

(Ex. 1008, FIG. 6D; Ex. 1002, ¶118.)

Brask discloses that the gate spacers are formed by blanket depositing a dielectric layer (“depositing a dielectric material layer over the sacrificial non-planar transistor gate and the non-planar transistor fin”) and then etching to remove the dielectric material from the areas other than the sidewalls of the gate electrode (“forming non-planar transistor gate spacers from a portion of the dielectric material layer adjacent the sacrificial non-planar transistor gate”):

[D]ielectric sidewall spacers 612 can be formed along opposite sidewalls of the sacrificial gate electrodes 604

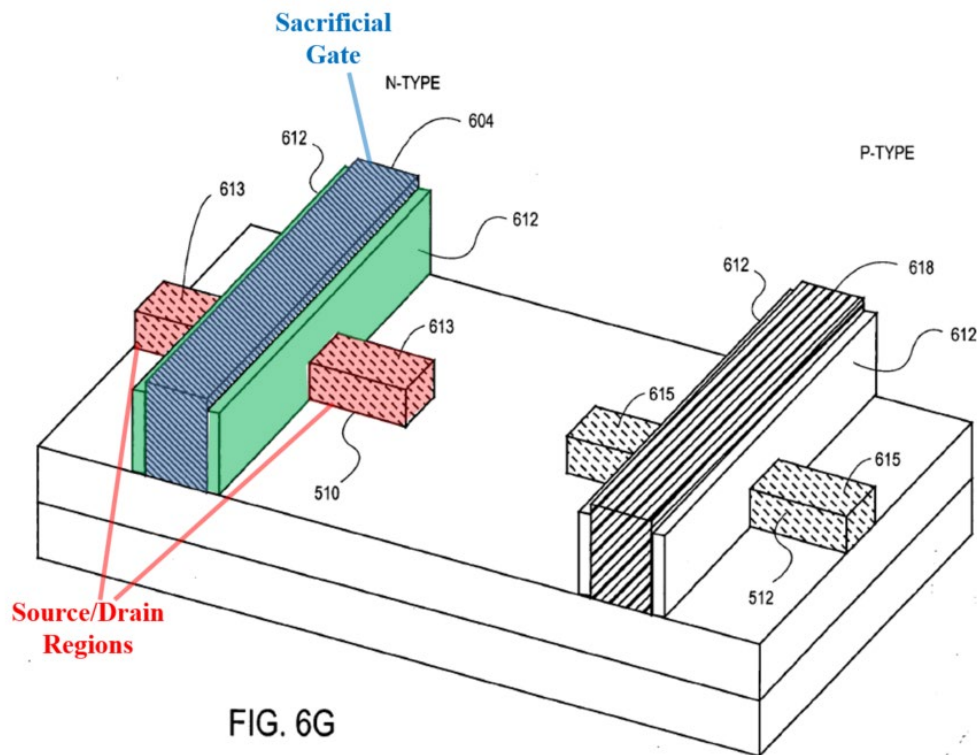
and 606 ... by any well known techniques, such as by blanket depositing the conformal sidewall spacer dielectric over the substrate including the top surface and sidewalls of the sacrificial gate electrodes 604 and 606 as well as on the top surface and sidewalls of semiconductor bodies 510 and 512 as well as onto the exposed surface of the insulating substrate. ... The dielectric spacer material is then anisotropically etched back to remove the dielectric spacer material from a horizontal surface (e.g., top surface) of the sacrificial gate electrodes 604 and 606 and the top surface of the semiconductor bodies 510 and 512 and insulating substrate 602, while leaving spacer material on the vertical surfaces (e.g., sidewalls) of sacrificial gate electrodes 604 and 606 to form sidewall spacers 612 as shown in FIG. 6D.

(Ex. 1008, ¶[0065]; Ex. 1002, ¶119.)

e) Element 1[e]

Brask discloses this feature. (Ex. 1002, ¶120.) As shown in annotated figure 6G below, Brask discloses that “additional silicon can be formed onto the exposed top surface and sidewalls of the semiconductor bodies 510 and 512 in order to form raised source and drain regions.” (Ex. 1008, ¶[0066].) Heavy source/drain contact regions are then formed in the semiconductor bodies 510 and 512 on opposite sides

of the sacrificial gate (*id.*, ¶¶[0067]-[0068]), and then annealing is used to activate the dopants in the semiconductor bodies 510 and 512 to form the n-type source/drain regions 613 and p-type source/drain regions 615 (*id.*, ¶[0069].) (Ex. 1002, ¶120.)

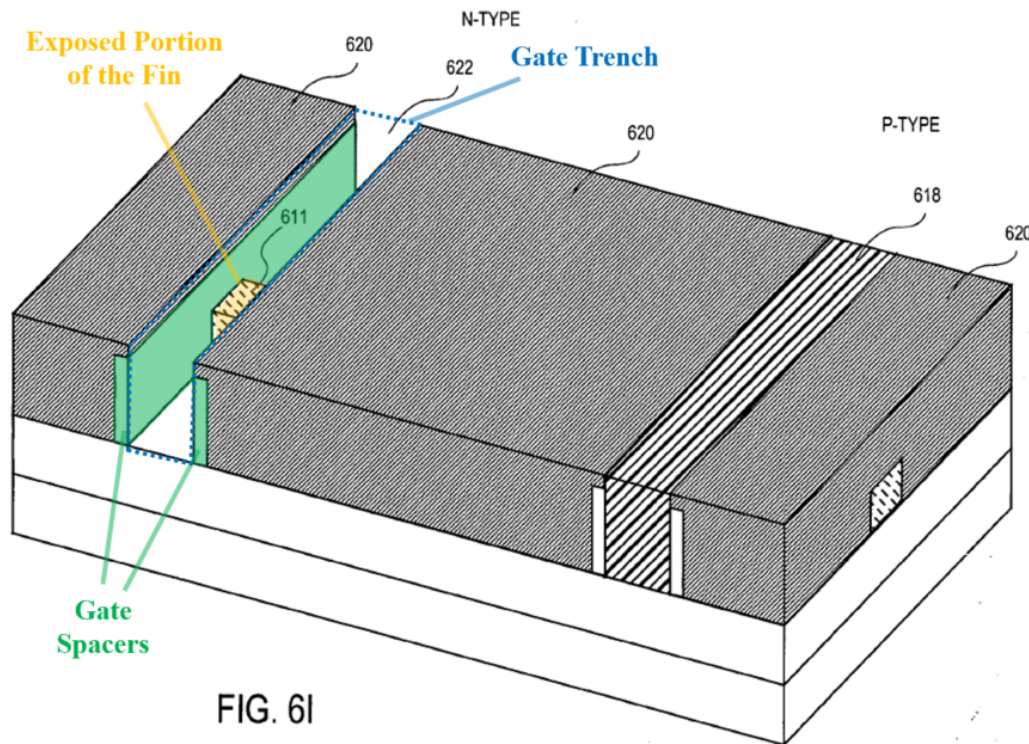


(Ex. 1008, FIG. 6G (annotated); Ex. 1002, ¶120.)

f) Element 1[f]

Brask discloses these features. (Ex. 1002, ¶121.) As illustrated in annotated figure 6I below, Brask discloses removing the sacrificial gate structure, which includes the gate electrode 604 and gate dielectric layer 602 for the n-type transistor,

to form opening 622 between the spacers (“gate trench between the non-planar transistor gate spacers”) that exposes the channel region 611 of the semiconductor body 510 (“a portion of the non-planar transistor fin”). (Ex. 1008, ¶¶[0072]-[0073]; Ex. 1002, ¶121.)



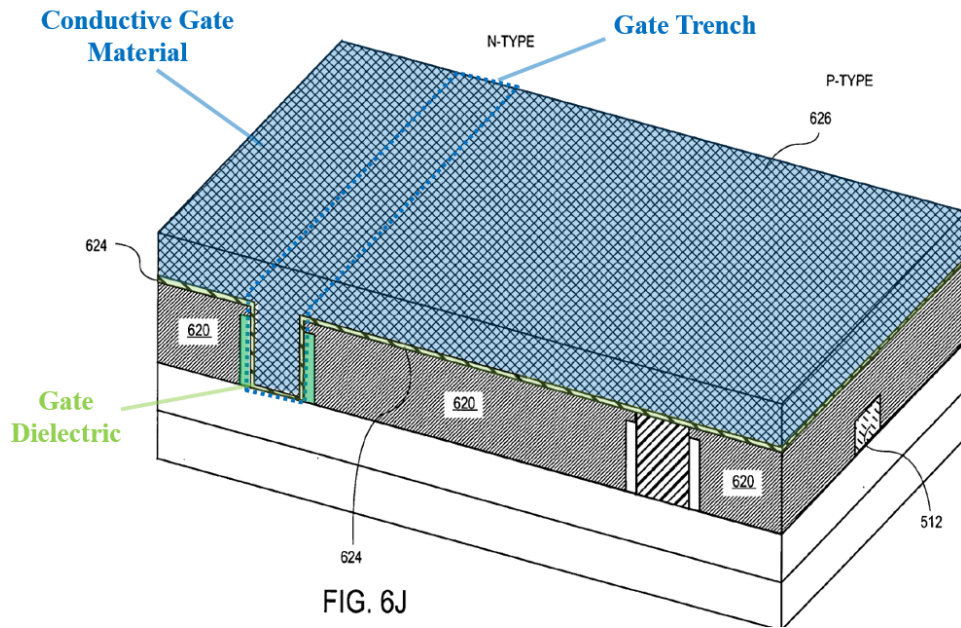
(Ex. 1008, FIG. 6I (annotated); Ex. 1002, ¶121.)

g) Element 1[g]

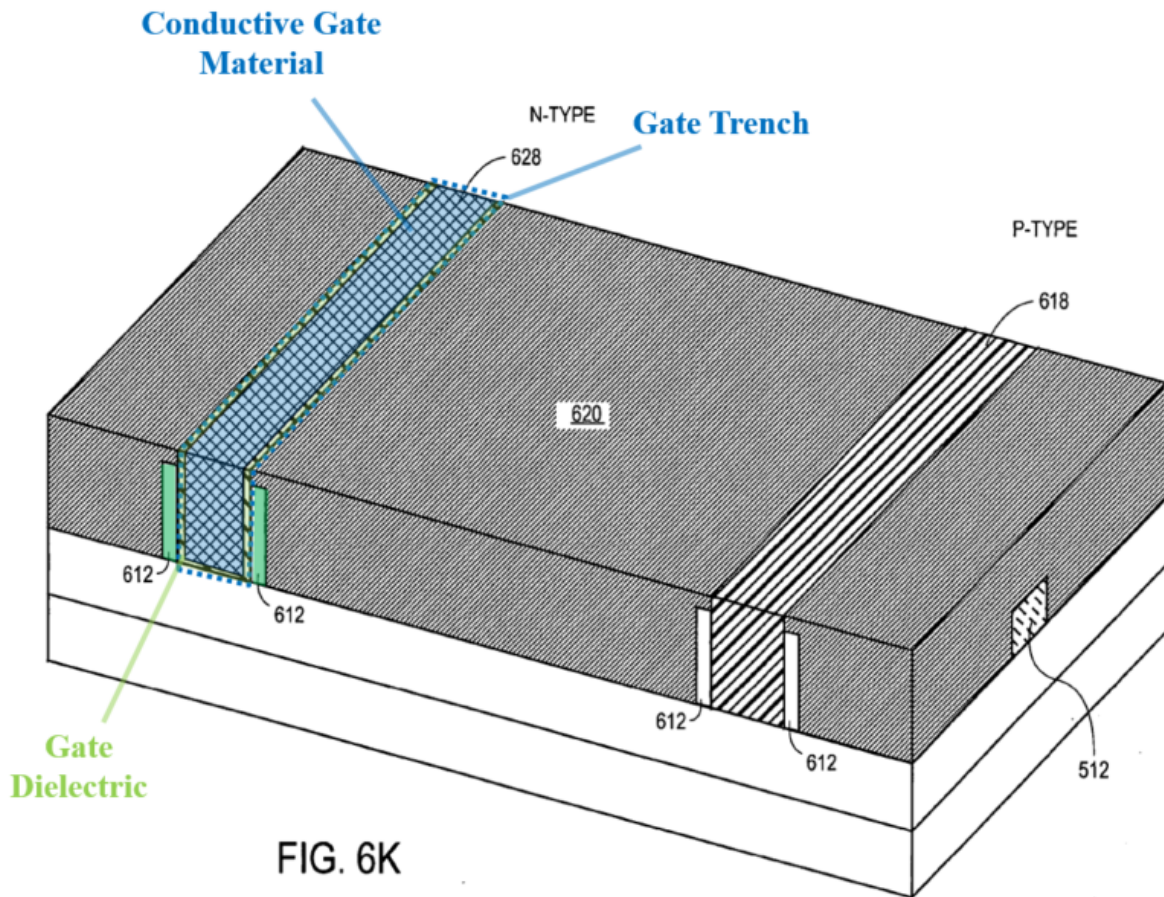
h) Element 1[h]

Brask discloses these features. (Ex. 1002, ¶122.) As illustrated in annotated figures 6J and 6K below, Brask discloses forming a replacement gate structure in the opening 622 (“gate trench”), where the replacement gate structure includes gate

dielectric film 624 formed on the channel region 611 (“adjacent the non-planar transistor fin”) and gate electrode material 626 (“conductive gate material”) deposited in the gate trench for the n-type transistor. (Ex. 1008, ¶[0074]; Ex. 1002, ¶122.)



(Ex. 1008, FIG. 6J (annotated); Ex. 1002, ¶122.)



(Ex. 1008, FIG. 6K (annotated); Ex. 1002, ¶122.)

i) **Element 1[i]**

j) **Element 1[j]**

The Brask-Cheng combination discloses or suggests these features. (Ex. 1002, ¶¶123-133.) While Brask discloses the formation of a non-planar transistor and recognizes that electrical connections to the transistor are required, Brask does not provide explicit disclosure of providing a source/drain contact. (Ex. 1008, ¶[0079]; Ex. 1002, ¶123.) Cheng, however, discloses additional steps that enable

the interconnection of a transistor to surrounding circuitry using a borderless (self-aligned) contact, and a POSITA would have found it obvious to implement such a borderless source/drain contact in conjunction with Brask's transistor. (Ex. 1002, ¶124.)

Like Brask, Cheng's third embodiment is related to transistors that utilize sacrificial gate structures, and a POSITA implementing a transistor like that disclosed by Brask would have had reason to look to Cheng. (Ex. 1007, ¶[0052]; Ex. 1002, ¶125.)

Cheng discloses that FinFETs have allowed the size of FET transistors to be reduced, which in turn has reduced the critical dimensions (CDs) of those transistors, thereby making the formation of contacts more difficult. (Ex. 1007, ¶¶[0008]-[0009]; Ex. 1017, 3 (FIG. 1-2); Ex. 1018, 1; Ex. 1019, 1; Ex. 1002, ¶125.) In this context, Cheng discloses that "[b]orderless contacts and techniques relating thereto help reduce the amount of space required for contacts, and enable production of smaller devices having a tighter pitch." (*Id.*, ¶[0009]; *see also id.*, ¶[0031] ("As noted above, device scaling results in a small space for forming the borderless contact."); Ex. 1002, ¶126.) Therefore, a POSITA would have understood that Cheng discloses or suggests that borderless contacts (i.e., self-aligned contacts) are

applicable to devices with reduced critical dimensions like the FinFET disclosed by Brask. (Ex. 1002, ¶126.)

Cheng's transistor formation, like that of Brask, includes removal of dummy gates (e.g. sacrificial gates) and then formation of a replacement gate structure in the resulting opening between gate spacers, where the gate is formed by first depositing a dielectric layer and then depositing conductive gate material in the form of a metal gate. (Ex. 1007, ¶[0053] (“As depicted in FIG. 22, a high-k dielectric (HKD) 330 is deposited over the structure (e.g., the entire structure, including the ILD 324). Subsequently, and as shown in FIG. 23, a metal gate (MG) 332 is deposited, planarized and recessed.”), ¶¶[0043], [0051]; Ex. 1002, ¶127.)

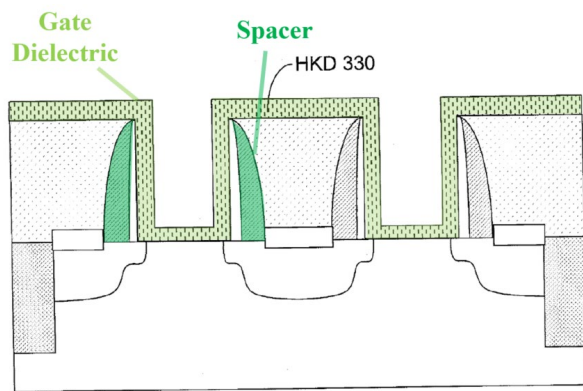


FIG. 22

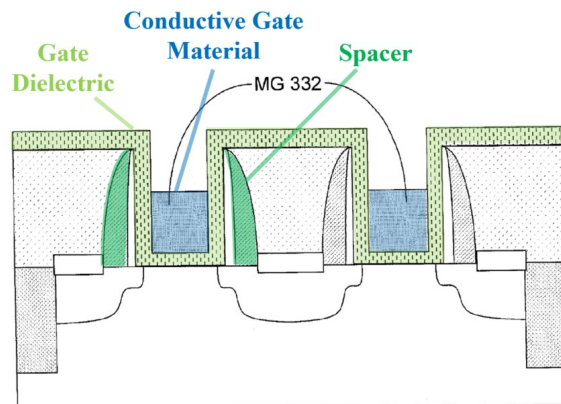


FIG. 23

(Ex. 1007, FIGs. 22, 23 (annotated); Ex. 1002, ¶127.)

Cheng further discloses that after depositing the metal gate, the gate material is recessed in order to allow for formation of a cap (Ex. 1007, ¶[0054]) that, along with spacers, isolates the gate from a subsequently formed borderless contact:

The exemplary technique illustrated by FIGS. 20-26 depict the formation of a borderless contact ... **The borderless contact is isolated from the gate by a spacer(s) and insulating cap layer (CAP2 340).**

(Ex. 1007, ¶[0055]; Ex. 1002, ¶128.)

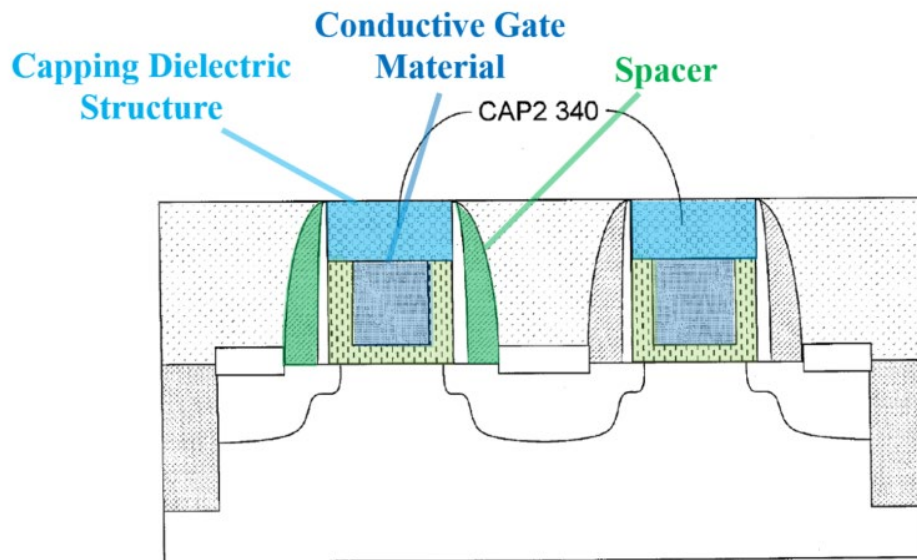


FIG. 25

(Ex. 1007, FIG. 25 (annotated); Ex. 1002, ¶128.)

A POSITA would have found it obvious to form, and been motivated to form, a contact to the source/drain region in a transistor like that disclosed by Brask based

on the disclosure of Cheng both because Brask does not provide any description as to how to form such contacts and because the borderless or self-aligned contact formation technique of Cheng provides advantages applicable to FinFET devices. (Ex. 1002, ¶129.) As discussed above in section IX.A.1[i]-[j], self-aligned borderless contacts are useful in devices having reduced critical dimensions (e.g. gate length) such as FinFETs as they allow the contact to be formed closer to the gate structure, reduce the risk of shorting, reduce the area needed to form the transistor and associated interconnect, and provide increased tolerance with respect to possible lithographic misalignment. (Section IX.A.1[i]-[j]; Ex. 1007, ¶¶[0008]-[0009]; Ex. 1020, ¶¶[0002]-[0003], [0008]; Ex. 1002, ¶129.) Therefore, a POSITA would have been motivated to form self-aligned borderless contacts to provide the needed connections to the transistor of the Brask-Cheng combination. (Ex. 1002, ¶129.)

Such borderless contact formation includes removing a portion of the conductive material corresponding to the gate electrode to form a recess between the gate spacers as recited in claim element 1[i]. (Ex. 1007, ¶[0054]; Ex. 1002, ¶130.) Following recessing of the gate material, a cap (“capping dielectric structure”) is formed in the recess, where, as disclosed by Cheng, the cap is a nitride cap. (Ex. 1007, ¶[0054], (“CAP2 340 may comprise a nitride cap”).) A POSITA would have

understood that the cap protects the gate electrode from being damaged during the etching process and provides electrical isolation for the gate structure to avoid unwanted shorts between the gate and other contacts (e.g., source/drain contacts). (Ex. 1002, ¶130; Ex. 1007, ¶[0055]; Ex. 1006, ¶¶[0059]-[0072] (disclosing a protective cap structure to protect the gate structure from being damaged by an etching process to form a contact hole).)

Cheng discloses that “CAP2 340 may be formed by deposition and planarization” (Ex. 1007, ¶[0054]), where Cheng further discloses that such deposition can be performed using high density plasma CVD (HDPCVD). (Ex. 1007, ¶[0085] (“Unless described otherwise herein, **“depositing” may include any now known or later developed techniques appropriate for the material to be deposited, including, but not limited to: ... high density plasma CVD (HDPCVD), ...**”); Ex. 1002, ¶131.)

A POSITA would have found it obvious to use high density plasma deposition to form the dielectric cap based on Cheng’s disclosure and their knowledge that such deposition provides superior gap-filling capabilities and therefore is suited to filling the recess formed between the spacers in the transistor of the Brask-Cheng combination. (Ex. 1010, 6:32-37; Ex. 1015, 1:65-2:2; Ex. 1016, 1:65-2:6; Ex. 1002, ¶132.) Therefore, the Brask-Cheng combination discloses or suggests that the

dielectric cap (“capping dielectric structure”) is formed by high density plasma depositing as recited in claim element 1[j]. (Ex. 1002, ¶133.)

Forming a contact for the transistor of the Brask-Cheng combination would have simply been the use of known techniques (e.g., forming borderless source/drain contacts as disclosed by Cheng) to a known device (Brask’s FinFET) ready for improvement to yield predictable results of a FinFET device having a borderless source/drain contact. (*Id.*) See *KSR* at 416-18. Therefore, the Brask-Cheng combination discloses or suggests claim elements 1[i] and 1[j], as these steps are included in the borderless contact formation process disclosed by Cheng that a POSITA would have found it obvious to use in conjunction with a transistor as disclosed by Brask. (Ex. 1002, ¶133.)

k) Element 1[k]

The Brask-Cheng combination discloses or suggests this feature. (Ex. 1002, ¶¶134-135.) As discussed above for claim elements 1[i]-1[j], the Brask-Cheng combination discloses or suggests the formation of a borderless contact. (Sections IX.C.1[i]-[j].) Cheng discloses that, as a part of the contact formation process and before etching to form contact area 326, an interlayer dielectric layer ILD2 is deposited over the cap 340, gate spacers, and source/drain regions. (Ex. 1007,

¶[0054] (“[A]s shown in FIG. 26, a second layer of ILD (ILD2) 342 is deposited and planarized.”), FIG. 26; *see also id.*, ¶[0029]; Ex. 1002, ¶134.)

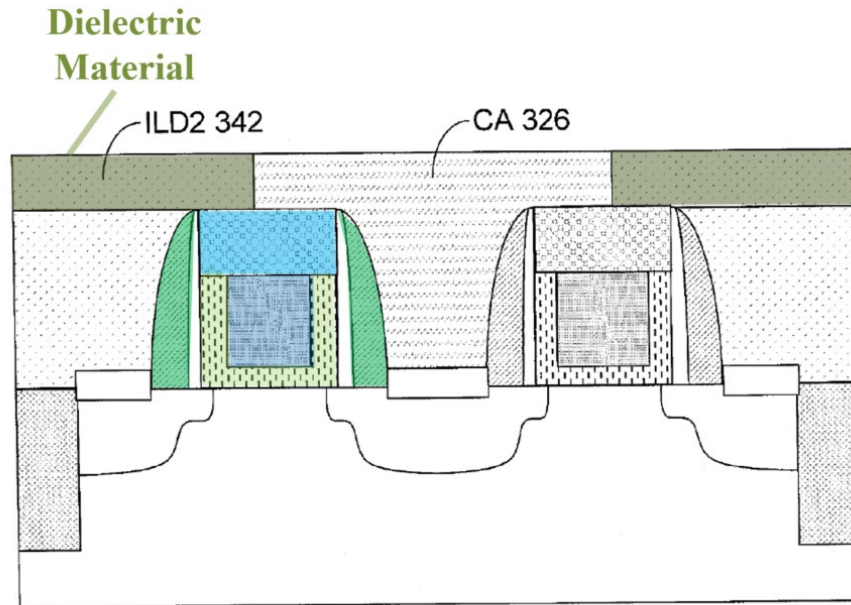


FIG. 26

(Ex. 1007, FIG. 6 (annotated); Ex. 1002, ¶134.)

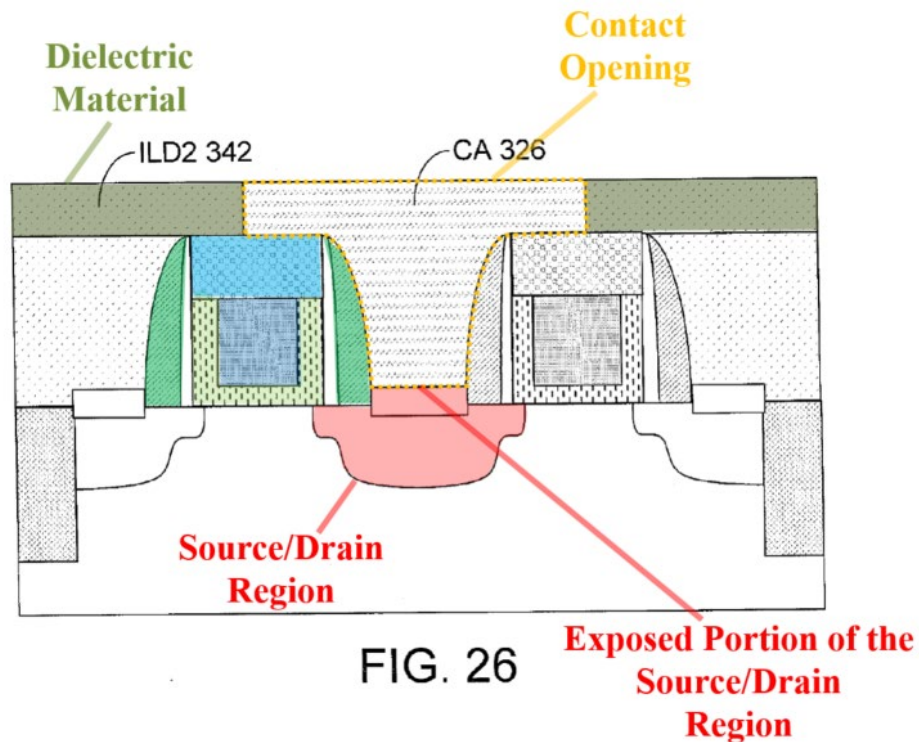
A POSITA would have understood that the interlevel dielectric layer is used to separate layers within the integrated circuit structure and isolate different contact structures (e.g., source/drain contacts) and would have been motivated to include such a dielectric layer. (Ex. 1002, ¶135.)

I) Element 1[i]

The Brask-Cheng combination discloses or suggests this feature. (Ex. 1002, ¶¶136-138.) As discussed above for claim elements 1[i]-1[j], the Brask-Cheng

combination discloses or suggests the formation of a borderless contact. (Sections IX.C.1[i]-[j].) Cheng discloses etching to form the space (“contact opening”) for contact area (CA) 326 through the interlevel dielectric layer 342 (“the at least one dielectric material”) and ILD 324 to expose the underlying source/drain region⁷ as a part of the contact formation process. (Ex. 1007, ¶[0054] (“A contact mask and a contact RIE are used to remove the ILD material from between the gates, thus forming the space for the borderless contact.”), FIG. 26.); Ex. 1002, ¶136.)

⁷ While Cheng discloses that “[s]ilicide may be formed at the source/drain regions” (Ex. 1007, ¶[0051]), a POSITA would have understood that silicides provide improved contact to the source/drain regions and are optional, which is consistent with the disclosure of Cheng. (Ex. 1002, ¶137; Ex. 1007, ¶[0048] (“To reduce resistance, there **may be** a silicide (SIL) 22 over the S/D 216.”).) A POSITA would have understood that silicides need not be included in the Brask-Cheng transistor. (Ex. 1002, ¶137.)



(Ex. 1007, FIG. 26 (annotated)⁸; Ex. 1002, ¶137.)

Consistent with the disclosure of Cheng, a POSITA would have understood that such an opening allows for the subsequent deposition of conductive material to provide electrical contact to the source/drain region. (Ex. 1007, ¶[0054]; Ex. 1002, ¶138.)

⁸ Annotated figure 26 shows silicide 222 as part of the source/drain region, but a POSITA would have known that such a silicide is optional such that the opening exposes the source/drain region directly. (See note 7.)

2. Claim 2

The Brask-Cheng combination discloses or suggests this feature. (Ex. 1002, ¶¶139-141.) As discussed above for claim element 1[j], the Brask-Cheng combination discloses or suggests forming a dielectric (“capping dielectric structure”) over the conductive material of the gate structure using high density plasma depositing according to the teaching of Cheng. (Section IX.C.1(j).) Cheng further discloses that the dielectric material can be “nitride.” (Ex. 1007, ¶[0054] (“CAP2 340 may comprise a nitride cap.”); Ex. 1002, ¶139.)

To the extent that Cheng does not disclose that the “nitride” used to form the cap is silicon nitride, a POSITA would have found it obvious to form the nitride capping layer using silicon nitride. (*Id.*, ¶140.) Cheng discloses that the spacers and capping layer isolate the gate region from the formed contact, and that the dielectric material of the spacers and capping layer is not removed when the etch to form the contact hole is performed. (Ex. 1007, ¶[0054].) Cheng further discloses silicon nitride spacers (*id.*, ¶[0043]), and a POSITA would have understood that using silicon nitride for both the cap and spacers would provide the ability to perform selective etches that remove the interlayer dielectric while leaving the silicon nitride cap and spacers. (Ex. 1006, ¶[0062]; Ex. 1002, ¶¶140-141.)

3. Claim 5

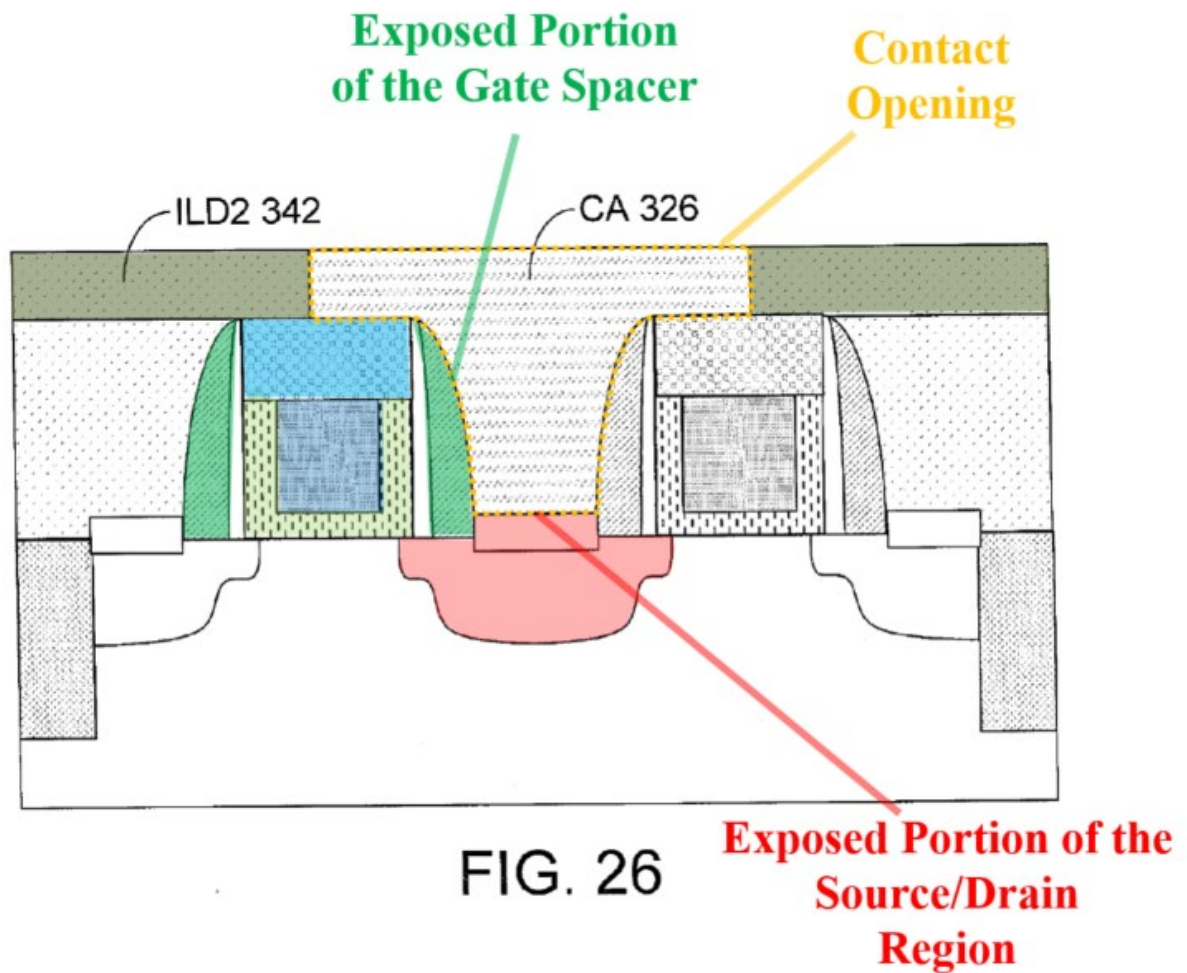
The Brask-Cheng combination discloses or suggests this feature. (Ex. 1002, ¶¶142-143.) As discussed above for claim element 1[j], the Brask-Cheng combination discloses or suggests forming a cap (“capping dielectric structure”) over the conductive material of the gate structure using high density plasma depositing. (Section IX.C.1(j).) Cheng further discloses that after deposition of the material for the cap, planarization occurs, which a POSITA would have understood removes excess capping dielectric material. (Ex. 1007, ¶[0054] (“The CAP2 340 may be formed by deposition and planarization.”); Ex. 1002, ¶142; *see also* Ex. 1006, ¶[0064].)

A POSITA would have been motivated to include such a step in the self-aligned contact formation process to promote formation of subsequent overlying layers. (Ex. 1002, ¶143.)

4. Claim 6

The Brask-Cheng combination discloses or suggests this feature. (Ex. 1002, ¶¶144-146.) As discussed above for claim element 1[l], the Brask-Cheng combination discloses or suggests forming a contact opening as disclosed by Cheng to expose a portion of the source/drain region. (Section IX.C.1(l).) As shown in annotated figure 26 below, Cheng discloses that the etching operation used to form

that opening does not remove the cap and spacers, which isolate the gate from the subsequently formed contact, where the opening exposes a portion of the spacer and a portion of the insulating cap layer. (Ex. 1007, ¶[0055], FIG. 26; Ex. 1002, ¶¶144-146; *see also* Ex. 1006, ¶¶[0068]-[0070].)

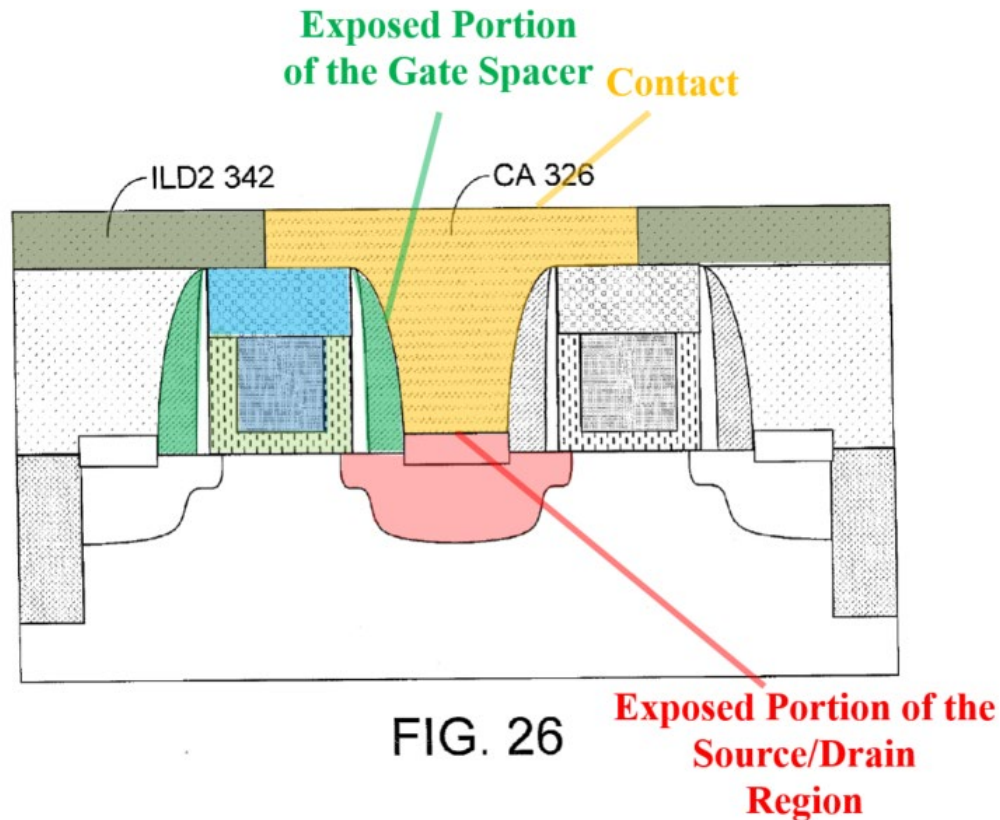


(Ex. 1007, FIG. 26 (annotated); Ex. 1002, ¶144.)

5. Claim 7

The Brask-Cheng combination discloses or suggests this feature. (Ex. 1002, ¶147.) As discussed above for claim element 1[l] and claim 6, the Brask-Cheng combination discloses or suggests forming a contact opening to expose a portion of the source/drain region and a portion of the gate spacer. (Sections IX.C.1(l), IX.C.4.) Cheng further discloses that the space corresponding to the contact area (CA) 326 is filled with conductive metal to form the contact for the transistor. (Ex. 1007, ¶[0054]; Ex. 1002, ¶147.) Therefore, the self-aligned contact formation of the Brask-Cheng combination fills the contact hole with conductive material to form a source/drain contact, where, because it fills the opening, the contact abuts the exposed portions of the source/drain region and the gate spacer. (Ex. 1002, ¶147.) Annotated figure 26 of Cheng shows the filled contact abutting the exposed portions of the source/drain region and gate spacer.⁹ (*Id.*)

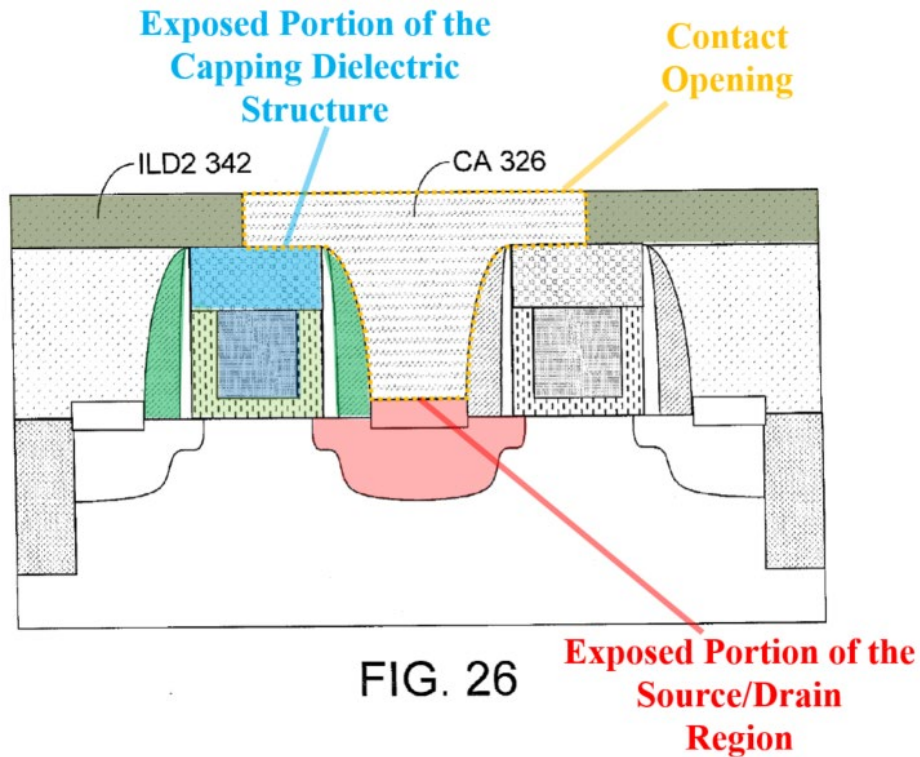
⁹ The silicide 222 in figure 26 is optional. (*See* note 7.)



(Ex. 1007, FIG. 26 (annotated); Ex. 1002, ¶147.)

6. Claim 8

The Brask-Cheng combination discloses or suggests this feature for the same reasons discussed above for claim 6, where, as shown in annotated figure 26 of Cheng below, the selective etching of the Brask-Cheng combination exposes a portion of the source/drain region and a portion of the insulating cap layer (“capping dielectric structure”). (Section IX.C.4; Ex. 1002, ¶¶148-149.)



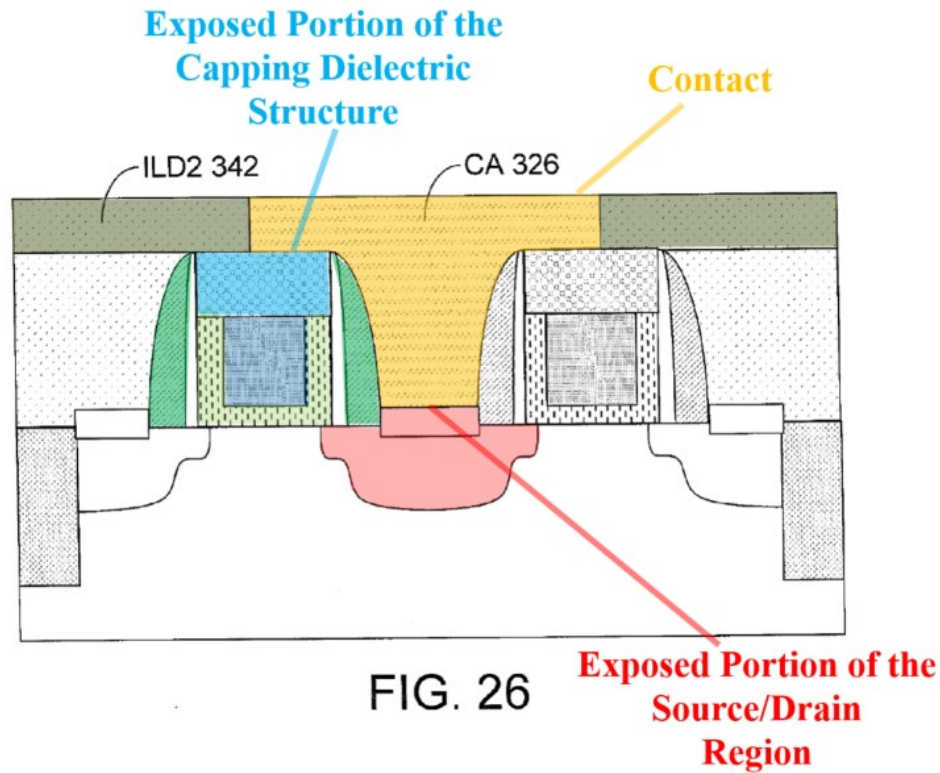
(Ex. 1007, FIG. 26 (annotated); Ex. 1002, ¶148.)

7. Claim 9

The Brask-Cheng combination discloses or suggests this feature to the extent it can be understood¹⁰ for the same reasons discussed above for claim 7, where, as shown in annotated figure 26 of Cheng below, the contact abuts the exposed portions

¹⁰ See note 5.

of the source/drain region and the insulating cap layer (“capping dielectric structure”).¹¹ (Section IX.C.5; Ex. 1002, ¶150.)



(Ex. 1007, FIG. 26 (annotated); Ex. 1002, ¶150.)

8. Claim 10

The Brask-Cheng combination discloses or suggests this feature for the reasons presented above for claims 6 and 8. (Sections IX.C.4, 6; Ex. 1002, ¶151.)

¹¹ The silicide 222 in figure 26 is optional. (See note 7.)

9. Claim 11

The Brask-Cheng combination discloses or suggests this feature for the reasons presented above for claims 7 and 9. (Sections IX.C.5, 7; Ex. 1002, ¶152.)

D. Ground 4 – Brask in View of Cheng and Park Renders Claims 1, 2, and 4-11 Obvious

1. Claims 1, 2, and 5-11

As discussed above in Section IX.C, the Brask-Cheng combination discloses or suggests the features of claims 1, 2, and 5-11, including claim element 1[j], which requires “forming a capping dielectric structure within the recess by high density plasma depositing a dielectric material.” (Section IX.C.) To the extent PO argues that the Brask-Cheng combination does not disclose or suggest forming the capping dielectric by “high density plasma deposition,” a POSITA would have found it obvious to form the capping layer using high density plasma chemical vapor deposition (HDPCVD) in view of Park and their knowledge of the state of the art. (Ex. 1002, ¶¶153-156.)

Park, like Brask and Cheng, is directed to forming transistors with improved performance, where, like Cheng, Park discloses a forming a nitride capping layer overlying the transistor structure using HDPCVD, where Park is specific that the “nitride” capping layer is silicon nitride. (Ex. 1010, Abstract, 1:14-17, 6:32-37; Ex. 1002, ¶154.)

In view of Park, a POSITA would have found it obvious to form the nitride capping layer in a transistor of the Brask-Cheng combination discussed above in section IX.C using HDPCVD to deposit silicon nitride. (Ex. 1002, ¶155.) Park discloses that silicon nitride is an appropriate material to use for a capping layer, and further discloses that HDPCVD is an appropriate method to deposit such a capping layer. (Ex. 1010, 6:32-37.) A POSITA would have understood that HDPCVD is one of a finite number of identified and predictable options for depositing silicon nitride capping layers (as disclosed by Park), and would have found it obvious to try using HDPCVD to form the silicon nitride capping layer with a reasonable expectation of success. (Ex. 1002, ¶155.) *See KSR* at 416-18. Moreover, doing so would have been nothing more than the application of a known technique (HDPCVD deposition of silicon nitride) to a known device ready for improvement (the transistor of the Brask-Cheng combination) to yield predictable results (a functional transistor with a silicon nitride capping layer). (Ex. 1002, ¶155.) *See KSR* at 416-18.

A POSITA would also have understood that using HDPCVD to form the silicon nitride cap can provide certain advantages, including improved gap-fill capability, and would have been motivated to form, and had a high likelihood of success in forming, the capping dielectric structure in the Brask-Cheng combination

in such a manner. (Section IX.B.1; Ex. 1015, 1:65-2:2; Ex. 1016, 1:65-2:6; Ex. 1002, ¶156.)

Therefore, the Brask-Cheng-Park combination discloses or suggests claim element 1[j], whereas the remaining features of claims 1, 2, and 5-11 are disclosed or suggested for the reasons provided above in section IX.C. (Sections IX.C.1-9; Ex. 1002, ¶156.) Moreover, the Brask-Cheng-Park combination also discloses or suggests that the nitride material for the cap (“capping dielectric structure”) is silicon nitride, as recited in claim 2. (Ex. 1002, ¶156.)

2. Claim 4

The Brask-Cheng-Park combination discloses or suggests this feature for similar reasons discussed above for the Cappellani-Siddiqui-Park combination in Section IX.B.2, as Park discloses that the protective cap structure is formed using high density plasma chemical vapor deposition (HDPCVD) at a temperature of 350-500° C, which is within the claimed range of 300-600° C. (Ex. 1002, ¶157; Ex. 1010, 6:32-37.)

E. Ground 5 – Brask in View of Siddiqui Renders Claims 1, 2, and 5-11 Obvious

1. Claim 1

Elements 1[a]-1[h]

Brask discloses these claim features for the same reasons presented in sections IX.C.1(a)-(h) above. (Ex. 1002, ¶¶158-164.)

Elements 1[i]-[j]

The Brask-Siddiqui combination discloses or suggests these features. (Ex. 1002, ¶¶165-176.) As discussed above in sections IX.C.1(a)-(h) and IX.C(i)-(j), Brask discloses the formation of a non-planar transistor that includes a replacement gate structure, but does not disclose the additional steps to provide needed electrical connections to the source and drain regions for the transistor. (Ex. 1002, ¶165.)

Siddiqui, however, discloses forming a self-aligned source/drain contact, and a POSITA would have found it obvious to implement such a self-aligned source/drain contact in conjunction with Brask's transistor. (*Id.*, ¶166.)

Like Brask, Siddiqui is related to field effect transistors (FETs) that utilize sacrificial gate structures, and a POSITA implementing a transistor like that disclosed by Brask would have had reason to look to Siddiqui. (Ex. 1006, Abstract, ¶[0022]; Ex. 1002, ¶167.)

Siddiqui discloses forming silicon nitride dielectric spacers 18 on sidewalls of the sacrificial gate structure that can be used together with a silicon nitride protective capping layer over gate to provide the ability to control etching of the opening for the source/drain contacts. (Section IX.A.1(b); Ex. 1006, ¶[0032]-[0034]; Ex. 1002, ¶168.)

As shown in figure 3 below, Siddiqui discloses that after removing the sacrificial gate, a functional gate structure that includes conductive gate material is formed. (Ex. 1006, ¶¶[0040], [0043], [0056]-[0057]; Ex. 1002, ¶169.) Therefore, like Brask, Siddiqui discloses reforming a gate structure that includes a gate dielectric and conductive gate material.

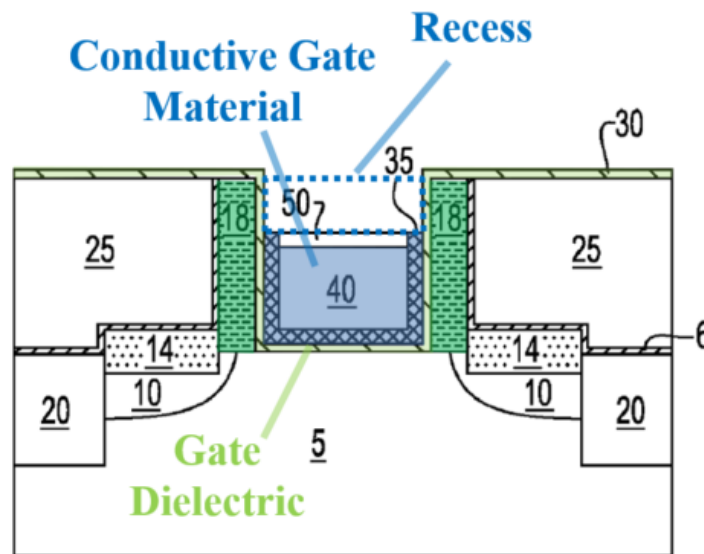


FIG. 3

(Ex. 1006, FIG. 3 (annotated); Ex. 1002, ¶169.)

As discussed for the Cappellani-Siddiqui combination in sections IX.A.1(i)-(j) above, Siddiqui further discloses that the conductive gate material shown in annotated figure 3 above is recessed and a dielectric protective cap structure is formed to protect the gate during etching for the self-aligned contact. (Sections IX.A.1(i)-(j); Ex. 1006, ¶[0058]-[0062]; Ex. 1002, ¶¶170-171.)

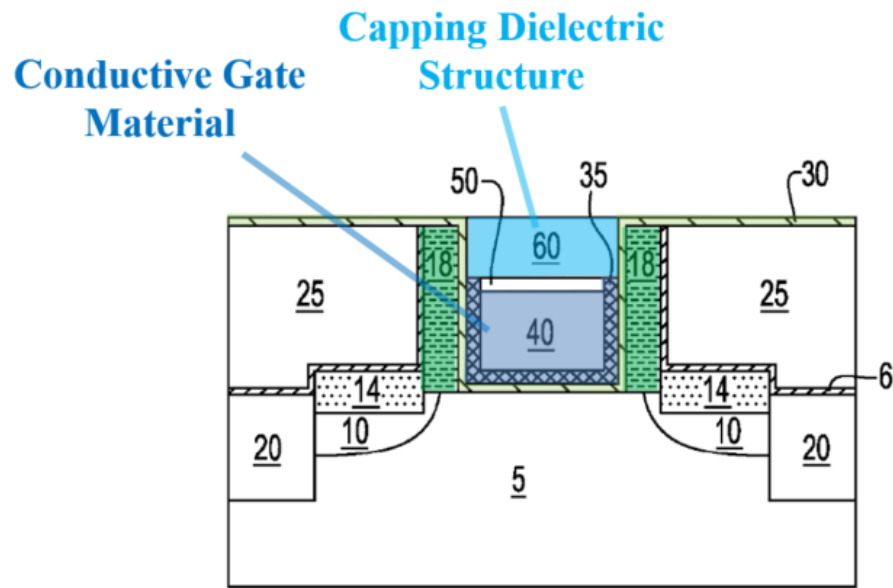


FIG. 4

(Ex. 1006, FIG. 4 (annotated); Ex. 1002, ¶171.)

Therefore, Siddiqui discloses that, in order to form a self-aligned source/drain contact, a capping dielectric structure like that shown in figure 4 above is used to act as an etch stop and protect the gate structure during subsequent etching to form the openings for the contacts. (Ex. 1006, ¶[0062]; Ex. 1002, ¶172.) In view of

Siddiqui's disclosure, a POSITA would have found it obvious to recess the conductive material of the gate in a transistor like that disclosed by Brask to form a recess between the transistor gate spacers, where a capping dielectric structure is then formed in the recess. (Ex. 1002, ¶172.) As disclosed by Siddiqui, these steps are part of the process for forming self-aligned source/drain contacts. (Ex. 1006, ¶[0070]; Ex. 1002, ¶172.)

Brask contemplates the need for electrical connections to the transistor (e.g., source/drain contacts), but does not disclose the steps to form such electrical connections. (Ex. 1008, ¶[0079]; Ex. 1002, ¶173.) Siddiqui, however, provides such disclosure, and a POSITA would have found it obvious to use Siddiqui's contact-formation method in conjunction with a transistor as disclosed by Brask. (Ex. 1002, ¶173.) Formation of the source/drain contacts in a transistor as disclosed by Brask using the methodology disclosed by Siddiqui would have been nothing more than the application of a known technique (Siddiqui's self-aligned contact formation) to a known device (Brask's transistor) ready for improvement (adding electrical connections known to be needed) to yield predictable results (a transistor having connectivity to other circuit elements). (*Id.*) See *KSR* at 417.

A POSITA would have been motivated to use Siddiqui's contact formation technique both because Brask does not provide any description as to how to form

such contacts and because, as discussed above for the Cappellani-Siddiqui combination and the Brask-Cheng combination, such self aligned contacts present advantages applicable to FinFET devices with small dimensions like Brask's transistor. (Sections IX.A.1(i)-(j), IX.C.1(i)-(j); Ex. 1002, ¶174.)

As discussed in sections IX.A.1(i)-(j) Siddiqui discloses or suggests forming the that protective cap structure using "high density plasma deposition" as recited in claim element 1[j]. (Sections IX.A.1(i)-(j); Ex. 1002, ¶175.) Therefore, the Brask-Siddiqui combination discloses or suggests claim elements 1[i] and 1[j], as these steps are included in the self-aligned contact formation process disclosed by Siddiqui that a POSITA would have found it obvious to use in conjunction with a transistor as disclosed by Brask. (Ex. 1002, ¶176.)

Elements 1[k]-[l]

The Brask-Siddiqui combination discloses or suggests these features. (Ex. 1002, ¶¶177-181.) As discussed above for claim elements 1[i]-1[j], the Brask-Siddiqui combination discloses or suggests forming self-aligned contacts for Brask's transistor. A POSITA would have found it obvious to include formation of a dielectric layer as recited in claim element 1[k] and a contact opening as recited in claim element 1[l] as a part of the contact formation in the Brask-Siddiqui combination for the same reasons discussed above for the Cappellani-Siddiqui

combination in sections IX.A.1(k)-(l). (Sections IX.A.1(k)-(l); Ex. 1006, ¶¶[0065]-[0068]; Ex. 1002, ¶¶177-181.)

2. Claim 2

The Brask-Siddiqui combination discloses or suggests this feature for the same reasons presented above with respect to the self-aligned contact formation for the Cappellani-Siddiqui combination in section IX.A.2. (Section IX.A.2; Ex. 1006, ¶[0062]; Ex. 1002, ¶182.)

3. Claim 5

The Brask-Siddiqui combination discloses or suggests this feature for the same reasons presented above with respect to the self-aligned contact formation for the Cappellani-Siddiqui combination in section IX.A.3. (Section IX.A.3; Ex. 1006, ¶[0064]; Ex. 1002, ¶¶183-184.)

4. Claim 6

The Brask-Siddiqui combination discloses or suggests this feature for the same reasons presented above with respect to the self-aligned contact formation for the Cappellani-Siddiqui combination in section IX.A.4. (Section IX.A.4; Ex. 1006, ¶¶[0068]-[0070]; Ex. 1002, ¶¶185-186.)

5. Claim 7

The Brask-Siddiqui combination discloses or suggests this feature for the same reasons presented above with respect to the self-aligned contact formation for the Cappellani-Siddiqui combination in section IX.A.5. (Section IX.A.5; Ex. 1006, ¶[0070]; Ex. 1002, ¶¶187-188.)

6. Claim 8

The Brask-Siddiqui combination discloses or suggests this feature for the same reasons presented above with respect to the self-aligned contact formation for the Cappellani-Siddiqui combination in section IX.A.6. (Section IX.A.6; Ex. 1006, ¶¶[0068]-[0070]; Ex. 1002, ¶¶189-190.)

7. Claim 9

The Brask-Siddiqui combination discloses or suggests this feature for the same reasons presented above with respect to the self-aligned contact formation for the Cappellani-Siddiqui combination in section IX.A.7. (Section IX.A.7; Ex. 1006, ¶[0070]; Ex. 1002, ¶¶191-192.)

8. Claim 10

The Brask-Siddiqui combination discloses or suggests this feature for the reasons presented above for claims 6 and 8. (Sections IX.E.4, 6; Ex. 1002, ¶193.)

9. Claim 11

The Brask-Siddiqui combination discloses or suggests this feature for the reasons presented above for claims 7 and 9. (Sections IX.E.5, 7; Ex. 1002, ¶194.)

F. Ground 6 – Brask in View of Siddiqui and Park Renders Claims 1, 2, and 4-11 Obvious

1. Claims 1, 2, and 5-11

As discussed above in section IX.E, the Brask-Siddiqui combination discloses or suggests the features of claims 1, 2, and 5-11, including claim element 1[j], which requires “forming a capping dielectric structure within the recess by high density plasma depositing a dielectric material.” (Section IX.E.) To the extent PO argues that the Brask-Siddiqui combination does not disclose or suggest forming the capping dielectric by “high density plasma deposition,” a POSITA would have found it obvious to form the capping layer using high density plasma chemical vapor deposition (HDPCVD) in view of Park and their knowledge of the state of the art. (Ex. 1002, ¶¶195-199.)

Park, like Brask and Siddiqui, is directed to forming transistors with improved performance, where, like Siddiqui, Park discloses a nitride capping layer overlying the transistor structure, where Park is specific that the “nitride” capping layer is silicon nitride. (Ex. 1010, Abstract (“forming a first capping nitride layer covering the gate electrode and the source/drain regions, the first capping nitride layer

including a Si—H rich SiN layer”), 1:14-17; Ex. 1002, ¶196.) Park further discloses that the nitride capping layer can be formed using high density plasma chemical vapor deposition (HDPCVD). (Ex. 1010, 6:32-37; Ex. 1002, ¶196.)

In view of Park, a POSITA would have found it obvious to form the silicon nitride protective cap structure in a transistor of the Brask-Siddiqui combination discussed above in section IX.E using HDPCVD to deposit the silicon nitride. (Sections IX.E.1(b), IX.E.2; Ex. 1002, ¶197.) Park discloses that silicon nitride is an appropriate material to use for a capping layer, and further discloses that HDPCVD is an appropriate method to deposit such a capping layer. (Ex. 1010, 6:32-37.) A POSITA would have understood that HDPCVD is one of a finite number of identified and predictable options for depositing silicon nitride capping layers (as disclosed by Park), and would have found it obvious to try using HDPCVD to form the silicon nitride capping layer with a reasonable expectation of success. (Ex. 1002, ¶197.) *See KSR* at 416-18. Moreover, doing so would have been nothing more than the application of a known technique (HDPCVD deposition of silicon nitride) to a known device ready for improvement (the transistor of the Brask-Siddiqui combination) to yield predictable results (a functional transistor with a silicon nitride capping layer). (Ex. 1002, ¶197.) *See KSR* at 416-18.

A POSITA would also have understood that using HDPCVD to form the silicon nitride can provide certain advantages, including improved gap-fill capability, which such a skilled person would have recognized is particularly relevant to formation of the capping dielectric structure in the recessed gate region in the Brask-Siddiqui combination. (Ex. 1015, 1:65-2:2; Ex. 1016, 1:65-2:6; Ex. 1002, ¶198.) Therefore, a POSITA would have been motivated to use HDPCVD for forming the capping dielectric structure in order to avoid voids in the dielectric that could result in unwanted short circuits or damage to the gate structure the dielectric is protecting. (Ex. 1002, ¶198.) Based on their knowledge of the state of the art and Park’s disclosure, a POSITA would have had a high likelihood of success. (*Id.*)

Therefore, the Brask-Siddiqui-Park combination discloses or suggests claim element 1[j], whereas the remaining features of claims 1, 2, and 5-11 are disclosed or suggested for the reasons provided above in section IX.E. (Sections IX.E.1-9; Ex. 1002, ¶199.)

2. Claim 4

The Brask-Siddiqui-Park combination discloses or suggests this feature. (Ex. 1002, ¶200.) As discussed above in section IX.F.1, the Brask-Siddiqui-Park combination discloses or suggests forming protective cap structure (“capping dielectric structure”) over the conductive material of the gate structure using high

density plasma depositing. (Section IX.F.1.) Park further discloses that the nitride capping layer can be formed using high density plasma chemical vapor deposition (HDPCVD) at a temperature of 350-500° C, which is within the claimed range of 300-600° C. (Ex. 1010, 6:32-37; Ex. 1002, ¶200.) Therefore, the Brask-Siddiqui-Park combination discloses or suggests claim 4.

X. Discretionary Denial is not Appropriate

A. The Board Should Not Deny Institution Under *Fintiv*

The six *Fintiv* factors do not justify denying institution.

The **first factor** is neutral because Samsung has not yet moved to stay the district court proceeding. *See, e.g., Hulu LLC v. SITO Mobile R&D IP, LLC et al.*, IPR2021-00298, Paper 11 at 10-11 (PTAB May 19, 2021).

The **second factor** is neutral. Jury selection is scheduled for May 20, 2024. (Ex. 1028, 1.) Even if trial proceeds as scheduled, the timing does not tip in favor of denying institution in this case as a FWD would be expected around October 2024. *See also, e.g., Apple Inc. v. Koss Corp.*, IPR2021-00305, Paper 14 at 13 (PTAB June 3, 2021).

The **third factor** weighs against denial. The district court case is in its early stages, and the Parties' have made little investment to date. PO filed its complaint on September 12, 2022, served its initial infringement contentions on November 17,

2022, and filed an amended complaint on January 24, 2023. Petitioner's diligence in pursuing this petition about seven months after PO's Complaint and not long after receiving the infringement contentions weighs in favor of institution. *Facebook, Inc. v. USC IP P'ship, L.P.*, IPR2021-00033, Paper 13 at 13 (PTAB April 30, 2021) (finding it was reasonable for Petitioner to wait to file the Petition until shortly after receiving infringement contentions). Indeed, Petitioner already filed three IPR petitions against additional patents asserted in the district court litigation, IPR2023-00562, -00563, and 00841.

The **fourth factor** weighs against denial because this Petition challenges claim 4, which is not asserted against Petitioner in district court. This IPR petition is thus the only venue in which certain invalidity challenges will be adjudicated, which promotes system efficiency. *See Fintiv*, Paper 11 at 4. Accordingly, this factor weighs against denial. *See, e.g., Vudu, Inc. v. Ideahub, Inc.*, IPR2020-01688, Paper 16 at 14-15 (PTAB April 19, 2021).

Regarding the **fifth factor**, the Board should give no weight to the fact that Petitioner and PO are the same parties as in district court. *See Weatherford U.S., L.P., v. Enventure Global Tech., Inc.*, IPR2020-01684, Paper 16 at 11-13 (April 14, 2021).

The **sixth factor** (other circumstances) weighs heavily against denial given the undeniable similarity between the prior art references presented herein and the '699 patent. *See Align Technology, Inc. v. 3Shape A/S*, IPR2020-01087, Paper 15 at 42-43 (PTAB Jan 20, 2021); *see also* Section IX. There is also a significant public interest against “leaving bad patents enforceable,” and institution will further that interest. *Thryv, Inc v. Click-To-Call Techs., LP*, 140 S. Ct. 1367, 1374 (2020).

XI. Conclusion

For the foregoing reasons, Petitioner requests IPR and cancellation of claims 1, 2, and 4-11 of the '699 patent.

Respectfully submitted,

Dated: April 20, 2023

By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner

CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(d), the undersigned certifies that the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 9,202,699 contains, as measured by the word processing system used to prepare this paper, 13,307 words. This word count does not include the items excluded by 37 C.F.R. § 42.24 as not counting towards the word limit.

Respectfully submitted,

Dated: April 20, 2023

By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner

CERTIFICATE OF SERVICE

I hereby certify that on April 20, 2023, I caused a true and correct copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 9,202,699 and supporting exhibits to be served via express mail on the Patent Owner at the following correspondence address of record:

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5 Centerpointe Dr.
Suite 400
Lake Oswego, OR 97035

Respectfully submitted,

Dated: April 20, 2023

By: /Naveen Modi/
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