

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SMA SOLAR TECHNOLOGY AMERICA, LLC,
Petitioner,
v.

TIGO ENERGY, INC.,
Patent Owner.

Patent 9,584,021
Filing Date: August 8, 2015
Issue Date: February 28, 2017
Title: SYSTEMS AND METHODS FOR ENHANCED EFFICIENCY
AUXILLARY POWER SUPPLY MODULE

Inter Partes Review No.: IPR2023-00879

**PETITION FOR *INTER PARTES* REVIEW
UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. § 42.100 *et seq.***

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PETITIONER'S EXHIBIT LIST

Exhibit	Description
Ex.1001	U.S. Patent No. 9,584,021
Ex.1002	Certified English Translation of DE3725476 (Mieth)
Ex.1003	U.S. Patent No. 6,246,592 (Balogh)
Ex.1004	U.S. Patent Publication No. 2005/105224 (Nishi)
Ex.1005	U.S. Patent No. 6,798,177 (Liu)
Ex.1006	File wrapper of U.S. Patent No. 9,584,021
Ex.1007	Declaration of Dr. Doug Holberg
Ex.1008	German Language DE3725476 (Mieth)
Ex.1009	Allen, Philip E., and Douglas R. Holberg. "CMOS Analog Circuit Design" (2002) ("CMOS")
Ex.1010	Solibro GmbH Data Sheet, CIGS THIN FILM SOLAR MODULE SL2 ("Solibro")
Ex.1011	MITSUBISHI ELECTRIC Data Sheet, PHOTOVOLTAIC MODULE ("ME")
Ex.1012	US Patent Publication No. 2007/0001653 (Xu)
Ex.1013	U.S. Patent Publication No. 2006/0207192 (Durham)
Ex.1014	Arias et al., "A Modular PV Regulator Based on Microcontroller with Maximum Power Point Tracking," IEEE, IAS 2004
Ex.1015	U.S. Patent No. 4,617,529 (Suzuki)

Note Regarding Page Citations

For exhibits including page numbers as originally published, Petitioner's citations are to those original page numbers for compliance with 37 C.F.R. § 42.63(d)(2)(ii).

Petition for *Inter Partes* Review

SMA Solar Technology America, LLC ("Petitioner") petitions for *inter partes* review of claims 1-20 of U.S. Patent No. 9,584,021 ("the '021 patent")(Ex. 1001).

I. MANDATORY NOTICES PURSUANT TO 37 C.F.R. § 42.8(A)(1), 37 C.F.R. § 42.8(b)(1)&(2):

A. Real Parties in Interest, § 42.8(b)(1)

The real party-in-interest is Petitioner SMA Solar Technology America, LLC. No unnamed entity is funding, controlling, or directing this Petition, or otherwise has had an opportunity to control or direct this Petition or Petitioner's participation in any resulting IPR.

B. Related Matters, § 42.8(b)(2)

Petitioner is not aware of any disclaimers, reexamination certificates or other petitions for *inter partes* review for the '021 Patent. The '021 patent is the subject of a civil action: *Tigo Energy Inc. v. SMA Solar Technology America LLC*, 22-915-VAC (D. Del.).

No references relied upon herein for disclosing elements of the issued claims were cited during prosecution of the '405 patent. It is noted that one reference, Ex. 1012, U.S. Patent Publication No. 2007/0001653 (Xu), that was cited during prosecution of the '405 patent, is not being relied upon herein for teaching any element of the issued claims, but rather is relied upon solely as evidence of the general knowledge of a PHOSITA prior to the priority date of the '405 patent. No arguments presented in this Petition were raised during prosecution of the '405 patent.

37 C.F.R. § 42.8(b)(3)&(4):

C. Lead & Back-Up Counsel and Service Information

Petitioner designates counsel listed below. A power of attorney for counsel is being concurrently filed.

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II. COMPLIANCE WITH THE REQUIREMENTS FOR A PETITION FOR *INTER PARTES* REVIEW

A. Payment of Fees

The undersigned authorizes the charge of fees to Deposit
Account No. 50-1733.

B. Grounds for Standing

This petition is filed within one year of service of a complaint against SMA
Solar Technology America LLC, in *Tigo Energy Inc. v. SMA Solar Technology
America LLC*, 22-915-VAC (D. Del.).

Petitioner certifies the '021 patent is available for review and Petitioner is not barred/estopped from requesting review challenging claims 1-20.

III. OVERVIEW OF THE '021 PATENT

A. Brief Description

The '021 patent is directed to a power supply in a solar system. Ex.1001,1:50-51;Ex.1007,¶63. Figure 4 shows a power supply having a first stage 401 and a second stage 402. The first stage 401 receives an input voltage from a photovoltaic ("PV") panel and outputs a first voltage at a first output. The second stage 402 is connected to the first stage 401. Ex.1001,1:51-56;Ex.1007,¶63. The second stage 402 operates in two states: (1) a first, deactivated state, and (2) a second, enabled state. In the second state the second stage 402 generates a second voltage at a second output using the first voltage to supply a micro-controller with a voltage. Ex.1001,8:41-48;Ex.1007,¶63.

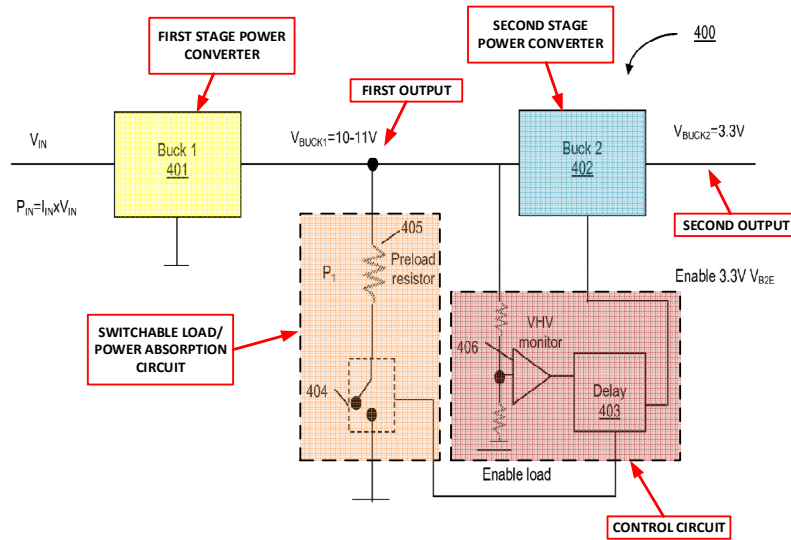
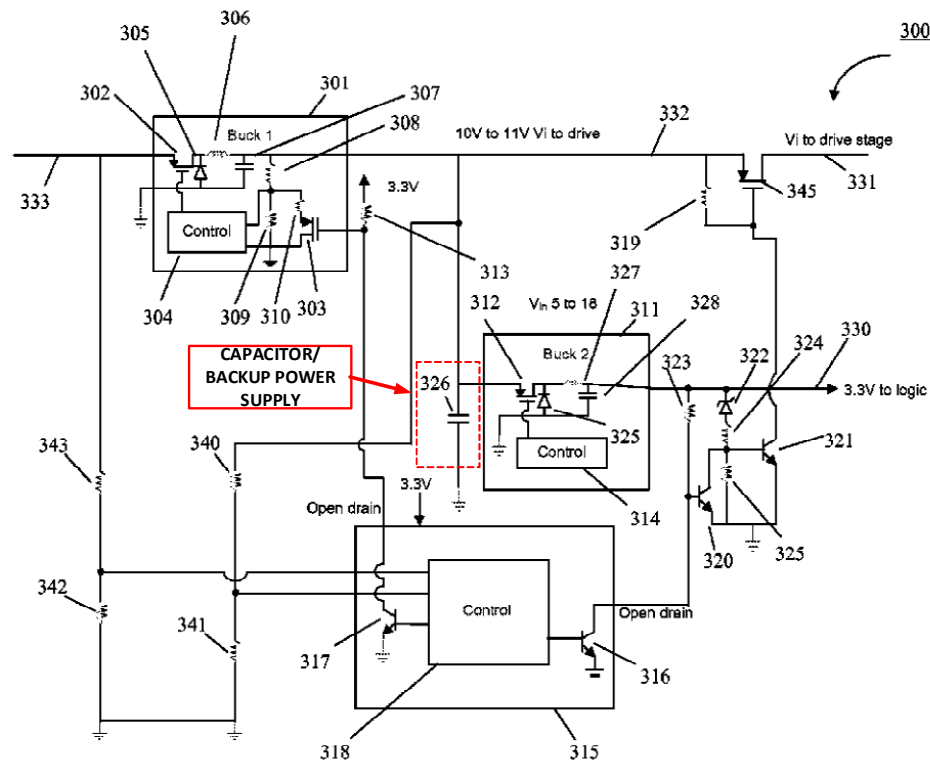


Figure 4

The power supply includes a control circuit (406,403) to prevent false start problems when the solar panel is providing insufficient power. Ex.1001,8:19-22;Ex.1007,¶64. The control circuit, in the first state, connects a preload resistor 405 to the first output by closing a switch 404 via a first control signal to emulate the load of the second stage 402 on the first stage output prior to activating the second stage 402 via a second control signal. Ex.1001,8:22-23,8:35-37;Ex.1007,¶64. If the first stage output voltage exceeds a threshold, the control circuit disconnects the preload resistor 405 by opening the switch 404 via the first control signal. Ex.1001,8:41-45;Ex.1007,¶64. The control circuit employs a delay 403 to delay the second control signal with respect to the first control signal to ensure the second stage operation remains disabled until after the switch 404 is opened, thus providing a “break before make condition,” wherein the switch 404

opens before the second stage 402 is enabled in the second state. Ex.1001,8:40-48;Ex.1007,¶64.

In another embodiment (Figure 3 of Ex.1001), a capacitor 326 is connected to the input of the second stage 311/402. Ex.1001,9:32-34;Ex.1007,¶65.



Ex.1001,Figure3

Capacitor 326 operates as a backup power supply to keep the second stage 311/402 running longer than the first stage 401. Thus, in the first state, the capacitor 326 is charged and absorbs power, and when the first stage 401 is inoperative/unstable, the capacitor discharges to keep the second stage 402 working to provide the second voltage at the second output. Ex.1001,4:60-66;Ex.1007,¶66.

B. Relevant Prosecution History

The '021 patent was filed as App. No. 14/822,227 on August 10, 2015, as a continuation of App. No. 12/787,205 (issued as Patent No. 9,143,036), filed on May 25, 2010, claiming priority to U.S. App. No. 61/275,734, filed on September 2, 2009, and U.S. App. No. 61/336,743, filed on January 26, 2010. Ex.1001,P.1;Ex.1006,P.31. At least 61/275,734, and arguably 61/336,743, does not provide support under 35 U.S.C. §112, first paragraph, for the claimed subject matter. Petitioner does not rely on prior art published in the time period between the priority dates and the non-provisional filing date of May 25, 2010, but reserves the right to challenge the priority date of the '021 Patent.

No substantive Office Actions were issued in the '227 application. An allowance was issued on November 18, 2016. Subsequent to the allowance, an amendment under 37 C.F.R. §1.312 was filed to address an informality. Ex.1006,P.3.

C. Earliest Priority Date for the Claims

The earliest alleged priority date for the '021 patent claims is September 2, 2009. Each reference in the grounds for rejection predates this date and constitutes available prior art under 35 U.S.C. § 311(b).

IV. OVERVIEW OF PRIOR ART

A. DE3725476 (Mieth)(Ex.1002)

Mieth discloses a circuit and method that supplies power to a load 20 from a solar generator 1. Ex.1002,8:8-9;Ex.1007,¶68. For energy sources that vary in performance, like a solar converter (due to time of day/weather conditions), the circuit operates in two different states, depending on the power provided by the energy source at the solar generator 1. Ex.1002,1:23-28;5:22-27;Ex.1007,¶69. In a first state, lower source voltages, a preliminary load 11 is switched “in” to the circuit, while a downstream auxiliary power supply circuit 19 is disabled. In a second state, higher source voltages, the preliminary load 11 is switched “out” of the circuit, and the solar generator 1 is connected to the auxiliary power supply. Ex.1002,1:28-34;claim 1, 2:10-34;Ex.1007,¶69.

Fig.1(annotated A) shows solar generator 1 as an input source that provides direct current to a first stage capacitor 2 that provides a first voltage at a first output.

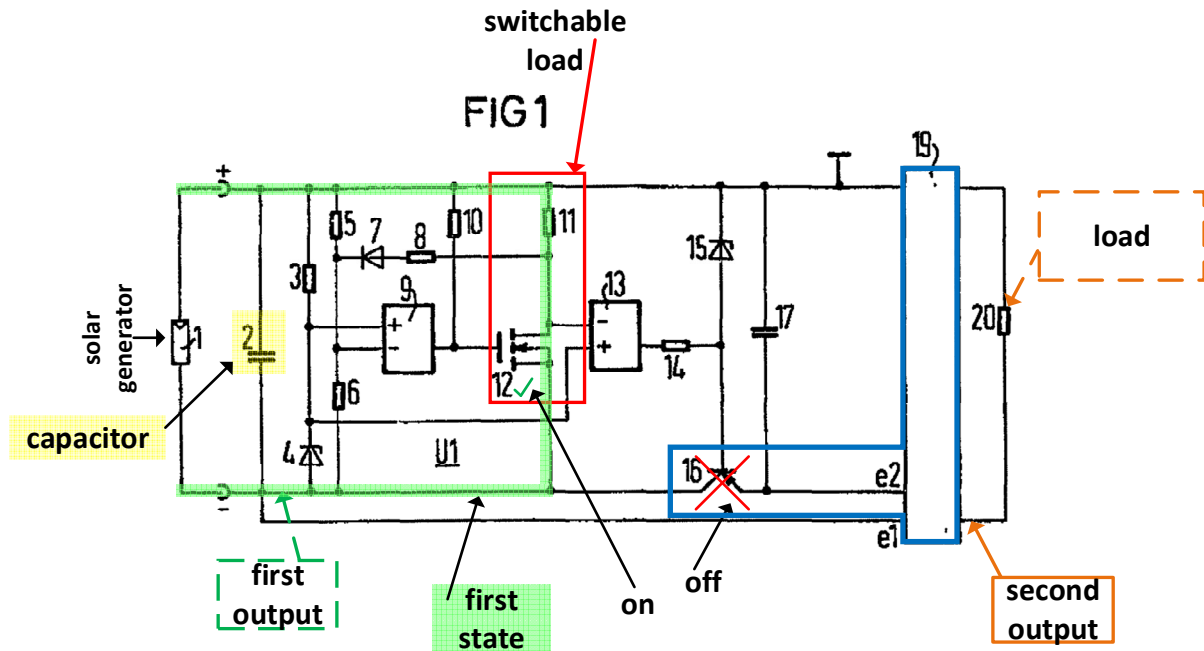
The diagram shows a circuit powered by a solar generator (1) connected to a capacitor (2). The circuit includes two operational amplifiers (9 and 13), several resistors (3, 4, 5, 6, 7, 8, 10, 11, 14, 15, 16, 17), a diode (12), and a load (20). The first output (e1) is taken from the output of the first op-amp (9), and the second output (e2) is taken from the output of the second op-amp (13). The circuit is labeled with component numbers 1 through 20.

Ex.1002, Fig.1(annotated A)

The circuit includes a first comparator 9 and second comparator 13 that operate to generate the first and second states. In the first state, low voltages, first comparator 9 “trips” and switches “in” preliminary load 11, while second comparator 13 is not tripped, resulting in auxiliary power supply 19 being disabled.

Ex.1002,6:14-23;9:15-32;, Ex.1007,¶71.

Fig.1(annotated B) highlights the first state at low source voltages; first comparator 9 is “high” and preliminary load 11 (*i.e.*, resistor 11) is switched “in” due to transistor 12 being “on.”



Ex.1002, Fig.1(annotated B)

Further, in the first state, the second comparator 13 output is “high”, shutting pnp bipolar transistor 16 “off,” and power supply apparatus 19 is disabled.

Ex.1002,12:12-19;Ex.1007,¶73.

Fig.1(annotated C) illustrates the second state when power provided by solar generator 1 provides high voltages at the first output. With higher voltages, the voltage at first comparator 9 exceeds a reference voltage, causing first comparator 9 output to transition “low” and turn off transistor 12 (i.e., “switching out” the switchable load/resistor 11).

in”) is concluded before the second state (when auxiliary power converter 19 is enabled) is initiated. This “break before make” is facilitated by the cascaded first and second comparators 9 and 13. When the voltage at the first output exceeds the reference voltage, the first comparator 9 output goes “low” to turn off transistor 12. Only after transistor 12 stops conducting does the second comparator 13 output transition from “high” to “low” to activate transistor 16. Ex.1007,¶76. Thus, a delay is built into the cascaded comparator arrangement to ensure that the first control signal that disables preliminary load 11 always occurs before the second control signal that enables power supply apparatus 19. Thus, Mieth teaches a delay between first and second control signals. Ex.1007,¶76.

B. U.S. Patent No. 6,246,592 (Balogh)(Ex.1003)

Balogh is a United States patent that issued on June 12, 2001. Balogh discloses that cascaded power converter arrangements that include two or more power converters are well known. Ex.1003,1:21-22;Ex.1007,¶83. Balogh further discloses that cascaded converters are commonly used to provide large input to output voltage conversion ratios. Ex.1003,1:25-28. Solar power applications often employ high voltages where cascaded power converter systems having large input to output voltage conversion ratios are advantageous. Ex.1007,¶¶83-84.

Balogh discloses multiple cascaded buck converter arrangements in prior art Figs.1B-1D, respectively. One is illustrated in Fig.1D shown below.

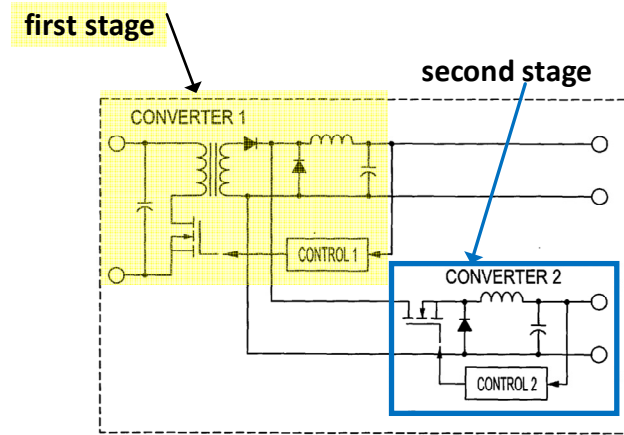


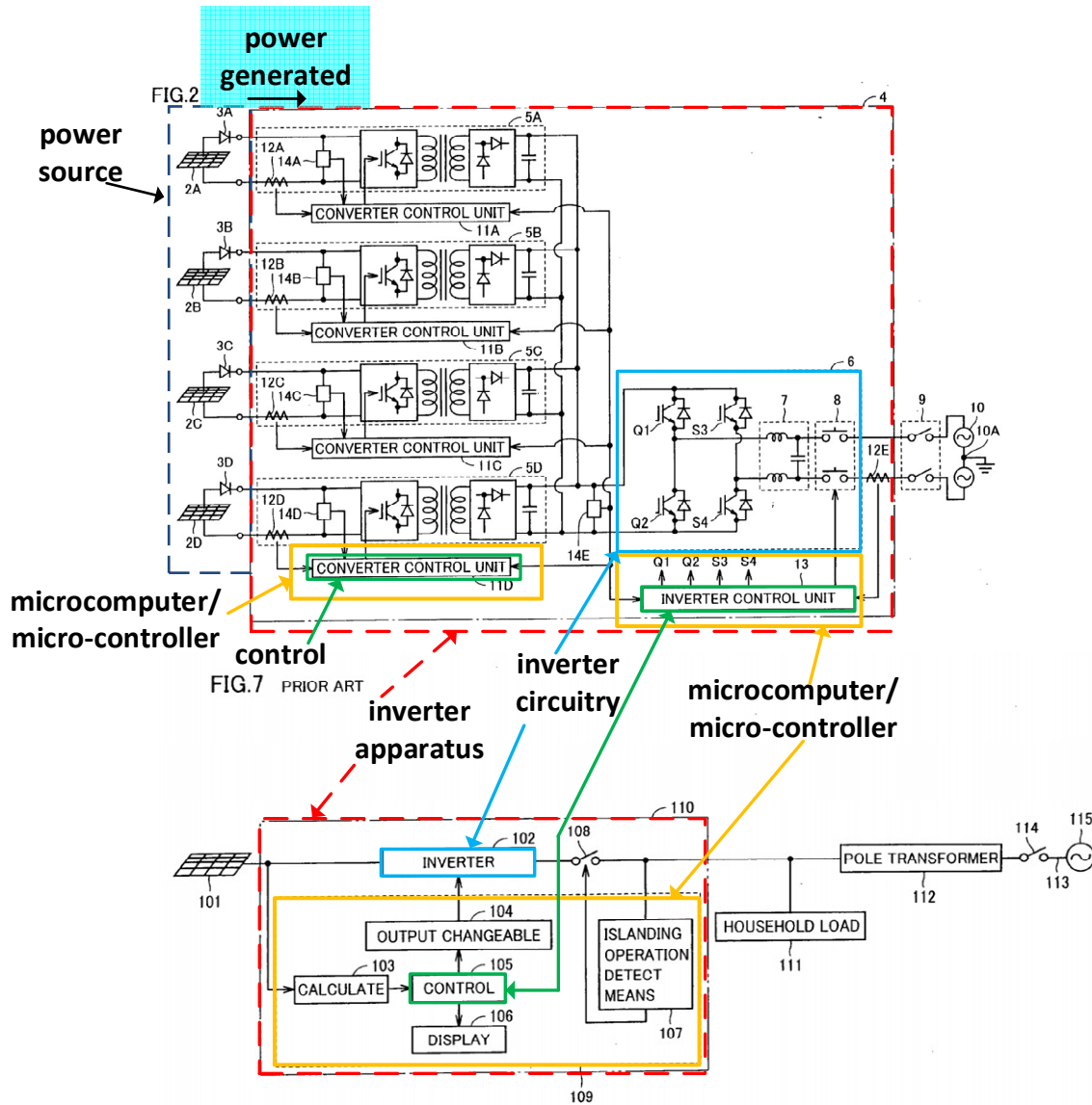
FIG. 1D
PRIOR ART

In Fig.1D, an isolated DC-DC converter (converter 1) feeds a post regulator circuit (converter 2) to form first and second buck converter stages, respectively. The first converter is a transformer-coupled input power converter that steps down the input voltage to an intermediate voltage. Ex.1003,1:61-66,3:8-13. The second converter is a buck power converter. Ex.1003,1:62-63;Ex.1007,¶86.

C. U.S. Patent Publication No. 2005/105224 (Nishi)(Ex.1004)

Nishi is a United States published patent application that published on May 19, 2005.

Figs. 2 and 7 of Nishi each show a photovoltaic power generation system. Each figure shows an inverter apparatus 4 and 110 that includes inverter circuitry (6 in Fig.2, 102 in Fig.7) and a micro-computer 109 that includes control circuitry 105 in Fig.7, or control units 11D and 13 in Fig.2. Ex.1004,¶[8],[88].



The control unit 13 receives input voltages and output current from sensors 14E and 12E and controls a pulse width of a pulse width modulation (“PWM”) control signal to control the input voltage of the inverter circuitry 6 to a specified range. *Id.*,¶[88]. In doing so, each converter 5A-5D in Fig.2 is controlled by the inverter micro-computer (i.e., control unit 11A-11D) to output a constant voltage. The control units 11A-11D control an operating point of an input voltage of each

converter to maximize the output power from each corresponding solar cells 2A-2D. Ex.1004,¶[97];Ex.1007,¶[89].

D. U.S. Patent No. 6,798,177 (Liu)(Ex.1005)

Liu is a United States patent that published on September 28, 2004. Liu discloses a multi-stage converter circuit that employs a storage capacitor in-between, and in parallel with, the two converter stages. The multi-stage converter circuit includes an input stage 50, a storage or reservoir capacitor 58, and an output stage 60 that connects to a power amplifier (“PA”) 68. Ex.1005, Fig.5, 4:25-28;Ex.1007,¶[90].

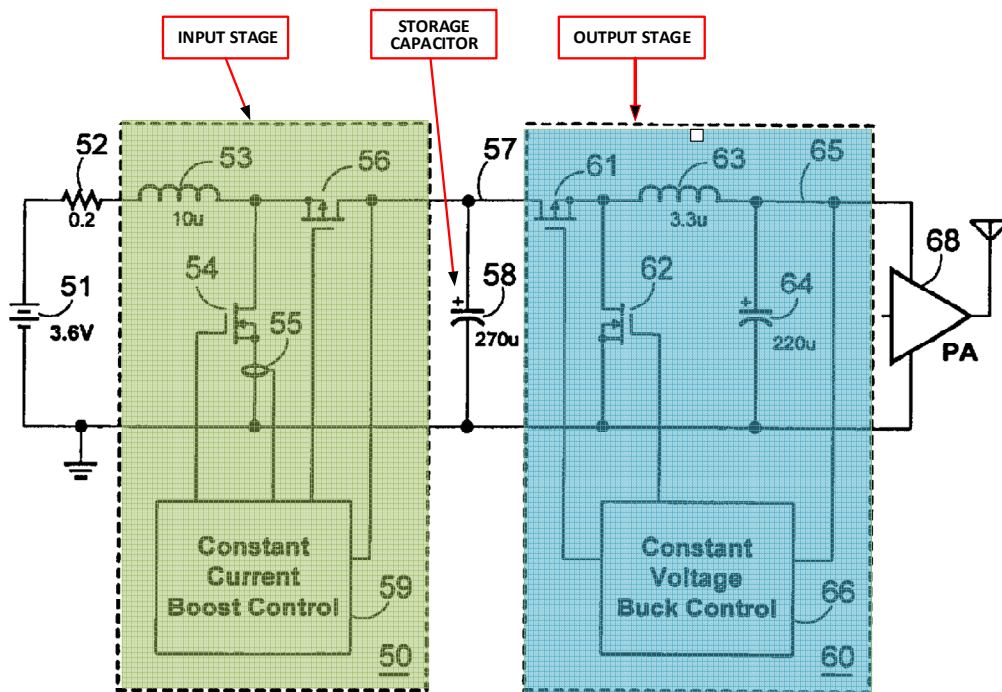


FIG. 5

The input stage 50 charges the storage capacitor 58 and increases the voltage across the capacitor. The output stage 60 down-converts the voltage on reservoir capacitor 58 to an output voltage, for example, 3.4V, needed by the PA 68, which the output stage 60 regulates. The storage/reservoir capacitor 58 supplies energy to PA 68, such that if input stage 50 ceases operating, the output stage continues powering PA 68 for some further time period. *Id.*,4:36-50;Ex.1007,¶¶91.

V. SUMMARY OF ARGUMENT

The '021 patent claims a method and circuit for an auxiliary power supply. The prior art herein is replete with this auxiliary power supply circuitry. Mieth teaches most elements of the '021 patent's independent claims. For independent claim elements arguably not taught by Mieth, Balogh teaches first stage features and cascaded first and second stages such as step-down power converters. Nishi teaches a micro-controller as a load, and Liu discloses a capacitor as a power absorption circuit between cascaded power converters. Adding these features to Mieth's auxiliary power supply system would have been obvious, and yields the alleged invention claimed in the '021 patent.

In sum, as demonstrated by a preponderance of the evidence herein, including the Declaration of Dr. Doug Holberg (Ex.1007), the '021 patent claims are unpatentable as being anticipated and/or obvious in view of the cited prior art.

VI. IDENTIFICATION OF CHALLENGE PURSUANT TO 37 C.F.R.

§ 42.104(B) AND STATEMENT OF THE RELIEF REQUESTED

A. Claims for Which Review is Requested and Grounds on Which Challenge is Based

Petitioner requests review on the following grounds under 35 U.S.C. §§ 102 and 103.

Ground	Prior Art	Claims Challenged
A	Mieth	1-7, 9
B	Mieth in view Balogh	1, 8, 10-12, 15-18, 20
C	Mieth in view of Balogh and Nishi	13-14
D	Mieth in view of Balogh and Liu	19

B. How Claims Are to Be Construed and Level of Skill

1. How Claims Are to Be Construed

A claim subject to *inter partes* review shall be given its ordinary and customary meaning to a PHOSITA, consistent with the prosecution history, as it would be given in a civil action under 35 U.S.C. § 282(b). 37 C.F.R. § 42.100(b).

All claim terms should be construed according to their ordinary and customary

meaning at the time of invention to a PHOSITA.

Regarding the claim feature: “a first stage and a second stage”

The proper construction of “a first stage and a second stage” is a first group of one or more circuit elements and a second group of one or more circuit elements. Neither the “first stage” nor “second stage” are defined in the disclosure of the ‘021 patent. Ex.1001;Ex.1007,¶99. The ‘021 patent does, however, refer to portions of circuits with the term stage. For example, the ‘021 patent refers to a first stage having an input connected to a photovoltaic panel and output that provides a voltage from the photovoltaic panel, and a second stage that supplies power. Ex.1001,1:49-55. The ‘021 patent also uses the word “stage” to refer to a “drive stage output 331” of a MOSFET 345. Ex.1001,6:11-15. Therefore the ‘021 patent assumes the reader understands what a “stage” is in relation to circuits, and uses the phrase to relate to portions of an electrical circuit with a particular functionality, for example, functionality as recited in a remaining portion of the claim.

A PHOSITA understands a “stage” to refer to a generic portion of an electrical circuit. Ex.1007,¶98. In fact, among circuit engineers it is a common term of art in the field of electronics, and the term is employed in the ‘021 patent consistent with its ordinary and common meaning. Ex.1007,¶99. For example, Nishi (Ex.1004), which predates the ‘021 patent, uses the phrase “stage” to refer to

a general circuit component, referencing a “front stage” of an inverter apparatus 10 when discussing a booster chopper 206 that receives DC power. Ex.1004,¶¶31-34; Ex.1007.¶98. As such, the “front stage” refers to the input portion of the circuit for the inverter apparatus. Ex.1007.¶98. Additionally, Liu, which predates the ‘021 patent, uses “stage” to refer to one or more circuit components, referring to “[a] power converter including a first stage,... and a second stage.” Ex.1005,Abstract.

No prosecution history exists that addresses the construction of the claim language at issue. Ex.1006.

Therefore, based on the ordinary and customary meaning of the terms, common usage in the art, and a consistent usage of the terms in the detailed description of the ‘021 patent, the term “stage” means “one or more circuit components” that operate alone or together to provide a specified function set forth in the claim. Ex.1007, ¶¶99-100.

2. Level of Skill

A PHOSITA would have had a bachelor’s degree in electrical engineering, or a similar discipline and at least two years of design experience with circuit design. Ex.1007,¶30.

VII. SPECIFIC GROUNDS FOR UNPATENTABILITY

A. Ground A: Anticipation of claims 1-7, and 9 in view of Mieth

1. Independent Claim 1

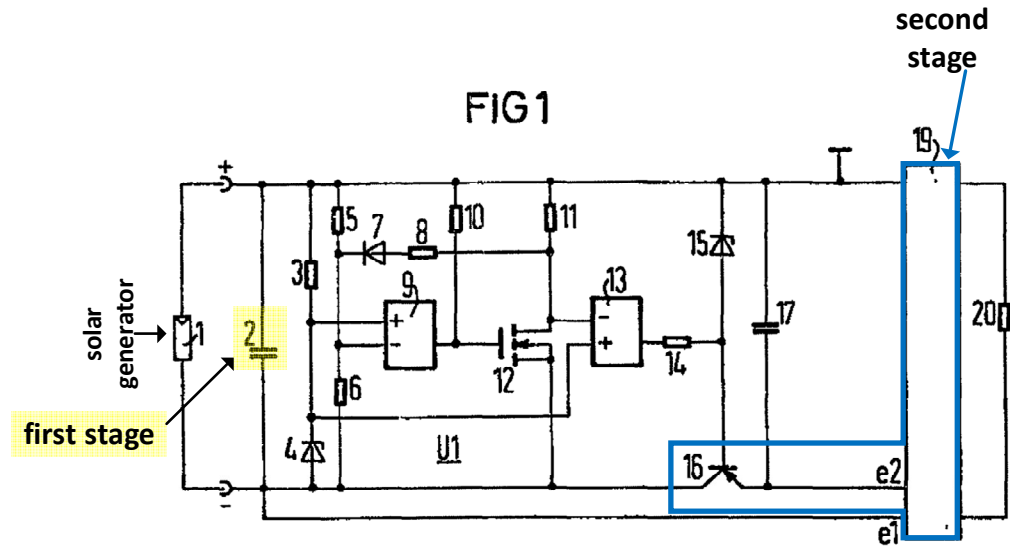
With reference to the claim listing appendix, Mieth discloses Elements [1A]-[1G]. As explained below, a PHOSITA would have been motivated by Mieth to arrive at the alleged invention of claim 1.

i. [1A]: “A method to supply power”

Mieth (Ex.1002) discloses a circuit that supplies power to an electrical load from a solar generator. Ex.1002 (Mieth),8:8-9. A PHOSITA would understand that when the circuit of Mieth supplies power to the electrical load, the circuit is performing a method to supply power to the electrical load. Ex.1007,¶96. Thus, Mieth teaches [1A].

ii. [1B]: “the method comprising: providing a power supply having a first stage and a second stage,”

Mieth discloses a circuit with a *power supply* as shown below in Fig.1(annotated-1B). Mieth discloses a capacitor 2 (yellow) in parallel with the solar generator 1, and a power supply apparatus 19 connected to a bipolar transistor 16 (blue). Ex.1002,9:5-9,11:14-16;Ex.1007,¶97. The capacitor 2 is analogous to the *first stage* and the power supply apparatus 19 connected to the bipolar transistor 16 is analogous to the *second stage* of the claimed power supply. Ex.1007,¶¶97-100.



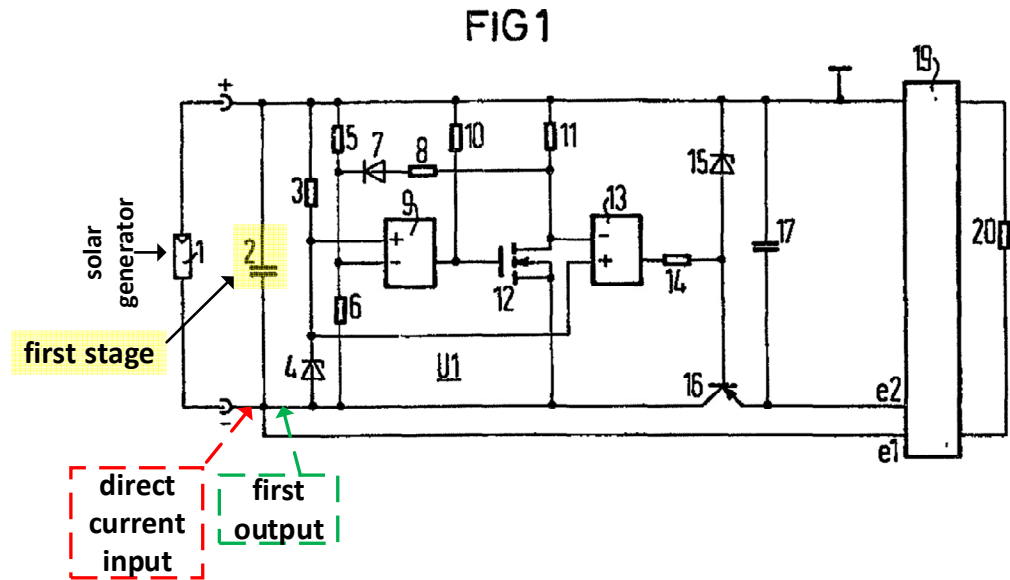
Ex.1002, Fig.1(annotated-1B)

Thus, Mieth teaches [1B].

Additionally, the combination of Mieth and Balogh disclose the features of [1B] as discussed in further detail in §VII.B.1.

iii. [1C]: “wherein the first stage converts power from a direct current input into a first output,”

A PHOSITA would understand that solar generators generate a direct current. Ex.1007,¶102. As such, the solar generator 1 of Mieth supplies the *direct current input* (dashed-red) to the capacitor 2 as shown in Fig. 1 (annotated-1C) below. The first stage of Mieth is a parallel capacitor 2 which a PHOSITA would understand converts power associated with the direct current input into a *first output* (dashed-green). Ex.1007,¶103.



Ex.1002, Fig.1 (annotated-1C)

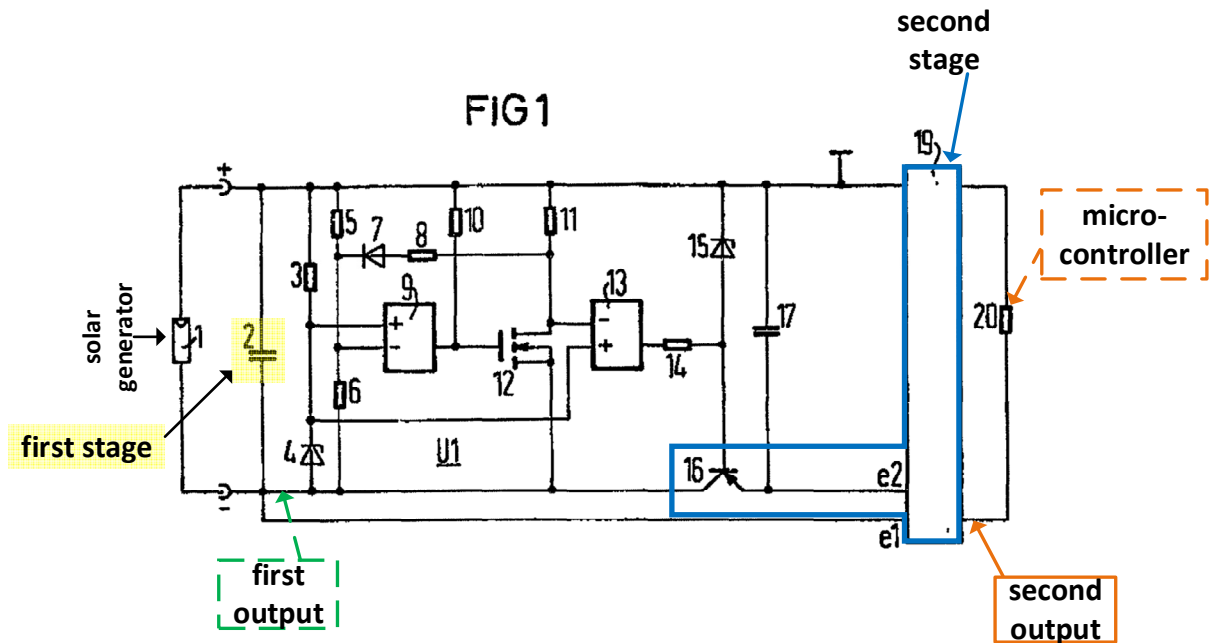
Thus, Mieth teaches [1C]. Additionally, the combination of Mieth and Balogh disclose the features of [1C] as discussed in further detail in §VII.B.1.

iv. [1D]: “and the second stage powered by the first output has a second output for a micro-controller;”

In Mieth, a power supply apparatus 19 connected to a bipolar transistor 16 (second stage-blue) is powered by the first output (dashed-green). Specifically, the power supply apparatus 19 *is powered* by way of auxiliary voltage input e2 which is associated with the first output when bipolar transistor 16 is conducting.

Ex.1002,8:29-35;Ex.1007,¶104. The power supply apparatus 19 is a DC-DC voltage converter or a charging converter and outputs a voltage and current to power a load 20. *Id.* The output of power supply apparatus 19 is analogous to the claimed *second output* (orange) as shown in Fig.1(annotated-1D.1) below.

Ex.1007,¶104. A PHOSITA would understand that a load in a circuit can be or include a micro-controller, as such the load 20 is analogous to the claimed *micro-controller* (dashed-orange). Ex.1007,¶105;Ex.1014,1180,Fig.5.

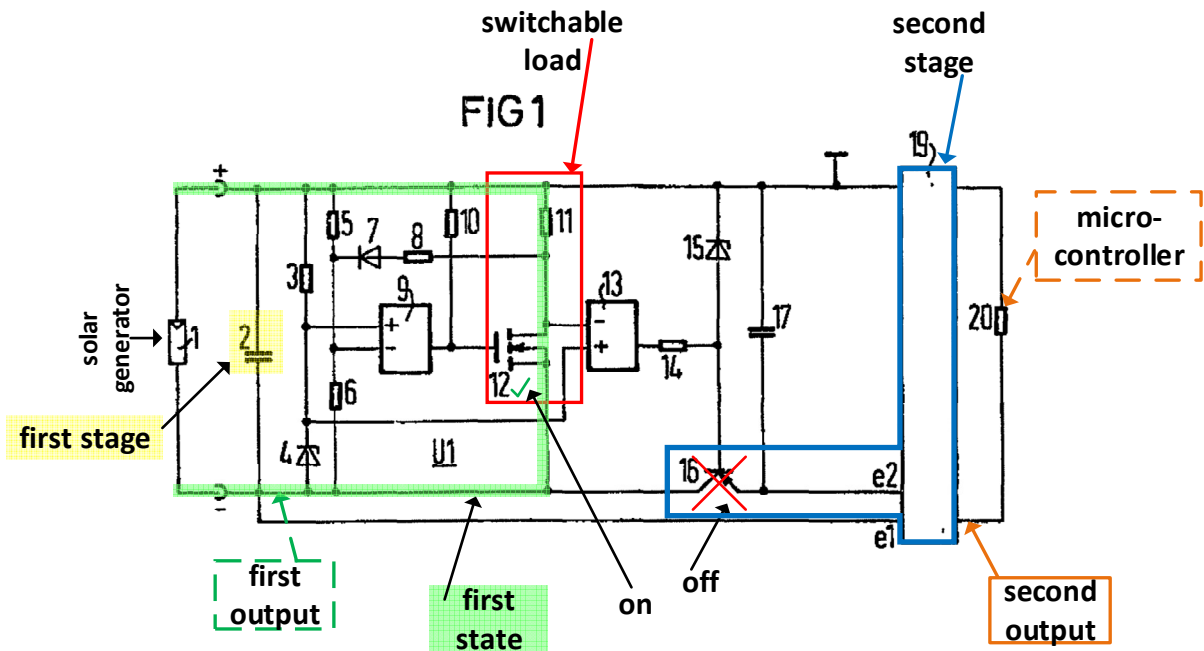


Ex.1002, Fig.1(annotated-1D.1)

Thus, Mieth teaches [1D]. Additionally, the combination of Mieth and Balogh teach the features of [1D] as discussed in further detail in §VII.B.1.

- v. [1E]: “connecting the first output of the first stage to a switchable load to consume at least a portion of the first output while disabling the second stage in supplying the second output to the micro-controller;”

Mieth discloses that the first output (dashed-green) of capacitor 2 is connected to a field-effect transistor 12 that is connected to a preliminary load 11 as shown in Fig.1(annotated-1E). Ex.1002,10:5-14;Ex.1007,¶106.



Ex.1002, Fig.1(annotated-1E)

The field-effect transistor 12, which operates as a switch, and the preliminary load 11 in combination are analogous to the claimed *switchable load* (red).

Ex.1007,¶107. Mieth discloses that when voltages at the first output are below a predefined minimum value for reliable operation of the power supply apparatus 19, the field-effect transistor 12 is “on”, and operates as a closed switch where the preliminary load 11 is connected to the solar generator 1 by the first output.

Ex.1002,9:15-23;Ex.1007,¶107. As such, because the preliminary load 11 is connected to the first output, during this state, the preliminary load 11 *consumes at least a portion of the first output* as recited in claim 1. Ex.1007,¶107.

As shown in Fig.1(annotated-1E), a first state (highlighted-green) illustrates that the switchable load is powered by the first output from the capacitor 2 (i.e.,

field-effect transistor 12 is “on” or in a conducting state). Ex.1007,¶108.

Additionally, in the first state, bipolar transistor 16 is “off” or in a non-conducting state, preventing the power supply apparatus 19 from being powered by the first output. Ex.1007,¶108. When the preliminary load 11 is connected to the first output, the power supply apparatus 19 (second stage, blue) is not powered by the first stage (*i.e.*, the first output) because the bipolar transistor 16 is “off”.

Ex.1002,9:9-13,9:23-32;Ex.1007,¶108. That is, the auxiliary voltage input e2 is associated with the first output only when the bipolar transistor 16 is conducting.

Id. As such, in the first state the power supply apparatus 19 is ***disabled in supplying the second output to the micro-controller*** as recited in claim 1.

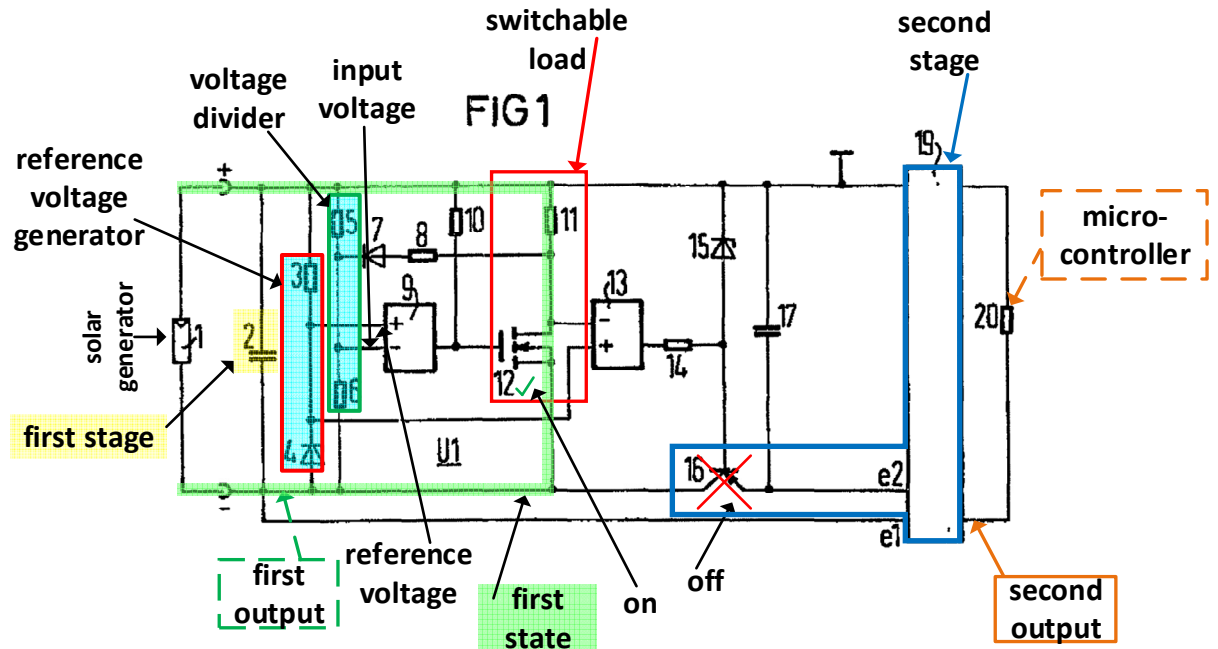
Ex.1007,¶108. The condition where the preliminary load 11 is connected to the first output and the power supply apparatus 19 is not powered is discussed further herein as a “first state.”

Thus, Mieth teaches [1E].

- vi. **[1F]: “determining whether the first output from the first stage powering the switchable load is above a threshold during a time period in which the second output to the micro-controller is disabled; and”**

As discussed in §VII.A.1.v., when the circuit of Mieth is configured for the first state, bipolar transistor 16 is non-conducting, and the power supply apparatus 19 (*i.e.*, second stage-blue) is disabled from supplying the load 20 (*i.e.*, micro-

controller-dashed-orange) with the second output (orange), see Fig.1(annotated-1F).



Ex.1002, Fig.1(annotated-1F)

While in the first state, transistor 12 is turned “on” by a comparator 9 (hereinafter the first comparator 9) thereby loading the first output with the preliminary load 11 (controlled through the field-effect transistor 12 when conducting, *i.e.*, the first state – analogous to the switchable load-red). Ex.1002, 9:15-32,10:5-14;Ex.1007,¶111. In the first state, the first comparator 9 compares a reference voltage from a reference voltage generator (highlighted-teal-outlined-red) connected to a positive terminal of the first comparator 9 to a representative voltage from a voltage divider (highlighted-teal-outlined-green) connected to a negative terminal of the first comparator 9. Ex.1002,9:34-10:3;Ex.1007,¶111. The

reference voltage generator is defined by the Zener diode 4 and the resistor 3. *Id.* The voltage divider is defined by resistors 5 and 6 and the representative voltage is representative of the first output. *Id.* The first comparator 9 compares the representative voltage provided by the voltage divider 5, 6 to the reference voltage to determine if the monitored voltage exceeds a threshold related to the reference voltage. Ex.1002,12:12-26,Ex.1007,¶111.

In the first state, the representative voltage is less than the reference voltage, and the circuit of Mieth powers the preliminary load 11 and field-effect transistor 12 by the first output of capacitor 2 (*i.e.*, first stage) which is the same as the claimed *first output from the first stage powering the switchable load*.

Ex.1002,12:12-19;Ex.1007,¶112. The first state of Mieth concurrently disables the second output of the power supply apparatus 19 to the load 20 by turning the bipolar transistor 16 “off,” which is the same as the claimed *the second output to the micro-controller is disabled*. *Id.* The time period the circuit of Mieth is in the first state is the same as the claimed *time period* and the predefined minimum value of Mieth is the same as the claimed *threshold*. Ex.1002,9:15-

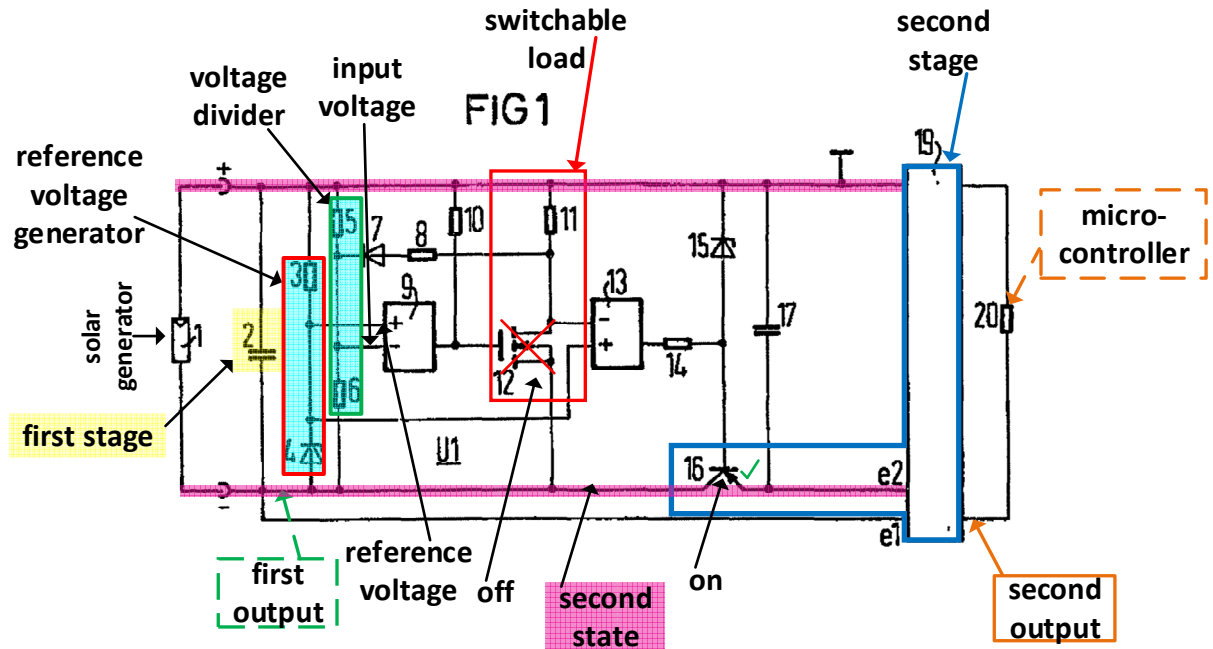
26;Ex.1007,¶112. The circuit of Mieth is in the first state for the time period when the circuit determines whether the predefined minimum value is satisfied, which is equivalent to the claimed *determining whether the first output . . . is above a threshold during a time period*. Ex.1007,¶112.

Thus, Mieth teaches [1F].

- vii. [1G]: “in response to a determination that the first output from the first stage powering the switchable load is above the threshold during the time period in which the second output to the micro-controller is disabled, disconnecting the switchable load from the first output of the first stage; and instructing the second stage to enable the second output to the micro-controller using power from the first output of the first stage.”

As discussed in accordance with [1F] in §VII.A.1.vi., in the first state, the preliminary load 11 and the field-effect transistor 12 (i.e., switchable load-red) are powered by the first output of capacitor 2 (i.e., first stage-highlighted-yellow).

Mieth further discloses that when voltages from the solar generator 1 (as represented at the negative terminal of first comparator 9) are above a predefined minimum value (as represented at the positive terminal of first comparator 9), the auxiliary voltage input e2 of the power supply apparatus 19 is connected to the first output of the solar generator 1. Ex.1002,9:23-26. As shown in Fig.1(annotated-1G) below, when the predefined minimum value is satisfied, the circuit of Mieth operates in a second state (highlighted-pink) where the bipolar transistor 16 is “on” or conducting, causing the first output (dashed-green) of capacitor 2 to be connected to e2 thereby powering the power supply apparatus 19. Ex.1002,10:16-29;Ex.1007,¶114.



Ex.1002, Fig.1(annotated-1G)

Furthermore, in the second state, the field-effect transistor 12 is “off” or non-conducting, thereby disconnecting the preliminary load 11 from the first output. *Id.* As discussed in §VII.A.1.vi., the first comparator 9 compares a reference voltage from a reference voltage generator (highlighted-teal-outlined-red) to a representative voltage from a voltage divider (highlighted-teal-outlined-green) to determine if the representative voltage exceeds a value defined by the reference voltage. Ex.1002,12:12-26,Ex.1007,¶115. While in the first state, when the first output of capacitor 2 rises and the representative voltage across voltage divider 5, 6 is above the value (i.e., “predefined minimum value” as quoted by Mieth), the circuit disconnects the preliminary load 11 from the first output by configuring the field-effect transistor 12 to an “off” state, which is the same as the

claimed *disconnecting the switchable load from the first output of the first stage*.
Id.

The bipolar transistor 16 that connects the power supply apparatus 19 to the first output which results in the second output of the power supply apparatus 19 powering the load 20 is the same as the claimed *instructing the second stage to enable the second output to the micro-controller using power from the first output of the first stage*. Ex.1007,¶116.

When the circuit of Mieth is in the first state, the circuit makes a determination that the predefined minimum value is satisfied while the second stage is disabled, and in response changes to the second state, which is analogous to the claimed *in response to a determination . . . the micro-controller is disabled*. Ex.1002,9:15-23;Ex.1007,¶117.

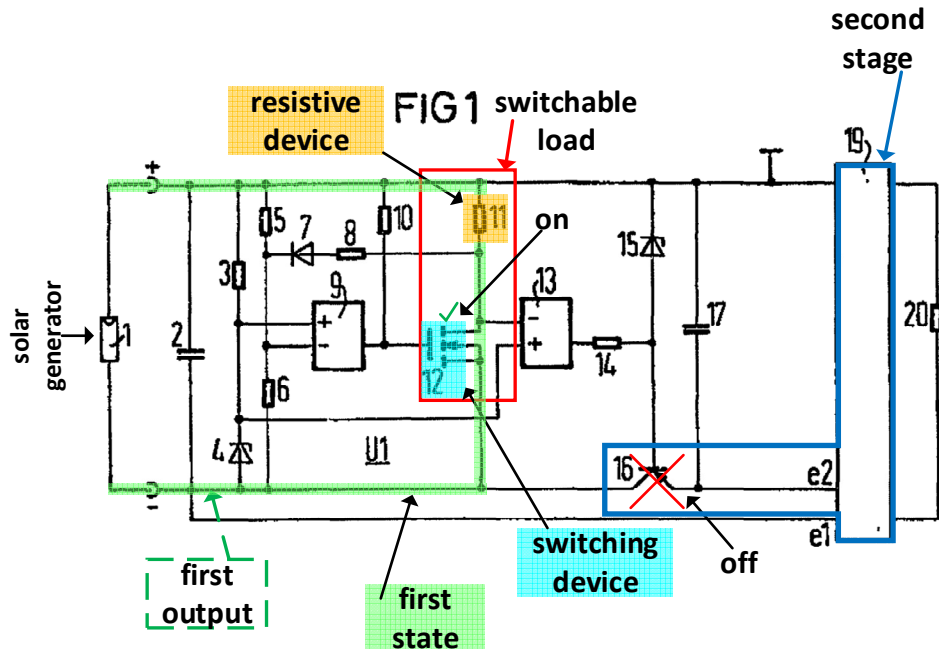
As such, Mieth teaches [1G], and every feature of claim 1.

2. Dependent Claim 2

Claim 1 is disclosed by Mieth. *Supra*, §VII.A.1. Claim 2 depends from claim 1 and requires [2A], “the switchable load comprises: a resistive device.” Ex.1001, claim 2. As shown below in Fig.1(annotated-Claim-2) of Mieth, preliminary load 11 (highlighted-orange) can be a resistor. Ex.1002,12:14-20 (“preliminary load formed by the resistor 11”);Ex.1007,¶119. Since the preliminary load 11 can be a resistor, and a resistor is a resistive device,

preliminary load 11 of Mieth is analogous to the *resistive device* of claim 2.

Ex.1007,¶119.



Ex.1002, Fig.1(annotated-Claim-2)

Claim 2 further requires [2B], “a switching device connected to the resistive device.” Ex.1001, claim 2. As shown in Fig.1(annotated-Claim-2), the field-effect transistor 12 (highlighted-teal) is connected to the preliminary load 11.

Supra,§VII.A.1.v. Mieth describes the field-effect transistor 12 as a first electronic switch, and thus a PHOSITA would understand that the field-effect transistor 12 is a switching device. Ex.1002,10:5-14;Ex.1007,¶120. As such, the field-effect transistor 12 is analogous to the *switching device* of claim 2 and the field-effect transistor 12 connected to the preliminary load 11 is analogous to feature [2B].

Ex.1007,¶120.

Claim 2 further requires [2C], “wherein the switching device is configured to be turned on to be connected to the first output to consume the portion of the first output and turned off to be disconnected from the first stage.” Ex.1001, claim 2. As shown in Fig.1(annotated-Claim-2) of Mieth, the field-effect transistor 12 is “on” or in a conducting state to connect the switchable load to the first output (dashed-green) when the circuit is in the first state (highlighted-green).

Supra,§VII.A.1.v. When the field-effect transistor 12 is in the “on” state, the preliminary load 11 is connected to the solar generator 1 by the first output, and thus consumes the portion of the first output. *Supra*,§VII.A.1.v.;Ex.1002,9:15-23;Ex.1007,¶121. Furthermore, as shown in Fig.1(annotated-1G) of Mieth, in the second state, the field-effect transistor 12 is “off” or in a non-conducting state to disconnect the switchable load 11 from the first output.

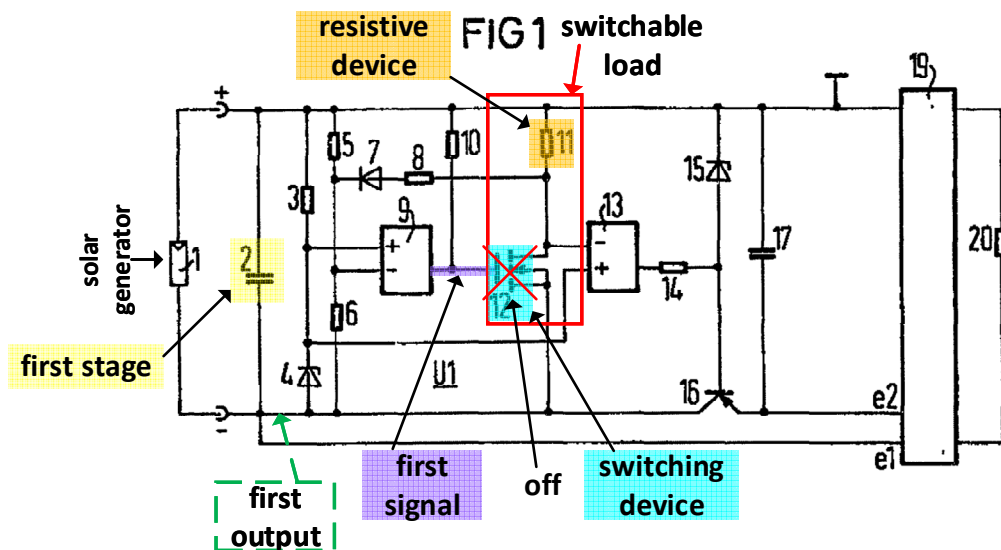
Supra,§VII.A.1.vii.;Ex.1002,12:21-26;Ex.1007,¶121. Thus, the field-effect transistor 12 connects or disconnects the preliminary load 11 from the first output according to the first state or the second state, respectively, *which is the same as [2C]*. Thus, Mieth discloses every feature of claim 2.

3. Dependent Claim 3

Claim 2 is taught by Mieth. *Supra*,§VII.A.2. Claim 3 depends from claim 2 and requires, “wherein the disconnecting of the switchable load from the first

output of the first stage comprises sending a first signal to the switching device to turn off the switching device.” Ex.1001, claim 3.

As shown in Fig.1(annotated-Claim-3) of Mieth, the first comparator 9 is connected to the first output by a Zener diode 4, and resistor 3. Ex.1002,12:12-19;Ex.1007,¶123.



Ex.1002, Fig.1(annotated-Claim-3)

The first comparator 9 outputs a first signal (highlighted-purple) to the field-effect transistor 12 (switching device, highlighted-teal) based on a comparison of the representative voltage at the negative comparator terminal and a reference voltage at the positive comparator terminal. Ex.1007,¶124. The first signal from first comparator 9 is a voltage connected to the gate of the field-effect transistor 12. Ex.1007,¶124. When the first signal from the first comparator 9 is low or zero (e.g., high voltages at the first output and thus the second state), the field-effect

transistor 12 is in a non-conducting or “off”. Ex.1007,¶124. When the first signal from the first comparator 9 is high (e.g., low voltages at the first output and thus the first state), the field-effect transistor 12 conducts or is in an “on” state.

Ex.1007,¶124. Since the output of the first comparator 9 turns the field-effect transistor 12 “on” and “off”, a PHOSITA would understand that the output is analogous to the claimed *first signal* as the output from the first comparator 9 operates the field-effect transistor 12 just as the claimed first signal operates the claimed switching device. Ex.1007,¶124.

When the voltage input to the negative terminal of the first comparator 9, which represents the voltage at the first output, rises above a predefined value, the field-effect transistor 12 is turned “off” by the first comparator 9 outputting the first signal with a low voltage, and the preliminary load 11 (resistive device-
highlighted-orange) is electrically disconnected from the first output.

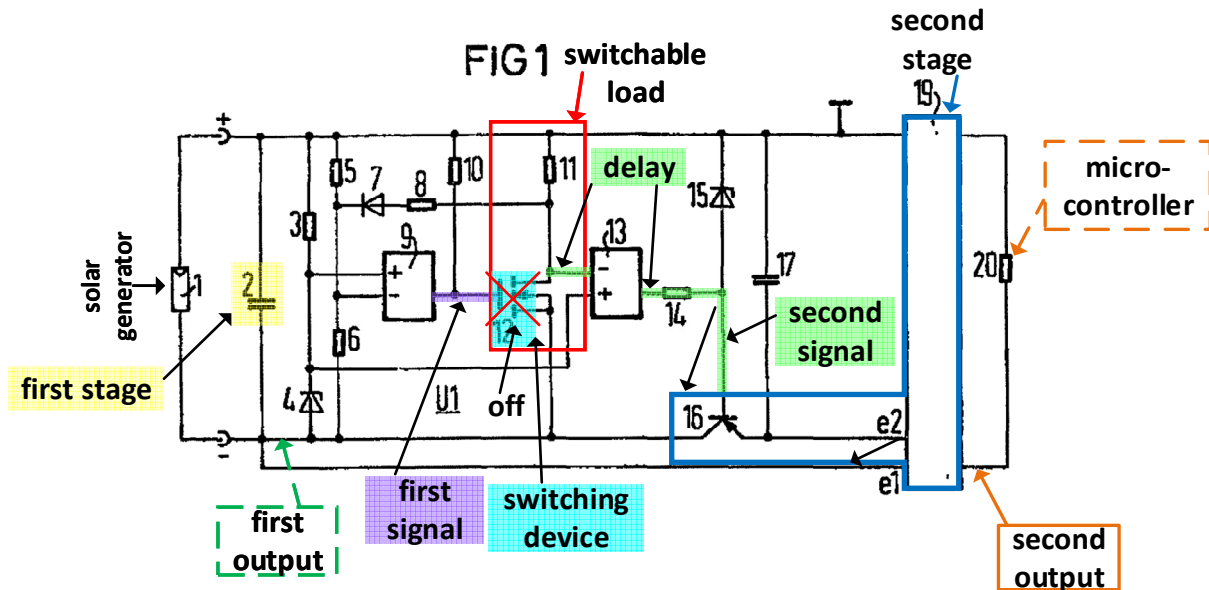
Ex.1002,12:12-30;Ex.1007,¶125. As such, the preliminary load 11 is disconnected from the first output of capacitor 2 (first stage-**highlighted-yellow**) by a first signal from the first comparator 9 that signals the field-effect transistor 12 to turn “off”, which is analogous to *disconnecting of the switchable load from the first output of the first stage comprises sending a first signal to the switching device to turn off the switching device* as recited in claim 3. Ex.1007,¶125.

Thus, Mieth discloses every feature of claim 3.

4. Dependent Claim 4

Claim 3 is disclosed by Mieth. *Supra*, §VII.A.3. Claim 4 depends from claim 3 and requires [4A], “further comprising: generating the first signal based on the determining of whether the first output from the first stage powering the switchable load is above the threshold; and.” Ex.1001, claim 4.

The first output of capacitor 2 is represented at the positive terminal of first comparator 9 as an input “sensed” or representative voltage defined by the first output and the voltage divider 5, 6. Ex.1007, ¶128. The output of the first comparator 9 (e.g., the claimed first signal, highlighted-purple) controls the field-effect transistor 12 (switching device, highlighted-teal) based on whether the representative voltage to the first comparator 9 (negative terminal) satisfies the predefined limit voltage (e.g., analogous to the claimed threshold). Ex.1002, 12:21-30; Ex.1007, ¶128; Ex.1002, Fig.1 (annotated-Claim-4).



Ex.1002, Fig.1(annotated-Claim-4)

Specifically, the output of the first comparator 9 turns the transistor 12 “off” when the predefined voltage is satisfied (*i.e.*, when the output voltage at the first output reaches the desired level, the corresponding representative voltage at the comparator input dictated by the voltage divider circuit of resistors 5 and 6 exceeds the predefined minimum value). Ex.1002,10:16-29,12:21-30;Ex.1007,¶129. The circuit of Mieth generating the first signal (*i.e.*, the output of the first comparator 9 that feeds the gate of the transistor 12) based on the first output of the capacitor 2 exceeding the predefined threshold voltage **is analogous to [4A]**.

Claim 4 further requires feature [4B], “delaying the first signal to generate a second signal to the second stage, the second signal enabling the second output to the micro-controller.” Ex.1001, claim 4.

Mieth discloses delaying the first signal from the first comparator 9 to generate a second signal from the output of the field-effect transistor 12 to enable the load 20. Ex.1007,¶131. Mieth discloses that the field-effect transistor 12 and a comparator 13 (hereinafter the second comparator 13) delays the first signal from the first comparator 9 to generate a second signal (highlighted-green) that turns on the bipolar transistor 16. When bipolar transistor 16 turns on, the first output is connected to the e2 input to energize the power supply apparatus 19 (second stage-blue) which enables the second output (orange) of the power supply apparatus 19 to power the load 20 (micro-controller-dashed-orange), which is analogous to the features of [4B] as discussed below. Ex.1002, Fig.1, 11:4-12, 12:12-19; Ex.1007, ¶131.

The bipolar transistor 16 operates as a switch that can connect the first output to the power supply apparatus 19. Ex.1002, 10:31-36, Ex.1007, ¶132. The base of the bipolar transistor 16, which controls the conducting or non-conducting state of the bipolar transistor 16, is controlled by the second comparator 13. Ex.1002, 10:36-11:12; Ex.1007, ¶132. The second comparator 13 outputs the second signal based on an input from the field-effect transistor 12, where the input from the field-effect transistor 12 is itself based on the first signal. *Id.* As such, the state of the second signal is dictated by the state of the first signal, and the transition of the second signal to activate bipolar transistor 16 is delayed with respect to the

transition of the first signal by the transistor 12 and the second comparator 13 which is analogous to the claimed *delaying the first signal*. Ex.1007,¶132. The second comparator 13 generates the second signal based on the first signal which is analogous to the claimed *to generate a second signal*, and the second signal controls the bipolar transistor 16 which is analogous to the claimed *to the second stage*. Ex.1007,¶132. Furthermore, if the *delaying the first signal* should be defined by a specific delay circuitry rather than the intrinsic switching characteristics of comparator 13 and switch 12, a PHOSITA would have known to add a capacitor (optionally with a series resistor) parallel to resistor 11 according to customary practices in the art at the time of filing. Further, or in alternative, one or more buffer circuits or delay elements could be interposed between the second comparator output and the base of bipolar transistor 16 to define a larger delay period. Ex.1007,¶132;Ex.1015,3:53-63,Fig.3.

The second signal turns the bipolar transistor 16 on when the output of the first stage, as represented at the negative terminal of second comparator 13, is above a limit voltage of the second comparator 13, and powers the power supply apparatus 19. Ex.1002,12:21-30;Ex.1007,¶133. When the power supply apparatus 19 is powered, the second output is enabled to the load 20. Ex.1002,8:29-35;Ex.1007,¶133. The bipolar transistor 16 of Mieth turned on by the second

signal, which enables the second output to the load 20, is analogous to the claimed *second signal enabling the second output to the micro-controller*.

Thus, Mieth teaches all the features of claim 4.

5. Dependent Claim 5

Claim 4 is disclosed by Mieth. *Supra*, §VII.A.4. Claim 5 depends from claim 4 and requires [5A], “further comprising: providing a control circuit comprising: a hysteresis amplifier configured to receive the first output of the first stage and generate the first signal.”

As shown in Fig.1(annotated-[5A]) below, Mieth discloses a capacitor 2 (highlighted-yellow) analogous to the claimed first stage and outputs a first output (dashed-green) analogous to the claimed first output, a first comparator 9 (dashed-blue) that is analogous to the claimed hysteresis amplifier and outputs a first signal (highlighted-purple) analogous to the claimed first signal that teach [5A] as discussed further below.

comprising resistors, 8, 11 and diode 7 are in parallel with resistor 5 forming a voltage divider with resistor 6. When the switch 12 is on, diode 7 is off and no current flows through resistor 8 leaving only resistors 5 and 6 to form the voltage divider. In this way the comparator 8 and associated circuitry exhibit hysteretic behavior. Ex.1007,¶¶137,55-62,77-82;Ex.1009,462. Since the first comparator 9 can be an amplifier with a positive feedback loop, the first comparator 9 is the same as the claimed *hysteresis amplifier*. Ex.1007,¶137. The first output of the capacitor 2 is represented at the negative input of the first comparator 9 through a voltage divider defined by resistors 5 and 6 in addition to resistors 8 and 11 and diode 7 when comparator 9 output is low, which is analogous to the claimed *hysteresis amplifier configured to receive the first output of the first stage*. Ex.1002,9:34-38;Ex.1007,¶137. The output of the first comparator 9 is a first signal as discussed previously in §VII.A.3., and is analogous to the claimed recitation *generate the first signal*. Ex.1007,¶137. A PHOSITA would understand that the circuitry of Mieth, that includes the first comparator 9, is analogous to the claimed *control circuitry* as the first comparator 9 generates the first signal that controls the field-effect transistor 12. Thus, Mieth teaches [5A].

Claim 5 further requires [5B], “a delay circuit to generate the second signal according to the first signal.” Fig.1(annotated-[5A]) further illustrates the field-effect transistors 12 (switching device, highlighted-teal) and the second comparator

13 that delays the first signal (highlighted-purple) from first comparator 9 to generate a second signal (highlighted-green). Ex.1002, Fig.1, 11:4-12; Ex.1007, ¶138. Since, the field-effect transistor 12 and the second comparator 13 delays the first signal to generate the second signal, the field-effect transistor 12 and the second comparator 13 are analogous to the claimed *delay circuit to generate the second signal according to the first signal*. However, if the *delay circuit* should be defined by a specific circuitry rather than the intrinsic switching characteristics of comparator 13 and switch 12, delay elements discussed in accordance with claim 4 in §VII.A.4 can be implemented.

Thus, Mieth teaches [5B].

6. Dependent Claim 6

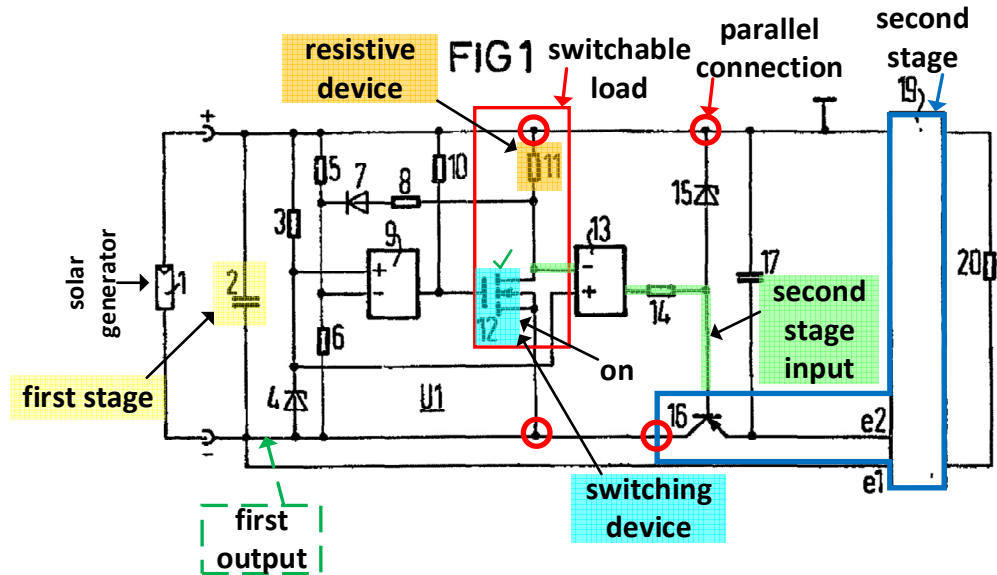
Claim 3 is taught by Mieth. *Supra*, §VII.A.3. Claim 6 depends from claim 3 and requires, “wherein the switching device includes one of: a field effect transistor (FET), a metal-oxide-semiconductor field-effect-transistor (MOSFET), and a bipolar junction transistor.” Ex.1001, claim 6.

As discussed in §VII.A.2, the field-effect transistor 12 (highlighted-teal) is analogous to the *switching device*. See Ex.1002, Fig.1(annotated-Claim-2). The field-effect transistor 12 is the same as the claimed *field effect transistor (FET)*. Ex.1007, ¶141. As such, Mieth teaches all the features of claim 6.

7. Dependent Claim 7

Claim 6 is taught by Mieth. *Supra*, §VII.A.6. Claim 7 depends from claim 6 and requires, “wherein when the switch device is turned on, the switchable load and an input of the second stage are connected in parallel to the first output of the first stage.” Ex.1001, claim 7.

As shown in Fig.1(annotated-Claim-7) below, Mieth discloses a first output (dashed-green) of the capacitor 2 (first stage-highlighted-yellow), field-effect transistor 12 (switch device-highlighted-teal) connected to a preliminary load 11 analogous to the claimed switchable load (red), an output signal from the field-effect transistor 12 (highlighted-green) analogous to the claimed second stage input, where the output signal controls the transistor 16 and power supply apparatus 19 (second stage-blue), and parallel connection nodes (circles-red) as discussed below. Ex.1002,9:15-18,10:5-14,11:14-16;Ex.1007,¶144.



Ex.1002, Fig.1(annotated-Claim7)

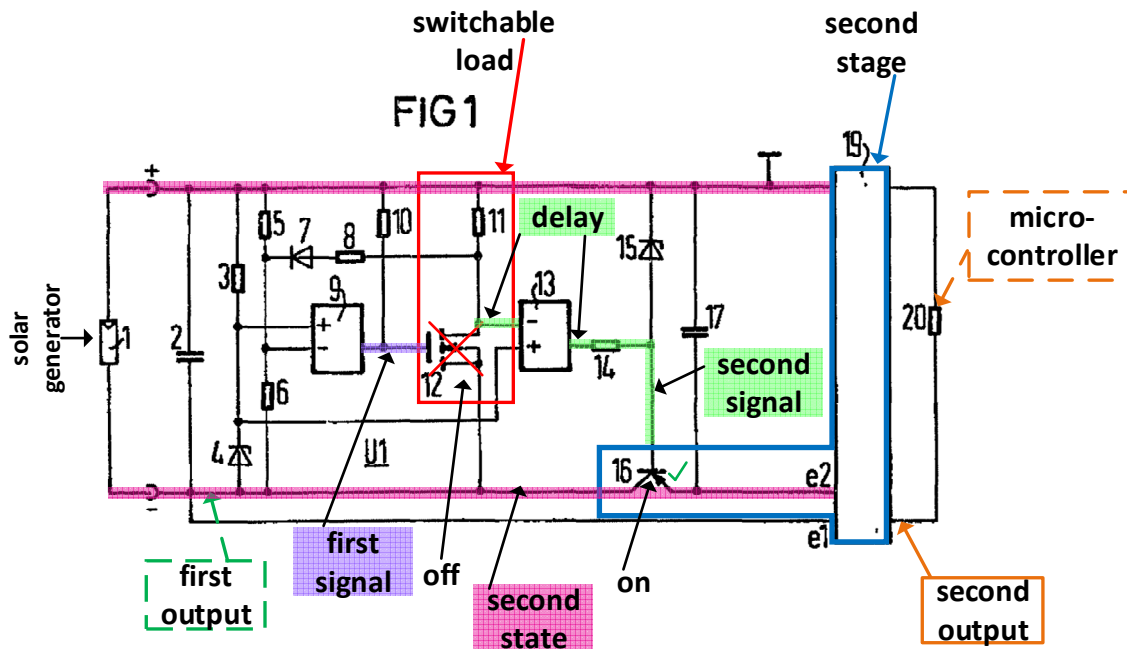
When the field-effect transistor 12 is “on”, the load 11 is connected to the first output as described previously in conjunction with the first state of §VII.A.1.v., and is analogous to the claimed *when the switch device is turned on*. Furthermore, the field-effect transistor 12 outputs a signal to the second comparator 13, which then connects to the transistor 16 of the second stage and is analogous to the claimed *input of the second stage*. Ex.1002,11:4-12;Ex.1007,¶145. The parallel connection nodes show that the switchable load is connected in a parallel configuration with the first output of capacitor 2, and the second stage input to the transistor 16 (i.e., the collector terminal) is connected in parallel with the first output which is analogous to the claimed *the switchable load and an input of the second stage are connected in parallel to the first output of the first stage*. Ex.1007,¶145.

Thus, Mieth teaches all the features of claim 7.

8. Dependent Claim 9

Claim 1 is taught by Mieth. *Supra*, §VII.A.1. Claim 9 depends from claim 1 and requires, “wherein the disconnecting is performed prior to the instructing of the second stage to enable the second output to the micro-controller.” Ex.1001, claim 9.

As discussed in §VII.A.1.v.-§VII.A.1.vii., Mieth discloses a power supply apparatus 19 connected to a bipolar transistor 16 (second stage-blue), a second output from the power supply apparatus 19 is connected to the load 20 (micro-controller-dashed-orange), and a field-effect transistor 12 that disconnects the switchable load (red) from the first output when configured in a second state (highlighted-pink), see Fig.1(annotated-Claim-9) below.



Ex.1002, Fig.1(annotated-Claim-9)

The field-effect transistor 12 is controlled by a first signal from first comparator 9 which has a representative voltage associated with the first output connected to the negative terminal of first comparator 9. Ex.1002,9:15-18;Ex.1007,¶149. The field-effect transistor 12 outputs a signal to the second comparator 13 and the output of the second comparator 13 is a second signal (highlighted-green) that controls the transistor 16 to turn the second stage on, thereby enabling the second output to the load 20. Ex.1002,10:36-11:12;Ex.1007,¶149. Since the second signal controls the “on” or “off” state of the bipolar transistor 16 which enables the second output of the power supply apparatus 19 to the load 20, the second signal is analogous to the claimed *instructing of the second stage to enable the second output to the micro-*

controller. Ex.1007,¶149. A PHOSITA would understand that the field-effect transistor 12 has a switching delay time, and that the second comparator 13 has a propagation delay time. Ex.1007,¶149. As such, the first signal that turns “off” the field-effect transistor 12, which is analogous to the claimed *disconnecting* of the switchable load, is delayed by the field-effect transistor 12 and second comparator 13 to generate the second signal that enables the power supply apparatus 19. Ex.1007,¶149. The second signal of Mieth is delayed (with respect to the first signal) to turn on bipolar transistor 16 after the field-effect transistor 12 is turned “off” (i.e., a “break before make” arrangement), that is, the field-effect transistor 12 is turned “off” prior to the bipolar transistor 16 being turned on, which is analogous to the claimed *disconnecting is performed prior to the instructing of the second stage*. Ex.1007,¶149. However, if the “*disconnecting is performed prior to . . .*” should be defined by a specific circuitry rather than the intrinsic switching characteristics of comparator 13 and switch 12, delay elements discussed in accordance with claim 4 in §VII.A.4 can be implemented.

Thus, Mieth teaches all the features of claim 9.

B. Ground B: Anticipation/obviousness of claims 1, 8, 10-12, 15-18, and 20 in view of Mieth and Balogh

1. Independent Claim 1 features [1B]-[1D]

Independent claim 1 features [1B]-[1D] are taught by Mieth as discussed in §VII.A.1.ii-§VII.A.1.iv. As discussed previously, Mieth teaches the first stage.

However, Balogh (Ex.1003) also discloses a first stage, and a PHOSITA would have been motivated to combine Mieth and Balogh for at least the following reasons.

Balogh discloses cascaded converter arrangements (*e.g.*, Balogh Figs. 1B and 1C), and states that such cascaded arrangements using first and second buck converters are employed in circuit applications that require large input/output conversion ratios. Ex.1003,1:21-27. It is well known to a PHOSITA that photovoltaic systems couple together multiple photovoltaic cells that form photovoltaic panels or modules to realize high input voltages, and such high input voltages need large conversion ratios to step down the input voltage.

Ex.1003,1:21-27,Ex.1007,¶152. Even a single photovoltaic module can see a voltage as high as 80V, which may necessitate a large conversion ratio.

Ex.1007,152;Ex.1010;Ex.1011. Balogh further teaches a cascaded converter arrangement using a first stage transformer-coupled input power converter that steps down an input voltage to an intermediate voltage, followed by a second stage buck output converter that further steps down the intermediate voltage to a final voltage. Ex.1003,1:62-66.

Mieth states that applications having photovoltaic energy sources or wind energy sources often provide varying levels of input voltage, and that such voltages can create difficulties when serving as an input to a power converter.

Ex.1002,5:22-38. Mieth further teaches the use of a switchable load in situations where an input voltage to a power converter varies, such as the voltage from a photovoltaic system that will vary depending upon the time of day, or weather conditions. Ex.1002,5:22-38.

A PHOSITA is motivated to combine the cascaded power converter architecture of Balogh with the switchable load feature of Mieth for DC applications with high input voltages. Ex.1007,¶¶153-156. Mieth is directed towards solar generators that generate up to 36 volts (V). Ex.1002,12:21-26. Balogh discloses higher DC voltages relative to Mieth, for example, 48V with large step-down ratios, for example, 48V to 1.5V. Ex.1003,10:45-52. In other examples, solar panel modules can have 80V output voltages requiring large step-down ratios. Ex.1010;Ex.1011; Ex.1007,¶¶156. As such, a PHOSITA would have known to combine the cascaded power converter architecture of Balogh for high DC applications (e.g., 48V or 80V solar panel modules) to realize an appropriate intermediate voltage for the switchable load and load 20 of Mieth. Ex.1007,¶¶156.

The combination of Mieth and Balogh merely involves combining known prior-art elements (Mieth's switchable load and Balogh's cascaded step down converter architecture) according to known methods to yield predictable results, a cascaded step down power converter having a switchable load at the second power converter input that is selectively employed based on the state of the first stage step

down power converter. A PHOSITA would have had the skills, knowledge, and motivation to carry out the combination. Ex.1007,¶157. A PHOSITA would have reasonably expected success in combining Mieth and Balogh. *Id.* A PHOSITA would have appreciated the benefit of adapting the high DC voltage stepped down to an intermediate voltage of Balogh to situations with a variable input voltage to a power converter as shown in Mieth. *Id.* As understood by a PHOSITA, there would have been no undue technical hurdles to applying Mieth with Balogh, as such a combination would have been a simple modification to Mieth's system, readily accomplished by a PHOSITA. *Id.* Accordingly, Mieth in combination with Balogh is proper and teaches [1B]-[1D]. *Id.*

Specifically, while the capacitor 2 discussed in §VII.A.1.ii-§VII.A.1.iv. (see Fig. 1(annotated-1D.1) above) is analogous to the claimed first stage, and the bipolar transistor 16/power supply apparatus 19 is analogous to the claimed second stage, Balogh discloses a cascaded converter arrangement having an isolated DC-DC converter followed by a post regulator circuit that reads on the claimed *first and second stages*, respectively. Ex.1003,10:45-52;Ex.1007,¶158.

Balogh's isolated DC-DC converter (analogous to the first stage-yellow) and post regulator circuit (analogous to the second stage-blue) are cascaded step-down converters and are shown in Fig.1D(annotated-1D.2). Ex.1003,2:61-64;Ex.1007,¶159.

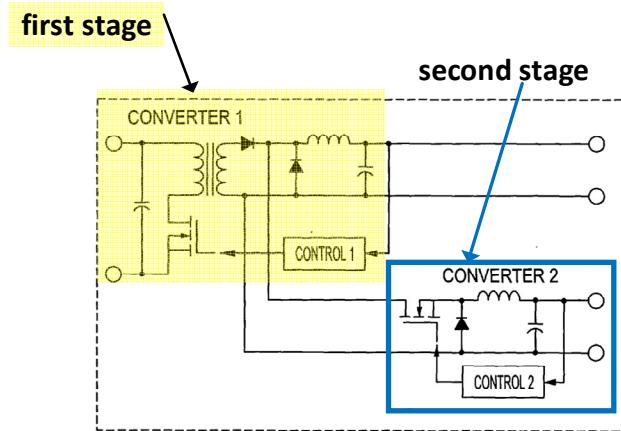


FIG. 1D
PRIOR ART

Ex.1003, Fig.1D(annotated-1D.2)

Based on Balogh, a PHOSITA would understand that cascaded converters are commonly used to provide input to output power conversion that is not optimally implemented in a single converter. Ex.1003,1:25-28.Ex.1007,¶160. Thus, the purpose of the first stage and the second stage was previously described by Balogh, that is to provide input and output power conversion that is not optimally implemented in a single converter, for example, in high DC voltage applications. Ex.1003,10:45-52. The claimed first stage provides a first output to be consumed by the switchable load or to power the second stage, and the claimed second stage uses the first output from the first stage to power the micro-controller, which is not optimally implemented by a single converter (e.g. the first stage or the second stage alone). Ex.1007,¶160. As such, a PHOSITA, at the time of filing, would know that the capacitor 2 and the power supply apparatus 19 of Mieth could be the

cascaded converters as disclosed by Balogh. *Id.* It would be obvious to a PHOSITA to supply power to the claimed micro-controller with a first stage and a second stage separated by a switchable load as recited in claim features [1B]-[1D]. *Id.*

Thus, Mieth-Balogh disclose [1B]-[1D].

Additionally, claims 2-7 and 9 are obvious in view of Mieth-Balogh for the reasons set forth in §VII.B.1. and §VII.B.2.-§VII.B.8.

2. Dependent Claim 8

Claim 1 is taught by Mieth, or by a combination of Mieth and Balogh. Claim 8 depends from claim 1 and requires, “wherein the first stage comprises a first step-down converter; and the second stage comprises a second step-down converter.” Ex.1001, claim 8. As discussed in *Supra*, §VII.B.1., a PHOSITA would have been motivated to combine the cascaded power converter architecture of Balogh with the switchable load features of Mieth. As discussed in *Supra*, §VII.A.1.ii., and Fig.1(annotated-1B), Mieth discloses a capacitor 2 (highlighted-yellow) which is analogous to the claimed *first stage* and discloses power supply apparatus 19 connected to the bipolar transistor 16 (blue) which is analogous to the claimed *second stage*. The power supply apparatus 19 is a DC-DC voltage converter or charging converter which a PHOSITA would understand can step-down DC power and is analogous to the claimed *second stage comprising*

a step-down converter. Ex.1002,8:29-35;Ex.1007,¶163. Mieth teaches that the capacitor 2 is a first stage and Balogh teaches a first stage and a second stage that can each comprise step-down converters. Ex.1003,1:29-36;Ex.1007,¶163. Balogh teaches that a cascaded arrangement can include a first buck converter and a second buck converter where a buck converter steps an input voltage down to an output voltage that is lower than the input voltage. *Id.* It would be obvious to a PHOSITA to modify the capacitor 2 of Mieth with the step-down converter from Balogh to realize the claimed *first stage comprises a first step-down converter; and the second stage comprises a second step-down converter.* Thus, Mieth-Balogh disclose the features of claim 8.

3. Independent Claim 10

With reference to the claim listing appendix, Mieth and Balogh disclose Elements [10A]-[10I]. As explained below, a PHOSITA would have been motivated by Mieth and Balogh to arrive at the alleged invention of claim 10.

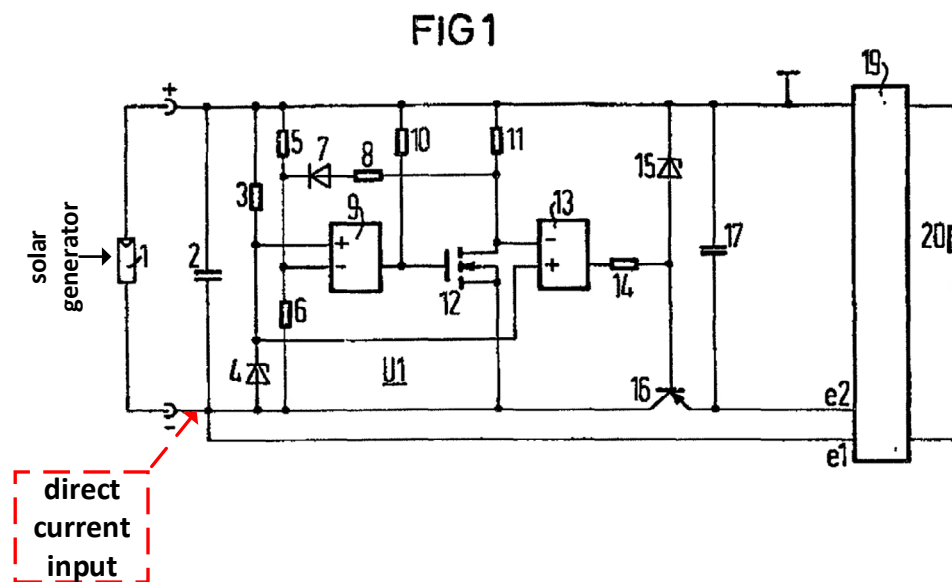
i. [10A]: “A system to supply power, the system comprising:”

Mieth discloses a circuit that supplies power to an electrical load from a solar generator. Ex.1002,8:8-9. A PHOSITA would understand that when the circuit of Mieth supplies power to the electrical load, the circuit is supplying power which is the same as the claimed *system to supply power.* Ex.1007,¶165. Thus, Mieth-Balogh disclose [10A].

ii. [10B]: “a power source to provide a direct current input”

The circuit of Mieth discloses a solar generator 1 that is a power source as shown in Fig.1(annotated-[10B]). Ex.1002,4:29-32. A PHOSITA would understand that solar generators generate a direct current, thus the solar generator 1 provides a direct current input (dashed-red). Ex.1007,¶166.

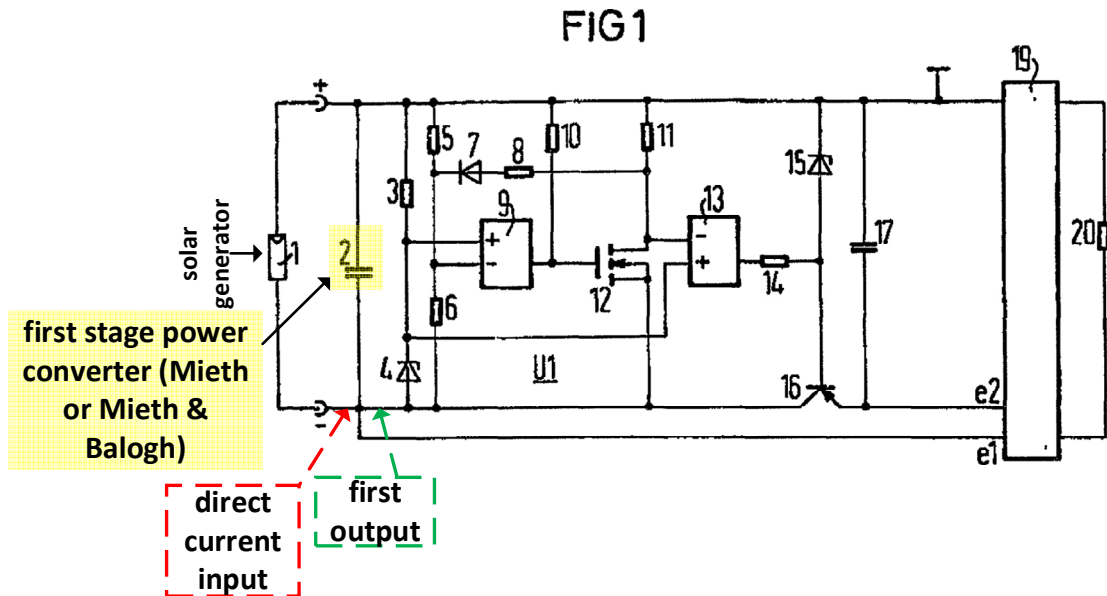
Thus, Mieth-Balogh disclose [10B].



Ex.1002, Fig.1(annotated-[10B])

iii. [10C]: “a first stage power converter configured to convert the direct current input into a first output”

The circuit of Mieth discloses a capacitor 2 (yellow) connected in parallel with solar generator 1 in Fig.1(annotated-[10C]).



Ex.1002, Fig.1(annotated-[10C])

As discussed in §VII.A.1.iii capacitor 2 converts power and thus Mieth teaches a *first stage power converter*, which is anticipatory of claim 10. Additionally, Balogh discloses a first stage power converter and a PHOSITA is motivated to combine Mieth and Balogh for at least the reasons described in accordance with features [1B]-[1D] of claim 1 as discussed in §VII.B.1. Ex.1007,¶168.

Balogh's isolated DC-DC converter (yellow) is a step-down converter and thus analogous to the claimed *first stage power converter* as shown in Fig.1D (annotated-[10C]). Ex.1003,2:61-64;Ex.1007,¶169.

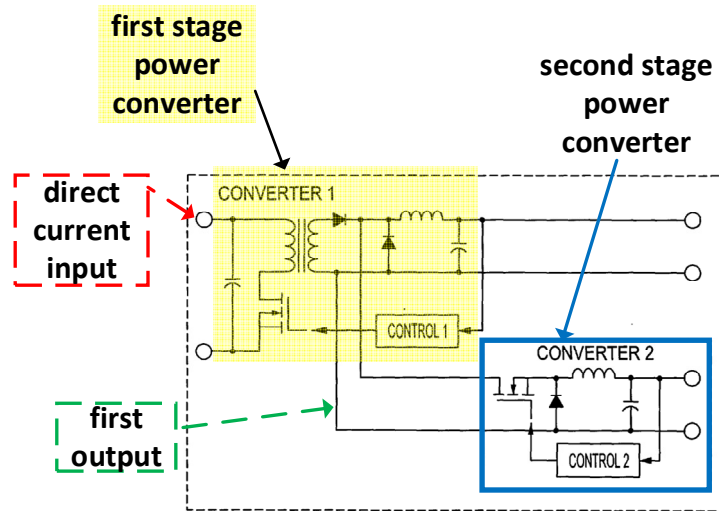


FIG. 1D
PRIOR ART

Ex.1003, Fig.1D (annotated-[10C])

The isolated DC-DC converter shows a capacitor in parallel with a transformer that converts the direct current input (**dashed-red**) to a first output (**dashed-green**). Ex.1003, Fig.1D(annotated-[10C]); Ex.1007, ¶170. A PHOSITA would have been motivated to add a transformer after the capacitor 2 of Mieth to realize the power converter of Balogh to convert the direct current input into a first output. §VII.B.1; §VII.B.1; Ex.1007, ¶170. Since the isolated DC-DC converter converts power from the direct current input to a first output, the isolated DC-DC converter is analogous to the claimed *first stage power converter* and the power converted by the DC-DC converter is analogous to the claimed *convert the direct current input into a first output*. Ex.1007, ¶170.

Since capacitor 2 of Mieth can be replaced or supplemented with the DC-DC converter of Balogh, further discussion of Mieth will refer to capacitor 2 as

analogous to the first stage power converter in view of Balogh for ease of discussion as shown in Fig.1(annotated-[10C]) of Mieth.

Thus, Mieth-Balogh disclose [10C]. Ex.1007,¶171.

- iv. **[10D]: “a second stage power converter configured to be powered by the first output to generate a second output;”**

[10D] is analogous to [1D], and thus Mieth-Balogh disclose [10D] for at least the same reasons Mieth discloses [1D] as described in §VII.A.1.iv. and §VII.B.1. Ex.1007,¶¶173-176.

- v. **[10E]: “a micro-controller powered by the second output; a switchable load; and”**

[10E] is analogous to the micro-controller of [1D] and the switchable load of [1E], and thus Mieth-Balogh disclose [10E] for at least the same reasons Mieth discloses [1D],[1E] as described in §VII.A.1.iv., §VII.B.1., and §VII.A.1.v. Ex.1007,¶¶177-181;Ex.1014,1180,Fig.5.

- vi. **[10F]: “a control circuit powered by the first output and configured to connect the first output to the switchable load to consume at least a portion of the first output while disabling the second stage power converter in supplying the second output to the micro-controller;”**

[10F] is essentially the same as [1E], as such, Mieth-Balogh disclose [10F] just as Mieth discloses [1E]. *Supra*,§VII.A.1.v;Ex.1007,¶¶182-183. [10F] differs from [1E] by reciting “a control circuit powered by the first output.” A PHOSITA would understand that the circuitry that controls the field-effect

transistor 12, which includes the first comparator 9, voltage divider 5, 6 and reference input generator 3, 4, which are powered by the first output from the capacitor 2, is analogous to the claimed *control circuit powered by the first output*. Ex.1002,9:34-10:3;FIG.1(annotated-1E);Ex.1007,¶183.

Thus, Mieth-Balogh disclose [10F].

- vii. [10G]: “determine whether a voltage of the first output powering the switchable load is above a threshold during a time period in which the second output to the micro-controller is disabled; and”

[10G] is analogous to the portion of [1G] that recites, “*in response to . . . the micro-controller is disabled,*” and thus, Mieth-Balogh disclose [10G] for at least the same reasons Mieth discloses [1G] as described in §VII.A.1.vii. Ex.1007, ¶¶185-186.

- viii. [10H]: “in response to the voltage being above the threshold during the time period in which the second output to the micro-controller is disabled, disconnect the switchable load from the first output of the first stage power converter”

[10H] is analogous to the portion of [1G] that recites, “*disconnecting the switchable load from the first output of the first stage,*” and thus, Mieth-Balogh disclose [10H] for at least the same reasons Mieth discloses [1G] as described in §VII.A.1.vii. Ex.1007,¶ ¶188-194.

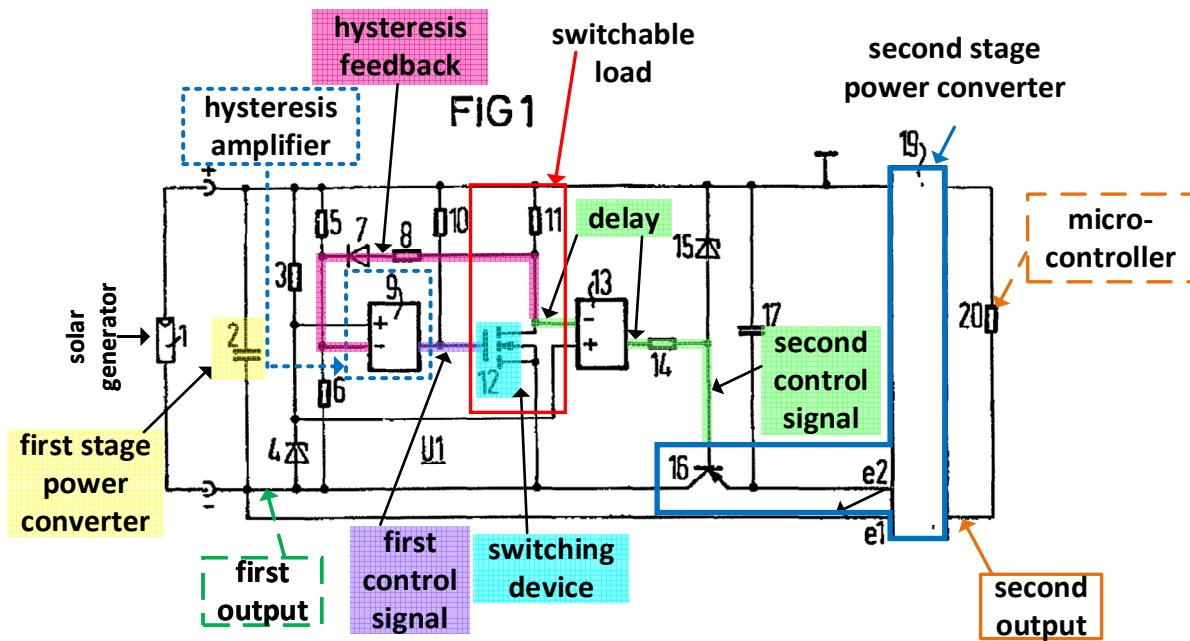
- ix. [10I]: “and signal the second stage power converter to enable the second output to the micro-controller using power from the first output of the first stage power converter.”

[10I] is analogous to the portion of [1G] that recites, “*and instructing . . . of the first stage,*” and thus, Mieth-Balogh disclose [10I] for at least the same reasons Mieth discloses [1G] as described in §VII.A.1.vii. Ex.1007,¶¶195-197.

4. Dependent Claim 11

Claim 10 is disclosed by Mieth-Balogh. *Supra*,§VII.B.3. Claim 11 depends from claim 10 and requires [11A], “wherein the control circuit comprising: a hysteresis amplifier configured to receive the first output and generate a first control signal for the switchable load.” Ex. 1001, claim 11.

As shown in Fig.1(annotated-Claim-11), Mieth discloses a capacitor 2 (highlighted-yellow) analogous to the claimed first power converter and outputs a first output (dashed-green) analogous to the claimed first output, first comparator 9 (dashed-blue) that is analogous to the claimed hysteresis amplifier that outputs a first signal (highlighted-purple) analogous to the claimed first signal that teach [11A] as discussed below.



Ex.1002, Fig.1(annotated-Claim-11)

The hysteresis amplifier of claim 11 is analogous to the hysteresis amplifier of [5A] and thus the comparator 9 of Mieth discloses the claimed hysteresis amplifier for at least the same reasons described in §VII.A.5. Ex.1007,¶¶55-62,77-82,200-201.

The first output of capacitor 2 is represented at the first comparator 9 through a voltage divider defined by resistors 5 and 6 in addition to resistors 8 and 11 and diode 7 when comparator 9 output is low, which is analogous to the claimed *hysteresis amplifier configured to receive the first output*. Ex.1002,9:34-38;Ex.1007,¶202. The output of first comparator 9 is a first signal as discussed previously in §VII.A.3. (e.g., claim 3 recites “first signal” which is analogous to claim 11’s “first control signal”), and is analogous to the claimed recitation

generate a first control signal. Ex.1007,¶202. Specifically, since the output of first comparator 9 turns transistor 12 “on” and “off,” a PHOSITA understands that the output is analogous to the claimed *first control signal* as the output from first comparator 9 operates transistor 12 just as the claimed first control signal for the claimed switchable load. Ex.1007,¶202.

A PHOSITA understands that the circuitry of Mieth, including first comparator 9, is analogous to the claimed *control circuit* as first comparator 9 generates the first control signal that controls transistor 12. Ex.1007,¶203. Thus, Mieth teaches [11A].

Claim 11 further requires feature [11B], “a delay circuit to generate a second control signal for the second stage power converter by delaying the first signal.” [11B] is analogous to [5B], and thus, Mieth-Balogh disclose [11B] for at least the same reasons Mieth discloses [5B] as described in §VII.A.5. Ex.1007,¶¶204-208.

Thus, Mieth-Balogh discloses [11B] and all the features of claim 11.

5. Dependent Claim 12

Claim 11 is disclosed by Mieth-Balogh. *Supra*,§VII.B.4. Claim 12 depends from claim 11 and requires [12A], “wherein in response to the voltage going above the threshold: the first control signal causes the switchable load to be disconnected from the first output of the first stage power converter.” Ex.1001, claim 12.

preliminary load 11 is disconnected from the first output of capacitor 2 (first stage power converter-highlighted-yellow). *Id.* As such, first comparator 9 outputting the first control signal that turns off transistor 12 to disconnect the preliminary load 11 from the first output of the capacitor 2 is analogous to the claimed *the first control signal causes the switchable load to be disconnected from the first output of the first stage power converter.* Ex.1007,¶211.

Thus, Mieth teaches [12A].

Claim 12 further requires [12B], “the second control signal causes the second stage power converter to enable the second output to the micro-controller.”

Mieth discloses that transistor 12 is connected to second comparator 13 and delays the first signal from first comparator 9 to generate a second control signal (highlighted-green) that turns on transistor 16. Ex.1002,11:1-12;Ex.1007,¶214.

When transistor 16 turns on, the first output is connected to the e2 input to energize power supply apparatus 19 (second stage-blue) which enables the second output (orange) of power supply apparatus 19 to power load 20 (micro-controller-dashed-orange), which is analogous to the features of [12B] as discussed below.

Ex.1002,Fig.1,11:4-12,12:12-19;Ex.1007,¶214.

Transistor 16 operates as a switch that connects the first output to power supply apparatus 19. Ex.1002,10:31-36,Ex.1007,¶215. The base of transistor 16, which controls the conducting/non-conducting state of transistor 16, is controlled

by second comparator 13. Ex.1002,10:36-11:12;Ex.1007,¶215. Second comparator 13 outputs the second control signal based on an input from transistor 12, where the output from transistor 12, when it turns off, “trips” second comparator 13. *Id.* Second comparator 13 generates the second control signal based on the first control signal which is analogous to the claimed *second control signal*, and the second control signal controls transistor 16 which is analogous to the claimed *causes the second stage power converter stage*... Ex.1007,¶215.

When power supply apparatus 19 is powered, the second output is enabled to load 20. Ex.1002,8:29-35;Ex.1007,¶216. Transistor 16 turned on by the second control signal, which enables the second output to load 20, is analogous to the claimed *second control signal . . . enable the second output to the micro-controller*. Ex.1007,¶216.

Thus, Mieth-Balogh disclose [12A], [12B], and all of claim 12.

6. Dependent Claim 15

Claim 12 is disclosed by Mieth-Balogh. *Supra*,§VII.B.5. Claim 15 depends from claim 12 and requires [15A], “wherein the switchable load comprises: a resistive device; and a switching device connected to the resistive device”.

Ex.1001,claim 15.

[15A] is analogous to [2A]-[2B] thus, Mieth-Balogh disclose [15B] for at least the same reasons Mieth discloses [2A]-[2B] as described in §VII.A.2. Ex.1007,¶¶218-221.

Claim 15 further requires [15B], “wherein the switching device is configured to be turned on to be connected to the first output to consume the portion of the first output and turned off to be disconnected from the first stage.” Ex.1001, claim 15. [15B] is analogous to [2C], thus, Mieth-Balogh disclose [15C] for at least the same reasons as Mieth discloses [2C] as described in §VII.A.2. Ex.1007,¶ 222.

Claim 15 further requires [15C], “wherein the first control signal is connected to control the switching device.” Ex.1001, claim 15. The output (highlighted-purple) of first comparator 9 (Fig.1(annotated-Claim-3)) is a first signal as discussed previously in §VII.A.3. (*e.g.*, claim 3 recites “first signal”), and is analogous to the claimed *first control signal*. Ex.1007,¶223. The output of the first comparator 9 turns transistor 12 “on” and “off,” thus a PHOSITA understands that the output of comparator 9 controls transistor 12. Ex.1007,¶223. Thus, the output of comparator 9 that turns transistor 12 “on” and “off” is analogous to the claimed *first control signal is connected to control the switching device*. Ex.1007,¶223.

As such, Mieth-Balogh disclose all the features of claim 15.

7. Dependent Claim 16

Claim 15 is disclosed by Mieth-Balogh. *Supra*, §VII.B.6. Claim 16 depends from claim 15 and requires, “wherein the switching device includes one of: a field effect transistor (FET), a metal-oxide-semiconductor field-effect-transistor (MOSFET), and a bipolar junction transistor.” Ex.1001, claim 15.

Claim 16 is the same as claim 6, and Thus, Mieth discloses claim 16 for the same reasons that Mieth discloses claim 6. *Supra*, §VII.A.6.; Ex.1007, ¶¶ 225-226.

8. Dependent Claim 17

Claim 16 is disclosed by Mieth-Balogh. *Supra*, §VII.B.7. Claim 17 depends from claim 16 and requires, “wherein when the switch device is turned on, the switchable load and an input of the second stage are connected in parallel to the first output of the first stage.” Ex.1001, claim 15.

Claim 17 is the same as claim 7, and thus, Mieth-Balogh disclose claim 17 for the same reasons that Mieth disclose claim 7. *Supra*, §VII.A.7.; Ex.1007, ¶¶ 227-228.

9. Independent Claim 18

With reference to the claim listing appendix, Mieth discloses Elements [18A]-[18I]. As explained below, a PHOSITA would have been motivated by Mieth and Balogh to arrive at the alleged invention of claim 18.

i. [18A]: “A system to supply power, the system comprising:”

[18A] is identical to [10A] Thus, Mieth discloses [18A] for at least the same reasons as Mieth disclose [10A] as described in §VII.B.3.i. Ex.1007,¶230.

ii. [18B]: “a photovoltaic panel to provide a direct current input”

[18B] is essentially the same as [10B], as such, Mieth discloses [18B] for at least the same reasons Mieth discloses [10B]. §VII.B.3.ii,Ex.1007,¶234. [18F] differs from [10B] by reciting “a photovoltaic panel” rather “a power source.” A PHOSITA would understand that the solar generator 1 of Mieth is analogous to the claimed *photovoltaic panel*. Ex.1007,¶¶233-235.

iii. [18C]: “a first stage power converter connected to the photovoltaic panel to generate a first output from the direct current input”

[18C] is analogous to [10C]. Thus, Mieth or Mieth-Balogh disclose [18C] for at least the same reasons described in §VII.B.3.iii. Ex.1007,¶¶236-242.

iv. [18D]: “a second stage power converter connected to convert the first output to a second output”

[18D] is analogous to [1D]. Thus, Mieth or Mieth-Balogh disclose [18D] for at least the same reason Mieth discloses [1D] as described in §VII.A.1.iv. Ex.1007,¶¶243-246.

v. [18E]: “a micro-controller”

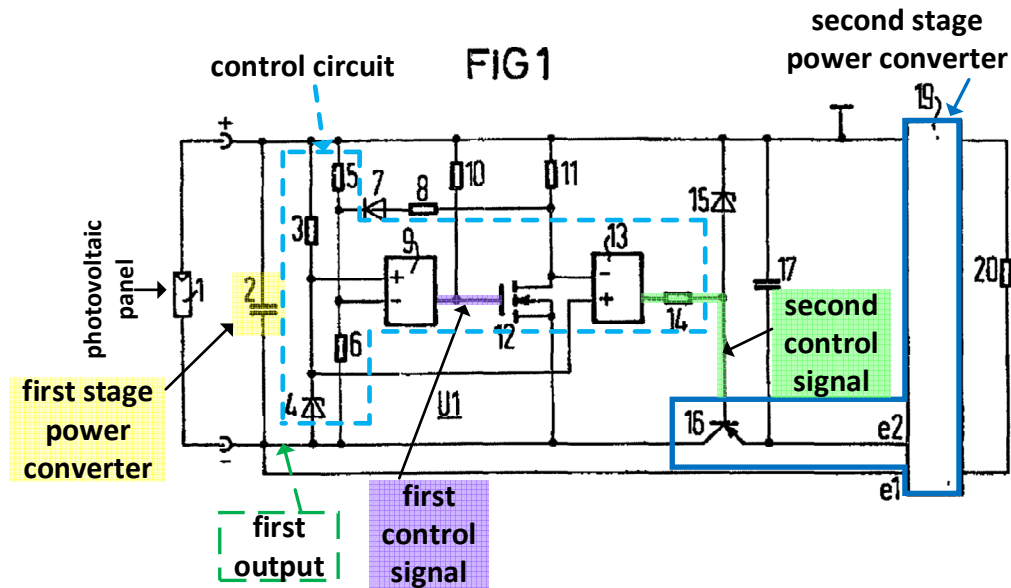
[18E] is analogous to the micro-controller of [1D]. Thus, Mieth or Mieth-Balogh disclose [18E] for at least the same reasons Mieth discloses [1D] described in §VII.A.1.iv. Ex.1007,¶¶247-250;Ex.1014,1180,Fig.5.

vi. [18F]: “a power absorption circuit”

[18F] is analogous to the “*switchable load*” of [1F] as such, Mieth discloses [18F] just as Mieth discloses [1F]. §VII.A.1.vi,Ex.1007,¶¶251-253. That is, the preliminary load 11 (see Fig.1(annotated-1F)) would be understood by a PHOSITA as the claimed *power absorption circuit*. *Id.*

vii. [18G]: “a control circuit coupled with the first stage power converter and the second stage power converter, the control circuit powered by the first output to control the second stage power converter”

Mieth discloses a first comparator 9 that turns the transistor 12 “on” or “off” as shown in Fig.1(annotated-[18G]). Ex.1002,9:34-10-14;Ex.1007,¶254.



Ex.1002, Fig.1 (annotated-[18G])

First comparator 9 compares a reference voltage from a reference voltage generator to a representative voltage from a voltage divider. Ex.1002,9:34-10:3;Ex.1007,¶255. The reference voltage generator is defined by the Zener diode 4 and the resistor 3. *Id.* The voltage divider is defined by the voltage divider of resistors 5 and 6 and the representative voltage is representative of the first output (dashed-green) of capacitor 2 (first stage power converter-yellow). *Id.* First comparator 9 compares the representative voltage to the reference voltage to determine if the representative voltage exceeds a value defined by the reference voltage, and outputs a first control signal (highlighted-purple) to transistor 12 based on the comparison. Ex.1002,12:12-26,Ex.1007,¶255.

A PHOSITA understands that the circuitry (dashed-blue) that controls transistor 12, which includes first comparator 9, voltage divider 5, 6 and reference

input generator 3, 4, which are powered by the first output from the capacitor 2, is analogous to the claimed **a control circuit coupled with the first stage power converter** and the claimed **the control circuit powered by the first output**.

Ex.1002,9:34-10:3,Ex.1007,¶256.

The first control signal output from first comparator 9 controls transistor 12, and the output of transistor 12 is used by second comparator 13 to generate a second control signal (**highlighted-green**). Ex.1002,11:4-12,12:12-19;Ex.1007,¶257. The second control signal output from second comparator 13 operates transistor 16, turning the transistor “on” or “off” which connects or disconnects power supply apparatus 19 to or from the first output. *Id.* When the first control signal is low, transistor 12 is “off” and second comparator 13 outputs a low voltage which turns transistor 16 “on,” connecting the power supply apparatus 19 to the first output of capacitor 2. Ex.1002,12:12-30;Ex.1007,¶257. When the first control signal is high, transistor 12 is “on” which connects preliminary load 11 to the first output of capacitor 2, and second comparator 13 outputs a high voltage which turns transistor 16 “off,” disconnecting power supply apparatus 19 from the first output of capacitor 2. Ex.1002,9:15-23,12:12-30;Ex.1007,¶257.

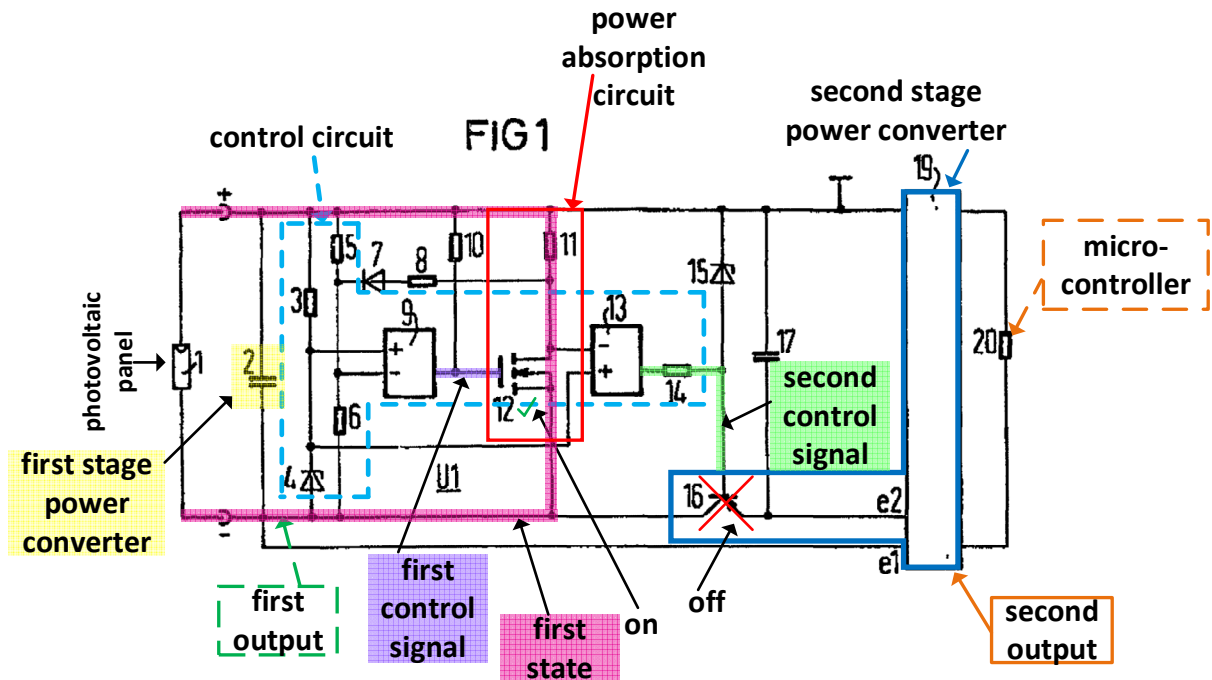
Since first comparator 9 generates the first control signal that controls transistor 16/power supply apparatus 19 through transistor 12 and the second comparator, Mieth discloses the claimed **to control the second stage power**

converter. Ex.1007,¶258. Furthermore, the first comparator 9 couples to transistor 16/power supply apparatus 19 through transistor 12 and the second comparator 13, which is analogous to the claimed *a control circuit coupled with . . . the second stage power converter*. Ex.1007,¶258.

Thus, Mieth teaches [18G].

- viii. [18H]: “when the second stage power converter is disabled in providing the second output to the micro-controller, the control circuit monitors a voltage of the first output powering the power absorption circuit and signals the second stage power converter to continue disabling the providing of the second output to the micro-controller during a time period in which the voltage is below a threshold;”

As shown in Fig.1(annotated-[18H]), Mieth can be configured in a first state (highlighted-pink) where transistor 16 is “off” and power supply apparatus 19 (second stage-blue) is disconnected from the first output of capacitor 2 (*i.e.*, first stage-highlighted-yellow). *Supra*,§VII.A.15.vii., Ex.1002,12:12-30;Ex.1007,¶260.



Ex.1002, Fig.1(annotated-[18H])

When transistor 16 is “off,” power supply apparatus 19 is disconnected from the first output (dashed-green) of capacitor 2, and load 20 (micro-controller-dashed-orange) is not powered by the second output (orange).

Supra, §VII.A.15.vii.; Ex.1002, 8:29-35, 9:9-13, 9:23-32; Ex.1007, ¶261. Transistor 16/power supply apparatus 19 being off and disconnected from the first output of capacitor 2, which results in load 20 not powered by the second output is analogous to the claim feature *when the second stage power converter is disabled in providing the second output to the micro-controller*. Ex.1007, ¶261.

Furthermore, in the first state, transistor 12 is turned “on” and the first output powers preliminary load 11 (power absorption circuit-red). Ex.1002, 10:5-14; Ex.1007, ¶262. First comparator 9 (control circuit-dashed-blue) turns transistor

12 “on” based on a comparison of a reference voltage (from reference voltage generator defined by Zener diode 4 and resistor 3) and a representative voltage (based on a tap of voltage divider 5, 6 representative of the first output voltage. Ex.1002,9:34-10:3,Ex.1007,¶262. First comparator 9 that connects preliminary load 11 to the first output through control of transistor 12 based on the representative voltage of the first output is analogous to the claimed ***the control circuit monitors a voltage of the first output powering the power absorption circuit***. Ex.1007,¶262.

The representative voltage at first comparator 9 is compared to a “predefined minimum value,” (e.g., associated with a threshold voltage) and during a time period when the reference voltage is lower than the predefined minimum value, the first control signal from first comparator 9 is a high voltage which turns transistor 12 “on.” Ex.1002,11:4-12,12:12-26;Ex.1007,¶263. The time period when the representative voltage is lower than the predefined minimum value is analogous to the claimed ***during a time period in which the voltage is below a threshold***. Ex.1007,¶263.

When transistor 12 is “on,” preliminary load 11 is connected to the first output of capacitor 2, which signals a high voltage to second comparator 13, which signals a high voltage to transistor 16, turning power supply apparatus 19 “off,” which disables the second output from powering load 20. Ex.1002,9:15-23,12:12-

30;Ex.1007,¶264. Therefore, first comparator 9 turning transistor 12 “on” signals power supply apparatus 19 to be turned “off” through transistor 16, thereby disabling the second output from powering the load, which is analogous to the claimed *signals the second stage power converter to continue disabling the providing of the second output to the micro-controller*. Ex.1007,¶264.

Thus, Mieth disclose [18H].

- ix. [18I]: “when the voltage is above the threshold, the control circuit signals the second stage power converter to enable the providing of the second output to the micro-controller”

[18I] is analogous to the portion of [1G] that recites, “*in response to . . . is above the threshold,*” and “*instructing the second stage to enable the second output to the micro-controller.*” Thus, Mieth discloses [18I] for at least the same reasons Mieth discloses [1G] as described in §VII.A.1.vii. Ex.1007,¶¶266-270.

10. Dependent Claim 20

Claim 18 is disclosed by Mieth or Mieth-Balogh. *Supra*,§VII.B.9. Claim 20 depends from claim 18 and requires [20A], “wherein the power absorption circuit comprises a switchable load” Ex.1001, claim 20.

[20A] is analogous to the “*switchable load*” of [1F] as such, Mieth-Balogh discloses [20A] just as Mieth discloses [1F]. §VII.A.1.vi.;Ex.1007,¶273.

Claim 20 further requires [20B], “and the control circuit signals the switchable load to be in a first state to consume a portion of the first output when the voltage is below the threshold.” Ex.1001, claim 20.

[20B] is analogous to the “*switchable load to consume . . . of the first output*” of [1E]-[1F] as such, Mieth-Balogh disclose [20B] just as Mieth discloses [1E]-[1F]. §VII.A.1.v.- §VII.A.1.vi.;Ex.1007,¶¶274-276.

Claim 20 further requires [20C], “and to be in a second state not to consume a portion of the first output when the voltage is above the threshold.” Ex. 1001, claim 20.

[20C] is analogous to the “*is above the threshold . . . disconnecting the switchable load*” of [1G]. Thus, Mieth or Mieth-Balogh disclose [20C] just as Mieth discloses [1G]. §VII.A.1.vii;Ex.1007, ¶¶278-281.

C. Ground C: Obviousness of claims 13 and 14 in view of Mieth, Balogh, and further in view of Nishi

1. Dependent Claim 13

Claim 12 is taught by Mieth-Balogh. *Supra*,§IIV.B.5. Claim 13 depends from claim 12 and requires, “wherein the micro-controller is configured to maximize power generated by the power source.”

Mieth discloses a circuit that supplies power to an electrical load from a solar generator, such as load 20 and the solar generator 1 in Fig.1(annotated-[10B]) above. Ex.1002,8:8-9,20-27;Ex.1007,¶283. A PHOSITA would understand that

the solar generator 1 generates power and is analogous to the claimed *power source*. Ex.1007,¶283. Nishi (Ex.1004) discloses a microcomputer 109 that controls input voltage so that output power from a solar cell array is maximized, which is analogous to the features of claim 13 as discussed further below. Ex.1004,¶¶[0008],[0098];Ex.1007,¶283.

Figs.2,7(annotated-Claim-13) of Nishi below shows solar cell arrays 2A-2D connected to converters 5A-5D and controlled by an inverter 6, where an input voltage to the inverter 6 (i.e., output voltage of converters 5A-5D) is controlled so that the output power from the solar cell arrays 2A-2D is maximized. Ex.1004,¶¶[0096]-[0098];Ex.1007,¶284.

generated by the power source, and further analogous to the output of the solar generator 1 of Mieth. Ex.1007,¶285. The inverter 6 (blue) changes an output current of the inverter 6 in accordance with a pulse width modulation (PWM) control signal from inverter control unit 13 (green). Ex.1004,¶¶[0070],[0083]-[0084]. Inverter control unit 13 controls the PWM control signal based on an input and output of inverter 6 (e.g., voltage sensor 14E and current sensor 12E), to realize a desired input voltage of inverter 6. Ex.1004,¶[0088]. Further, the inverter control unit 13 operates converter control units 11A-11D based on the input and output of inverter 6 to realize the desired input voltage of inverter 6. Ex.1004,¶¶[0083]-[0084], ¶[0097]. Subsequently, the converter control units 11A-11D to adjust a pulse width of a pulse frequency modulation (PFM) to the converters 5A-5D such that the “output power from a corresponding solar cell array becomes maximum” Ex.1004,¶[0098].

Nishi discloses, in Fig. 7, that an inverter apparatus (dashed-red) can include an inverter 102 (blue), and a microcomputer 109 (orange), where the microcomputer 109 can have control means 105 (green). Ex.1004,¶[0008]. The inverter 6, inverter control unit 13, converter control units 11A-11D and converters 5A-5D are all part of an inverter apparatus (dashed-red) of Nishi-Fig. 2 and analogous to the inverter apparatus of Nishi-Fig. 7. Ex.1007,¶286. As such, the inverter 6 of Nishi-Fig. 2 is analogous to the inverter 102 of Nishi-Fig. 7. *Id.*

Nishi-Fig. 2 shows that control circuitry 105 can be implemented in a microcomputer, thus inverter control unit 13 (green) and converter control units 11A-11D (green), which are analogous to control 105, can be implemented in a microcomputer (orange). *Id.*

A PHOSITA would understand that a microcomputer is analogous to a micro-controller, and thus the inverter control unit 13 and the converter control units 11A-11D of Nishi can be microcomputers and are analogous to the claimed ***micro-controller***. Ex.1007,¶¶286-287. Since inverter control unit 13 is controlling inverter 6 to maximize the output power from the solar array, the features of Nishi are analogous to the claimed ***micro-controller is configured to maximize power generated by the power source***. *Id.*

Nishi discloses an inverter apparatus with a microcomputer that maximizes the output power of a solar cell array. Ex.1004,¶¶[0008],[0085],[0096]-[0098];Ex.1007,¶288. Mieth discloses a solar generator 1 analogous to the solar cell array of Nishi, where the solar generator 1 connects to a load 20 that is analogous to the inverter apparatus of Nishi. Ex.1002,4:29-32,8:29-35;Ex.1007,¶288. It is well known to a PHOSITA that solar systems that include solar panels and loads with inverters benefit from maximum power point tracking to maximize the power generated from a solar array. Ex.1004,¶¶[0030];Ex.1007,¶288. Thus it would have been obvious to a PHOSITA

to combine the reliable startup circuit of Mieth with the maximum power point tracking configuration of Nishi to realize the features of claim 13. Ex.1007,¶288.

Thus, Mieth-Balogh-Nishi disclose the features of claim 13.

2. Dependent Claim 14

Claim 13 is taught by the combination of Mieth-Balogh-Nishi. *Supra*, §VII.C.1. Claim 14 depends from claim 13 and requires, “wherein the power source comprises a photovoltaic panel; the first stage power converter comprises a first step-down converter; and the second stage power converter comprises a second step-down converter.” The claimed **photovoltaic panel** is analogous to the solar cell arrays 2A-2D of Nishi. Ex.1004,¶[0060];Ex.1007,¶¶291-293. The claimed **first step-down converter** and **second step-down converter** are identical to the features of claim 8 as discussed in §VII.B.2. Ex.1007, ¶¶291-293. Thus, Mieth-Balogh-Nishi disclose the features of claim 14.

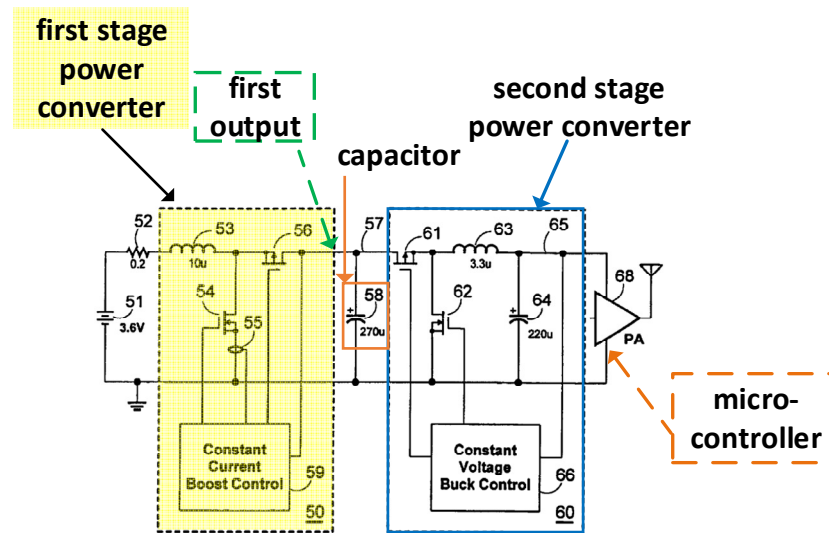
D. Ground D: Obviousness of Claim 19 in view of Mieth, Balogh, and further in view of Liu

Claim 18 is taught by the combination of Mieth and Balogh. *Supra*,§VII.B.9. Claim 19 depends from claim 18 and requires [19A], “wherein the power absorption circuit includes a capacitor coupled to the first output.”

Mieth discloses transistor 12 connected to preliminary load 11 to form the claimed ***power absorption circuit coupled to the first output*** as discussed in §VII.B.9.viii. Ex.1007,¶295. Additionally, Liu (Ex.1005) discloses a capacitor as

a power absorption circuit coupled to the first output, and a PHOSITA is motivated to combine Mieth and Liu for the following reasons.

As shown in Fig.5(annotated-Claim-19), Liu discloses cascaded DC voltage converters with an input stage 50 separated from an output stage 60 by a reservoir capacitor 58. Ex.1005,4:25-35;Ex.1007,¶296.



Ex.1005, Fig.5(annotated-Claim-19)

Input stage 50 up-converts the voltage from battery 51 to charge reservoir capacitor 58, and output stage 60 down converts the voltage of reservoir capacitor 58 to power a power amplifier (“PA”) 68. Ex.1005,4:36-43;Ex.1007,¶297. Since input stage 50 (highlighted-yellow) converts an input voltage to an output voltage, input stage 50 is analogous to the claimed first stage power converter of claim 18, and the output (dashed-green) of input stage 50 is analogous to the claimed *first output* of claim 19. Ex.1007,¶297. Since reservoir capacitor 58 (orange) is

charged from the first output of input stage 50, reservoir capacitor 58 absorbs the first output of input stage 50 and is analogous to the claimed ***power absorption circuit includes a capacitor coupled to the first output***. Ex.1007,¶297. Thus, Liu teaches [19A].

Claim 19 further requires [19B], “and the threshold allows the capacitor to power the second stage to operate the micro-controller for a predetermined period of time even without the output of the first stage.” neither claim 18 nor 19 provides antecedence for “first stage” and “second stage” and thus are interpreted to mean “first stage power converter” and “second stage power converter,” respectively, as recited in claim 18.

It is unclear to a PHOSITA how the claimed “threshold” allows a capacitor to power the second stage, as a threshold is a value or a level and not a circuit component such as a control circuit. Ex.1007,¶299. For purposes of interpretation, the claimed threshold that allows the capacitor to power the second stage is interpreted as, “when the voltage (of claim 18) is above the threshold, the capacitor powers the second stage . . . ” Ex.1007,¶299. As such, the capacitor that powers the second stage is charged to the threshold voltage capable of providing power to the second stage and operate the micro-controller for a predetermined period of time without the output of the first stage. Ex.1007,¶299.

Liu teaches that reservoir capacitor 58 provides most of the energy to PA 68 through output stage 60 for a period of time when battery 51 cannot supply power to the PA 68. Ex.1005,1:8-12,4:43-51;Ex.1007,¶300. A PHOSITA understands that capacitor 58 provides power to the PA 68 for a predetermined period of time by sizing the capacitor appropriately. Ex.1007,¶300. Furthermore, while Liu shows PA 68 powered by reservoir capacitor 58 through output stage 60, a PHOSITA understands that reservoir capacitor 58 and output stage 60 could power another load such as the claimed *micro-controller*. *Id.* Thus, capacitor 58 that can provide power to the PA 68 for a period of time is analogous to the claimed *capacitor to power the second stage to operate the micro-controller for a predetermined period of time even without the output of the first stage*. *Id.*

Liu discloses cascaded power converters with a capacitor that provides power to a load through a second power converter for a period of time without incoming power from a first power converter. Ex.1005,4:36-43;Ex.1007,¶301. Mieth teaches use of a power absorption circuit when an input voltage to a power converter varies, such as the voltage from a photovoltaic system that varies depending upon time of day, or weather conditions. Ex.1002,5:22-38. Mieth disconnects the switchable load between first stage and second stage power converters when the input voltage to the first stage power converter meets a stable criteria according to a voltage threshold. *Id.* A PHOSITA is motivated to combine

the capacitor of Liu with the power absorption circuit of Mieth, as the capacitor provides a more stable power source to Mieth's load for a predetermined time period when the power absorption circuit is disconnected from the circuit or voltage from the photovoltaic system is varying due to dynamic conditions. *Id.*

A PHOSITA is motivated to employ known means in the art, as taught in Liu, to modify the circuit of Mieth (e.g., Fig. 1(annotated-[18H]) such that when the representative voltage connected to comparator 9 is below the predefined minimum value according to the first output, the capacitor of Liu powers load 20 (i.e., micro-controller) through power supply apparatus 19 (i.e., the second stage power converter) for a predetermined period of time, *which is analogous to [19B]*. Ex.1007, ¶¶301-302. Therefore, both Mieth and Liu provide an express motivation to combine together to improve a cascaded power converter system by including a capacitor in the power absorption circuit. *Id.*

The combination of Mieth-Liu involves combining known prior-art elements (replacing/combining Mieth's resistive load between converters with Liu's capacitive load between converters) according to known methods to yield predictable results, a cascaded power converter having a capacitive load at the second power converter input. A PHOSITA has the skills, knowledge, and motivation to carry out the combination. Ex.1007,¶303. A PHOSITA would reasonably expect success in combining Mieth and Liu, and there is no undue

technical hurdles in combining Mieth with Liu, as the combination is a simple modification to Mieth's system. *Id.*

Thus, Mieth-Balogh-Liu disclose [19B].

E. CONCLUSION

Inter partes review of claims 1-20 should be instituted and the claims cancelled.

Respectfully submitted,

April 24, 2023

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F. CERTIFICATE OF COMPLIANCE WITH WORD COUNT

Pursuant to 37 C.F.R. § 42.24(a)(1)(i), I certify that this paper includes 13,992 words. In accordance with 37 C.F.R. § 42.24(a)(1), this word count does not include a count of the words in a table of contents, a table of authorities, mandatory notices under § 42.8, a certificate of service or word count, or appendix of exhibits or claim listing. Furthermore, in accordance with 37 C.F.R. § 42.24(d), this word count is the word count of the word-processing system used to prepare the paper.

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.105, I hereby certify that I caused a true and correct copy of the Petition for *Inter Partes* Review in connection with U.S. Patent No. 9,584,021 and supporting evidence to be served via FedEx Priority Overnight on April 21, 2023, on the following:

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CLAIM LISTING APPENDIX

U.S. Patent No. 9,584,021 - Avrutsky	
Claim Element Designation	Claim Element
Claim 1	
[1A]	A method to supply power,
[1B]	the method comprising: providing a power supply having a first stage and a second stage,
[1C]	wherein the first stage converts power from a direct current input into a first output,
[1D]	and the second stage powered by the first output has a second output for a micro-controller;
[1E]	connecting the first output of the first stage to a switchable load to consume at least a portion of the first output while disabling the second stage in supplying the second output to the micro-controller;
[1F]	determining whether the first output from the first stage powering the switchable load is above a threshold during a time period in which the second output to the micro-controller is disabled; and
[1G]	in response to a determination that the first output from the first stage powering the switchable load is above the threshold during the time period in which the second output to the micro-controller is disabled, disconnecting the switchable load from the first output of the first stage; and instructing the second stage to enable the second output to the micro-controller using power from the first output of the first stage.
Claim 2	
[2A]	The method of claim 1, wherein the switchable load comprises: a resistive device; and
[2B]	a switching device connected to the resistive device,
[2C]	wherein the switching device is configured to be turned on to be connected to the first output to consume the portion of the first output and turned off to be disconnected from the first stage.
Claim 3: The method of claim 2, wherein the disconnecting of the switchable load from the first output of the first stage comprises sending a first signal to the switching device to turn off the switching device.	
Claim 4	

[4A]	The method of claim 3, further comprising: generating the first signal based on the determining of whether the first output from the first stage powering the switchable load is above the threshold; and
[4B]	delaying the first signal to generate a second signal to the second stage, the second signal enabling the second output to the micro-controller.
Claim 5	
[5A]	The method of claim 4, further comprising: providing a control circuit comprising: a hysteresis amplifier configured to receive the first output of the first stage and generate the first signal; and
[5B]	a delay circuit to generate the second signal according to the first signal.
Claim 6: The method of claim 3, wherein the switching device includes one of: a field effect transistor (FET), a metal-oxide-semiconductor field-effect-transistor (MOSFET), and a bipolar junction transistor.	
Claim 7: The method of claim 6, wherein when the switch device is turned on, the switchable load and an input of the second stage are connected in parallel to the first output of the first stage.	
Claim 8: The method of claim 1, wherein the first stage comprises a first step-down converter; and the second stage comprises a second step-down converter.	
Claim 9: The method of claim 1, wherein the disconnecting is performed prior to the instructing of the second stage to enable the second output to the micro-controller.	
Claim 10	
[10A]	A system to supply power, the system comprising:
[10B]	a power source to provide a direct current input;
[10C]	a first stage power converter configured to convert the direct current input into a first output;
[10D]	a second stage power converter configured to be powered by the first output to generate a second output;
[10E]	a micro-controller powered by the second output; a switchable load; and
[10F]	a control circuit powered by the first output and configured to connect the first output to the switchable load to consume at least a portion of the first output while disabling the second stage power converter in supplying the second output to the micro-controller;

[10G]	determine whether a voltage of the first output powering the switchable load is above a threshold during a time period in which the second output to the micro-controller is disabled; and
[10H]	in response to the voltage being above the threshold during the time period in which the second output to the micro-controller is disabled, disconnect the switchable load from the first output of the first stage power converter
[10I]	and signal the second stage power converter to enable the second output to the micro-controller using power from the first output of the first stage power converter.
Claim 11	
[11A]	The system of claim 10, wherein the control circuit comprising: a hysteresis amplifier configured to receive the first output and generate a first control signal for the switchable load; and
[11B]	a delay circuit to generate a second control signal for the second stage power converter by delaying the first signal.
Claim 12	
[12A]	The system of claim 11, wherein in response to the voltage going above the threshold: the first control signal causes the switchable load to be disconnected from the first output of the first stage power converter; and
[12B]	the second control signal causes the second stage power converter to enable the second output to the micro-controller.
Claim 13: The system of claim 12, wherein the micro-controller is configured to maximize power generated by the power source.	
Claim 14: The system of claim 13, wherein the power source comprises a photovoltaic panel; the first stage power converter comprises a first step-down converter; and the second stage power converter comprises a second step-down converter.	
Claim 15	
[15A]	The system of claim 12, wherein the switchable load comprises: a resistive device; and a switching device connected to the resistive device,
[15B]	wherein the switching device is configured to be turned on to be connected to the first output to consume the portion of the first output and turned off to be disconnected from the first stage, and
[15C]	wherein the first control signal is connected to control the switching device.

Claim 16: The system of claim 15, wherein the switching device includes one of: a field effect transistor (FET), a metal-oxide-semiconductor field-effect-transistor (MOSFET), and a bipolar junction transistor.	
Claim 17: The system of claim 16, wherein when the switch device is turned on, the switchable load and an input of the second stage are connected in parallel to the first output of the first stage.	
Claim 18	
[18A]	A system to supply power, the system comprising:
[18B]	a photovoltaic panel to provide a direct current input;
[18C]	a first stage power converter connected to the photovoltaic panel to generate a first output from the direct current input;
[18D]	a second stage power converter connected to convert the first output to a second output;
[18E]	a micro-controller;
[18F]	a power absorption circuit; and
[18G]	a control circuit coupled with the first stage power converter and the second stage power converter, the control circuit powered by the first output to control the second stage power converter, wherein
[18H]	when the second stage power converter is disabled in providing the second output to the micro-controller, the control circuit monitors a voltage of the first output powering the power absorption circuit and signals the second stage power converter to continue disabling the providing of the second output to the micro-controller during a time period in which the voltage is below a threshold;
[18I]	when the voltage is above the threshold, the control circuit signals the second stage power converter to enable the providing of the second output to the micro-controller.
Claim 19	
[19A]	The system of claim 18, wherein the power absorption circuit includes a capacitor coupled to the first output;
[19B]	and the threshold allows the capacitor to power the second stage to operate the micro-controller for a predetermined period of time even without the output of the first stage.
Claim 20	
[20A]	The system of claim 18, wherein the power absorption circuit comprises a switchable load;

[20B]	and the control circuit signals the switchable load to be in a first state to consume a portion of the first output when the voltage is below the threshold
[20C]	and to be in a second state not to consume a portion of the first output when the voltage is above the threshold.