

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SMA SOLAR TECHNOLOGY AMERICA, LLC,
Petitioner,
v.

TIGO ENERGY, INC.,
Patent Owner.

Patent 9,584,021
Filing Date: August 8, 2015
Issue Date: February 28, 2017
Title: SYSTEMS AND METHODS FOR ENHANCED EFFICIENCY
AUXILLARY POWER SUPPLY MODULE

Inter Partes Review No.: IPR2023-00879

Declaration of Douglas Holberg

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I. INTRODUCTION

- 1) I have been engaged by SMA Solar Technology America, LLC to opine on the patentability or otherwise of U.S. Patent No. US9584021 (—the '021 Patent), entitled —SYSTEMS AND METHODS FOR ENHANCED EFFICIENCY AUXILIARY POWER SUPPLY MODULE. My opinions are set forth herein. I submit this Declaration on behalf of SMA Solar Technology America, LLC in connection with its request for *inter partes* review of the '021 Patent.

A. Education and Relevant Experience

- 2) My education includes a B.S. in Electrical Engineering from Texas A&M University in 1977, followed by a M.S. in Electrical Engineering from the University of Texas at Austin in 1989. I earned a Ph.D. in Electrical Engineering from the University of Texas at Austin in 1992.
- 3) I have over 40 years of experience in the electronics field. During that time, I have worked for several different electronics companies including: Mostek, Texas Micro Engineering (acquired by Crystal Semiconductor), Crystal Semiconductor, Cirrus Logic, Cygnal Integrated Products, and Silicon Laboratories. I joined Silicon Laboratories when they acquired Cygnal, which I co-founded in 1999.
- 4) I am a named inventor on 43 U.S. granted patents. I have held a variety of engineering positions throughout my career, from circuit designer, design manager, Director of Engineering, Chief Technology Officer (CTO), Vice President (V.P.)

of Engineering, and V.P. of Technology. In addition to my engineering experience, I also have served as an adjunct faculty member at the University of Texas, where I taught CMOS analog and mixed-signal design for six years.

- 5) I am the co-author of the textbook —CMOS Analog Circuit Design, the first edition of which published 1987. As explained in the Preface of the second edition, published in 2002, the objective of the textbook is to teach the fundamentals and background that are necessary to understand how a —circuit works. It is now available in third edition and published in English and Chinese (first and second edition). This textbook is widely used throughout the world by new and experienced engineers in industry and by students in the classroom.
- 6) Upon graduating from Texas A&M University, I went to work for Mostek Corporation designing integrated circuits for telecommunications applications. I designed an integrated dual tone multi frequency (DTMF) generator. I received my first patent for this integrated DTMF generator. After leaving Mostek, I joined a startup company, Texas Micro Engineering, as the second employee. At Texas Micro Engineering, I designed, among other things, a dual-channel (atrium-ventricle) pacemaker sense amplifier/filter using discrete-time switched-capacitor technology.
- 7) While enrolled in the Masters/Ph.D. program at the University of Texas at Austin, I worked on the application of bipolar technology to dynamic random access

memory (DRAM) sense-amplifier architectures and circuit-simulation algorithms.

While at The University of Texas at Austin, I also designed and laid out the mask set (The Holberg Mask Set) still in use by the fabrication class/lab.

- 8) Upon graduating with a Ph.D. in Electrical Engineering, I went to work for Crystal Semiconductor/Cirrus Logic, where I designed high frequency synthesizers for hard-disk read-channel applications. I managed a group designing charge-coupled device (CCD) interface circuits for digital camera applications, as well as television encoder chips and CMOS imagers.
- 9) Upon leaving Cirrus, I started a company called Cygnal Integrated Products that developed mixed-signal microcontrollers. At Cygnal, I was the founder, CTO), V.P. of Engineering, and an individual contributor. While at Cygnal, I designed analog-to-digital converters (ADCs), V_{be} temperature sensors, input/output (I/O) cells/pads (both design and layout), as well as many additional miscellaneous circuits. My company was later purchased by Silicon Labs, where I remained employed as a manager of the microcontroller group, followed by the position of V.P. of Technology.
- 10) I have significant experience with the technology described in the '021 patent, including resistors, capacitors, diodes, inductors, transistors, transformers, oscillators, operational amplifiers, comparators, general integrated-circuit technology, analog/digital mixed-signal circuits, device analysis and modeling,

floor-planning, and layout of integrated circuits, and the tools used to design, and verify integrated circuits (CAD tools). In addition, I have experience with device modeling and characterization, which has been applied throughout my career.

- 11) My analyses set forth in this declaration are informed by my experience in the field of electrical engineering, including analog circuitry, ADCs, and digital circuits.

Based on my above-described experience, I believe that I am considered to be an expert in the field.

- 12) The '021 Patent is entitled —Systems and Methods for Enhanced Efficiency Auxiliary Power Supply Module. Prior to reviewing the '021 Patent, I was well familiar with the subject matter described and claimed therein. I am well familiar with circuits generally, such as disclosed in the '021 Patent.

B. Materials Considered

- 13) The analysis that I provide in this Declaration is based on my education and experience as an engineer, and upon my knowledge of CMOS integrated circuit design, as well as the documents I have considered, including the '021 Patent (Ex.1001). I have reviewed the prosecution history for the '021 Patent (Ex.1006).
- 14) I have reviewed various publications from the prior art at the time of the alleged invention of the '021 Patent. These publications, along with other materials I have reviewed, include those listed below:

- 15) Certified English Translation of German Publication DE3725476 (Mieth) (Ex. 1002).
- 16) U.S. Patent No. 6,246,592 (Balogh) (Ex. 1003).
- 17) U.S. Patent Publication No. 2005/105224 (Nishi) (Ex. 1004).
- 18) U.S. Patent No. 6,798,177 (Liu) (Ex. 1005).
- 19) File wrapper of U.S. Patent No. 9,584,021 (Ex. 1006).
- 20) Allen, Philip E., and Douglas R. Holberg. "CMOS Analog Circuit Design" (2002) ("CMOS") (Ex. 1009)
- 21) Solibro GmbH CIGS THIN FILM SOLAR MODULE SL2 ("Solibro") (Ex. 1010).
- 22) MITSUBISHI ELECTRIC PHOTOVOLTAIC MODULE ("ME") (Ex. 1011).
- 23) U.S. Patent Application No. 2007/0001653 (Xu) (Ex. 1012).
- 24) U.S. Patent Publication No. 2006/0207192 (Durham) (Ex. 1013).
- 25) Arias et al., "A Modular PV Regulator Based on Microcontroller with Maximum Power Point Tracking," IEEE, IAS 2004. (Ex. 1014).
U.S. Patent No. 4,617,529 (Suzuki) (Ex. 1015)

II. LEGAL PRINCIPLES USED IN MY ANALYSIS

- 26) I understand that in writing this Declaration I am obliged to follow existing applicable law. I have therefore been asked to apply the following legal principles to my analysis, and I have done so.

A. Person Having Ordinary Skill in the Art

- 27) I understand that my assessment of the claims of the '021 Patent must be undertaken from the perspective of what would have been known or understood by a person having ordinary skill in the art, reading the '021 Patent on its relevant filing date and in light of the specification and file history of that patent. I often refer to such a person as a —PHOSITA in this Declaration.
- 28) I am informed and understand that various factors can be considered in determining a person having ordinary skill in the art (PHOSITA). I am informed and understand that those factors include: (1) the educational level of the inventor(s);
- 29) (2) the type of problems encountered in the art; (3) prior art solutions to those problems; (4) the rapidity with which innovations are made; (5) sophistication of the technology; and (6) education level of active workers in the field.
- 30) I understand that SMA Solar Technology America, LLC proposed in the Petition that a person having ordinary skill in the art (—PHOSITA) in the field of the '021 Patent in 2009 would have a bachelor's degree in electrical engineering, or a similar discipline and at least two years of experience designing circuits.
- 31) I agree with this level of ordinary skill for the '021 Patent. Based on my experience, I understand and know of the capabilities of a person of this skill level as of the time the '021 Provisional Patent was filed. (i.e., the priority application to

which the '021 Patent claims its earliest priority) in 2009. I am familiar with how a PHOSITA would have understood and used the terminology found in the '021 Patent at the time of its filing, and with the state of the art at that time.

- 32) My analysis and opinions regarding the claims of the '021 Patent have been based on the perspective of a PHOSITA as defined above as of September 2, 2009, the filing date of the provisional application to which the application which later issued as the '021 Patent claimed priority. As described above and as shown in my CV, I have extensive experience in the field of electronics in the relevant timeframe.

B. The Prior Art

- 33) I understand that applicable patent law provides categories of information that constitute prior art that may be used to anticipate patent claims or to render them obvious. I understand that for a reference to qualify as prior art to a particular patent claim under the relevant law, that reference must have been made, known, used, published, or patented, or must have been the subject of a patent application by another person, before the priority date of the patent, and in this matter, must satisfy one of the standards of pre-AIA 35 U.S.C. § 102.

C. Claim Construction Standard

- 34) In making this Declaration, I have been asked to review the terms in the '021 Patent claims to determine what a PHOSITA would have understood those terms

to have meant at the time of the alleged invention. In addition, I have been informed that, in an *inter partes* review proceeding, the claim terms under consideration are to be construed using the same claim construction standard used in a civil action under 35 U.S.C. § 282(b), which is articulated in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc), and its progeny. I further understand that under the *Phillips* standard, the claim terms are given their ordinary and customary meaning, as would be understood by a PHOSITA at the time of the invention, consistent with the specification and the prosecution history. My opinions regarding the meaning of claim terms of the '021 Patent are based on the construction of the claim terms using the *Phillips* standard in view of the specification and the prosecution history of the '021 Patent.

D. Anticipation

- 35) I understand that to be valid, a patent claim must be —novel, and that a claim is invalid if it is —anticipated by a single prior art reference. I further understand that a reference anticipates if it discloses each and every element of the claim and enables a PHOSITA to make and use the claimed invention without undue experimentation.

E. Obviousness

- 36) I also understand that even if a claim of a patent is not anticipated, that claim is still invalid if the differences between the claimed subject matter and the prior art

are such that the subject matter as a whole would have been obvious to a PHOSITA at the time the invention was made.

- 37) I understand further that the condition “at the time the invention was made” in an obviousness determination is imposed to rule out impermissible hindsight.

Accordingly, permissible reasoning takes into account only knowledge which was within the level of ordinary skill in the art at the time the claimed invention was made and does not include knowledge gleaned from the applicant’s disclosure in the patent under analysis. I also understand that an opining expert is required to analyze prior art from the perspective of a PHOSITA and may not simply provide his or her own personal conclusions.

- 38) I also understand that an obviousness determination includes several factual inquiries, including: (1) determining the scope and content of the prior art;

- 39) (2) ascertaining the differences between the claimed invention and the prior art; (3) resolving the level of ordinary skill in the pertinent art; and (4) taking into consideration any secondary indicia (objective evidence) of non-obviousness.

- 40) I also understand that such objective evidence of non-obviousness may include: (1) a long felt but unsolved need that was satisfied by the claimed invention; (2) commercial success attributable to the claimed invention; (3) unexpected results achieved by the claimed invention; (4) praise by experts of the claimed invention

with factual support; (5) taking of licenses under the patent by others for reasons related to the alleged non-obviousness of the claimed invention;

- 41) (6) the failure of others; (7) the teaching away of others; (8) skepticism by experts; and (9) evidence that competitors in the marketplace have copied the invention instead of using the prior art. I also understand that, in order to establish non-obviousness, there must be a demonstrated relationship, or nexus, between any such secondary indicia and the claimed invention, i.e., there must be objective evidence of non-obviousness attributable to the claimed invention.
- 42) I further understand that near simultaneous invention by two or more equally talented inventors working independently may or may not be an indication of obviousness when considered in light of all the circumstances.
- 43) I understand that a conclusion of obviousness can be based on a combination of multiple prior art references. I understand that rationales that may support a conclusion of obviousness include:
- (A) Combining prior art elements according to known methods to yield predictable results;
 - (B) Simply substituting one known element for another to obtain predictable results;
 - (C) Using known techniques to improve similar devices (methods, or products) in the same way;

(D) Applying a known technique to a known device (method, or product) ready for improvement to yield predictable results;

(E) Using an —obvious to try solution, i.e., choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success;

(F) Applying known work in one field of endeavor to yield variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations are predictable to one of ordinary skill in the art;

(G) Applying some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference disclosures to arrive at the claimed invention.

44) I further understand that an analysis of obviousness should recognize that market demand, rather than scientific literature, often drives design trends.

45) I also understand that if a technique has been used to improve one device, and if a PHOSITA would recognize the technique would improve similar devices in the same way, then using that technique would be obvious to a PHOSITA unless actual application of that technique is beyond his or her skill.

46) I also understand that practical and common-sense considerations should guide an analysis of obviousness, because familiar items may have obvious uses beyond their primary purposes. I further understand that applying common sense does not require a —specific hint or suggestion in a particular reference. Rather, applying

common sense requires a reasoned explanation that avoids conclusory generalizations and false deductions.

- 47) I also understand that, when addressing a problem, a PHOSITA will often be able to fit together the disclosures of multiple publications. In this regard, I understand that an analysis of obviousness may consider inferences and creative steps that a PHOSITA would normally employ.
- 48) I also understand that a particular combination of prior art may be proven obvious merely by showing that it was obvious for a PHOSITA to try that combination. For example, when there is a design need or a market pressure to solve a problem, and/or there exists a finite number of identified, predictable solutions with a reasonable expectation of success, a PHOSITA has good reason to pursue the known options within his or her technical grasp. I understand that if this leads to anticipated success, it is likely that the result is not of innovation but of ordinary skill and common sense.
- 49) I also understand that a combination of familiar elements according to known methods is presumed to be obvious when that combination does no more than yield predictable results. Work known in one field of endeavor may prompt variations of that work for use in either the same field or a different field, based on design incentives and other market forces. If a technique has been used to improve some

device, and a PHOSITA can implement a predictable variation of that technique, then that variation is likely unpatentable.

- 50) I further understand that to be proper for use in an analysis of obviousness, a reference must teach art that is analogous to the claimed invention. I also understand that under a correct analysis, any need or problem known in the field of endeavor at the time of the invention and addressed by the claimed invention can provide a reason for combining the elements in the manner claimed.
- 51) I understand that a claim can be obvious in light of a single reference, without the need to combine references, if the elements of the claim that are not found explicitly or inherently in that single reference can be supplied by the common sense or technical knowledge of a PHOSITA. For example, combining two embodiments disclosed adjacent to each other in a prior art patent likely does not require a leap of inventiveness.
- 52) I also understand that a claimed invention may be obvious if it merely involves simple substitution of one known element for another to obtain predictable results.
- 53) I understand further that, in an analysis of obviousness, two items of prior art need not be like two puzzle pieces that must fit together perfectly. For example, a claimed invention may be found obvious if a PHOSITA would view rearrangement as an obvious matter of design choice.

54) I also understand that an analysis of obviousness requires a comparison between the properly construed claim language and the prior art on a limitation-by-limitation basis.

III. BACKGROUND OF THE TECHNOLOGY

55) Comparators are a widely used component that detects and indicates the relationship between its two inputs. A symbol for a comparator is shown in Fig. 1 below, but can be illustrated in other ways as well.

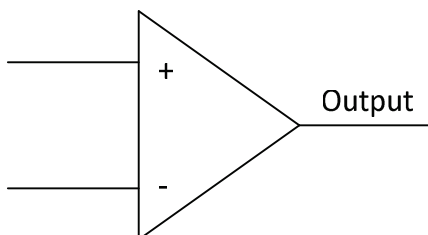


Fig. 1

56) The inputs are characterized as the positive input and the negative input. Sometimes also referred to as the non-inverting and inverting inputs, respectively. A comparator generally has, but is not limited to, a single output that indicates the relationship between the input signals at the positive and negative inputs. If the positive input is greater than the negative input, then the output of the comparator will be high. Alternatively, if the positive input is less than the negative input, then the output of the comparator is low. Theoretically for an ideal comparator, if the inputs are equal, the output is indeterminate. The ideal transfer curve for a comparator is shown in Fig. 2 below. (Ex. 1009, Fig 8.1-4).

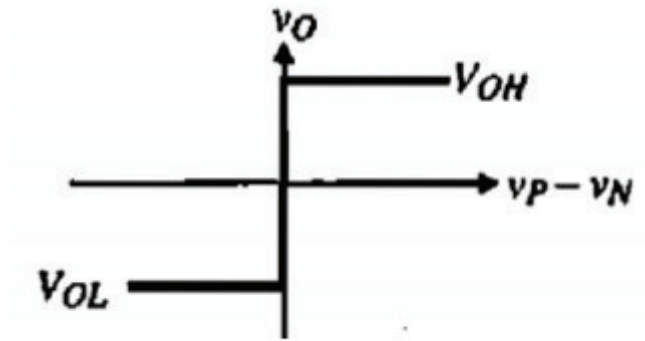


Fig. 2

57) Comparators, like all electronic devices, are subject to noise—both internal and external noise. When comparators are intrinsically noisy, or are placed in a noisy environment they can “chatter” when the input is close to the switching threshold (comparator threshold) (Ex. 1009, 462). This is illustrated in Fig. 3 below. (Ex. 1009, Fig 8.4-6a).

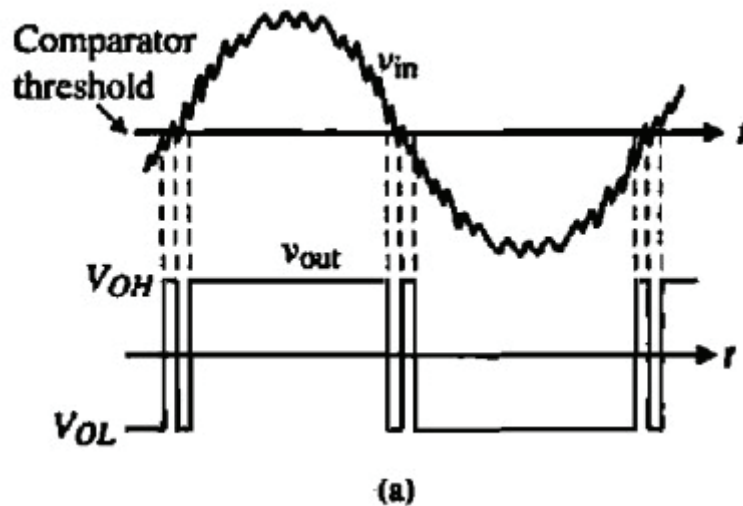


Fig. 3

58) As seen in Fig. 3, due to the noise on v_{in} (the positive input terminal of the comparator), at the comparator threshold, the noise of the signal bounces above and below the threshold, causing the signal at the output (v_{OUT}) to switch quickly or “chatter” between V_{OH} and V_{OL} , in some instances, multiple times depending upon the frequency of the noise on the input signal. One of the methods to avoid this “chatter” on a comparator output is to add hysteresis to the transfer function curve of the comparator. To add hysteresis, the trip threshold of the comparator is varied based on the state of the comparator. This can be understood as follows. When the input signal to the comparator is rising, the state of the comparator does not change until the input signal reaches a positive trip point threshold (V_{TRP}^+ as shown in Fig. 4 below). Once the state has changed due to the input signal exceeding the threshold, the trip-point threshold is reduced to a negative trip point so that the state of the comparator output does not change until the input signal falls below the negative trip point (V_{TRP}^- as shown in Fig. 4 below). This is illustrated in Fig. 4 below (Ex. 1009, Fig. 8.4-5).

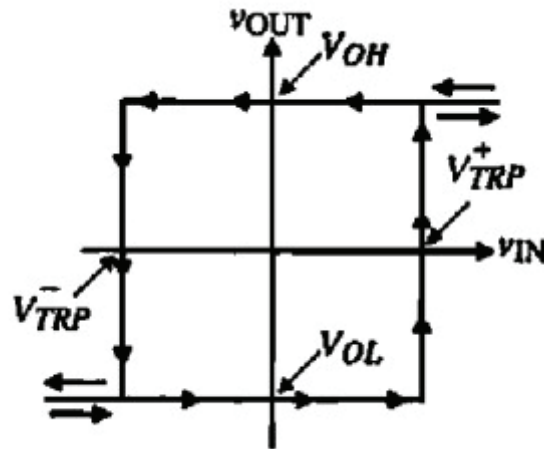


Fig. 4

- 59) As shown, the input signal, v_{IN} , starting from the left is low causing v_{OUT} to be low (V_{OL} or the “first state”). As v_{IN} increases to the right, a positive trip point is reached, V_{TRP}^+ . At that point v_{OUT} goes high (V_{OH} or the “second state”). v_{IN} can continue increasing with no change in state. As v_{IN} starts decreasing, the output, v_{OUT} , remains high (second state) until it reaches a negative trip point threshold V_{TRP}^- (which is lower than the initial positive trip point V_{TRP}^+) causing the comparator output, v_{OUT} , to go low (first state).
- 60) Once hysteresis is introduced to the comparator, the “chatter” effect is removed as long as the noise amplitude on the signal is less than the difference of the positive and negative trip voltages (i.e., keeping the noise less than the hysteresis “window”). This is illustrated in Fig. 5 below (Ex. 1009, Fig. 8.4-6b) where the “chatter” on the output signal of the comparator no longer exists.

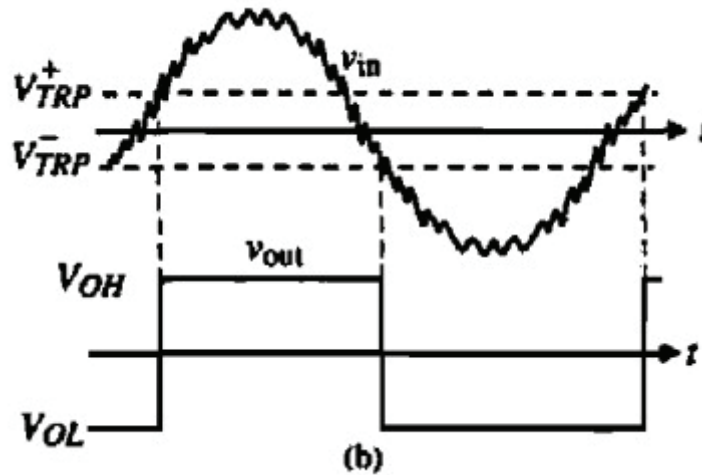


Fig. 5

- 61) When the signals at the positive and negative inputs cross (e.g., when the positive input becomes greater than the negative input), the state of the comparator output changes (e.g., goes from a low state to a high state in this case). This transition does not happen instantaneously—there is some intrinsic delay. This delay is generally referred to as propagation delay as illustrated in Fig. 6 below (Ex. 1009, Fig. 8.1-9). In fact, nothing in real-world circuitry happens instantaneously, i.e., without delay.

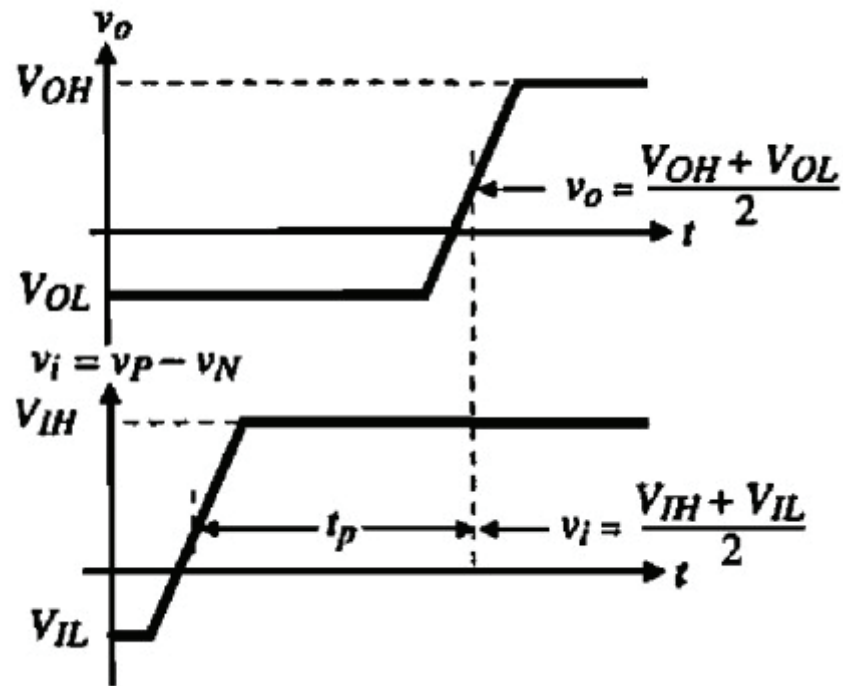


Fig. 6

- 62) As can be seen in the figure, if the midpoint of the transition is taken as the reference point between the low state and high state of both the input signal and the output signal, respectively, it is clear that a delay of t_p represents the time delay between the transition at the comparator input and the corresponding signal transition at the comparator output. This delay, t_p , represents a delay associated with the various internal circuitry of the comparator to effectuate the corresponding signal transition at the output in response to the transition at the comparator input.

IV. OVERVIEW OF THE '021 PATENT

A. Brief Description

63) The '021 patent is directed to a power supply for use in a solar electric production system. Ex.1001, 1:50-51. One embodiment illustrating various features of the '021 patent is shown in Fig. 4 of the patent, but labeled as Fig. 7 herein. The power supply has a first stage 401 and a second stage 402. The term stage is not explicitly defined in the '021 patent, but a "stage" is a term sometimes employed to describe some group of one or more circuit elements that operate to provide a circuit function. In one example of the '021 patent the first stage 401 comprises a group of circuit elements that form a first power converter that receives an input voltage from a photovoltaic ("PV") panel and outputs a first voltage at a first output. The second stage 402 is connected to the first stage 401 and in one example comprises a second power converter. Ex.1001, 1:51-56. The second stage 402 operates in two states: (1) a first, deactivated state, and (2) a second, enabled state. In the second state, the second stage 402 generates a second voltage at a second output using the first voltage received from the first stage to supply a micro-controller with a voltage. Ex.1001, 8:41-48.

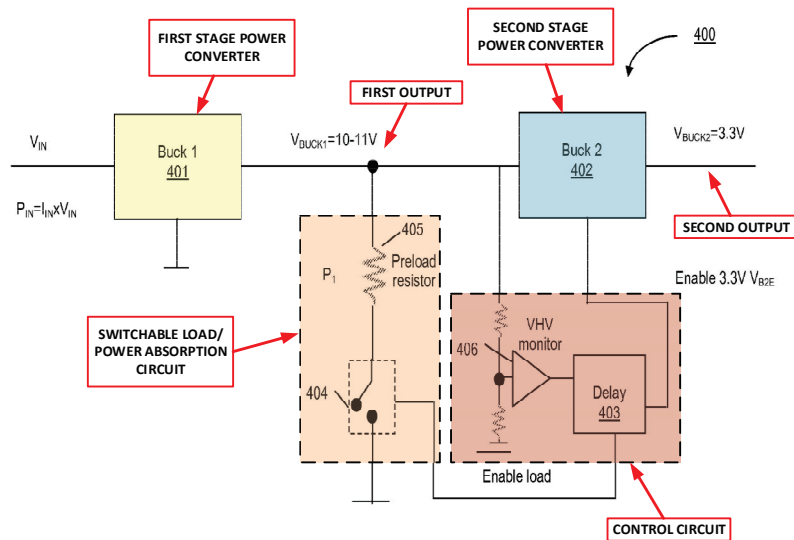


Figure 4

Fig. 7

- 64) The power supply includes a control circuit (406, 403) to prevent false start problems when the solar panel is providing insufficient power. Ex.1001, 8:19-22.
- The control circuit, in the first state, connects a preload resistor 405 to the first output by closing a switch 404 via a first control signal to emulate the load of the second stage 402 on the first stage output prior to activating the second stage 402 via a second control signal. Ex.1001, 8:22-23, 8:35-37. If the first stage output voltage exceeds a threshold, the control circuit, in the second state, disconnects the preload resistor 405 by opening the switch 404 via the first control signal. Ex.1001, 8:41-45. The control circuit employs a delay 403 to delay the second control signal with respect to the first control signal to ensure the second stage operation remains suppressed (*i.e.*, not enabled) until after the switch 404 is opened, thus providing a

“break before make condition,” wherein the switch 404 opens (*i.e.*, “breaks”, switches out the preload resistor 405) before the second stage 402 is enabled (*i.e.*, “makes” the second stage 402 receive power via the second control signal).

Ex.1001, 8:40-48.

- 65) In another embodiment, a capacitor is connected to the input of the second stage 402, in a manner similar to capacitor 326 and second stage 311 in Figure 3 of the ‘021 patent in Fig. 8 shown below. Ex.1001, 9:32-34.

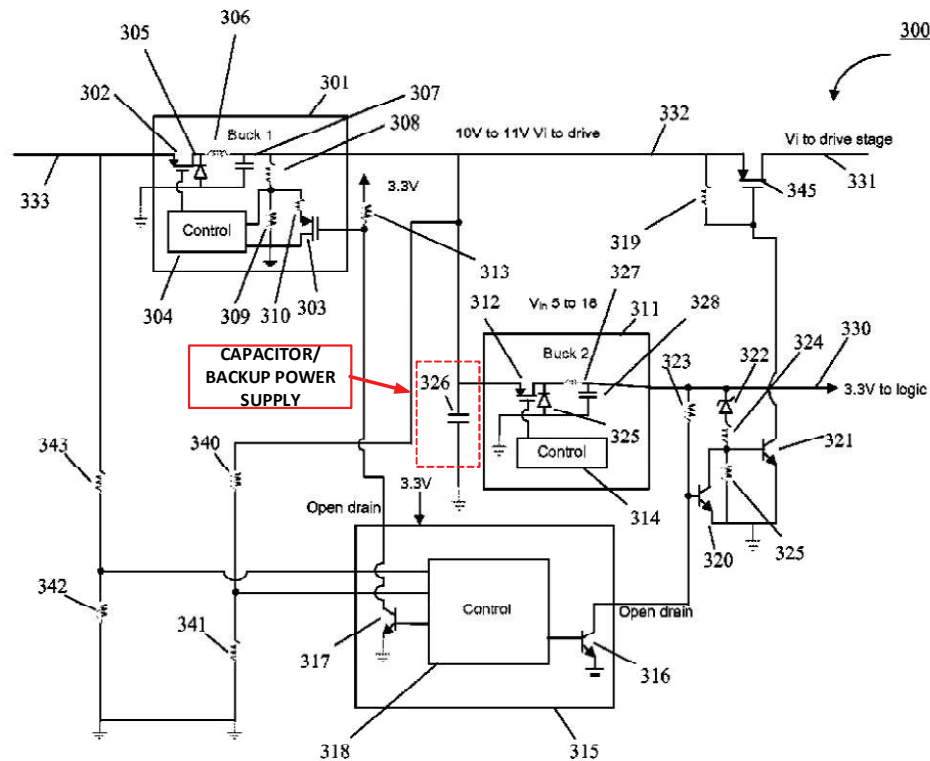


Fig. 8

- 66) Such a capacitor is employed as a backup power supply to keep the second stage 402 running longer than the first stage 401. Ex.1001, 4:51-60. Thus, in the first state, the capacitor 326 is charged and absorbs power from the first stage 401, and

when the first stage 401 is inoperative or unstable, the capacitor provides charge to keep the second stage 402 working to provide the second voltage at the second output. Ex.1001, 4:60-66.

B. Earliest Priority Date for the Claims

67) The earliest claimed priority date for the '021 patent claims, by the applicant, is the filing date of the U.S. provisional application—filed September 2, 2009. At least the first provisional application filed in 2009, and arguably the second provisional filed in 2010, does not provide support under 35 U.S.C. §112, first paragraph, for the claimed subject matter. I do not rely on any prior art that is intervening art published in the time period between the provisional application filing dates and the non-provisional filing date of May 25, 2010. Each reference discussed herein predates the filing date of this U.S. provisional priority application and constitutes available prior art under 35 U.S.C. § 311(b).

V. OVERVIEW OF PRIOR ART

A. DE3725476 (Mieth) (Ex.1002)

68) Mieth discloses a circuit and associated method that supplies power to an electrical load from a solar generator. See Fig. 9 below. Ex.1002, 8:8-9, Fig. 1.

69) For electrical energy sources that exhibit variability in performance, such as a solar converter (due to the time of day or weather conditions), depending on the power provided by the energy source, the circuit arrangement operates in two different

states. Ex.1002, 1:23-28; 5:22-27. In a first state, at lower source voltages, a preliminary load is switched “in” to the circuit, while a downstream auxiliary power supply circuit is disabled. In a second state, at higher source voltages, the preliminary load is switched “out” of the circuit arrangement, and the energy source is connected to the auxiliary power supply circuit (e.g., power supply apparatus 19). *Id.* 1:28-34; claim 1, 2:10-34.

- 70) Fig. 9 provided below shows the solar generator 1 that provides a direct current to a first stage capacitor 2 that provides a first voltage at a first output.

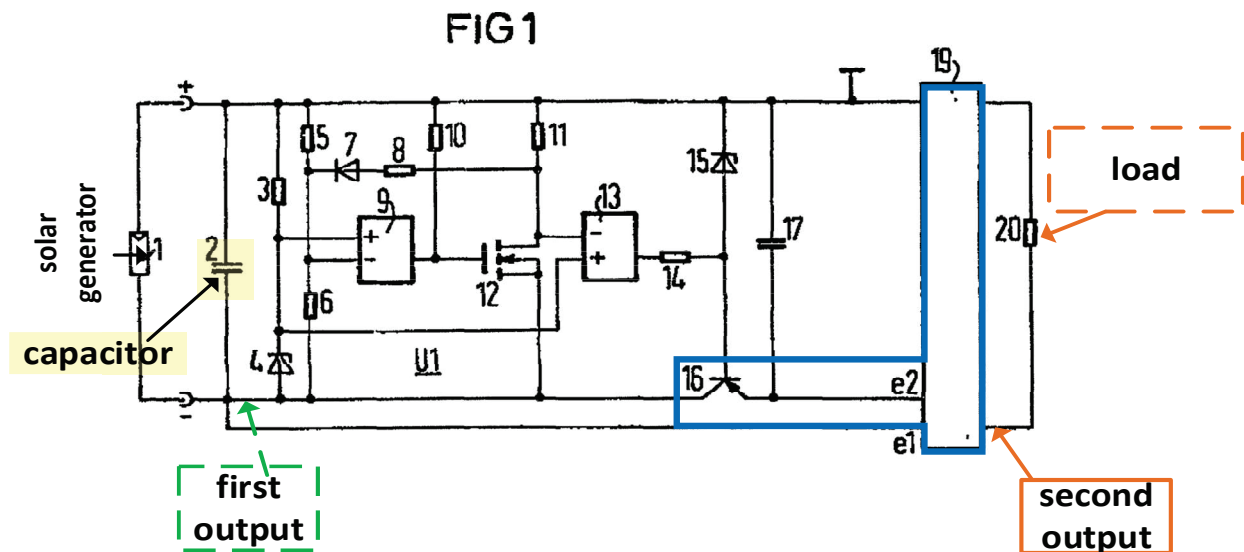


Fig. 9

- 71) The circuit arrangement includes two comparators, a first comparator 9, and a second comparator 13 that operate in one of two states. In the first state, at low voltages, the first comparator 9 switches “in” the preliminary load, while the state

of the second comparator 13 results in the power supply apparatus 19 being disabled. *Id.* 6:14-23; 9:15-32.

- 72) Fig. 10 highlights the first state at low input voltages, where first comparator 9 is “high” and preliminary switchable load 11 (i.e., resistor 11), is switched “in” due to transistor 12 being “on” (i.e., conducting).

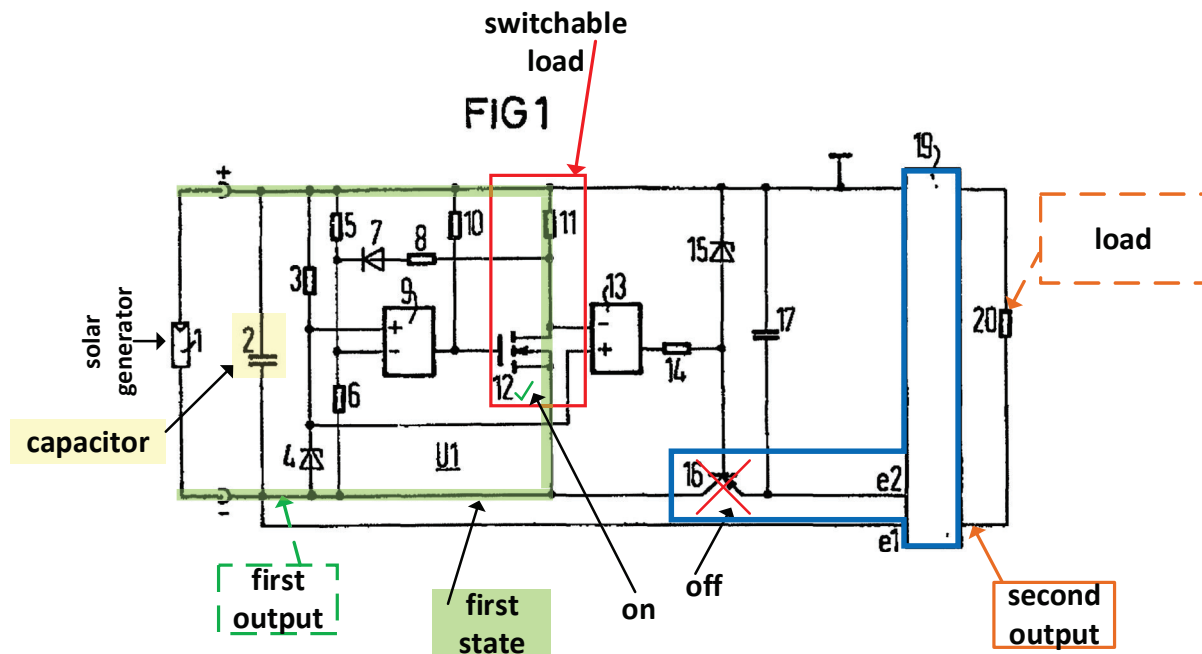


Fig. 10

- 73) Further, in the first state, second comparator 13 output is “high”, causing the pnp bipolar transistor 16 to be “off” (i.e., non-conducting), and power supply apparatus 19 to be disabled. *Id.* 12:12-19.
- 74) Fig. 11 illustrates the second state when power provided by solar generator 1 is high, and thus first voltage at the first output is low (relative to the positive terminal of the PV). With lower input voltages (relative to the positive terminal of

the PV), the voltage at the negative input of first comparator 9 exceeds the reference voltage at the positive input terminal, causing the first comparator output to transition “low” and turning off transistor 12 (i.e., “switching out” switchable load, resistor 11).

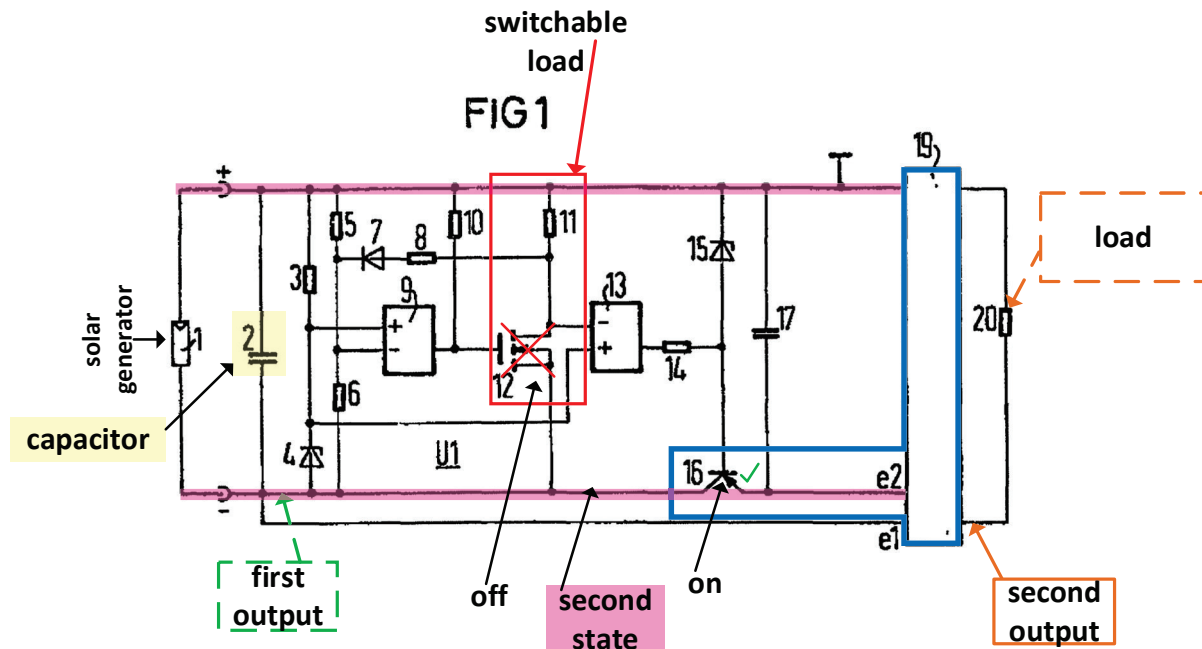


Fig. 11

75) With transistor 12 off, the negative input of second comparator 13 gets pulled high, causing second comparator 13 output to go “low,” turning on transistor 16. *Id.*

12:21-30. With transistor 16 conducting, the first output is passed to the e2 input of auxiliary power converter 19, enabling such circuitry, which provides the second output to load 20. *Id.* 9:15-32. Auxiliary power converter 19 is also connected to solar generator 1 via supply voltage input e1. Ex.1002 8:29-35. Mieth does not discuss the function of supply voltage input e1, a PHOSITA would understand that

supply voltage input e1 may provide additional functionality to the circuit of Mieth, perhaps, for a product or particular implementation that is extraneous to the detailed description.

- 76) In addition, Mieth discloses a “break before make” operation between the first and second states, wherein an exit from the first state (preliminary load 11 is “switched in”) is concluded before the second state (where auxiliary power converter 19 is enabled) is initiated. This “break before make” operability is facilitated by the cascaded first and second comparators 9 and 13. When the first voltage at the first output goes low (relative to the positive terminal of the PV), first comparator 9 output changes state to turn off the transistor 12. Only after transistor 12 stops conducting does second comparator 13 output transition from “high” to “low” in order to activate the transistor 16. Thus when transistor 12 shuts off, the voltage at the negative input terminal of second comparator 13 rises and exceeds the reference voltage at the positive input terminal, causing output of the second comparator 13 to transition low. Transistor 16 is a pnp-type transistor, and is activated or turned “on” when the voltage at its base terminal that connects to the output of the second comparator 13 is low. Because comparator 9 must change state before the output of transistor 12 (the negative input of comparator 13) changes state and comparator 13 changes state only after the negative input changes state, there is an intrinsic delay built into the cascaded comparator

arrangement to ensure that the first control signal that disables preliminary load 11 always occurs before the second control signal that enables power supply apparatus 19. Thus, Mieth teaches a delay between first and second control signals.

- 77) Mieth includes a hysteresis circuit comprising comparator 9, voltage divider resistors 5, 6, 8, 11, and diode 7. *Id.* 12:21-30. The hysteresis function is provided by the positive feedback via resistor 8 and diode 7. *Id.* Using the nomenclature shown in the Fig. 12 below, Mieth's hysteresis will be analyzed.

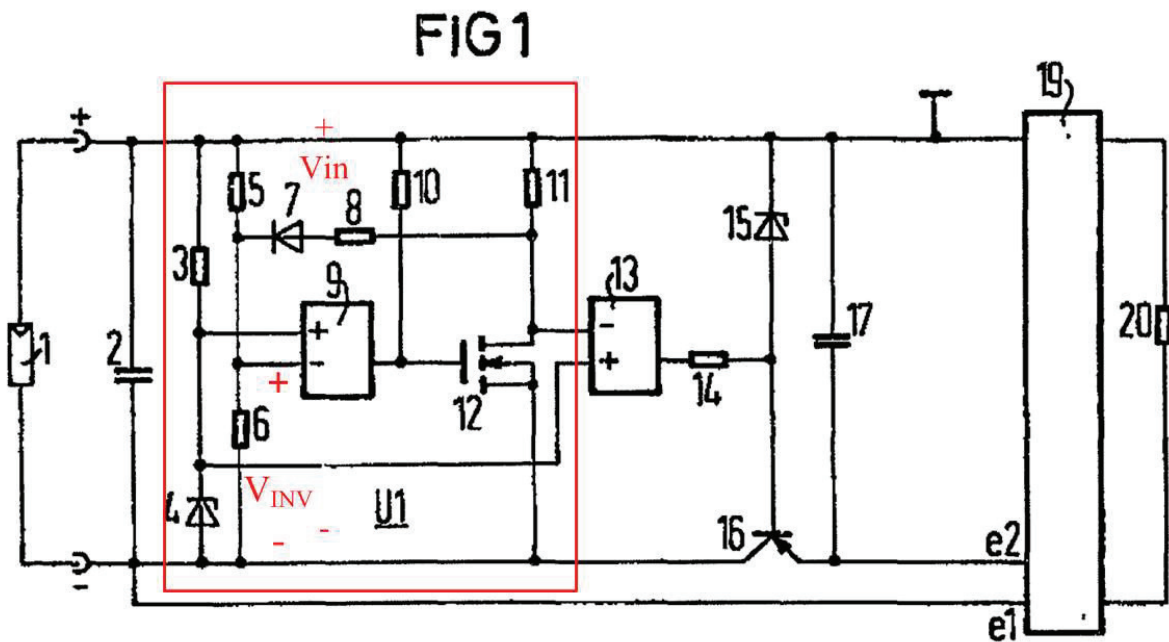


Fig. 12

- 78) Mieth incorporates a diode in the hysteresis circuit so that the hysteresis feedback is applied in only one state (when the output of comparator 9 is low causing drain of transistor 12 to be high). Thus, in the first state where $V_{in} \frac{R_6}{R_5 + R_6} < V_{ZENER}$, the drain of transistor 12 is low, so diode 7 does not conduct. When V_{in} increases so

that when $V_{in} \frac{R6}{R5 + R6} > V_{ZENER}$, the output of the comparator goes low and the drain of transistor 12 goes high so that diode 7 is conducting and as a result changes the voltage at the inverting input of comparator 9 to:

$$\frac{V_{in} \left(\frac{R6}{R5} + \frac{R6}{R8 + R11} \right) - V_{DIODE} \frac{R6}{R8 + R11}}{1 + \frac{R6}{R5} + \frac{R6}{R8 + R11}} = V_{INV}$$

79) Ignoring the forward voltage of the diode (setting $V_{DIODE} = 0$) this expression simplifies to:

$$V_{in} \frac{R6}{R_{EQ} + R6} = V_{INV}$$

where:

$$R_{EQ} = \frac{R5(R8 + R11)}{R5 + R8 + R11} = V_{INV}$$

80) Thus there are two thresholds. The upper threshold (magnitude) is given by:

$$V_{in} = \frac{R5 + R6}{R6} V_{ZENER}$$

81) and the lower threshold (magnitude) given by:

$$V_{in} = \frac{R_{EQ} + R6}{R6} V_{ZENER}$$

82) The hysteresis curve resulting from this circuit arrangement is shown in Fig. 13 below.

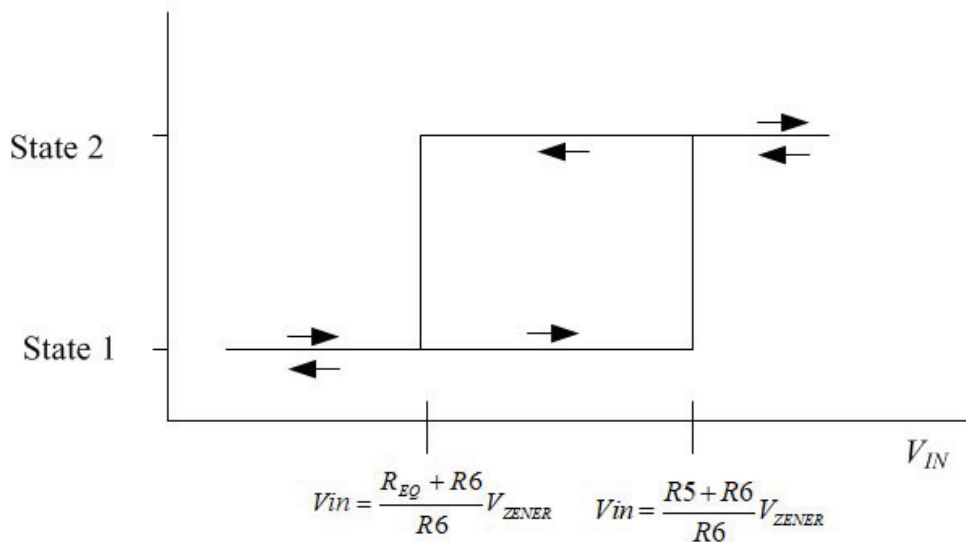


Fig. 13

B. U.S. Patent No. 6,246,592 (Balogh) (Ex.1003)

83) Balogh is a United States patent that issued on June 12, 2001. Balogh discloses that cascaded power converter arrangements that include two or more power converters are well known. Ex.1003, 1:21-22. Balogh further discloses that cascaded converters are commonly used to provide large input to output voltage conversion ratios (step-up or step-down). *Id.* 1:25-28. Solar power applications often employ individual modules with voltages as high as 75-80V under some operation conditions, and as low as 10V in other instances, while still providing enough power to operate a load such as a microcontroller. Ex. 1010; Ex. 1011. Consequently solar power applications including cascaded power converter systems having large input to output voltage conversion ratios can be advantageous.

- 84) It is well known in the art that improved efficiency can be achieved by cascading buck converters when there is a large ratio of input to output voltage as described in Patent application: US 2007/0001653 (hereafter “Xu”). Ex. 1012. Xu states: “The present invention provides a two-stage power delivery system that employs cascaded buck stages. For high input-to-output voltage ratios, each cascaded buck stage has a more suitable (i.e., larger) duty cycle that results in a much lower total power loss than in a single-stage buck.” Ex. 1012, ¶6. Xu teaches using cascaded buck converters where the input is in the range from 6 to 24 volts and an output voltage on the order of 1 volt. *Id.* ¶18. Thus, as will be discussed in greater detail *infra*, Xu provides a teaching that a PHOSITA would readily consider a cascaded converter arrangement in various solar applications, such as the application taught in Mieth.
- 85) Balogh discloses multiple cascaded buck converter arrangements in prior art Figs.1B-1D, respectively. One example of a conventional, cascaded converter arrangement provided in Fig. 1D thereof is illustrated in Fig. 14 below.

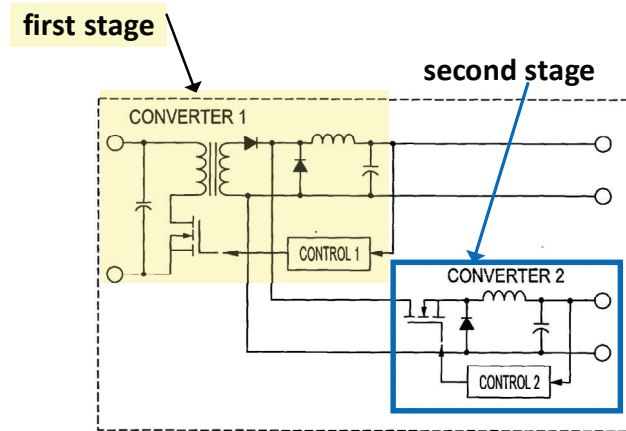


FIG. 1D
PRIOR ART

Fig. 14

- 86) In Fig. 14, an isolated DC-DC converter (converter 1) feeds a post regulator circuit (converter 2) to form first and second buck converter stages, respectively. In one example, the first converter is a transformer-coupled input power converter that steps down the input voltage to an intermediate voltage. Ex.1003, 1:61-66; 3:8-13. The second converter is a buck power converter. *Id.*, 1:62-63.

C. U.S. Patent Publication No. 2005/105224 (Nishi) (Ex.1004)

- 87) Nishi is a United States published patent application that published on May 19, 2005.
- 88) Figs. 2 and 7 of Nishi provided collectively in Fig. 15 below each show functional block diagrams of a photovoltaic power generation system. Each system shows an inverter apparatus 4 and 110 that includes both inverter circuitry (6 in Fig.2, 102 in Fig.7) and a micro-computer 109 that includes control circuitry 105, as discussed

inverter circuitry 6 to a specified range. *Id.*, ¶88. In doing so, each converter 5A-5D in Fig. 2 that feeds inverter circuitry 6 is controlled by the inverter micro-computer (i.e., control unit 11A-11D) to output a constant voltage. The control units 11A-11D control an operating point of an input voltage of each converter to maximize the output power from corresponding solar cells 2A-2D. *Id.*, ¶97.

D. U.S. Patent No. 6,798,177 (Liu) (Ex.1005)

- 90) Liu is a United States patent that published on September 28, 2004. Liu discloses a multi-stage converter circuit that employs a storage capacitor in between, and in parallel with, the two converter stages. As shown in Fig. 16 below (which corresponds to Fig. 5 of Liu), the multi-stage converter circuit includes an input stage 50, a storage or reservoir capacitor 58, and output stage 60. Output stage 60 connects to a power amplifier (“PA”) 68. Ex.1005, Fig.5, 4:25-28.

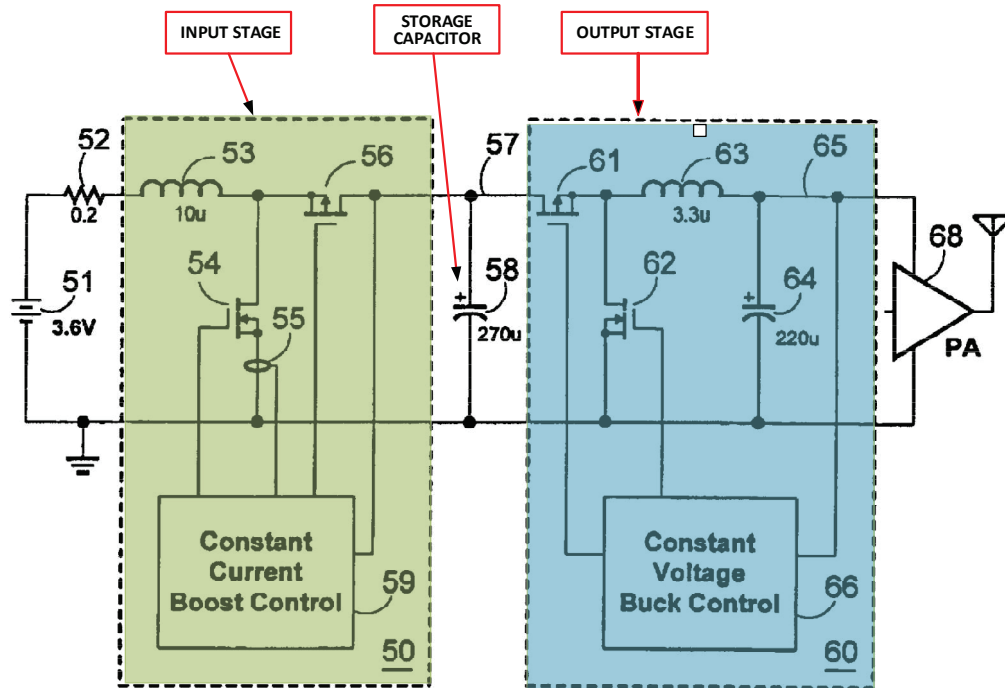


FIG. 5

Fig. 16

91) The input stage 50 operates to charge the storage capacitor 58 and thus increase the voltage across the capacitor. The output stage 60 operates to down-convert the voltage on the reservoir capacitor 58 to an output voltage, for example, 3.4V, needed by the PA 68, which the output stage 60 regulates. *Id.*, 4:36-50 During operation the storage or reservoir capacitor 58 supplies energy to the PA 68, such that if the input stage 50 ceases operating, the output stage continues powering the PA 68 for some further period of time. *Id.*

VI. SUMMARY OF ARGUMENT

- 92) The '021 patent claims a method and circuit arrangement related to an auxiliary power supply. As I will show, it is my opinion that the prior art discloses this sort of supply circuitry. As explained herein, Mieth teaches most elements of the '021 patent's independent claims. For independent claim elements arguably not taught by Mieth, Balogh teaches first stage features and cascaded first and second stages such as step-down power converters. Further, it is my view that a combination of Mieth and Balogh is proper as a PHOSITA would be motivated to make the combination.
- 93) In addition, Nishi teaches a micro-controller as a load, and Liu discloses a capacitor as a power absorption circuit between cascaded power converters. Adding these features to Mieth's system would have been obvious, and yields the alleged invention claimed in the '021 patent. Consequently, the alleged invention would have been obvious at least because a PHOSITA would have been motivated to combine Balogh, Nishi, and Liu with Mieth's system. *See* ¶¶ 152-157; 283-288; 301-303, *infra*.
- 94) In sum, as demonstrated by a preponderance of the evidence, including this prior art, the '021 patent claims are unpatentable as being anticipated and/or obvious in view of the cited prior art.

VII. SPECIFIC GROUNDS FOR UNPATENTABILITY

A. Ground A: Anticipation of claims 1-7, and 9 in view of Mieth

1. Independent Claim 1

95) With reference to the claim listing appendix, Mieth discloses Elements [1A]-[1G], that is, the alleged inventive features of claim 1.

i. [1A]: “A method to supply power”

96) Mieth (Ex.1002) discloses a circuit that supplies power to an electrical load from a solar generator. Ex.1002 (Mieth), 8:8-9. A PHOSITA understands that when the circuit of Mieth supplies power to the electrical load, the circuit is performing a method to supply power to the electrical load. Thus, Mieth teaches [1A].

ii. [1B]: “the method comprising: providing a power supply having a first stage and a second stage,”

97) Mieth discloses a *power supply* as shown below in Fig. 17. Mieth discloses a capacitor 2 (yellow) in parallel with the solar generator 1, and a power supply apparatus 19 connected to a bipolar transistor 16 (blue). Ex.1002, 9:5-9, 11:14-16. The capacitor 2 is analogous to the *first stage* and the power supply apparatus 19 connected to transistor 16 is analogous to the *second stage* of the claimed power supply.

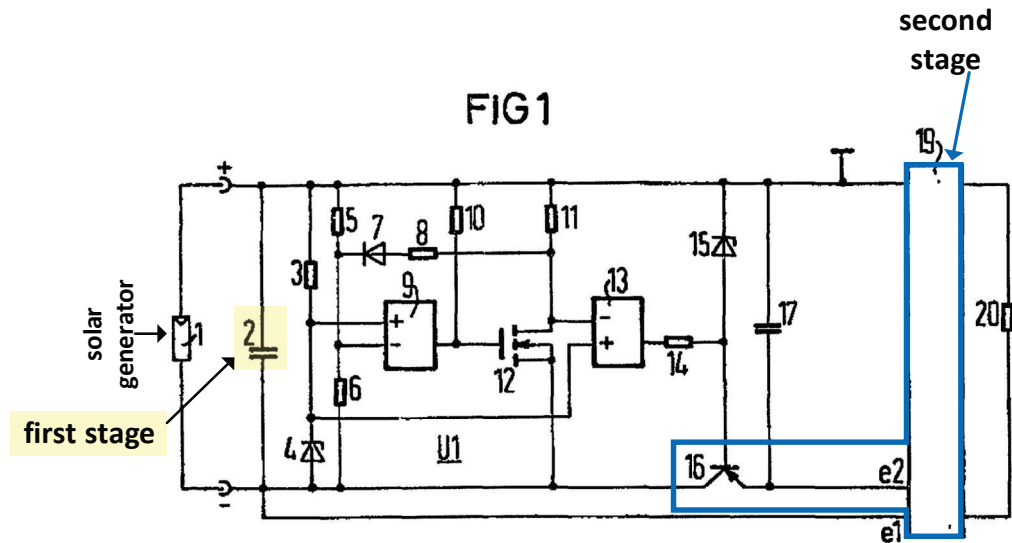


Fig. 17

98) A PHOSITA would understand a “stage” to refer to a generic portion of an electrical circuit. Not only have I used the term “stage” to refer to one or more circuit components that provide a specified function when working as a circuit design engineer, this is a common term of art in the field of electronics, and is employed in this manner. For example, Nishi (Ex. 1004), which predates the ‘021 patent, similarly makes use of the phrase “stage” to refer to a general circuit component. Nishi references a “front stage” of an inverter apparatus 10 when discussing a booster chopper 206 that receives DC power. As such, the “front stage” refers to the input portion of the circuit for the inverter apparatus. Ex. 1004, ¶¶31-34. Additionally, Liu, which predates the ‘021 patent, similarly makes use of the phrase “stage” to refer to one or more circuit components. For example, Liu

refers to “[a] power converter including a **first stage**,... and a **second stage**,” and generally refers to the second stage as a voltage converter. Ex. 1005: Abstract.

99) At the time of filing, the ‘021 patent does not define what a stage is and refers to portions of circuits generally with the term stage. For example, the ‘021 patent refers to a first stage having an input connected to a photovoltaic panel and output that provides a voltage from the photovoltaic panel, and a second stage that supplies power. Ex. 1001, 1:49-55. The ‘021 patent further generally makes use of the word “stage” to a “drive stage output 331” of a MOSFET 345. Ex. 1001, 6:11-15. As such, the ‘021 patent assumes the reader understands what a “stage” is in relation to circuits, and uses the phrase to generally relate to portions of an electrical circuit with particular functionality. Thus, based on the plain, ordinary meaning of the term, common usage in the art, and a consistent usage of the term in the detailed description of the ‘021 patent, the term “stage” is used to generally refer to one or more circuit components that operate alone or together to provide a specified function.

100) Thus, in my opinion, it is clear that at the time of the invention, that in the art prior to the ‘021 patent, “stage” referred to one or more general circuit components that could be the input (*e.g.*, front stage of Nishi) to a device in a circuit (*e.g.*, the inverter apparatus of Nishi), or a power converter (*e.g.*, second stage of Liu). Similarly, the power supply apparatus 19 connected to transistor 16 of Mieth,

which is a circuit component and acts as a power converter similar to the second stage of Liu, can be referred to as a “stage” and thus is analogous to the *second stage* of [1B].

101) Thus, Mieth teaches [1B]. Additionally, the combination of Mieth and Balogh teach the features of [1B] as discussed in further detail in ¶¶ 151-161.

iii. [1C]: “wherein the first stage converts power from a direct current input into a first output,”

102) As a PHOSITA, I understand that solar generators generate a direct current. For example, U.S. Patent Publication No. 2006/0207192 (Durham) states, “[t]he photovoltaic device may be any suitable photovoltaic device or material known in the art for converting light energy into electrical current.” Ex. 1013, ¶21.

103) As such, the solar generator 1 of Mieth supplies the *direct current input* (dashed-red) to the capacitor 2 as shown in Fig. 18 below. Ex.1002 Fig. 1. The first stage of Mieth is a parallel capacitor 2 which I, as a PHOSITA, understand converts power associated with the direct current input into a *first output* (dashed-green), as required by this element of claim 1. A PHOSITA would understand how a capacitor works in that the voltage across a capacitor is proportional to the integral of the current through the capacitor. Thus capacitor 2 of Mieth can stabilize the voltage across it (at the first output) due to fluctuations from the direct current input.

105) As a PHOSITA, I understand that a load in a circuit can include a micro-controller, as such, the load 20 is analogous to the claimed *micro-controller* (dashed-orange). Since the introduction of the Intel 8051 circa 1980, the micro-controller has become ubiquitous in electronic systems. When these devices are powered, invariably, the raw power source is the ac mains, a battery or some other unregulated source that must be reduced and stabilized. Thus it is commonplace for a micro-controller to load the output of a voltage regulator whether it is a linear regulator or a switch-mode regulator. For example, Arias et al. illustrates a PV system with a buck converter powering a microcontroller operating as a load. Ex. 1014, 1180; Fig. 5.

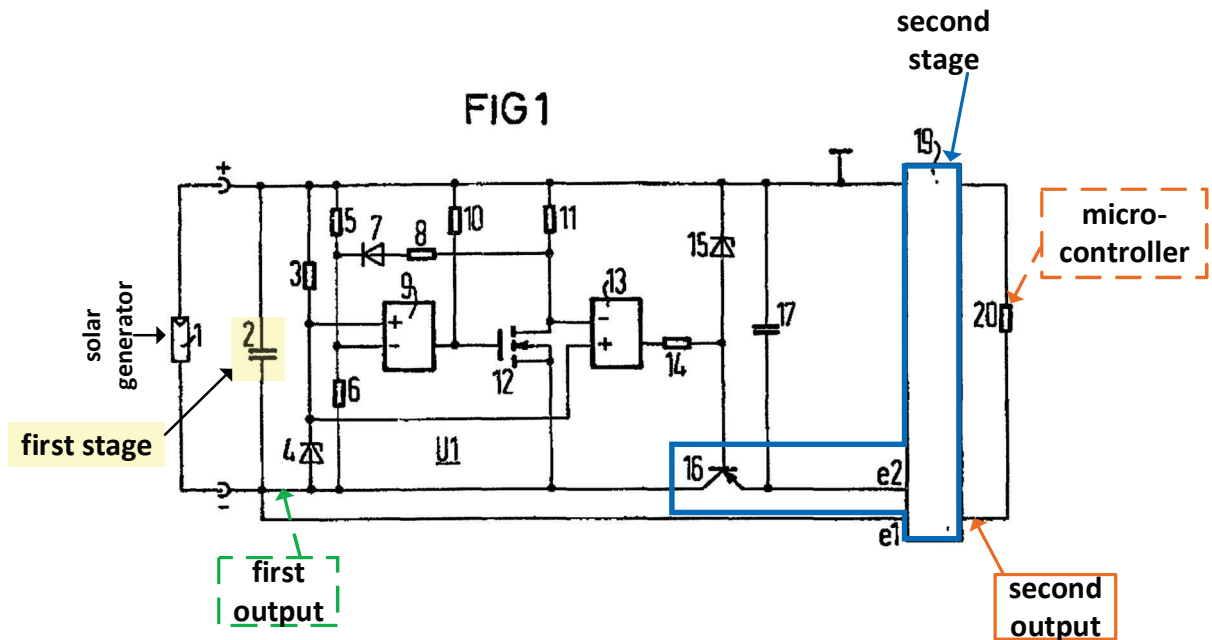


Fig. 19

Thus, Mieth teaches [1D].

- v. [1E]: “connecting the first output of the first stage to a switchable load to consume at least a portion of the first output while disabling the second stage in supplying the second output to the micro-controller;”

106) Mieth discloses that the first output (dashed-green) of capacitor 2 is connected to transistor 12 that is connected to a preliminary load 11 as shown in Fig. 20 below.

Ex.1002, Fig.1, 10:5-14.

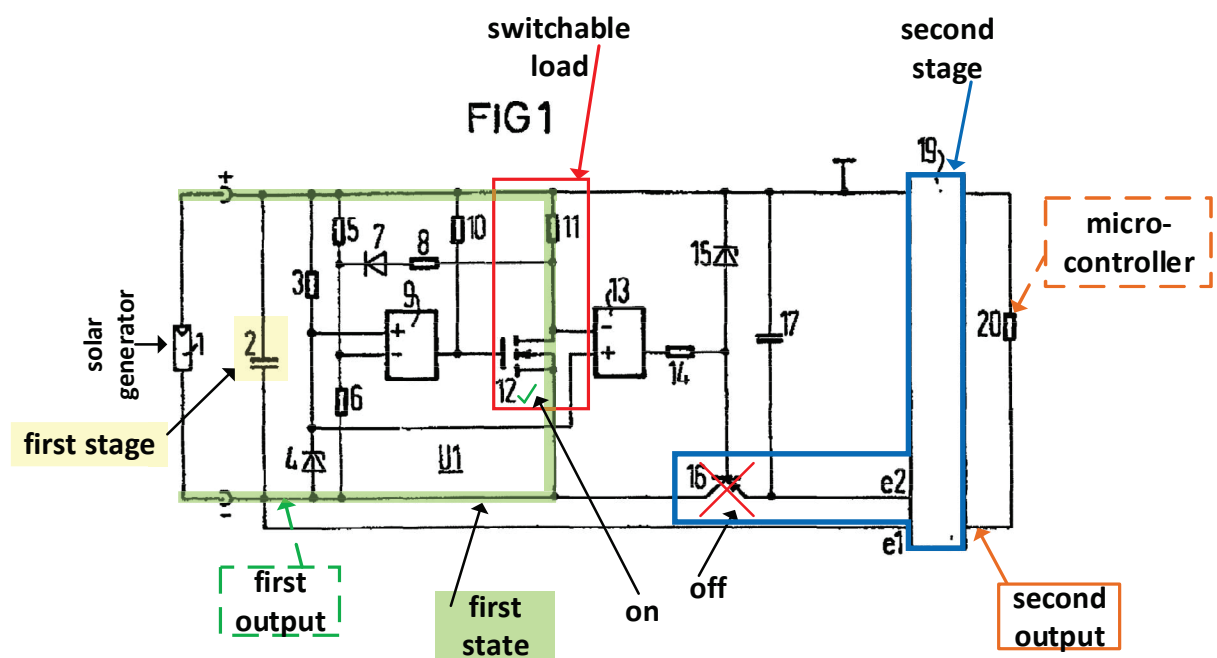


Fig. 20

107) The field-effect transistor 12, which operates as a switch, and the preliminary load 11 in combination are analogous to the claimed *switchable load* (red). Mieth discloses that when voltages at the first output are below a predefined minimum value, transistor 12 is “on”, and operates as a closed switch where the preliminary load 11 is connected to the solar generator 1 by the first output. Ex.1002, 9:15-23.

As such, because the preliminary load 11 is connected to the first output during this state, the preliminary load 11 *consumes at least a portion of the first output* as recited in claim 1.

108) As shown in Fig. 20 above, a first state (highlighted-green) illustrates that the switchable load is powered by the first output from the capacitor 2 (i.e., field-effect transistor 12 is “on” or in a conducting state). Additionally, in the first state, bipolar transistor 16 is “off” or in a non-conducting state, preventing the power supply apparatus 19 from being powered by the first output. When the preliminary load 11 is connected to the first output, the power supply apparatus 19 (second stage, blue) is not powered by the first stage (i.e., the first output) because the bipolar transistor 16 is “off”. Ex.1002, 9:9-13, 9:23-32. That is, the auxiliary voltage input e2 is associated with the first output only when the bipolar transistor 16 is conducting. *Id.* As such, in the first state the power supply apparatus 19 is *disabled in supplying the second output to the micro-controller* as recited in claim 1. The condition where the preliminary load 11 is connected to the first output and the power supply apparatus 19 is not powered is a “first state.”

109) Thus, Mieth teaches [1E].

- 110) As discussed above for feature [1E], when the circuit of Mieth is configured for the first state, bipolar transistor 16 is non-conducting, and the power supply apparatus 19 (i.e., second stage-blue) is disabled from supplying the load 20 (i.e., micro-controller-dashed-orange) with the second output (orange), see Fig. 21 below.

The diagram, labeled FIG1, illustrates a two-stage solar power converter. It begins with a solar generator (1) connected to a voltage divider (2). The first stage (3) includes a reference voltage generator (4) and a first output (5). The input voltage (6) is fed into a switchable load (7) which can be turned 'on' or 'off'. The second stage (8) produces a second output (9). A micro-controller (10) is connected to the circuit, and a second stage (11) is also indicated. The circuit includes various components like resistors (12, 13, 14, 15, 16, 17, 18, 19, 20), capacitors (21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100), and a micro-controller (10).

111) While in the first state, transistor 12 is turned “on” by a comparator 9 (hereinafter the first comparator 9) thereby loading the first output with the preliminary load 11 (controlled through transistor 12 when conducting (*i.e.*, the first state – analogous

to the switchable load-red). Ex.1002, 9:15-32, 10:5-14. In the first state, the first comparator 9 compares a reference voltage from a reference voltage generator (highlighted-teal-outlined-red) connected to a positive terminal of the first comparator 9 to a voltage from a voltage divider (highlighted-teal-outlined-green) connected to a negative terminal of the first comparator 9. Ex.1002, 9:34-10:3. The reference voltage generator is defined by the Zener diode 4. *Id.* The voltage divider is defined by resistors 5 and 6, and the monitored voltage is representative of the first output. *Id.* The first comparator 9 compares the voltage provided by the voltage divider 5 and 6 to the reference voltage to determine if the monitored voltage magnitude exceeds a threshold voltage. See ¶80 Ex.1002, 12:12-26.

112) In the first state, the monitored voltage magnitude is less than the threshold voltage magnitude, and the circuit of Mieth powers the preliminary load 11 and field-effect transistor 12 by the first output of capacitor 2 (*i.e.*, first stage) which is the same as the claimed ***first output from the first stage powering the switchable load.***

Ex.1002, 12:12-19. In the first state of Mieth where transistor 12 is on, the drain voltage of transistor 12 is approximately the same as the *first output* voltage thus driving the negative input of the second comparator 13 to a voltage less than the voltage at the positive input of the second comparator 13. This causes the output of the second comparator 13 to go high and as a result, turns off the bipolar transistor 16. Thus, the first state of Mieth disables the second output of the power supply

apparatus 19 to the load 20 by turning the bipolar transistor 16 “off,” which is the same as the claimed *the second output to the micro-controller is disabled. Id.* The time period the circuit of Mieth is in the first state is the same as the claimed *time period* and the predefined minimum value of Mieth is the same as the claimed *threshold*. Ex.1002, 9:15-26. The circuit of Mieth is in the first state for the time period when the circuit determines whether the predefined minimum value is satisfied, which is equivalent to the claimed *determining whether the first output . . . is above a threshold during a time period.*

113) Thus, Mieth teaches [1F].

- vii. [1G]: “in response to a determination that the first output from the first stage powering the switchable load is above the threshold during the time period in which the second output to the micro-controller is disabled, disconnecting the switchable load from the first output of the first stage; and instructing the second stage to enable the second output to the micro-controller using power from the first output of the first stage.”

114) As discussed in accordance with the features of [1F] above, in the first state, the preliminary load 11 and the field-effect transistor 12 (i.e., switchable load-red) are powered by the first output of capacitor 2 (i.e., first stage-highlighted-yellow).

Mieth further discloses that when voltages from the solar generator 1 (as represented at the negative terminal of first comparator 9) are above a predefined minimum value (as represented at the positive terminal of first comparator 9), the auxiliary voltage input e2 of the power supply apparatus 19 is connected to the first

output of the solar generator 1. Ex.1002, 9:23-26. As shown in Fig. 22 below, (Ex.1002, Fig.1 when the predefined minimum value is satisfied, the circuit of Mieth operates in a second state (highlighted-pink) where the bipolar transistor 16 is “on” or conducting, causing the first output (dashed-green) of capacitor 2 to be connected to e2, thereby powering the power supply apparatus 19. Ex.1002, 10:16-29.

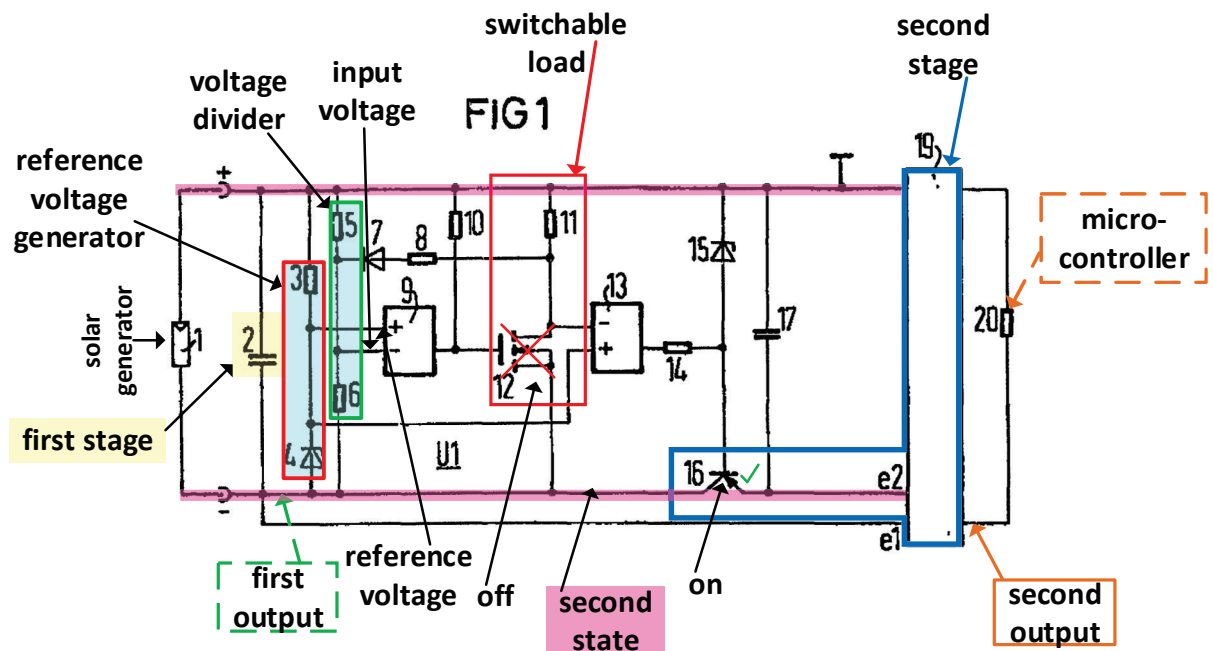


Fig. 22

115) Furthermore, in the second state, the field-effect transistor 12 is “off” or non-conducting, thereby disconnecting the preliminary load 11 from the first output. *Id.* As discussed above, the first comparator 9 compares a reference voltage from a reference voltage generator (highlighted-teal-outlined-red) to a voltage from a voltage divider (highlighted-teal-outlined-green) to determine if the monitored

voltage magnitude exceeds a threshold voltage. See ¶80 Ex.1002, 12:12-26. While in the first state, when the first output voltage magnitude across capacitor 2 rises above the threshold (*i.e.*, “predefined minimum value” as quoted by Mieth, as in the voltage magnitude is above the threshold), the circuit disconnects the preliminary load 11 from the first output by configuring the field-effect transistor 12 to an “off” state, which is the same as the claimed ***disconnecting the switchable load from the first output of the first stage. Id.***

116) The bipolar transistor 16, that connects the power supply apparatus 19 to the first output which results in the second output of the power supply apparatus 19 powering the load 20, is the same as the claimed ***instructing the second stage to enable the second output to the micro-controller using power from the first output of the first stage.***

117) When the circuit of Mieth is in the first state, the circuit makes a determination that the predefined minimum value is satisfied while the second stage, including the micro-controller, is disabled, and in response changes to the second state, which is analogous to the claimed ***in response to a determination . . .*** Ex.1002, 9:15-23.

118) As such, Mieth teaches [1G], and every feature of claim 1.

2. Dependent Claim 2

119) Claim 1 is disclosed by Mieth, as highlighted above. Claim 2 depends from claim 1 and requires [2A], “the switchable load comprises: a resistive device.” Ex.1001,

claim 2. As shown below in Fig. 23 (Ex.1002, Fig.1) and disclosed by Mieth, preliminary load 11 (highlighted-orange) can be a resistor. Ex.1002, 12:14-20 (preliminary load formed by the resistor 11). Since the preliminary load 11 can be a resistor, and a resistor is a resistive device, preliminary load 11 of Mieth is analogous to the *resistive device* of claim 2.

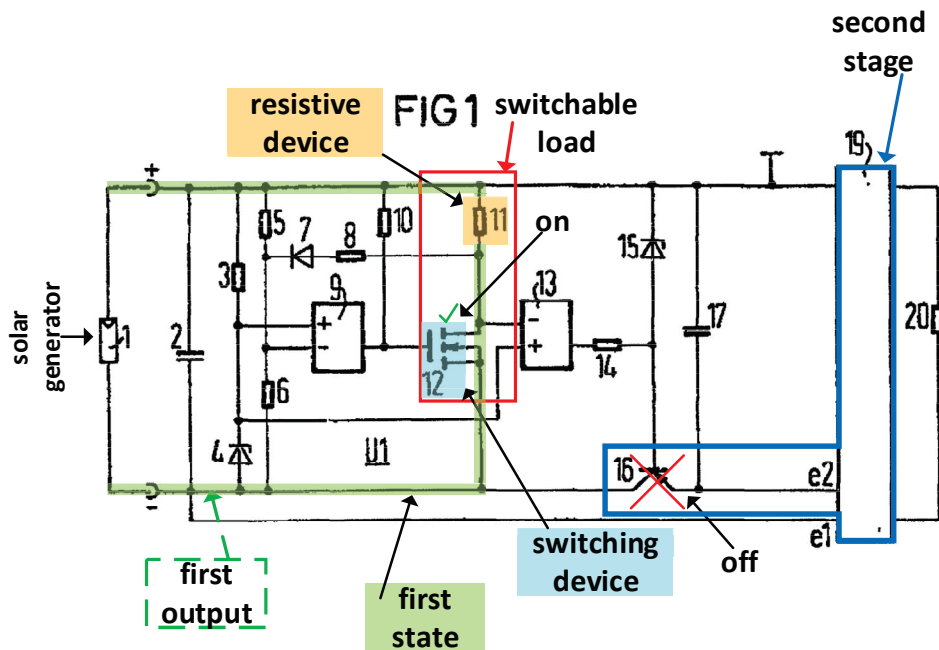


Fig. 23

120) Claim 2 further requires [2B], “a switching device connected to the resistive device.” Ex.1001, claim 2. As shown in Fig. 23 (Ex.1002 Fig.1), a field-effect transistor 12 (highlighted-teal) is connected to the preliminary load 11. Mieth describes the field-effect transistor 12 as a first electronic switch, and thus a PHOSITA would understand that the field-effect transistor 12 is a switching device. Ex.1002, 10:5-14. As such, the field-effect transistor 12 is analogous to the

switching device of claim 2 and the field-effect transistor 12 connected to the preliminary load 11 is analogous to feature [2B].

121) Claim 2 further requires [2C], “wherein the switching device is configured to be turned on to be connected to the first output to consume the portion of the first output and turned off to be disconnected from the first stage.” Ex.1001, claim 2. As shown in Fig. 23 (Ex.1002, Fig.1) of Mieth, the field-effect transistor 12 is “on” or in a conducting state to connect the switchable load to the first output (dashed-green) when the circuit is in the first state (highlighted-green). When the field-effect transistor 12 is in the “on” state, the preliminary load 11 is connected to the solar generator 1 by the first output, and thus consumes the portion of the first output. Ex.1002, 9:15-23. Furthermore, as shown in Fig. 1 of Mieth (reproduced in Fig. 22 provided above), in the second state the field-effect transistor 12 is “off” or in a non-conducting state to disconnect the switchable load 11 from the first output. Ex.1002, 12:21-26. Thus, the field-effect transistor 12 connects or disconnects the preliminary load 11 from the first output according to the first state or the second state, respectively, *which is the same as [2C]*. Thus, Mieth discloses every feature of claim 2.

3. Dependent Claim 3

122) Claim 2 is taught by Mieth for the reasons discussed above. Claim 3 depends from claim 2 and requires, “wherein the disconnecting of the switchable load from the

first output of the first stage comprises sending a first signal to the switching device to turn off the switching device.” Ex.1001, claim 3.

123) As shown in Fig. 24 below (Ex.1002, Fig.1), the first comparator 9 is connected to the first output by a Zener diode 4, and resistor 3. Ex.1002, 12:12-19.

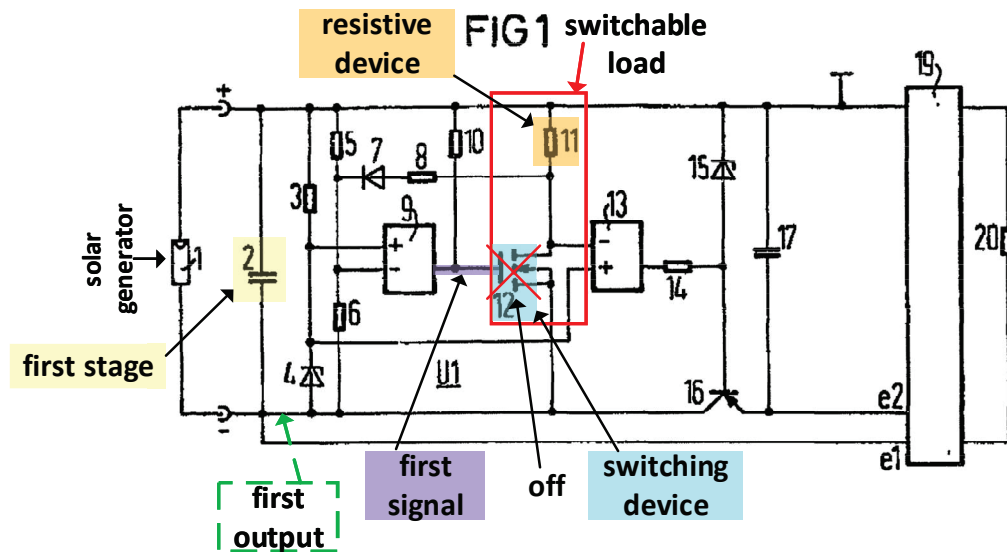


Fig. 24

124) The first comparator 9 outputs a first signal (highlighted-purple) to the field-effect transistor 12 (switching device, highlighted-teal) based on a comparison of the monitored voltage and a threshold voltage. See ¶80. *Id.* The first signal from first comparator 9 is a voltage connected to the gate of the field-effect transistor 12. When the first signal from the first comparator 9 is low or zero (e.g., high voltages at the first output and thus the second state), the field-effect transistor 12 is in a non-conducting or “off” state. When the first signal from the first comparator 9 is high (e.g., low voltages at the first output and thus the first state), the field-effect

transistor 12 conducts or is in an “on” state. Since the output of the first comparator 9 turns the field-effect transistor 12 “on” and “off”, a PHOSITA would understand that the output of the first comparator 9 is analogous to the claimed *first signal* as the output from the first comparator 9 operates the field-effect transistor 12 just as the claimed first signal operates the claimed switching device in claim 3.

125) When the magnitude of the voltage at the first output rises above a predefined threshold, the field-effect transistor 12 is turned “off” by the first comparator 9 outputting the first signal with a low voltage, and the preliminary load 11 (resistive device-highlighted-orange) is electrically disconnected from the first output.

Ex.1002, 12:12-30. As such, the preliminary load 11 is disconnected from the first output of capacitor 2 (first stage-highlighted-yellow) by a first signal from the first comparator 9 that signals the field-effect transistor 12 to turn “off”, which is analogous to *disconnecting of the switchable load from the first output of the first stage comprises sending a first signal to the switching device to turn off the switching device* as recited in claim 3.

126) Thus, Mieth discloses every feature of claim 3.

4. Dependent Claim 4

127) Claim 3 is disclosed by Mieth, as shown above. Claim 4 depends from claim 3 and requires [4A], “further comprising: generating the first signal based on the

determining of whether the first output from the first stage powering the switchable load is above the threshold; and.” Ex.1001, claim 4.

128) As shown in Fig. 25 below (Ex.1002, Fig.1), the first output of capacitor 2 is represented at the positive terminal of first comparator 9 as an input “sensed” voltage defined by the first output and the voltage divider 5, 6. The output of the first comparator 9 (e.g., the claimed first signal, **highlighted-purple**) controls the field-effect transistor 12 (switching device, **highlighted-teal**) based on whether the magnitude of the monitored voltage satisfies the predefined threshold voltage (e.g., the claimed threshold). Ex.1002, 12:21-30.

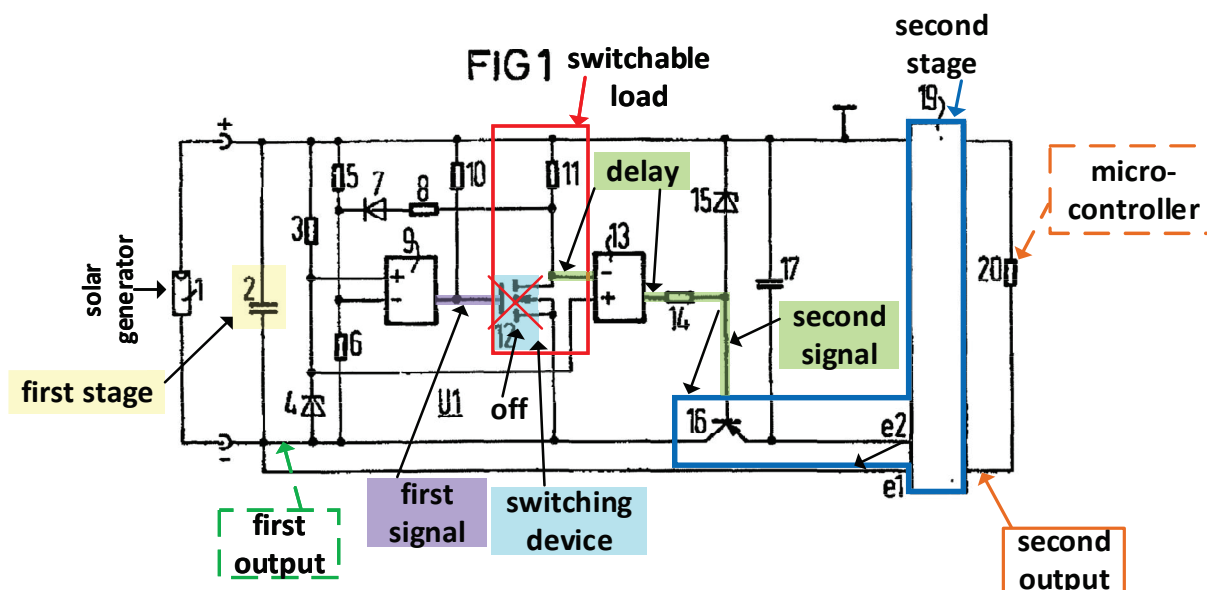


Fig. 25

129) Specifically, the output of the first comparator 9 turns the transistor 12 “off” when the predefined threshold voltage is satisfied. See ¶80, Ex.1002, 10:16-29, 12:21-30.

The circuit of Mieth generating the first signal (i.e., the output of the first

comparator 9 that feeds the gate of the transistor 12) based on the first output of the capacitor 2 exceeding the predefined threshold voltage is analogous to [4A].

130) Claim 4 further requires feature [4B], “delaying the first signal to generate a second signal to the second stage, the second signal enabling the second output to the micro-controller.” Ex.1001, claim 4.

131) Mieth discloses delaying the first signal from the first comparator 9 to generate a second signal from the output of the second comparator 13 to enable the load 20. Mieth discloses that the field-effect transistor 12 and a comparator 13 (hereinafter the second comparator 13) delays the first signal from the first comparator 9 to generate a second signal (highlighted-green) that turns on the bipolar transistor 16. When bipolar transistor 16 turns on, the first output is connected to the e2 input to energize the power supply apparatus 19 (second stage-blue) which enables the second output (orange) of the power supply apparatus 19 to power the load 20 (micro-controller-dashed-orange), which is analogous to the features of [4B] as discussed below. Ex.1002, Fig.1, 11:4-12, 12:12-19.

132) The bipolar transistor 16 operates as a switch that can connect the first output to the power supply apparatus 19. Ex.1002, 10:31-36. The base of the bipolar transistor 16, which controls the conducting or non-conducting state of the bipolar transistor 16, is controlled by the output of the second comparator 13. Ex.1002, 10:36-11:12. The second comparator 13 outputs the second signal based on an

input from the field-effect transistor 12, where the input from the field-effect transistor 12 is itself based on the first signal. *Id.* As such, the state of the second signal is dictated by the state of the first signal, and the transition of the second signal to activate bipolar transistor 16 is delayed with respect to the transition of the first signal by the transistor 12 and the second comparator 13 which is analogous to the claimed *delaying the first signal*. The second comparator 13 generates the second signal based on the first signal which is analogous to the claimed *to generate a second signal*, and the second signal controls the bipolar transistor 16 which is analogous to the claimed *to the second stage*. Furthermore, if the *delaying the first signal* should be defined by a specific delay circuitry rather than the intrinsic switching characteristics of comparator 13 and switch 12, a PHOSITA would have known to add a capacitor parallel to resistor 11 according to customary practices in the art at the time of filing. Further, or in alternative, one or more buffer circuits or delay elements could be interposed between the second comparator output and the base of bipolar transistor 16 to define a larger delay period. For example, U.S. Patent No. 4,617,529 (Suzuki) clearly shows the use of adding a delay element composed of a resistor and capacitor in one or more locations in an oscillator circuit to adjust an amount of desired delay. Ex. 1015, Fig. 3; 3:53-63.

133) The second signal turns the bipolar transistor 16 on when the output of the first stage, as represented at the negative input terminal of second comparator 13, is above a threshold voltage of the second comparator 13, and powers the power supply apparatus 19. Ex.1002, 12:21-30. When the power supply apparatus 19 is powered, the second output is enabled to the load 20. Ex.1002, 8:29-35. The bipolar transistor 16 of Mieth turned on by the second signal, which enables the second output to the load 20, is analogous to the claimed *second signal enabling the second output to the micro-controller*.

134) Thus, Mieth teaches all the features of claim 4.

5. Dependent Claim 5

135) Claim 4 is disclosed by Mieth, as highlighted above. Claim 5 depends from claim 4 and requires [5A], “further comprising: providing a control circuit comprising: a hysteresis amplifier configured to receive the first output of the first stage and generate the first signal”.

136) As shown in Fig. 26 below, (Ex.1002, Fig.1), Mieth discloses a capacitor 2 (highlighted-yellow) analogous to the claimed first stage and outputs a first output (dashed-green) analogous to the claimed first output, a first comparator 9 (dashed-blue) that is analogous to the claimed hysteresis amplifier and outputs a first signal (highlighted-purple) analogous to the claimed first signal that teach [5A] as discussed further below.

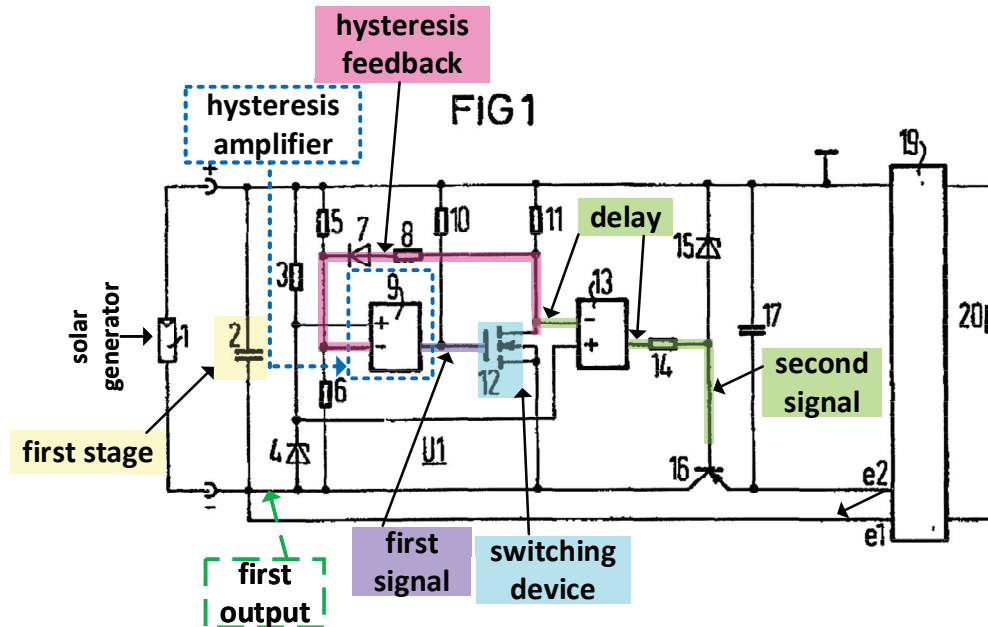


Fig. 26

137) Feature [5A] recites hysteresis, which a PHOSITA would understand is a positive feedback loop between the output of a device and an input of a device, such as an amplifier or comparator, to mitigate instability in switched signals. For example, my CMOS text states, “[t]here are many ways to introduce hysteresis in a comparator. All of them use some form of positive feedback.” Ex. 1009, 467. A PHOSITA would further understand that an amplifier can be configured as a comparator, and thus the first comparator 9 can be an amplifier. Ex. 1009, 439 (stating, “... because a comparator has many of the same characteristics as a high-gain amplifier.”) The Mieth hysteresis operation was described previously in detail and summarized here (see above ¶¶ 57-60, 77-82). The first comparator 9 is configured with hysteresis where the hysteresis feedback path (highlighted-pink) from the output of the switching device (field-effect transistor 12) is connected to

the negative input of the first comparator 9 through resistor 8 and diode 7.

Ex.1002, 9:34-38. Furthermore, Mieth recites that “Hysteresis is achieved by means of the resistor 8.” Ex.1002, 12:26-27. Specifically, when switch 12 is off, the series circuit comprising resistors, 8, 11 and diode 7 are in parallel with resistor 5 forming a voltage divider with resistor 6. When switch 12 is on, diode 7 is off and no current flows through resistor 8, leaving only resistors 5 and 6 to form the voltage divider. In this way the first comparator 9 and associated circuitry exhibit hysteretic behavior. Since the first comparator 9 can be an amplifier with a positive feedback loop, the first comparator 9 is the same as the claimed ***hysteresis amplifier***. The first output of the capacitor 2 is represented at the negative input of the first comparator 9 through a voltage divider defined by resistors 5 and 6, which is analogous to the claimed ***hysteresis amplifier configured to receive the first output of the first stage***. Ex.1002, 9:34-38. The output of the first comparator 9 is a first signal as discussed previously, and is analogous to the claimed recitation ***generate the first signal***. As a PHOSITA, I understand that the circuitry of Mieth, that includes the first comparator 9, is analogous to the claimed ***control circuitry***, as the first comparator 9 generates the first signal that controls the field-effect transistor 12. Thus, Mieth teaches [5A].

138) Claim 5 further requires [5B], “a delay circuit to generate the second signal according to the first signal.” Fig. 26 above, which corresponds to Fig.1 of Mieth

further illustrates the field-effect transistor 12 (switching device, highlighted-teal) and the second comparator 13 that delays the first signal (highlighted-purple) from first comparator 9 to generate a second signal (highlighted-green). Ex.1002, Fig.1, 11:4-12. Since, the field-effect transistor 12 and the second comparator 13 delays the first signal to generate the second signal, the field-effect transistor 12 and the second comparator 13 are analogous to the claimed *delay circuit to generate the second signal according to the first signal*. However, if the *delay* circuit should be defined by a specific circuitry rather than the intrinsic switching characteristics of comparator 13 and switch 12, delay elements discussed above in accordance with claim 4 can be implemented.

139) Thus, Mieth teaches [5B] and all features of claim 5.

6. Dependent Claim 6

140) As discussed above, claim 3 is taught by Mieth. Claim 6 depends from claim 3 and requires, “wherein the switching device includes one of: a field effect transistor (FET), a metal-oxide-semiconductor field-effect-transistor (MOSFET), and a bipolar junction transistor.” Ex.1001, claim 6.

141) As discussed in great detail in analyzing various claims above, the field-effect transistor 12 (highlighted-teal) is analogous to the *switching device*. See Ex.1002, Fig.1 (annotated-Claim-2). The field-effect transistor 12 is the same as the claimed *field effect transistor (FET)*.

142) As such, Mieth teaches all the features of claim 6.

7. Dependent Claim 7

143) Claim 6 is taught by Mieth, as shown above. Claim 7 depends from claim 6 and requires, “wherein when the switch device is turned on, the switchable load and an input of the second stage are connected in parallel to the first output of the first stage.” Ex.1001, claim 7.

144) As shown in Fig. 27 below (Ex.1002 Fig.1), Mieth discloses a first output (dashed-green) of the capacitor 2 (first stage-highlighted-yellow), field-effect transistor 12 (switch device-highlighted-teal) connected to a preliminary load 11 analogous to the claimed switchable load (red), an output signal from the field-effect transistor 12 (highlighted-green) analogous to the claimed second stage input, where the output signal controls the transistor 16 and power supply apparatus 19 (second stage-blue), and parallel connection nodes (circles-red) as discussed below.
Ex.1002, 9:15-18, 10:5-14, 11:14-16.

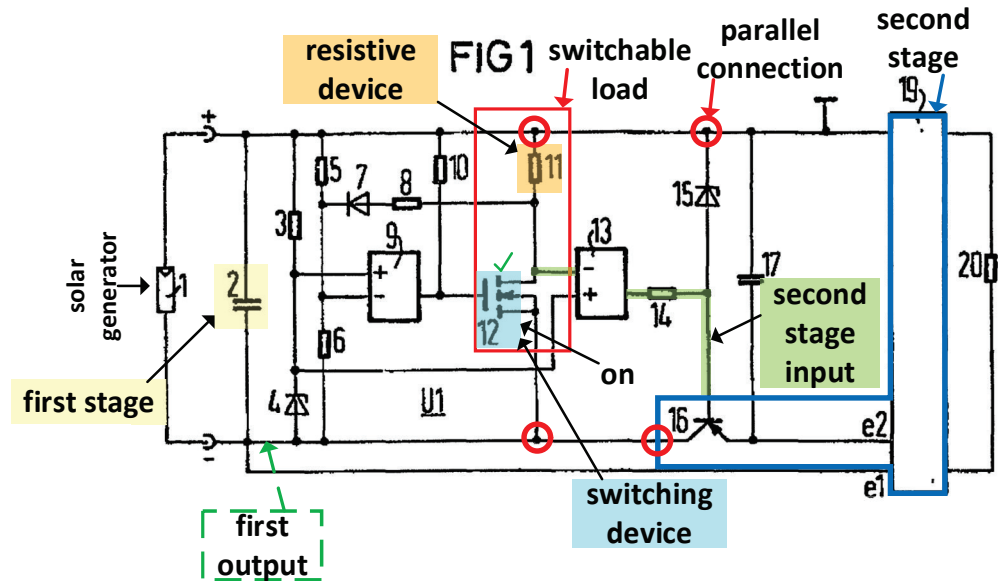


Fig. 27

145) When the field-effect transistor 12 is “on”, the load 11 is connected to the first output as described previously in conjunction with the first state, and is analogous to the claimed *when the switch device is turned on*. Furthermore, the field-effect transistor 12 outputs a signal to the second comparator 13, which then connects to the transistor 16 of the second stage and is analogous to the claimed *input of the second stage*. Ex.1002, 11:4-12. The parallel connection nodes show that the switchable load is connected in a parallel configuration with the first output of capacitor 2, and the second stage input to the transistor 16 (i.e., the collector terminal) is connected in parallel with the first output which is analogous to the claimed *the switchable load and an input of the second stage are connected in parallel to the first output of the first stage*.

146) Thus, Mieth teaches all the features of claim 7.

8. Dependent Claim 9

147) Claim 1 is taught by Mieth, as discussed above. Claim 9 depends from claim 1 and requires, “wherein the disconnecting is performed prior to the instructing of the second stage to enable the second output to the micro-controller.” Ex.1001, claim 9.

148) As discussed above, Mieth discloses a power supply apparatus 19 connected to a bipolar transistor 16 (second stage-blue), a second output from the power supply apparatus 19 is connected to the load 20 (micro-controller-dashed-orange), and a field-effect transistor 12 that disconnects the switchable load (red) from the first output when configured in a second state (highlighted-pink), see Fig. 28 below (Ex.1002, Fig. 1).

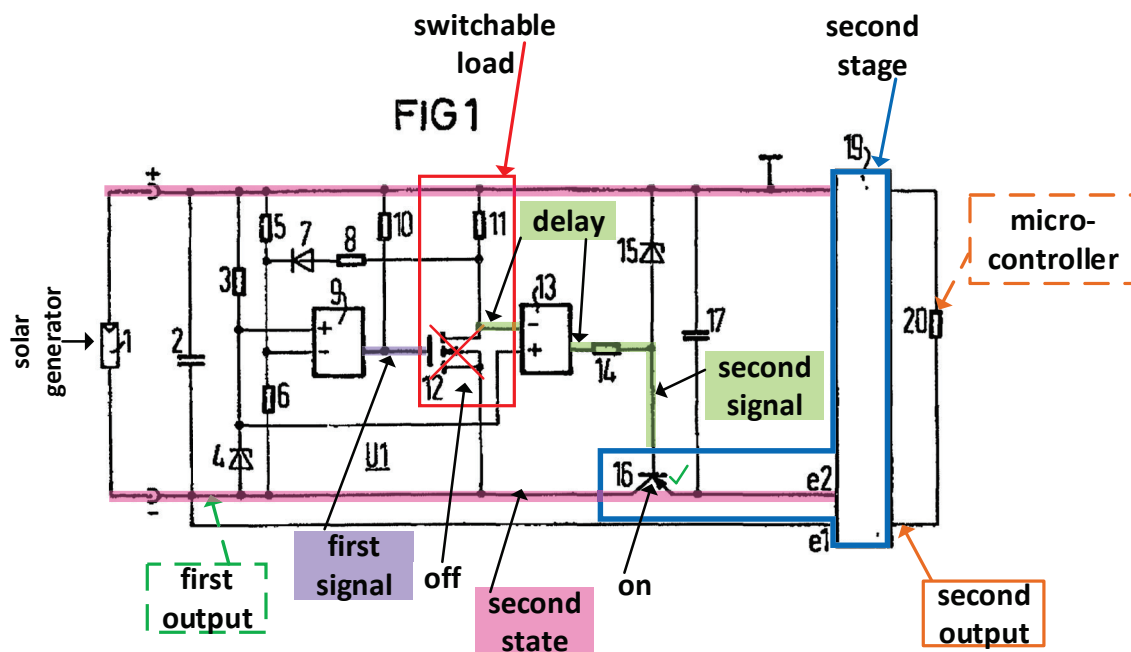


Fig. 28

149) The field-effect transistor 12 is controlled by a first signal from first comparator 9 which has a monitored voltage associated with the first output connected to the inputs of first comparator 9 via resistor divider 5, 6, and Zener diode 4. Ex.1002, 9:15-18. The field-effect transistor 12 outputs a signal to second comparator 13 and the output of the second comparator 13 is a second signal (**highlighted-green**) that controls the bipolar transistor 16 to turn the second stage on, thereby enabling the second output to the load 20. Ex.1002, 10:36-11:12. Since the second signal controls the “on” or “off” state of the bipolar transistor 16 which enables the second output of the power supply apparatus 19 to the load 20, the second signal is analogous to the claimed *instructing of the second stage to enable the second output to the micro-controller*. A PHOSITA would understand that the field-effect transistor 12 has a switching delay time, and that the second comparator 13 has a propagation delay time as discussed previously in paragraphs 130-133 and Fig. 25. As such, the first signal that turns “off” the field-effect transistor 12, which is analogous to the claimed *disconnecting* of the switchable load, is delayed by the field-effect transistor 12 and second comparator 13 to generate the second signal that enables the power supply apparatus 19. The second signal of Mieth is delayed (with respect to the first signal) to turn on bipolar transistor 16 after the field-effect transistor 12 is turned “off” (i.e., a “break before make” arrangement), that is, the field-effect transistor 12 is turned “off” prior to the bipolar transistor 16 being

turned on, which is analogous to the claimed *disconnecting is performed prior to the instructing of the second stage*. However, if the “*disconnecting is performed prior to . . .*” should be defined by a specific circuitry rather than the intrinsic switching characteristics of comparator 13 and switch 12, delay elements discussed in accordance with claim 4 (in paragraphs 130-133 above) can be implemented.

150) Thus, Mieth teaches all the features of claim 9.

B. Ground B: Anticipation/obviousness of claims 1-12, 15-18, and 20 in view of Mieth and Balogh

- 1. Independent Claim 1 features [1B]: “the method comprising: providing a power supply having a first stage and a second stage”, [1C]: “wherein the first stage converts power from a direct current input into a first output, and;”, [1D]: “the second stage powered by the first output has a second output for a micro-controller;”**

151) Independent claim 1 features [1B]-[1D] are taught by Mieth as discussed above in paragraphs 97-105. As discussed previously, Mieth teaches the first stage.

However, Balogh (Ex.1003) also discloses a first stage, and a PHOSITA would have been motivated to combine Mieth and Balogh together for at least the following reasons.

152) Balogh discloses cascaded converter arrangements (*e.g.*, Balogh Figs. 1B and 1C), and states that such cascaded arrangements using first and second buck converters are employed in circuit applications that require large input/output conversion ratios. Ex.1003, 1:21-27. It is well known to a PHOSITA that photovoltaic systems

sometimes couple together multiple photovoltaic cells that form photovoltaic panels or modules to realize high input voltages, and such high input voltages need large conversion ratios to step down the input voltage. Ex.1003, 1:21-27. Even PV applications that employ a single PV module can experience voltages as high as 80V that may require a large conversion ratio to step down the voltage. Ex. 1010, Ex. 1011. Thus, Balogh makes clear that cascaded step-down converters (or buck converters) readily find use in photovoltaic applications where a significant step-down ratio may be needed.

153) In addition, Xu reflects further general knowledge of a PHOSITA that cascaded converters advantageously improve circuit efficiency. Ex. 1012. Xu states that in some applications where there is a lower input-to-output voltage ratio the first converter is configured with a duty cycle of one so that it operates as a well-known L-C filter for second stage whereby reducing the input L-C filter for the overall system. For at least these reasons, it would have been obvious for a PHOSITA to combine Balogh with Mieth in view of the general knowledge of a PHOSITA, as shown by the teaching of Xu, where large output/input ratios are more efficient when implemented with cascaded buck converters.

154) Balogh further teaches a cascaded converter arrangement using a first stage transformer-coupled input power converter that steps down an input voltage to an

intermediate voltage, followed by a second stage buck output converter that further steps down the intermediate voltage to a final voltage. Ex.1003, 1:62-66, Fig. 1D.

155) Mieth states that applications having photovoltaic energy sources or wind energy sources often provide varying levels of input voltage, and that such voltages can create difficulties when serving as an input to a power converter. Ex.1002, 5:22-38.

Mieth further teaches the use of a switchable load in situations where an input voltage to a power converter varies in a particular way, such as the voltage from a photovoltaic system that will vary depending upon the time of day, partial shading conditions, or weather conditions. Ex.1002, 5:22-38.

156) A PHOSITA would have been motivated to combine the cascaded power converter architecture of Balogh with the switchable load feature of Mieth for DC applications with high input voltages based on the motivation provided by Balogh alone, or further in view of the general knowledge of a PHOSITA as evidenced by Xu highlighted in paragraph 153 above. Mieth is directed towards solar generators that generate up to 36 volts (V). Ex.1002, 12:21-26. Balogh discloses higher DC voltages relative to Mieth, for example, 48V with large step-down ratios, for example, 48V to 1.5V. Ex.1003, 10:45-52. In other examples, solar panel modules can have 80V output voltages requiring large step-down ratios. “ME,” a data sheet from Mitsubishi, for example, offers PV modules with open-circuit output voltages on the order of 30 volts. Ex. 1011. SOLIBRO PV modules (Q-CELLS) offer even

higher open circuit output voltages in the range of 90V. Ex. 1010. In order to maximize efficiency, a PHOSITA would look to Xu as a guide and Exs. 1010 and 1011 as a reflection of the general knowledge in the art and use a cascaded buck architecture, as taught in Balogh. As such, a PHOSITA would have known to combine the cascaded power converter architecture of Balogh with Mieth for high DC applications typical in solar applications (e.g., 48V or 80V solar panel modules) to realize an appropriate intermediate voltage for the switchable load 11 and the output load 20 of Mieth.

157) The combination of Mieth and Balogh merely involves combining known prior-art elements (Mieth's switchable load and Balogh's cascaded step down converter architecture) according to known methods to yield predictable results; that is, a cascaded step down power converter having a switchable load at the second power converter input that is selectively employed based on the state of the first stage step-down power converter. Based on my experience as a PHOSITA, I would have no difficulty combining together the circuit features set forth in the Mieth and Balogh references, respectively. Based on my knowledge and experience, a PHOSITA readily had, at the time of filing the '021 patent, the skills, knowledge, and motivation to carry out the combination of Mieth and Balogh, and a PHOSITA would have a reasonable expectation of success in combining Mieth and Balogh. As a PHOSITA, upon reading Mieth and Balogh, and further evaluating Xu and

the data sheets in Exs. 1010 and 1011, I readily appreciate the benefit of adapting the high DC voltage stepped down to an intermediate voltage of Balogh to situations with a variable input voltage to a power converter as shown in Mieth. Further, as a PHOSITA, I do not foresee any undue technical hurdles to applying Mieth with Balogh, as such a combination would have been a simple modification to Mieth's system, readily accomplished by a PHOSITA. Accordingly, Mieth in combination with Balogh is proper and teaches [1B]-[1D]. *Id.*

158) Specifically, while the capacitor 2 in Fig. 1 of Mieth is analogous to the claimed first stage, and the bipolar transistor 16/power supply apparatus 19 is analogous to the claimed second stage, Balogh discloses a cascaded converter arrangement having an isolated DC-DC converter followed by a post regulator circuit that reads on the claimed ***first and second stages***, respectively. Ex.1003 10:45-52.

159) Balogh's isolated DC-DC converter (analogous to the first stage-yellow) and post regulator circuit (analogous to the second stage-blue) are cascaded step-down converters and are shown in Fig. 29. Ex.1003, Fig.1D; 2:61-64.

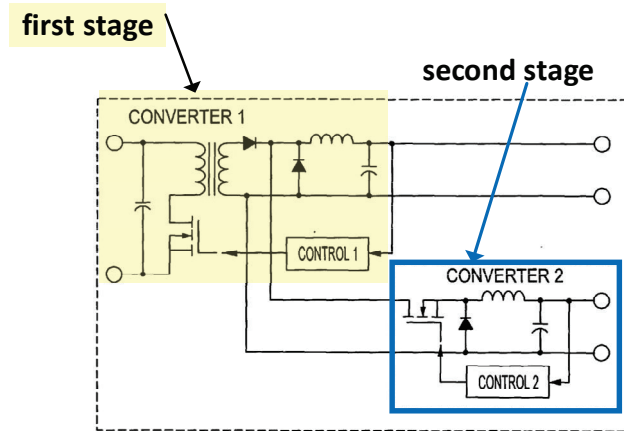


FIG. 1D
PRIOR ART

Fig. 29

160) Based on Balogh and the teachings of Xu, a PHOSITA would understand that cascaded converters are commonly used to provide input to output power conversion that is not optimally implemented in a single converter. Ex.1003, 1:25-28; Ex. 1012 (Xu). Thus, the purpose of the first stage and the second stage was previously described by Balogh, that is to provide input and output power conversion that is not optimally implemented in a single converter, for example, in high DC voltage applications. Ex.1003 10:45-52. The claimed first stage provides a first output to be consumed by the switchable load or to power the second stage, and the claimed second stage uses the first output from the first stage to power the micro-controller, which is not optimally implemented by a single converter (e.g. the first stage or the second stage alone). As such, a PHOSITA, at the time of filing, would know that the capacitor 2 and the power supply apparatus 19 of Mieth could be the cascaded converters as disclosed by Balogh. It would be obvious to a

PHOSITA to supply power to the claimed micro-controller with a first stage and a second stage separated by a switchable load as recited in claim features [1B]-[1D].

161) Thus, Mieth in combination with Balogh discloses [1B]-[1D].

162) Additionally, claims 2-7 and 9 are obvious in view of Mieth-Balogh for the reasons set forth above in ¶¶ 119-150.

2. Dependent Claim 8

163) Claim 1 is taught by Mieth, or alternatively by a combination of Mieth and Balogh, as discussed above. Claim 8 depends from claim 1 and requires, “wherein the first stage comprises a first step-down converter; and the second stage comprises a second step-down converter.” Ex.1001, claim 8. As discussed previously, a PHOSITA would have been motivated to combine the cascaded power converter architecture of Balogh with the switchable load features of Mieth. As discussed above and shown in Fig.1 of the reference, Mieth discloses a capacitor 2 (highlighted-yellow) which is analogous to the claimed *first stage* and discloses power supply apparatus 19 connected to the bipolar transistor 16 (blue) which is analogous to the claimed *second stage*. The power supply apparatus 19 is a DC-DC voltage converter or charging converter which a PHOSITA would understand can step-down DC power and is analogous to the claimed *second stage comprising a step-down converter*. Ex.1002, 8:29-35. Balogh teaches a first stage and a second stage that can each comprise step-down converters. Ex.1003, 1:29-36. Balogh

teaches that a cascaded arrangement can include a first buck converter and a second buck converter where a buck converter steps an input voltage down to an output voltage that is lower than the input voltage. *Id.* It would be obvious to a PHOSITA to modify the capacitor 2 of Mieth with the step-down converter from Balogh to realize the claimed *first stage comprises a first step-down converter; and the second stage comprises a second step-down converter.* Thus, Mieth-Balogh teach the features of claim 8.

3. Independent Claim 10

164) With reference to the claim listing appendix, Mieth and Balogh disclose elements [10A]-[10I]. As explained below, a PHOSITA would have been motivated by Mieth and Balogh to arrive at the alleged invention of claim 10.

i. [10A]: “A system to supply power, the system comprising:”

165) Mieth discloses a circuit that supplies power to an electrical load from a solar generator. Ex.1002, 8:8-9. A PHOSITA would understand that when the circuit of Mieth supplies power to the electrical load, the circuit is supplying power which is the same as the claimed *system to supply power.* Thus, Mieth teaches [10A].

ii. [10B]: “a power source to provide a direct current input”

166) The circuit of Mieth discloses a solar generator 1 that is a power source as shown in Fig. 30 (Ex.1002 Fig.1). Ex.1002, 4:29-32. A PHOSITA would understand that

solar generators generate a direct current, thus the solar generator 1 provides a direct current input (dashed-red).

167) Thus, Mieth teaches [10B].

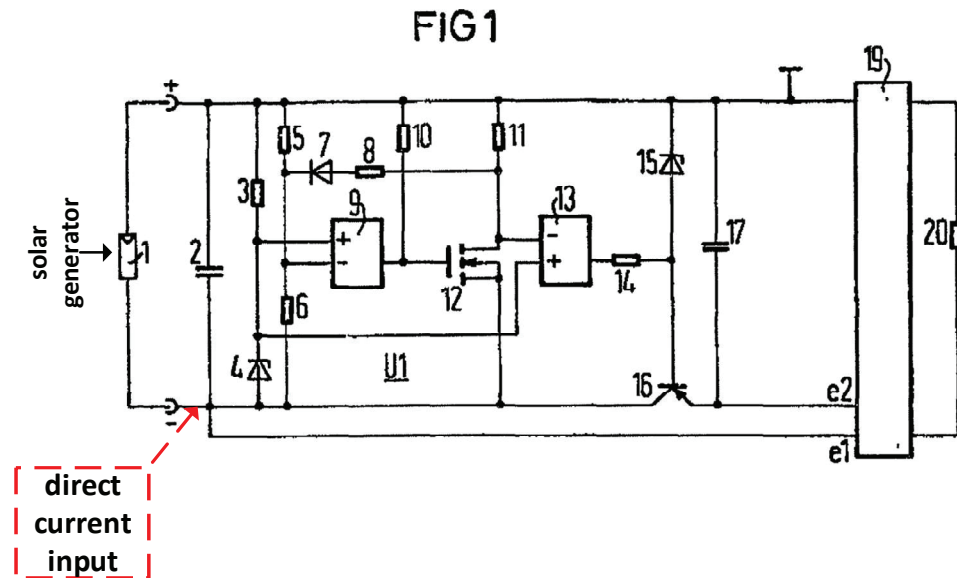


Fig. 30

iii. [10C]: “a first stage power converter configured to convert the direct current input into a first output”

168) The circuit of Mieth discloses a capacitor 2 connected in parallel with the solar generator 1 (Ex.1002 Fig. 1). As discussed in accordance with feature [1C] above, capacitor 2 converts power and thus capacitor 2 teaches a *first stage power converter*. Thus, the capacitor 2 of Mieth is anticipatory of claim 10 for the same reasons discussed in accordance with feature [1C]. Specifically, the capacitor 2 can stabilize the voltage across it (at the first output) due to fluctuations from the direct current input. As discussed *infra* in accordance with feature [10G], the first

output of capacitor 2 is converted according to the direct current input by the well known relationship $v = \frac{1}{C} \int i dt$. While Mieth teaches a first stage power converter, Balogh also discloses a first stage power converter and a PHOSITA would have been motivated to combine Mieth and Balogh for at least the reasons described in accordance with features [1B]-[1D] of claim 1 as discussed above in paragraphs 151-160, and in accordance with claim 8 as discussed in paragraph 163.

169) Balogh's isolated DC-DC converter (**yellow**) is a step-down converter and thus analogous to the claimed *first stage power converter* as shown in Fig. 31 (Ex.1003 Fig.1D), Ex.1003, 2:61-64.

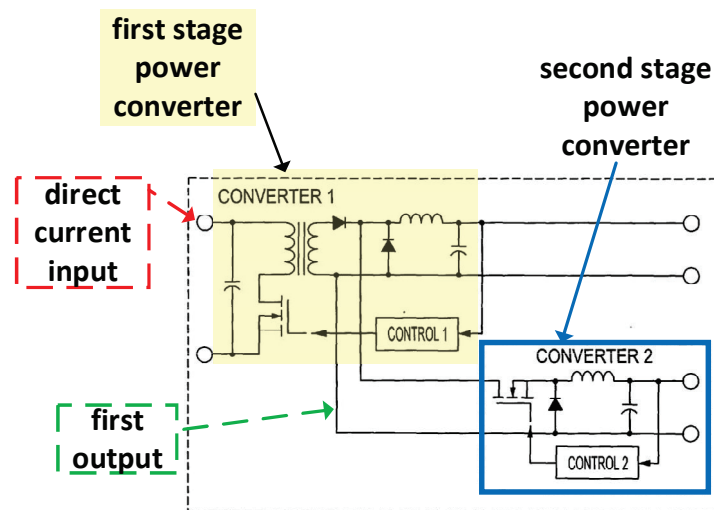


FIG. 1D
PRIOR ART

Fig. 31

170) The isolated DC-DC converter shows a capacitor in parallel with a transformer that converts the direct current input (**dashed-red**) to a first output (**dashed-green**).

Ex.1003 Fig. 1D. A PHOSITA would have been motivated to add a transformer

after the capacitor 2 of Mieth to realize the power converter of Balogh to convert the direct current input into a first output as described previously in paragraphs 151-160. Since the isolated DC-DC converter converts power from the direct current input to a first output, the isolated DC-DC converter is analogous to the claimed *first stage power converter* and the power converted by the DC-DC converter is analogous to the claimed *convert the direct current input into a first output*.

171) Since the capacitor 2 of Mieth can be replaced or supplemented with the DC-DC converter of Balogh, further discussion of Mieth will refer to capacitor 2 as analogous to the first stage power converter in view of Balogh for ease of discussion as shown below in Fig. 32 (Ex.1002 Fig. 1).

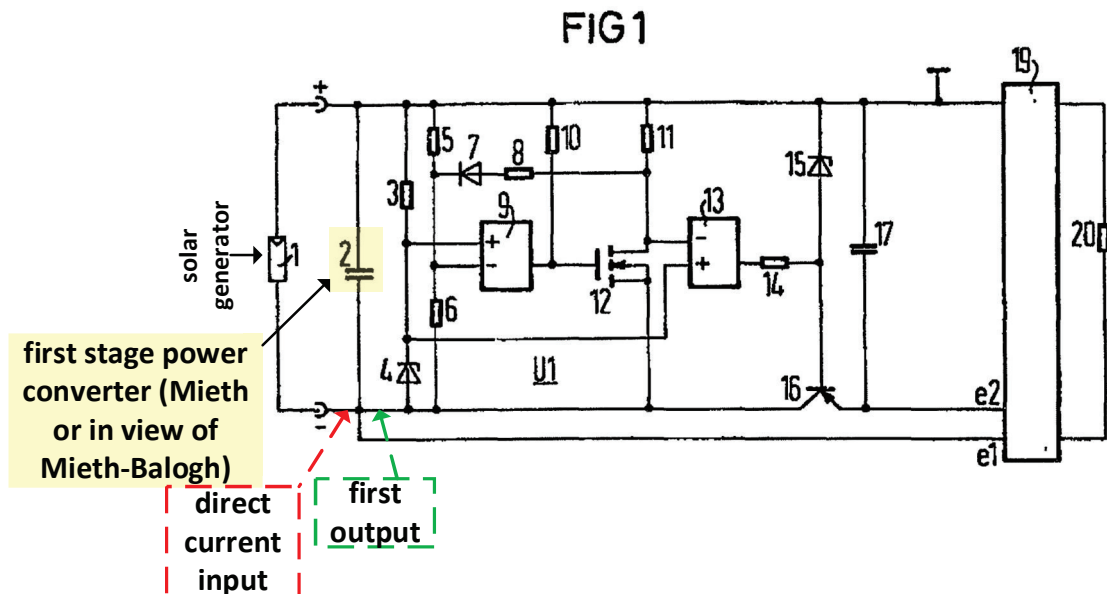


Fig. 32

172) Thus, Mieth or Mieth in view of Balogh teaches [10C].

- iv. [10D]: “a second stage power converter configured to be powered by the first output to generate a second output;”

173) In addition to the capacitor 2, Mieth further discloses a bipolar transistor 16 connected to a power supply apparatus 19 (blue), where the power supply apparatus 19 is a charging converter, as shown in Fig. 33 (Ex.1002 Fig.1. Ex.1002, 11:14-16, 8:29-35).

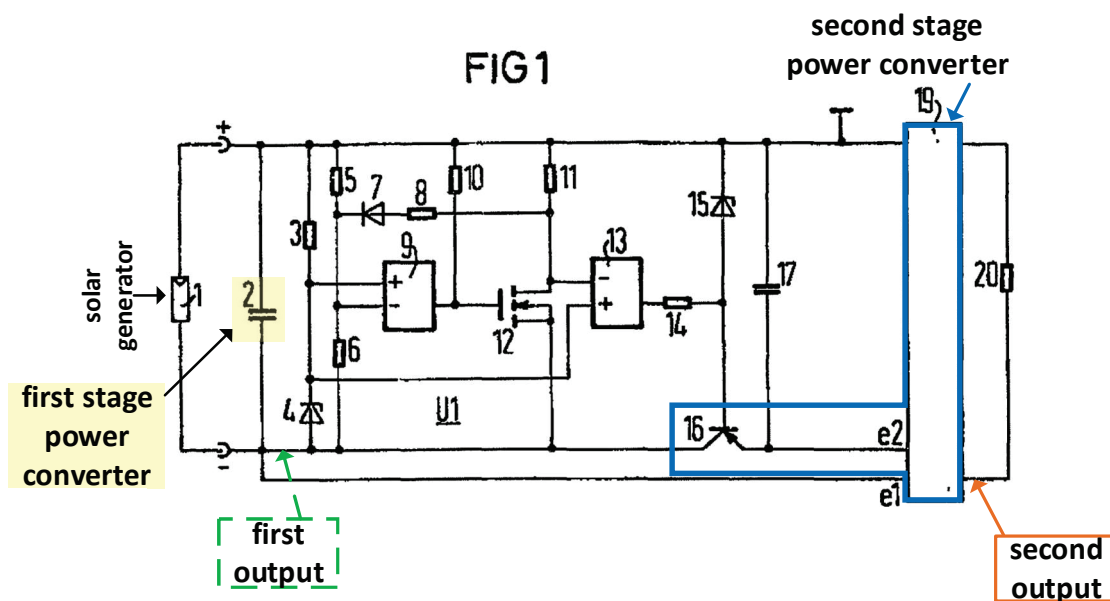


Fig. 33

174) Since the bipolar transistor 16 connected to the power supply apparatus 19 combination is a charging converter, the bipolar transistor 16/power supply apparatus 19 combination is analogous to the claimed *a second stage power converter*. The power supply apparatus 19 is connected to the first output (dashed-green) via bipolar transistor 16 by way of supply voltage input e2. Ex.1002, 8:29-35. The power supply apparatus 19 has an output that is connected to the load 20

based on the supply voltage input e2. *Id.* Since the power supply apparatus 19 output is based on the first output of capacitor 2 that provides voltage to the supply voltage input e2, the power supply apparatus 19 is ***configured to be powered by the first output*** as recited in [10D]. The output (orange) of the power supply apparatus 19 powers the load 20 and thus the output of the power supply apparatus 19 is analogous to the claimed ***second output***.

175) Additionally, [10D] is analogous to [1D], and thus Mieth-Balogh disclose [10D] for at least the same reasons described in conjunction with [1D] above.

176) Thus, Mieth teaches [10D].

v. **[10E]: “a micro-controller powered by the second output; a switchable load; and”**

177) Mieth shows the output (orange) of power supply apparatus 19 (blue) connected to a load 20 in Fig. 34 below (Ex.1002, Fig.1, 8:29-35.)

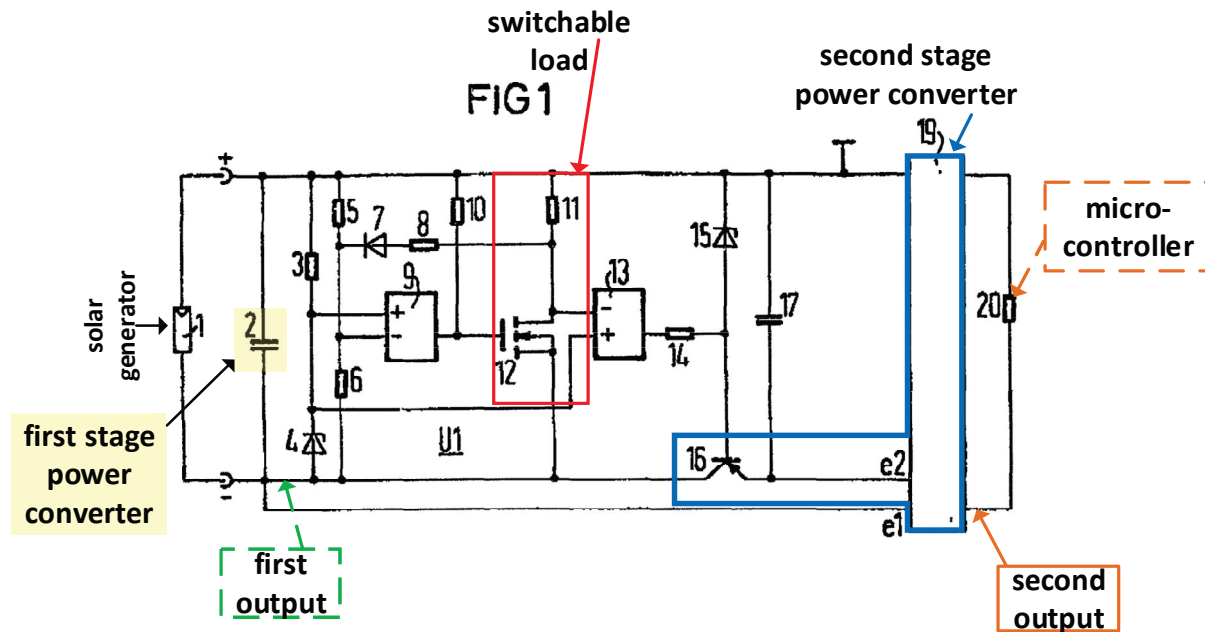


Fig. 34

178) A PHOSITA would understand that a load in a circuit can include a micro-controller, as such the load 20 is analogous to the claimed *micro-controller* (dashed-orange). See previous discussion of micro-controllers in conjunction with the Intel 8051 as discussed in paragraph 105. The load 20 is powered by the output of the power supply apparatus 19, thus the load 20 which can readily be a micro-controller is *powered by the second output* as recited in claim 10.

179) Mieth discloses that the output of the first comparator 9 is connected to a first electronic switch (field-effect transistor 12) that is connected in series to a preliminary load 11 as shown in Fig. 1. Ex.1002, 10:5-14. The field-effect transistor 12 can connect the preliminary load 11 to the first output of capacitor 2.

Ex.1002, 9:15-32. Thus, the field-effect transistor 12 and the preliminary load 11 in combination are analogous to the claimed *switchable load* (red).

180) Additionally, feature [10E] is analogous to the micro-controller of feature [1D] and the switchable load of feature [1E], and thus Mieth-Balogh discloses feature [10E] for at least the same reasons described in accordance with features [1D] and [1E].

181) Thus, Mieth teaches [10E].

- vi. [10F]: “a control circuit powered by the first output and configured to connect the first output to the switchable load to consume at least a portion of the first output while disabling the second stage power converter in supplying the second output to the micro-controller;”

182) Mieth discloses that the first output (dashed-green) of capacitor 2 (yellow) is connected to a first electronic switch (field-effect transistor 12) that controls a preliminary load 11 (switchable load-red) to consume some of the first output, while disabling the power supply apparatus 19, by turning the bipolar transistor 16 to an “off” state (second stage-blue), from supplying the output (orange) of the power supply apparatus 19 to the load 20 (dashed-orange), which is the same as [10F]. Fig. 35. Ex.1002 Fig. 1.

- vii. [10G]: “determine whether a voltage of the first output powering the switchable load is above a threshold during a time period in which the second output to the micro-controller is disabled; and”

185) Mieth discloses a first comparator 9 that compares a monitored voltage magnitude to a threshold voltage, and determines whether a voltage magnitude of the first output (dashed-green) of capacitor 2 (yellow) is above (*i.e.*, in voltage magnitude) a predefined minimum value while the circuit of Mieth is in the first state (highlighted-green), which is the same as [10G]. Fig. 36. Ex.1002; Fig. 1.

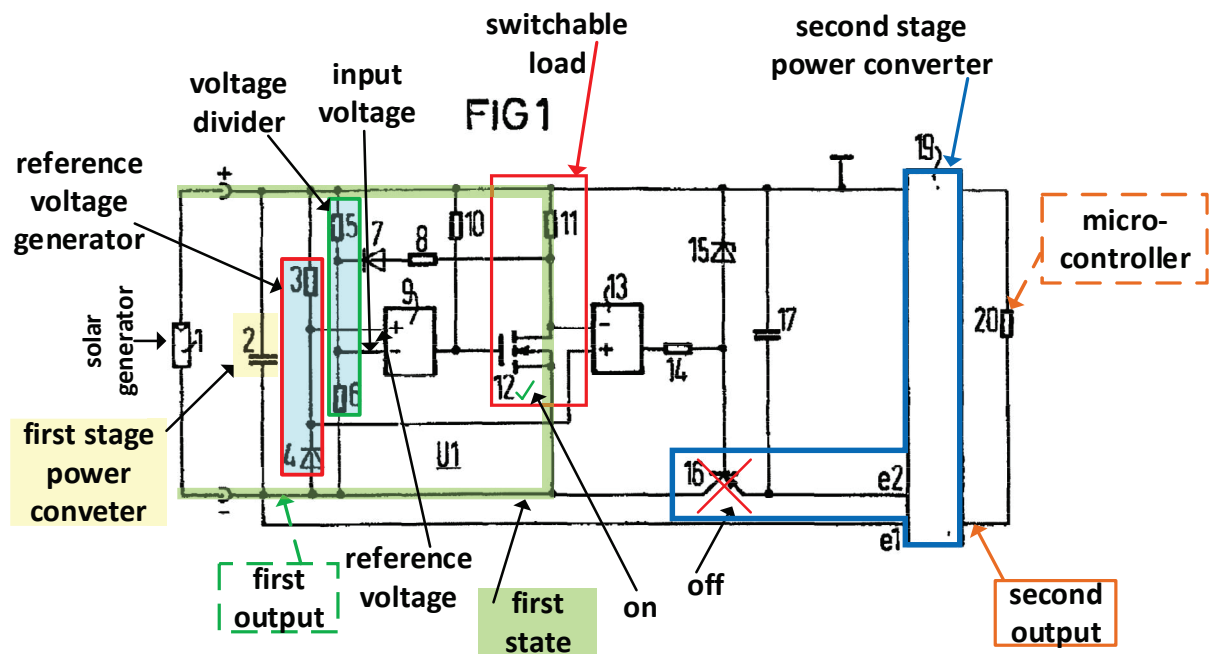


Fig. 36

186) Feature [10G] is analogous to the portion of feature [1G] that recites, “*in response to . . . the micro-controller is disabled,*” and thus Mieth-Balogh disclose [10G] for at least the same reasons described in accordance with feature [1G]. Feature [10G]

differs from feature [1G] by reciting “*a voltage of the first output powering the switchable load*” rather than “*the first output from the first stage powering the switchable load*”. A PHOSITA would understand that the first output of the capacitor 2 (i.e., first power converter) includes power defined by voltage and current (the voltage across a capacitor is proportional to the integral of the current through the capacitor, as appreciated by the well known relationship $v = \frac{1}{C} \int i dt$), thus the first output of capacitor 2 includes the claimed ***voltage of the first output powering the switchable load***.

187) Thus, Mieth teaches [10G].

viii. [10H]: “in response to the voltage being above the threshold during the time period in which the second output to the micro-controller is disabled, disconnect the switchable load from the first output of the first stage power converter”

188) The first comparator 9 of Mieth compares a monitored voltage magnitude to a threshold voltage derived from a reference voltage generator (highlighted-teal-outlined-red) and a voltage divider (highlighted-teal-outlined-green) to determine if the monitored voltage magnitude exceeds a threshold voltage magnitude defined by the voltage divider 5, 6, Zener diode 4, which is analogous to the claimed ***voltage being above the threshold***. Ex.1002, 12:12-26, Fig.1. In Figs. 36-37 provided herein, Fig. 36 illustrates the first state of Mieth, where the voltage provided at the first output is still below a threshold amount (e.g., the voltage

magnitude is below the threshold amount - predefined minimum value), while Fig. 37 shows the result of the monitored voltage associated with the first output exceeding the threshold (*e.g.*, voltage magnitude exceeding the threshold). Thus, Fig. 37, as annotated, does not illustrate the first state, but instead illustrates the second state of Mieth associated with “high” voltages at the first output.

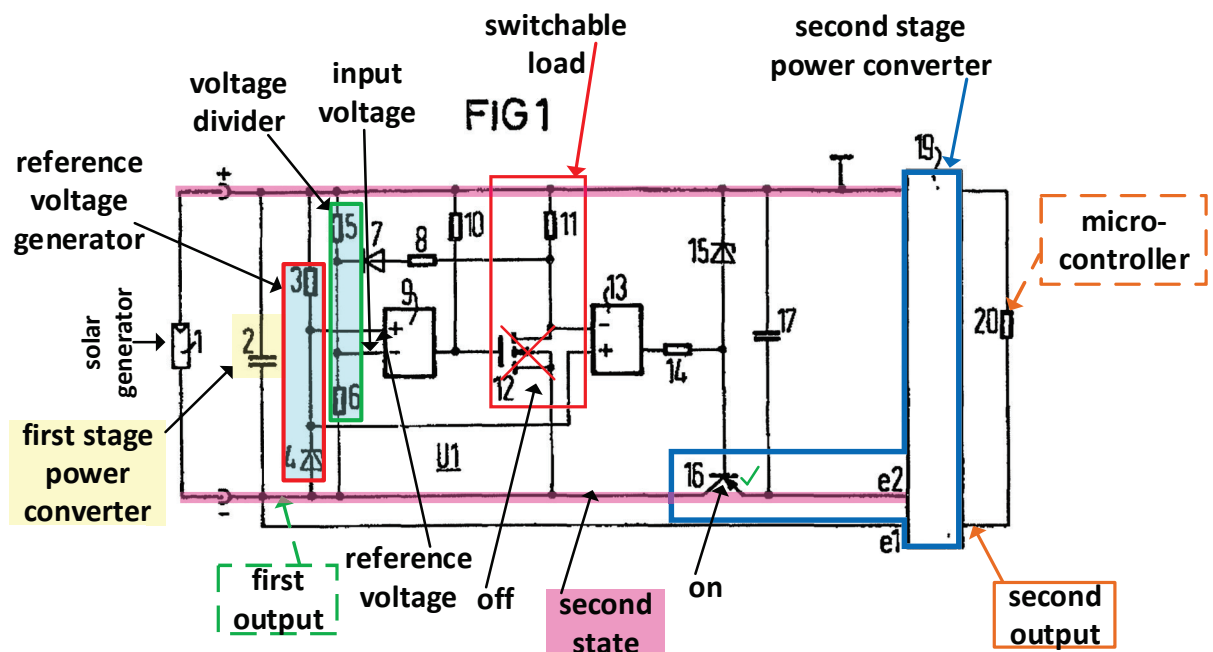


Fig. 37

189) The first state of Mieth shown in Fig. 36 concurrently disables the second output of the power supply apparatus 19 to the load 20 by turning the bipolar transistor 16 “off,” which is the same as the claimed *the second output to the micro-controller is disabled*. Ex.1002, 12:12-19. The time period the circuit of Mieth is in the first state is the same as the claimed *time period* and the predefined minimum value of Mieth is the same as the claimed *threshold*. Ex.1002, 9:15-26. The circuit of Mieth

is in the first state (e.g., Ex.1002, Fig.1) for the time period when the circuit determines whether the predefined minimum value is satisfied, which is equivalent to the claimed *the voltage being above the threshold during the time period in which the second output to the micro-controller is disabled.*

190) As shown in Fig. 37, when the predefined minimum value is satisfied, the circuit of Mieth operates in a second state (highlighted-pink) where the bipolar transistor 16 is “on” or conducting, causing the first output (dashed-green) of capacitor 2 to be connected to e2, thereby powering the power supply apparatus 19. Ex.1002, 10:16-29.

191) Furthermore, in the second state, the field-effect transistor 12 is “off” or non-conducting, thereby disconnecting the preliminary load 11 from the first output. *Id.* As discussed above, the first comparator 9 compares a reference voltage from a reference voltage generator (highlighted-teal-outlined-red) to a voltage from a voltage divider (highlighted-teal-outlined-green) to determine if the monitored voltage magnitude exceeds a threshold defined by the voltage divider 5, 6, and Zener diode 4. Ex.1002, 12:12-26. While in the first state, when the first output of capacitor 2 rises and the monitored voltage magnitude across voltage divider 5, 6 is above the threshold (i.e., “predefined minimum value” as quoted by Mieth), the circuit disconnects the preliminary load 11 from the first output by configuring the field-effect transistor 12 to an “off” state, which is the same as the claimed

disconnect the switchable load from the first output of the first stage power converter. Id.

192) When the circuit of Mieth is in the first state, the circuit makes a determination that the predefined minimum value is satisfied while the second stage is disabled, and in response changes to the second state, which is analogous to the claimed *in response to the voltage being above . . . the micro-controller is disabled, disconnect the switchable load . . .* Ex.1002, 9:15-23.

193) Additionally, feature [10H] is analogous to the portion of feature [1G] that recites, “*disconnecting the switchable load from the first output of the first stage,*” and thus Mieth-Balogh disclose [10H] for at least the same reasons described in accordance with feature [1G].

194) Thus, Mieth teaches [10H].

ix. [10I]: “and signal the second stage power converter to enable the second output to the micro-controller using power from the first output of the first stage power converter.”

195) As shown in Fig. 37 above and as described in the reference, Mieth discloses that the bipolar transistor 16 (see Ex.1002, Fig.1 (annotated-10G)) connects the power supply apparatus 19 to the first output of capacitor 2, which results in the second output of the power supply apparatus 19 powering the load 20, and is the same as the claimed *and signal the second stage power converter to enable the second*

output to the micro-controller using power from the first output of the first stage power converter.

196) Additionally, feature [10I] is analogous to the portion of feature [1G] that recites, “and instructing . . . of the first stage,” and thus, Mieth-Balogh disclose feature [10I] for at least the same reasons Mieth discloses feature [1G].

197) As such, Mieth teaches [10I]. Additionally, Mieth anticipates each and every feature of claim 10 or the combination of Mieth and Balogh render obvious each and every feature of claim 10.

4. Dependent Claim 11

198) As discussed above, claim 10 is disclosed by Mieth and Balogh. ¶¶ 164-197. Claim 11 depends from claim 10 and requires [11A], “wherein the control circuit comprising: a hysteresis amplifier configured to receive the first output and generate a first control signal for the switchable load.” Ex. 1001, claim 11.

199) As shown in Fig. 38 below. (Ex.1002, Fig. 1), Mieth discloses a capacitor 2 (highlighted-yellow) analogous to the claimed first power converter and outputs a first output (dashed-green) analogous to the claimed first output, and this capacitor 2 can be modified by Balogh to be a first power converter. Mieth also discloses a first comparator 9 (dashed-blue) that is analogous to the claimed hysteresis amplifier that outputs a first signal (highlighted-purple) analogous to the claimed first signal that teach [11A] as discussed further below.

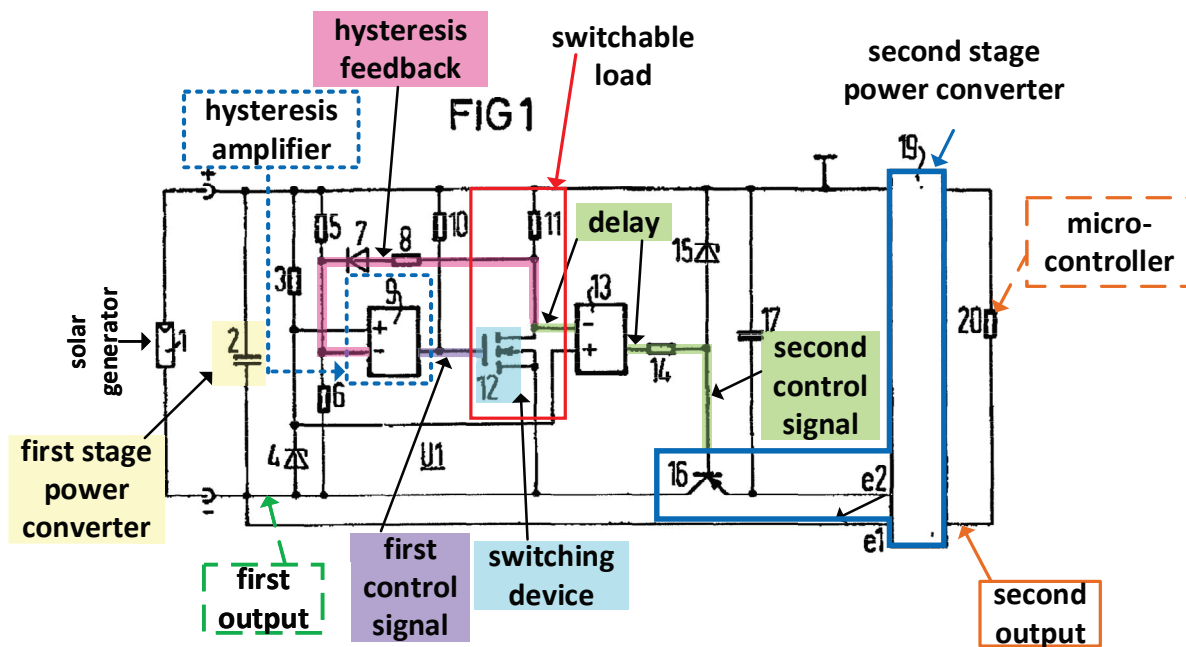


Fig. 38

200) Feature [11A] recites hysteresis, which a PHOSITA would understand is a positive feedback loop between the output of a device and an input of a device, such as an amplifier or comparator, to mitigate instability in switched signals. A PHOSITA would further understand that an amplifier can be configured as a comparator, and thus the first comparator 9 can be an amplifier. The first comparator 9 is configured with hysteresis where the hysteresis feedback path (highlighted-pink) from the output of the switching device (field-effect transistor 12) is connected to the negative input of the first comparator 9 through resistor 8 and diode 7.

Ex.1002, 9:34-38. Furthermore, Mieth recites that “Hysteresis is achieved by means of the resistor 8.” Ex.1002, 12:26-27. Specifically, when the switch 12 is off, the series circuit comprising resistors, 8, 11 and diode 7 are in parallel with

resistor 5 forming a voltage divider with resistor 6. When the switch 12 is on, diode 7 is off and no current flows through resistor 8 leaving only resistors 5 and 6 to form the voltage divider. For more details regarding the hysteresis of Mieth, see ¶¶ 77-82 above. In this way the comparator 8 and associated circuitry exhibit hysteretic behavior. Since the first comparator 9 can be an amplifier with a positive feedback loop, the first comparator 9 is the same as the claimed *hysteresis amplifier*.

201) Additionally, the hysteresis amplifier of claim 11 is analogous to the hysteresis amplifier of feature [5A] and thus the comparator 9 of Mieth discloses the claimed hysteresis amplifier for at least the same reasons described above in accordance with feature [5A].

202) The first output of the capacitor 2 is represented at the negative input of the first comparator 9 through a voltage divider defined by resistors 5 and 6 in addition to resistors 8 and 11 and diode 7 when comparator 9 output is low, which is analogous to the claimed *hysteresis amplifier configured to receive the first output*. Ex.1002, 9:34-38. The output of the first comparator 9 is a first signal as discussed previously (e.g., claim 3 recites “first signal” which is analogous to claim 11’s “first control signal”), and is analogous to the claimed recitation *generate a first control signal*. Specifically, since the output of the first comparator 9 turns the field-effect transistor 12 “on” and “off”, a PHOSITA would

understand that the output is analogous to the claimed *first control signal* as the output from the first comparator 9 operates the field-effect transistor 12 just as the claimed first control signal for the claimed switchable load.

203) A PHOSITA would understand that the circuitry of Mieth, that includes the first comparator 9, is analogous to the claimed *control circuit* as the first comparator 9 generates the first control signal that controls the field-effect transistor 12. Thus, Mieth teaches [11A].

204) Claim 11 further requires feature [11B], “a delay circuit to generate a second control signal for the second stage power converter by delaying the first signal.”

205) Mieth discloses delaying the first control signal from the first comparator 9 to generate a second control signal from the output of the field-effect transistor 12 to enable the load 20. Mieth discloses that the field-effect transistor 12 and a comparator 13 (hereinafter the second comparator 13) are a delay circuit that generates a second control signal (highlighted-green) that is input to the bipolar transistor 16/power supply apparatus 19 (second stage-blue) by delaying the first signal from the first comparator 9, which is analogous to the features of [11B] as discussed below. Ex.1002, Fig.1, 11:4-12, 12:12-19.

206) The bipolar transistor 16 operates as a switch that can connect the first output to the power supply apparatus 19. Ex.1002, 10:31-36. The base of the bipolar transistor 16, which controls the conducting or non-conducting state of the bipolar

transistor 16, is controlled by the output of the second comparator 13. Ex.1002, 10:36-11:12. The second comparator 13 outputs the second control signal based on an input from the field-effect transistor 12, where the input from the field-effect transistor 12 is itself based on the first control signal. *Id.* As such, the state of the second control signal is dictated by the state of the first control signal, and the transition of the second control signal occurs in response to the first control signal, and thus is delayed with respect to the transition of the first control signal by the transistor 12 and the second comparator 13, which is analogous to the claimed ***delaying the first signal***. Claim 11 does not provide antecedence for “the first signal,” which is interpreted herein as the “first control signal” as presented in [11A]. The second comparator 13 generates the second control signal based on the first control signal, which is analogous to the claimed ***to generate a second control signal***, and the second signal controls the bipolar transistor 16 which is analogous to the claimed ***for the second power converter***. A PHOSITA would understand that the field-effect transistor 12 and the second comparator 13 that delays the first control signal is analogous to the claimed ***a delay circuit to generate***.

207) Additionally, feature [11B] is analogous to feature [5B], and thus, Mieth-Balogh disclose feature [11B] for at least the same reasons Mieth discloses feature [5B].

208) Thus, Mieth teaches [11B] and all the features of claim 11.

5. Dependent Claim 12

209) Claim 11 is disclosed by Mieth and Balogh. ¶¶ 198-208. Claim 12 depends from claim 11 and requires [12A], “wherein in response to the voltage going above the threshold: the first control signal causes the switchable load to be disconnected from the first output of the first stage power converter.” Ex.1001, claim 12.

210) As discussed in ¶¶ 188-192, the circuit of Mieth shows first comparator 9 that compares a reference voltage from a reference voltage generator (highlighted-teal-outlined-red) to a voltage from a voltage divider (highlighted-teal-outlined-green) to determine if the monitored voltage magnitude exceeds a predefined minimum value defined by the voltage divider 5, 6, and Zener diode 4 (e.g., voltage magnitude exceeding the predefined minimum value), which is analogous to the claimed *wherein in response to the voltage going above the threshold*. Fig. 39. Ex.1002, 12:12-26; Fig.1.

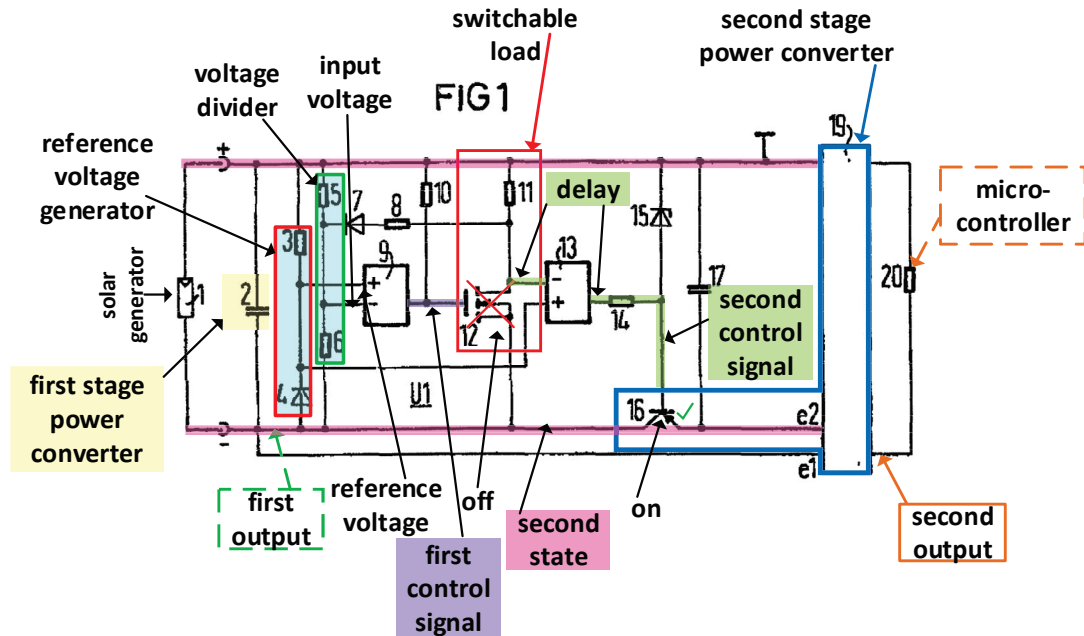


Fig. 39

211) The first comparator 9 outputs a first control signal (highlighted-purple) to the field-effect transistor 12 and preliminary load 11 (switchable load-red) that turns the field-effect transistor 12 “off” by outputting a low or zero voltage (e.g., corresponding to high voltages at the first output and thus the second state-highlighted-pink). Ex.1002, 12:12-30. When the field-effect transistor 12 is “off”, the preliminary load 11 is disconnected from the first output of capacitor 2 (first stage power converter-highlighted-yellow). *Id.* As such, the first comparator 9 outputting the first control signal that turns off the field-effect transistor 12 to disconnect the preliminary load 11 from the first output of the capacitor 2 is analogous to the claimed *the first control signal causes the switchable load to be disconnected from the first output of the first stage power converter.*

212) Thus, Mieth teaches [12A].

213) Claim 12 further requires [12B], “the second control signal causes the second stage power converter to enable the second output to the micro-controller.”

214) Mieth discloses that the field-effect transistor 12 is connected to the second comparator 13 and delays the first signal from the first comparator 9 to generate a second control signal (**highlighted-green**) that turns on the bipolar transistor 16.

Ex.1002, 11:1-12. When bipolar transistor 16 turns on, the first output is connected to the e2 input to energize the power supply apparatus 19 (second stage-**blue**) which enables the second output (**orange**) of the power supply apparatus 19 to power the load 20 (micro-controller-**dashed-orange**), which is analogous to the features of [12B] as discussed below. Ex.1002, Fig. 1, 11:4-12, 12:12-19.

215) The bipolar transistor 16 operates as a switch that can connect the first output to the power supply apparatus 19. Ex.1002, 10:31-36. The base of the bipolar transistor 16, which controls the conducting or non-conducting state of the bipolar transistor 16, is controlled by the second comparator 13. Ex.1002, 10:36-11:12. The second comparator 13 outputs the second control signal based on an input from the field-effect transistor 12, where the input from the field-effect transistor 12, when it turns off, “trips” the second comparator 13. *Id.* The second comparator 13 generates the second control signal based on the first control signal which is analogous to the claimed *second control signal*, and the second control signal

controls the bipolar transistor 16 which is analogous to the claimed *cause the second stage power converter stage . . .*

216) When the power supply apparatus 19 is powered, the second output is enabled to the load 20. Ex. 1002, 8:29-35. The bipolar transistor 16 of Mieth turned on by the second control signal, which enables the second output to the load 20, is analogous to the claimed *second control signal . . . enable the second output to the micro-controller*.

217) Thus, Mieth-Balogh disclose [12B] and all of claim 12, and therefore is obvious in view of a combination of Mieth and Balogh in view of its dependency of claim 11.

6. Dependent Claim 15

218) Claim 12 is disclosed by Mieth and Balogh. Claim 15 depends from claim 12 and requires [15A], “wherein the switchable load comprises: a resistive device; and a switching device connected to the resistive device”. Ex.1001, claim 15.

219) As shown below in Fig. 40 (Ex.1002 Fig. 1) and disclosed by Mieth, preliminary load 11 (**highlighted-orange**) can be a resistor. Ex.1002, 12:14-20 (“preliminary load formed by the resistor 11”). Since the preliminary load 11 can be a resistor, and a resistor is a resistive device, preliminary load 11 of Mieth is analogous to the *resistive device* of claim 15.

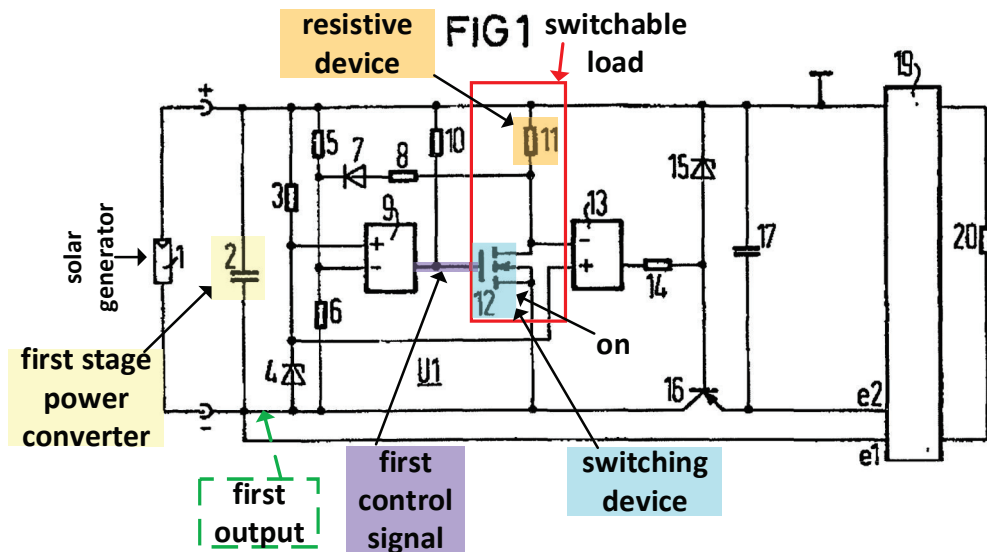


Fig. 40

220) As shown in Fig. 40, a field-effect transistor 12 (highlighted-teal) is connected to the preliminary load 11. Ex.1002, 10:5-14. Mieth describes the field-effect transistor 12 as a first electronic switch, and thus a PHOSITA would understand that the field-effect transistor 12 is a switching device. Ex.1002, 10:5-14. As such, the field-effect transistor 12 is analogous to the *switching device* of claim 15 and the field-effect transistor 12 connected to the preliminary load 11 is *analogous to feature [15A]*.

221) Additionally, feature [15A] is analogous to features [2A]-[2B], thus, Mieth-Balogh disclose feature [15B] for at least the same reasons Mieth discloses features [2A]-[2B] as discussed previously.

222) Claim 15 further requires [15B], “wherein the switching device is configured to be turned on to be connected to the first output to consume the portion of the first

output and turned off to be disconnected from the first stage.” Ex.1001, claim 15.

Feature [15B] from claim 15 is the same as feature [2C] from claim 2, and thus Mieth-Balogh discloses feature [15B] for the same reasons that Mieth discloses feature [2C]. The field-effect transistor 12 connects or disconnects the preliminary load 11 from the first output according to the first state or the second state, respectively, which is the same as [15B].

223) Claim 15 further requires [15C], “wherein the first control signal is connected to control the switching device.” Ex.1001, claim 15. The output (highlighted-purple) of the first comparator 9 is a first signal as discussed previously in accordance with claim 3 (e.g., claim 3 recites “first signal”), and is analogous to the claimed recitation ***first control signal***. The output of the first comparator 9 turns the field-effect transistor 12 “on” and “off,” thus a PHOSITA would understand that the output of the comparator 9 controls the field-effect transistor 12. Thus, the output of the comparator 9 that turns the field-effect transistor 12 “on” and “off” is analogous to the claimed ***first control signal is connected to control the switching device***.

224) As such, Mieth-Balogh disclose all the features of claim 15.

7. Dependent Claim 16

225) Claim 15 is disclosed by Mieth and Balogh. Claim 16 depends from claim 15 and requires, “wherein the switching device includes one of: a field effect transistor

(FET), a metal-oxide-semiconductor field-effect-transistor (MOSFET), and a bipolar junction transistor.” Ex.1001, claim 15.

226) As discussed in accordance with claim 6, the field-effect transistor 12 (highlighted-teal) is analogous to the *switching device*. See Ex.1002, Fig. 1. The field-effect transistor 12 is the same as the claimed *field effect transistor (FET)*. Claim 16 is the same as claim 6, and thus Mieth-Balogh disclose claim 16 for the same reasons that Mieth discloses claim 6. As such, Mieth teaches all the features of claim 16.

8. Dependent Claim 17

227) Claim 16 is disclosed by Mieth and Balogh. Claim 17 depends from claim 16 and requires, “wherein when the switch device is turned on, the switchable load and an input of the second stage are connected in parallel to the first output of the first stage.” Ex.1001, claim 15.

228) Claim 17 is the same as claim 7, and thus Mieth-Balogh disclose claim 17 for the same reasons that Mieth discloses claim 7.

9. Independent Claim 18

229) With reference to the claim listing appendix, Mieth discloses elements [18A]-[18I]. As explained below, a PHOSITA would have been motivated to combine together Mieth and Balogh to arrive at the alleged invention of claim 18.

i. [18A]: “A system to supply power, the system comprising:”

230) Mieth discloses a circuit that supplies power to an electrical load from a solar generator. Ex.1002, 8:8-9. A PHOSITA would understand that when the circuit of Mieth supplies power to the electrical load, the circuit is supplying power which is the same as the claimed *system to supply power*.

231) Additionally, feature [18A] is identical to feature [10A]. Thus, Mieth discloses feature [18A] for at least the same reasons as Mieth discloses [10A].

232) Thus, Mieth disclose feature [18A].

ii. [18B]: “a photovoltaic panel to provide a direct current input”

233) The circuit of Mieth discloses a solar generator 1, as shown in Fig. 41 (Ex.1002 Fig.1). Ex.1002, 4:29-32. As a PHOSITA, I understand that the solar generator 1 produces a direct current from a solar source such as the sun. As a PHOSITA, I further understand that a photovoltaic panel generates power from solar energy sources like the sun, thus the solar generator 1 of Mieth is analogous to the claimed *photovoltaic panel*. Since the solar generator 1 produces a direct current from a solar source, the direct current output from the solar generator 1 is analogous to the claimed *to provide a direct current input*.

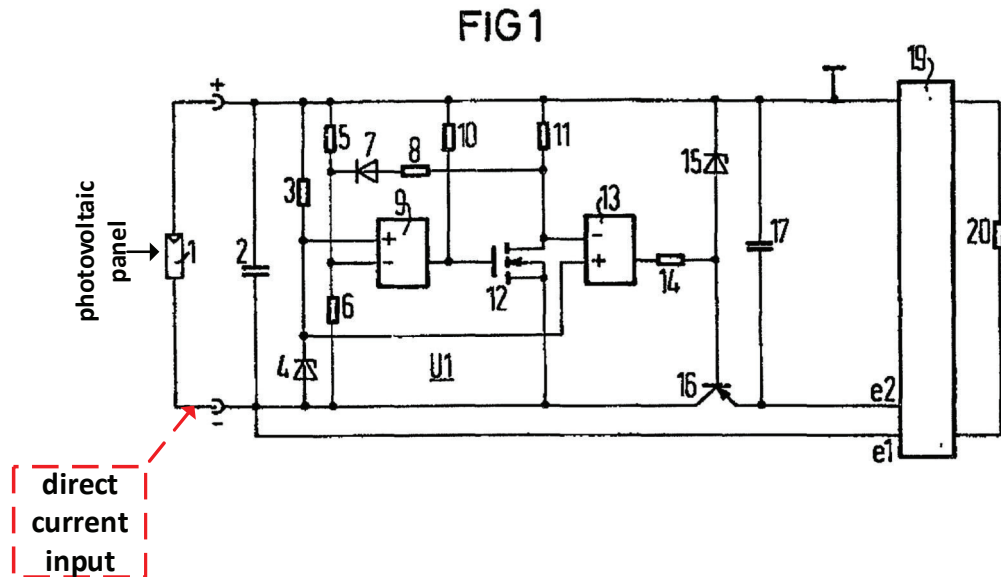


Fig. 41

234) Additionally, feature [18B] is essentially the same as feature [10B], as such, Mieth discloses feature [18B] for at least the same reasons Mieth disclose feature [10B].

235) Thus, Mieth discloses feature [18B].

iii. [18C]: “a first stage power converter connected to the photovoltaic panel to generate a first output from the direct current input”

236) The circuit of Mieth discloses a capacitor 2 connected in parallel with the solar generator 1. Ex.1002, Fig.1. As discussed in accordance with feature [1C] above, capacitor 2 converts power and thus the capacitor 2 of Mieth teaches a *first stage power converter*. Thus, the capacitor 2 of Mieth is anticipatory of claim 18 for the same reasons discussed in accordance with feature [1C]. Specifically, the capacitor 2 can stabilize the voltage across it (at the first output) due to fluctuations from the direct current input. As discussed *supra* in accordance with feature [10G],

the first output of capacitor 2 is converted according to the direct current input by the well known relationship $v = \frac{1}{c} \int idt$. While Mieth teaches a first stage power converter, Balogh also discloses a first stage power converter and a PHOSITA would have been motivated to combine Mieth and Balogh for at least the reasons described in accordance with features [1B]-[1D] of claim 1 as discussed in paragraphs 151-162 and 168-175 above and in accordance with claim 8 as discussed in paragraph 163 above.

237) Balogh's isolated DC-DC converter (yellow) is a step-down converter and thus analogous to the claimed *first stage power converter* as shown in Fig. 42 (Ex.1003, Fig.1D, 2:61-64.

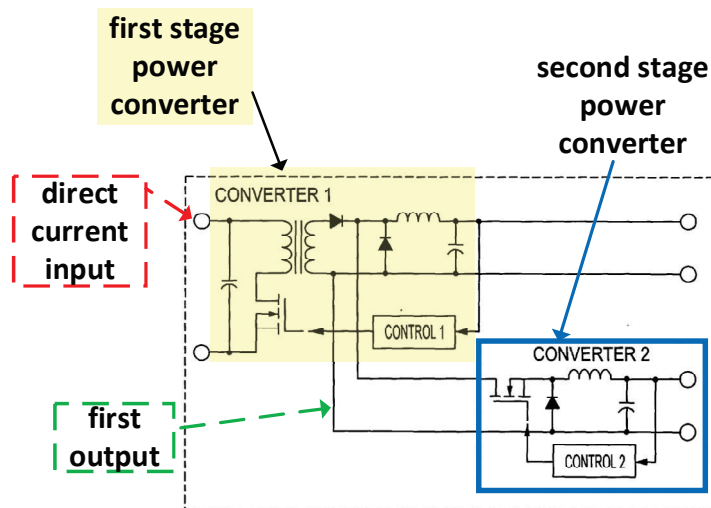


FIG. 1D
PRIOR ART

Fig. 42

238) The isolated DC-DC converter shows a capacitor in parallel with a transformer that converts the direct current input (**dashed-red**) to a first output (**dashed-green**).

Ex.1003, Fig. 1D. A PHOSITA would have been motivated to add a transformer after the capacitor 2 of Mieth to realize the power converter of Balogh to convert the direct current input into a first output. ¶¶ 151-162. Since the isolated DC-DC converter converts power from the direct current input to a first output, the isolated DC-DC converter is analogous to the claimed *first stage power converter* and the power converted by the DC-DC converter is analogous to the claimed *convert the direct current input into a first output*.

239) Since the capacitor 2 of Mieth can be replaced or supplemented with the DC-DC converter of Balogh, further discussion of Mieth will refer to capacitor 2 as analogous to the first stage power converter in view of Balogh for ease of discussion as shown below in Fig. 43. Ex.1002, Fig. 1.

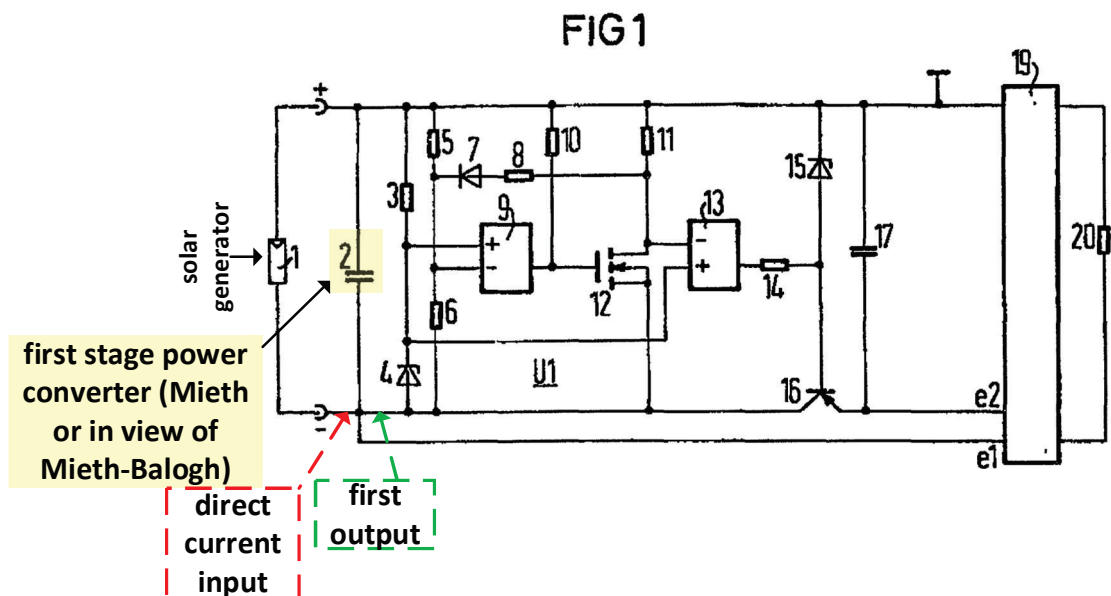


Fig. 43

240) Since the capacitor 2 of Mieth can be replaced or supplemented with the DC-DC converter of Balogh to convert power and could be connected in parallel with the solar generator 1 of Mieth, the capacitor 2 combined with the DC-DC converter of Balogh is analogous to the claimed **a *first stage power converter connected to the photovoltaic panel***. Since capacitor 2 can be combined with the DC-DC converter of Balogh to convert power from the output of the solar generator 1, the capacitor 2 in combination with the DC-DC converter of Balogh is analogous to the claimed **convert the direct current input** and the output of capacitor 2 is analogous to the claimed **into a first output**.

241) Additionally, feature [18C] is analogous to feature [10C]. Thus, Mieth-Balogh disclose feature [18C] for at least the same reasons described in accordance with feature [10C].

242) Thus, Mieth or Mieth-Balogh disclose feature [18C].

iv. [18D]: “a second stage power converter connected to convert the first output to a second output”

243) In addition to the capacitor 2, Mieth further discloses a bipolar transistor 16 connected to a power supply apparatus 19 (blue), where the power supply apparatus 19 is a “charging converter,” or a “DC-DC voltage converter” as shown in Fig. 44 (Ex.1002 Fig.1); Ex.1002, 11:14-16, 8:29-35.

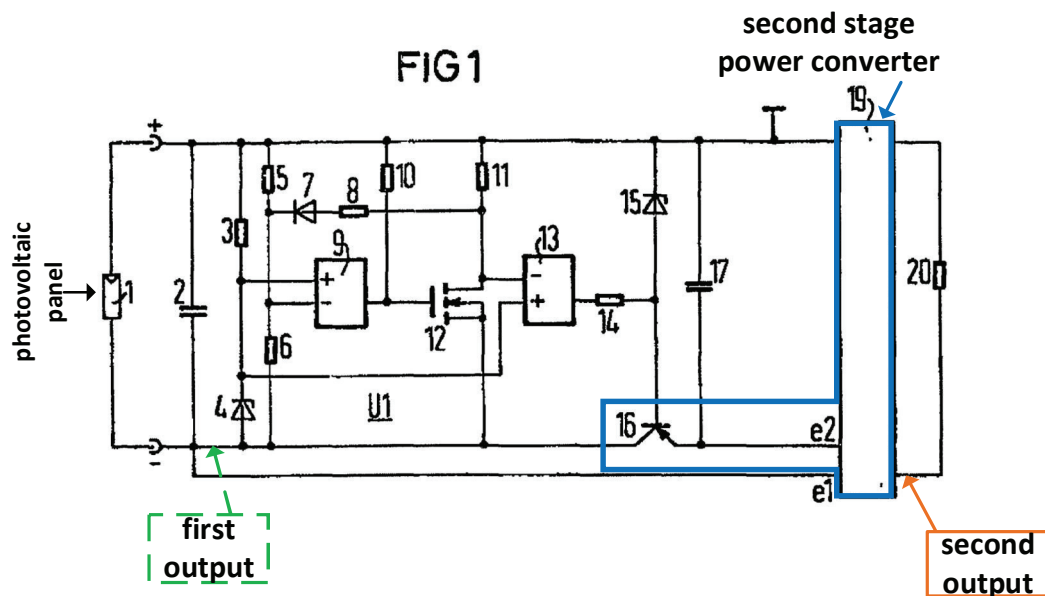


Fig. 44

244) Since the bipolar transistor 16 connected to the power supply apparatus 19 is the “charging converter,” the bipolar transistor 16/power supply apparatus 19 combination (blue) is analogous to the claimed *a second stage power converter*. The power supply apparatus 19 is connected to the first output (dashed-green) by bipolar transistor 16 by way of supply voltage input e2. Ex.1002, 8:29-35. Since

the power supply apparatus 19 is a converter, the power supply apparatus 19 converts the first output of capacitor 2 into an output, which is analogous to the claimed *connected to convert the first output to a second output*. The output (orange) of the power supply apparatus 19 powers the load 20 and thus the output of the power supply apparatus 19 is analogous to the claimed *second output*.

245) Additionally, feature [18D] is analogous to feature [1D]. Thus, Mieth-Balogh disclose feature [18D] for at least the same reason Mieth discloses feature [1D].

246) Thus, Mieth or Mieth-Balogh disclose feature [18D].

v. [18E]: “a micro-controller”

247) Mieth shows the output (orange) of power supply apparatus 19 (blue) connected to a load 20 in Fig. 45 (Ex.1002, Fig.1); Ex.1002, 8:29-35.

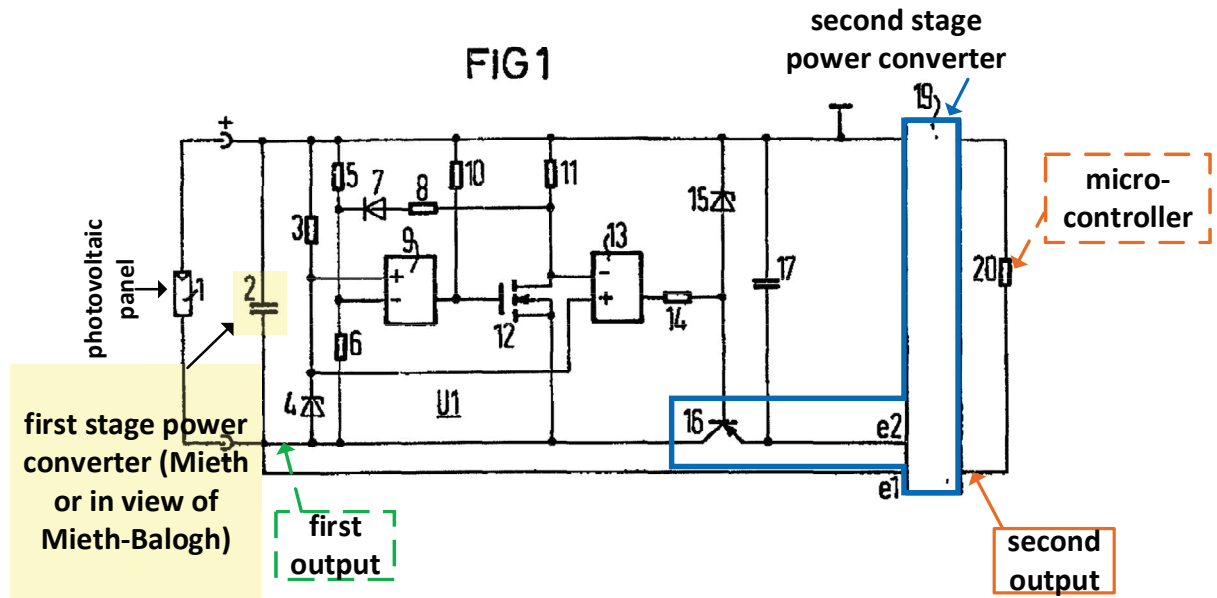


Fig. 45

248) As a PHOSITA I understand that a load on the output of a solar generator 1 circuit can include a micro-controller, and that micro-controllers regularly operate as loads in circuits such as that disclosed in Mieth. As such, the load 20 is analogous to the claimed *micro-controller* (dashed-orange).

249) Additionally, feature [18E] is analogous to the micro-controller of feature [1D]. Thus, Mieth discloses feature [18E] for at least the same reasons Mieth discloses [1D].

250) Thus, Mieth discloses feature [18E].

vi. [18F]: “a power absorption circuit”

251) Mieth discloses that the first output (dashed-green) of capacitor 2 (yellow) is connected to a first electronic switch (field-effect transistor 12) that is connected to a preliminary load 11 as shown in Fig. 46 (Ex.1002 Fig.1). Ex.1002, 10:5-14.

Furthermore, the preliminary load 11 is described as a “resistor 11,” and a PHOSITA would understand that a resistor absorbs power. Ex.1002, 12:12-19. The field-effect transistor 12 can connect the preliminary load 11 to the first output of capacitor 2. Ex.1002, 9:15-32. Thus, the field-effect transistor 12 and the preliminary load 11 in combination are analogous to the claimed *power absorption circuit* (red).

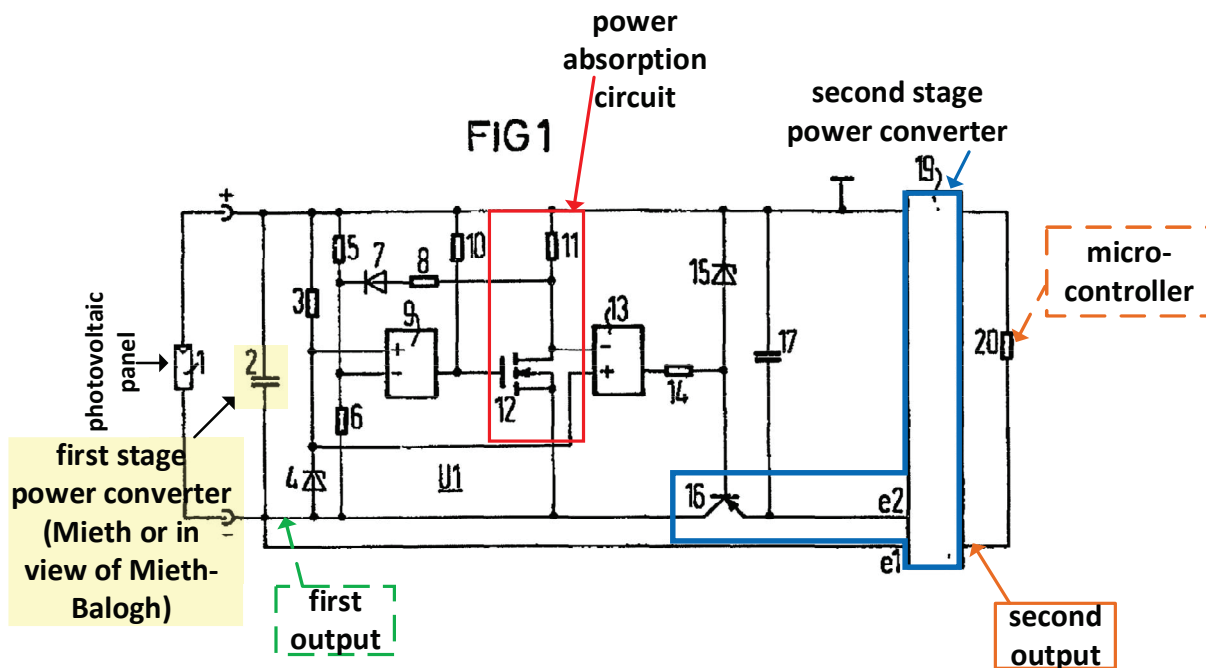


Fig. 46

252) Additionally, feature [18F] is analogous to the “switchable load” of feature [1F] as such, Mieth discloses feature [18F] just as Mieth discloses feature [1F].

253) Thus, Mieth discloses feature [18F].

- vii. **[18G]: “a control circuit coupled with the first stage power converter and the second stage power converter, the control circuit powered by the first output to control the second stage power converter”**

254) Mieth discloses a comparator 9 (hereinafter the first comparator 9) that turns the field-effect transistor 12 “on” (conducting) or “off” (non-conducting) as shown in Fig. 47 (Ex.1002 Fig.1). Ex.1002, 9:34-10:14.

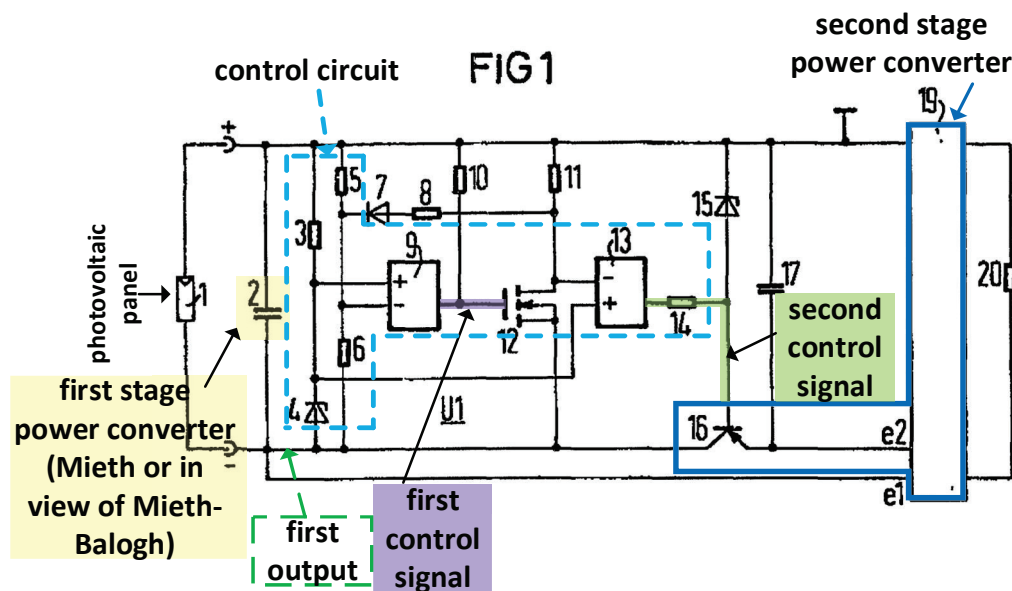


Fig. 47

255) The first comparator 9 compares a reference voltage from a reference voltage generator connected to a positive terminal of the first comparator 9 to a voltage from a voltage divider connected to a negative terminal of the first comparator 9. Ex.1002, 9:34-10:3. The reference voltage generator is defined by the Zener diode 4. *Id.* The voltage divider is defined by the voltage divider 5, 6 *Id.* The first comparator 9 compares the monitored voltage magnitude to the threshold voltage

defined by voltage divider 5, 6, and Zener diode 4 (see ¶ 80) to determine if the monitored voltage magnitude exceeds the threshold voltage and the first comparator 9 outputs a first control signal (**highlighted-purple**) to field-effect transistor 12 based on the comparison. Ex.1002, 12:12-26.

256) A PHOSITA would understand that the circuitry (**dashed-blue**) that controls the field-effect transistor 12, which includes the first comparator 9, voltage divider 5, 6 and reference input generator 3, 4, which are powered by the first output from the capacitor 2, is analogous to the claimed **a control circuit coupled with the first stage power converter** and the claimed **the control circuit powered by the first output**. Ex.1002, 9:34-10:3.

257) The first control signal that is output from first comparator 9 controls the field-effect transistor 12, and the output of the field-effect transistor 12 is used by comparator 13 (hereinafter second comparator 13) to generate a second control signal (**highlighted-green**). Ex.1002, 11:4-12, 12:12-19. The second control signal that is output from the second comparator 13 operates a bipolar transistor 16, thereby turning the bipolar transistor “on” or “off” which connects or disconnects the power supply apparatus 19 (combined with bipolar transistor 16 to be the second stage power converter- **blue**) from the first output. *Id.* When the first control signal is low or zero voltage, the field effect-transistor 12 is “off” and the second comparator 13 outputs a low voltage which turns bipolar transistor 16 “on,”

thereby connecting the power supply apparatus 19 to the first output of capacitor 2. Ex.1002, 12:12-30. When the first control signal is high, the field effect-transistor 12 is “on” which connects preliminary load 11 to the first output of capacitor 2, and the second comparator 13 outputs a high voltage which turns bipolar transistor 16 “off,” thereby disconnecting the power supply apparatus 19 from the first output of capacitor 2. Ex.1002, 9:15-23, 12:12-30.

258) Since the first comparator 9 generates the first control signal that controls the bipolar transistor 16/power supply apparatus 19 through the field effect-transistor 12 and the second comparator, Mieth discloses the claimed *to control the second stage power converter*. Furthermore, the first comparator 9 couples to the bipolar transistor 16/power supply apparatus 19 through the field effect-transistor 12 and the second comparator, which is analogous to the claimed *a control circuit coupled with . . . the second stage power converter*.

259) Thus, Mieth discloses feature [18G].

- viii. [18H]: “when the second stage power converter is disabled in providing the second output to the micro-controller, the control circuit monitors a voltage of the first output powering the power absorption circuit and signals the second stage power converter to continue disabling the providing of the second output to the micro-controller during a time period in which the voltage is below a threshold;”

260) As shown in Fig. 48 (Ex.1002 Fig. 1), the circuit of Mieth can be configured in a first state (highlighted-pink) where the bipolar transistor 16 is “off” and the power

262) Furthermore, in the first state, the field-effect transistor 12 is turned “on” and the first output powers the preliminary load 11 (power absorption circuit-**red**).

Ex.1002, 10:5-14. The first comparator 9 (control circuit-**dashed-blue**) turns the field-effect transistor 12 “on” based on a comparison of a threshold voltage defined by voltage divider 5, 6, and Zener diode 4 with the monitored voltage magnitude.

See ¶80. Ex. 1002, 9:34-10:3. The first comparator 9 that connects the preliminary load 11 to the first output through control of the field-effect transistor 12 based on the monitored voltage of the first output is analogous to the claimed ***the control circuit monitors a voltage of the first output powering the power absorption circuit.***

263) The monitored voltage magnitude is compared to a “predefined minimum value,” (related to a predefined threshold voltage) and during a time period when the monitored voltage magnitude is lower than the predefined minimum value, the first control signal from the first comparator 9 is a high voltage which turns the field-effect transistor 12 “on.” Ex.1002, 11:4-12, 12:12-26. The time period in which the monitored voltage is lower than the predefined minimum value is analogous to the claimed ***during a time period in which the voltage is below a threshold.***

264) When the field-effect transistor 12 is “on,” the preliminary load 11 is connected to the first output of capacitor 2, which signals a high voltage at the negative terminal of the second comparator 13, which signals a high voltage to the bipolar transistor

16, thereby turning the power supply apparatus 19 “off” which disables the second output from powering the load 20. Ex.1002, 9:15-23, 12:12-30. Therefore, first comparator 9 turning the field-effect transistor 12 “on” signals the power supply apparatus 19 to be turned “off” through bipolar transistor 16, thereby disabling the second output from powering the load, which is analogous to the claimed *signals the second stage power converter to continue disabling the providing of the second output to the micro-controller.*

265) Thus, Mieth discloses feature [18H].

- ix. [18I]: “when the voltage is above the threshold, the control circuit signals the second stage power converter to enable the providing of the second output to the micro-controller”

266) As shown in Fig. 49 (Ex.1002 Fig.1), the circuit of Mieth can be configured in a second state (highlighted-pink) where the bipolar transistor 16 is “on” and the power supply apparatus 19 (second stage-blue) is connected to the first output of capacitor 2 (i.e., first stage-highlighted-yellow). Ex.1002, 12:12-30.

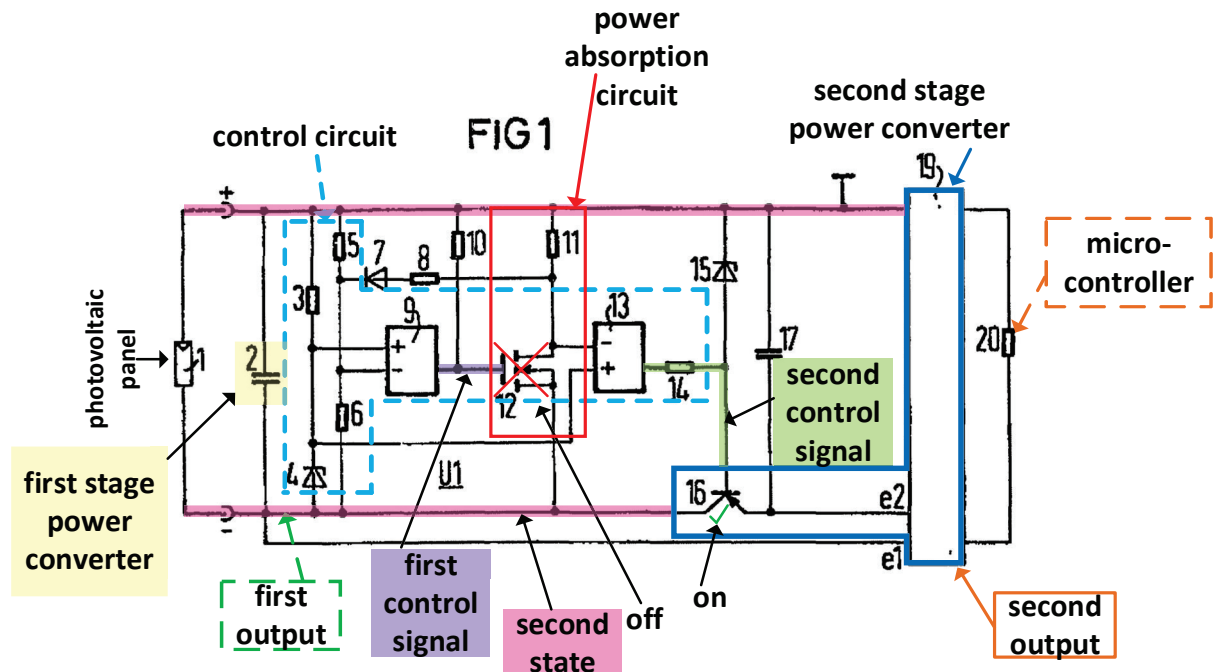


Fig. 49

267) The first comparator 9 (part of control circuit-dashed-blue) turns the field-effect transistor 12 “off” when the monitored voltage magnitude representative of the first output (dashed-green) voltage exceeds the threshold voltage. See ¶80, Ex.1002, 9:34-10:3. The monitored voltage magnitude is compared to the “predefined minimum value,” and when the monitored voltage magnitude is higher than the predefined minimum value (*i.e.*, threshold voltage magnitude), the first control signal from the first comparator 9 is a low voltage, which turns the field-effect transistor 12 “off.” Ex.1002, 11:4-12, 12:12-26. The time period when the monitored voltage magnitude at the first comparator 9 is above the predefined

minimum value is analogous to the claimed *when the voltage is above the threshold*.

268) When the field-effect transistor 12 is “off,” the preliminary load 11 is disconnected from the first output of capacitor 2, which signals a low voltage at the negative terminal of the second comparator 13, which signals a low voltage to the bipolar transistor 16, thereby turning the power supply apparatus 19 “on” which enables the second output (orange) to power the load 20 (micro-controller-dashed-orange).

Ex.1002, 9:15-23, 12:12-30. The first comparator 9 disconnecting the preliminary load 11 from the first output, which signals the second comparator 13 to turn on the bipolar transistor, thereby powering the second output of the power supply apparatus 19 to the load 20 is analogous to the claimed *the control circuit signals the second stage power converter to enable the providing of the second output to the micro-controller*.

269) Additionally, feature [18I] is analogous to the portion of feature [1G] that recites, “in response to . . . is above the threshold,” and “instructing the second stage to enable the second output to the micro-controller.” Thus, Mieth-Balogh disclose feature [18I] for at least the same reasons Mieth discloses feature [1G].

270) Thus, Mieth discloses feature [18I].

271) As each of the elements of claim 18 are disclosed by Mieth or a combination of Mieth and Balogh, and claim 18 is anticipated by Mieth or obvious in view of Mieth and Balogh.

10. Dependent Claim 20

272) Claim 18 is disclosed by Mieth and Balogh. Claim 20 depends from claim 18 and requires [20A], “wherein the power absorption circuit comprises a switchable load” Ex.1001, claim 20.

273) Mieth discloses a field-effect transistor 12 and a preliminary load 11, where the preliminary load 11 is connected or disconnected from the first output of capacitor 2 which is analogous to the claimed *switchable load*. Thus, Mieth-Balogh disclose feature [20A]. Furthermore, feature [20A] is analogous to the “*switchable load*” of feature [1F] as such, Mieth-Balogh discloses [20A] just as Mieth discloses [1F] as discussed above.

274) Claim 20 further requires [20B], “and the control circuit signals the switchable load to be in a first state to consume a portion of the first output when the voltage is below the threshold.” Ex.1001, claim 20.

275) Mieth discloses that the first comparator 9 (i.e. part of control circuit) signals the field-effect transistor 12 in a first state (e.g., see Fig. 48) such that the preliminary load 11 consumes a portion of the first output of capacitor 2 when a monitored

voltage of the first comparator 9 is lower than a predefined minimum value, which is analogous to the features of [20B]. See paragraphs 260-264 above.

276) Additionally, feature [20B] is analogous to the “*switchable load to consume . . . of the first output*” of features [1E]-[1F] as such, Mieth-Balogh disclose feature [20B] just as Mieth discloses features [1E]-[1F]. See paragraphs 106-112 above.

277) Thus, Mieth-Balogh disclose feature [20B].

278) Claim 20 further requires [20C], “and to be in a second state not to consume a portion of the first output when the voltage is above the threshold.” Ex. 1001, claim 20.

279) Mieth discloses that the first comparator 9 signals the field-effect transistor 12 in a second state such that the preliminary load 11 is disconnected from the first output of capacitor 2 when the monitored voltage at the first comparator 9 is above the predefined minimum value, thus the preliminary load 11 does not consume the first output, which is analogous to the features of [20C]. *Supra*, § VII.B.9.viii.

280) Additionally, feature [20C] is analogous to the “*is above the threshold . . . disconnecting the switchable load*” of feature [1G]. Thus, Mieth-Balogh disclose feature [20C] just as Mieth discloses feature [1G].

281) Thus, Mieth-Balogh disclose all of claim 20, and based on its dependence upon claim 18, is taught by a combination of Mieth and Balogh.

**C. Ground C: Obviousness of claims 13 and 14 in view of Mieth, Balogh,
and further in view of Nishi**

1. Dependent Claim 13

282) Claim 12 is taught by Mieth and Balogh. Claim 13 depends from claim 12 and requires, “wherein the micro-controller is configured to maximize power generated by the power source.”

283) Mieth discloses a circuit that supplies power to an electrical load from a solar generator, such as load 20 and the solar generator 1 in Fig. 49 above. Ex.1002, 8:8-9,20-27. A PHOSITA would understand that the solar generator 1 generates power and is analogous to the claimed *power source*. Nishi (Ex.1004) discloses a microcomputer 109 that controls input voltage so that output power from a solar cell array is maximized, which is analogous to the features of claim 13 as discussed further below. Ex.1004, ¶¶ 8, 98.

284) Fig. 50 (Ex.1004, Figs.2, 7) below shows solar cell arrays 2A-2D connected to converters 5A-5D and controlled by an inverter 6, where an input voltage to the inverter 6 (i.e., output voltage of converters 5A-5D) is controlled so that the output power from the solar cell arrays 2A-2D is maximized. Ex.1004, ¶¶ 96-98.

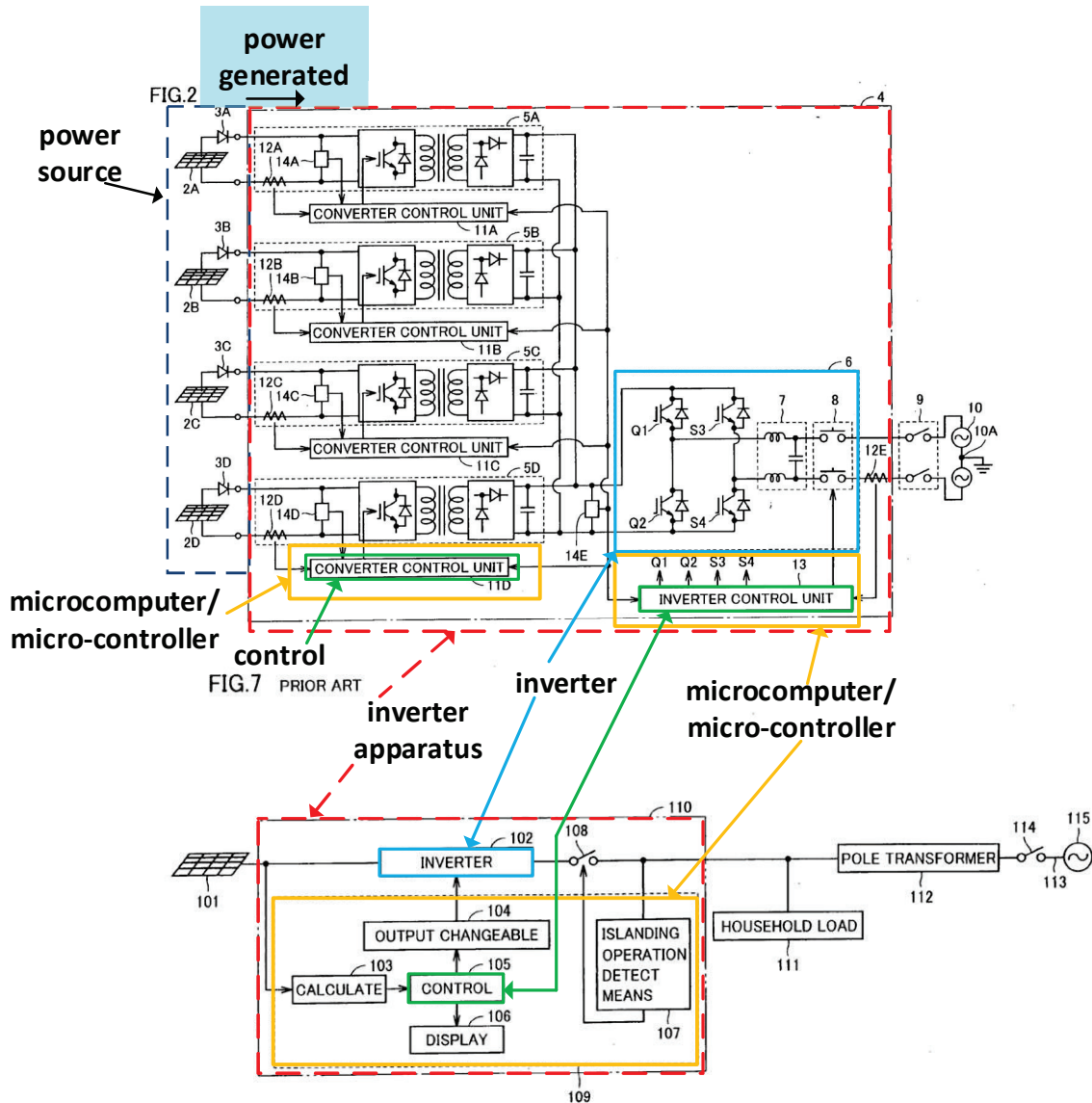


Fig. 50

285) A PHOSITA would understand that the solar cell arrays 2A-2D (dashed-black) generate power and thus the solar cell arrays 2A-2D are analogous to the claimed **power source** and further analogous to the solar generator 1 of Mieth. Further, a PHOSITA would understand that the power generated (highlighted-teal) by the solar cell arrays 2A-2D is analogous to the claimed **power generated by the power**

source, and further analogous to the output of the solar generator 1 of Mieth. The inverter 6 (**blue**) changes an output current of the inverter 6 in accordance with a pulse width modulation (PWM) control signal from inverter control unit 13 (**green**). Ex.1004, ¶¶ 70, 83-84. Inverter control unit 13 controls the PWM control signal based on an input and output of the inverter 6 (e.g., voltage sensor 14E and current sensor 12E), to realize a desired input voltage of inverter 6. Ex.1004, ¶ 88. Further, the inverter control unit 13 operates converter control units 11A-11D based on the input and output of inverter 6 to realize the desired input voltage of inverter 6. Ex.1004, ¶¶ 83-84, 97. Subsequently, the converter control units 11A-11D to adjust a pulse width of a pulse frequency modulation (PFM) to the converters 5A-5D such that the “output power from a corresponding solar cell array becomes maximum” Ex.1004, ¶ 98.

286) Nishi discloses, in Fig. 7, that an inverter apparatus (**dashed-red**) can include an inverter 102 (**blue**), and a microcomputer 109 (**orange**), where the microcomputer 109 can have control means 105 (**green**). Ex.1004, ¶ 8. The inverter 6, inverter control unit 13, converter control units 11A-11D and converters 5A-5D are all part of an inverter apparatus (**dashed-red**) of Nishi-Fig. 2 and analogous to the inverter apparatus of Nishi-Fig. 7. As such, the inverter 6 of Nishi-Fig. 2 is analogous to the inverter 102 of Nishi-Fig. 7. Nishi-Fig. 2 shows that control circuitry 105 can be implemented in a microcomputer, thus inverter control unit 13 (**green**) and

converter control units 11A-11D (green), which are analogous to control 105, can be implemented in a microcomputer (orange). Each system shows an inverter apparatus 4 and 110 that includes both inverter circuitry (6 in Fig.2, 102 in Fig.7 of Nishi) and a micro-computer 109 that includes control circuitry 105, as discussed in conjunction with Fig.7, or is simply shown as control units 11 and 13 in Fig. 2. Ex.1004, ¶¶[8], [88]. A PHOSITA appreciates that a micro-computer is the same as a micro-controller. For example, Nishi, which predates the effective filing date of the '021 patent, recites in paragraph [0008] that, “Microcomputer 109 is formed of calculate means 103, output changeable means 104, control means 105, display means 106, and islanding operation detect means 107.” Paragraph [0008] of Nishi references Fig. 7 which shows microcomputer 109 with a control 105 function. Nishi further recites at paragraph [0013] that control means 105 provides several functions including receiving a generation value, tracking voltage, controlling other devices such as changeable means 104, the display 106, etc... As such, “control” is a function that a micro-computer provides, and thus “control” would be understood at the time of filing as a function provided by micro-computers. As such, the claimed micro-controller would be understood by a PHOSITA at the time of filing as analogous to a microcomputer, or a device that provides controlling functionality within a circuit, as disclosed in Nishi.

287) As a PHOSITA, I understand that a microcomputer is analogous to a micro-controller, and thus the inverter control unit 13 and the converter control units 11A-11D of Nishi can be microcomputers and are analogous to the claimed ***micro-controller***. Since inverter control unit 13 is controlling inverter 6 to maximize the output power from the solar array, the features of Nishi are analogous to the claimed ***micro-controller is configured to maximize power generated by the power source***.

288) Nishi discloses an inverter apparatus with a microcomputer that maximizes the output power of a solar cell array. Ex.1004, ¶¶ 8, 85, 96-98. Mieth discloses a solar generator 1 analogous to the solar cell array of Nishi, where the solar generator 1 connects to a load 20 that is analogous to the inverter apparatus of Nishi. Ex. 1002, 4:29-32, 8:29-35. It is well known to a PHOSITA that solar systems that include solar panels and loads with inverters benefit from maximum power point tracking (MPPT) to maximize the power generated from a solar array. Ex.1004, ¶ 30. Thus it would have been obvious to a PHOSITA to combine the reliable startup circuit of Mieth with the maximum power point tracking configuration of Nishi to realize the features of claim 13, as the MPPT microcomputer is a simple substitution of elements with the load 20 of Mieth. As a simple substitution of elements, a reasonable expectation of success exists, and no undue technical hurdles are needed to be overcome. Thus, such a combination of prior art is proper.

289) Thus, Mieth in combination with Balogh and Nishi disclose the features of claim 13.

2. Dependent Claim 14

290) Claim 13 is taught by the combination of Mieth, Balogh, and Nishi. See paragraphs 282-289 above. Claim 14 depends from claim 13 and requires, “wherein the power source comprises a photovoltaic panel; the first stage power converter comprises a first step-down converter; and the second stage power converter comprises a second step-down converter.”

291) Mieth discloses a solar generator 1 which a PHOSITA would understand can include a photovoltaic panel, as the claimed *photovoltaic panel* generates power from solar energy sources like the sun. Ex. 1002, 8:8-9. Furthermore, Nishi discloses solar cell arrays 2A-2D which are understood by a PHOSITA to be the claimed *power source comprises a photovoltaic panel*. Ex.1004, ¶ 60.

292) As discussed above in paragraphs 151-162, a PHOSITA would have been motivated to combine the cascaded power converter architecture of Balogh with the switchable load features of Mieth. As discussed in above, Mieth discloses a capacitor 2 which is analogous to the claimed *first stage* and discloses power supply apparatus 19 connected to the bipolar transistor 16 which is analogous to the claimed *second stage*. The power supply apparatus 19 is a DC-DC voltage converter or charging converter which a PHOSITA would understand can step-

down DC power and is analogous to the claimed *second stage comprising a step-down converter*. Ex.1002, 8:29-35. Balogh teaches a first stage and a second stage that can each comprise step-down converters. Ex.1003, 1:29-36. Balogh teaches that a cascaded arrangement can include a first buck converter and a second buck converter where a buck converter steps an input voltage down to an output voltage that is lower than the input voltage. *Id.* It would be obvious to a PHOSITA to modify the capacitor 2 of Mieth with the step-down converter from Balogh to realize the claimed *first stage power converter comprises a first step-down converter; and the second stage power converter comprises a second step-down converter*.

293) Thus, the combination of Mieth-Nishi-Balogh teaches the features of claim 14.

D. Ground D: Obviousness of Claim 19 in view of Mieth, Balogh, and further in view of Liu

294) Claim 18 is taught by the combination of Mieth and Balogh. Claim 19 depends from claim 18 and requires [19A], “wherein the power absorption circuit includes a capacitor coupled to the first output.”

295) Mieth discloses a field-effect transistor 12 connected to a preliminary load 11 to form the claimed *power absorption circuit coupled to the first output* as discussed above in paragraphs 251-252; Fig. 46. Additionally, Liu (Ex.1005) discloses a capacitor as a power absorption circuit coupled to the first output, and a PHOSITA

would have been motivated to combine Mieth and Liu for at least the following reasons.

296) As shown in Fig. 51 below (Ex.1005 Fig. 5), Liu discloses cascaded DC voltage converters with an input stage 50 separated from an output stage 60 by a reservoir capacitor 58. Ex. 1005, 4:25-35.

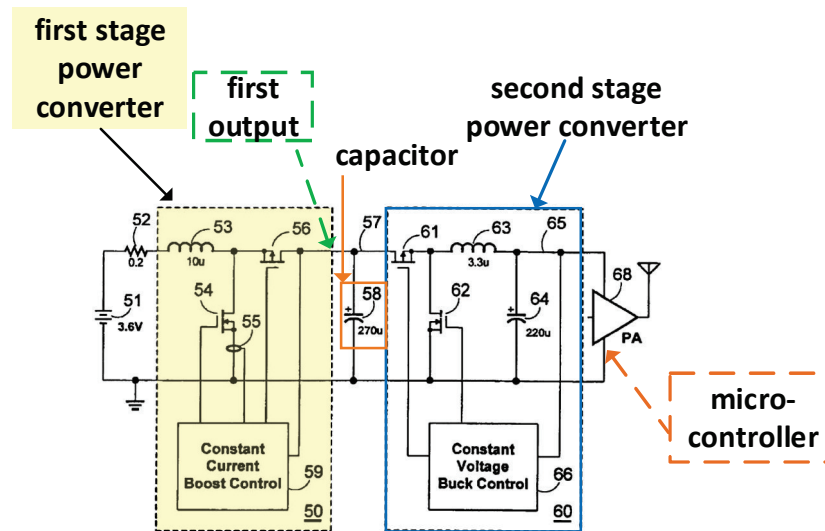


Fig. 51

297) The input stage 50 boosts (i.e., converts) the voltage from battery 51 to charge reservoir capacitor 58, and the output stage 60 down converts the voltage of the reservoir capacitor 58 to power a power amplifier (“PA”) 68. Ex.1005, 4:36-43.

Since the input stage 50 (highlighted-yellow) converts an input voltage to an output voltage, the input stage 50 is analogous to the claimed first stage power converter of claim 18, and the output (dashed-green) of the input stage 50 is analogous to the claimed *first output* of claim 19. Since the reservoir capacitor 58 (orange) is charged from the first output of the input stage 50, the reservoir

capacitor 58 absorbs the first output of the input stage 50 and is analogous to the claimed *power absorption circuit includes a capacitor coupled to the first output*.

Thus Liu discloses [19A].

298) Claim 19 further requires 19B, “and the threshold allows the capacitor to power the second stage to operate the micro-controller for a predetermined period of time even without the output of the first stage.” It is noted that neither claims 18 or 19 provide antecedence for the terms “first stage” and “second stage” and thus are interpreted to mean the “first stage power converter” and “second stage power converter” respectively as recited in claim 18.

299) It is unclear to a PHOSITA how the claimed “threshold” can allow a capacitor to power the second stage as a threshold is understood to be a value or a level and not a circuit component or connection between circuit components such as a capacitor, a control circuit, or the like. For the purposes of interpretation, the claimed threshold that allows the capacitor to power the second stage is interpreted as meaning, “when the voltage (of claim 18) is above the threshold, the capacitor powers the second stage . . .” As such, the capacitor that powers the second stage is charged to the threshold voltage that is capable to provide power to the second stage and operate the micro-controller for a predetermined period of time without the output of the first stage.

300) Liu teaches that the reservoir capacitor 58 provides most of the energy to PA 68 through the output stage 60 for a period of time when the battery 51 cannot supply power to the pulsating load requirement of PA 68. Ex.1005, 1:8-12, 4:43-51. A PHOSITA would understand that the capacitor 58 could provide all of the power to the PA 68 for a predetermined period of time by sizing the capacitor appropriately. Furthermore, where Liu shows a PA 68 powered by the reservoir capacitor 58 through the output stage 60, a PHOSITA would understand that the reservoir capacitor 58 and output stage 60 could power another load such as the claimed micro-controller, thus the PA 68 is analogous to the claimed *micro-controller*. Thus, the capacitor 58 that can provide power to the PA 68 for a period of time is analogous to the claimed *capacitor to power the second stage to operate the micro-controller for a predetermined period of time even without the output of the first stage*.

301) Liu discloses cascaded power converters with a capacitor, where the capacitor provides power to a load through a second power converter for a period of time without incoming power from a first power converter. Ex.1005, 4:36-43. Mieth teaches the use of a power absorption circuit in situations where an input voltage to a power converter varies, such as the voltage from a photovoltaic system that will vary depending upon the time of day, or weather conditions. Ex.1002, 5:22-38. The circuit of Mieth disconnects the switchable load located between a first stage

power converter and a second stage power converter when the input voltage to the first stage power converter meets a stable criteria according to a voltage threshold.

Id. A PHOSITA would have been motivated to combine the capacitor of Liu with the power absorption circuit of Mieth, as the capacitor of Liu would provide the benefit of a more stable power source to the load of Mieth for a predetermined period of time when the power absorption circuit of Mieth is disconnected from the circuit and voltage from the photovoltaic system is varying due to dynamic conditions.

302) As such, a PHOSITA would be motivated to employ known means in the art, such as that taught in Liu, to modify the circuit of Mieth (*e.g.*, Fig. 1) such that when the reference voltage connected to comparator 9 satisfies the predefined minimum value according to the output of capacitor 2 (*i.e.*, the first stage power converter), the capacitor of Liu powers the load 20 (*i.e.*, micro-controller) through the power supply apparatus 19 (*i.e.*, the second stage power converter) for a predetermined period of time even without the first output of capacitor 2, ***which is analogous to [19B]***. Therefore, the teaching of both Mieth and Liu provide an express motivation to improve a cascaded power converter system by including a capacitor in the power absorption circuit. A PHOSITA would thus have been motivated to use a cascaded power converter system with capacitor between the cascaded converters taught in Liu with the application of Mieth.

303) The combination of Mieth and Liu merely involves combining known prior-art elements (replacing or combining Mieth's resistive load between converters with Liu's capacitive load between converters) according to known methods to yield predictable results, a cascaded step power converter having a capacitive load at the second power converter input. A PHOSITA would have had the skills, knowledge, and motivation to carry out the combination. A PHOSITA would have reasonably expected success in combining Mieth and Liu. *Id.* As understood by a PHOSITA, there would have been no undue technical hurdles to applying Mieth with Liu, as such a combination would have been a simple modification to Mieth's system, readily accomplished by a PHOSITA.

304) Thus, the combination of Mieth and Liu discloses feature [19B].

305) As such, the combination of Mieth, Balogh, and Liu make obvious the features of claim 19.

VIII. CONCLUDING STATEMENT

306) In conclusion, as set forth above, claims 1-20 of the '021 patent are unpatentable as anticipated or rendered obvious by the aforementioned prior art references.

307) Under penalty of perjury, all statements made herein of my own knowledge are true, and I believe that all statements made herein on information and belief to be true. I have been warned and I am aware that willful false statements are punishable by fine or imprisonment or both under Section 1001 of Title 18 of the United States Code. In signing this Declaration, I understand that the Declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of 12 the United States Patent and Trademark Office. I acknowledge that I may be subject to cross-examination in the case and that cross-examination will take place in the United States. If cross examination is required of me, I undertake to appear within the United States during the time allotted for cross-examination, and within the limits of my ability so to do. I declare under penalty of perjury that the foregoing is true and correct.

A handwritten signature in black ink, appearing to read "Hanyu H. Hanyu". The signature is fluid and cursive, with the first name "Hanyu" and last name "Hanyu" clearly distinguishable.

Executed on April 21, 2023.

IV. CLAIM LISTING APPENDIX

U.S. Patent No. 9,584,021 - Avrutsky	
Claim Element Designation	Claim Element
Claim 1	
[1A]	A method to supply power,
[1B]	the method comprising: providing a power supply having a first stage and a second stage,
[1C]	wherein the first stage converts power from a direct current input into a first output,
[1D]	and the second stage powered by the first output has a second output for a micro-controller;
[1E]	connecting the first output of the first stage to a switchable load to consume at least a portion of the first output while disabling the second stage in supplying the second output to the micro-controller;
[1F]	determining whether the first output from the first stage powering the switchable load is above a threshold during a time period in which the second output to the micro-controller is disabled; and
[1G]	in response to a determination that the first output from the first stage powering the switchable load is above the threshold during the time period in which the second output to the micro-controller is disabled, disconnecting the switchable load from the first output of the first stage; and instructing the second stage to enable the second output to the micro-controller using power from the first output of the first stage.
Claim 2	
[2A]	The method of claim 1, wherein the switchable load comprises: a resistive device; and
[2B]	a switching device connected to the resistive device,
[2C]	wherein the switching device is configured to be turned on to be connected to the first output to consume the portion of the first output and turned off to be disconnected from the first stage.
Claim 3: The method of claim 2, wherein the disconnecting of the switchable load from the first output of the first stage comprises sending a first signal to the switching device to turn off the switching device.	
Claim 4	

[4A]	The method of claim 3, further comprising: generating the first signal based on the determining of whether the first output from the first stage powering the switchable load is above the threshold; and
[4B]	delaying the first signal to generate a second signal to the second stage, the second signal enabling the second output to the micro-controller.
Claim 5	
[5A]	The method of claim 4, further comprising: providing a control circuit comprising: a hysteresis amplifier configured to receive the first output of the first stage and generate the first signal; and
[5B]	a delay circuit to generate the second signal according to the first signal.
Claim 6: The method of claim 3, wherein the switching device includes one of: a field effect transistor (FET), a metal-oxide-semiconductor field-effect-transistor (MOSFET), and a bipolar junction transistor.	
Claim 7: The method of claim 6, wherein when the switch device is turned on, the switchable load and an input of the second stage are connected in parallel to the first output of the first stage.	
Claim 8: The method of claim 1, wherein the first stage comprises a first step-down converter; and the second stage comprises a second step-down converter.	
Claim 9: The method of claim 1, wherein the disconnecting is performed prior to the instructing of the second stage to enable the second output to the micro-controller.	
Claim 10	
[10A]	A system to supply power, the system comprising:
[10B]	a power source to provide a direct current input;
[10C]	a first stage power converter configured to convert the direct current input into a first output;
[10D]	a second stage power converter configured to be powered by the first output to generate a second output;
[10E]	a micro-controller powered by the second output; a switchable load; and
[10F]	a control circuit powered by the first output and configured to connect the first output to the switchable load to consume at least a portion of the first output while disabling the second stage power converter in supplying the second output to the micro-controller;
[10G]	determine whether a voltage of the first output powering the switchable load is above a threshold during a time period in which

	the second output to the micro-controller is disabled; and
[10H]	in response to the voltage being above the threshold during the time period in which the second output to the micro-controller is disabled, disconnect the switchable load from the first output of the first stage power converter
[10I]	and signal the second stage power converter to enable the second output to the micro-controller using power from the first output of the first stage power converter.
Claim 11	
[11A]	The system of claim 10, wherein the control circuit comprising: a hysteresis amplifier configured to receive the first output and generate a first control signal for the switchable load; and
[11B]	a delay circuit to generate a second control signal for the second stage power converter by delaying the first signal.
Claim 12	
[12A]	The system of claim 11, wherein in response to the voltage going above the threshold: the first control signal causes the switchable load to be disconnected from the first output of the first stage power converter; and
[12B]	the second control signal causes the second stage power converter to enable the second output to the micro-controller.
Claim 13: The system of claim 12, wherein the micro-controller is configured to maximize power generated by the power source.	
Claim 14: The system of claim 13, wherein the power source comprises a photovoltaic panel; the first stage power converter comprises a first step-down converter; and the second stage power converter comprises a second step-down converter.	
Claim 15	
[15A]	The system of claim 12, wherein the switchable load comprises: a resistive device; and a switching device connected to the resistive device,
[15B]	wherein the switching device is configured to be turned on to be connected to the first output to consume the portion of the first output and turned off to be disconnected from the first stage, and
[15C]	wherein the first control signal is connected to control the switching device.
Claim 16: The system of claim 15, wherein the switching device includes one of: a field effect transistor (FET), a metal-oxide-semiconductor field-effect-transistor (MOSFET), and a bipolar junction transistor.	

Claim 17: The system of claim 16, wherein when the switch device is turned on, the switchable load and an input of the second stage are connected in parallel to the first output of the first stage.	
Claim 18	
[18A]	A system to supply power, the system comprising:
[18B]	a photovoltaic panel to provide a direct current input;
[18C]	a first stage power converter connected to the photovoltaic panel to generate a first output from the direct current input;
[18D]	a second stage power converter connected to convert the first output to a second output;
[18E]	a micro-controller;
[18F]	a power absorption circuit; and
[18G]	a control circuit coupled with the first stage power converter and the second stage power converter, the control circuit powered by the first output to control the second stage power converter, wherein
[18H]	when the second stage power converter is disabled in providing the second output to the micro-controller, the control circuit monitors a voltage of the first output powering the power absorption circuit and signals the second stage power converter to continue disabling the providing of the second output to the micro-controller during a time period in which the voltage is below a threshold;
[18I]	when the voltage is above the threshold, the control circuit signals the second stage power converter to enable the providing of the second output to the micro-controller.
Claim 19	
[19A]	The system of claim 18, wherein the power absorption circuit includes a capacitor coupled to the first output;
[19B]	and the threshold allows the capacitor to power the second stage to operate the micro-controller for a predetermined period of time even without the output of the first stage.
Claim 20	
[20A]	The system of claim 18, wherein the power absorption circuit comprises a switchable load;
[20B]	and the control circuit signals the switchable load to be in a first state to consume a portion of the first output when the voltage is below the threshold
[20C]	and to be in a second state not to consume a portion of the first

	output when the voltage is above the threshold.
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