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CHAPTER 8

Comparators

In the previous two chapters, we have focused on the op amp and its design. Before considering how the op amp is used to accomplish various types of analog signal processing and analog-digital conversion, we will examine the comparator. The comparator is a circuit that compares an analog signal with another analog signal or reference and outputs a binary signal based on the comparison. What is meant here by an analog signal is one that can have any of a continuum of amplitude values at a given point in time (see Section 1.1). In the strictest sense a binary signal can have only one of two given values at any point in time, but this concept of a binary signal is too ideal for real-world situations, where there is a transition region between the two binary states. It is important for the comparator to pass quickly through the transition region.

The comparator is widely used in the process of converting analog signals to digital signals. In the analog-to-digital conversion process, it is necessary to first sample the input. This sampled signal is then applied to a combination of comparators to determine the digital equivalent of the analog signal. In its simplest form, the comparator can be considered as a 1-bit analog-digital converter. The application of the comparator in analog-to-digital converters will be presented in Chapter 10.

The presentation on comparators will first examine the requirements and characterization of comparators. It will be seen that comparators can be divided into open-loop and regenerative comparators. The open-loop comparators are basically op amps without compensation. Regenerative comparators use positive feedback, similar to sense amplifiers or flip-flops, to accomplish the comparison of the magnitude between two signals. A third type of comparator emerges that is a combination of the open-loop and regenerative comparators. This combination results in comparators that are extremely fast.

8.1 CHARACTERIZATION OF A COMPARATOR

Figure 8.1-1 shows the circuit symbol for the comparator that will be used throughout this book. This symbol is identical to that for an operational amplifier, because a comparator has many of the same characteristics as a high-gain amplifier. A positive voltage applied at the v_p input will cause the comparator output to go positive, whereas a positive voltage applied at the v_n input will cause the comparator output to go negative. The upper and lower voltage limits of the comparator output are defined as V_{OH} and V_{OL} respectively.

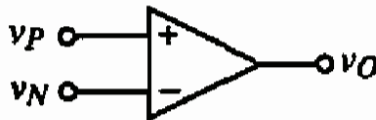


Figure 8.1-1 Circuit symbol for a comparator.

Static Characteristics

A comparator was defined above as a circuit that has a binary output whose value is based on a comparison of two analog inputs. This is illustrated in Fig. 8.1-2. As shown in this figure, the output of the comparator is high (V_{OH}) when the difference between the noninverting and inverting inputs is positive, and low (V_{OL}) when this difference is negative. Even though this type of behavior is impossible in a real-world situation, it can be modeled with ideal circuit elements with mathematical descriptions. One such circuit model is shown in Fig. 8.1-3. It comprises a voltage-controlled voltage source (VCVS) whose characteristics are described by the mathematical formulation given on the figure.

The ideal aspect of this model is the way in which the output makes a transition between V_{OL} and V_{OH} . The output changes states for an input change of ΔV , where ΔV approaches zero. This implies a gain of infinity, as shown below.

$$\text{Gain} = A_v = \lim_{\Delta V \rightarrow 0} \frac{V_{OH} - V_{OL}}{\Delta V} \quad (8.1-1)$$

Figure 8.1-4 shows the dc transfer curve of a first-order model that is an approximation to a realizable comparator circuit. The difference between this model and the previous one is the gain, which can be expressed as

$$A_v = \frac{V_{OH} - V_{OL}}{V_{IH} - V_{IL}} \quad (8.1-2)$$

where V_{IH} and V_{IL} represent the input-voltage difference $v_P - v_N$ needed to just saturate the output at its upper and lower limit, respectively. This input change is called the *resolution* of the comparator. Gain is a very important characteristic describing comparator operation, for it defines the minimum amount of input change (resolution) necessary to make the output swing between the two binary states. These two output states are usually defined by the input requirements of the digital circuitry driven by the comparator output. The voltages V_{OH} and V_{OL} must be adequate to meet the V_{IH} and V_{IL} requirements of the following digital stage. For CMOS technology, these values are usually 70% and 30%, respectively, of the rail-to-rail supply voltage.

The transfer curve of Fig. 8.1-4 is modeled by the circuit of Fig. 8.1-5. This model looks similar to the model of Fig. 8.1-3, the only difference being the functions f_1 and f_0 .

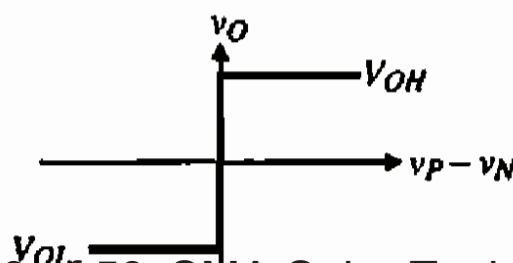


Figure 8.1-2 Ideal transfer curve of a comparator.

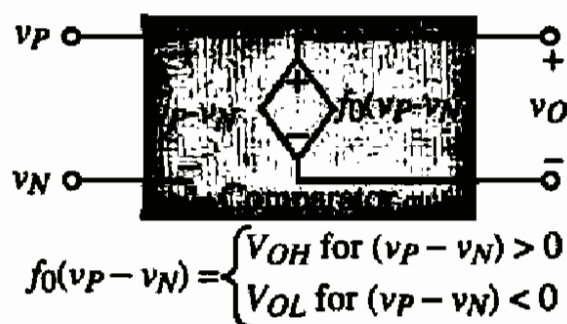


Figure 8.1-3 Model for an ideal comparator.

The second nonideal effect seen in comparator circuits is input-offset voltage, V_{OS} . In Fig. 8.1-2 the output changes as the input difference crosses zero. If the output did not change until the input difference reached a value $+V_{OS}$, then this difference would be defined as the offset voltage. This would not be a problem if the offset could be predicted, but it varies randomly from circuit to circuit [1] for a given design. Figure 8.1-6 illustrates offset in the transfer curve for a comparator, with the circuit model including an offset generator shown in Fig. 8.1-7. The $\pm$ sign of the offset voltage accounts for the fact that V_{OS} is unknown in polarity.

In addition to the above characteristics, the comparator can have a differential input resistance and capacitance and an output resistance. In addition, there will also be an input common-mode resistance, R_{icm} . All these aspects can be modeled in the same manner as was done for the op amp in Section 6.1. Because the input to the comparator is usually differential, the input common-mode range is also important. The ICMR for a comparator would be that range of input common-mode voltage over which the comparator functions normally. This input common-mode range is generally the range where all transistors of the comparator remain in saturation. Even though the comparator is not designed to operate in the transition region between the two binary output states, noise is still important to the comparator. The noise of a comparator is modeled as if the comparator were biased in the transition region of the voltage-transfer characteristics. The noise will lead to an uncertainty in the transition region as shown in Fig. 8.1-8. The uncertainty in the transition region will lead to jitter or phase noise in the circuits where the comparator is employed.

Dynamic Characteristics

The dynamic characteristics of the comparator include both small-signal and large-signal behavior. We do not know, at this point, how long it takes for the comparator to respond to the given differential input. The characteristic delay between input excitation and output transition is the time response of the comparator. Figure 8.1-9 illustrates the response of a comparator to an input as a function of time. Note that there is a delay between the input excitation and the output response. This time difference is called the *propagation delay time* of the comparator. It is a very important parameter since it is often the speed limitation in the conversion

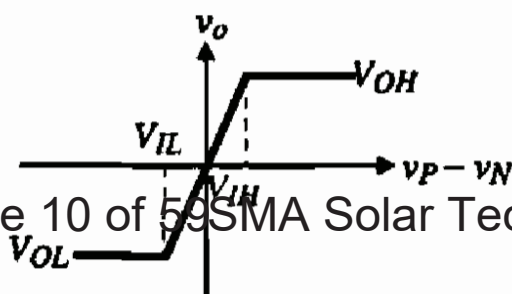


Figure 8.1-4 Transfer curve of a comparator with finite gain.

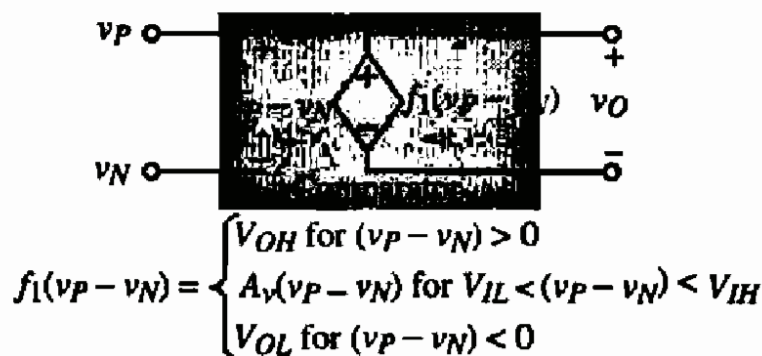


Figure 8.1-5 Model for a comparator with finite gain.

rate of an A/D converter. The propagation delay time in comparators generally varies as a function of the amplitude of the input. A larger input will result in a smaller delay time. There is an upper limit at which a further increase in the input voltage will no longer affect the delay. This mode of operation is called *slewing* or *slew rate*.

The small-signal dynamics are characterized by the frequency response of the comparator. A simple model of this behavior assumes that the differential voltage gain, A_v , is given as

$$A_v(s) = \frac{A_v(0)}{\frac{s}{\omega_c} + 1} = \frac{A_v(0)}{s\tau_c + 1} \quad (8.1-3)$$

where $A_v(0)$ is the dc gain of the comparator and $\omega_c = 1/\tau_c$ is the -3 dB frequency of the single (dominant) pole approximation to the comparator frequency response. Normally, the $A_v(0)$ and ω_c of the comparator are smaller and larger, respectively, than for an op amp.

Let us assume that the minimum change of voltage at the input of the comparator is equal to the resolution of the comparator. We will define this minimum input voltage to the comparator as

$$V_{in}(\min) = \frac{V_{OH} - V_{OL}}{A_v(0)} \quad (8.1-4)$$

For a step input voltage, the output of the comparator modeled by Eq. (8.1-3) rises (or falls) with a first-order exponential time response from V_{OL} to V_{OH} (or V_{OH} to V_{OL}) as shown in Fig. 8.1-10. If V_{in} is larger than $V_{in}(\min)$, the output rise or fall time is faster. When $V_{in}(\min)$ is applied to the comparator, we can write the following equation:

$$\frac{V_{OH} - V_{OL}}{2} = A_v(0) [1 - e^{-t_p/\tau_c}] V_{in}(\min) = A_v(0) [1 - e^{-t_p/\tau_c}] \left(\frac{V_{OH} - V_{OL}}{A_v(0)} \right) \quad (8.1-5)$$

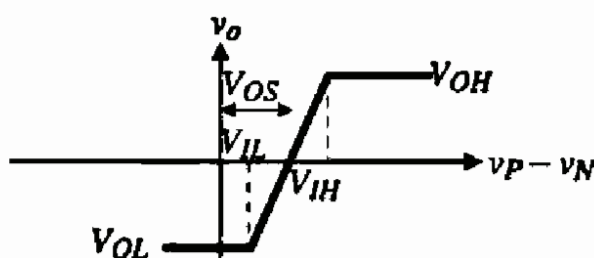


Figure 8.1-6 Transfer curve of a comparator including input-offset voltage.



Figure 8.1-7 Model for a comparator including input-offset voltage.

Therefore, the propagation delay time for an input step of $v_{in}(\min)$ can be expressed as

$$t_p(\max) = \tau_c \ln(2) = 0.693\tau_c \quad (8.1-6)$$

This propagation delay time will be valid for either positive-going or negative-going comparator outputs. Note in Fig. 8.1-10 that if the applied input is k times greater than $V_{in}(\min)$, then the propagation delay time is given as

$$t_p = \tau_c \ln\left(\frac{2k}{2k-1}\right) \quad (8.1-7)$$

where

$$k = \frac{V_{in}}{V_{in}(\min)} \quad (8.1-8)$$

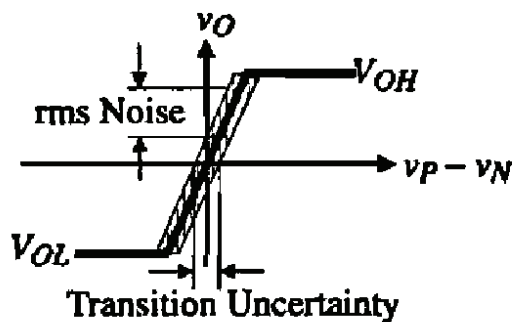


Figure 8.1-8 Influence of noise on a comparator.

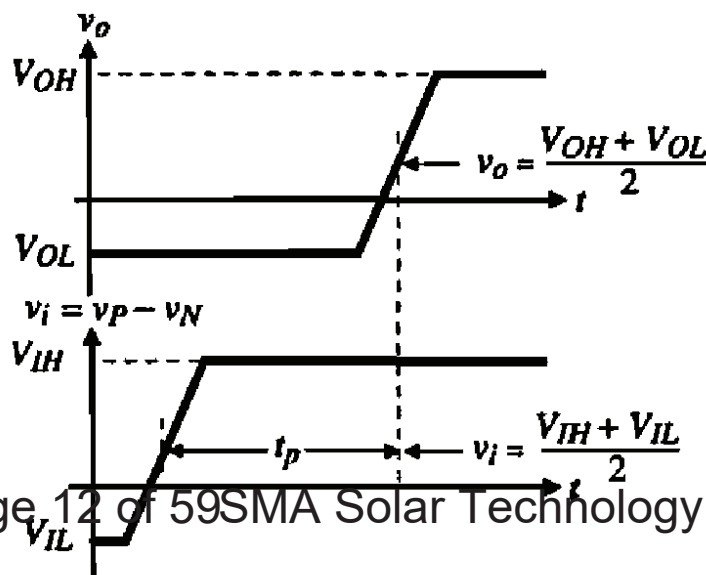


Figure 8.1-9 Propagation delay time of a noninverting comparator.

Obviously, the more overdrive applied to the input of this comparator, the smaller the propagation delay time.

As the overdrive increases to the comparator eventually the comparator enters a large-signal mode of operation. Under large-signal operation, a slew-rate limit will occur due to limited current to charge or discharge capacitors. If the propagation delay time is determined by the slew-rate of the comparator, then this time can be written as

$$t_p = \Delta T = \frac{\Delta V}{SR} = \frac{V_{OH} - V_{OL}}{2 \cdot SR} \quad (8.1-9)$$

In the case where the propagation time is determined by the slew rate, the most important factor to decrease the propagation time is increasing the sinking or sourcing capability of the comparator.

PROPGATION DELAY TIME OF A COMPARATOR

Find the propagation delay time of an open-loop comparator that has a dominant pole at 10^3 rad/s, a dc gain of 10^4 , a slew rate of $1 \text{ V}/\mu\text{s}$, and a binary output voltage swing of 1 V . Assume the applied input voltage is 10 mV .

Solution

The input resolution for this comparator is $1 \text{ V}/10^4$ or 0.1 mV . Therefore, the 10 mV input is 100 times larger than $v_{in(\text{min})}$, giving a k of 100. From Eq. (8.1-7) we get

$$t_p = \frac{1}{10^3} \ln\left(\frac{2 \cdot 100}{2 \cdot 100 - 1}\right) = 10^{-3} \ln\left(\frac{200}{199}\right) = 5.01 \mu\text{s}$$

From Eq. (8.1-9) we get

$$t_p = \frac{1}{2 \cdot 1 \times 10^6} = 0.5 \mu\text{s}$$

Therefore, the propagation delay time for this case is the larger or $5.01 \mu\text{s}$.

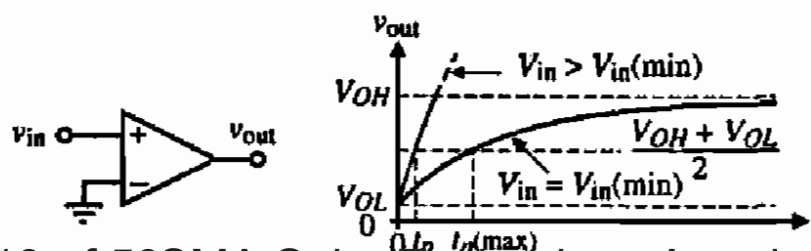


Figure 8.1-10 Small signal transient response for a comparator.

8.2 TWO-STAGE, OPEN-LOOP COMPARATORS

A close examination of the previous requirements for a comparator reveal that it requires a *differential input and sufficient gain to be able to achieve the desired resolution*. As a result, the two-stage op amp of Chapter 6 makes an excellent implementation of the comparator [1]. A simplification occurs because the comparator will generally be used in an open-loop mode and therefore it is not necessary to compensate the comparator. In fact, it is preferred not to compensate the comparator so that it has the largest bandwidth possible, which will give a faster response. Therefore, we will examine the performance of the two-stage, uncompensated op amp shown in Fig. 8.2-1 used as a comparator.

Two-Stage, Open-Loop Comparator Performance

The first item of interest is the values of V_{OH} and V_{OL} for the two-stage comparator of Fig. 8.2-1. Since the output stage is a current-sink inverter, the approach used in Section 5.1 for the current-sink/source inverter can be used. The maximum output voltage, assuming that the gate of M6 has a minimum voltage given as $V_{G6(\min)}$, can be expressed as

$$V_{OH} = V_{DD} - (V_{DD} - V_{G6(\min)} - |V_{TP}|) \left[1 - \sqrt{1 - \frac{2I_7}{\beta_6(V_{DD} - V_{G6(\min)} - |V_{TP}|)^2}} \right] \quad (8.2-1)$$

The minimum output voltage is

$$V_{OL} = V_{SS} \quad (8.2-2)$$

The small-signal gain of the comparator was developed in Section 6.2 and is given as

$$A_v(0) = \left(\frac{g_{m1}}{g_{ds2} + g_{ds4}} \right) \left(\frac{g_{m6}}{g_{ds6} + g_{ds7}} \right) \quad (8.2-3)$$

Using Eqs. (8.2-1) through (8.2-3) and Eq. (8.1-4) gives the resolution of the comparator, which is $V_{in(\min)}$.

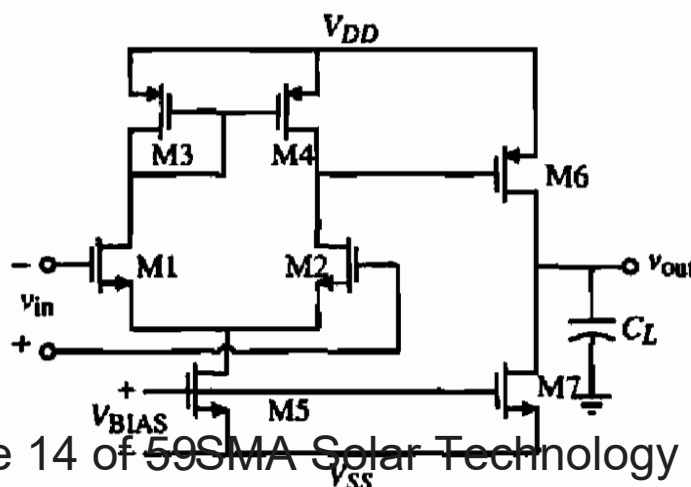


Figure 8.2-1 Two-stage comparator.

The comparator of Fig. 8.2-1 has two poles of interest. One is the output pole of the first stage, p_1 , and the second is the output pole of the second stage, p_2 . These poles are expressed as

$$p_1 = \frac{-1}{C_I(g_{ds2} + g_{ds4})} \quad (8.2-4a)$$

and

$$p_2 = \frac{-1}{C_{II}(g_{ds2} + g_{ds4})} \quad (8.2-4b)$$

where C_I is the sum of the capacitances connected to the output of the first stage and C_{II} is the sum of the capacitances connected to the output of the second stage. C_{II} will generally be dominated by C_L . The frequency response of the two-stage comparator can be expressed using the above results as

$$A_v(s) = \frac{A_v(0)}{\left(\frac{s}{p_1} + 1\right)\left(\frac{s}{p_2} + 1\right)} \quad (8.2-5)$$

The following example illustrates the practical values for the two-stage, open-loop comparator.

PERFORMANCE OF A TWO-STAGE COMPARATOR

Evaluate V_{OH} , V_{OL} , $A_v(0)$, $V_{in}(\min)$, p_1 , and p_2 for the two-stage comparator shown in Fig. 8.2-1. Assume that this comparator is the circuit of Example 6.3-1 with no compensation capacitor, C_c , and the minimum value of $V_{GS} = 0$ V. Also, assume that $C_I = 0.2$ pF and $C_{II} = 5$ pF.

Solution

Using Eq. (8.2-1), we find that

$$V_{OH} = 2.5 - (2.5 - 0 - 0.7) \left[1 - \sqrt{1 - \frac{2 \cdot 95 \times 10^{-6}}{50 \times 10^{-6} \cdot 14(2.5 - 0 - 0.7)^2}} \right] = 2.42 \text{ V}$$

The value of V_{OL} is found from Eq. (8.2-2) and is 2.5 V. Equation (8.2-3) was evaluated in Example 6.3-1 as $A_v(0) = 7696$. Thus, from Eq. (8.1-2) we find the input resolution as

$$V_{in}(\min) = \frac{V_{OH} - V_{OL}}{A_v(0)} = \frac{4.92 \text{ V}}{7696} = 0.640 \text{ mV}$$

Next, we find the poles of the comparator, p_1 and p_2 . From Example 6.3-1 we find that

$$p_1 = \frac{g_{ds2} + g_{ds4}}{C_I} = \frac{15 \times 10^{-6}(0.04 + 0.05)}{0.2 \times 10^{-12}} = 6.75 \times 10^6 \text{ (1.074 MHz)}$$

and

$$p_2 = \frac{g_{ds6} + g_{ds7}}{C_{II}} = \frac{95 \times 10^{-6}(0.04 + 0.05)}{5 \times 10^{-12}} = 1.71 \times 10^6 \text{ (0.670 MHz)}$$

The response of a two-stage, open-loop comparator having two poles to a step input of V_{in} is given as

$$v_{out}(t) = A_v(0)V_{in} \left[1 + \frac{p_2 e^{-tp_1}}{p_1 - p_2} - \frac{p_1 e^{-tp_2}}{p_1 - p_2} \right] \quad (8.2-6)$$

where $p_1 \neq p_2$. Equation (8.2-6) is valid for the output unless the rate of rise or fall of the output exceeds the slew rate of the output of the comparator. The slew rate of the output is similar to a Class A inverter and the negative slew rate is

$$SR^- = \frac{I_7}{C_{II}} \quad (8.2-7)$$

The positive slew rate is determined by the current sourced by M6. This slew rate is expressed as

$$SR^+ = \frac{I_6 - I_7}{C_{II}} = \frac{\beta_6(V_{DD} - V_{G6}(\min) - |V_{TP}|)^2 - I_7}{C_{II}} \quad (8.2-8)$$

If the rate of rise or fall of Eq. (8.2-6) exceeds the positive or negative slew rate, then the output response is simply a ramp whose slope is given by Eq. (8.2-7) or (8.2-8).

Assuming that slew does not occur, the step response of the two-pole comparator of Eq. (8.2-6) can be plotted by normalizing the amplitude and time. The result is

$$v'_{out}(t_n) = \frac{v_{out}(t_n)}{A_v(0)V_{in}} = 1 - \frac{m}{m-1}e^{-t_n} + \frac{1}{m-1}e^{-mt_n} \quad (8.2-9)$$

where

$$m = \frac{p_2}{p_1} \neq 1 \quad (8.2-10)$$

and

$$t_n = tp_1 = \frac{1}{\tau_1} \quad (8.2-11)$$

If $m = 1$, then Eq. (8.2-9) becomes

$$v'_{out}(t_n) = 1 - p_1 e^{-t_n} - \frac{t_n}{p_1} e^{-t_n} = 1 - e^{-t_n} - t_n e^{-t_n} \quad (8.2-12)$$

where p_1 is assumed to be unity. Equations (8.2-9) and (8.2-12) are shown in Fig. 8.2-2 for values of m from 0.25 to 4.

If the input step is larger than $v_{in}(\min)$, then the amplitudes of the curves in Fig. 8.2-2 become limited at V_{OH} . We note with interest that the slope at $t = 0$ is zero. This can be seen by differentiating Eq. (8.2-9) and letting $t = 0$. The steepest slope of Eq. (8.2-9) occurs at

$$t_n(\max) = \frac{\ln(m)}{m - 1} \quad (8.2-13)$$

which is found by differentiating Eq. (8.2-9) twice and setting the result equal to zero. The slope at $t_n(\max)$ can be written as

$$\frac{dv'_{out}(t_n(\max))}{dt_n} = \frac{m}{m - 1} \left[\exp\left(\frac{-\ln(m)}{m - 1}\right) - \exp\left(-m \frac{\ln(m)}{m - 1}\right) \right] \quad (8.2-14)$$

If the slope of the linear response exceeds the slew rate, then the step response becomes slew limited. If the slew rate is close to the value of Eq. (8.2-14) it is not clear how to model the step response. One could assume a slew limited response until the slope of the linear response becomes less than the slew rate but this point is not easy to find. If the comparator is overdriven, $V_{in} > V_{in}(\min)$, then if the slew rate is smaller than Eq. (8.2-14), the slew rate can be used to predict the step response.

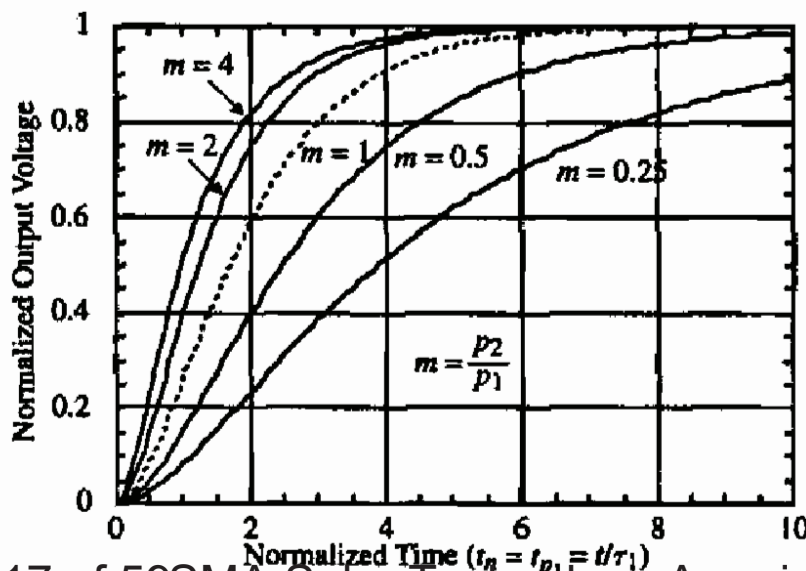


Figure 8.2-2 Linear step response of a comparator with two real axis poles, p_1 and p_2 .

STEP RESPONSE OF EXAMPLE 8.2-1

Find the maximum slope of Example 8.2-1 and the time at which it occurs if the magnitude of the input step is $V_{in(min)}$. If the dc bias current in M7 of Fig. 8.2-1 is $100\text{ }\mu\text{A}$, at what value of load capacitance, C_L , would the transient response become slew limited? If the magnitude of the input step is $100V_{in(min)}$ and $V_{OH} - V_{OL} = 1\text{ V}$, what would be the new value of C_L at which slewing would occur?

Solution

The poles of the comparator were given in Example 8.2-1 as $p_1 = -6.75 \times 10^6\text{ rad/s}$ and $p_2 = -1.71 \times 10^6\text{ rad/s}$. This gives a value of $m = 0.253$. From Eq. (8.2-13), the maximum slope occurs at $t_n(max) = 1.84\text{ s}$. Dividing by $|p_1|$ gives $t(max) = 0.273\text{ }\mu\text{s}$. The slope of the transient response at this time is found from Eq. (8.2-14) as

$$\frac{dv'_{out}(t_n(max))}{dt_n} = -0.338[\exp(-1.84) - \exp(-0.253 \cdot 1.84)] = 0.159\text{ V/s}$$

Multiplying the above by $|p_1|$ gives

$$\frac{dv'_{out}(t(max))}{dt} = 1.072\text{ V}/\mu\text{s}$$

Therefore, if the slew rate of the comparator is less than $1.072\text{ V}/\mu\text{s}$, the transient response will experience slewing. If the load capacitance, C_L , becomes larger than $(100\text{ }\mu\text{A})/(1.072\text{ V}/\mu\text{s})$ or 93.3 pF , the comparator will experience slewing.

If the comparator is overdriven by a factor of $100V_{in(min)}$, then we must unnormalize the output slope as follows:

$$\frac{dv'_{out}(t(max))}{dt} = \frac{v_{in}}{V_{in(min)}} \frac{dv'_{out}(t(max))}{dt} = 100 \cdot 1.072\text{ V}/\mu\text{s} = 107.2\text{ V/s}$$

Therefore, the comparator will now slew with a load capacitance of 0.933 pF . For large overdrives, the comparator will generally experience slewing.

It is of interest to predict the propagation delay time for the two-pole comparator when slewing does not occur. To do this, we set Eq. (8.2-9) equal to $0.5(V_{OH} + V_{OL})$ and solve for the propagation delay time, t_p . Unfortunately, this equation is not easily solved. An alternate approach is to replace the exponential terms in Eq. (8.2-9) with their power series representations. This results in

$$v_{out}(t_n) \approx A_v(0)V_{in} \left[1 - \frac{m}{m-1} \left(1 - t_n + \frac{t_n^2}{2} + \dots \right) + \frac{1}{m-1} \left(1 - mt_n + \frac{mt_n^2}{2} + \dots \right) \right] \quad (8.2-15)$$

Equation (8.2-15) can be simplified to

$$v_{out}(t_n) \approx \frac{mt_n^2 A_v(0) V_{in}}{2} \quad (8.2-16)$$

Setting $v_{out}(t_n)$ equal to $0.5(V_{OH} + V_{OL})$ and solving for t_n gives the normalized propagation delay time, t_{pm} , as

$$t_{pm} \approx \sqrt{\frac{V_{OH} + V_{OL}}{mA_v(0)V_{in}}} = \sqrt{\frac{V_{in}(\min)}{mV_{in}}} = \frac{1}{\sqrt{mk}} \quad (8.2-17)$$

where k was defined in Eq. (8.1-8). This result approximates the response of Fig. 8.2-2 as a parabola. For values of t_n that are less than 1, this is a reasonable approximation. If one considers the influence of overdriving the input, then Eq. (8.2-17) is even a better approximation. The influence of overdriving is to only use the initial part of the response (i.e., it is like V_{OH} is being lowered and brought closer to zero). The following example explores the application of Eq. (8.2-17) to predict the propagation time delay for a two-pole comparator.

EXAMPLE 8.2-1

PROPAGATION DELAY TIME OF A TWO-POLE COMPARATOR THAT IS NOT SLEWING

Find the propagation delay time of the comparator of Example 8.2-1 if $V_{in} = 10$ mV, 100 mV, and 1 V.

Solution

From Example 8.2-1 we know that $V_{in}(\min) = 0.642$ mV and $m = 0.253$. For $V_{in} = 10$ mV, $k = 15.576$, which gives $t_{pm} = 0.504$. This corresponds well with Fig. 8.2-2, where the normalized propagation time delay is the time at which the amplitude is $1/(2k)$ or 0.032. Dividing by $|p_1|$ gives the propagation time delay as 72.7 ns. Similarly, for $V_{in} = 100$ mV and 1 V we get propagation delays time of 23.6 ns and 7.5 ns, respectively.

Initial Operating States for the Two-Stage, Open-Loop Comparator

In order to analyze the propagation time delay of a slewing, two-stage, open-loop comparator, it is necessary to first be able to find the initial operating states of the output voltages of the first and second stages. Consider the two-stage, open-loop comparator of Fig. 8.2-3. The capacitances at the outputs of the first and second stages are C_1 and C_2 , respectively.

Our approach will be to choose one of the input gates equal to a dc voltage and find the output voltage of the first and second stages when the other input gate is above and below the dc voltage on the first gate. Actually, we need to consider two cases for each of the previous possibilities. These cases are when the currents in M1 and M2 are different but neither is zero and when one of the input transistors has a current of I_{SS} and the other current is zero.

We begin by first assuming that v_{G2} is equal to a dc voltage, V_{G2} , and that $v_{G1} > V_{G2}$ with $i_1 < I_{SS}$ and $i_2 > 0$. In this case, as long as M4 remains in saturation, $i_4 = i_3 = i_1$, which is greater than i_2 . Consequently, v_{o1} increases because of the difference current flowing into C_1 .

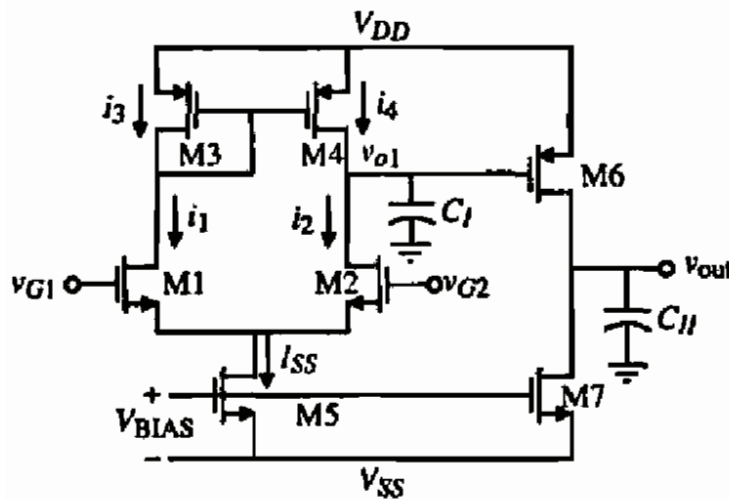


Figure 8.2-3 Two-stage, open-loop comparator used to find initial states.

As v_{o1} continues to increase, M4 will become active and $i_4 < i_3$. When the voltage across the source-drain of M4 decreases to the point where $i_4 = i_2$, the output voltage of the first stage, v_{o1} , stabilizes. This value of voltage is

$$V_{DD} - V_{SD4}(\text{sat}) < v_{o1} < V_{DD}, \quad v_{G1} > V_{G2}, \quad i_1 < I_{SS} \quad \text{and} \quad i_2 > 0 \quad (8.2-18)$$

Under the conditions of Eq. (8.2-18), the value of $v_{SG6} < |V_{TP}|$ and M6 will be off and the output voltage will be

$$v_{out} = V_{SS}, \quad v_{G1} > V_{G2}, \quad i_1 < I_{SS} \quad \text{and} \quad i_2 > 0 \quad (8.2-19)$$

If $v_{G1} \gg V_{G2}$, then $i_1 = I_{SS}$ and $i_2 = 0$ and v_{o1} will be at V_{DD} and v_{out} is still at V_{SS} .

Next, assume that v_{G2} is still equal to V_{G2} , but now $v_{G1} < V_{G2}$ with $i_1 > 0$ and $i_2 < I_{SS}$. In this case, $i_4 = i_3 = i_1$ is less than i_2 and v_{o1} decreases. When $v_{o1} \leq V_{G2} - V_{TN}$, then M2 becomes active. As v_{o1} continues to decrease, $v_{DS2} < V_{DS2}(\text{sat})$, the current through M2 decreases until $i_1 = i_2 = I_{SS}/2$ at which point v_{o1} stabilizes. At this point,

$$V_{G2} - V_{GS2} < v_{o1} < V_{G2} - V_{GS2} + V_{DS2}(\text{sat}) \quad (8.2-20)$$

or

$$V_{S2} < v_{o1} < V_{S2} + V_{DS2}(\text{sat}), \quad v_{G1} < V_{G2}, \quad i_1 > 0 \quad \text{and} \quad i_2 < I_{SS} \quad (8.2-21)$$

Under the conditions of Eq. (8.2-21), the output voltage, v_{out} , will be near V_{DD} and can be found following the approach used in Example 5.1-2. If $v_{G1} \ll V_{G2}$, the previous results are still valid until the source voltage of M1 or M2 causes M5 to leave the saturated region. When that happens, I_{SS} decreases and v_{o1} can approach V_{SS} and v_{out} will be determined as was illustrated in Example 5.1-2.

If the gate of M1 is equal to a dc voltage of V_{G1} , we can now examine the initial states of the outputs of the first and second stages by repeating the above process. First assume that $v_{G1} = V_{G1}$ and $v_{G2} > V_{G1}$ with $i_2 < I_{SS}$ and $i_1 > 0$. As a result, $i_1 < i_2$ gives $i_4 < i_2$ as long as M4 is saturated. Therefore, v_{o1} decreases because of the difference current flowing out of C_I . As v_{o1} decreases, M2 will become active and i_2 will decrease to the point where $i_1 = i_2 = I_{SS}/2$. Therefore, v_{o1} stabilizes and has a value given as

$$V_{G1} - V_{GS2}(I_{SS}/2) < v_{o1} < V_{G1} - V_{GS2}(I_{SS}/2) + V_{DS2}(\text{sat}) \quad (8.2-22)$$

or

$$V_{S2}(I_{SS}/2) < v_{o1} < V_{S2}(I_{SS}/2) + V_{DS2}(\text{sat}), \quad v_{G2} > V_{G1}, \quad i_1 > 0 \quad \text{and} \quad i_2 < I_{SS} \quad (8.2-23)$$

Under the conditions of Eq. (8.2-23), the output voltage, v_{out} , will be near V_{DD} and can be found following the approach used in Example 5.1-2. If $v_{G2} \gg V_{G1}$, the previous results are still valid until the source voltage of M1 or M2 causes M5 to leave the saturated region. When that happens, I_{SS} decreases and v_{o1} can approach V_{SS} and v_{out} will be determined as was illustrated in Example 5.1-2.

Next, assume that v_{G1} is still equal to V_{G1} , but now $v_{G2} < V_{G1}$ with $i_1 < I_{SS}$ and $i_2 > 0$. As a result, $i_1 > i_2$, which gives $i_4 > i_2$, causing v_{o1} to increase. As long as M4 is saturated, $i_4 > i_2$. When M4 enters the active region, i_4 will decrease until $i_4 = i_2$ at which point v_{o1} stabilizes and is given as

$$V_{DD} - V_{SD4}(\text{sat}) < v_{o1} < V_{DD}, \quad v_{G2} < V_{G1}, \quad i_1 < I_{SS} \quad \text{and} \quad i_2 > 0 \quad (8.2-24)$$

Under the conditions of Eq. (8.2-24), the value of $v_{SG6} < |V_{TP}|$ and M6 will be off and the output voltage will be

$$v_{out} = V_{SS}, \quad v_{G2} < V_{G1}, \quad i_1 < I_{SS} \quad \text{and} \quad i_2 > 0 \quad (8.2-25)$$

If $v_{G2} \ll V_{G1}$, then $i_1 = I_{SS}$ and $i_2 = 0$ and v_{o1} will be at V_{DD} and v_{out} is still at V_{SS} . The above results are summarized in Table 8.2-1.

Propagation Delay Time of a Slewing, Two-Stage, Open-Loop Comparator

In most applications, the two-stage, open-loop comparator is overdriven to the point where the propagation delay time is determined by the slewing performance of the comparator. In this case, the propagation delay time is found by evaluating the equation

$$i_i = C_i \frac{dv_i}{dt_i} = C_i \frac{\Delta v_i}{\Delta t_i} \quad (8.2-26)$$

TABLE 8.2-1 Initial Operating States of the Two-Stage, Open-Loop Comparator of Fig. 8.2-3

Conditions	Initial State of v_{o1}	Initial State of v_{out}
$i_1 > V_{G2}$, $i_1 < I_{SS}$ and $i_2 > 0$	$V_{DD} - V_{SD4}(\text{sat}) < v_{o1} < V_{DD}$	V_{SS}
$i_1 \gg V_{G2}$, $i_1 = I_{SS}$ and $i_2 = 0$	V_{DD}	V_{SS}
$i_1 < V_{G2}$, $i_1 > 0$ and $i_2 < I_{SS}$	$V_{S2} < v_{o1} < V_{S2} + V_{DS2}(\text{sat})$	Eq. (5.1-19) for PMOS
$i_1 \ll V_{G2}$, $i_1 = 0$ and $i_2 = I_{SS}$	V_{DD}	Eq. (5.1-19) for PMOS
$i_2 > V_{G1}$, $i_1 > 0$ and $i_2 < I_{SS}$	$V_{S2}(I_{SS}/2) < v_{o1} < V_{S2}(I_{SS}/2) + V_{DS2}(\text{sat})$	Eq. (5.1-19) for PMOS
$i_2 \gg V_{G1}$, $i_1 = 0$ and $i_2 = I_{SS}$	V_{SS}	Eq. (5.1-19) for PMOS
$i_2 < V_{G1}$, $i_1 < I_{SS}$ and $i_2 > 0$	$V_{DD} - V_{SD4}(\text{sat}) < v_{o1} < V_{DD}$	V_{SS}
$i_2 \ll V_{G1}$, $i_1 = I_{SS}$ and $i_2 = 0$	V_{DD}	V_{SS}

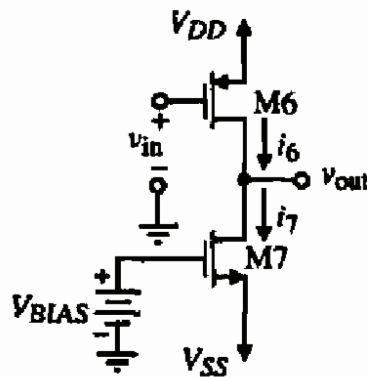


Figure 8.2-4 Second stage of the two-stage, open-loop comparator.

where C_i is the capacitance to ground at the output of the i th stage. The propagation delay time of the i th stage is found by solving for Δt_i from Eq. (8.2-26) to get

$$t_i = \Delta t_i = C_i \frac{\Delta V_i}{I_i} \quad (8.2-27)$$

The propagation delay time is found by summing the delays of each stage.

The term ΔV_i in Eq. (8.2-27) is generally equal to half of the output swing of the i th stage. In some cases, the value of ΔV_i is determined by the threshold or trip point of the next stage. The trip point of an amplifier is the value of input that causes the output to be midway between its limits. In the two-stage, open-loop comparator, the second stage is generally a Class A inverting amplifier similar to that shown in Fig. 8.2-4. The trip point can be calculated by assuming both transistors are in saturation and equating the currents. The only unknown is the input voltage. Solving for this input voltage gives

$$v_{in} = V_{TRP} = V_{DD} - |V_{TP}| - \sqrt{\frac{K_N(W_7/L_7)}{K_P(W_6/L_6)}} (V_{BIAS} - V_{SS} - V_{TN}) \quad (8.2-28)$$

If we refer back to Fig. 5.1-5, we see that the trip point is really a range and not a specific value. However, if the slope of the inverting amplifier in the region where both transistors are saturated is steep enough, then the trip point can be considered to be a point.

FIGURE 8.2-4

CALCULATION OF THE TRIP POINT OF AN INVERTING AMPLIFIER

Use the model parameters of Table 3.1-2 and calculate the trip point of the inverter in Fig. 5.1-5.

Solution

It is probably easier to redevelop Eq. (8.2-28) for the inverter of Fig. 5.1-5 than to use Eq. (8.2-28). Equating the currents of M1 and M2 of Fig. 5.1-5 gives

$$V_{TRP} = V_{TN} + \sqrt{\frac{\beta_2}{\beta_1}} (V_{DD} - V_{BIAS} - |V_{TP}|) = 0.7 + \sqrt{\frac{50(2)}{110(2)}} (2.5 - 0.7) = 1.913 \text{ V}$$

We note that this value corresponds very closely with the value of input voltage at which the output of Fig. 5.1-5 is midway between power supplies.

The propagation delay time of a two-stage, open-loop comparator that is slewing can be calculated using the above ideas. The delay of the first stage is added to the delay of the second stage to get the total propagation delay time. Let us illustrate the procedure with an example.

CALCULATION OF THE PROPAGATION DELAY TIME OF A TWO-STAGE, OPEN-LOOP COMPARATOR

For the two-stage comparator shown in Fig. 8.2-5, assume that $C_I = 0.2$ pF and $C_{II} = 5$ pF. Also, assume that $v_{G1} = 0$ V and that v_{G2} has the waveform shown in Fig. 8.2-6. If the input voltage is large enough to cause slew to dominate, find the propagation delay time of the rising and falling output of the comparator and give the propagation delay time of the comparator.

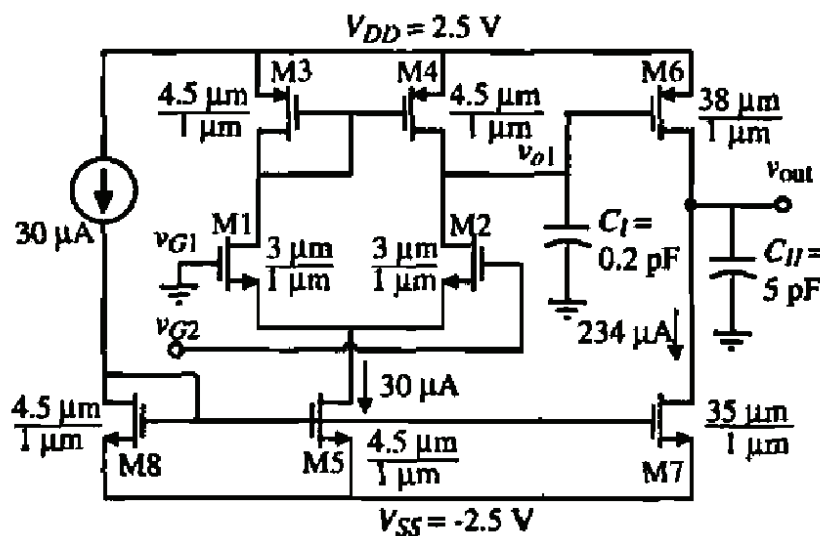


Figure 8.2-5 Two-stage comparator for Example 8.2-5.

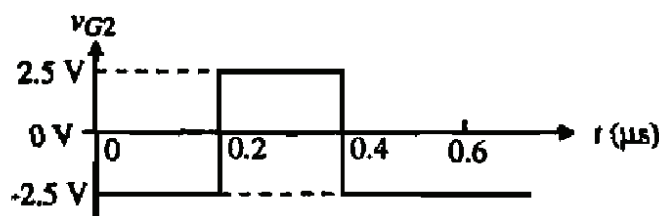


Figure 8.2-6 Input to the comparator of Example 8.2-5.

Solution

The total delay will be given as the sum of the first and second stages delays, t_1 and t_2 , respectively. First, consider the change of v_{G2} from -2.5 to 2.5 V at 0.2 μ s. From Table 8.2-1, the last row, the initial states of v_{o1} and v_{out} are $+2.5$ and -2.5 V, respectively. To find the falling delay of the first stage, t_{f1} , requires C_I , ΔV_{o1} , and I_3 . $C_I = 0.2$ pF, $I_3 = 30$ μ A, and ΔV_1 can be calculated by finding the trip point of the output stage. Although we could use Eq. (8.2-8), it is easier to set the current of M6 when saturated equal to 234 μ A to get the trip point. Doing this we get

$$\frac{\beta_6}{2} (V_{DD} - |V_{TP}|)^2 = 234 \mu\text{A} \rightarrow V_{SG6} = 0.7 + \sqrt{\frac{234 \cdot 2}{16 \cdot 38}} = 1.035 \text{ V}$$

Subtracting this voltage from 2.5 V gives the trip point of the second stage as

$$V_{TRP2} = 2.5 - 1.035 = 1.465 \text{ V}$$

Therefore, $\Delta V_1 = 2.5 \text{ V} - 1.465 \text{ V} = V_{SG6} = 1.035 \text{ V}$. Thus, the falling propagation time delay of the first stage is

$$t_{f01} = (0.2 \text{ pF}) \left(\frac{1.035 \text{ V}}{30 \mu\text{A}} \right) = 6.9 \text{ ns}$$

The rising propagation time delay of the second stage requires knowledge of C_{II} , ΔV_{out} , and I_6 . C_{II} is given as 5 pF, $\Delta V_{out} = 2.5 \text{ V}$ (assuming the trip point of the circuit connected to the output of the comparator is 0 V), and I_6 can be found as follows. When the gate of M6 is at 1.465 V, the current is 234 μA . However, the output of the first stage will continue to fall so what value should be used for the gate in order to calculate I_6 ? The lowest value of V_{G6} is given as

$$V_{G6} = V_{G1} - V_{GS2}(I_{SS}/2) + V_{DS2} \approx -V_{GS2}(I_{SS}/2) = -0.7 - \sqrt{\frac{2 \cdot 15}{110 \cdot 3}} = -1.00 \text{ V}$$

Let us take the approximate value of V_{G6} as midway between 1.465 and -1.00 V , which is 0.232 V. Therefore, $V_{SG6} = 2.27 \text{ V}$ and the value of I_6 is

$$I_6 = \frac{\beta_6}{2} (V_{SG6} - |V_{TP}|)^2 = \frac{38 \cdot 50}{2} (2.27 - 0.7)^2 = 2342 \mu\text{A}$$

which is a reminder that the active transistor can generally sink or source more current than the fixed transistor in the Class A inverting stage. The rising propagation time delay for the output can be expressed as

$$t_{r,out} = (5 \text{ pF}) \left(\frac{2.5 \text{ V}}{2342 \mu\text{A}} \right) = 5.3 \text{ ns}$$

Thus, the total propagation time delay of the rising output of the comparator is approximately 12.2 ns and most of this delay is attributable to the first stage.

Next, consider the change of v_{G2} from 2.5 to -2.5 V , which occurs at 0.4 μs . We shall assume that v_{G2} has been at 2.5 V long enough for the conditions of Table 8.2-1 to be valid. Therefore, $v_{o1} \approx V_{SS} = -2.5 \text{ V}$ and $v_{out} \approx V_{DD}$. Rather than use Eq. (5.1-19), we have assumed that v_{out} is approximately V_{DD} . The propagation delay times for the first and second stages are calculated as

and

$$t_{f, \text{out}} = (5 \text{ pF}) \left(\frac{2.5 \text{ V}}{234 \text{ } \mu\text{A}} \right) = 53.42 \text{ ns}$$

The total propagation delay time of the falling output is 79.85 ns. Taking the average of the rising and falling propagation delays time gives a propagation delay time for this two-stage, open-loop comparator of about 44.93 ns. These values compare favorably with the simulation of the comparator shown in Fig. 8.2-7.

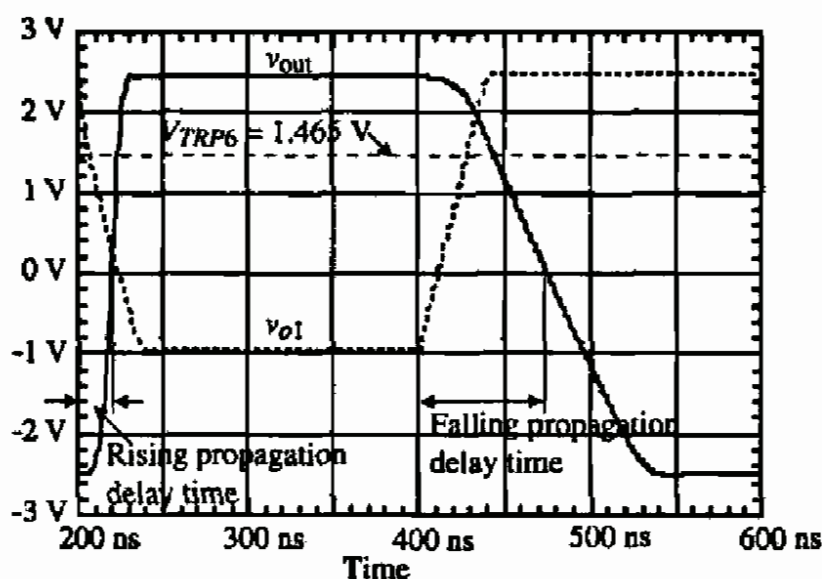


Figure 8.2-7 Response of Fig. 8.2-3 to the input shown in Fig. 8.2-6.

The previous example can be reworked for the case where v_{O2} is held constant and v_{O1} varies (see Problem 8.2-8). If the comparator is not slewing, then the propagation time delay will be determined by the linear step response of the comparator. The propagation time delay analysis becomes more complex if the comparator slews only for part of the step response. This is a case where simulation would provide the desired details.

Design of a Two-Stage, Open-Loop Comparator

The design of a two-stage, open-loop comparator is similar in many respects to the two-stage op amp. The primary difference is that the comparator is not compensated. The typical input specifications include the propagation time delay, the output voltage swing, the resolution, and input common-mode range. There are two approaches to the design of the comparator depending on whether it is slewing or not. If the comparator is not slewing, then the pole locations are extremely important. On the other hand, if the comparator slews, then the ability to charge and discharge capacitors becomes more important.

For the nonslewing comparator, the propagation time is reduced by a large overdrive and the pole placement. The larger the magnitude of the poles, the shorter the propagation delay time. Since the poles are due to the capacitance and resistance to ground at the output of each stage, the input resistance of the second stage and the resistance to ground at the output of the first stage are important. The input resistance of the second stage is small because of the design

procedure illustrated in Table 8.2-2 can be used to accomplish a minimum propagation delay time for the two-stage, open-loop comparator. This procedure attempts to design the pole locations to correspond to a desired propagation delay time. The procedure is simplified by assuming that $m = 1$ or the poles are equal.

TABLE 8.2-2 Design of the Two-Stage, Open-Loop Comparator of Fig. 8.2-3 for a Linear Response

Specifications: t_p , C_{II} , $V_{in}(\min)$, V_{OH} , V_{OL} , V_{icm}^+ , V_{icm}^- , and overdrive Constraints: Technology, V_{DD} , and V_{SS}		
Step	Design Relationships	Comments
1	$ p_I = p_{II} = \frac{1}{t_p \sqrt{mk}}$, and $I_7 = I_6 = \frac{ p_{II} C_{II}}{\lambda_N + \lambda_P}$	Choose $m = 1$
2	$\frac{W_6}{L_6} = \frac{2 \cdot I_6}{K'_P (V_{SD6}(\text{sat}))^2}$ and $\frac{W_7}{L_7} = \frac{2 \cdot I_7}{K'_N (V_{DS7}(\text{sat}))^2}$	$V_{SD6}(\text{sat}) = V_{DD} - V_{OH}$ $V_{DS7}(\text{sat}) = V_{OL} - V_{SS}$
3	Guess C_I as 0.1–0.5 pF $\therefore I_3 = I_7 \frac{2C_I}{C_{II}}$	A result of choosing $m = 1$; will check C_I later
4	$\frac{W_3}{L_3} = \frac{W_4}{L_4} = \frac{I_3}{K'_P (V_{SG3} - V_{TP})^2}$	$V_{SG3} = V_{DD} - V_{icm}^+ + V_{TH}$
5	$g_{m1} = \frac{A_v(0)(g_{ds2} + g_{ds4})(g_{ds6} + g_{ds7})}{g_{m6}}$	$g_{m6} \approx \sqrt{\frac{2K'_P W_6 I_6}{L_6}}$
	$\frac{W_1}{L_1} = \frac{W_2}{L_2} = \frac{g_{m1}^2}{K'_N I_3}$	$A_v(0) = \frac{V_{OH} + V_{OL}}{V_{in}(\min)}$
6	Find C_I and check assumption $C_I = C_{gd2} + C_{gd4} + C_{gs6} + C_{hd2} + C_{hd4}$ If C_I is greater than the guess in step 3, then increase the value of C_I and repeat steps 4 through 6	$AD_2 = W_2(L_1 + L_2 + L_3)$ $PD_2 = 2(W_2 + L_1 + L_2 + L_3)$ $AD_4 = W_4(L_1 + L_2 + L_3)$ $PD_4 = 2(W_4 + L_1 + L_2 + L_3)$
7	$V_{DS5}(\text{sat}) = V_{icm}^- - V_{GS1} - V_{SS}$ $\frac{W_5}{L_5} = \frac{2 \cdot I_3}{K'_N (V_{DS5}(\text{sat}))^2}$	If $V_{DS5}(\text{sat})$ is less than 100 mV, increase W_1/L_1

DESIGN OF THE TWO-STAGE, OPEN-LOOP COMPARATOR OF FIG. 8.2-3 FOR A LINEAR RESPONSE

Assume the specifications of Fig. 8.2-3 are given below:

$$\begin{array}{lll}
 t_p = 50 \text{ ns} & V_{OH} = 2 \text{ V} & V_{OL} = -2 \text{ V} \\
 V_{DD} = 2.5 \text{ V} & V_{SS} = -2.5 \text{ V} & C_{II} = 5 \text{ pF} \\
 V_{in}(\min) = 1 \text{ mV} & V_{icm}^+ = 2 \text{ V} & V_{icm}^- = -1.25 \text{ V}
 \end{array}$$

Also assume that the overdrive will be a factor of 10. Design a two-stage, open-loop comparator using Fig. 8.2-3 to achieve the above specifications and assume that all channel lengths are to be 1 μm .

Solution

Following the procedure outlined in Table 8.2-2, we choose $m = 1$ to get

$$|p_I| = |p_{II}| = \frac{10^9}{50\sqrt{10}} = 6.32 \times 10^6 \text{ rad/s}$$

This gives

$$I_6 = I_7 = \frac{6.32 \times 10^6 \cdot 5 \times 10^{-12}}{0.04 + 0.05} = 351 \mu\text{A} \rightarrow I_6 = I_7 = 400 \mu\text{A}$$

Therefore,

$$\frac{W_6}{L_6} = \frac{2 \cdot 400}{(0.5)^2 \cdot 50} = 64 \quad \text{and} \quad \frac{W_7}{L_7} = \frac{2 \cdot 400}{(0.5)^2 \cdot 110} = 29$$

Next, we guess $C_I = 0.2$ pF. This gives $I_3 = 32 \mu\text{A}$ and we will increase it to $40 \mu\text{A}$ for a margin of safety. Step 4 gives V_{SG3} as 1.2 V, which results in

$$\frac{W_3}{L_3} = \frac{W_4}{L_4} = \frac{40}{50(1.2 - 0.7)^2} = 3.2 \rightarrow \frac{W_3}{L_3} = \frac{W_4}{L_4} = 4$$

The desired gain is found to be 4000, which gives an input transconductance of

$$g_{m1} = \frac{4000 \cdot 0.09 \cdot 20}{44.44} = 162 \mu\text{S}$$

This gives the W/L ratios of M1 and M2 as

$$\frac{W_1}{L_1} = \frac{W_2}{L_2} = \frac{(162)^2}{110 \cdot 40} = 5.96 \rightarrow \frac{W_1}{L_1} = \frac{W_2}{L_2} = 6$$

To check the guess for C_I we need to calculate it, which is done as

$$C_I = C_{gd2} + C_{gd4} + C_{gs6} + C_{bd2} + C_{bd4} = 0.9 \text{ fF} + 1.3 \text{ fF} + 119.5 \text{ fF} + 20.4 \text{ fF} + 36.8 \text{ fF} = 178.9 \text{ fF}$$

which is less than what was guessed so we will make no changes.

Finally, the W/L value of M5 is found by finding V_{GS1} as 0.946 V, which gives $V_{DS5}(\text{sat}) = 0.304$ V. This gives

$$\frac{W_5}{L_5} = \frac{2 \cdot 40}{(0.304)^2 \cdot 110} = 7.87 \approx 8$$

Obviously, M5 and M7 cannot be connected gate–gate and source–source. The values of I_3 and I_7 must be derived separately as illustrated in Fig. 8.2-8. The W values are summarized below assuming that all channel lengths are $1 \mu\text{m}$.

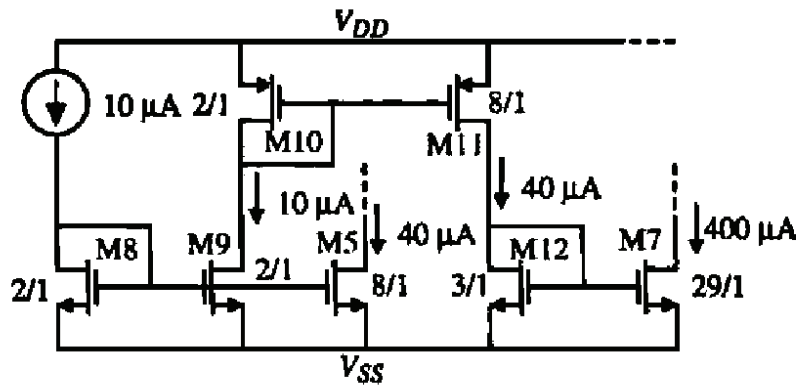


Figure 8.2-8 Biasing scheme for the comparator of Example 8.2-6.

$$W_1 = W_2 = 6 \mu\text{m} \quad W_3 = W_4 = 4 \mu\text{m} \quad W_5 = 8 \mu\text{m}$$

$$W_6 = 64 \mu\text{m} \quad W_7 = 29 \mu\text{m}$$

The design of the slewing, two-stage, open-loop comparator has a different focus than the design suggested in Table 8.2-2 for the linear response. In this case we assume that the large-signal conditions dominate the design. A typical design procedure for the slewing case is shown in Table 8.2-3.

TABLE 8.2-3 Design of the Two-Stage, Open-Loop Comparator of Fig. 8.2-3 for a Slewing Response

Specifications: t_p , C_{II} , $V_{in}(\text{min})$, V_{OH} , V_{OL} , V_{cm}^- , and V_{cm}^+
Constraints: Technology, V_{DD} , and V_{SS}

Step	Design Relationships	Comments
1	$I_7 = I_6 = C_{II} \frac{dv_{out}}{dt} = \frac{C_{II}(V_{OH} - V_{OL})}{t_p}$	Assume the trip point of the output is $(V_{OH} - V_{OL})/2$
2	$\frac{W_6}{L_6} = \frac{2 \cdot I_6}{K'_P(V_{SD6}(\text{sat}))^2}$ and $\frac{W_7}{L_7} = \frac{2 \cdot I_7}{K'_N(V_{DS7}(\text{sat}))^2}$	$V_{SD6}(\text{sat}) = V_{DD} - V_{OH}$ $V_{DS7}(\text{sat}) = V_{OL} - V_{SS}$
3	Guess a value of C_I and check later	Typically $0.1 \text{ pF} < C_I < 0.5 \text{ pF}$
4	$I_3 = C_I \frac{dv_{o1}}{dt} = \frac{C_I(V_{OH} - V_{OL})}{t_p}$	Assume that v_{o1} swings between V_{OH} and V_{OL}
5	$\frac{W_3}{L_3} = \frac{W_4}{L_4} = \frac{I_3}{K'_P(V_{SG3} - V_{TP})^2}$	$V_{SG3} = V_{DD} - V_{cm}^+ + V_{TN}$
6	$g_{m1} = \frac{A_v(0)(g_{ds2} + g_{ds4})(g_{ds6} + g_{ds7})}{g_{m6}}$ $\frac{W_1}{L_1} = \frac{W_2}{L_2} = \frac{g_{m1}^2}{K'_N I_5}$	$g_{m6} = \sqrt{\frac{2K'_P W_6 I_6}{L_6}}$ $A_v(0) = \frac{V_{OH} + V_{OL}}{V_{in}(\text{min})}$
7	Find C_I and check assumption $C_I = C_{gd2} + C_{gd4} + C_{gm6} + C_{bd2} + C_{bd4}$ If C_I is greater than the guess in step 3, increase the value of C_I and repeat steps 4 through 6	$AD_2 = W_2(L_1 + L_2 + L_3)$ $PD_2 = 2(W_2 + L_1 + L_2 + L_3)$ $AD_4 = W_4(L_1 + L_2 + L_3)$ $PD_4 = 2(W_4 + L_1 + L_2 + L_3)$
8	$V_{DS3}(\text{sat}) = V_{cm}^- - V_{GS1} - V_{SS}$, $\frac{W_5}{L_5} = \frac{2 \cdot I_5}{K'_N(V_{DS3}(\text{sat}))^2}$	If $V_{DS3}(\text{sat})$ is less than 100 mV, increase W_1/L_1

PROBLEM 8.23

DESIGN OF THE TWO-STAGE, OPEN-LOOP COMPARATOR OF FIG. 8.2-3 FOR A SLEWING RESPONSE

Assume the specifications of Fig. 8.2-3 are given below.

$$\begin{array}{lll} t_p = 50 \text{ ns} & V_{OH} = 2 \text{ V} & V_{OL} = -2 \text{ V} \\ V_{DD} = 2.5 \text{ V} & V_{SS} = -2.5 \text{ V} & C_{II} = 5 \text{ pF} \\ V_{in}(\text{min}) = 1 \text{ mV} & V_{icm}^+ = 2 \text{ V} & V_{icm}^- = -1.25 \text{ V} \end{array}$$

Design a two-stage, open-loop comparator using the circuit of Fig. 8.2-3 to the above specifications and assume all channel lengths are to be $1 \mu\text{m}$.

Solution

Following the procedure outlined in Table 8.2-3, we calculate I_6 and I_7 as

$$I_6 = I_7 = \frac{5 \times 10^{-12} \cdot 4}{50 \times 10^{-9}} = 400 \mu\text{A}$$

Therefore,

$$\frac{W_6}{L_6} = \frac{2 \cdot 400}{(0.5)^2 \cdot 50} = 64 \quad \text{and} \quad \frac{W_7}{L_7} = \frac{2 \cdot 400}{(0.5)^2 \cdot 110} = 29$$

Next, we guess $C_f = 0.2 \text{ pF}$. This gives

$$I_5 = \frac{(0.2 \text{ pF})(4 \text{ V})}{50 \text{ ns}} = 16 \mu\text{A} \rightarrow I_5 = 20 \mu\text{A}$$

Step 5 gives V_{SG3} as 1.2 V , which results in

$$\frac{W_3}{L_3} = \frac{W_4}{L_4} = \frac{20}{50(1.2 - 0.7)^2} = 1.6 \rightarrow \frac{W_3}{L_3} = \frac{W_4}{L_4} = 2$$

The desired gain is found to be 4000, which gives an input transconductance of

$$g_{m1} = \frac{4000 \cdot 0.09 \cdot 10}{44.44} = 81 \mu\text{S}$$

This gives the W/L ratios of M1 and M2 as

$$\frac{W_3}{L_3} = \frac{W_4}{L_4} = \frac{(81)^2}{100} = 1.49 \rightarrow \frac{W_1}{L_1} = \frac{W_2}{L_2} = 2$$

To check the guess for C_I we need to calculate it, which is done as

$$C_I = C_{gd2} + C_{gd4} + C_{gs6} + C_{hd2} + C_{hd4} = 0.9 \text{ fF} + 0.4 \text{ fF} + 119.5 \text{ fF} + 20.4 \text{ fF} + 15.3 \text{ fF} \\ = 156.5 \text{ fF}$$

which is less than what was guessed.

Finally, the W/L value of M5 is found by finding V_{GS1} as 1.00 V, which gives $V_{DS5}(\text{sat}) = 0.25$ V. This gives

$$\frac{W_5}{L_5} = \frac{2 \cdot 20}{(0.25)^2 \cdot 110} = 5.8 \approx 6$$

As in the previous example, M5 and M7 cannot be connected gate–gate and source–source and a scheme like Fig. 8.2-8 must be used. The W values are summarized below assuming that all channel lengths are 1 μm .

$$\begin{array}{lll} W_1 = W_2 = 2 \mu\text{m} & W_3 = W_4 = 4 \mu\text{m} & W_5 = 6 \mu\text{m} \\ W_6 = 64 \mu\text{m} & W_7 = 29 \mu\text{m} & \end{array}$$

The above examples should help to illustrate the design of a two-stage, open-loop comparator. It is interesting to note there may be little difference in a comparator designed for linear response or for slewing response. This comes about from the fact that what causes the poles to be large is also what causes the slew rate to be fast. For example, large poles require low resistance and small capacitance from a node to ac ground. Low resistances come from larger bias currents. Hence, large bias currents and smaller capacitors lead to improved slew rate. Generally, a fast comparator will also be one that dissipates more power. In the next section, we will examine other forms of the open-loop comparator that offer more trade-offs between speed and power.

8.3 OTHER OPEN-LOOP COMPARATORS

There are many other types of comparators besides the two-stage comparator of the previous section. In fact, most of the op amps of the previous two chapters could be used as comparators. In this section we will examine comparators with push–pull outputs, the folded-cascode comparator, and comparators capable of driving very large capacitive loads.

Push–Pull Output Comparators

We noted in the two-stage comparator of the previous section that the propagation delay time was due to both the transition of the first-stage output and the second-stage output. If we replace the current-mirror load in the first stage with MOS diodes (gate–drain-connected MOSFETs), then the signal at the output of the first stage will be reduced in magnitude. This type of comparator is called a *clamped* comparator and is shown in Fig. 8.3-1.

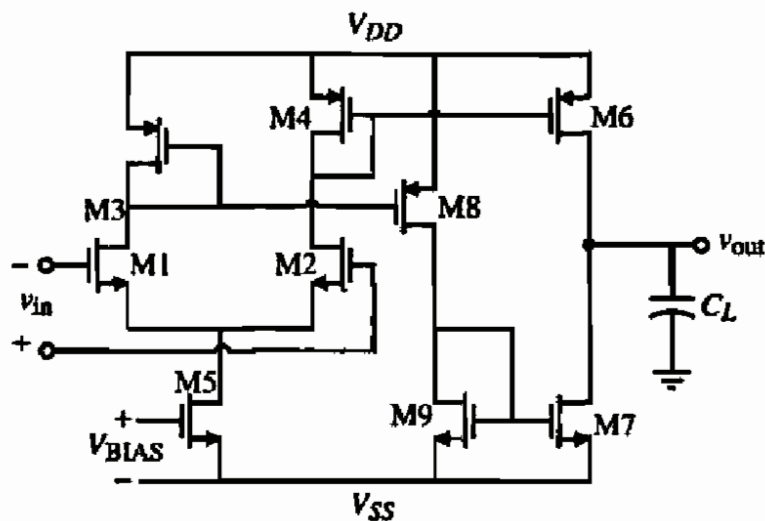


Figure 8.3-1 Clamped push-pull output comparator.

There are several interesting features of Fig. 8.3-1. First, the gain has been reduced because the current-mirror load of the first stage has been replaced by MOS diodes. Second, we note that the output is push-pull. The maximum sinking and sourcing current at the output would be I_5 times any current gain in M3–M8 (M4–M6). The gain equivalent to a two-stage comparator can be achieved by cascoding the output as shown in Fig. 8.3-2. We note that this circuit is simply the op amp of Fig. 6.5-4. The large output resistance leads to a single-pole response. This pole is at lower frequencies than the poles of the two-stage, open-loop comparator and therefore the linear response will be slower with the same amount of overdrive. However, because the comparator is push-pull, it will be able to sink and source large currents into the output capacitance, C_H . The design procedure used in Example 6.5-2 can be applied to this circuit as well.

The dynamics of Fig. 8.3-2 depend on the output resistance, R_{out} . From Example 6.5-2, the output resistance is about 11 M Ω . If C_H is 5 pF, the dominant pole is -18.12 krad/s. For an overdrive factor of 10, Eq. (8.1-7) gives a propagation delay time of 2.83 μ s. Compared to the two-stage, open-loop comparator of Example 8.2-6 this is much slower. However, if the comparator is slewing, then the clamped comparator with a cascoded output stage can compete with the two-stage, open-loop comparator.

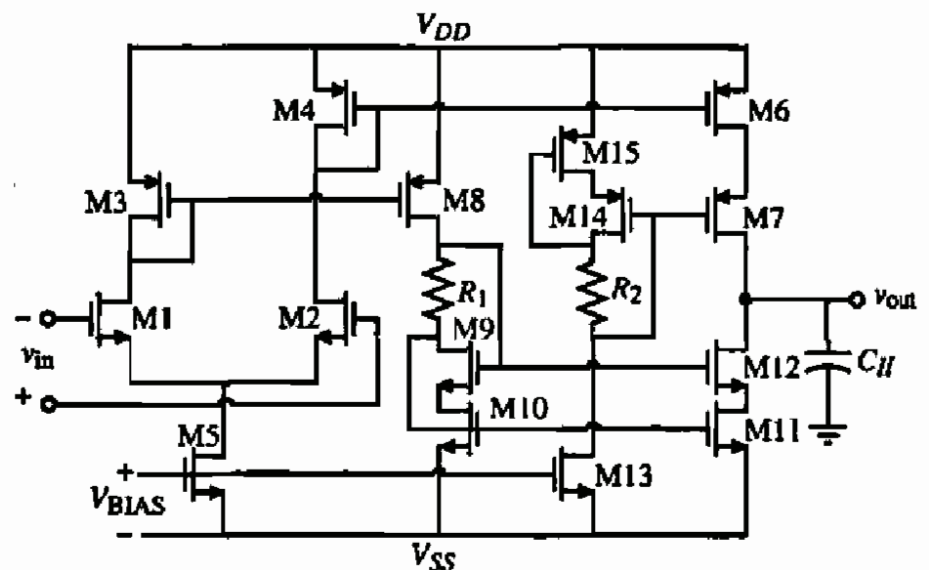


Figure 8.3-2 Clamped comparator of Fig. 8.3-1 using a cascode output stage.

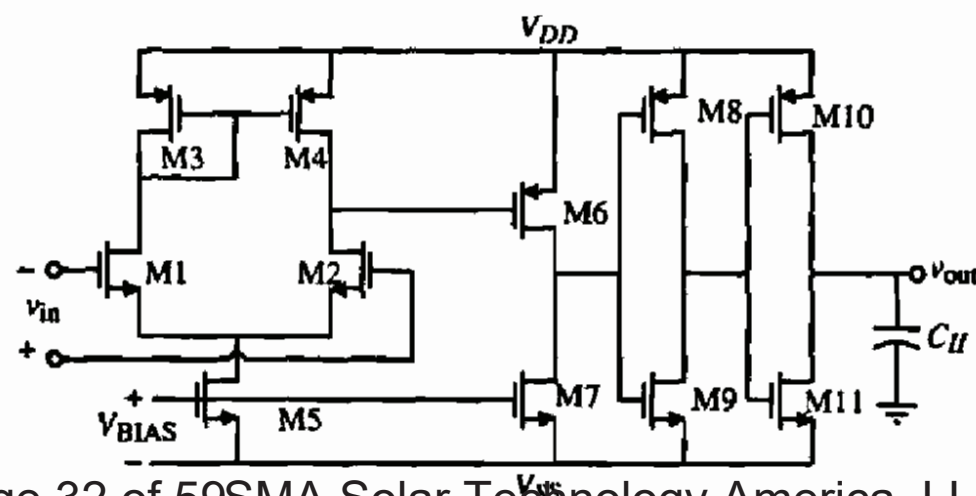
The folded-cascode op amp of Chapter 6 also makes a satisfactory comparator. Its performance is similar to the comparator of Fig. 8.3-2. The primary difference would be a better input common-mode voltage range because the MOS diodes are not used to load the first stage. From a linear speed viewpoint, the comparators with cascoded output stage are slow. In general, these types of comparators should not be used if the response is to be linear. They do have satisfactory performance as a comparator if the response is slewing.

Comparators That Can Drive Large Capacitive Loads

If a comparator has a large capacitive load, the chances are that it is slew rate limited. Under these conditions, we will show several methods capable of driving large values of C_H . The first method is simply to add several push-pull inverters in cascade with the output of a two-stage, open-loop comparator as shown in Fig. 8.3-3.

The inverters, M8–M9 and M10–M11, allow C_H to be large without sacrificing the speed. The principle is well understood in high-speed digital buffers. If a large capacitance was connected to the drains of M6 and M7, the slew rate would be poor because the current sinking and sourcing is not large. The M8–M9 inverter allows the current driving capability to be increased without sacrificing the slew rate. The W/L value of M8 and M9 must be large enough to increase the current sinking and sourcing capability without loading M6 and M7. Similarly, the inverter M10–M11 allows the current sinking and sourcing to be further increased without loading M8–M9. It can be shown that, if the W/L increases by a factor of 2.72, the minimum propagation delay time is achieved. However, this is a very broad optimum so that larger factors like 10 are used to reduce the required number of stages.

The overdrive techniques introduced for low-power op amps in Section 7.4 can be used for comparators to increase the output current sinking and sourcing capability of the comparator. These methods included boosting the tail current (Fig. 7.4-4) and using current mirrors whose output transistor switches from the active to the saturation region when output current is required (Fig. 7.4-6). Another circuit that has the ability to sink and source large amounts of current is called the self-biased differential amplifier [2] and is shown in Fig. 8.3-4. This amplifier consists of two differential amplifiers each serving as the load for the other as illustrated in Fig. 8.3-4(a). The tail currents of the differential amplifiers become adaptive by connecting the gates of M5 and M6 to the drains of M1 and M3 as shown in



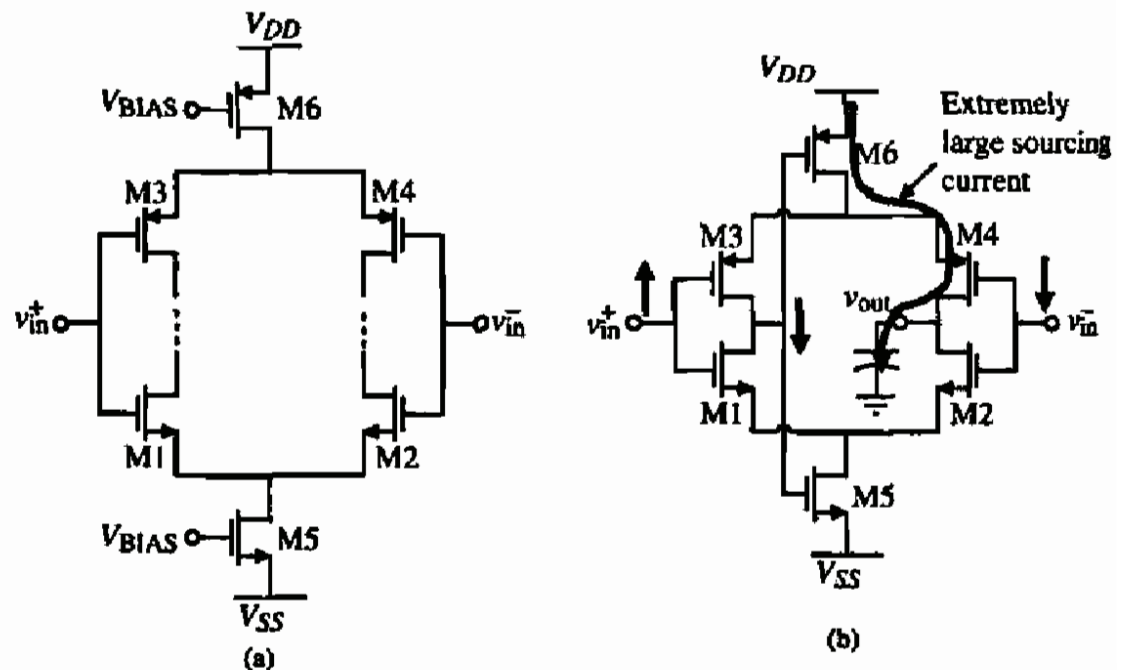


Figure 8.3-4 (a) Two differential amplifiers loading each other, (b) Evolution of (a) into the self-biased differential amplifier.

Fig. 8.3-4(b). When the positive input voltage, v_{in}^+ , is increased, the drains of M1 and M3 fall and turn on M6 to a large current, which is sourced to the output capacitance connected to the drains of M2 and M4 through M4. During this condition, the current in M5 is zero. When v_{in}^+ is decreased, M5 turns on and a large current is sunk through the output capacitance via M2. Thus, this circuit has the ability to source and sink large currents without a large quiescent current. A disadvantage of the circuit is that the delay time from v_{in}^+ to the output is slower than from v_{in}^- to the output.

8.4 IMPROVING THE PERFORMANCE OF OPEN-LOOP COMPARATORS

There are two areas in which the performance of an open-loop, high-gain comparator can be improved with little extra effort. These areas are the input-offset voltage and a single transition of the comparator in a noisy environment. The first problem can be solved by *autozeroing* and the second can be solved by the introduction of hysteresis using a bistable circuit. These two techniques will be examined in the following.

Autozeroing Techniques

Input-offset voltage can be a particularly difficult problem in comparator design. In precision applications, such as high-resolution A/D converters, large input-offset voltages cannot be tolerated. While systematic offset can nearly be eliminated with proper design (though still affected by process variations), random offsets still remain and are unpredictable. Fortunately, there are techniques in MOS technology to remove a large portion of the input offset using offset-cancellation techniques. These techniques are available in MOS because of the nearly infinite input resistance of MOS transistors. This characteristic allows long-term storage of voltages on the transistor's gate. As a result, offset voltages can be measured, stored on capacitors, and summed with the input so as to cancel the offset.

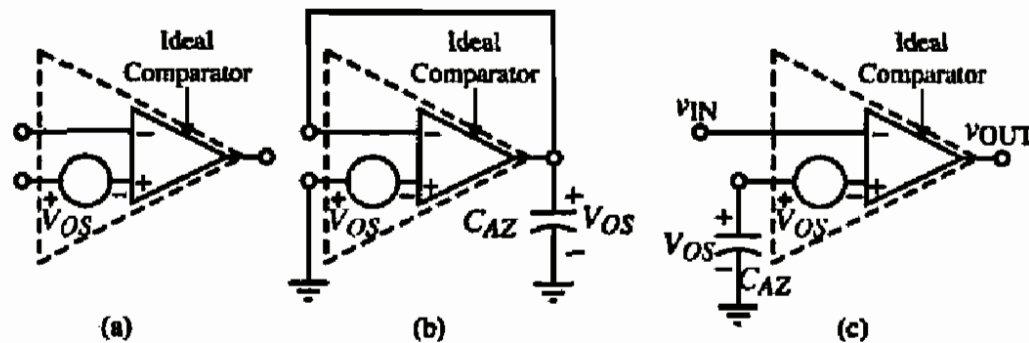


Figure 8.4-1 (a) Simple model of a comparator including offset. (b) Comparator in unity-gain configuration storing the offset on autozero capacitor C_{AZ} during the first half of the autozero cycle. (c) Comparator in open-loop configuration with offset cancellation achieved at the noninverting input during the second half of the autozero cycle.

Figure 8.4-1 shows symbolically an offset-cancellation algorithm. A model of a comparator with an input-offset voltage is shown in Fig. 8.4-1(a). A known polarity is given to the offset voltage for convenience. Neither the value nor the polarity can be predicted in reality. Figure 8.4-1(b) shows the comparator connected in the unity-gain configuration so that the input offset is available at the output. In order for this circuit to work properly, it is necessary that the comparator be stable in the unity-gain configuration. This implies that only self-compensated high-gain amplifiers would be suitable for autozeroing. One could use the two-stage, open-loop comparator but a compensation circuit should be switched into the circuit during autozeroing. In the final operation of the autozero algorithm C_{AZ} is placed at the input of the comparator in series with V_{OS} . The voltage across C_{AZ} adds to V_{OS} , resulting in zero volts at the noninverting input of the comparator. Since there is no dc path to discharge the autozero capacitor, the voltage across it remains indefinitely (in the ideal case). In reality, there are leakage paths in shunt with C_{AZ} that can discharge it over a period of time. The solution to this problem is to repeat the autozero cycle periodically.

A practical implementation of a differential-input, autozeroed comparator is shown in Fig. 8.4-2(a). The comparator is modeled with an offset-voltage source as before. Figure 8.4-2(b) shows the state of the circuit during the first phase of the cycle when ϕ_1 is high. The offset is stored across C_{AZ} . Figure 8.4-2(c) shows the circuit in the second phase of the autozero cycle when ϕ_2 is high. The offset is canceled by the addition of V_{OS} on C_{AZ} . It is during this portion of the cycle that the circuit functions as a comparator.

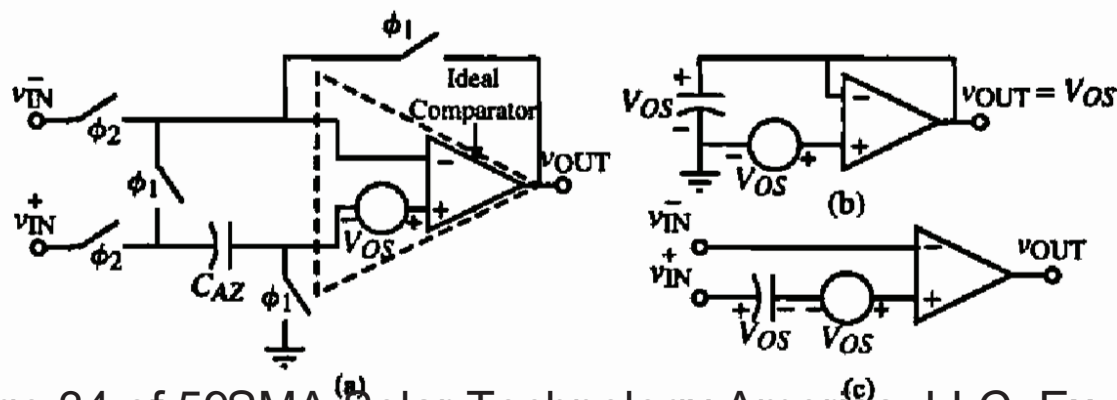


Figure 8.4-2 (a) Differential circuit implementation of an autozeroed comparator. (b) Comparator during ϕ_1 phase. (c) Comparator during ϕ_2 phase.

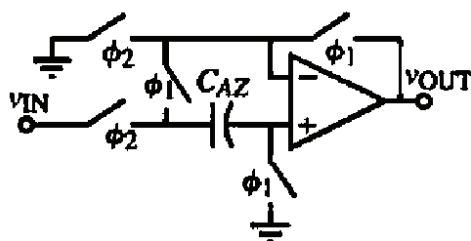


Figure 8.4-3 Noninverting autozeroed comparator.

There are other ways to implement an autozeroed comparator other than the one just described. A slight variation of Fig. 8.4-2(a) is shown in Fig. 8.4-3. This is a noninverting version of the previous autozeroed comparator. Yet another version is shown in Fig. 8.4-4. This one is simpler in operation since the noninverting input is always connected to ground.

The switch implementations of the autozeroed comparator can be single-channel MOSFETs or complementary MOSFETs. It is important to use nonoverlapping clocks to drive the switches so that any given switch turns off before another turns on. Autozeroing techniques can be very effective in removing a large amount of a comparator's input offset, but the offset cancellation is not perfect. Charge injection resulting from clock feedthrough (Section 4.1) can by itself introduce an offset. This too can be canceled, but it is usually the cause of the lower limit of the offset voltage being greater than zero.

Comparator Using Hysteresis

Often a comparator is placed in a very noisy environment in which it must detect signal transitions at the threshold point. If the comparator is fast enough (depending on the frequency of the most prevalent noise) and the amplitude of the noise is great enough, the output will also be noisy. In this situation, a modification on the transfer characteristic of the comparator is desired. Specifically, hysteresis is needed in the comparator.

Hysteresis is the quality of the comparator in which the input threshold changes as a function of the input (or output) level. In particular, when the input passes the threshold, the output changes and the input threshold is subsequently reduced so that the input must return beyond the previous threshold before the comparator's output changes state again. This can be illustrated much more clearly with the diagram shown in Fig. 8.4-5. Note that as the input starts negative and goes positive, the output does not change until it reaches the positive trip point, V_{TRP}^+ . Once the output goes high, the effective trip point is changed. When the input returns in the negative direction, the output does not switch until it reaches the negative trip point, V_{TRP}^- .

The advantage of hysteresis in a noisy environment can clearly be seen from the illustration given in Fig. 8.4-6. In this figure, a noisy signal is shown as the input to a comparator without hysteresis. The intent is to have the comparator output follow the low-frequency signal. Because of noise variations near the threshold points, the comparator output is too noisy. The response of the comparator can be improved by adding hysteresis equal to or greater than the amount of the largest expected noise amplitude. The response of such a comparator is shown in Fig. 8.4-6(b).

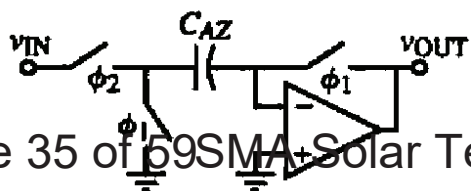


Figure 8.4-4 Inverting autozeroed comparator.

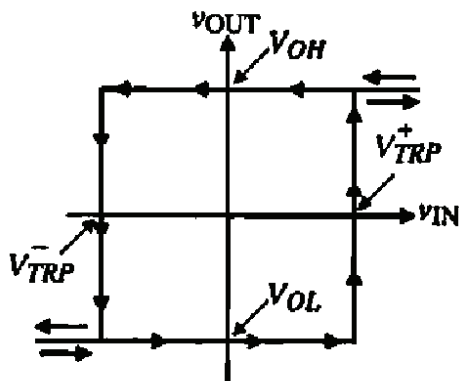


Figure 8.4-5 Comparator transfer curve with hysteresis.

The voltage-transfer function shown in Fig. 8.4-5 is called a *bistable* characteristic. A bistable circuit can be clockwise or counterclockwise. Figure 8.4-5 is an example of a counterclockwise bistable characteristic. Sometimes, the counterclockwise bistable circuit is called noninverting and the clockwise bistable is called inverting. The bistable characteristic is defined by its width and height and whether it is clockwise or counterclockwise. The width is given by the difference between V_{TRP}^+ and V_{TRP}^- . The height is generally the difference between V_{OH} and V_{OL} . In addition, the bistable characteristic can be shifted horizontally to the left or right by addition of a dc offset voltage.

There are many ways to introduce hysteresis in a comparator. All of them use some form of positive feedback. The methods can be categorized into external methods and internal methods. External hysteresis uses external positive feedback to implement hysteresis and can be accomplished after the comparator is built. Internal hysteresis is implemented into the comparator and does not require external feedback. We shall examine these two methods in the following.

Figure 8.4-7 shows a noninverting bistable circuit using external positive feedback to accomplish the hysteresis. This bistable characteristic is counterclockwise. We assume that the maximum and minimum output voltages of the comparator are V_{OH} and V_{OL} , respectively. The trip points are found as follows. Assume that v_{IN} is much less than the voltage at the positive input to the comparator. In this case, the output voltage will be at V_{OL} . As v_{IN} is increased, the upper trip point, V_{TRP}^+ , is found by setting the voltage due to v_{IN} and V_{OL} at the positive input to the comparator equal to zero. This results in

$$0 = \left(\frac{R_1}{R_1 + R_2} \right) V_{OL} + \left(\frac{R_2}{R_1 + R_2} \right) V_{TRP}^+ \quad (8.4-1)$$

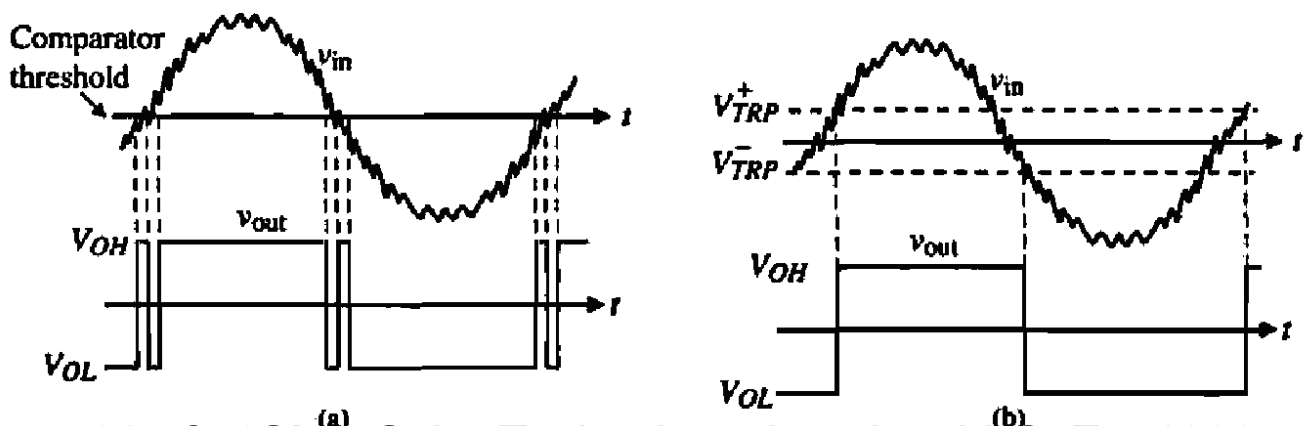


Figure 8.4-6 (a) Comparator response to a noisy input. (b) Comparator response to a noisy input when hysteresis is added.

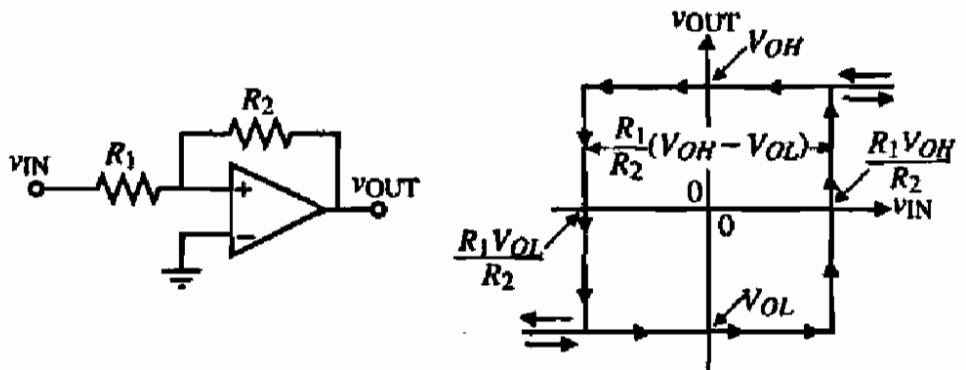


Figure 8.4-7 Noninverting bistable circuit using external positive feedback.

Solving for the upper trip point gives

$$V_{TRP}^+ = -\frac{R_1}{R_2} V_{OL} \quad (8.4-2)$$

Generally, V_{OL} is negative so that the upper trip point is a positive voltage.

The lower trip point, V_{TRP}^- , can be found by assuming that v_{IN} is much greater than the voltage at the positive input to the comparator so that the output state, which is V_{OH} , is known. As v_{IN} is decreased, V_{TRP}^- occurs when the voltage at the positive input to the comparator is equal to zero. Therefore,

$$0 = \left(\frac{R_1}{R_1 + R_2}\right)V_{OH} + \left(\frac{R_2}{R_1 + R_2}\right)V_{TRP}^- \quad (8.4-3)$$

which gives

$$V_{TRP}^- = -\frac{R_1}{R_2} V_{OH} \quad (8.4-4)$$

The width of the bistable characteristic is given as

$$\Delta V_{in} = V_{TRP}^+ - V_{TRP}^- = \left(\frac{R_1}{R_2}\right)(V_{OH} - V_{OL}) \quad (8.4-5)$$

The counterclockwise bistable circuit resulting from this analysis is shown in Fig. 8.4-7.

Figure 8.4-8 shows the clockwise bistable circuit using external positive feedback. Assuming that the input is much less than the voltage at the positive input of the comparator allows us to define the output state at V_{OH} . The upper trip point can be found by setting the input equal to the voltage at the positive input of the comparator. The result is

$$v_{IN} = V_{TRP}^+ = \left(\frac{R_1}{R_1 + R_2}\right)V_{OH} \quad (8.4-6)$$

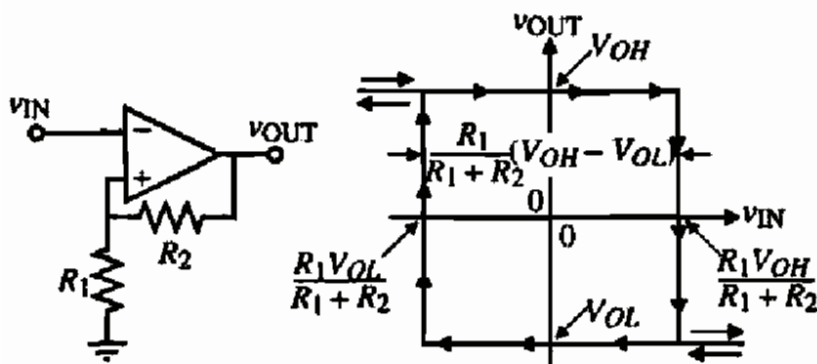


Figure 8.4-8 Inverting bistable circuit using external positive feedback.

Next, assuming that the input is much greater than the voltage at the positive input of the comparator defines the output voltage as V_{OL} . The lower trip point can be found by setting the input equal to the voltage at the positive input of the comparator. Therefore,

$$v_{IN} = V_{TRP}^- = \left(\frac{R_1}{R_1 + R_2} \right) V_{OL} \quad (8.4-7)$$

The width of the bistable characteristic is given as

$$\Delta V_{in} = V_{TPR}^+ - V_{TRP}^- = \left(\frac{R_1}{R_1 + R_2} \right) (V_{OH} - V_{OL}) \quad (8.4-8)$$

The clockwise bistable circuit resulting from this analysis is shown in Fig. 8.4-8.

The center point of the bistable characteristics of Figs. 8.4-7 and 8.4-8 can be shifted horizontally by inserting a battery, V_{REF} , as shown in Fig. 8.4-9 for the counterclockwise bistable circuit. If we solve for the trip points of the counterclockwise bistable circuit in Fig. 8.4-9 we get

$$V_{REF} = \left(\frac{R_1}{R_1 + R_2} \right) V_{OL} + \left(\frac{R_2}{R_1 + R_2} \right) V_{TRP}^+ \quad (8.4-9)$$

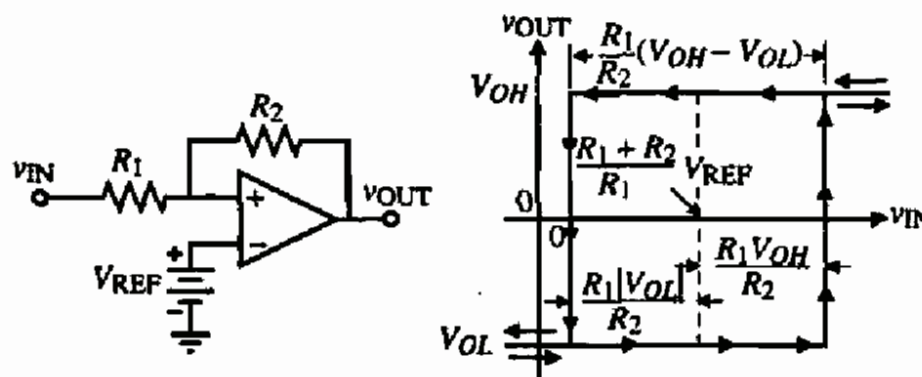


Figure 8.4-9 Horizontally shifted noninverting bistable circuit using external positive feedback.

DESIGN OF AN INVERTING COMPARATOR WITH HYSTERESIS

Use the circuit of Fig. 8.4-10 to design a high-gain, open-loop comparator having an upper trip point of 1 V and a lower trip point of 0 V if $V_{OH} = 2$ V and $V_{OL} = -2$ V.

Solution

Putting the values of this example into Eqs. (8.4-13) and (8.4-14) gives

$$1 = \left(\frac{R_1}{R_1 + R_2} \right) 2 + \left(\frac{R_1}{R_1 + R_2} \right) V_{REF}$$

and

$$0 = \left(\frac{R_1}{R_1 + R_2} \right) (-2) + \left(\frac{R_1}{R_1 + R_2} \right) V_{REF}$$

Solving these two equations gives $3R_1 = R_2$ and $V_{REF} = 2$ V.

The previous circuits are examples of using external positive feedback to implement hysteresis in a high-gain, open-loop comparator. The hysteresis can also be accomplished by using internal positive feedback. Figure 8.4-11 shows the differential input stage of a comparator such as Fig. 8.3-1 or 8.3-2 [1]. In this circuit there are two paths of feedback. The first is current-series [3,4] feedback through the common-source node of transistors M1 and M2. This feedback path is negative. The second path is the voltage-shunt feedback through the gate-drain connections of transistors M6 and M7. This path of feedback is positive. If the positive-feedback factor is less than the negative-feedback factor, then the overall feedback will be negative and no hysteresis will result. If the positive-feedback factor becomes greater, the overall feedback will be positive, which will give rise to hysteresis in the voltage-transfer curve. As long as the ratio β_6/β_3 is less than one, there is no hysteresis in the transfer function. When this ratio is greater than one, hysteresis will result. The following analysis will develop the equations for the trip points when there is hysteresis.

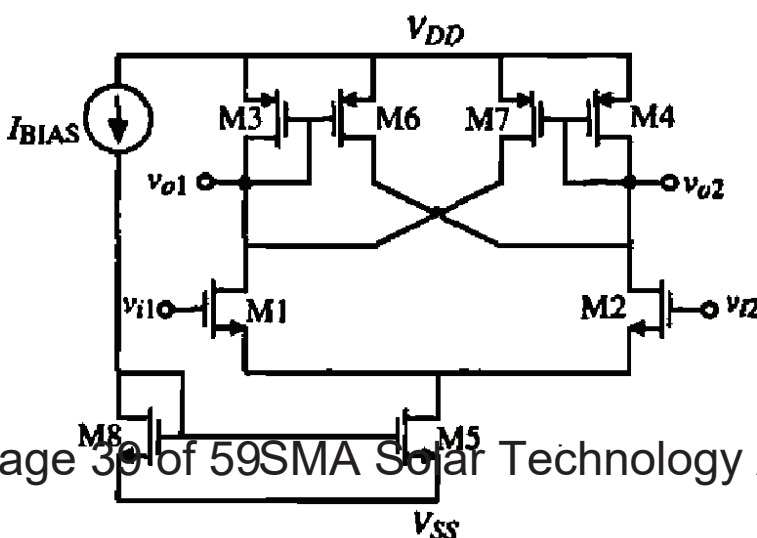


Figure 8.4-11 Implementation of hysteresis using internal positive feedback in the input stage of a high-gain, open-loop comparator.

Assume that plus and minus supplies are used and that the gate of M1 is tied to ground. With the input of M2 much less than zero, M1 is on and M2 off, thus turning on M3 and M6 and turning off M4 and M7. All of i_5 flows through M1 and M3, so v_{o2} is high. The resulting circuit is shown in Fig. 8.4-12(a). Note that M2 is shown even though it is off. At this point, M6 is attempting to source the following amount of current:

$$i_6 = \frac{(W/L)_6}{(W/L)_3} i_5 \quad (8.4-15)$$

As v_{in} increases toward the threshold point (which is not yet known), some of the tail current i_5 begins to flow through M2. This continues until the point where the current through M2 equals the current in M6. Just beyond this point the comparator switches state. To approximately calculate one of the trip points, the circuit must be analyzed right at the point where i_2 equals i_6 . Mathematically this is

$$i_6 = \frac{(W/L)_6}{(W/L)_3} i_3 \quad (8.4-16)$$

$$i_2 = i_6 \quad (8.4-17)$$

$$i_5 = i_2 + i_1 \quad (i_1 = i_3) \quad (8.4-18)$$

Therefore,

$$i_3 = \frac{i_5}{1 + [(W/L)_6/(W/L)_3]} = i_1 \quad (8.4-19)$$

$$i_2 = i_5 - i_1 \quad (8.4-20)$$

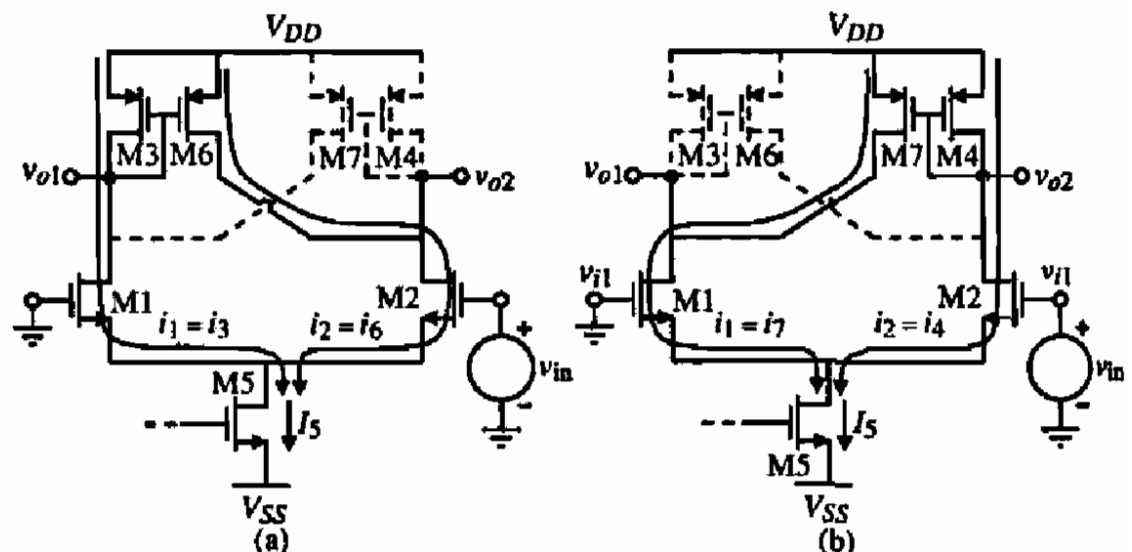


Figure 8.4-12 (a) Comparator of Fig. 8.4-11 where v_{in} is very negative and increasing toward V_{TRP} . (b) Comparator of Fig. 8.4-11 where v_{in} is very positive and decreasing toward V_{TRP} .

Knowing the currents in both M1 and M2, it is easy to calculate their respective v_{GS} voltages. Since the gate of M1 is at ground, the difference in their gate–source voltages will yield the positive trip point as given below:

$$v_{GS1} = \left(\frac{2i_1}{\beta_1} \right)^{1/2} + V_{T1} \quad (8.4-21)$$

$$v_{GS2} = \left(\frac{2i_2}{\beta_2} \right)^{1/2} + V_{T2} \quad (8.4-22)$$

$$V_{TRP}^+ = v_{GS2} - v_{GS1} \quad (8.4-23)$$

Once the threshold is reached, the comparator changes state so that the majority of the tail current now flows through M2 and M4. As a result, M7 is also turned on, thus turning off M3, M6, and M1. As in the previous case, as the input decreases the circuit reaches a point at which the current in M1 increases until it equals the current in M7. The input voltage at this point is the negative trip point V_{TRP}^- . The equivalent circuit in this state is shown in Fig. 8.4-12(b). To calculate the trip point, the following equations apply:

$$i_7 = \frac{(W/L)_7}{(W/L)_4} i_4 \quad (8.4-24)$$

$$i_1 = i_7 \quad (8.4-25)$$

$$i_5 = i_2 + i_1 \quad (8.4-26)$$

Therefore,

$$i_4 = \frac{i_5}{1 + [(W/L)_7/(W/L)_4]} = i_2 \quad (8.4-27)$$

$$i_1 = i_5 - i_2 \quad (8.4-28)$$

Using Eqs. (8.4-21) and (8.4-22) to calculate v_{GS} , the trip point is

$$V_{TRP}^- = v_{GS2} - v_{GS1} \quad (8.4-29)$$

These equations do not take into account the effect of channel length modulation. Their use is illustrated in the following example.

CALCULATION OF TRIP VOLTAGES FOR A COMPARATOR WITH HYSTERESIS

Consider the circuit shown in Fig. 8.4-11. Using the transistor device parameters given in Table 3.1-2 calculate the positive and negative threshold points if the device lengths are all $1 \mu\text{m}$ and the widths are given as: $W_1 = W_2 = W_{10} = W_{11} = 10 \mu\text{m}$ and $W_3 = W_4 = 2 \mu\text{m}$.

The gate of M1 is tied to ground and the input is applied to the gate of M2. The current $i_3 = 20 \mu\text{A}$. Simulate the results using simulation.

Solution

To calculate the positive trip point, assume that the input has been negative and is heading positive.

$$i_6 = \frac{(W/L)_6}{(W/L)_3} i_3 = (5/1)(i_3)$$

$$i_3 = \frac{i_3}{1 + [(W/L)_6/(W/L)_3]} = i_1 = \frac{20 \mu\text{A}}{1 + 5} = 3.33 \mu\text{A}$$

$$i_2 = i_3 - i_1 = 20 - 3.33 = 16.67 \mu\text{A}$$

$$v_{GS1} = \left(\frac{2i_1}{\beta_1} \right)^{1/2} + V_{T1} = \left(\frac{2 \cdot 3.33}{(5) 110} \right)^{1/2} + 0.7 = 0.81 \text{ V}$$

$$v_{GS2} = \left(\frac{2i_2}{\beta_2} \right)^{1/2} + V_{T2} = \left(\frac{2 \cdot 16.67}{(5) 110} \right)^{1/2} + 0.7 = 0.946 \text{ V}$$

$$V_{TRP}^+ \cong v_{GS2} - v_{GS1} = 0.946 - 0.810 = 0.136 \text{ V}$$

Determining the negative trip point, similar analysis yields

$$i_4 = 3.33 \mu\text{A}$$

$$i_1 = 16.67 \mu\text{A}$$

$$v_{GS2} = 0.81 \text{ V}$$

$$v_{GS1} = 0.946 \text{ V}$$

$$V_{TRP}^- \cong v_{GS2} - v_{GS1} = 0.81 - 0.946 = -0.136 \text{ V}$$

PSPICE simulation results of this circuit are shown in Fig. 8.4-13.

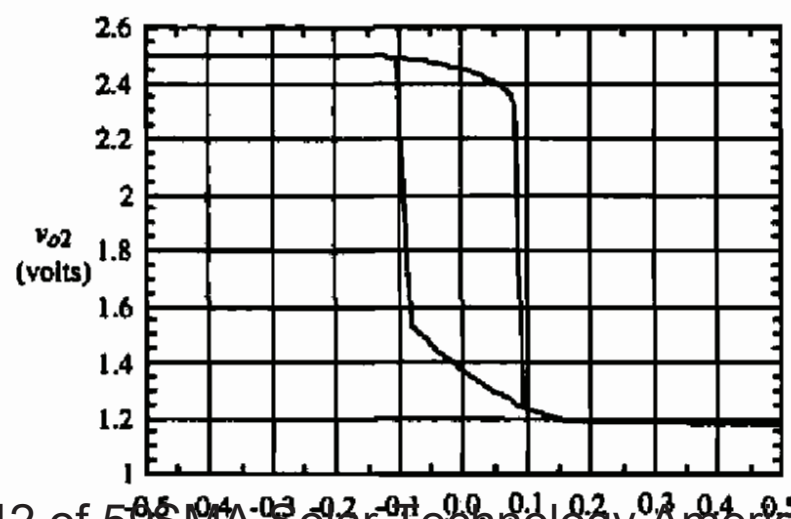


Figure 8.4-13 Simulation of the comparator of Example 8.4-2.

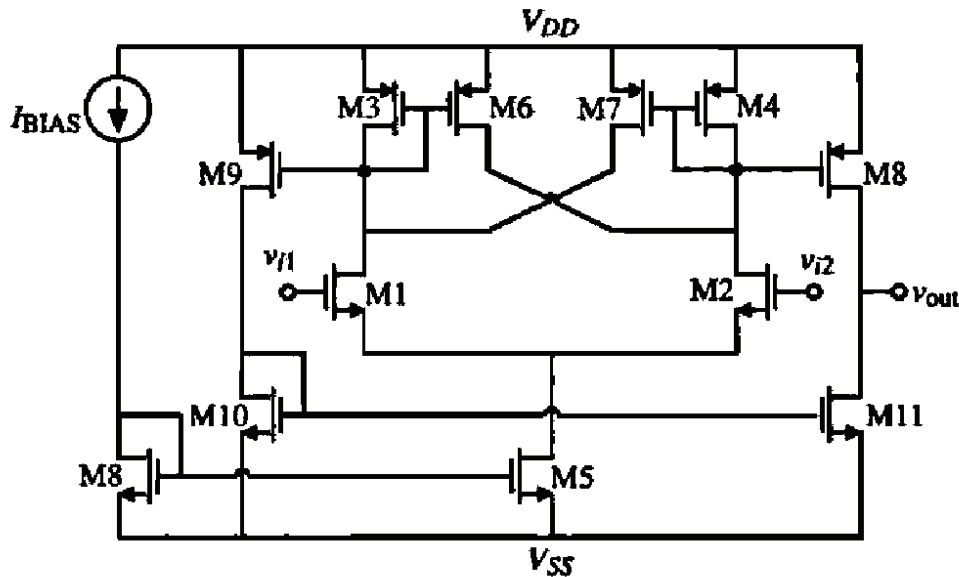


Figure 8.4-14 Complete comparator with internal hysteresis including an output stage.

The differential stage described thus far is generally not useful alone and thus requires an output stage to achieve reasonable voltage swings and output resistance. There are a number of ways to implement an output stage for this type of input stage. One of these is given in Fig. 8.4-14. Differential-to-single-ended conversion is accomplished at the output and thus provides a Class AB type of driving capability.

8.5 DISCRETE-TIME COMPARATORS

In many applications the comparator only functions over a portion of a time period. Such circuits are driven by a clock and will have a portion of time or phase when the comparator is functioning as a comparator and a phase when the comparator is not being used. In this circumstance, other forms of comparators can be used that are efficient and have a small propagation delay time. We will examine two such comparators in this section. They are the switched capacitor comparator and the regenerative comparator.

Switched Capacitor Comparators

The switched capacitor comparator uses a combination of switched capacitors and open-loop comparators. The advantages of the switched capacitor comparator are that differential signals can be compared using single-ended circuits and the switched capacitor comparator naturally lends itself to autozeroing the dc offset voltage of the open-loop comparator. Figure 8.5-1(a) shows a typical switched capacitor comparator. The voltages applied to the circuit are normally sampled and held so that capital variables are used.

When the ϕ_1 switches are closed in Fig. 8.5-1, the capacitor C autozeros the offset voltage of the comparator, V_{os} . The capacitor C_p represents the parasitic capacitance from the input of the comparator to ground. We recall that the comparator must be stable in unity-gain

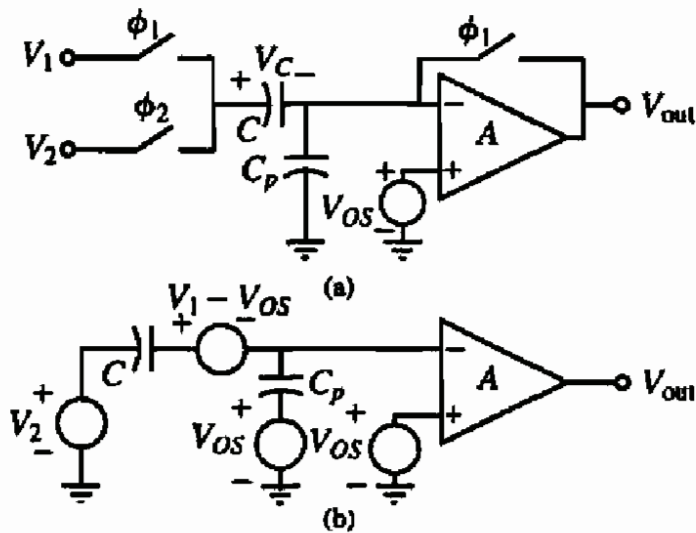


Figure 8.5-1 (a) A switched capacitor comparator. (b) Equivalent circuit of (a) when the ϕ_2 switches are closed.

operation for this circuit to work properly. It can be shown that the voltage across C_1 and C_p at the end of the ϕ_1 phase period is

$$V_C(\phi_1) = V_1 - V_{os} \quad (8.5-1)$$

and

$$V_{C_p}(\phi_1) = V_{os} \quad (8.5-2)$$

Now when the ϕ_2 switch is closed, the equivalent circuit at the beginning of the ϕ_2 phase period is shown in Fig. 8.5-1(b). In this circuit, the voltage across each capacitor has been removed and represented by a step voltage source. This allows us to use the principle of superposition to easily solve for the output as illustrated below.

$$\begin{aligned} V_{out}(\phi_2) &= -A \left[\frac{V_2 C}{C + C_p} - \frac{(V_1 - V_{os})C}{C + C_p} + \frac{V_{os} C_p}{C + C_p} \right] + A V_{os} \\ &= -A \left[(V_2 - V_1) \frac{C}{C + C_p} - V_{os} \left(\frac{C}{C + C_p} + \frac{C_p}{C + C_p} \right) \right] + A V_{os} = -A(V_2 - V_1) \frac{C}{C + C_p} \end{aligned} \quad (8.5-3)$$

If C_p is smaller than C , then Eq. (8.5-3) can be simplified to

$$V_{out}(\phi_2) \approx A(V_1 - V_2) \quad (8.5-4)$$

Therefore, the difference between the voltages V_1 and V_2 is amplified by the gain of the comparator.

The gain of the comparator used for the switched capacitor comparator must be large enough to satisfy the resolution requirements. In many cases, the resolution is large (i.e., 100 mV), so that a very simple single-stage amplifier is sufficient for the comparator. The speed of the comparator depends on how long it takes the circuit to settle to its steady state after the switches have been closed for a given period. During the ϕ_1 phase, the response of the circuit in Fig. 8.5-1(a) is very fast. The time constants of the circuit are associated with the product of the switch-on resistances and the capacitor C and the dynamics of the comparator

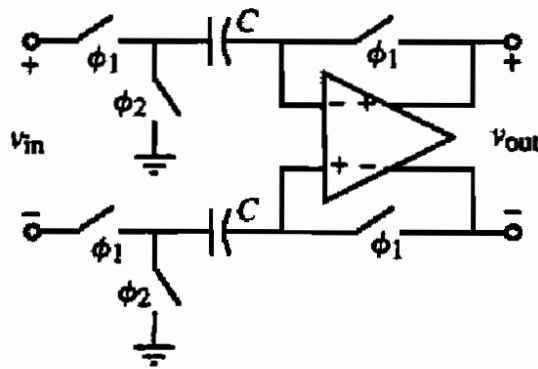


Figure 8.5-2 A differential-in, differential-out, switched capacitor comparator.

in unity-gain configuration. Both of these time constants can be small. During ϕ_2 , the open-loop response of the comparator will determine the speed. This subject has been covered in detail in Section 8.1 for a single-pole approximation and in Section 8.2 for a multiple-pole approximation of the comparator.

A differential switched capacitor comparator is shown in Fig. 8.5-2. The input is sampled on the two identical capacitors, C , during the ϕ_1 phase period. The dc offsets of the differential-in, differential-out comparator are also autozeroed during this period. During the ϕ_2 phase period, the voltages sampled across the capacitors are applied to the comparator input. As the ϕ_1 switches open at the end of the ϕ_1 phase period, the charge injection will be reduced because the signal is a differential voltage and the charge injection is a common-mode voltage.

Regenerative Comparators

Regenerative comparators use positive feedback to accomplish the comparison of two signals. The regenerative comparator is also called a *latch* or a *bistable* [5]. The simplest form of a latch is shown in Fig. 8.5-3 and consists of two cross-coupled MOSFETs. Figure 8.5-3(a) uses NMOS transistors while Fig. 8.5-3(b) is a PMOS latch. The current sources/sinks are used to identify the dc currents in the transistors. Normally, the latch has two modes of operation. The first mode disables the positive feedback and applies the input signal to the terminals designated as v_{o1} and v_{o2} . The initial voltages applied during this mode will be designated as v'_{o1} and v'_{o2} . The second mode enables the latch and depending on the relative values of v'_{o1} and v'_{o2} , one of the outputs will go high and the other will go low. A two-phase clock is used to determine the modes of operation.

It is important to characterize the time it takes for the latch to go from its initial state to the final state during the enabled mode of operation. Figure 8.5-4(a) is a redrawing of

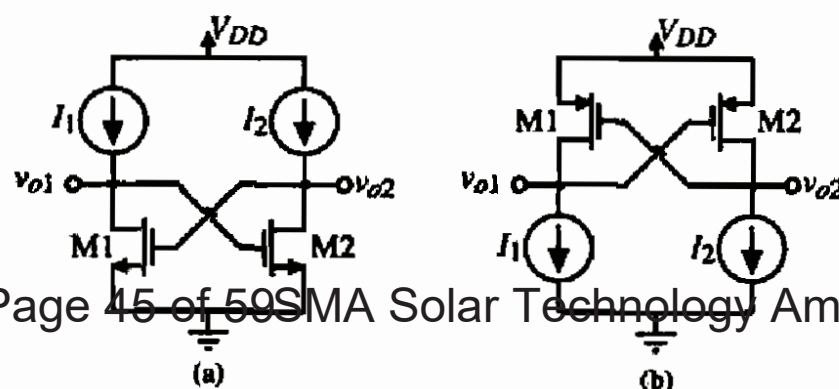


Figure 8.5-3 (a) NMOS latch.
(b) PMOS latch.

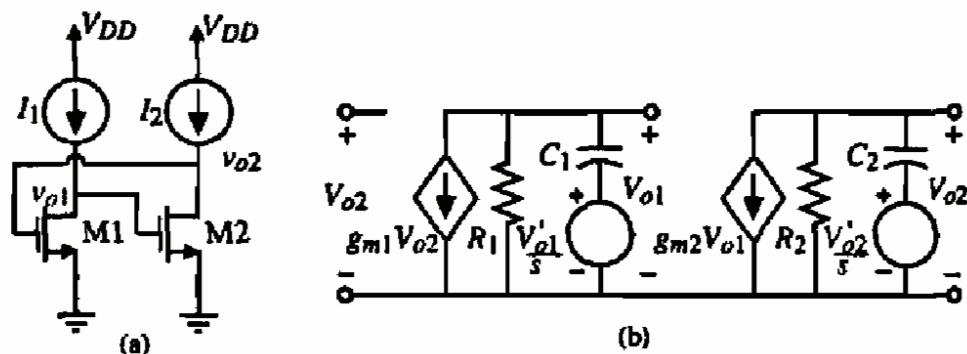


Figure 8.5-4 (a) Redrawing of Fig. 8.5-3(a). (b) Equivalent model of (a).

the latch in Fig. 8.5-3(a). Let us assume that the initial values of v_{o1} and v_{o2} have been established and find the time it takes for the latch to operate. We will use the model of Fig. 8.5-4(b) to analyze the latch of Fig. 8.5-4(a). The voltage sources in series with the capacitances represent the initial values of v_{o1} and v_{o2} and are step functions.

We may write the nodal equations of Fig. 8.5-4(b) as

$$g_{m1}V_{o2} + G_1V_{o1} + sC_1\left(V_{o1} - \frac{V'_{o1}}{s}\right) = g_{m1}V_{o2} + G_1V_{o1} + sC_1V_{o1} - C_1V'_{o1} = 0 \quad (8.5-5)$$

and

$$g_{m2}V_{o1} + G_2V_{o2} + sC_2\left(V_{o2} - \frac{V'_{o2}}{s}\right) = g_{m2}V_{o1} + G_2V_{o2} + sC_2V_{o2} - C_2V'_{o2} = 0 \quad (8.5-6)$$

where G_1 and G_2 are the conductances seen from the drains of M1 and M2 to ground and C_1 and C_2 are the capacitances seen from the drains of M1 and M2 to ground. Solving Eqs. (8.5-5) and (8.5-6) for V_{o1} and V_{o2} gives

$$V_{o1} = \frac{R_1C_1}{sR_1C_1 + 1}V'_{o1} - \frac{g_{m1}R_1}{sR_1C_1 + 1}V_{o2} = \frac{\tau_1}{s\tau_1 + 1}V'_{o1} - \frac{g_{m1}R_1}{s\tau_1 + 1}V_{o2} \quad (8.5-7)$$

and

$$V_{o2} = \frac{R_2C_2}{sR_2C_2 + 1}V'_{o2} - \frac{g_{m2}R_2}{sR_2C_2 + 1}V_{o1} = \frac{\tau_2}{s\tau_2 + 1}V'_{o2} - \frac{g_{m2}R_2}{s\tau_2 + 1}V_{o1} \quad (8.5-8)$$

where τ_i is the time constant R_iC_i . Assume that both transistors are identical so that $g_{m1} = g_{m2} = g_m$, $R_1 = R_2 = R$, and $C = C_1 = C_2$, which gives $\tau_1 = \tau_2 = \tau$. Let us define the difference between V_{o2} and V_{o1} as ΔV_o and the difference between V'_{o2} and V'_{o1} as ΔV_i .

Therefore,

$$\Delta V_o = V_{o2} - V_{o1} = \frac{\tau}{s\tau + 1}\Delta V_i + \frac{g_m R}{s\tau + 1}\Delta V_o \quad (8.5-9)$$

Solving for ΔV_o gives

$$\Delta V_o = \frac{\tau \Delta V_i}{s\tau + (1 - g_m R)} = \frac{\frac{\tau \Delta V_i}{1 - g_m R}}{\frac{s\tau}{1 - g_m R} + 1} = \frac{\tau' \Delta V_i}{s\tau' + 1} \quad (8.5-10)$$

where

$$\tau' = \frac{\tau}{1 - g_m R} \quad (8.5-11)$$

Taking the inverse Laplace transform of Eq. (8.5-10) gives

$$\Delta V_o(t) = \Delta V_i' e^{-t/\tau'} = \Delta V_i e^{-t(1 - g_m R)/\tau} \approx e^{g_m R t/\tau} \Delta V_i \quad (8.5-12)$$

if $g_m R$ is greater than one. The time constant of the latch as expressed in Eq. (8.5-12) is given as

$$\tau_L \approx \frac{\tau}{g_m R} = \frac{C}{g_m} \quad (8.5-13)$$

If C is mostly the gate-source capacitance, then the latch time constant can be expressed as

$$\tau_L = \frac{0.67 W L C_{ox}}{\sqrt{2K'(W/L)I}} = 0.67 C_{ox} \sqrt{\frac{W L^3}{2K'I}} \quad (8.5-14)$$

Equation (8.5-14) shows the strong dependence of the latch time constant on the channel length. Therefore, the latch time response can be expressed as

$$\Delta V_{out}(t) = e^{t/\tau_L} \Delta V_i \quad (8.5-15)$$

Equation (8.5-15) gives the difference between the latch output voltages, ΔV_{out} , at a time t after enabling the latch. The voltage ΔV_i is the difference between the latch output voltages, V_{o2} and V_{o1} , before the latch is enabled.

Fig. 8.5-5 shows the time-domain response of the latch for various values of ΔV_i . This figure has been normalized by dividing Eq. (8.5-15) by $V_{OH} - V_{OL}$ to get

$$\frac{\Delta V_{out}(t)}{V_{OH} - V_{OL}} = e^{t/\tau_L} \frac{\Delta V_i}{V_{OH} - V_{OL}} \quad (8.5-16)$$

It is important to remember that ΔV_i will always be less than $V_{OH} - V_{OL}$. The propagation time delay of a latch can be found by setting Eq. (8.5-16) equal to 0.5. The result is

$$t_p = \tau_L \ln \left(\frac{V_{OH} - V_{OL}}{2 \Delta V_i} \right) \quad (8.5-17)$$

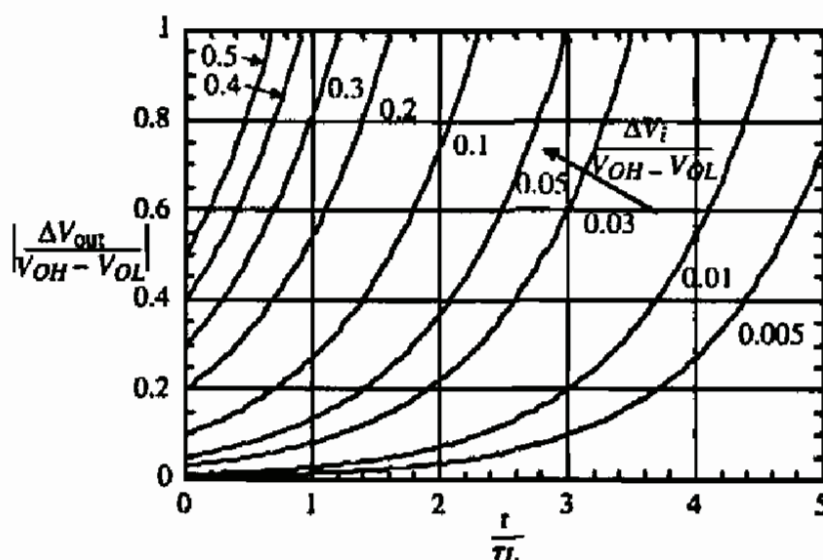


Figure 8.5-5 Normalized time-domain response of a latch.

Since ΔV_i is always less than $0.5 (V_{OH} - V_{OL})$, the argument of the logarithm is always greater than unity.

Figure 8.5-5 illustrates the time-domain response characteristics of a latch. There are several important observations to be made. The first is that the time required for ΔV_{out} to reach $V_{OH} - V_{OL}$ is decreased by applying a larger input to the latch, ΔV_i , before enabling the latch. The second and more obvious is that the smaller the latch time constant, the faster the response. If the input to the latch before enabling the latch, ΔV_i , is small, the latch takes a long time for the output voltage, ΔV_{out} , to reach $V_{OH} - V_{OL}$. Therefore, it is desirable to apply a reasonably large value of ΔV_i in order to take advantage of the rapidly increasing slope of the positive exponential characteristics of the latch.

TIME-DOMAIN CHARACTERISTICS OF A LATCH

Find the time it takes from the time the latch is enabled until the output voltage, ΔV_{out} , equals $V_{OH} - V_{OL}$ if the W/L of the latch NMOS transistors is $10 \mu\text{m}/1 \mu\text{m}$ and the latch dc current is $10 \mu\text{A}$ when $\Delta V_i = 0.01 V_{in}(\text{min})$ and $\Delta V_i = 0.1 V_{in}(\text{min})$. Find the propagation time delay for the latch for each of these conditions.

Solution

The transconductance of the latch transistors is

$$g_m = \sqrt{2 \cdot 110 \cdot 10 \cdot 10} = 148 \mu\text{S}$$

The output conductance is $0.4 \mu\text{S}$ given a latch gain of 59.2 V/V . Since $g_m R$ is greater than one, we can use Eq. (8.5-14). Therefore, the latch time constant is found as

$$\tau_L = \frac{1}{g_m R} = \frac{1}{148 \times 10^{-6} \times 10^{-6}} = 6.76 \times 10^{-4} \text{ s} = 676 \text{ ns}$$

Using Eq. (8.5-17) or Fig. 8.5-5 we find for $\Delta V_i = 0.01(V_{OH} - V_{OL})$ that $t = 4.6\tau_L = 496$ ns and for $\Delta V_i = 0.1(V_{OH} - V_{OL})$ that $t = 2.3\tau_L = 248$ ns.

The propagation time delay can be found using Eq. (8.5-17) and is 174 ns and 422 ns for $\Delta V_i = 0.01(V_{OH} - V_{OL})$ and $\Delta V_i = 0.1(V_{OH} - V_{OL})$, respectively.

A practical latch comparator is shown in Fig. 8.5-6 [6]. M7 and M8 are the latch transistors and are PMOS in this case. M9 and M10 are used to reset the latch by setting the source-drain voltages of M7 and M8 to zero. The input to the latch is applied to the gates of M1A and M1B. The transistors M1A, M1B, M2A, and M2B are operating in the triode region. The values of the inputs will cause the resistance seen by the sources of M3 and M4 to ground to vary. When the latch is enabled the drains of M3 and M4 are connected to the latch outputs. M3 and M4 form a parallel positive-feedback path for the latch. For example, the signal at the gate of M7 can go through M7 or can go through M3 (M5 is a closed switch). The gain of the M3 and M4 feedback paths depends on the value of the resistor, R_1 or R_2 , respectively. If the resistor is small the gain is large and that side of the latch will go high.

When the latch/reset goes high, the latch goes into its regenerative mode. The drain currents of M5 and M6 are steered to obtain a final state determined by the mismatch between the R_1 and R_2 resistances. These resistances are given as

$$\frac{1}{R_1} = K'_N \left[\frac{W_{1A}}{L} (v_{in}^+ - V_T) + \frac{W_{2A}}{L} (V_{REF}^- - V_T) \right] \quad (8.5-18)$$

and

$$\frac{1}{R_2} = K'_N \left[\frac{W_{1B}}{L} (v_{in}^- - V_T) + \frac{W_{2B}}{L} (V_{REF}^+ - V_T) \right] \quad (8.5-19)$$

The value of the input voltage that causes R_1 and R_2 to be equal is given as

$$v_{in}(\text{threshold}) = \left(\frac{W_2}{W_1} \right) V_{REF} \quad (8.5-20)$$

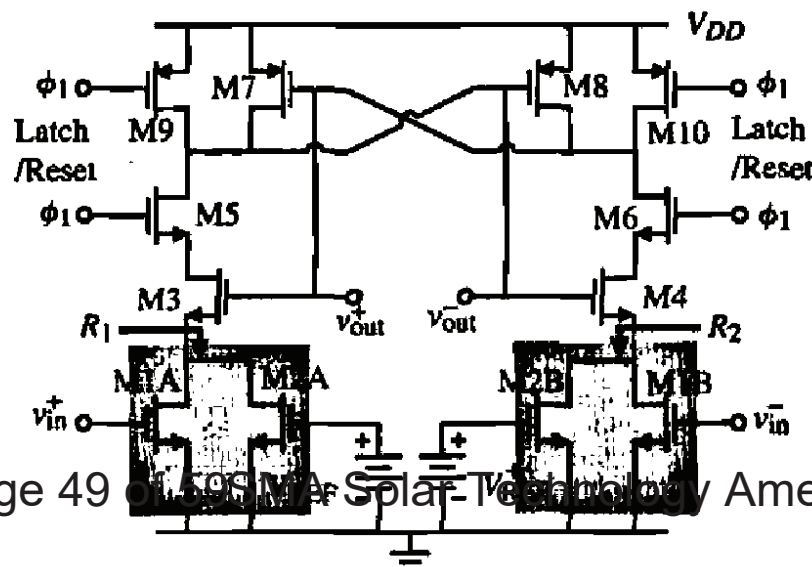


Figure 8.5-6 Comparator using a latch with a built-in threshold.

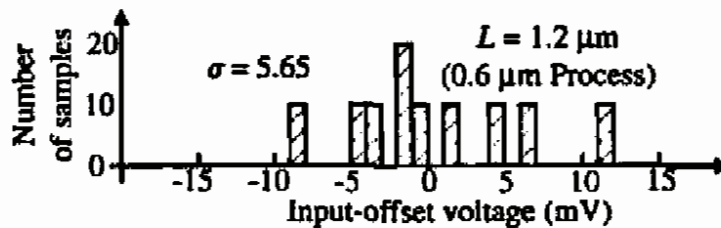


Figure 8.5-9 Input-offset voltage distribution histogram of the dynamic latch of Fig. 8.5-8.

input-offset voltage is distributed over a range of ± 10 mV. This comparator can only discriminate the difference between two signals to a 5 bit accuracy if the reference voltage was 1 V. This range can be reduced by preceding the latch by a preamplifier, which will be discussed in the next section.

8.6 HIGH-SPEED COMPARATORS

A high-speed comparator should have a propagation delay time as small as possible. In order to achieve this goal, one must understand the requirements for a fast comparator. This is best understood by separating the comparator into a number of cascaded stages. Figure 8.6-1 illustrates how this can be accomplished. A number of stages with a gain of A_0 and a single pole at $1/\tau$ are shown. If the input change is slightly larger than $V_{in(min)}$, then the function of the stages is to amplify the input with as little delay per stage as possible. We note that the signal swings in the initial stages will be small. As the signal swing begins to approach the desired range, the amplifiers will be limited by their slew rate. Thus, for initial stages, the important parameter is to have a high bandwidth so that there is little delay in amplifying the signal and passing it on to the next stage. However, at the end of the cascade of amplifiers, it is more important to have a high slew rate capability so that the voltage across the interstage capacitors and the load capacitor rises or falls quick enough. Therefore, the stages at the beginning should be designed differently than the stages at the end of the amplifier chain.

The basic principle behind the high-speed comparator is to use a preamplifier to build up the input change to a sufficiently large value and then apply it to the latch. This combines the best aspects of circuits with a negative exponential response (the preamplifier) with circuits with a positive exponential response (the latch). This is illustrated in Fig. 8.6-2 where the time-domain response for a preamplifier and a latch are illustrated. In this figure, the gain of the preamplifier times the input voltage is not sufficient to reach the desired output level. Rather, during time t_1 the preamplifier amplifies the input voltage to a value of V_x . The voltage V_x is applied to the latch input, which then goes to the desired output voltage in time t_2 . Thus, the total response time is $t_1 + t_2$. If the comparator consisted only of the preamplifier,

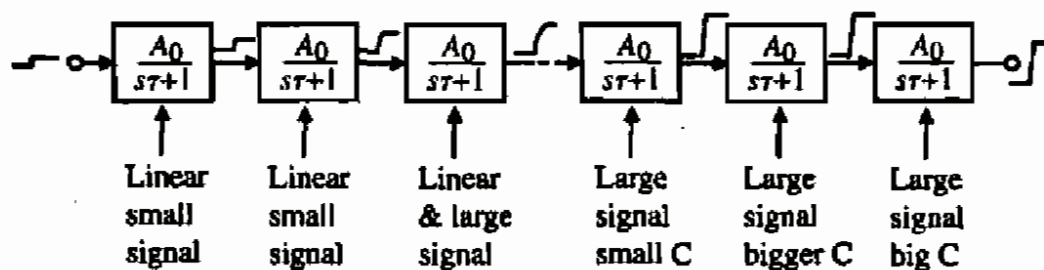


Figure 8.6-1 Conceptual illustration of a cascaded comparator.

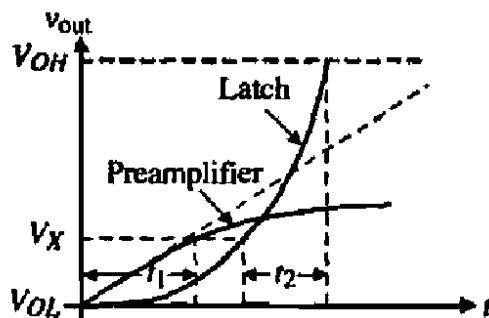


Figure 8.6-2 Preamplifier and latch step response.

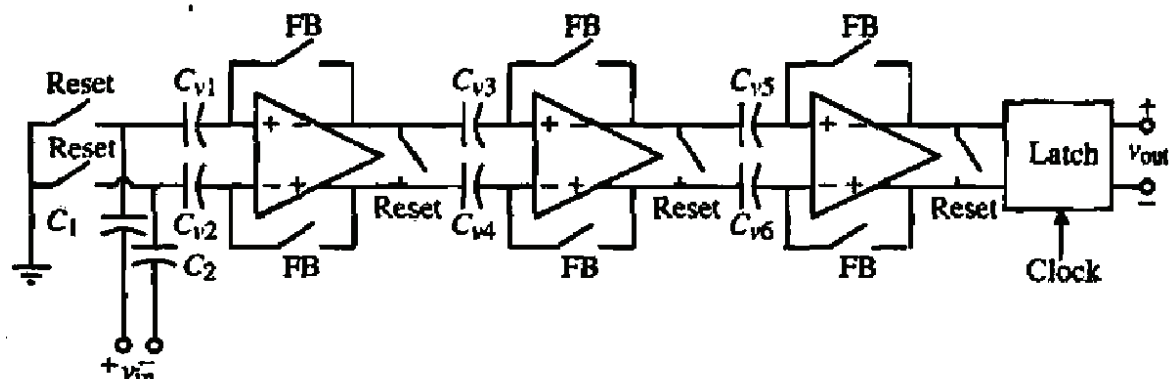
the gain would have to be larger and the delay to make the transition from V_{OL} to V_{OH} would be longer than $t_1 + t_2$. On the other hand, the latch would require more time than $t_1 + t_2$ if the input was small. We saw from Fig. 8.5-5 that the larger the input to the latch the shorter the time for the output to reach its maximum value.

The design of the preamplifier must be done in such a manner that the desired latch input voltage, V_X , is achieved in minimum time. Since the preamplifier is working in the linear region, this means that the bandwidth must be as large as possible. We know that the gain bandwidth of an amplifier is normally constant. Therefore, a single amplifier has a limited capability. If a number of low-gain, wide-bandwidth amplifiers are cascaded, the delay time, t_1 , can be minimized. In fact, it has been shown that the optimum number of identical low-gain amplifiers is six each with a gain of 2.72. However, this optimum is very broad and three amplifiers each with a gain of 6 gives equally good results with less area [9].

A high-speed comparator using three cascaded low-gain amplifiers as the preamplifier and a latch at the output is shown in Fig. 8.6-3. When the FB and Reset switches are closed, the capacitors designated as C_i are autozeroed for each amplifier. Unfortunately, each amplifier must be autozeroed by itself. More switches would be required to autozero all three amplifiers at the same time. The input is applied through the capacitors C_1 and C_2 . For high-speed applications, the clocks to the comparator of Fig. 8.6-3 can be as high as 100 MHz, resulting in a comparator that can run at 100 Msp/s. As the sample time is increased, the power consumption of the comparator also increases.

The low-gain preamplifiers must compromise between a high bandwidth and sufficient gain. A simple preamplifier is shown in Fig. 8.6-4. The connection with the latch (for the last preamplifier) is shown. The gain of this preamplifier is

$$A_v = g_{m1}/g_{m3} \approx g_{m2}/g_{m4} \quad (8.6-1)$$



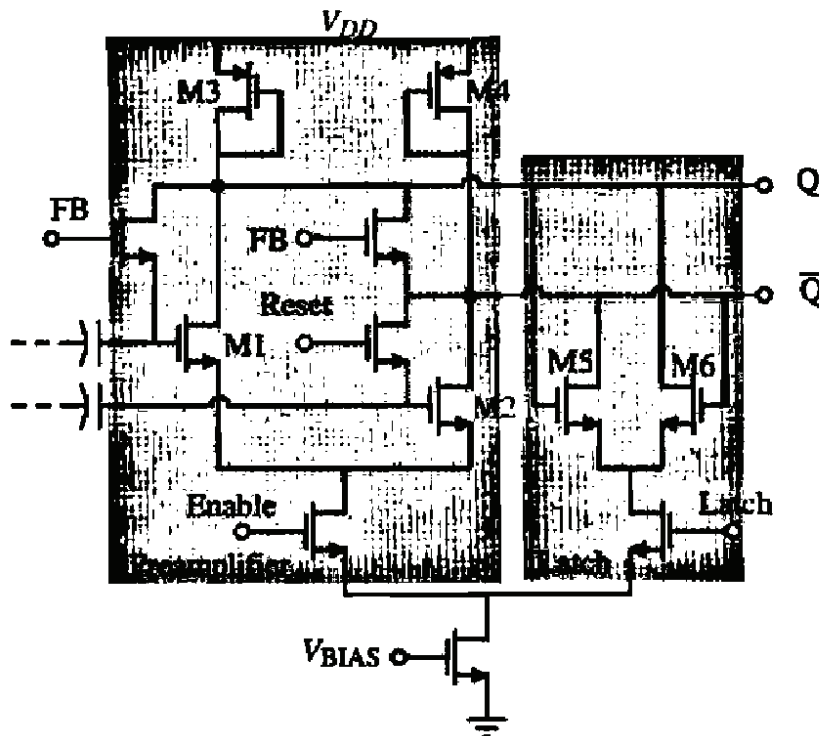


Figure 8.6-4 Example of a pre-amplifier and latch.

The dominant pole is given by

$$|p_{\text{dominant}}| = \frac{g_{m3}}{C} = \frac{g_{m4}}{C} \quad (8.6-2)$$

where C is the capacitance seen from the output nodes to ground. If the bias current in the transistors is $25 \mu\text{A}$, the W/L values of M1 and M2 are 100 and M3 and M4 are 1, then the gain is 3.85 V/V and if $C = 0.5 \text{ pF}$, the pole is 10^8 rad/s or 15.9 MHz . We see that it is important to keep the pole as large as possible. Sometimes it is necessary to buffer the output of the amplifier from the capacitive load of the next stage. Unfortunately, the buffer will have a gain loss 2–3 dB, which is undesirable.

There are several problems with the preamplifier of Fig. 8.6-4. One is that the gain is very small even for large differences of W/L values. Another is that there is no isolation between the latch outputs and the inputs to the preamplifier. Rapid changes in the output of the latch can propagate through the drain–gate capacitances of M1 and M2 and appear at the input of the latch. Figure 8.6-5 shows a preamplifier that solves these two problems. Transistors M5 and M6 are used to increase the current in M1 and M2 so that the gain is enhanced by the square root of the difference of currents in M1 and M2 to the currents in M3 and M4. This can be illustrated as follows. The gain of the preamplifier was given in Eq. (8.6-1) and can be expressed further as

$$A_v = -\frac{g_{m1}}{g_{m3}} = -\sqrt{\frac{K'_N(W_1/L_1)I_1}{K'_P(W_3/L_3)I_3}} = -\sqrt{\frac{K'_N(W_1/L_1)}{K'_P(W_3/L_3)}} \sqrt{1 + \frac{I_5}{I_3}} \quad (8.6-3)$$

If I_5 is greater than I_1 , the gain can be enhanced by the square root of 1 plus the ratio of I_5 to I_3 . If $I_5 = 24I_3$, the gain is boosted by a factor of 5. Transistors M7 and M8 isolate the input from rapid changes in the latch output.

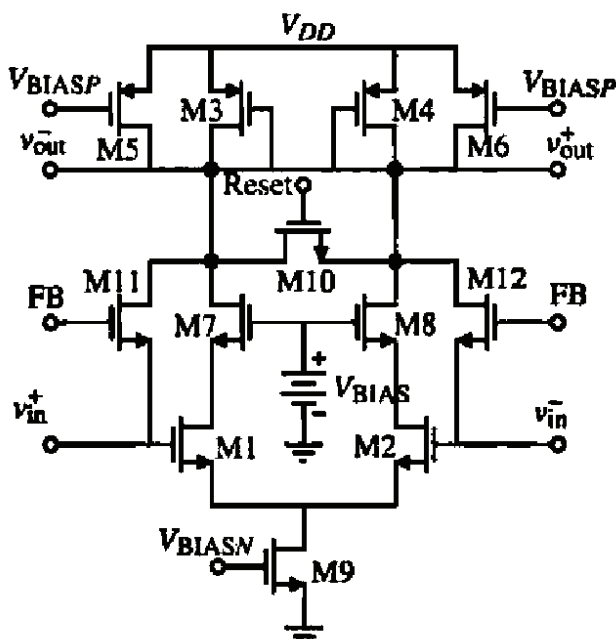


Figure 8.6-5 An improved preamplifier.

The use of a preamplifier before the latch also has the advantage of reducing the input-offset voltage of the latch by the gain of the preamplifier. The input-offset voltage of the comparator will now become that of the preamplifier, which can be autozeroed, resulting in small values of input-offset voltage.

The preamplifier can be replaced by a charge-transfer circuit resulting in simplification of the preamplifier [8]. A simple charge-transfer circuit is shown in Fig. 8.6-6(a), where the capacitor C_T is larger than C_O . This charge-transfer amplifier has three phases of operation. The first phase of operation is a reset phase, where switch S1 is closed discharging C_T . The second phase is the precharge phase shown in Fig. 8.6-6(b), where switch S2 is closed. In this phase, the capacitor C_T is charged to $v_{in} - V_T$ and the output capacitor, C_O , is charged to the preset voltage, V_{PR} . The third phase is the amplification phase and is shown in Fig. 8.6-6(c), where both switches are open. In this phase, the input has been assumed to change by an amount ΔV . This causes a current to flow in C_T which also flows in C_O . Since the charge change must be equal for both C_T and C_O , the change across C_O is $-(C_T/C_O)\Delta V$. If C_T is greater than C_O , the input change, ΔV , is amplified at the output by the factor of C_T/C_O .

The charge-transfer amplifier has several problems that must be solved. The first is that only positive values of voltage will be amplified and the second is that large offset voltages result as a function of the subthreshold current. A circuit that solves these problems is shown in Fig. 8.6-7 and uses both NMOS and PMOS transistors. Switches S3 are used to prevent a

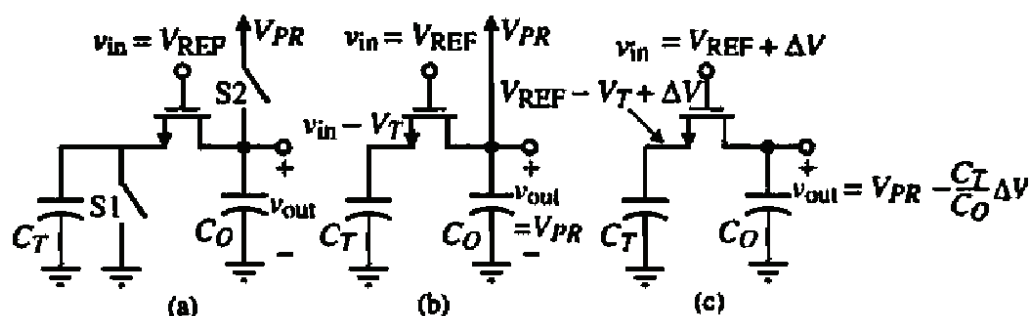


Figure 8.6-6 (a) Charge-transfer amplifier. (b) Precharge phase. (c) Amplification phase.

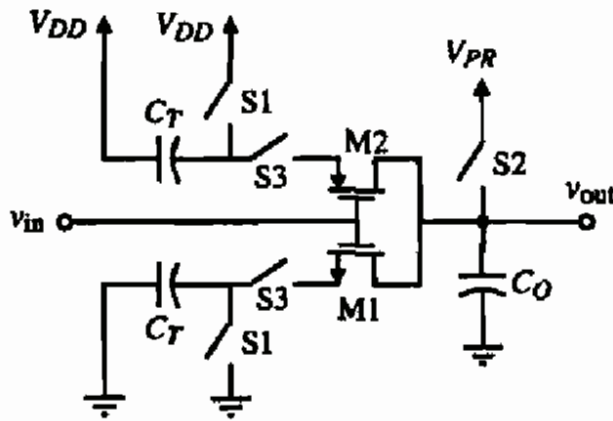
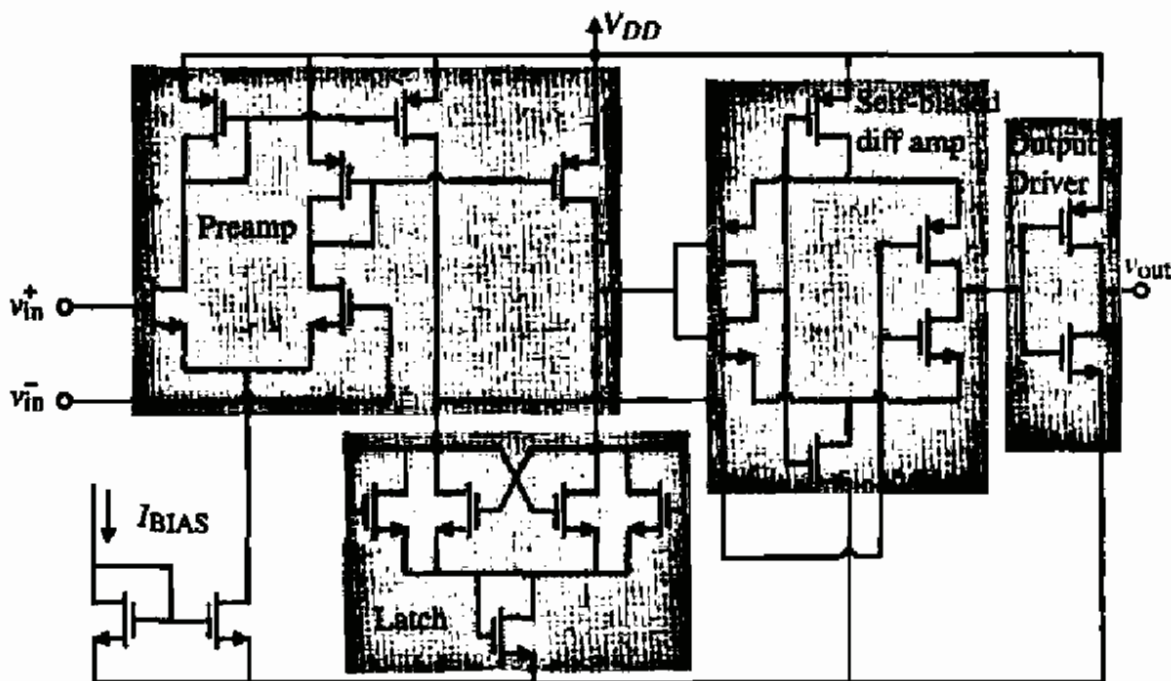


Figure 8.6-7 A CMOS charge-transfer preamplifier.

current path during the reset phase. This circuit was used in cascade with a dynamic latch to function as a comparator up to 20 Ms/s with 8 bit linearity and a power dissipation of less than 5 μ W. One of the limitations of the charge-transfer comparator is charge feedthrough. Dummy switches have been used to cancel some of the effects of charge feedthrough that occurs when the various switches are opened.

When a comparator must drive a significant amount of output capacitance in very short times, the latch is generally not sufficient. In this case it is advisable to follow the latch by circuits that can quickly generate large amounts of current. A high-speed comparator following these principles is shown in Fig. 8.6-8 [10]. The first stage is a low-gain, high-bandwidth preamplifier that drives a latch. The latch outputs are used to drive a self-biased differential amplifier. The output of the self-biased differential amplifier drives a push-pull output driver.

The comparator of Fig. 8.6-8 was designed to have a propagation time delay of 10 ns with a 5 pF load capacitor and a 10 mV overdrive. It is interesting to note that the comparator is synchronous (clocks are not used). The gain of the comparator in midswing is greater than 2000 V/V and the quiescent current is 100 μ A. More design details can be found in Baker et al. [10.]



8.7 SUMMARY

This chapter has introduced the comparator function along with the CMOS implementation of that function. The development of the CMOS comparator relied on previous work covering basic CMOS circuits in Chapters 4 and 5. The op amp of Chapter 6 makes an excellent open-loop, high gain comparator realization. The characterization of the two-stage, open-loop comparator illustrated the performance capabilities. It was seen that two modes of response can exist in a linear comparator. One is small signal and the other is large signal. The difference is whether or not slewing occurs. When a comparator does not slew (small signal) the bandwidth is key to reducing the propagation delay time. However, when the comparator slews, then current sinking and sourcing capability is crucial to fast operation.

The performance of the open-loop comparator can be improved by the use of hysteresis to remove the influence of a noisy input signal. Autozeroing can be used in comparators to reduce the input-offset voltage. It is necessary that the comparator be stable in the unity-gain mode during autozeroing, which can be difficult to accomplish in some types of comparators. It was seen that self-biased comparators were always stable in the autozeroing operation. Although we did not examine the noise of the comparator, it would be analyzed in the same manner as was done for op amps. We assume that the noise which is a linear phenomenon is important during the switching of the comparator, which is in the linear region.

In many comparator applications, the signal is discrete time rather than continuous. In this case it is possible to use regenerative circuits as comparators. Unfortunately, the transient response of regenerative circuits is characterized by a positive exponential argument. This means that if the input signal is small a long time will be required for the signal to reach the region of the exponential response where the slope is steep. A solution for this problem is to cascade the latch with a preamplifier. The function of the preamplifier is to quickly build up the input to the latch so that the slow rate of rise of the exponential response can be avoided. This has resulted in a comparator capable of operating up to 20 Ms/s and greater.

The comparator will play an important role in the remainder of the text, particularly in the area of analog-digital converters. It will be one of the major factors determining how accurately and how quickly analog signal processing can be accomplished.

PROBLEMS

8.1-1. Give the equivalent figures for Figs. 8.1-2, 8.1-4, 8.1-6, and 8.1-9 for an inverting comparator.

8.1-2. Use the macromodel techniques of Section 6.6 to model a comparator having a dc gain of 10,000 V/V, an offset voltage of 10 mV, $V_{OH} = 1$ V, $V_{OL} = 0$ V, a dominant pole at -1000 rad/s, and a slew rate of 1 V/ μ s. Verify your macromodel by using it to simulate Example 8.1-1.

8.1-3. Draw the first-order time response of an inverting comparator with a 20 μ s propagation delay time. The input is described by the following equations:

$$v_{in} = 0 \quad \text{for } t < 5 \mu\text{s}$$

$$v_{in} = 5(t - 5 \mu\text{s}) \quad \text{for } 5 \mu\text{s} < t < 7 \mu\text{s}$$

$$v_{in} = 10 \quad \text{for } t > 7 \mu\text{s}$$

8.1-4. Repeat Example 8.1-1 if the pole of the comparator is -10^5 rad/s rather than -10^3 rad/s.

8.1-5. What value of V_{in} in Example 8.1-1 will give a slewing response?

- 8.2.1. Repeat Example 8.2-1 for the two-stage comparator of Fig. 8.2-5.
- 8.2.2. If the poles of a two-stage comparator are both equal to -10^7 rad/s, find the maximum slope and the time it occurs if the magnitude of the input step is $10V_{in(min)}$. What must be the SR of this comparator to avoid slewing?
- 8.2.3. Repeat Example 8.2-3 if $p_1 = -5 \times 10^6$ rad/s and $p_2 = -10 \times 10^6$ rad/s.
- 8.2.4. For Fig. 8.2-5, find all of the possible initial states listed in Table 8.2-1 of the first-stage output voltage and the comparator output voltage.
- 8.2.5. Calculate the trip voltage for the comparator shown in Fig. 8.2-4. Use the parameters given in Table 3.1-2. Also, $(W/L)_2 = 100$ and $(W/L)_1 = 10$. $V_{BIAS} = 1$ V, $V_{SS} = 0$ V, and $V_{DD} = 4$ V.
- 8.2.6. Using Problem 8.2-5, compute the worst-case variations of the trip voltage assuming a $\pm 10\%$ variation on V_T , K' , V_{DD} , and V_{BIAS} .
- 8.2.7. Sketch the output response of the circuit in Problem 8.2-5, given a step input that goes from 4 to 1 V. Assume a 10 pF capacitive load. Also assume the input has been at 4 V for a very long time. What is the delay time from the step input to when the output changes logical (CMOS) states?
- 8.2.8. Repeat Example 8.2-5 with v_{G2} constant and the waveform of Fig. 8.2-6 applied to v_{G1} .
- 8.2.9. Repeat Example 8.2-5 using the two-stage op amp designed in Example 6.3-1 if the compensation capacitor is removed.
- 8.2.10. Repeat Example 8.2-6 if the propagation time is $t_p = 25$ ns.
- 8.2.11. Design a comparator given the following requirements: $P_{diss} < 2$ mW, $V_{DD} = 3$ V, $V_{SS} = 0$ V, $C_{load} = 3$ pF, $t_{prop} < 1$ μ s, $ICMR = 1.5$ – 2.5 V, $A_{vD} > 2200$, and output voltage swing within 1.5 V of either rail. Use Tables 3.1-2 and 3.3-1. Use 1 μ m channel lengths for all transistors.
- 8.3.1. Assume that the dc current in M5 of Fig. 8.3-1 is 100 μ A. If $W_6/L_6 = 5(W_4/L_4)$ and $W_8/L_8 = 5(W_3/L_3)$, what is the propagation delay time of this comparator if $C_L = 10$ pF and $V_{DD} = -V_{SS} = 2$ V?
- 8.3.2. If the folded-cascode op amp of Example 6.5-3 is used as a comparator, find the dominant pole if $C_L = 5$ pF. If the input step is 10 mV, determine whether the response is linear or slewing and find the propagation delay time.

- 8.3.3. Find the open-loop gain of Fig. 8.3-3 if the two-stage op amp is the same as Example 6.3-1 without the compensation and $W_{10}/L_{10} = 10(W_8/L_8) = 100(W_6/L_6)$, $W_9/L_9 = (K'_P/K'_N)(W_8/L_8)$, $W_{11}/L_{11} = (K'_P/K'_N)(W_{10}/L_{10})$ and the quiescent current in M8 and M9 is 100 μ A and in M10 and M11 is 500 μ A. What is the propagation time delay if $C_H = 100$ pF and the step input is large enough to cause slewing?
- 8.3.4. Figure P8.3-4 shows a circuit called a clamped comparator. Use the parameters of Table 3.1-2 and calculate the gain of this comparator. What is the positive and negative slew rate of this comparator if the load capacitance is 5 pF?

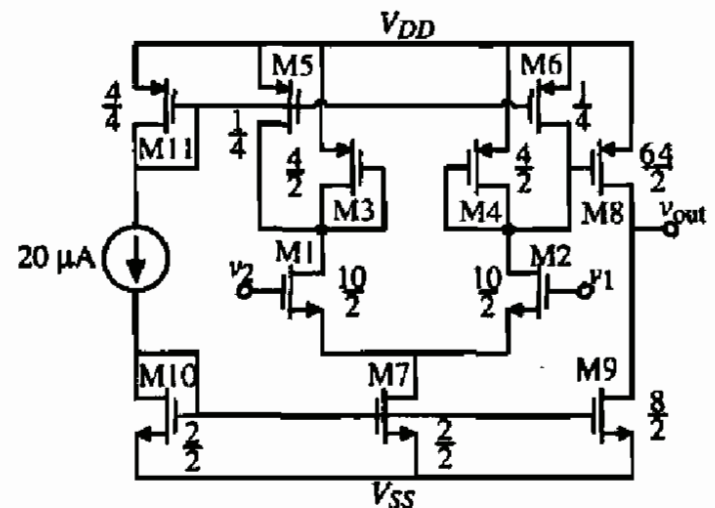


Figure P8.3-4

- 8.4.1. If the comparator used in Fig. 8.4-1 has a dominant pole at 10^4 rad/s and a gain of 10^3 , how long does it take C_{AZ} to charge to 99% of its final value, V_{OS} ? What is the final value that the capacitor, C_{AZ} , will charge to if left in the configuration of Fig. 8.4-1(b) for a long time?
- 8.4.2. Use the circuit of Fig. 8.4-9 and design a hysteresis characteristic that has $V_{TRP}^- = 0$ V and $V_{TRP}^+ = 1$ V if $V_{OH} = 2$ V and $V_{OL} = 0$ V. Let $R_1 = 100$ k Ω .
- 8.4.3. Repeat Problem 8.4-2 for Fig. 8.4-10.
- 8.4.4. Assume that all transistors in Fig. 8.4-11 are operating in the saturation mode. What is the gain of the positive-feedback loop, M6–M7, using the W/L values and currents of Example 8.4-2?
- 8.4.5. Repeat Example 8.4-1 to design $V_{TRP}^+ = -V_{TRP}^- = 0.5$ V.
- 8.4.6. Repeat Example 8.4-2 if $i_s = 50$ μ A. Confirm using a simulator.

- 8.5-1. List the advantages and disadvantages of the switched capacitor comparator of Fig. 8.5-1 over an open-loop comparator having the same gain and frequency response.
- 8.5-2. If the current and W/L values of the two latches in Fig. 8.5-3 are identical, which latch will be faster? Why?
- 8.5-3. Repeat Example 8.5-1 if $\Delta V_{out} = (0.5)(V_{OH} - V_{OL})$.
- 8.5-4. Repeat Example 8.5-1 if the dc latch current is $50 \mu\text{A}$.
- 8.5-5. Redevelop the expression for $\Delta V_{out}/\Delta V_i$ for the circuit of Fig. P8.5-5, where $\Delta v_{out} = v_{o2} - v_{o1}$ and $\Delta v_i = v_{i1} - v_{i2}$.

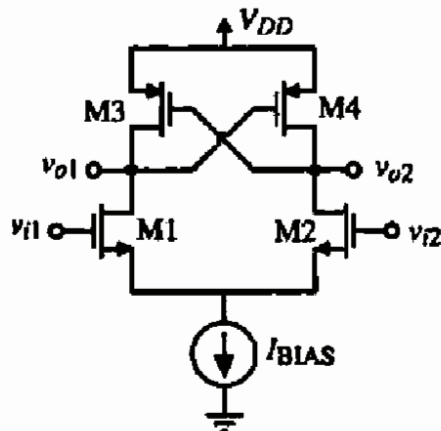


Figure P8.5-5

- 8.5-6. Compare the dynamic latch of Fig. 8.5-8 with the NMOS and PMOS latches of Fig. 8.5-3. What are the advantages and disadvantages of the two latches?
- 8.5-7. Use the worst-case values of the transistor parameters in Table 3.1-2 and calculate the worst-case voltage offset for the NMOS latch of Fig. 8.5-3(a).
- 8.6-1. Assume an op amp has a low-frequency gain of 1000 V/V and a dominant pole at -10^4 rad/s . Compare the -3 dB bandwidths of the configurations in Fig. P8.6-1 using this op amp.

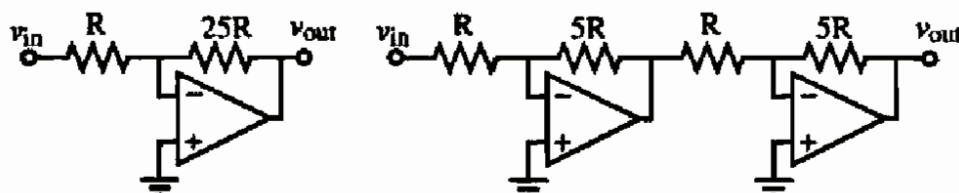


Figure P8.6-1

- 8.6-2. What is the gain and -3 dB bandwidth (in Hz) of Fig. P8.6-2 if $C_L = 1 \text{ pF}$? Ignore reverse-bias voltage effects on the pn junctions and assume the bulk-source and bulk-drain areas are given by $W \times 5 \mu\text{m}$.

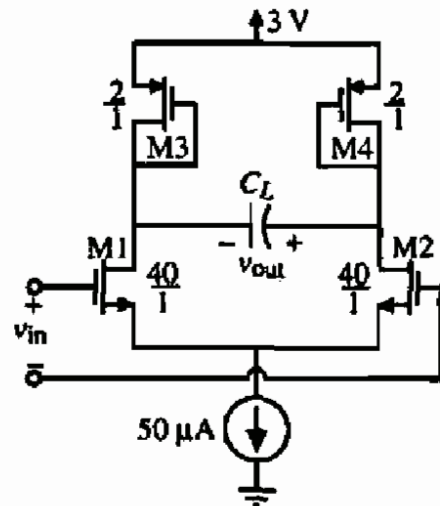


Figure P8.6-2

- 8.6-3. Repeat Problem 8.6-2 for Fig. P8.6-3. The W/L ratios for M1 and M2 are $10 \mu\text{m}/1 \mu\text{m}$ and for the remaining PMOS transistors the W/L ratios are all $2 \mu\text{m}/1 \mu\text{m}$.

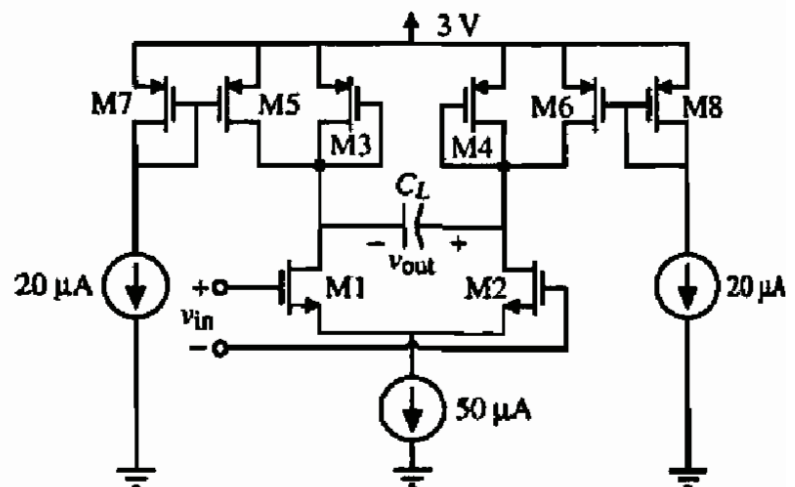


Figure P8.6-3

8.6-4. Assume that a comparator consists of an amplifier cascaded with a latch. Assume the amplifier has a gain of 5 V/V and a -3 dB bandwidth of $1/\tau_L$, where τ_L is the latch time constant. Find the normalized propagation delay time for the overall configuration if the applied input voltage is $0.05(V_{OH} - V_{OL})$ and the voltage applied to the latch is (a) $\Delta V_i = 0.05(V_{OH} - V_{OL})$, (b) $\Delta V_i = 0.1(V_{OH} - V_{OL})$, (c) $\Delta V_i = 0.15(V_{OH} - V_{OL})$, and (d) $\Delta V_i = 0.2(V_{OH} - V_{OL})$. From your results, what value of ΔV_i would give minimum propagation delay time?

8.6-5. Assume that a comparator consists of two identical amplifiers cascaded with a latch. Assume the amplifier has the characteristics given in Problem 8.6-4. What would be the normalized propagation delay time if the applied input voltage is $0.05(V_{OH} - V_{OL})$ and the voltage applied to the latch is $\Delta V_i = 0.1(V_{OH} - V_{OL})$?

8.6-6. Repeat Problem 8.6-5 if there are three identical amplifiers cascaded with a latch. What would be the normalized propagation delay time if the applied input voltage is $0.05(V_{OH} - V_{OL})$ and the voltage applied to the latch is $\Delta V_i = 0.2(V_{OH} - V_{OL})$?

8.6-7. A comparator consists of an amplifier cascaded with a latch as shown in Figure P8.6-7. The amplifier has voltage gain of 10 V/V and $f_{-3\text{dB}} = 100$ MHz and the latch has a time constant of 10 ns. The maximum and minimum voltage swings of the amplifier and latch are V_{OH} and V_{OL} . When should the latch be enabled after the application of a step input to the amplifier of $0.05(V_{OH} - V_{OL})$ to get minimum overall propagation time delay? What is the value of the minimum propagation time delay? It may be useful to recall that the propagating time delay of the latch is given as

$$t_p = \tau_L \ln \left(\frac{V_{OH} - V_{OL}}{2v_H} \right) \text{ where } v_H \text{ is the latch}$$

input (ΔV_i of the text).

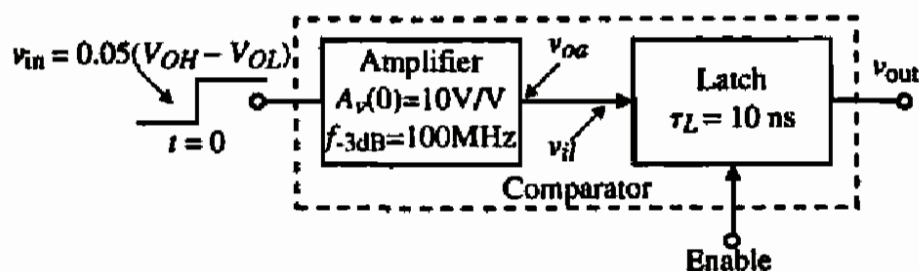


Figure P8.6-7

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