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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NETL.071PR
	Application Number	
Title of Invention	ARCHITECTURE FOR MEMORY MODULE WITH PACKAGES OF THREE-DIMENSIONAL STACKED (3DS) MEMORY CHIPS	

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Applicant 1

Applicant Authority ◉ Inventor ◯ Legal Representative under 35 U.S.C. 117 ◯ Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix

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Application Information:

Title of the Invention	ARCHITECTURE FOR MEMORY MODULE WITH PACKAGES OF THREE-DIMENSIONAL STACKED (3DS) MEMORY CHIPS		
Attorney Docket Number	NETL.071PR	**Small Entity Status Claimed**	☐
Application Type	Provisional		
Subject Matter	Utility		
Suggested Class (if any)		**Sub Class (if any)**	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)		**Suggested Figure for Publication (if any)**	

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Publication Information:

☐	Request Early Publication (Fee required at time of Request 37 CFR 1.219)
☐	**Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S. C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

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Prior Application Status			Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)

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			Remove
Application Number	Country[1]	Parent Filing Date (YYYY-MM-DD)	Priority Claimed
			○ Yes ○ No

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NETL.071PR
	Application Number	
Title of Invention	ARCHITECTURE FOR MEMORY MODULE WITH PACKAGES OF THREE-DIMENSIONAL STACKED (3DS) MEMORY CHIPS	

If the Assignee is an Organization check here. ☐				
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Signature				Date (YYYY-MM-DD)	2010-11-03
First Name	Bruce	Last Name	Itchkawitz	Registration Number	47677

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ARCHITECTURE FOR MEMORY MODULE WITH PACKAGES OF THREE-DIMENSIONAL STACKED (3DS) MEMORY CHIPS

BRIEF DESCRIPTION OF THE DRAWINGS

[0001] Figure 1 schematically illustrates the architecture of a load reduced DIMM (LRDIMM) and the distributed architecture of a HyperCloud DIMM (HCDIMM).

[0002] Figure 2 schematically illustrates the architecture of a 3DS-DIMM.

[0003] Figure 3 schematically illustrates a memory module architecture in accordance with certain embodiments described herein.

DETAILED DESCRIPTION

[0004] The proposed three-dimensional stacking (3DS) standard for dual in-line memory modules (DIMMs) being considered by the Joint Electron Devices Engineering Council (JEDEC) addresses the three major shortcomings in the current JEDEC registered DIMM (RDIMM) and JEDEC load reduced DIMM (LRDIMM) standards. These shortcomings are:

a) The DIMM density limitation due to the fixed number of chip-select signals received by the DIMM from the system memory controller.
b) The performance loss due to the increased load on the data bus as the DIMM density (e.g., the number of DRAM devices and number of ranks) increases.
c) The upper bound of the DIMM density due to the physical DIMM form factor.

[0005] The proposed 3DS-DIMM standard (see, e.g., Figure 2) includes two new components. One component of the 3DS-DIMM is a 3DS register (also known as an enhanced DDR3 register). This component contains a DDR3 JEDEC standard register with a "rank multiplication" circuit, which increases the number of the output chip-select signals by decoding the higher-order row or column address bits with the incoming chip-select signals from the system controller. The 3DS Register includes a command/address buffer, a register operational code buffer (RC word buffer), and rank multiplication logic (which supports rank multiplication of 1-to-2, 1-to-4, and/or 1-to-8). The 3DS register addresses shortcoming (a) of the JEDEC RDIMM and LRDIMM listed above.

[0006] Another component of the 3DS-DIMM is a 3DS dynamic random-access memory (DRAM) package. The 3DS DRAM package includes a plurality of stacked DDR

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DRAM chips or dies with a data I/O load that is equivalent to the data I/O load of a single-die DRAM package, regardless of the actual number of DRAM dies in the 3DS DRAM package. The 3DS DRAM package comprises 2, 4 or 8 DDR DRAM dies and a controller die. The controller die includes data buffers, a data path timing controller, a secondary command/address buffer, a programmable secondary 1-to-2 rank decoder, and a data path signal (e.g., ODT, ODT, RTT) controller. The 3DS DRAM package addresses the shortcomings (b) and (c) of the JEDEC RDIMM and LRDIMM listed above.

[0007] However, there are deficiencies in the proposed 3DS-DIMM standard. The JEDEC DDR3 RDIMM standard contains two major components: a DDR3 register and a plurality of DRAM packages each comprising one or more DRAM chips or dies. The DDR3 register serves as a command/address signal buffer and as a command/control decoder. This DDR3 register holds a set of register control (RC) words, which the computer system configures to ensure the proper operation of the RDIMM. The DDR3 register contains a phase-lock-loop (PLL), which functions as a clock synchronizer for each RDIMM. The DDR3 register outputs a set of buffered command/address signals to all the DRAM packages on the RDIMM, but the data signals are directly fed to the DRAM packages from the system memory controller.

[0008] In contrast to the JEDEC DDR3 RDIMM standard, the 3DS-DIMM proposal requires the DRAM package to contain a controller die that controls all data paths timing and operations (see, e.g., Figure 2). This arrangement of the DRAM package reduces the load on the data bus, however, it presents three significant shortcomings:

1) The command/address buffer in the 3DS DRAM package introduces clock cycle latency since it needs to provide clock synchronous operation to the DRAM dies in the package.
2) The data path control circuit (e.g., ODT, read/write data direction) in the control die becomes very complicated to support semi-synchronous (fly-by) data path control among all 3DS DRAM packages that are on a DIMM.
3) The variations in the DRAM die timing characteristics within each 3DS DRAM package would be likely to require resynchronization of the data signals during the read/write operations, which increases the read/write latency and the read-to-write and write-to-read turn around time.

[0009] The 3DS-DIMM proposal can also be compared to the HyperCloud (HC) DIMM architecture of Netlist, Inc. (see, e.g., Figure 1 and U.S. Pat. Nos. 7,289,386,

7,532,537, 7,619,912, and 7,636,274, each of which is incorporated in its entirety by reference herein). The 3DS-DIMM architecture is very similar with the HCDIMM architecture. The main topological difference is that while 3DS-DIMM architecture requires a control die to buffer the data signals and to provide interface with command/address signals from the 3DS register, the HCDIMM architecture includes a plurality of isolation devices (ID), each of which only contains data buffers. Unlike the HCDIMM architecture, since the command/address signal needs to pass through the control die in the 3DS DRAM package, the 3DS-DIMM proposal presents the same shortcoming (b) of the controller die described above. The data path control signals are generated by the register device (RD) in the HCDIMM architecture, while these data path control signals are generated by the control die in the 3DS DRAM. This creates unneeded timing critical control paths in 3DS-DIMM architecture.

[0010] In certain embodiments described herein, a memory module architecture is proposed that includes a set of device components that supports JEDEC 3DS operation with the benefit of RDIMM and HCDIMM (see, e.g., Figure 3). This set of device components comprises two components: a register device (RD) (e.g., the same RD component as in HCDIMM), and a DDR DRAM Stack Package (DDSP) that comprises a DRAM control die that serves as command/address buffers and a data path control circuit. Certain embodiments of the architecture described herein differs from the 3DS-DIMM architecture in that instead of the controller die of the 3DS-DIMM (which provides selective isolation, a secondary address buffer, and a second rank multiplication decoder), certain embodiments described herein use an "ID+" die that provides both selective isolation and address pass-through (e.g., compare Figures 2 and 3).

[0011] The data path control circuit of certain embodiments has two operational modes: mode-C (HCDIMM/RDIMM Compatible mode) and mode-3DS (3DS DIMM compatible mode). In mode-C, the DDR DRAM Stack Package (DDSP) receives all the data path control signals from the RD, and the RD manages the data path by controlling the command/address time slot and the data bus time slot. In mode-3DS, the "ID+" die in the DDSP internally generates the data path control signals to ensure the proper operation of the data path.

[0012] The DDSP of certain embodiments allows the DDSP-DIMM to work as either a 3DS-DIMM, a RDIMM, or a HCDIMM. However, in mode-C, the DDSP comprises a set of optional control input pins (in addition to the package pins that are included in 3DS-DRAM) to receive the data path control signals from the RD.

[0013] The following U.S. patents are incorporated in their entirety by reference herein: U.S. Pat. Nos. 7,289,386, 7,286,436, 7,442,050, 7,375,970, 7,254,036, 7,532,537, 7,636,274, 7,630,202, 7,619,893, 7,619,912, 7,811,097. The following U.S. patent applications are incorporated in their entirety by reference herein: U.S. Pat. Appl. Nos. 12/422,912, 12/422,853, 12/577,682, 12/629,827, 12/606,136, 12/874,900, 12/422,925, 12/504,131, 12/761,179, and 12/815,339.

[0014] Various embodiments have been described above. Although this invention has been described with reference to these specific embodiments, the descriptions are intended to be illustrative of the invention and are not intended to be limiting. Various modifications and applications may occur to those skilled in the art without departing from the true spirit and scope of the invention.

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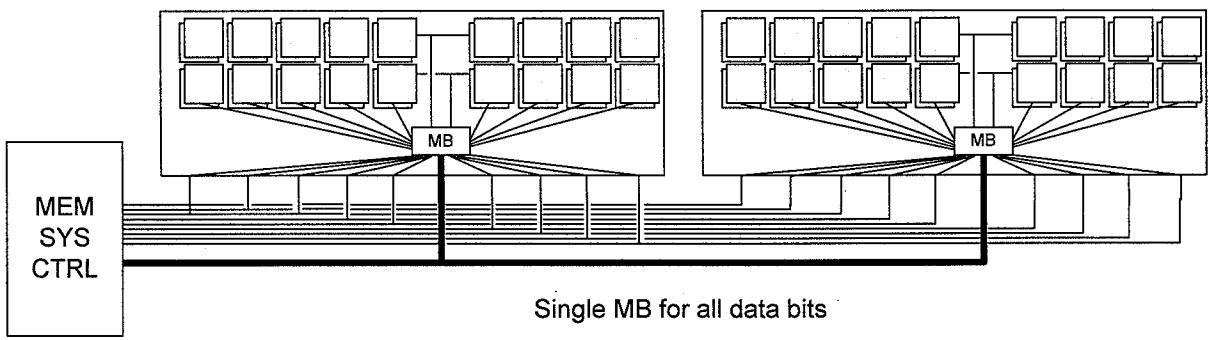
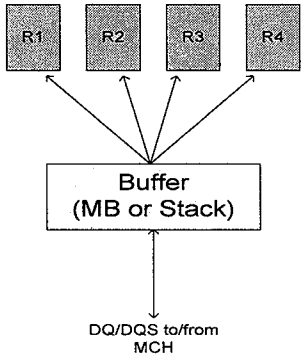
HCDIMM vs LRDIMM

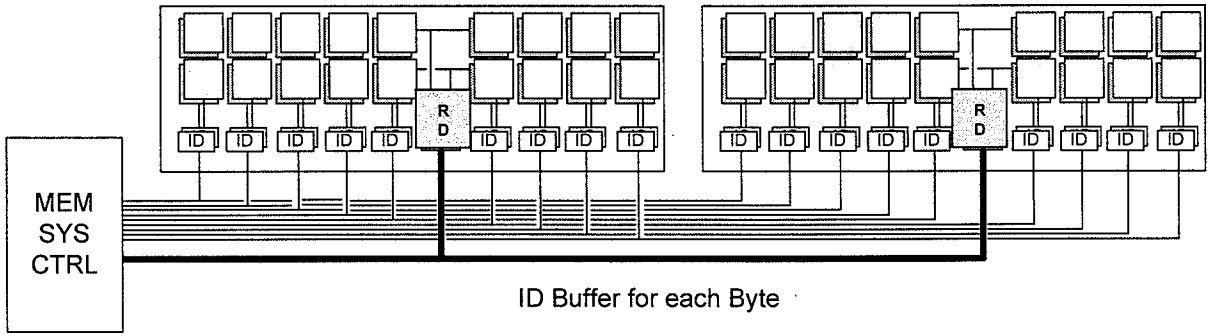
- All signals go through single memory buffer (MB) in LRDIMM (causes timing issues)
- LRDIMM has longer data path (more latency and SI issues)

LRDIMM





HCDIMM – Distributed Architecture



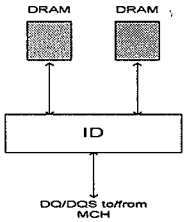
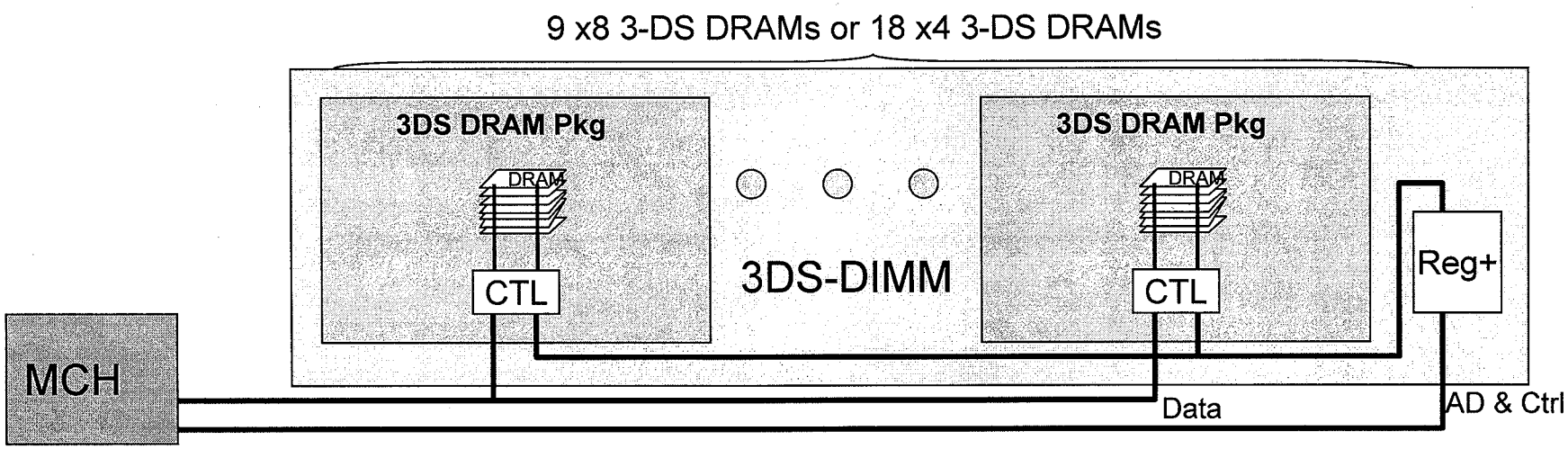


Figure 1

3DS-DIMM (Distributed Topology)

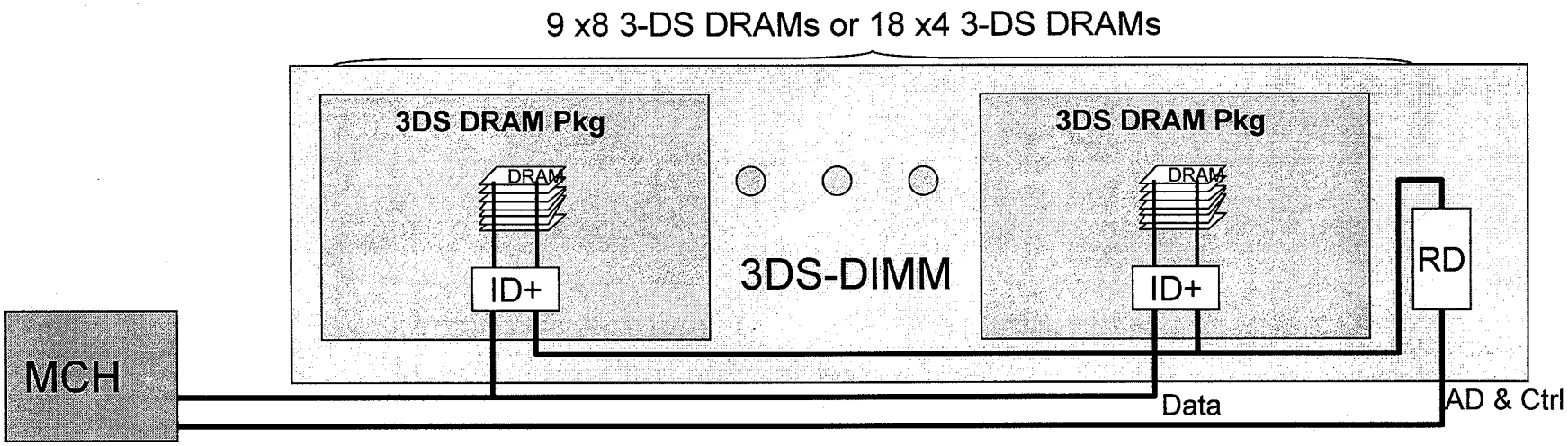


3DS-DIMM – Based on Distributed Architecture:
New Components
Reg+ = DDR3_Register + RM decoder
CTL = ID + Secondary address buffer + 2^{nd}_RM decoder

More Complexity in Design and Performance Degradation and Added Latency

Figure 2

3DS-DIMM+ (Distributed Topology based HCDIMM)



3DS-DIMM – Based on Distributed Architecture
ID+ = ID + Address Pass-through.

Simple Design without Performance Loss or Added Latency

Figure 3

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	ARCHITECTURE FOR MEMORY MODULE WITH PACKAGES OF THREE-DIMENSIONAL STACKED (3DS) MEMORY CHIPS
First Named Inventor/Applicant Name:	TBD TBD
Filer:	Bruce S. Itchkawitz/Jessica Noda
Attorney Docket Number:	NETL.071PR

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Application Number:	61409893
International Application Number:	
Confirmation Number:	4751
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First Named Inventor/Applicant Name:	TBD TBD
Customer Number:	20995
Filer:	Bruce S. Itchkawitz/Quyen Lieu
Filer Authorized By:	Bruce S. Itchkawitz
Attorney Docket Number:	NETL.071PR
Receipt Date:	03-NOV-2010
Filing Date:	
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Application Type:	Provisional

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