UTILITY PATENT APPLICATION TRANSMITTAL (Only for new nonprovisional applications under 37 CFR § 1.53(b))	Attorney Docket No.	129980-5070-US01
	First Inventor	Hyun Lee
	Title	MEMORY MODULE WITH BUFFERED MEMORY PACKAGES
	Electronically filed	May 14, 2019

APPLICATION ELEMENTS

See MPEP Chapter 600 concerning utility patent application contents.

Address to: **Commissioner for Patents**
P.O. Box 1450
Alexandria, VA 22313-1450

1. ☐ Fee Transmittal Form *(with duplicate for fee processing)*
2. ☐ Applicant claims Small Entity status, see 37 C.F.R. § 1.27
3. ☒ Specification [Total Pages 37]
4. ☒ Drawing(s) *(35 USC § 113)* [Total Sheets 8]
5. ☒ Oath or Declaration [Total Pages 1]
   a. ☐ Newly executed *(original or copy)*
   b. ☒ Copy from a prior application *(37 CFR § 1.63(d))*
6. ☒ Application Data Sheet, see 37 C.F.R. § 1.76
7. ☐ CD-ROM or CD-R in duplicate, large table or Computer Program *(Appendix)*
   ☐ Landscape Table on CD
8. ☐ Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. ☐ Computer Readable Form (CRF)
   b. ☐ Specification Sequence Listing on
      i. ☐ CD-ROM or CD-R (2 copies); or
      ii. ☐ Paper
   c. ☐ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

9. ☐ Assignment Papers *(cover sheet & document(s))*
   Name of Assignee:
10. ☒ 37 CFR § 3.73(c) Statement
    a. ☒ Power of Attorney
11. ☐ English Translation Document *(if applicable)*
12. ☐ Information Disclosure Statement and PTO-1449
    a. ☐ Copies of citations attached
13. ☐ Preliminary Amendment
14. ☐ Return Receipt Postcard *(MPEP 503)*
15. ☐ Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
16. ☐ Non-Publication Request under 35 U.S.C. § 122 (b)(2)(B)(i)
17. ☐ Other:

Note: (1) Benefit claims under 37 CFR 1.78 and foreign priority claims under 1.55 **MUST** be included in an Application Data Sheet (ADS).

(2) For applications filed under 35 U.S.C. 111, the application must contain an ADS specifying the applicant if the applicant is an assignee, person to whom the inventor is under an obligation to assign, or person who otherwise shows sufficient proprietary interest in the matter. See 37 CFR 1.46(b).

19. CORRESPONDENCE ADDRESS: Customer Number 79141

Signature	/Jamie J. Zheng/	Date	May 14, 2019
Name (Print/Type)	Jamie J. Zheng	Registration No. (Attorney/Agent)	51,167

GENERAL POWER OF ATTORNEY BY APPLICANT FOR UNITED STATES PATENT

I hereby revoke all previous powers of attorney given in the application referenced in the attached transmittal letter (form PTO/AIA/82A or equivalent).

I hereby appoint the practitioner associated with the following Customer Number :

79141

as my/our attorney or agent, and to transact all business in the United States Patent and Trademark Office in connection with the application referenced in the attached transmittal letter (form PTO/AIA/82A or equivalent).

Please recognize or change the **correspondence address** for the application referenced in the attached transmittal letter to the address associated with the above-mentioned **Customer Number**.

I am the Applicant:

- [ ] Inventor or Joint Inventor
- [ ] Legal Representative of a Deceased or Legally Incapacitated Inventor
- [x] Assignee or Person to Whom the Inventor is Under an Obligation to Assign
- [ ] Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is currently being filed in this document)

SIGNATURE of Applicant for Patent

Signature		Date: January 9, 2013
Name	Gail Sasaki	
Title	Vice President and Chief Financial Officer	
Company	Netlist, Inc.	

Note: Signature - this form must be signed by the Applicant or a person authorized to act on behalf of Applicant.

Submit multiple forms for more than one signature
Total of ___ forms are submitted.

Electronically filed May 14, 2019

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun Lee	Confirmation No.:	To be assigned
Serial No.:	To be assigned	Art Unit	To be assigned
Filed:	Filed herewith	Examiner:	To be assigned
For:	MEMORY MODULE WITH BUFFERED MEMORY PACKAGES	Attorney Docket No.:	129980-5070-US01

STATEMENT UNDER 37 C.F.R. § 3.73(c)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Netlist, Inc., a corporation, states that it is the assignee of the entire right, title and interest in the patent application/patent identified above by virtue of an assignment from the inventor(s) of the parent of the patent application/patent identified above.

The assignment was recorded in the United States Patent and Trademark Office on May 23, 2017 at Reel 042475, Frame 0107, or for which a copy thereof is attached.

The undersigned is authorized to act on behalf of the assignee.

Date: May 14, 2019

/Jamie J. Zheng/ 51167

Jamie J. Zheng (Reg. No.)
MORGAN, LEWIS & BOCKIUS LLP
1400 Page Mill Road
Palo Alto, CA 94304
(650) 843-4000

PTO/AIA/14 (11-15)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	129980-5070-US01
	Application Number	
Title of Invention	MEMORY MODULE WITH BUFFERED MEMORY PACKAGES	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Hyun		Lee	

Residence Information (Select One) ● US Residency Non US Residency Active US Military Service

City	Ladera Ranch	State/Province	CA	Country of Residence i	US

Mailing Address of Inventor:

Address 1	175 TECHNOLOGY		
Address 2	#150 IRVINE		
City	Irvine	State/Province	CA
Postal Code	92618	Country i	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	79141		
Email Address		Add Email	Remove Email

Application Information:

Title of the Invention	MEMORY MODULE WITH BUFFERED MEMORY PACKAGES		
Attorney Docket Number	129980-5070-US01	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	8	Suggested Figure for Publication (if any)	

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	129980-5070-US01
	Application Number	
Title of Invention	MEMORY MODULE WITH BUFFERED MEMORY PACKAGES	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	● Customer Number	US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	79141		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Continuation of	15/602099	2017-05-22

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	129980-5070-US01
	Application Number	
Title of Invention	MEMORY MODULE WITH BUFFERED MEMORY PACKAGES	

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15/602099	Continuation of	15/095288	2016-04-11	9659601	2017-05-23
Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15/095288	Continuation of	14/337168	2014-07-21	9318160	2016-04-19
Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14/337168	Continuation of	13/288850	2011-11-03	8787060	2014-07-22
Prior Application Status	Expired				Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
13/288850	Claims benefit of provisional	61/409893	2010-11-03		

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	129980-5070-US01
	Application Number	
Title of Invention	MEMORY MODULE WITH BUFFERED MEMORY PACKAGES	

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	129980-5070-US01
	Application Number	
Title of Invention	MEMORY MODULE WITH BUFFERED MEMORY PACKAGES	

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	129980-5070-US01
	Application Number	
Title of Invention	MEMORY MODULE WITH BUFFERED MEMORY PACKAGES	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1 Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section. Clear

● Assignee	Legal Representative under 35 U.S.C. 117	Joint Inventor
Person to whom the inventor is obligated to assign.	Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

Organization Name	NETLIST, INC.		
Mailing Address Information For Applicant:			
Address 1	175 TECHNOLOGY		
Address 2	#150		
City	Irvine	**State/Province**	CA
Country	US	Postal Code	92618
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	129980-5070-US01
	Application Number	
Title of Invention	MEMORY MODULE WITH BUFFERED MEMORY PACKAGES	

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

Remove

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button. Add

Signature:

Remove

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Jamie J. Zheng/			Date (YYYY-MM-DD)	2019-05-14
First Name	Jamie J.	Last Name	Zheng	Registration Number	51167

Additional Signature may be generated within this form by selecting the Add button. Add

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	129980-5070-US01
	Application Number	
Title of Invention	MEMORY MODULE WITH BUFFERED MEMORY PACKAGES	

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1 The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3 A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent CooperationTreaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

MEMORY MODULE WITH BUFFERED MEMORY PACKAGES

ABSTRACT OF THE DISCLOSURE

A memory module includes a plurality of DRAM packages mounted on a printed circuit board. Each DRAM package includes a control die, stacked array dies, and first and second die interconnects coupling the stacked array dies to the control die. The control die includes data signal conduits coupled to the first die interconnects and control signal conduits coupled to the second die interconnects. The control die is configured to receive control signals, and to control the data signal conduits in accordance with the control signals. Each of the DRAM packages is configurable to communicate a respective set of bits of a data signal between a selected die among the stacked array dies and the data conduits in response to the control signals.

WHAT IS CLAIMED IS:

1. A memory module operable in a computer system to communicate with a system memory controller via a command/address bus and a data bus, comprising:

a printed circuit board;

a register device mounted on the printed circuit board and configured to receive input command/address signals from the system memory controller via the command/address bus and to output control signals in response to the input command/address signals, the control signals including chip-select signals; and

a plurality of DRAM packages mounted on the printed circuit board, each respective DRAM package comprising:

control terminals coupled to the register device;

data terminals coupled to a respective section of the data bus;

stacked array dies;

a control die including data signal conduits coupled to the data terminals and control signal conduits coupled to the control terminals, the control signal conduits including chip-select conduits for receiving the chip select signals and providing respective ones of the chip select signals to respective ones of the stacked array dies; and

die interconnects including first die interconnects coupled to the data signal conduits and second die interconnects coupled to the control signal conduits, each of at least a subset of the first die interconnects is coupled to at least two of the stacked array dies; and

wherein the control die is configured to control the data signal conduits in accordance with the control signals to enable the each respective DRAM package to communicate a respective set of bits of one or more data signals between a selected die among the stacked dies and the data terminals, the selected die having received one of the chip select signals that is different from any of the other ones of the chip select signals.

MEMORY MODULE WITH BUFFERED MEMORY PACKAGES

RELATED APPLICATION

[0001] This application is a continuation application of U.S. Pat. App. No. 15/602,099, filed May 22, 2017, which is a continuation application of U.S. Pat. App. No. 15/095,288, filed April 11, 2016, now U.S. Pat. No. 9,659,601 on May 23, 2017, which is a continuation of U.S. Pat. App. No. 14/337,168, filed July 21, 2014, now U.S. Pat. No. 9,318,160, which is a continuation of U.S. Pat. App. No. 13/288,850, filed November 3, 2011, now U.S. Pat. No. 8,787,060, which claims the benefit of priority under 35 U.S.C. § 119(e) of U.S. Provisional Patent Application No. 61/409,893, filed November 03, 2010, and entitled "ARCHITECTURE FOR MEMORY MODULE WITH PACKAGES OF THREE-DIMENSIONAL STACKED (3DS) MEMORY CHIPS." The disclosure of each of the above applications is hereby incorporated by reference in its entirety.

BACKGROUND

Technical Field

[0002] The present disclosure relates to memory devices and memory modules. More specifically, the present disclosure relates to systems and methods for reducing the load of drivers of memory packages included on the memory modules.

Description of the Related Art

[0003] Memory modules may include a number of memory packages. Each memory package may itself include a number of array dies that are packaged together. Each array die may include an individual semiconductor chip that includes a number of memory cells. The memory cell may serve as the basic building block of computer storage representing a single bit of data.

[0004] FIGS. 1A and 1B schematically illustrate examples of existing memory package designs currently used or proposed to be used to provide the dynamic random-access memory of memory modules. FIG. 1A schematically illustrates a memory package 100 with three array dies 110 and a control die 130. The control die

130 is configured to respond to signals received by the memory package 100 by sending appropriate control signals to the array dies 110 and includes a driver 134 for driving data signals to each of the array dies 110 via a corresponding die interconnect 120. Further, the control die 130 includes a driver 140 for driving command and/or address signals to each of the array dies 110 via another corresponding die interconnect 142. For simplicity, FIG. 1A shows only a single driver 134, die interconnect 120, driver 140, and die interconnect 142. However, additional drivers and die interconnects may be included for each bit the memory package 100 is designed to support. Thus, a 16-bit memory may include 16 pairs of drivers and die interconnects for the data signals and other similar drivers and die interconnects for the command and/or address signals. Each array die 110 also includes a chip select port 144, with the chip select ports 144 of the array dies 110 configured to receive corresponding chip select signals to enable or select the array dies for data transfer. The array dies 110 are configured to transfer data (e.g. read or write) to or from the selected memory cells identified by the command, address, and chip select signals via the die interconnects.

[0005] In some cases, the control die 130 may include memory cells and therefore, also serve as an array die. Thus, as can be seen from FIG. 1A, the control die 130 may also include a chip select port 144. Alternatively, the control die 130 and the array dies 110 may be distinct elements and the control die 130 may not include any memory cells.

[0006] FIG. 1B schematically illustrates an example of a memory package 150 that includes four array dies 160 and a control die 170 that does not include memory cells. As can be seen in FIG. 1B, each array die 160 includes a chip select port 174. However, because the control die 170 does not also serve as an array die, the control die 170 does not include a chip select port. As with memory package 100, memory package 150 includes a driver 184 that drives data signals to each of the array dies 160 along a corresponding die interconnect 182. Further, the memory package 150 includes a driver 186 for driving command and/or address signals to each of the array dies 160 via another die interconnect 188.

[0007] Generally, a load exists on each of the drivers 134, 140, 184, and 186 by virtue of the drivers being in electrical communication with the corresponding die

interconnects and the corresponding circuitry of the array dies. Thus, to drive a signal along a die interconnect, a driver typically must be large enough to overcome the load on the driver. However, generally a larger driver not only consumes more space on the control die, but also consumes more power.

SUMMARY

[0008] In certain embodiments, an apparatus is provided that comprises a plurality of array dies having data ports. The apparatus further comprises at least a first die interconnect and a second die interconnect. The first die interconnect is in electrical communication with at least one data port of a first array die of the plurality of array dies and at least one data port of a second array die of the plurality of array dies and not in electrical communication with the data ports of at least a third array die of the plurality of array dies. The second die interconnect is in electrical communication with at least one data port of the third array die and not in electrical communication with the data ports of the first array die and the data ports of the second array die. In addition, the apparatus comprises a control die. The control die comprises at least a first data conduit configured to transmit a data signal to the first die interconnect and to not transmit the data signal to the second die interconnect, and at least a second data conduit configured to transmit the data signal to the second die interconnect and to not transmit the data signal to the first die interconnect.

[0009] In certain embodiments, an apparatus is provided that comprises a plurality of array dies having ports. The apparatus further comprises at least a first die interconnect and a second die interconnect. The first die interconnect is in electrical communication with at least one port of a first array die of the plurality of array dies and at least one port of a second array die of the plurality of array dies and not in electrical communication with the ports of at least a third array die of the plurality of array dies. The second die interconnect is in electrical communication with at least one port of the third array die and not in electrical communication with the ports of the first array die and the ports of the second array die. In addition, the apparatus comprises a control die. The control die comprises at least a first conduit configured to transmit a signal to the first die interconnect and to not transmit the signal to the second die interconnect, and at least a second conduit configured to transmit the signal to the second die interconnect and to not transmit the signal to the first die

interconnect. Moreover, a first load on the first conduit comprises a load of the first die interconnect, a load of the first array die, and a load of the second array die. In addition, a second load on the second conduit comprises a load of the second die interconnect and a load of the third array die.

[0010] In certain embodiments, a method is provided for optimizing load in a memory package. The memory package comprises a plurality of array dies, at least a first die interconnect and a second die interconnect, and a control die. The control die comprises at least a first driver and a second driver, the first driver configured to drive a signal along the first die interconnect, and the second driver configured to drive the signal along the second die interconnect. The method comprises selecting a first subset of array dies of the plurality of array dies and a second subset of array dies of the plurality of array dies. The first subset of array dies and the second subset of array dies are exclusive of one another and are selected to balance a load on the first driver and on the second driver based at least in part on array die loads of array dies of the plurality of array dies and at least in part on die interconnect segment loads of segments of at least the first die interconnect and the second die interconnect. The method further comprises forming electrical connections between the first die interconnect and the first subset of array dies. In addition, the method comprises forming electrical connections between the second die interconnect and the second subset of array dies.

[0011] In certain embodiments, an apparatus is provided that comprises a register device configured to receive command/address signals from a memory control hub and to generate data path control signals. The apparatus further comprises a plurality of DRAM packages. Each of the DRAM packages comprises a control die. The control die comprises a plurality of command/address buffers and a data path control circuit configured to control command/address time slots and data bus time slots. The control die is configured to receive data signals from the memory control hub, the data path control signals from the register device, and command/address signals from the register device. Further, each of the DRAM packages comprises a plurality of DDR DRAM dies operatively coupled to the control die to receive the data signals from the control die. Moreover, the memory module is selectively configurable into at least two operational modes. The two operational modes comprise a first operational

mode and a second operational mode. In the first operational mode the register device generates the data path control signals, and the control die uses the data path control signals to operate the data path control circuit. In the second operational mode, the control die operates the data path control circuit to provide the command/address signals to the plurality of DDR DRAM dies without decoding the command/address signals.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] Throughout the drawings, reference numbers are re-used to indicate correspondence between referenced elements. The drawings are provided to illustrate certain example embodiments of the inventive subject matter described herein and not to limit the scope thereof.

[0013] FIGS. 1A and 1B schematically illustrate examples of existing memory package designs.

[0014] FIG. 2 schematically illustrates an example embodiment of a memory package in accordance with the present disclosure.

[0015] FIG. 3 schematically illustrates another example embodiment of a memory package in accordance with the present disclosure.

[0016] FIG. 4 schematically illustrates an example embodiment of a driver structure of a control die in accordance with the present disclosure.

[0017] FIG. 5 presents a flowchart for an example embodiment of a load optimization process.

[0018] FIGS. 6A and 6B schematically illustrate an example of a Load Reduction Dual In-line Memory Module (LRDIMM) and a HyperCloud™ Dual In-line Memory Module (HCDIMM) architecture respectively.

[0019] FIG. 7 schematically illustrates an example of a Three-Dimensional Structure Dual In-line Memory Module (3DS-DIMM) architecture.

[0020] FIG. 8 schematically illustrates an example embodiment of a memory module architecture in accordance with the present disclosure.

DETAILED DESCRIPTION OF SPECIFIC EMBODIMENTS

[0021] In addition to the below, the following U.S. patents are incorporated in their entirety by reference herein: U.S. Patent Nos. 7,289,386, 7,286,436, 7,442,050, 7,375,970, 7,254,036, 7,532,537, 7,636,274, 7,630,202, 7,619,893, 7,619,912, 7,811,097. Further, the following U.S. patent applications are incorporated in their entirety by reference herein: U.S. Patent Application Nos. 12/422,912, 12/422,853, 12/577,682, 12/629,827, 12/606,136, 12/874,900, 12/422,925, 12/504,131, 12/761,179, and 12/815,339.

[0022] Certain embodiments of the present disclosure reduce the size of drivers that are configured to drive a signal, such as a data signal, along a die interconnect to one or more array dies. Further, certain embodiments of the present disclosure reduce the power consumption of the drivers.

[0023] In certain embodiments, reducing one or both of driver size and driver power consumption may be accomplished by increasing the number of die interconnects and reducing the number of array dies that are in electrical communication with each die interconnect. For example, instead of one die interconnect in electrical communication with four array dies, there may be two die interconnects, each in electrical communication with a different pair of the four array dies.

[0024] In certain embodiments, determining the number of die interconnects and the number of array dies in electrical communication with each die interconnect is based, at least in part, on a load of each array die and a load of the die interconnect that is in electrical communication with one or more of the array dies.

[0025] In some embodiments, the load contribution from a die interconnect may be negligible compared to the load contribution from the array dies. In such embodiments, determining the number of die interconnects and the number of array dies in electrical communication with each die interconnect may be based, at least in part, on a load of each array die without considering the load of the die interconnect. However, as the physical size of a memory package shrinks, the load of a die interconnect becomes a non-negligible value relative to the load of the array dies. Thus, as memory packages become physically smaller, it becomes more important to consider the load of the die interconnect in determining the number of die

interconnects and the number of array dies in electrical communication with each die interconnect. Advantageously, certain embodiments of the present disclosure account for both the loads of the array dies and the loads of the die interconnects on a conduit (e.g., driver) in determining the number of die interconnects to be used and the number of array dies in electrical communication with each die interconnect.

[0026] FIG. 2 schematically illustrates an example embodiment of a memory package 200 in accordance with the present disclosure. One example of a memory package that includes array dies and a control die is the Hybrid Memory Cube (HMC). Examples of an HMC compatible with certain embodiments described herein are described by the IDF2011 Intel Developer Forum website, http://www.intel.com/idf/index.htm, which includes presentations and papers from the IDF2011 Intel Developer Forum including the keynote address given by Justin Rattner on September 15, 2011. Additional examples of an HMC compatible with certain embodiments described herein are described by the Hybrid Memory Cube Consortium website, http://www.hybridmemorycube.org. The memory package 200 can include any type of memory package. For example, the memory package 200 may be a DRAM package, a SDRAM package, a flash memory package, or a DDR SDRAM package (e.g., DDR3, DDR4), to name a few. A memory module (not shown) may include one or more memory packages in accordance with the memory package 200. Further, the memory package 200 may include input/output terminals (not shown) that are configured to be placed in electrical communication with circuitry of the memory module to transmit signals between the memory package 200 and a Memory Control Hub (MCH) (not shown).

[0027] The memory package 200 may include a plurality of array dies 210 (e.g., array dies 210a-210d). The plurality of array dies 210 may be sealed within the memory package 200. Further, circuitry of the array dies 210 may be in electrical communication with the input/output terminals of the memory package 200. Although generally referred to as array dies herein, the array dies 210 may also be called slave dies or slave chips. Each of the array dies 210a-210d may include circuitry (e.g., memory cells) (not shown) for storing data. Examples of array dies compatible with certain embodiments described herein are described by the existing literature regarding the Hybrid Memory Cube (e.g., as cited above). As illustrated in FIG. 2, the

plurality of array dies 210 may be arranged in a stack configuration known as a three-dimensional structure (30S). Examples of 30S compatible with certain embodiments described herein are described by the existing literature regarding the Hybrid Memory Cube (e.g., as cited above). However, the structure or layout of the plurality of array dies 210 is not limited as such, and other structures are possible in accordance with the present disclosure. For example, the plurality of array dies 210 may be arranged in a planar structure, or in a structure that combines 30S with a planar structure. Moreover, while the memory package 200 is illustrated as including four array dies, the memory package 200 is not limited as such and may include any number of array dies. For example, as illustrated in FIG. 3, the memory package 200 may include eight array dies. As further examples, the memory package 200 may include three or sixteen array dies.

[0028] Each of the array dies 210 may include one or more data ports (not shown). The data ports enable electrical communication and data transfer between the corresponding memory circuitry of the array dies 210 and a communication pathway (e.g., a die interconnect).

[0029] In the example schematically illustrated in FIG. 2, the memory package 200 includes a plurality of die interconnects 220 (e.g., die interconnects 220a, 220b). For example, certain versions of HMC have been reported to have 512 data ports per die, with the corresponding bits of each die all connected to a single die interconnect (e.g., TSV). Examples of die interconnects include, but are not limited to, through-silicon vias (TSV), conducting rods, wire bonds, and pins. (See e.g., U.S. Patent Nos. 7,633,165 and 7,683,459.) Each of these die interconnects 220 may be coupled to, or in electrical communication with at least one data port of at least one of the array dies 210. In certain embodiments, at least one of the die interconnects 220 is in electrical communication with at least one data port from each of at least two array dies 210 without being in electrical communication with a data port from at least one array die 210, which may be in electrical communication with a different die interconnect 220.

[0030] For example, die interconnect 220a may be in electrical communication with a data port from array die 210a and a data port from array die 210b (as illustrated by the darkened circles in FIG. 2) and not in electrical communication with any data ports from array die 210c or any data ports from array die 210d. The data ports of array dies

210a and 210b in electrical communication with the die interconnect 220a can be corresponding to the same data bit (e.g., 00). Other die interconnects (not shown) can be in electrical communication with other data ports corresponding to other data bits (e.g., 01, 02, ...) of array dies 210a and 210b. These other die interconnects can be electrically isolated from the corresponding data ports of array dies 210c and 210d.

[0031] However, continuing this example, the die interconnect 220b may be in electrical communication with a data port from array die 210c and a data port from array die 210d (as illustrated by the darkened circles in FIG. 2) (e.g., corresponding to the same data bit, e.g., 00) without being in electrical communication with any data ports from array die 210a and array die 210b. Other die interconnects (not shown) can be in electrical communication with other data ports corresponding to other data bits (e.g., 01, 02, ...) of array dies 210c and 210d. Despite not being in electrical communication with any data ports from array die 210a and 210b, in some implementations, the die interconnect 220b may pass through the array dies 210a and 210b (as illustrated by the unfilled circles) e.g., through through-holes or vias of array dies 210a and 210b. For some implementations, each of the array dies 210 may be in electrical communication with corresponding die interconnects 220, without any of the die interconnects 220 being in electrical communication with all of the array dies 210. Where existing systems may utilize a single die interconnect to be in electrical communication with the corresponding data ports of each array die (e.g., the data ports corresponding to the same bit), certain embodiments described herein utilize multiple die interconnects to provide electrical communication to the corresponding data ports of the array dies (e.g., the data ports corresponding to the same data bit) with none of the multiple die interconnects in electrical communication with data ports of all the array dies.

[0032] In addition to the plurality of array dies 210, the memory package 200 includes a control die 230, which may also be called a master die. Examples of master dies compatible with certain embodiments described herein are described by the existing literature regarding the Hybrid Memory Cube (e.g., as cited above). In some embodiments, the control die 230 may be one of the array dies 210. Alternatively, the control die 230 may be a modified version of one of the array dies 210. Thus, in some implementations, memory package 200 may include four dies or chips instead of the

five illustrated in FIG. 2. Further, in some embodiments, the control die 230 may comprise a logic layer (e.g., the logic layer of an HMC).

[0033] The control die 230 may include a number of data conduits 232, which includes data conduits 232a and 232b. Each of these data conduits 232 may be configured to transmit a data signal to a single die interconnect 220. For example, the data conduit 232a may be configured to transmit a data signal to the die interconnect 220a without transmitting the data signal to the die interconnect 220b. Conversely, the data conduit 232b may be configured to transmit the data signal to the die interconnect 220b without transmitting the data signal to the die interconnect 220a (e.g., data conduit 232b is electrically isolated from die interconnect 220a and data conduit 232a is electrically isolated from die interconnect 220b).

[0034] In some embodiments, the data conduits 232 may also include one or more drivers 234 as schematically illustrated by FIG. 2. The drivers 234 may be configured to drive the data signals along the corresponding die interconnects 220. In some embodiments, a single data conduit 232 or driver 234 may be in electrical communication with multiple die interconnects 220, each of which may be in electrical communication with different array dies 210.

[0035] Each of the data conduits 232 may be configured to receive the data signal from a common source. For instance, the data conduit 232a and the data conduit 232b may each receive a substantially similar, if not identical, data signal from the same signal source (e.g. the data signal corresponding to the same data bit). The source of the data signal may include a data path, a driver, a latch, a pin, or any other construct that may provide a data signal to a data conduit.

[0036] The data conduits 232 may each be subject to a load. Although not limited as such, this load may be measured as a capacitive load, such as a parasitic capacitance. The load on each of the data conduits 232 may include at least a load of the die interconnect 220 to which the data conduit 232 is coupled or connected as well as a load of each array die 210 with which the die interconnect 220 is in electrical communication via a data port of the die interconnect 220. Thus, for example, the load of the data conduit 232a may include loads of the die interconnect 220a, the array die 210a, and the array die 210b. Similarly, the load of the data conduit 232b may

include loads of the die interconnect 220b, the array die 210c, and the array die 210d.

[0037] Generally, a load that would be on a data conduit that was in electrical communication with a die interconnect that was in electrical communication with at least one data port of each of the array dies 210 can be considered the maximum load for a data conduit. This maximum load is the load of a data conduit of a memory package that does not implement the teachings of this disclosure, but is in accordance with conventional configurations.

[0038] In some implementations, the difference between the load of the data conduit 232a and the load of the data conduit 232b is less than the maximum load for a data conduit as described above. Thus, in some cases, there may exist a degree of balance or equalization between the loads of the data conduits 232a, 232b. In some implementations, the difference between the load of the data conduit 232a and the load of the data conduit 232b is zero or substantially zero. In some embodiments, the length of each die interconnect 220, and the number of array dies 210 in electrical communication with each die interconnect 220 may be selected to maintain the difference between the load of the data conduit 232a and the load of the data conduit 232b to be at or below a threshold load difference. For example, suppose that the load of each array die 210 is 1, the load of each segment of the die interconnects 220 is 0.25, and that the threshold load difference is 0.5. Using the configuration schematically illustrated in FIG. 2, the load on the data conduit 232a in this example is 2.5 and the load on the data conduit 232b in this example is 3. Thus, in this example, the difference between the load of the data conduit 232a and the load of the data conduit 232b is at the threshold load difference value of 0.5. However, an alternative configuration that places the die interconnect 220a in electrical communication with only the array die 210a, and the die interconnect 220b in electrical communication with the array dies 210b-210d would not satisfy the threshold load difference value of 0.5 of the above example. In the alternative configuration, the load on the data conduit 232a would be 1.25 and the load on the data conduit 232b would be 4. Thus, in the alternative configuration, the difference between the load of the data conduit 232a and the load of the data conduit 232b is 2.75, which is above the threshold load difference value of 0.5.

[0039] For certain embodiments, the load of each data conduit is less than the

maximum load as described above. Thus, in some cases, the load of the data conduit 232a is less than the maximum load and the load of the data conduit 232b is less than the maximum load. Further, in many implementations, the combined load of the data conduit 232a and the data conduit 232b is less than the maximum load of a single data conduit. In other words, it is possible to design the data conduit 232a and the data conduit 232b to reduce the overall load compared to a single data conduit that is in electrical communication with a die interconnect that is in electrical communication with at least one data port of each of the array dies 210. By reducing the overall load compared to the single data conduit, it is possible in many cases to reduce power consumption. Further, it is possible in many cases to maintain signal quality (e.g. maintain signal amplitude, maintain low signal distortion, etc.) while reducing power consumption. Advantageously, in a number of embodiments, by using multiple data conduits instead of a single data conduit, the speed of the memory package 200 can be increased. In some cases, this speed increase can include a reduced latency in accessing array dies 210 and/or operating the memory package 200 at a higher clock frequency.

[0040] Each of the die interconnects 220 may include any type of conducting material. For example, the die interconnects 220 may include copper, gold, or a conductive alloy, such as a copper/silver alloy. Further, the die interconnects 220 may include any type of structure for enabling electrical communication between the data conduits 232 and the data ports of the array dies 210. For example, the die interconnects 220 may include a wire, a conducting rod, or a conducting trace, to name a few. Moreover, the die interconnects 220 may use vias, or through-silicon vias (TSVs) to couple with or to electrically communicate with an array die. For instance, die interconnect 220a may be connected with data ports of the array dies 210a and 210b using vias (illustrated by the filled or darkened circles). Examples of TSVs which may be used with the present disclosure are described further in U.S. Patent Nos. 7,633,165 and 7,683,459.

[0041] In addition, the die interconnects 220 may use via holes to pass through an array die that is not configured to be in electrical communication with the die interconnect. For instance, die interconnect 220b may pass through array dies 210a and 210b using TSVs that do not electrical communication between the die

interconnect 220b and data ports of the array dies 210a and 210b (illustrated by the unfilled circles). In this way, the array dies 210a, 210b are not responsive to the data signals being transmitted by the die interconnect 220b. However, the die interconnect 220b may be connected with at least one data port of each of the array dies 210c and 210d using a via (illustrated by the filled or darkened circles). In cases where the die interconnect passes through an array die that is not configured to be in electrical communication with the die interconnect, the TSV may include an insulator or an air gap between the die interconnect and the array die circuitry that is large enough to prevent electrical communication between the die interconnect and the array die circuitry. In certain embodiments, the TSV for array dies that are configured to be in electrical communication with the die interconnect and for array dies that are not configured to be in electrical communication with the die interconnect may be configured the same. However, in such cases, electrical connections leading from the TSV of the array dies that are not configured to be in electrical communication with the die interconnect may not exist or may be stubs. These stubs are not configured to provide electrical communication with the memory cells of the array die.

[0042] Although FIG. 2 illustrates a single pair of data conduits 232 corresponding to a single pair of die interconnects 220, this is only to simplify the drawing figure. The memory package 200 may generally include as many additional data conduits and corresponding die interconnects as the number of bits the memory package 200 is designed or configured to support per memory address. Thus, if, for example, the memory package 200 is configured to be a 16-bit memory, the memory package 200 may include 16 pairs of data conduits 232 and 16 pairs of corresponding die interconnects 220. Similarly, if the memory package 200 is configured as a 32-or 64-bit memory, the memory package 200 may include 32 or 64 pairs of data conduits 232 and 32 or 64 pairs of corresponding die interconnects 220. Generally, the data conduits and die interconnects for each bit are configured identically. Thus, for the memory package 200, each data conduit is configured to be in electrical communication with a die interconnect that is configured to be in electrical communication with a pair of the array dies 210. However, it is possible that, in some embodiments, the data conduits and die interconnects of different bits may be configured differently.

[0043] In certain embodiments, the same die interconnects and the same corresponding data conduits may be used to transfer data both to and from the array dies 210. In such embodiments, the die interconnects may be bi-directional. In alternative embodiments, separate die interconnects and corresponding data conduits may be used to transfer data to the array dies 210 and data from the array dies 210 to the control die 230. Thus, such embodiments may include double the number of die interconnects and data conduits as embodiments that use the same die interconnect to transfer data to and from an array die.

[0044] In some embodiments, the control die 230 may include additional command/address conduits 240 and die interconnects 242, which may be in electrical communication with at least one port of each of the array dies 210. For simplicity, FIG. 2 shows only a single such conduit 240 and die interconnect 242. The command/address conduits 240 are configured to provide corresponding signals to the die interconnects 242. These signals may be command signals, address signals, or may serve as both command and address signals (e.g., may include a memory cell address and a write command or a read command) either simultaneously or based on a determining criterion, such as the edge of a clock signal. The command die 230 may include a command/address conduit 240 and corresponding die interconnect 242 for each bit of the command/address signals that the memory package 200 is configured to support. The number of bits of the command/address signals may be the same or may be different from the number of data bits of the memory package 200.

[0045] In addition, in certain embodiments, the control die 230 may include a plurality of chip select conduits 250 (e.g., chip select conduits 250a-250d as shown in FIG. 2). Further, the control die 230 may include corresponding die interconnects 252 (e.g., die interconnects 252a-252d) with one die interconnect 252 in electrical communication with one chip select conduit 250 and one array die 210. Each of the die interconnects 252 may be in electrical communication with a different array die 210. For example, the die interconnect 252a may be in electrical communication with the array die 210a and the die interconnect 252b may be in electrical communication with the array die 210b. Each of the chip select conduits 250 may be configured to provide a chip select signal to a corresponding array die 210 via a corresponding die interconnect 252.

[0046] In some embodiments, the control die 230 may include additional drivers that are configured to drive the chip select signals along the die interconnects 252. Alternatively, the chip select signals may be driven by drivers that are external to the control die 230. For example, a register (not shown) that is part of a memory module that includes the memory package 200 may determine the chip select signals and drive the chip select signals to the array dies 210. As a second example, the chip select signals may be provided by an MCH. In some embodiments, the control die 230 may determine the array die 210 to select based on, for example, an address signal. In such embodiments, the control die may generate the chip select signals.

[0047] FIG. 3 schematically illustrates another example embodiment of a memory package 300 in accordance with the present disclosure. In certain embodiments, some or all of the embodiments described above with respect to the memory package 200 may be applicable to the memory package 300. However, for ease of illustration and to simplify discussion, certain elements are omitted in FIG. 3, such as the chip select conduits. Nevertheless, it should be understood that the memory package 300 can include the same or similar elements as described above with respect to the memory package 200, including, for example, the chip select conduits.

[0048] The memory package 300 may include a plurality of array dies 310 (e.g., array dies 310a-310h). In the implementation illustrated in FIG. 3, the memory package includes eight array dies. However, as stated earlier, the memory package 300 may include more or fewer array dies. Each of the array dies 310 may include one or more ports (not shown) that enable electrical communication between the circuitry of the array dies 310 and one or more die interconnects 320. Each of these die interconnects 320 may be coupled to, or in electrical communication with at least one port of at least one of the array dies 310. As with the memory package 200, in certain embodiments, at least one of the die interconnects 320 is in electrical communication with at least one port from each of at least two array dies 310 without being in electrical communication with a port from at least one array die 310, which may be in electrical communication with a different die interconnect 320.

[0049] In addition to the plurality of array dies 310, the memory package 300 includes a control die 330. In some embodiments, the control die 330 may include a number of conduits 332 (e.g., conduits 332a-332f). Each of these conduits 332 may be

configured to transmit a signal to a single die interconnect 320.

[0050] Further, implementations of the conduits 332 may include one or more drivers 334 (e.g., drivers 334a-334f). Each of the drivers 334 may be configured to drive a signal along a corresponding die interconnect 320. For instance, the driver 334a of the conduit 332a may be configured to drive a signal along the die interconnect 320a to one or more of the array dies 310a and 310b. As a second example, the driver 334b of the conduit 332b may be configured to drive a signal along the die interconnect 320b to one or more of the array dies 310c and 310d. Although the die interconnect 320b may pass through the array dies 310a and 310b, because the die interconnect 320b, in the example illustrated in FIG. 3, is not configured to be in electrical communication with the array dies 310a and 310b, the driver 334b does not drive the signal to the array dies 310a and 310b.

[0051] In some embodiments, the signal can be a data signal, a command or address signal, a chip select signal, a supply voltage signal, or a ground voltage signal, to name a few. Further, as the signal is not limited to a data signal, in some embodiments, the conduits 332 may include conduits configured to provide signals other than data signals to the die interconnects 320. For example, the conduits may include conduits configured to provide a command or address signal, a chip select signal, a supply voltage signal, or a ground voltage signal to one or more die interconnects. Consequently, in some embodiments, the drivers 334 may be configured to drive signals other than data signals.

[0052] Generally, the signal that each of the drivers 334 drive to the corresponding die interconnects 320 is from a common source. Thus, each of the drivers 334, in certain embodiments, is driving the same signal to each corresponding die interconnect 320.

[0053] The size of the drivers 334 is generally related to the load on the driver 334. In certain embodiments, the load on each driver 334 corresponds to the load of the respective conduit 332. Although not limited as such, the load may be measured as a capacitive load, such as a parasitic capacitance.

[0054] The load on each of the conduits 332 may include at least the loads of the die interconnect 320 with which the conduit 332 is coupled or connected as well as the

loads of each array die 310 with which the die interconnect 320 is in electrical communication via a port of the die interconnect 320. Thus, for example, the loads of the conduit 332a may include the loads of the die interconnect 320a, the array die 310a, and the array die 310b. Similarly, the loads of the conduit 332b may include the loads of the die interconnect 320b, the array die 310c, and the array die 310d. The loads of both conduits 332a and 332b include a load of two array dies 310 because the corresponding die interconnects 320 are each configured to be in electrical communication with two array dies 310. On the other hand, the load of the conduit 332c, which may include the loads of the die interconnect 320c and the array die 310e, includes a load of one array die 310e because the corresponding die interconnect 320c is configured to be in electrical communication with only one array die 310.

[0055] As previously described with respect to FIG. 2, a load that would be on a conduit that was in electrical communication with a die interconnect that was in electrical communication with at least one port of each of the array dies 310 can be considered the maximum load for a conduit. This maximum load is the load of a conduit of a memory package that does not implement the teachings of this disclosure, but is used in accordance with conventional configurations.

[0056] In some implementations, the difference between the loads of any pair of the conduits 332 is less than the maximum load for a conduit as described above. For instance, the difference between the load of the conduit 332a and the load of the conduit 332b is less than the maximum load. As a second example, the difference between the load of the conduit 334f and anyone of the conduits 334a334e is less than the maximum load. Thus, in some cases, the load on each of the conduits 332 may be, at least partially balanced or equalized to reduce or minimize the difference between the load of any pair of the conduits 332. In some implementations, the difference between the load of a pair of the conduits 332 is zero or substantially zero. In some embodiments, the length of each die interconnect 320, and the number of array dies 310 in electrical communication with each die interconnect 320 may be selected to maintain the difference between the load of any pair of the conduits 332 to be at or below a threshold load difference.

[0057] For certain embodiments, the load of each conduit is less than the maximum

load as described above. Thus, for example, the load of the conduit 332a, the load of the conduit 332b, and the load of the conduit 332c are each less than the maximum load defined above.

[0058] In certain embodiments, the load associated with each of the array dies 310 may be substantially equivalent. For example, the load of the array die 310a may be substantially equal to the load of the array die 310h. Thus, the load contribution from the array dies 310 for a specific conduit 332 may be measured as a multiple of the array dies that are in electrical communication with a die interconnect 320 corresponding to a specific conduit 332. For example, assuming that the load of each of the array dies 310 is 'L', then the contribution of the load from the array dies 310 to the conduit 332a would be 2L because the die interconnect 320a corresponding to the conduit 332a is in electrical communication with two array dies 310, array dies 310a and 310b. In alternative embodiments, the load of each of the array dies 310a may differ. For example, the load of array die 310a may be L and the load of the array die 310b may be 1.25L.

[0059] Similar to the array dies 310, in some embodiments, a die interconnect 320 can be considered to comprise a plurality of segments, with each segment of a die interconnect 320 contributing a substantially equivalent load to the load of the die interconnect 320. In this case, the segment of the die interconnect 320 may refer to the portion of the die interconnect between two successive or adjacent dies (array die-to-array die, master die-to-array die, or both) along the die interconnect 320. Further, the segment may be defined as a portion of the die interconnect 320 between the dies exclusive of a portion of the dies. For example, one segment of the die interconnect 320a may extend from the top of the array die 310a to the bottom of the array die 310b. Alternatively, the segment may be defined to include at least a portion of at least one of the array dies 310. For example, one segment of the die interconnect 320a may extend from the center of array die 310a to the center of array die 310b. As a second example, one segment of the die interconnect 320a may extend from the top of the control die 330 to the top of the array die 310a, and therefore may include a portion of the die interconnect 320a extending from the bottom of the array die 310a to the top of the array die 310a. In some implementations, the segments are substantially equal in length to each other. Moreover, the load contribution of each

segment may be substantially equal to each other. Alternatively, the segments may be unequal in length and/or may each contribute a different load to the total load of a die interconnect 320. Further, in some cases, the load contribution of a segment of the die interconnect 320 that is in electrical communication with a port of an array die 310 may differ from the load contribution of a segment of the die interconnect 320 that is not in electrical communication with a port of an array die 310.

[0060] In some cases, the load contribution of each segment of the die interconnect 320 may be measured as a fraction of the load contribution from an array die 310. For example, the load of one segment of the die interconnect 320a may be equivalent to one quarter of the load of an array die 310. Thus, for example, the load of the conduit 332a may be 2.5L assuming a load contribution of L per array die 310 (two in this case) in electrical communication with the die interconnect 320a and a load contribution of 0.25L per segment (two in this case) of the die interconnect 320a. As a second example, the load of the conduit 332f may be 3L assuming the same load values as the previous example and a load contribution from one array die 310h and eight die interconnect 320f segments. Table 1 specifies the capacitive load values for each conduit 332 assuming, as with the previous two examples, that the load of each of the array dies 310 is L, and that the load of each segment of the die interconnects 320 is 0.25L. Table 1 also specifies the deviation in load from the conduits having the highest load value, which in this example are conduits 332b and 332f.

TABLE 1

Conduit	Number of Array Dies	Number of Die Interconnect Segments	Capacitive Load	Deviation from Maximum Load
332a	2	2	2.5L	0.5
332b	2	4	3L	0
332c	1	5	2.25L	0.75
332d	1	6	2.5L	0.5
332e	1	7	2.75L	0.25
332f	1	8	3L	0

[0061] As can be seen from Table 1, the maximum load of any conduit 332, using the example values previously described, is 3L, or rather three times the load of a single array die 310. Assuming the same example values, the load of a conduit in electrical communication with a die interconnect that itself is in electrical communication with each array die 310 would be 10L. Thus, certain embodiments of the present disclosure

enable a reduction in the load of the conduits 332. Consequently, in some embodiments, the drivers 334 may each be smaller than a single driver that is configured to drive a signal from a conduit along a single die interconnect that is in electrical communication with a port from each of the array dies 310. Moreover, the drivers 334 may include smaller transistor sizes than a single driver that is configured to drive a signal to each of the array dies 110.

[0062] As can be seen from Table 1, conduits 332b and 332f have the largest capacitive load of the group of conduits, which is 3L. Conduit 332 has the smallest capacitive load of the group of conduits, which is 2.25L and which is a deviation of only 0.75 from the maximum load. Thus, in some embodiments, each of the drivers 334 may be substantially similar in size. In certain implementations, the drivers 334 may vary in size based on the total capacitive load on each conduit 332. Thus, the driver 334f may be larger than the driver 334e. Alternatively, each driver 334 may be substantially equal and may be configured based on the drivers 334 with the largest load, which are drivers 334b and 334f in the example illustrated in FIG. 3 and Table 1.

[0063] In some embodiments, the capacitive load of each conduit 332 or driver 334 can be calculated using formula (1).

$$CL = AD + {}^{S}/_{M}$$

[0064] In formula (1), CL represents the capacitive load of a conduit 332 or driver 334, AD represents the number of array dies 310 in electrical communication with a die interconnect 320 that is in electrical communication with the conduit 332 and/or driver 334, S represents the number of die interconnect segments of the die interconnect 320, and M represents the ratio of the load of an array die 310 to the load of a segment of a die interconnect 320. Thus, using formula (1) and the example values described above, the load of the driver 332a, for example, can be calculated with the following values: AD=2, for two array dies 310; S=2, for the two segments of the die interconnect 320a; and M=4, for the ratio of the load of an array die 310, L, to the load of a segment of the die interconnect 320a, 0.25L. Therefore, as can be seen from Table 1, the capacitive load of the driver 332a is 2.5L where L is the load of a single array die.

[0065] In some cases, the load on each conduit 332 and/or driver 334 may be evenly balanced. In other words, the load on each conduit 332 and/or driver 334 may be substantially the same. To achieve a balanced load, each of the conduits 332 may be in electrical communication with a combination of array dies 310 and die interconnect 320 segments that results in a load that is substantially equivalent to the loads of the other conduits 332. In certain embodiments, the load of the conduits 332 is balanced despite each conduit 332 being in electrical communication with a different subset of the array dies 310. However, in alternative embodiments, the load of each conduit 332 and/or driver 334 may differ. This difference in the load of the conduits 332 and/or drivers 334 may be a design decision (e.g. to maintain a specific number of drivers). Alternatively, or in addition, the load difference between conduits 332 and/or drivers 334 may occur because the loads of the array dies 310 and the die interconnect segments 320 do not allow for perfect or substantially even load balancing.

[0066] As previously stated, in some embodiments the loads of the conduits 332 and/or drivers 334 may be balanced to minimize the difference between any pair of conduits 332 and/or drivers 334. For example, as illustrated in FIG. 3, a driver in electrical communication with a longer die interconnect, which may consequently include more die interconnect segments, is likely to obtain a larger load contribution from the die interconnect than a driver in electrical communication with a shorter die interconnect (e.g., compare driver 334f to 334a). Thus, the driver in electrical communication with the longer die interconnect may be in electrical communication with fewer array dies than the driver in electrical communication with the shorter die interconnect (e.g. compare driver 334f to 334a). The selection of die interconnect length and the selection of array dies to place in electrical communication with the die interconnects may therefore be dependent on the load of each segment of the die interconnects 320 and the loads of the array dies 310.

[0067] Alternatively, or in addition, the loads of the conduits 332 and/or drivers 334 may be balanced to reduce the maximum load of each conduit 332 and/or driver 334. Further, in some embodiments, the maximum load of each conduit 332 and/or driver 334 may be reduced to maintain the load of each conduit 332 and/or driver 334 to be at or below a threshold load difference.

[0068] Although not illustrated in FIG. 3, each of the conduits 332 may include one or

more additional drivers configured to drive a signal received from an array die via a corresponding die interconnect 320. The additional drivers may drive the signal to a processor, a register, a latch, or any other component or device that mayor may not be part of a memory module that includes the memory package 300. In some implementations, one or more of the die interconnects 320 are configured to be bi-directional, thereby enabling a signal to be driven to the array dies 310 via the die interconnect 320, and to enable a signal received from the array dies 310 along the same die interconnect 320 to be transmitted to a corresponding conduit 332 of the control die 330. Alternatively, the memory package 300 comprises one or more die interconnects 320 that are configured to enable a signal to be driven to the array dies 310 without enabling a signal to be received from the array dies 310 (e.g., the die interconnects 320 may not be bidirectional). In certain embodiments where one or more of the die interconnects 320 are not bi-directional, the memory package 300 may include additional die interconnects (not shown) that are in electrical communication with the one or more additional conduits or drivers and that are configured to enable a signal from the array dies 310 to be transmitted to the one or more additional conduits or drivers.

[0069] In addition to the drivers 334 of the control die 330, the memory package 300 may include one or more pre-drivers 340. A pre-driver 340, shown schematically in FIG. 3, may be large enough to drive a signal (e.g., a data signal) to any of the drivers 332 and subsequently, to any of the array dies 310. Thus, using the same example values as described above in relation to Table 1, a load of the pre-driver 340 may be at least 10l, which is the load of a conduit in electrical communication with a die interconnect that is in electrical communication with a port from each of the array dies 310. In some embodiments, the memory package 300 may include any number of additional drivers and/or latches for buffering and/or driving the signal to any of the array dies 310.

[0070] Just as the memory package 300 may include a pre-driver 340 for providing a signal to the conduits 332, the memory package 300 may include a post-driver (not shown) for driving an output signal from the control die 330. This post-driver may drive the output signal to additional latches and/or drivers. In some embodiments, the post-driver may drive the signal from the memory package 300 to a bus or other

electrical path that is in electrical communication with the memory package 300.

[0071] FIG. 4 illustrates an example embodiment of a driver structure 400 of a control die (e.g. control die 230) in accordance with the present disclosure. The driver structure 400 is configured for a single data bit. Thus, a control die for a 32-bit memory package will generally include at least 32 instances of the driver structure 400, one per bit. In some embodiments, the control die 230 may include the driver structure 400 in place of the combination of drivers 232a and 232b. Similarly, in certain embodiments, the control die 330 may include a structure similar to the driver structure 400 in place of the drivers 334. In such embodiments, the driver structure 400 would be modified to enable a signal (e.g., data signal) to be driven to the six conduits 332.

[0072] The driver structure 400 can include an input/output port 402 configured to receive or send a signal, such as a data signal. Signals received at the input/output port 402 can be provided to the drivers 404a and 404b. In turn, these drivers 404a and 404b can drive the signal to conduits 406a and 406b respectively, which are in electrical communication with corresponding die interconnects. Each of the die interconnects may be in electrical communication with different array dies in accordance with certain embodiments described herein.

[0073] In some embodiments, the driver structure 400 is bi-directional. In such embodiments, operation of the drivers 404a and 404b, and 408a and 408b may be controlled or enabled by a control signal (e.g., a directional control signal). This control signal, in some cases, may correspond to one or more of a command/address signal (e.g., read/write) and a chip select signal. In some implementations, the drivers 404a and 404b may drive a signal to the array die corresponding to the chip select signal, and not to array dies that do not correspond to a chip select signal. For example, suppose the conduit 406a is in electrical communication with array dies one and two (not shown), and that the conduit 406b is in electrical communication with array dies three and four (not shown). If a chip select signal is received corresponding to array die two, then in some implementations, driver 404a may be configured to drive a signal along a die interconnect in electrical communication with the conduit 406a to array die one and two. In this example, the driver 404b would not drive the signal because the chip select signal does not correspond to either array die three or

array die four.

[0074] In some embodiments, the drivers 404a and 404b may drive a signal to all of the array dies. For example, assume the memory package that includes the driver structure 400 also includes four array dies. If the die interconnect in electrical communication with the conduit 406a is in electrical communication with two of the array dies, and if the die interconnect in electrical communication with the conduit 406b is in electrical communication with the other two array dies, then the drivers 404a and 404b may drive a signal to all four of the array dies of this example.

[0075] Similar to the input/output port 402, the conduits 406a and 406b can be configured to receive a signal from the die interconnects that are in electrical communication with the conduits 406a and 406b. In turn, the signal received at one of the conduits 406a and 406b can be provided to drivers 408a and 408b respectively. The drivers 408a and 408b can each be configured to drive a signal received from a respective data conduit 406a and 406b to the input/output port 402 and to another component that may be in electrical communication with the input/output port 402, such as a MCH.

[0076] In some embodiments, one or more chip selects, as illustrated in FIG. 2, may be used to select, determine, or enable the array die that communicates the signal to or from one or more of the conduits 406a and 406b and the drivers 408a and 408b. Similarly, in some embodiments, the chip select may select, determine, or enable the array die to receive and/or respond to the signal driven by the drivers 404a and 404b to the array dies.

[0077] It should be noted that the driver structure 400 is a non-limiting example for arranging drivers in a control die. Other driver structures are possible. For example, instead of the drivers 404a and 408a being in electrical communication with the same conduit 406a, each of the drivers 404a and 408a can be in electrical communication with a separate conduit and consequently a separate die interconnect. In such an example, the drivers 404a and 408a may still be in electrical communication with the same input/output port 402, or each driver may be in electrical communication with a separate port, the driver 404a in electrical communication with an input port, and the driver 408a in communication with an output port.

[0078] FIG. 5 presents a flowchart for an example embodiment of a load optimization process 500. In certain embodiments, the load optimization process 500 may be performed, at least in part, by one or more computing systems. Further, the process 500, in some embodiments, may be used to optimize one or more loads in a memory package (e.g. memory package 200 or memory package 300). Optimizing the loads in the memory package can include optimizing the load on one or more conduits and/or drivers. As previously described with respect to FIGS. 2 and 3, the memory package can include a plurality of array dies, a plurality of die interconnects, and a control die. Furthermore, the control die can include a plurality of drivers, each of which may be configured to drive a signal along a die interconnect.

[0079] In some implementations, the process 500 can comprise selecting a first subset of array dies and a second subset of array dies from a plurality of array dies (e.g., array dies 310), as shown in operational block 502. Generally, the first subset of array dies and the second subset of array dies may be exclusive of one another. Thus, the first subset of array dies does not include any array dies from the second subset of array dies and vice versa. However, in some cases there may be some overlap between the first subset of array dies and the second subset of array dies. Further, in some cases, at least one of the subsets of array dies includes more than one array die. For instance, the first subset of array dies may include two array dies, and the second subset of array dies may include one array die, which, depending on the embodiment, mayor may not be included in the first subset of array dies.

[0080] Further, the first subset of array dies and the second subset of array dies may be selected to balance a load on a first driver and a load on a second driver based, at least in part, on the loads of the array dies 310 and on the loads of the die interconnect segments from a first and a second die interconnect. The first die interconnect may be in electrical communication with the first driver and the second die interconnect may be in electrical communication with the second driver. In some embodiments, the first subset of array dies and the second subset of array dies are selected to balance a load on a first conduit and a load on a second conduit. The load on each driver and/or conduit may be calculated using formula (1) as previously described above. In some embodiments, the first subset of array dies and the second subset of array dies may be selected to balance a load on a first driver and a load on a second driver based, at least

in part, on the loads of the array dies 310 without considering the loads of the die interconnect segments from the first die interconnect and the second die interconnect.

[0081] The process 500 further comprises forming electrical connections between the first die interconnect and the first subset of array dies in an operational block 504. The process 500 further comprises forming electrical connections between the second die interconnect and the second subset of array dies in an operational block 506. Forming the electrical connections places the die interconnects in electrical communication with the respective subsets of array dies. In some embodiments, forming the electrical connections can comprise forming electrical connections between the die interconnects and at least one port from each array die of the respective subsets of array dies.

[0082] The process 500 further comprises selecting a driver size for a first driver at block 508 and selecting a driver size for a second driver at block 510. Selecting the driver size can be based, at least in part, on the calculated load on the driver. Generally, the greater the load on the driver, the larger the driver is selected to drive a signal along, for example, a die interconnect. The size of the driver may be adjusted by the selection of the transistor size and/or number of transistors included in the driver. A larger driver often consumes more power than a smaller driver. Thus, in certain embodiments, balancing the loads on the drivers to reduce the load on each driver can reduce the power consumption of a memory package.

[0083] In some embodiments, the size of the first driver and the size of the second driver are both less than the size sufficient for a driver to drive a signal along a die interconnect to each of the array dies 310 (e.g., with less than a predetermined or threshold signal degradation). The threshold signal degradation can be based on anyone or more characteristics of a signal. For example, the threshold signal degradation can be based on the amplitude of the signal, the frequency of the signal, the noise distortion included in or introduced into the signal, or the shape of the signal, to name a few.

[0084] The process 500 further comprises forming electrical connections between the first die interconnect and the first driver in an operational block 512. Similarly, the process 500 further comprises forming electrical connections between the second die

interconnect and the second driver in an operational block 514. Forming the electrical connections places the die interconnects in electrical communication with the respective drivers. In some embodiments, forming the electrical connections can comprise forming electrical connections between the die interconnects and a data conduit that includes the respective driver.

[0085] Advantageously, certain embodiments of the present disclosure reduce the load on each conduit and on each corresponding driver. In certain embodiments, reducing the load on a driver may increase the speed of data transfer between the array dies and other components in a computer system (e.g. a MCH or a processor). Further, reducing the load on a driver may result in reduced power consumption by the driver and consequently, by the memory package. In addition, certain embodiments of the present disclosure may minimize current switching noise.

Operational Modes

[0086] A proposed three-dimensional stacking (3DS) standard for dual in-line memory modules (DIMMs) being considered by the Joint Electron Devices Engineering Council (JEDEC) addresses three major shortcomings in the current JEDEC registered DIMM (RDIMM) and JEDEC load reduced DIMM (LRDIMM) standards (an example LRDIMM structure 600 is schematically illustrated in FIG. 6A). These shortcomings include: a) The DIMM density limitation due to the fixed number of chip-select signals received by the DIMM from the system memory controller. b) The performance loss due to the increased load on the data bus as the DIMM density (e.g., the number of DRAM devices and number of ranks) increases. c) The upper bound of the DIMM density due to the physical DIMM form factor.

[0087] Further, the LRDIMM structure 600 may have timing issues due to signals passing through a single memory buffer 601. In addition, the increased size of the data path of the LRDIMM architecture 600, compared to the HCDIMM architecture 602, an example of which is schematically illustrated in FIG. 68, may result in more latency and signal integrity issues.

[0088] FIG. 7 schematically illustrates an example memory module 700 that has previously been proposed for the 3DS-DIMM standard. The proposed 3DS Dual In-line Memory Module (3DS-DIMM) schematically illustrated in FIG. 7 attempts to

address the above shortcomings using two components, a 3DS register 712 and a controller die 722. In some implementations, the 3DS-DIMM 700 includes the 3DS register 712 (also known as an enhanced DDR3 register). The 3DS register 712 may include a DDR3 JEDEC standard register with a "rank multiplication" circuit, which increases the number of the output chip-select signals for selecting an array die 710 by decoding one or more higher-order row or column address bits with the incoming chip-select signals from the system controller. The 3DS Register 712 can also include a command/address buffer, a register operational code buffer (RC word buffer), and rank multiplication logic (e.g., supporting rank multiplication of 1-to-2, 1-to-4, and/or 1-to-8). The 3DS register addresses shortcoming (a) of the JEDEC RDIMM and LRDIMM listed above.

[0089] Another component of the proposed 3DS-DIMM is a 3DS dynamic random-access memory (DRAM) package 720. The 3DS DRAM package 720 includes a plurality of stacked DDR DRAM chips 724 or array dies. The 3DS DRAM package 720 has a data I/O load that is equivalent to the data I/O load of a single-die DRAM package, regardless of the actual number of DRAM dies in the 3DS DRAM package 720. The 3DS DRAM package 720 may comprise a plurality of array dies (e.g., 2, 4 or 8 DDR DRAM dies) and a controller die 722. The controller die 722 may include data buffers, a data path timing controller, a secondary command/address buffer, a programmable secondary 1-to-2 rank decoder, and a data path signal (e.g., DDT, DDT, RTT) controller. Examples of such memory packages include HMC. The 3DS DRAM package 720 addresses the shortcomings (b) and (c) of the JEDEC RDIMM and LRDIMM listed above. However, there are deficiencies in the proposed 3DS-DIMM standard as described below.

[0090] The JEDEC DDR3 RDIMM standard contains two major components: a DDR3 register and a plurality of DRAM packages each comprising one or more DRAM chips or dies. The DDR3 register serves as a command/address signal buffer and as a command/control decoder. This DDR3 register holds a set of register control (RC) words, which a computer system configures to ensure the proper operation of the RDIMM. The DDR3 register contains a phase-lock-loop (PLL), which functions as a clock synchronizer for each RDIMM. The DDR3 register outputs a set of buffered command/address signals to all the DRAM packages on the RDIMM, but the

data signals are directly fed to the DRAM packages from the system memory controller.

[0091] In contrast to the JEDEC DDR3 RDIMM standard, the 3DS-DIMM proposal requires the DRAM package 720 to include the controller die 722 that controls all data paths timing and operations. This arrangement of the DRAM package reduces the load on the data bus, however, it presents three significant shortcomings: 1) The command/address buffer in the 3DS DRAM package introduces clock cycle latency since it needs to provide clock synchronous operation to the DRAM dies in the package. 2) The data path control circuit (e.g., DDT, read/write data direction) in the control die becomes very complicated to support semi-synchronous (flyby) data path control among all 3DS DRAM packages that are on a DIMM. 3) The variations in the DRAM die timing characteristics within each 3DS DRAM package would be likely to require resynchronization of the data signals during the read/write operations, which increases the read/write latency and the read-to-write and write-to-read turn around time.

[0092] The 3DS-DIMM proposal can also be compared to the HyperCloud™ (HC) DIMM architecture of Netlist, Inc. An example of the HCDIMM architecture 602 is illustrated in FIG. 68. Further details and embodiments of the HCDIMM architecture is disclosed in U.S. Pat. Nos. 7,289,386, 7,532,537, 7,619,912, and 7,636,274, each of which is incorporated in its entirety by reference herein. One of the main topological differences between the 3DS-DIMM and HCDIMM architectures is that while the 3DS-DIMM architecture uses a control die 722 to buffer the data signals and to decode command/address signals from the 3DS register, certain configurations of the HCDIMM architecture include a plurality of isolation devices (ID), each of which includes data buffers, but no decoding capability. Unlike the HCDIMM architecture, since the command/address signal needs to pass through the control die 722 in the 3DS DRAM package 720, the 3DSDIMM proposal presents the same shortcoming (b) of the controller die described above. The data path control signals are generated by the register device (RD) 612 in the HCDIMM architecture 602, while the data path control signals are generated by the control die 722 in the 3DS DRAM. This aspect of the 3DS-DIMM architecture creates timing critical control paths in 3DS-DIMM architecture.

[0093] In certain embodiments described herein, a memory module architecture is proposed that includes a set of device components that support JEDEC 3DS operation with the benefit of RDIMM and HCDIMM architectures (see, e.g., FIG. 8). This set of device components may comprise two components: a register device 812 (RD), which in some embodiments may be the same or similar RD component as used in HCDIMM architectures, and a plurality of array dies 824, such as a DDR DRAM Stack Package (DDSP). The DDSP may comprise a DRAM control die that can include command/address buffers and a data path control circuit. Certain embodiments of the architecture described herein differs from the 3DS-DIMM architecture in that instead of the controller die of the 3DS-DIMM (which provides a secondary address buffer, and a second rank multiplication decoder), certain embodiments described herein use an "ID+" die as a control die 822, which can provide both selective isolation and address pass-through. Selective isolation refers generally to a driver corresponding to an array die driving a signal to the array die in response to a corresponding chip select signal while additional drivers corresponding to additional array dies maintain a previous state (e.g. do not drive the signal). For example, assuming that the memory package 300 implements selective isolation, if a chip select signal is received that corresponds to a selection of array die 310b, then the driver 334a will drive a signal along the die interconnect 320a to the array die 310b, and the remaining drivers (e.g., drivers 334b-334f) will maintain their state (e.g., not drive the signal). Address pass-through is described in further detail below.

[0094] The data path control circuit of certain embodiments may have at least two operational modes: mode-C (HCDIMM/RDIMM Compatible mode) and mode-3DS (3DS DIMM compatible mode). In mode-C, the array dies 824 (e.g. a DDSP) receive the data path control signals from the register device 812, which can be configured to control a command/address time slot and a data bus time slot. In mode-3DS, the control die 822 internally generates the data path control signals to ensure the proper operation of the data path.

[0095] The control die 822 of certain embodiments enables the memory module 800 to work as either a 3DS-DIMM, a RDIMM, or a HCDIMM. However, the memory module 800 may comprise a set of optional control input pins (in addition to the package pins that are included in 3DS-DRAM packages) which in mode-C receive the

data path control signals from the register device 812.

[0096] As previously mentioned, FIG. 8 schematically illustrates an example embodiment of a memory module architecture 800 in accordance with the present disclosure. Advantageously, certain embodiments of the memory module architecture 800 address the shortcomings described above without adding complexity or latency, and without causing performance loss. The memory module architecture 800 includes a memory control hub 802 (also known as a memory controller hub, a memory control handler, or a northbridge) and a memory module 810. As schematically illustrated in FIG. 8, the memory control hub 802 may communicate directly with one or more components of the memory module 810. Alternatively, the memory control hub 802 may communicate with one or more intermediary system components (not shown), which in turn communicate with one or more components of the memory module 810. In some embodiments, the memory control hub 802 may be integrated with another component of the computer system, such as a Central Processing Unit (CPU).

[0097] Further, in some embodiments, the memory control hub 802 may communicate with one or more memory modules. Each of the memory modules may be similar or substantially similar to the memory module 810. Alternatively, some of the memory modules may differ from memory module 810 in configuration, type, or both. For example, some of the memory modules may be capable of operating at different frequencies, may include a different amount of storage capability, or may be configured for different purposes (e.g. graphics versus nongraphics memory). Although in some cases a system may include memory modules capable of operating at different frequencies, each memory module may be configured to operate at the same frequency when used in a specific device. In certain implementations, the memory control hub 802 may set the operating frequency for the one or more memory modules.

[0098] The memory module 810 may include a register device 812, which is configured to receive command, address, or command and address signals from the memory control hub 802. For the purpose of simplifying discussion, and not to limit these signals, the signals will be referred to herein as command/address signals.

[0099] In some embodiments, the register device 812 receives the command/address signals via a command/address bus 814. The command/address bus 814, although illustrated as a single line, may include as many lines or signal conduits as the number of bits of the command/address signal.

[0100] Further, the register device 812 may generate data path control signals, which can be provided to a control die 822, or isolation device, of a memory package 820 via one or more data path control lines 816. In certain embodiments, the control dies 822 can include some or all of the embodiments described above with respect to the control dies 230 and 330. Moreover, in certain embodiments, the memory packages 820 can include some or all of the embodiments described above with respect to the memory package 200 and 300. In general, the memory module 812 may include one or more memory packages 820.

[0101] In certain embodiments, each control die 822, or isolation device, may be capable of address pass-through. Address pass-through, in some cases, enables the control die 822 to provide an address signal to one or more array dies 824 without decoding the address signal. This is possible, in some implementations, because the address signal received by the control die 822 is not encoded.

[0102] Some implementations of the control dies 822 include a plurality of command/address buffers (not shown). These buffers may comprise latches. In certain embodiments, the buffers are configured to hold command/address signals to control the timing of command/address signals. In some cases, controlling the timing of the command/address signals may reduce or slow signal degradation. In some implementations, the control dies 822 include a plurality of data buffers, which may control the timing of data signals to reduce or slow signal degradation. Further, the control dies 822 may include a data path control circuit (not shown) that is configured to control command/address time slots and data bus time slots. Controlling the command/address time slots and the data bus time slots enables the control dies 822 to reduce or prevent signal collisions caused by multiple memory packages 820 sharing the data path control lines 816 and the data bus 818. In some implementations, the data path control circuit may be separate from the control die 822.

[0103] Each of the control dies 822 may be configured to receive data signals from

the memory control hub 802 via the data bus 818. Further, the control dies 822 may provide data signals to the memory control hub 802 via the data bus 818. The control dies 822 may also receive data path control signals and/or command/address signals from the register device 812 via the data path control lines 816.

[0104] As illustrated in FIG. 8, each memory package 820 may include one or more array dies 824 operatively coupled to the control die 822. The array dies 824 may be configured to receive data signals from the control die 822. As with the array dies 210 and 310, the array dies 824 may include any type of Random Access Memory (RAM) die. For example, the array dies 824 may include DDR DRAM, SDRAM, flash memory, or SRAM, to name a few. Further, if the memory module 810 is utilized for graphics, the array dies 824 may include GDDR SDRAM or any other type of graphics memory. In addition, the array dies 824 may be configured in a stack arrangement as illustrated in FIG. 8. Alternatively, the array dies 824 may be arranged in a planar configuration or a hybrid configuration utilizing both a planar and a stack arrangement.

[0105] In some embodiments, the memory module 810 is selectively configurable into two operational modes. In the first operational mode, the register device 812 generates data path control signals provided to the control dies 822 via the data path control lines 816. The control dies 822 may decode command/address signals included with the data path control signals generated by the register device 812. In some implementations, the control dies 822 use the data path control signals to operate the data path control circuits of the control dies 822.

[0106] In the second operational mode, the control dies 822 may operate the data path control circuits to provide command/address signals to the array dies 824 without decoding the command/address signals. In this mode, the control dies 822 may use address pass-through to provide received address signals to the array dies 824.

[0107] Other operational modes may also be possible. In some embodiments, the data path control signals generated by the register device 812 may include decoded command/address signals that are decoded from command/address signals received from the memory control hub 802 via the command/address bus 814.

[0108] In some embodiments, the register device 812 may be configured to perform

rank multiplication. In addition, or alternatively, the control dies 822 may be configured to perform rank multiplication. Embodiments of rank multiplication are described in greater detail in U.S. Patent Nos. 7,289,386 and 7,532,537, each of which are incorporated in their entirety by reference herein. In such embodiments, the register device 812 can generate additional chip select signals that are provided to the array dies 824. For instance, if the memory control hub 802 is configured to recognize a single array die 824 per memory package 820, but there exists four array dies 824 per memory package 820, the memory control hub 802 may not provide the correct number of chip select signals to access a specific memory location of the plurality of array dies 824 is memory package 820. Thus, to access the specific memory location, the register device 812 can determine the array die that includes the specific memory location to be accessed based on the command/address signals received from the memory control hub 802 and can generate the correct chip select signal to access the array die that includes the specific memory location. In certain embodiments, when the memory module 810 is operating in the second operation module as described above, the memory module 810 does not perform rank multiplication.

Terminology

[0109] Unless the context clearly requires otherwise, throughout the description and the claims, the words "comprise," "comprising," and the like are to be construed in an inclusive sense, as opposed to an exclusive or exhaustive sense; that is to say, in the sense of "including, but not limited to." The term "coupled" is used to refer to the connection between two elements, the term refers to two or more elements that may be either directly connected, or connected by way of one or more intermediate elements. Additionally, the words "herein," "above," "below," and words of similar import, when used in this application, shall refer to this application as a whole and not to any particular portions of this application. Where the context permits, words in the above Detailed Description using the singular or plural number may also include the plural or singular number respectively. The word "or" in reference to a list of two or more items covers all of the following interpretations of the word: any of the items in the list, all of the items in the list, and any combination of the items in the list.

[0110] The above detailed description of embodiments of the invention is not intended to be exhaustive or to limit the invention to the precise form disclosed above.

While specific embodiments of, and examples for, the invention are described above for illustrative purposes, various equivalent modifications are possible within the scope of the invention, as those skilled in the relevant art will recognize. For example, while processes or blocks are presented in a given order, alternative embodiments may perform routines having steps, or employ systems having blocks, in a different order, and some processes or blocks may be deleted, moved, added, subdivided, combined, and/or modified. Each of these processes or blocks may be implemented in a variety of different ways. Also, while processes or blocks are at times shown as being performed in series, these processes or blocks may instead be performed in parallel, or may be performed at different times.

[0111] The teachings of the invention provided herein can be applied to other systems, not necessarily the system described above. The elements and acts of the various embodiments described above can be combined to provide further embodiments.

[0112] Conditional language used herein, such as, among others, "can," "might," "may," "e.g.," and the like, unless specifically stated otherwise, or otherwise understood within the context as used, is generally intended to convey that certain embodiments include, while other embodiments do not include, certain features, elements and/or states. Thus, such conditional language is not generally intended to imply that features, elements and/or states are in any way required for one or more embodiments or that one or more embodiments necessarily include logic for deciding, with or without author input or prompting, whether these features, elements and/or states are included or are to be performed in any particular embodiment.

[0113] While certain embodiments of the inventions have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the disclosure. Indeed, the novel methods and systems described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the methods and systems described herein may be made without departing from the spirit of the disclosure. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the disclosure.

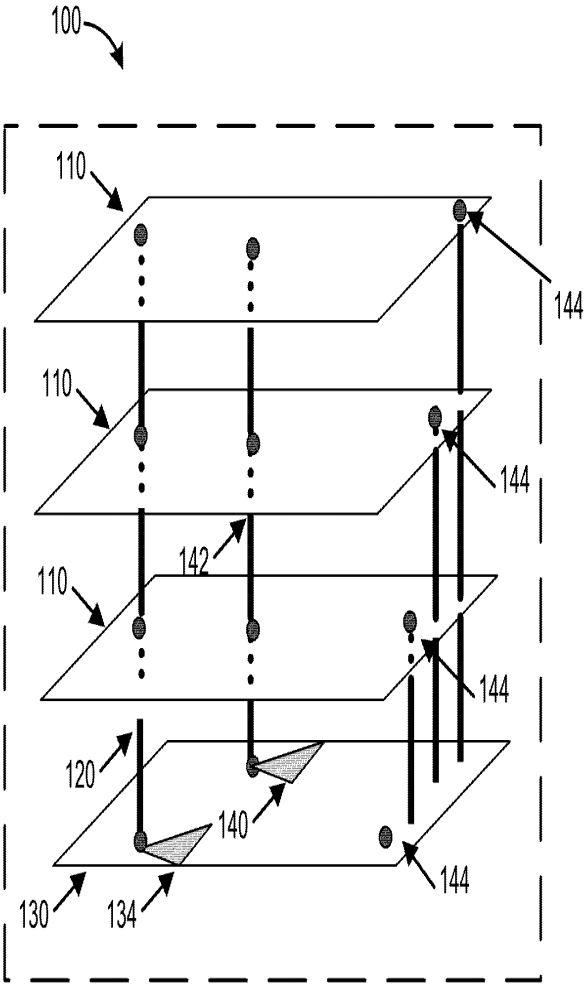
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FIG. 1A

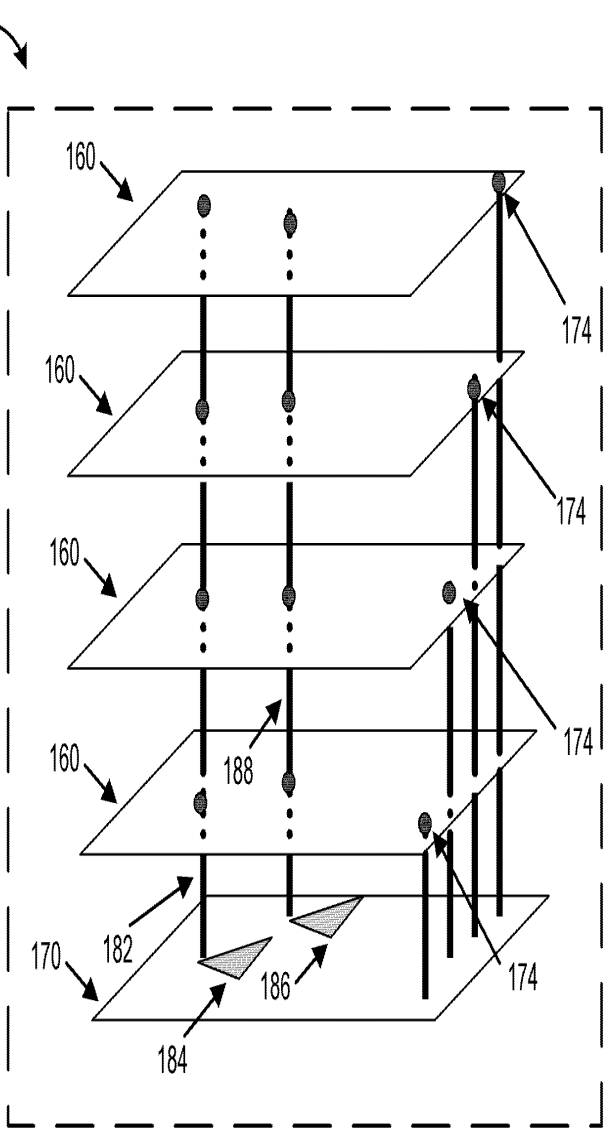
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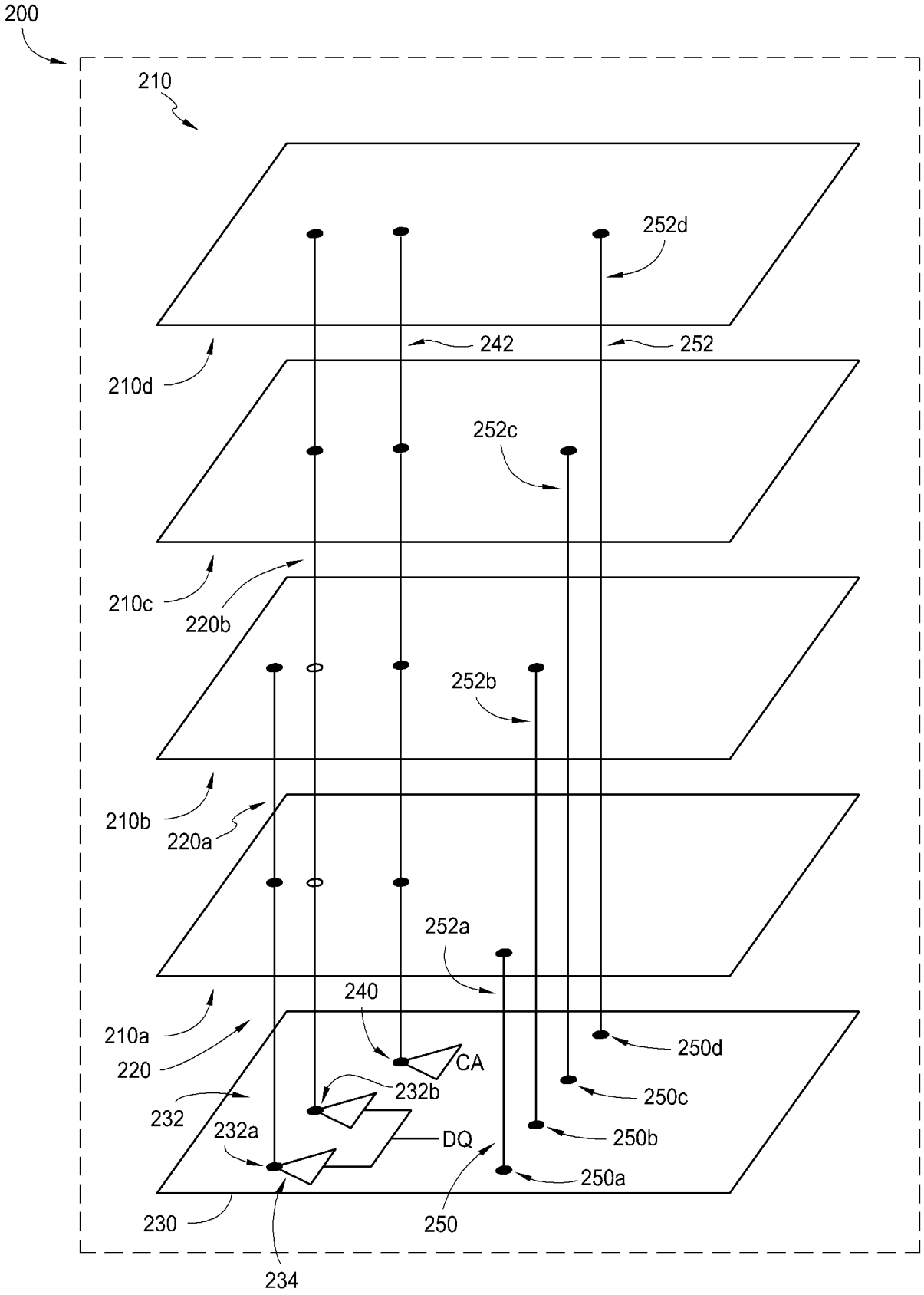
FIG. 1B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242
252
210d
252c
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FIG. 2

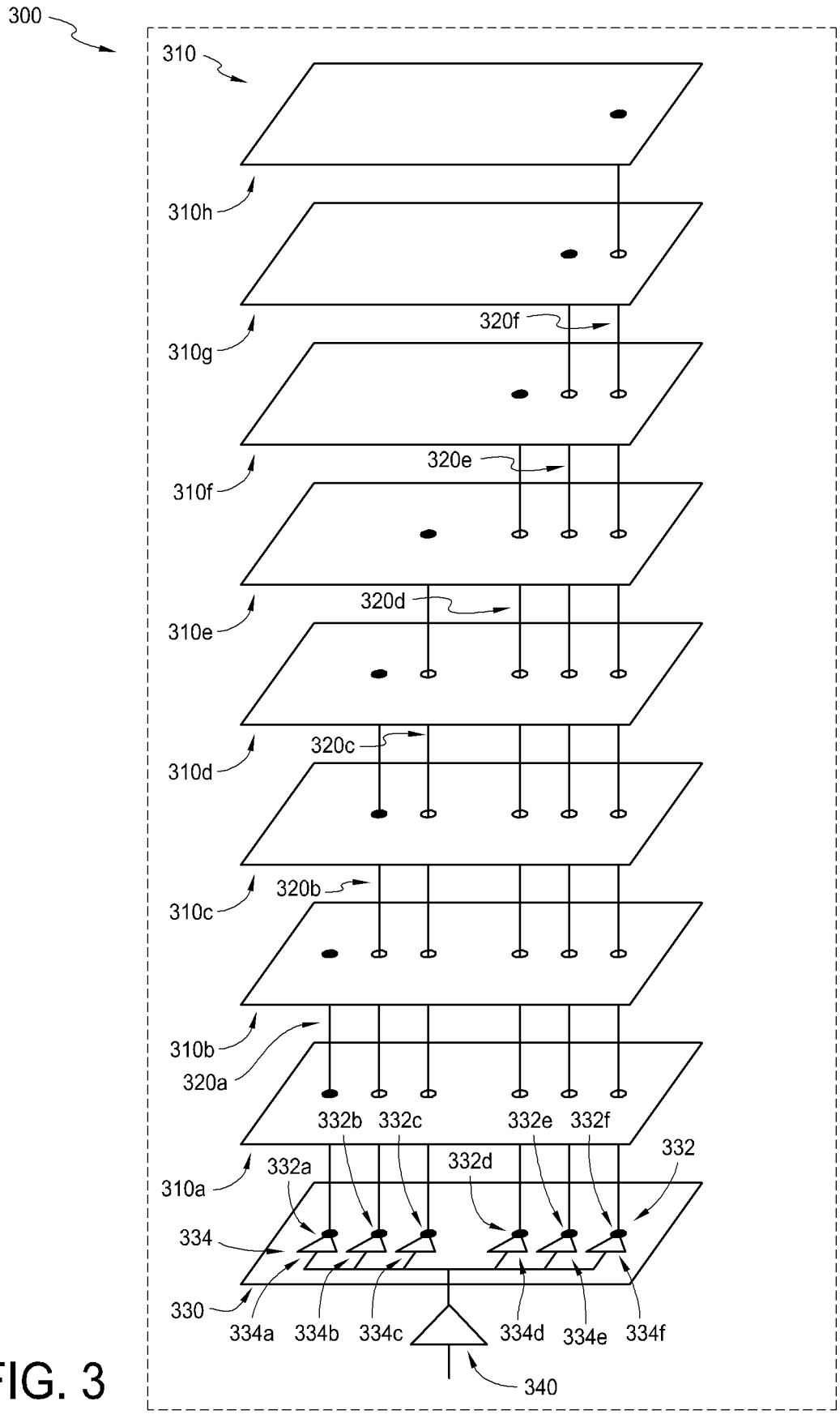
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FIG. 3

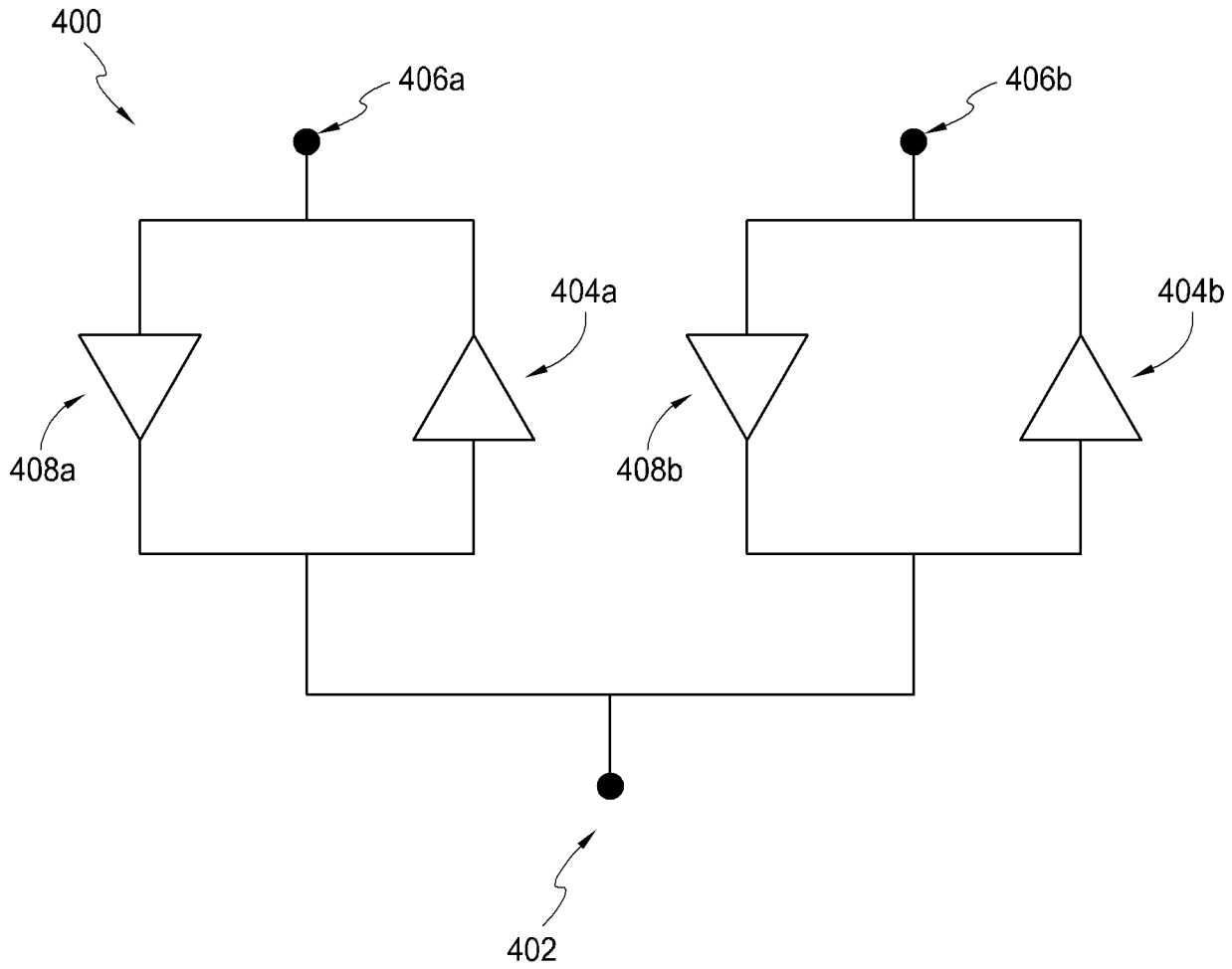
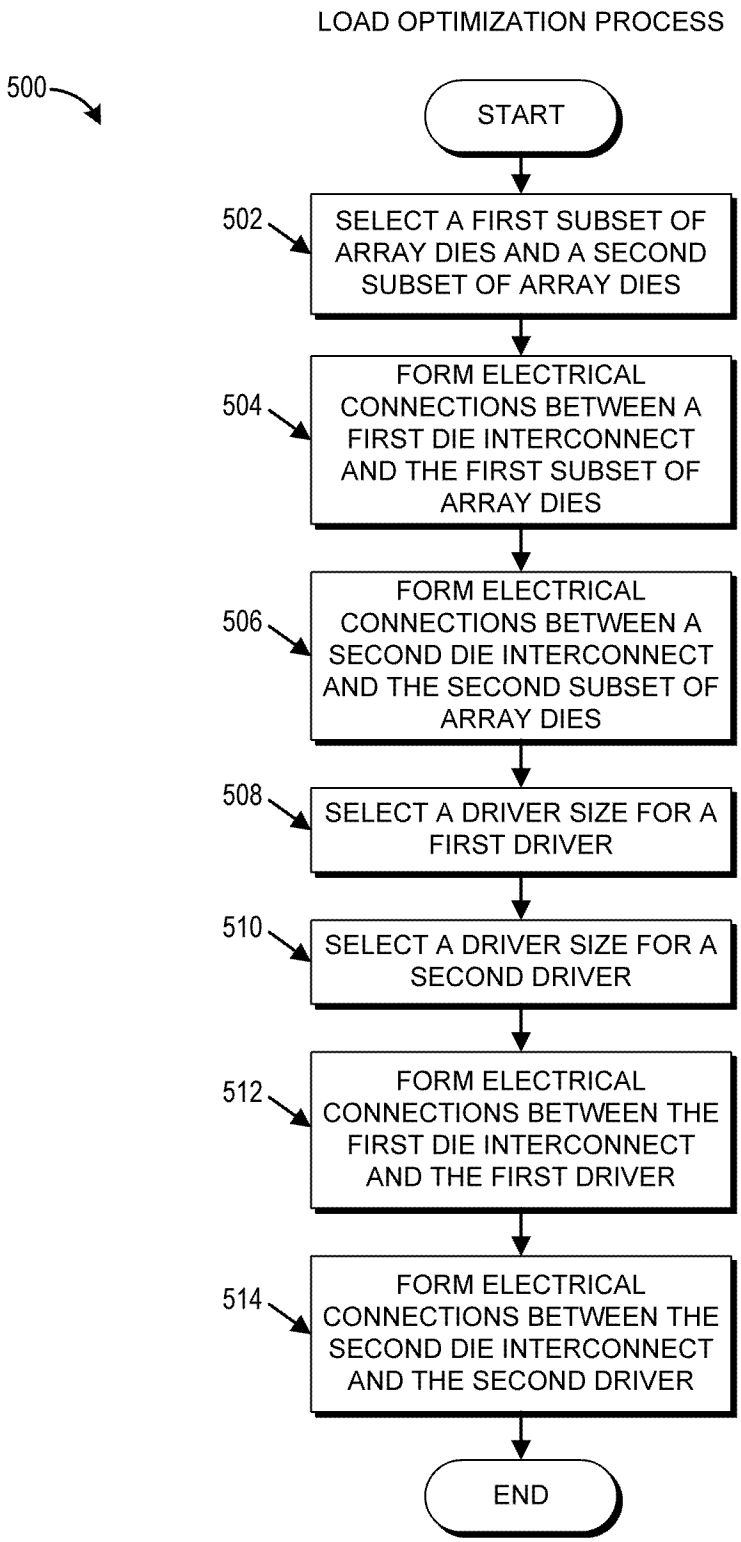


FIG. 4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START
502
SELECT A FIRST SUBSET OF ARRAY DIES AND A SECOND SUBSET OF ARRAY DIES
504
FORM ELECTRICAL CONNECTIONS BETWEEN A FIRST DIE INTERCONNECT AND THE FIRST SUBSET OF ARRAY DIES
506
FORM ELECTRICAL CONNECTIONS BETWEEN A SECOND DIE INTERCONNECT AND THE SECOND SUBSET OF ARRAY DIES
508
SELECT A DRIVER SIZE FOR A FIRST DRIVER
510
SELECT A DRIVER SIZE FOR A SECOND DRIVER
512
FORM ELECTRICAL CONNECTIONS BETWEEN THE FIRST DIE INTERCONNECT AND THE FIRST DRIVER
514
FORM ELECTRICAL CONNECTIONS BETWEEN THE SECOND DIE INTERCONNECT AND THE SECOND DRIVER
END

FIG. 5

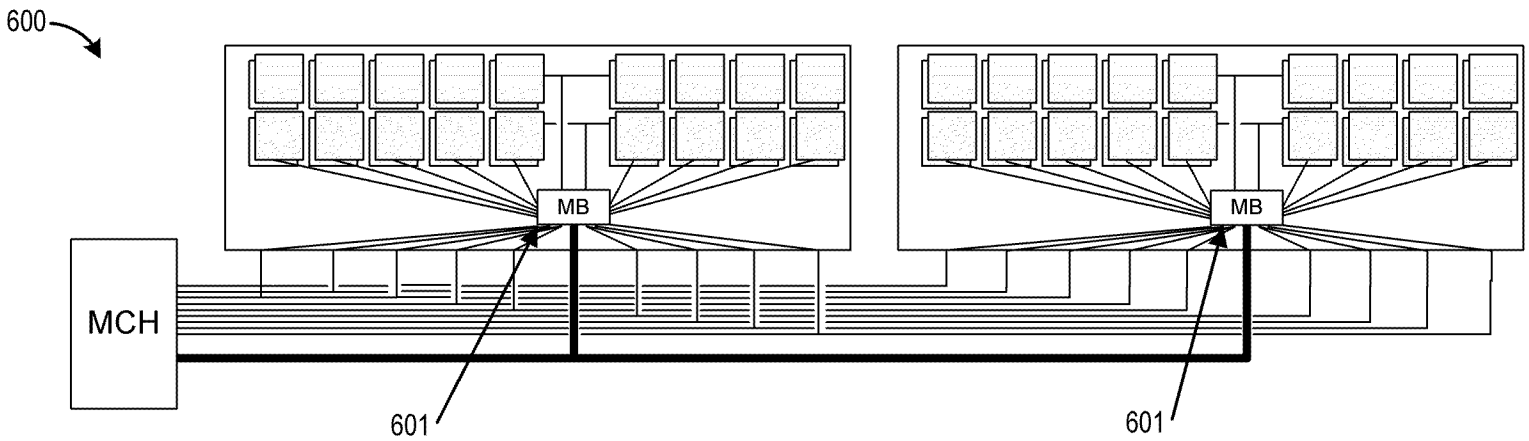


FIG. 6A

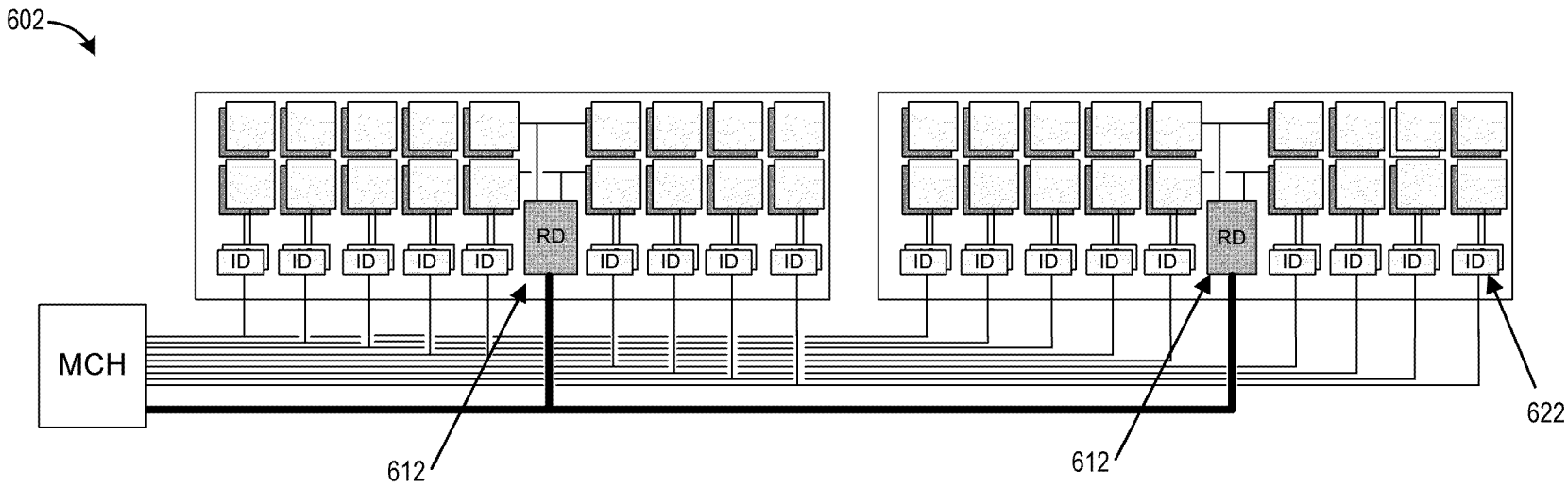
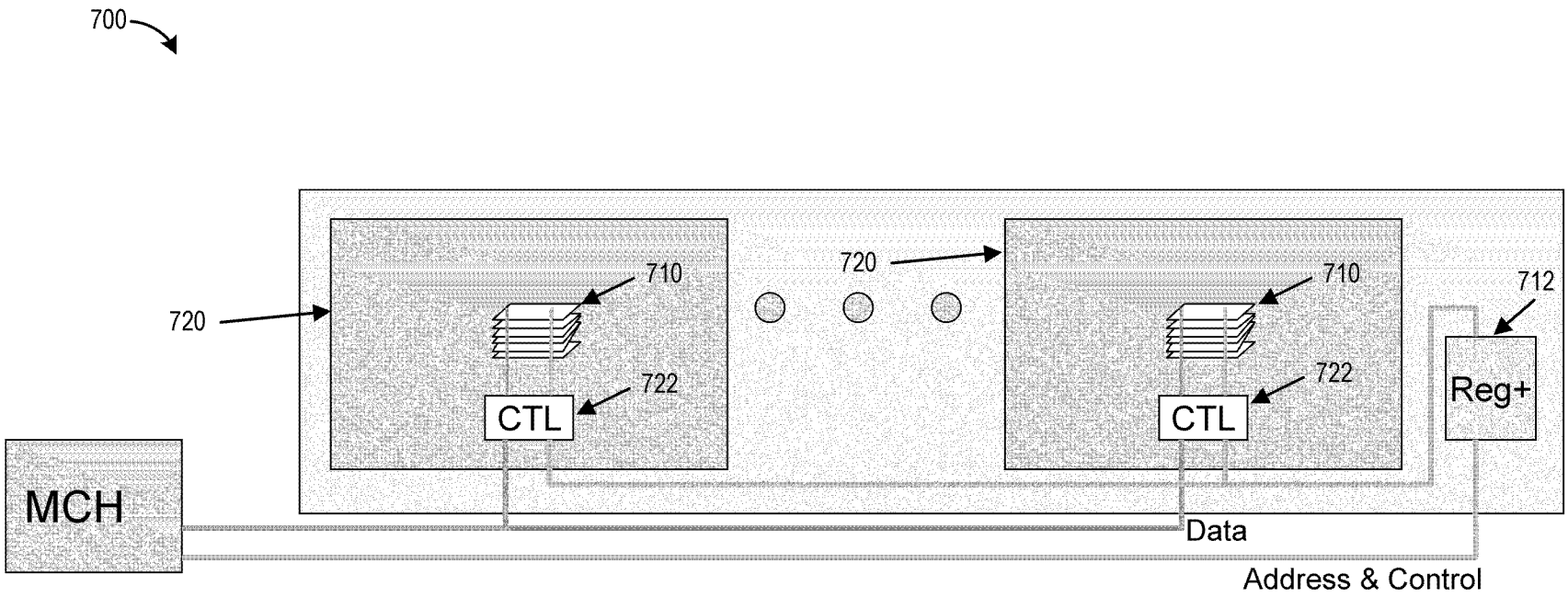


FIG. 6B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CTL
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722
CTL
712
Reg+
MCH
Data
Address & Control

FIG. 7

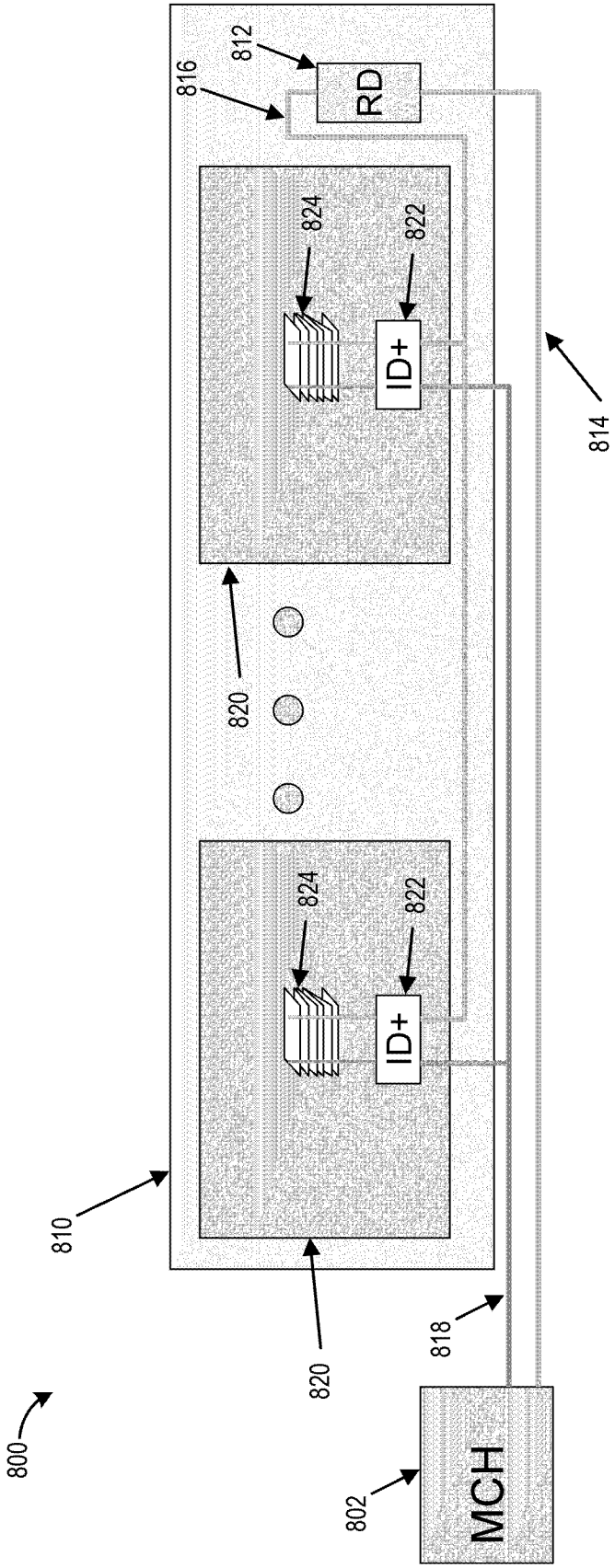

FIG. 8

Customer No. 79141
Attorney Docket No.: NETL.071C1

COMBINED DECLARATION AND ASSIGNMENT FOR UTILITY OR DESIGN APPLICATION

Title of Invention	MEMORY PACKAGE WITH OPTIMIZED DRIVER LOAD AND METHOD OF OPERATION

DECLARATION

As a below named inventor, I hereby declare that:

This declaration is directed to:

☐ The attached application, or

■ United States application or PCT international application number 14/337,168 filed on July 21, 2014.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

Note to Inventor: 37 C.F.R. § 1.63(c) states: "A person may not execute an oath or declaration for an application unless that person has reviewed and understands the contents of the application, including the claims, and is aware of the duty to disclose to the Office all information known to the person to be material to patentability as defined in § 1.56."

First Inventor (Legal Name): Hyun Lee

Signature: _____ Date: 3/2/2016

Electronic Acknowledgement Receipt

EFS ID:	36011443
Application Number:	16412308
International Application Number:	
Confirmation Number:	6765
Title of Invention:	MEMORY MODULE WITH BUFFERED MEMORY PACKAGES
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng/S. Olivier
Filer Authorized By:	Jamie Jie Zheng
Attorney Docket Number:	129980-5070-US01
Receipt Date:	14-MAY-2019
Filing Date:	
Time Stamp:	20:34:02
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal of New Application	129980_5070US01_TRANSMITTAL.pdf	145997 6ba56429e5d91622774eebb86a614b32199a6373	no	1

Warnings:

Information:					
2		129980_5070US01_STMT_POA.pdf	175719 24406ab6f0b3f6557eb56b6e3c21a10b433052be	yes	2
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Power of Attorney		2	2	
	Auth or Resc of Auth to Access Search Results		1	1	
Warnings:					
Information:					
3	Application Data Sheet	129980_5070US01_ADS.pdf	1823401 3feceb8e63e33d11e45deb1293b4f0aa1d2bcb5b	no	9
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4		129980_5070US01_APPLN.pdf	377259 888b5f564ab85e58e64693f488f7db8341f13b7a	yes	37
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	Document Description		**Start**	**End**	
	Abstract		37	37	
	Claims		36	36	
	Specification		1	35	
Warnings:					
Information:					
5	Drawings-only black and white line drawings	129980_5070US01_Drwgs.pdf	1267598 e858ac415d33dc16e51fb19a7d3c0033bbbbf5ef	no	8
Warnings:					
Information:					
6	Oath or Declaration filed	129980_5070US01_DECL.pdf	35819 c2e12b2f6b60d35840c19b3e3440800d1ddf0a47	no	1

Warnings:	
Information:	
Total Files Size (in bytes):	3825793

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number
16/412,308

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	300
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	660
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	760
TOTAL CLAIMS (37 CFR 1.16(i))	1 minus 20 =	*			OR	x 100 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1 minus 3 =	*				x 460 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1720

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
AMENDMENT A	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
AMENDMENT A	Application Size Fee (37 CFR 1.16(s))									
AMENDMENT A	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)		RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
AMENDMENT B	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
AMENDMENT B	Application Size Fee (37 CFR 1.16(s))									
AMENDMENT B	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

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Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/412,308	05/14/2019	Hyun Lee	129980-5070-US01

CONFIRMATION NO. 6765

FORMALITIES LETTER

79141
Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304

OC000000108394509

Date Mailed: 05/23/2019

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
- The application search fee must be submitted.
- The application examination fee must be submitted.
- Surcharge as set forth in 37 CFR 1.16(f) must be submitted.
  The surcharge is due for any one of:
  - late submission of the basic filing fee, search fee, or examination fee,
  - late submission of inventor's oath or declaration,
  - filing an application that does not contain at least one claim on filing, or
  - submission of an application filed by reference to a previously filed application.

SUMMARY OF FEES DUE:

The fee(s) required within **TWO MONTHS** from the date of this Notice to avoid abandonment is/are itemized below. No entity status discount is in effect. If applicant is qualified for small entity status, a written assertion of small entity status must be submitted to establish small entity status. (See 37 CFR 1.27). If applicant is qualified for micro entity status, an acceptable Certification of Micro Entity Status must be submitted to establish micro entity status. (See 37 CFR 1.29 and forms PTO/SB/15A and 15B.)

- $ **300** basic filing fee.
- $ **160** surcharge.
- $ **660** search fee.
- $ **760** examination fee.
- $(**0**) previous unapplied payment amount.
- $ **1880** TOTAL FEE BALANCE DUE.

Replies must be received in the USPTO within the set time period or must include a proper Certificate of Mailing or Transmission under 37 CFR 1.8 with a mailing or transmission date within the set time period. For more information and a suggested format, see Form PTO/SB/92 and MPEP 512.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web, including a copy of this Notice and selecting the document description "Applicant response to Pre-Exam Formalities Notice". https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html

For more information about EFS-Web please call the USPTO Electronic Business Center at 1-866-217-9197 or visit our website at http://www.uspto.gov/ebc.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/tlo/

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UNITED STATES DEPARTMENT OF COMMERCE
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Alexandria, Virginia 22313-1450
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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
16/412,308	05/14/2019	2811	0.00	129980-5070-US01	1	1

CONFIRMATION NO. 6765

FILING RECEIPT

OC000000108394508

79141
Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304

Date Mailed: 05/23/2019

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

Hyun Lee, Ladera Ranch, CA;

Applicant(s)

NETLIST, INC., Irvine, CA;

Power of Attorney: The patent practitioners associated with Customer Number 79141

Domestic Priority data as claimed by applicant

This application is a CON of 15/602,099 05/22/2017 PAT 10290328
which is a CON of 15/095,288 04/11/2016 PAT 9659601
which is a CON of 14/337,168 07/21/2014 PAT 9318160
which is a CON of 13/288,850 11/03/2011 PAT 8787060
which claims benefit of 61/409,893 11/03/2010

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 05/22/2019

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 16/412,308**

Projected Publication Date: To Be Determined - pending completion of Missing Parts

Non-Publication Request: No

Early Publication Request: No
Title

MEMORY MODULE WITH BUFFERED MEMORY PACKAGES

Preliminary Class

257

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific

countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop

technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

Electronically filed August 22, 2019

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun Lee	Confirmation No.:	6765
Serial No.:	16/412,308	Art Unit:	2811
Filed:	May 14, 2019	Examiner:	TBD
For:	Memory Module With Buffered Memory Packages	Attorney Docket No:	129980-5070-US01

RESPONSE TO THE NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

Mail Stop: MISSING PARTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Notice to File Missing Parts mailed May 23, 2019, enclosed is the Notice to File Missing Parts of Nonprovisional Application for the above-identified application. The fee for the late filing fees surcharge is estimated to be $160

Also enclosed please find a Fee Transmittal Form setting forth the calculation for the statutory basic filing, search and examination fees, together with the excess claim fees due in this matter. The fees calculated for the statutory basic filing, search and examination fees together with the excess claim fees and application size fee (if applicable) are estimated to be $1720.

The Commissioner is hereby authorized to charge any required fee(s) to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5070-US01).

Respectfully submitted,

Date: August 22, 2019

/ Jamie J. Zheng / 51,167

Jamie J. Zheng (Reg. No.)
MORGAN, LEWIS & BOCKIUS LLP
1400 Page Mill Road
Palo Alto, CA 94304
(650) 843-4000

129980-5070-US01
GEW/JZ

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/412,308	05/14/2019	Hyun Lee	129980-5070-US01

CONFIRMATION NO. 6765

79141
Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304

FORMALITIES LETTER

OC000000108394509

Date Mailed: 05/23/2019

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
- The application search fee must be submitted.
- The application examination fee must be submitted.
- Surcharge as set forth in 37 CFR 1.16(f) must be submitted.
  The surcharge is due for any one of:
  - late submission of the basic filing fee, search fee, or examination fee,
  - late submission of inventor's oath or declaration,
  - filing an application that does not contain at least one claim on filing, or
  - submission of an application filed by reference to a previously filed application.

SUMMARY OF FEES DUE:

The fee(s) required within **TWO MONTHS** from the date of this Notice to avoid abandonment is/are itemized below. No entity status discount is in effect. If applicant is qualified for small entity status, a written assertion of small entity status must be submitted to establish small entity status. (See 37 CFR 1.27). If applicant is qualified for micro entity status, an acceptable Certification of Micro Entity Status must be submitted to establish micro entity status. (See 37 CFR 1.29 and forms PTO/SB/15A and 15B.)

- $ **300** basic filing fee.
- $ **160** surcharge.
- $ **660** search fee.
- $ **760** examination fee.
- $(0) previous unapplied payment amount.
- $ **1880** TOTAL FEE BALANCE DUE.

DOCKETED
file missing parts
Due 23 JUL 2019
Final 23 DEC 2019
RECEIVED DOCKETING
MAY 23 2019
MORGAN LEWIS
PALO ALTO OFFICE

Replies must be received in the USPTO within the set time period or must include a proper Certificate of Mailing or Transmission under 37 CFR 1.8 with a mailing or transmission date within the set time period. For more information and a suggested format, see Form PTO/SB/92 and MPEP 512.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web, including a copy of this Notice and selecting the document description "Applicant response to Pre-Exam Formalities Notice". https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html

For more information about EFS-Web please call the USPTO Electronic Business Center at 1-866-217-9197 or visit our website at http://www.uspto.gov/ebc.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/tlo/

UTILITY PATENT APPLICATION FEE TRANSMITTAL (Only for new nonprovisional applications under 37 CFR § 1.53(b))	Attorney Docket No.	129980-5070-US01
	First Inventor	Hyun Lee
	Title	Memory Module With Buffered Memory Packages
	Electronically filed	August 22, 2019

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

BASIC FILING, SEARCH AND EXAMINATION FEES

Application Type	Filing Fees	Search Fees	Examination Fees	Fees Paid ($)
Utility	$ 300	$ 660	$ 760	$ 1720

EXCESS CLAIM FEES

Type	No. Filed	Less	Extra	Extra Rate ($)	Fee ($)
Total Claims	1	- 20	0	$ 100 each	0
Independent	1	- 3	0	$ 460 each	0
			Surcharge for late filing fee		160

APPLICATION SIZE FEE (Specification and Drawings)

Total Sheets	Extra Sheets	No. of each add'l 50 or fraction thereof	Fee ($)
45 x .75- 100	0 / 50	0 (round up to whole no.) x $400	0

Sub Total	1880
Applicant qualifies for the 50% Reduction for Independent Inventor, Nonprofit Organization or Small Business Concern minus electronic filing discount of $75	
TOTAL FILING FEE	**1880**

Please charge the total filing fee and any other additional fees to Morgan, Lewis & Bockius LLP Deposit Account 50-0310 (order no. 129980-5070-US01).

Respectfully submitted,

Date: August 22, 2019

/ Jamie J. Zheng /

Jamie J. Zheng — 51,167 (Reg. No.)

MORGAN, LEWIS & BOCKIUS LLP
1400 Page Mill Road
Palo Alto, CA 94304
(650) 843-4000

Electronic Patent Application Fee Transmittal

Application Number:	16412308
Filing Date:	14-May-2019
Title of Invention:	MEMORY MODULE WITH BUFFERED MEMORY PACKAGES
First Named Inventor/Applicant Name:	Hyun Lee
Filer:	Jamie Jie Zheng/S. Olivier
Attorney Docket Number:	129980-5070-US01

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY APPLICATION FILING	1011	1	300	300
UTILITY SEARCH FEE	1111	1	660	660
UTILITY EXAMINATION FEE	1311	1	760	760
Pages:				
Claims:				
Miscellaneous-Filing:				
LATE FILING FEE FOR OATH OR DECLARATION	1051	1	160	160
Petition:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Extension - 1 month with $0 paid	1251	1	200	200
Miscellaneous:				
		Total in USD ($)		**2080**

Electronic Acknowledgement Receipt

EFS ID:	36930416
Application Number:	16412308
International Application Number:	
Confirmation Number:	6765
Title of Invention:	MEMORY MODULE WITH BUFFERED MEMORY PACKAGES
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng/S. Olivier
Filer Authorized By:	Jamie Jie Zheng
Attorney Docket Number:	129980-5070-US01
Receipt Date:	20-AUG-2019
Filing Date:	14-MAY-2019
Time Stamp:	18:15:20
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$2080
RAM confirmation Number	E20198JI15481643
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		129980-5070US01_RES.pdf	785949 08973b901999834789a52b5d95ca4bd5df3f8cbe	yes	5

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Applicant Response to Pre-Exam Formalities Notice	1	4
	Fee Worksheet (SB06)	5	5

Warnings:

Information:

2	Fee Worksheet (SB06)	fee-info.pdf	39360 dba1e1742ba488d13dbc1c9a7279a6a3a9dca806	no	2

Warnings:

Information:

Total Files Size (in bytes):	825309

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed August 21, 2019	
				Application Number	16/412,308
				Filing Date	May 14, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2827
				Examiner Name	To be assigned
Sheet	1	of	14	Attorney Docket Number	129980-5070US01

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		2008/0296779 A1	12-04-2008	Matsui et al.	
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Examiner Signature		Date Considered	

DB2/ 36616000.1

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed August 21, 2019	
				Application Number	16/412,308
				Filing Date	May 14, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2827
				Examiner Name	To be assigned
Sheet	2	of	14	Attorney Docket Number	129980-5070US01

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Examiner Signature		Date Considered	

DB2/ 36616000.1

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FOREIGN PATENT DOCUMENTS

Examiner Initials	Cite No.	Foreign Patent Document Country Code – Number - Kind Code *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T
		WO 2010-138480	12/2/2010	Rambus Inc.		
		WO 2011-049710	4/28/2011	Rambus Inc.		

Examiner Signature		Date Considered	

DB2/ 36616000.1

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		EP1816570 A2	8/8/2007	Rambus, Inc.		
		JP10092169	10/4/1998	IBM		
		JP2000311485	10/13/2000	Fujitsu Ltd.		
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		JP2002184176	6/28/2002	NECTohoku Ltd.		
		JP2003007963	1/10/2003	Hitachi Ltd.et al.		
		JP2008046989	2/28/2008	Fujitsu Ltd		
		JP09237492	9/9/1997	Toshiba Corp.		
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		W099/30240				

NON PATENT LITERATURE DOCUMENTS

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				Art Unit	2827
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DB2/ 36616000.1

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				Art Unit	2827
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Sheet	6	of	14	Attorney Docket Number	129980-5070US01

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Sheet	10	of	14	Attorney Docket Number	129980-5070US01

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DB2/ 36616000.1

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DB2/ 36616000.1

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed August 21, 2019	
				Application Number	16/412,308
				Filing Date	May 14, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2827
				Examiner Name	To be assigned
Sheet	13	of	14	Attorney Docket Number	129980-5070US01

		U.S. District Court Northern District of California, Case No. 4.13-cn-05889-YGR, Netlist Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Joint Claim Construction and Prehearing Statement Pursuant to Patent L. T. 4-3, filed August 27, 2014, in 28 pages
		Excerpts from the Authoritative Dictionary of IEEE Standard Terms, Seventh Edition, Standards Information Network, IEEE Press (2000), pp. 349-411
		\Excerpts from the Authoritative Dictionary of IEEE Standard Terms, Seventh Edition, Standards Information Network, IEEE Press (2000), pp. 133-265
		Selected Entries in Oxford English Dictionary, Oxford University Press 2014, http://www.oed.com/view/Entry/175039?redirectedFrom=selectively#eid
		Web search results from the Oxford English Dictionary, Oxford University Press 2014, http://www.oed.com/search?searchType=dictionary&q=select&_searchBin=Search
		Inter Partes Review Case No. 2014-00883, Patent Owner Response, filed May 8, 2015
		Inter Partes Review Case No. 2014-00883, Petitioner Diablo Technologies, Inc.'s Reply to Patent Owner Netlist, Inc.'s Response, filed June 19, 2015
		Inter Partes Review Case No. 2014-00883, Petitioner's Request for Oral Argument, filed July 1, 2015
		Inter Partes Review Case No. 2014-00883, Patent Owner's Request for Oral Hearing, filed July 3, 2015
		Inter Partes Review Case No. 2014-00883, Order - Request for Oral Argument - 37 C.F.R. 42.70, filed July 10, 2015
		Inter Partes Review Case No. 2014-00883, Record of Oral Hearing, filed November 16, 2015
		Inter Partes Review Case No. 2014-00883, Final Written Decision - 35 USC 318 and 37 CFR 42.73, filed December 14, 2015
		Inter Partes Review Case No. 2014-00883, Netlist Inc.'s Notice of Appeal, filed February 10, 2016
		Inter Partes Review Case No. 2014-00883, Exhibit 1025, 'Professor Carl Sechen Deposition Transcript,' filed June 19,2015
		Inter Partes Review Case No. 2014-00883, Exhibit 1026, 'Dr. Srinivasan Jagannathan Supplemental Declaration,' filed June 19,2015
		Inter Partes Review Case No. 2014-01011, Patent Owner Response, filed May 8, 2015
		Inter Partes Review Case No. 2014-01011, Petitioner Diablo Technologies, Inc.'s Reply to Patent Owner Netlist, Inc.'s Response, filed June 19, 2015
		Inter Partes Review Case No. 2014-01011, Petitioner's Request for Oral Argument, filed July 1, 2015
		Inter Partes Review Case No. 2014-01011, Patent Owner's Request for Oral Hearing, filed July 3, 2015
		Inter Partes Review Case No. 2014-01011, Order - Request for Oral Argument - 37 C.F.R. 42.70, filed July 10, 2015

Examiner Signature		Date Considered	

DB2/ 36616000.1

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed August 21, 2019	
				Application Number	16/412,308
				Filing Date	May 14, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2827
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Sheet	14	of	14	Attorney Docket Number	129980-5070US01

		Inter Partes Review Case No. 2014-01011, Record of Oral Hearing, filed November 16, 2015
		Inter Partes Review Case No. 2014-01011, Final Written Decision - 35 USC 318 and 37 CFR 42.73, filed December 14, 2015
		Inter Partes Review Case No. 2014-01011, Netlist Inc.'s Notice of Appeal, filed February 10, 2016
		Inter Partes Review Case No. 2014-01011, Exhibit 1027, 'Professor Carl Sechen Deposition Transcript,' filed June 19,2015
		Inter Partes Review Case No. 2014-01011, Exhibit 1028, 'Dr. Srinivasan Jagannathan Supplemental Declaration,' filed June 19,2015

Examiner Signature		Date Considered	

Electronic Acknowledgement Receipt

EFS ID:	36944301
Application Number:	16412308
International Application Number:	
Confirmation Number:	6765
Title of Invention:	MEMORY MODULE WITH BUFFERED MEMORY PACKAGES
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng/Lamesha Robertson
Filer Authorized By:	Jamie Jie Zheng
Attorney Docket Number:	129980-5070-US01
Receipt Date:	21-AUG-2019
Filing Date:	14-MAY-2019
Time Stamp:	20:30:21
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		129980_5070US01_IDS.pdf	1610817 b1e3aee9567bb9a479c3a1def26bf6982e6ad920	yes	18

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Transmittal Letter	1	4
	Information Disclosure Statement (IDS) Form (SB08)	5	18
Warnings:			
Information:			
	Total Files Size (in bytes):	1610817	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronically filed August 21, 2019

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun Lee	Confirmation No.:	6765
Serial No.:	16/412,308	Art Unit:	2827
Filed:	May 14, 2019	Examiner:	To be assigned
For:	MEMORY MODULE WITH BUFFERED MEMORY PACKAGES	Attorney Docket No.:	129980-5070US01

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure provisions of 37 C.F.R. §1.56, there is hereby provided certain information which the Examiner may consider material to the examination of the subject U.S. patent application. It is requested that the Examiner make this information of record if it is deemed material to the examination of the application.

1. Enclosures accompanying this Information Disclosure Statement are:

1a. ☒ A list of all patents, publications, applications, or other information submitted for consideration by the office.

1b. A legible copy of:

☐ Each foreign patent;

☐ Each publication or that portion which caused it to be listed on the PTO-1449;

☐ For each cited pending U.S. application, the application specification including the claims, and any drawing of the application, or portion of the application which caused it to be listed on the PTO-1449 including any claims directed to that portion;

☐ all other information or portion which caused it to be listed on the PTO-1449.

1c. ☐ An English language copy of search report(s) from a counterpart foreign application or PCT International Search Report.

1d. ☐ Explanations of relevancy (ATTACHMENT 1(d), hereto) or English language abstracts of the non-English language publications.

2. ☒ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(b):

☐ Within three months of the filing date of a national application other than a continued prosecution application under §1.53(d);

☐ Within three months of the date of entry of the national stage as set forth in §1.491 in an international application;

☒ Before the mailing of the first Office action on the merits;

☐ Before the mailing of a first Office action after the filing of a request for continued examination under §1.114.

3. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(c) after the period specified in 37 C.F.R. §1.97(b), but before the mailing date of any of a final action under 37 C.F.R. §1.113, a notice of allowance under 37 C.F.R. §1.311 or an action that otherwise closes prosecution in the application.

(Check either Item 3a, 3b, 3c or 3d)

3a. ☐ The Certification Statement in Item 5 below is applicable. Accordingly, no fee is required.

3b. ☐ The $240 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

3c. ☐ The $120 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

3d. ☐ The $60 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

(Items 3b or 3c to be checked if any reference known for more than 3 months)

4. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(d) after the period specified in 37 C.F.R. §1.97(c), but on or before the date of payment of the issue fee.

(Check Item 4a, and 4b, 4c or 4d)

4a. ☐ The Certification Statement in Item 5 below is applicable.

4b. ☐ The $240 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

4c. ☐ The $120 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

4d. ☐ The $60 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

5. ☐ Certification Statement (applicable if Item 3a or Item 4a is checked)

(Check either Item 5a, 5b, 5c or 5d)

5a. ☐ In accordance with 37 C.F.R. §1.97(e)(1), it is certified that each item of information contained in this information disclosure statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement.

5b. ☐ In accordance with 37 C.F.R. §1.97(e)(2), it is certified that no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 C.F.R. §1.56(c) more than three months prior to the filing of this information disclosure statement.

5c. ☐ Each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

5d. ☐ Pursuant to 37 C.F.R. §1.704(d), each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

6. ☒ Copies of each cited U.S. patent and each U.S. patent application publication are not enclosed pursuant to the USPTO OG Notice dated 05 August 2003 waiving the requirement under 37 C.F.R. 1.98(a)(2)(i) for U.S. patent applications filed after June 30, 2003.

7. ☒ This application is a continuation application under 37 C.F.R. §1.53(b) or (d).

(Check appropriate Items 7a, 7b and/or 7c)

7a. ☐ A Petition to Withdraw from issue under 37 C.F.R. §1.313(b)(5) is concurrently filed herewith.

7b. ☒ Copies of publications listed on Form PTO-1449 from prior application Serial No. 15/602,099 filed on May 22, 2017, 15/095,288, filed on April 11, 2016, 14/337,168, filed on July 21, 2014, and 13/288,850, filed on November 3, 2011, of which this application claims priority under 35 U.S.C. §120, are not being submitted pursuant to 37 C.F.R. §1.98(d).

7c. ☐ Copies of the publications listed on the attached Form PTO-1449 that were not previously cited in prior application Serial No. , filed on , are provided herewith.

8. ☐ This is a Supplemental Information Disclosure Statement. (Check Item 8a)

8a. ☐ This Supplemental Information Disclosure Statement under 37 C.F.R. §1.97(f) supplements the Information Disclosure Statement filed on . A bona fide attempt was made to comply with 37 C.F.R. §1.98, but inadvertent omissions were made. These omissions have been corrected herein. Accordingly, additional time is requested so that this Supplemental Information Disclosure Statement can be considered as if properly filed on .

9. ☐ In accordance with 37 C.F.R. §1.98, a concise explanation of what is presently understood to be the relevance of each non-English language publication is:

(Check Item 9a, 9b, or 9c)

9a. ☐ satisfied because all non-English language publications were cited on the enclosed English language copy of the PCT International Search Report or the search report from a counterpart foreign application indicating the degree of relevance found by the foreign office.

9b. ☐ set forth in the application.

9c. ☐ enclosed as an attachment hereto.

10. ☒ The Commissioner is authorized to charge any additional fee required or credit any overpayment for this Information Disclosure Statement and/or Petition to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5070US01).

11. ☒ No admission is made that the information cited in this Statement is, or is considered to be, material to patentability nor a representation that a search has been made (other than a search report of a foreign counterpart application or PCT International Search Report if submitted herewith). 37 C.F.R. §§1.97(g) and (h).

Respectfully submitted,

Date: August 21, 2019

Jamie Zheng 51,167
(Reg. No.)
MORGAN, LEWIS & BOCKIUS LLP
1400 Page Mill Road
Palo Alto, CA 94304
(650) 843-4000

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
16/412,308	05/14/2019	2811	1880	129980-5070-US01	1	1

CONFIRMATION NO. 6765

UPDATED FILING RECEIPT

OC000000110579464

79141
Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304

Date Mailed: 08/22/2019

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

Hyun Lee, Ladera Ranch, CA;

Applicant(s)

NETLIST, INC., Irvine, CA;

Power of Attorney: The patent practitioners associated with Customer Number 79141

Domestic Priority data as claimed by applicant

This application is a CON of 15/602,099 05/22/2017 PAT 10290328
which is a CON of 15/095,288 04/11/2016 PAT 9659601
which is a CON of 14/337,168 07/21/2014 PAT 9318160
which is a CON of 13/288,850 11/03/2011 PAT 8787060
which claims benefit of 61/409,893 11/03/2010

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 05/22/2019

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 16/412,308**

Projected Publication Date: 11/28/2019

Non-Publication Request: No

Early Publication Request: No
Title

MEMORY MODULE WITH BUFFERED MEMORY PACKAGES

Preliminary Class

257

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific

countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop

technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number
16/412,308

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	300
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	660
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	760
TOTAL CLAIMS (37 CFR 1.16(i))	1 minus 20 =	*			OR	x 100 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1 minus 3 =	*				x 460 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1720

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
AMENDMENT A	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
AMENDMENT A	Application Size Fee (37 CFR 1.16(s))									
AMENDMENT A	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
AMENDMENT B	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
AMENDMENT B	Application Size Fee (37 CFR 1.16(s))									
AMENDMENT B	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/412,308	05/14/2019	Hyun Lee	129980-5070-US01	6765

79141 7590 10/03/2019
Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304

EXAMINER
HOANG, HUAN

ART UNIT	PAPER NUMBER
2827	

NOTIFICATION DATE	DELIVERY MODE
10/03/2019	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

padocketingdepartment@morganlewis.com
vskliba@morganlewis.com

Office Action Summary	Application No. 16/412,308	Applicant(s) Lee, Hyun	
	Examiner HUAN HOANG	Art Unit 2827	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 14 May 2019.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☑ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 14 May 2019 is/are: a)☑ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☑ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

DETAILED ACTION

Notice of Pre-AIA or AIA Status

1. The present application is being examined under the pre-AIA first to invent provisions.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112(a):

> (a) IN GENERAL.—The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor or joint inventor of carrying out the invention.

The following is a quotation of the first paragraph of pre-AIA 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claim 1 is rejected under 35 U.S.C. 112(a) or 35 U.S.C. 112 (pre-AIA), first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor or a joint inventor, or for pre-AIA the inventor(s), at the time the application was filed, had possession of the claimed invention.

The limitation “a printed circuit board” recited in claim 1, line 3 is not disclosed in the specification nor shown in the drawings.

Double Patenting

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on nonstatutory double patenting provided the reference application or patent either is shown to be commonly owned with the examined application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. See MPEP § 717.02 for applications subject to examination under the first inventor to file provisions of the AIA as explained in MPEP § 2159. See MPEP §§ 706.02(l)(1) - 706.02(l)(3) for applications not subject to examination under the first inventor to file

provisions of the AIA. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO Internet website contains terminal disclaimer forms which may be used. Please visit www.uspto.gov/patent/patents-forms. The filing date of the application in which the form is filed determines what form (e.g., PTO/SB/25, PTO/SB/26, PTO/AIA/25, or PTO/AIA/26) should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp.

5. Claim 1 is rejected on the ground of nonstatutory double patenting as being unpatentable over claims 29 and 30 of U.S. Patent No. 8,787,060. Although the claims at issue are not identical, they are not patentably distinct from each other because it would have been obvious to one of ordinary skill in the art to recognize that the module of claim 1 and the module of claims 29 and 30 of the patent are identical in structure; therefore, the differences between claim 1 and claims 29 and 30 of the patent are only the functional limitations.

Regarding claim 1: Claim 29 of the patent recites a memory module operable in a computer system to communicate with a system memory controller via a command/address bus and a data bus, comprising:

a printed circuit board (it is inherent that the memory module having the elements is mounted on a printed circuit board);

a register device (claim 29, line 3) mounted on the printed circuit board and configured to receive input command/address signals from the system memory controller via the command/address bus and to output control signals in response to the input command/address signals, the control signals including chip-select signals (claim 30); and

a plurality of DRAM packages (claim 29, line 6) mounted on the printed circuit board, each respective DRAM package comprising:

control terminals (claim 29, lines 9-11) coupled to the register device;

data terminals (claim 29, line 8) coupled to a respective section of the data bus;

stacked array dies claim 29, line 12);

a control die (claim 29, line 23) including data signal conduits coupled to the data terminals and control signal conduits coupled to the control terminals, the control signal conduits including chip-select conduits for receiving the chip select signals and providing respective ones of the chip select signals to respective ones of the stacked array dies; and

die interconnects (claim 29, line 15-16) including first die interconnects coupled to the data signal conduits and second die interconnects coupled to the control signal conduits, each of at least a subset of the first die interconnects is coupled to at least two of the stacked array dies; and

wherein the control die is configured to control the data signal conduits in accordance with the control signals to enable the each respective DRAM package to communicate a respective set of bits of one or more data signals between a selected die among the stacked dies and the data terminals, the selected die having

received one of the chip select signals that is different from any of the other ones of the chip select signals (functional limitations).

6. Claim 1 is rejected on the ground of nonstatutory double patenting as being unpatentable over claims 10 and 15 of U.S. Patent No.9,318,160 . Although the claims at issue are not identical, they are not patentably distinct from each other because it would have been obvious to one of ordinary skill in the art to recognize that the module of claim 1 and the module of claims 10 and 15 of the patent are identical in structure; therefore, the differences between claim 1 and claims 10 and 15 of the patent are only the functional limitations.

7. Claim 1 is rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1 and 5 of U.S. Patent No. 9,659,601. Although the claims at issue are not identical, they are not patentably distinct from each other because it would have been obvious to one of ordinary skill in the art to recognize that the module of claim 1 and the module of claims 1 and 5 of the patent are identical in structure; therefore, the differences between claim 1 and claims 1 and 5 of the patent are only the functional limitations.

8. Claim 1 is rejected on the ground of nonstatutory double patenting as being unpatentable over claim 1 of U.S. Patent No. 10,290,328. Although the claims at issue are not identical, they are not patentably distinct from each other because it would have been obvious to one of ordinary skill in the art to recognize that the module of claim 1 and the module of claim 1 of the patent are identical in structure; therefore, the differences between claim 1 of the instant application and claim 1 of the patent are only the functional limitations.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to HUAN HOANG whose telephone number is (571)272-1779. The examiner can normally be reached on 7:30AM-4:00PM M-F.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, AMIR ZARABIAN can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/HUAN HOANG/
Primary Examiner, Art Unit 2827

Notice of References Cited	Application/Control No. 16/412,308	Applicant(s)/Patent Under Reexamination Lee, Hyun	
	Examiner HUAN HOANG	Art Unit 2827	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-10290328-B2	05-2019	Lee; Hyun	G11C5/06	1/1
	B					
	C					
	D					
	E					
	F					
	G					
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	K					
	L					
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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/412,308	Lee, Hyun
	Examiner	**Art Unit**
	HUAN HOANG	2827

CPC - Searched*		
Symbol	**Date**	**Examiner**
G11C 5/066, G11C 5/06, G11C 7/1057, G11C 7/1094, G11C 7/12	09/29/2019	HH

CPC Combination Sets - Searched*		
Symbol	**Date**	**Examiner**

US Classification - Searched*			
Class	**Subclass**	**Date**	**Examiner**
365	63	09/29/2019	HH

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	**Date**	**Examiner**
EAST (text search)	09/29/2019	HH
Assignee and Inventor search	09/29/2019	HH

Interference Search			
US Class/CPC Symbol	**US Subclass/CPC Group**	**Date**	**Examiner**

/HUAN HOANG/ Primary Examiner, Art Unit 2827	

Petitioners
Ex. 1009, p. 113

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/412,308	Lee, Hyun
	Examiner	**Art Unit**
	HUAN HOANG	2827

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/29/2019								
	1	✓								

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed August 21, 2019	
				Application Number	16/412,308
				Filing Date	May 14, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2827
				Examiner Name	To be assigned
Sheet	1	of	14	Attorney Docket Number	129980-5070US01

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Examiner Signature		Date Considered	

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				Art Unit	2827
				Examiner Name	To be assigned
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				Examiner Name	To be assigned
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Examiner Signature		Date Considered	

DB2/ 36616000.1

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.L./

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				First Named Inventor	Hyun Lee
				Art Unit	2827
				Examiner Name	To be assigned
Sheet	4	of	14	Attorney Docket Number	129980-5070US01

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NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
		U.S. Application No. 12/422,912, (Attorney Docket No. NETL044A)
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Sheet	6	of	14	Attorney Docket Number	129980-5070US01

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Sheet	7	of	14	Attorney Docket Number	129980-5070US01

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Sheet	8	of	14	Attorney Docket Number	129980-5070US01

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Sheet	11	of	14	Attorney Docket Number	129980-5070US01

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Sheet	12	of	14	Attorney Docket Number	129980-5070US01

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		Microsoft Computer Dictionary, Fifth Edition, Microsoft Press, p. 334, 2002
		Jacob, Bruce, et al. "Memory Systems - Cache, DRAM, Disk," Elsevier Inc. 2008, Chapters 7 and 10

Examiner Signature		Date Considered	

DB2/ 36616000.1

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.H./

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed August 21, 2019	
				Application Number	16/412,308
				Filing Date	May 14, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2827
				Examiner Name	To be assigned
Sheet	13	of	14	Attorney Docket Number	129980-5070US01

		U.S. District Court Northern District of California, Case No. 4.13-cn-05889-YGR, Netlist Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Joint Claim Construction and Prehearing Statement Pursuant to Patent L. T. 4-3, filed August 27, 2014, in 28 pages
		Excerpts from the Authoritative Dictionary of IEEE Standard Terms, Seventh Edition, Standards Information Network, IEEE Press (2000), pp. 349-411
		\Excerpts from the Authoritative Dictionary of IEEE Standard Terms, Seventh Edition, Standards Information Network, IEEE Press (2000), pp. 133-265
		Selected Entries in Oxford English Dictionary, Oxford University Press 2014, http://www.oed.com/view/Entry/175039?redirectedFrom=selectively#eid
		Web search results from the Oxford English Dictionary, Oxford University Press 2014, http://www.oed.com/search?searchType=dictionary&q=select& _searchBin=Search
		Inter Partes Review Case No. 2014-00883, Patent Owner Response, filed May 8, 2015
		Inter Partes Review Case No. 2014-00883, Petitioner Diablo Technologies, Inc.'s Reply to Patent Owner Netlist, Inc.'s Response, filed June 19, 2015
		Inter Partes Review Case No. 2014-00883, Petitioner's Request for Oral Argument, filed July 1, 2015
		Inter Partes Review Case No. 2014-00883, Patent Owner's Request for Oral Hearing, filed July 3, 2015
		Inter Partes Review Case No. 2014-00883, Order - Request for Oral Argument - 37 C.F.R. 42.70, filed July 10, 2015
		Inter Partes Review Case No. 2014-00883, Record of Oral Hearing, filed November 16, 2015
		Inter Partes Review Case No. 2014-00883, Final Written Decision - 35 USC 318 and 37 CFR 42.73, filed December 14, 2015
		Inter Partes Review Case No. 2014-00883, Netlist Inc.'s Notice of Appeal, filed February 10, 2016
		Inter Partes Review Case No. 2014-00883, Exhibit 1025, 'Professor Carl Sechen Deposition Transcript,' filed June 19,2015
		Inter Partes Review Case No. 2014-00883, Exhibit 1026, 'Dr. Srinivasan Jagannathan Supplemental Declaration,' filed June 19,2015
		Inter Partes Review Case No. 2014-01011, Patent Owner Response, filed May 8, 2015
		Inter Partes Review Case No. 2014-01011, Petitioner Diablo Technologies, Inc.'s Reply to Patent Owner Netlist, Inc.'s Response, filed June 19, 2015
		Inter Partes Review Case No. 2014-01011, Petitioner's Request for Oral Argument, filed July 1, 2015
		Inter Partes Review Case No. 2014-01011, Patent Owner's Request for Oral Hearing, filed July 3, 2015
		Inter Partes Review Case No. 2014-01011, Order - Request for Oral Argument - 37 C.F.R. 42.70, filed July 10, 2015

Examiner Signature		Date Considered	

DB2/ 36616000.1

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.H/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed August 21, 2019	
				Application Number	16/412,308
				Filing Date	May 14, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2827
				Examiner Name	To be assigned
Sheet	14	of	14	Attorney Docket Number	129980-5070US01

		Inter Partes Review Case No. 2014-01011, Record of Oral Hearing, filed November 16, 2015
		Inter Partes Review Case No. 2014-01011, Final Written Decision - 35 USC 318 and 37 CFR 42.73, filed December 14, 2015
		Inter Partes Review Case No. 2014-01011, Netlist Inc.'s Notice of Appeal, filed February 10, 2016
		Inter Partes Review Case No. 2014-01011, Exhibit 1027, 'Professor Carl Sechen Deposition Transcript,' filed June 19,2015
		Inter Partes Review Case No. 2014-01011, Exhibit 1028, 'Dr. Srinivasan Jagannathan Supplemental Declaration,' filed June 19,2015

Examiner Signature	/HUAN HOANG/	Date Considered	09/29/2019

DB2/ 36616000.1

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.H/

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	31848	(G11C5/066 or G11C7/1057 or G11C7/12 or G11C7/1084 or G11C5/06).cpc. 365/63,063.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/29 15:23
L2	1898	1 and (printed adj circuit adj board pcb)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/29 15:24
L3	804	2 and register	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/29 15:24
L4	37	3 and (dram dynamic adj (random ram)) adj3 package	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/29 15:25
L5	13	stacked adj array adj dies	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/29 15:26
L6	0	4 and 5	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/29 15:52
L7	3268	1 and register and (dram dynamic adj (random ram))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/29 17:52
L8	8	7 and stacked adj array adj die	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/29 17:53
L9	222	7 and stack$3 adj3 die	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/29 17:53
L10	8	9 and control$4 with die with conduit	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/29 17:54
L11	70	9 and chip adj select$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/29 17:54
L13	50	11 and control$4 with die	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/29 17:55

L14	25	13 and select$3 with die with chip adj select	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/29 17:56
L15	2301872	netlist.as. lee.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/29 17:57
L16	63	15 and register and (dram dynamic adj (random ram)) adj3 package	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/29 17:57
L17	16	16 and stack$3 with die	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/29 17:58
L18	14	17 and interconnect$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/29 17:58
L19	9	17 and interconnect$3 and conduit	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/29 17:58

EAST Search History (Interference)

< This search history is empty>

9/ 29/ 2019 5:59:41 PM

UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/412,308	05/14/2019	Hyun Lee	129980-5070-US01

CONFIRMATION NO. 6765

PUBLICATION NOTICE

OC000000112994969

79141
Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304

Title:MEMORY MODULE WITH BUFFERED MEMORY PACKAGES

Publication No.US-2019-0362758-A1
Publication Date:11/28/2019

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Public Records Division. The Public Records Division can be reached by telephone at (571) 272-3150 or (800) 972-6382, by facsimile at (571) 273-3250, by mail addressed to the United States Patent and Trademark Office, Public Records Division, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently https://portal.uspto.gov/pair/PublicPair. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

Electronically filed March 3, 2020

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun Lee et al.	Confirmation No.:	6765
Serial No.:	16/412,308	Art Unit:	2827
Filed:	May 14, 2019	Examiner:	Hoang, Huan
For:	*Memory Module With Buffered Memory Packages*	Attorney Docket No.:	129980-5070-US01
		Date: March 3, 2020	

RESPONSE TO OFFICE ACTION

Mail Stop: Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The enclosed Amendment is in response to the Office Action dated October 3, 2019 for the above identified patent application.

Petition for Extension of Time under 37 CFR 1.136. It is respectfully requested that the time for response to the Office Action dated October 3, 2019 be extended for a period of two (2) months from January 3, 2020 to March 3, 2020.

The Commissioner is hereby authorized to charge any required fee(s) to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5070-US01).

Petitioners
Ex. 1009, p. 132

McKesson Statement

In view of *McKesson Information Solutions v. Bridge Medical* (Fed. Cir. 2007), Applicant wishes to inform the Examiner that the prosecution history of the following US Patent Application(s) may contain information relevant to the pending application:

(1) U.S. Application Serial No. 15/470,856, filed March 27, 2017.

(2) U.S. Application Serial No. 13/970.606, filed April 20, 2013. This application issued as U.S. Patent No. 9,606,907.

The Examiner is encouraged to review the art made of record, office action(s) and the notice(s) of allowance, if any, in the above-mentioned application(s), all of which are available on PAIR.

Petitioners
Ex. 1009, p. 133

Amendments to the Claims

The following listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Cancelled)

2. (New) A memory module operable in a computer system to communicate with a system memory controller via a command/address bus and a data bus, comprising:

a register device configurable to receive input command/address signals from the system memory controller via the command/address bus and to output control signals in response to the input command/address signals, the control signals including buffered command/address signals and data path control signals; and

a plurality of DRAM packages, each respective DRAM package comprising:

terminals including control terminals coupled to the register device and data terminals to be coupled to a respective section of the data bus, the control terminals including first control terminals and second control terminals;

stacked array dies; and

a control die coupled between the stacked array dies and the terminals of the respective DRAM package, the control die including data buffers and a data path control circuit; and

wherein the control die is configurable to:

receive the buffered command/address signals via the first control terminals and the data path control signals via the second control terminals;

pass at least some of the buffered command/address signals through the control die to the stacked array dies, the buffered command/address signals including chip-select signals that are provided to respective array dies of the stacked array dies; and

control the data buffers in response to the data path control signals to buffer data signals communicated between a selected array die of the stacked array dies and the respective section of the data bus, the selected array die having received one of the chip select signals that is different from any of the other ones of the chip select signals.

Petitioners
Ex. 1009, p. 134

3. (New) The memory module of claim 2, wherein the register device is configurable to decode the input command/address signals and to generate the data path control signals in accordance with the input command/address signals.

4. (New) The memory module of claim 2, wherein the data buffers are configurable to selectively isolate one or more array dies of the stacked array dies.

5. (New) The memory module of claim 2, wherein the control die does not secondarily buffer the buffered command/address signals.

6. (New) The memory module of claim 2, wherein the data path control circuit is configurable to control a command/address time slot for the buffered command/address signals passing through the control die.

7. (New) The memory module of claim 2, wherein the data path control circuit is configurable to control a data bus time slot for the data signals.

8. (New) The memory module of claim 2, wherein the buffered command/address signals include more chip select signals than the input command/address signals.

9. (New) The memory module of claim 2, further comprising die interconnects including first die interconnects coupled to the data buffers and second die interconnects coupled to the control terminals, each of the first die interconnects being coupled to one or more of the stacked array dies.

10. (New) The memory module of claim 9, wherein the data buffers include drivers coupled to respective ones of the first die interconnects, the drivers including a first driver coupled to one or more first array dies via a first die interconnect and a second driver and coupled to one or more second array dies via a second die interconnect, the first driver having a first driver size corresponding to a first capacitive load associated with the one or more first array dies and the first die interconnect, the second driver having a second driver size corresponding to a second capacitive load associated with the one or more second array dies and the second die interconnect.

Petitioners
Ex. 1009, p. 135

11. (New) A memory module operable in a computer system to communicate with a system memory controller via a command/address bus and a data bus, comprising:

a register device configurable to receive input command/address signals from the system memory controller via the command/address bus, to buffer the input command/address signals, and to output control signals in response to the input command/address signals, the control signals including buffered command/address signals; and

a plurality of DRAM packages, each respective DRAM package comprising:

terminals including control terminals coupled to the register device and data terminals to be coupled to a respective section of the data bus, the control terminals including first control terminals and second control terminals;

stacked array dies; and

a control die coupled between the stacked array dies and the terminals of the respective DRAM package, the control die including data buffers and a data path control circuit; and

wherein the memory module is operable in any one of a plurality of modes including a first mode and a second mode;

wherein, during the first mode, the register device is configurable to generate data path control signals in response to receiving the input command/address signals, the control signals further include the data path control signals, and the control die is configurable to:

receive the buffered command/address signals via the first control terminals and the data path control signals via the second control terminals; and

pass at least some of the buffered command/address signals through the control die to the stacked array dies, the buffered command/address signals including chip-select signals that are provided to respective array dies of the stacked array dies;

wherein, during the second mode, the control die is configurable to:

receive the buffered command/address signals via the first control terminals;

generate data path control signals in response to the buffered command/address signals; and

provide secondarily buffered command/address signals to the stacked array dies, the secondarily buffered command/address signals including chip-select signals that are provided to respective array dies of the stacked array dies; and

Petitioners
Ex. 1009, p. 136

wherein the control die is further configured to control the data buffers in response to the data path control circuit to buffer data signals communicated between a selected array die of the stacked array dies and the respective section of the data bus, the selected array die having received one of the chip select signals that is different from any of the other ones of the chip select signals.

12. (New) The memory module of claim 11, wherein, during the second mode, the control die is configurable to generate data path control signals after decoding the buffered command/address signals.

13. (New) The memory module of claim 12, wherein the secondarily buffered command/address signals include more chip select signals than the buffered command/address signals.

14. (New) The memory module of claim 11, wherein the data buffers are configurable to selectively isolate one or more array dies of the stacked array dies.

15. (New) The memory module of claim 11, wherein, during the first mode, the control die does not buffer at least some of the buffered command/address signals.

16. (New) The memory module of claim 11, wherein the data path control circuit is configurable to control a command/address time slot for the buffered command/address signals passing through the control die.

17. (New) The memory module of claim 11, wherein the data path control circuit is configurable to control a data bus time slot for the data signals.

18. (New) The memory module of claim 11, further comprising die interconnects including first die interconnects coupled to the data buffers and second die interconnects coupled to the control terminals, each of the first die interconnects being coupled to one or more of the stacked array dies.

19. (New) The memory module of claim 11, wherein the data buffers include drivers coupled to respective ones of the first die interconnects, the drivers including a first driver coupled to one

Petitioners
Ex. 1009, p. 137

or more first array dies via a first die interconnect and a second driver and coupled to one or more second array dies via a second die interconnect, the first driver having a first driver size corresponding to a first capacitive load associated with the one or more first array dies and the first die interconnect, the second driver having a second driver size corresponding to a second capacitive load associated with the one or more second array dies and the second die interconnect.

20. (New) The memory module of claim 11, wherein the control die does not receive data path control signals from the register device via the second control terminals during the second mode.

21. (New) The memory module of claim 11, wherein, during the first mode, the register device is configurable to perform rank multiplication, and wherein, during the second mode, the control die is configurable to perform rank multiplication.

Petitioners
Ex. 1009, p. 138

REMARKS

This amendment responds to the office action mailed October 3, 2019. In the office action, the Examiner:

- rejected claim 1 under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement;
- rejected claim 1 on the ground of nonstatutory double patenting as being unpatentable over claims 29 and 30 of U.S. Patent No. 8,787,060;
- rejected claim 1 on the ground of nonstatutory double patenting as being unpatentable over claims 10 and 15 of U.S. Patent No. 9,318,160;
- rejected claim 1 on the ground of nonstatutory double patenting as being unpatentable over claims 1 and 5 of U.S. Patent No. 9,659,601; and
- rejected claim 1 on the ground of nonstatutory double patenting as being unpatentable over claim 1 of U.S. Patent No. 10,290,328.

REMARKS CONCERNING CLAIMS

Claim 1 has been canceled.

Claims 2-21 have been added.

Support for the amendments can be found in at least paragraphs [0086] through [0108], and Figures 6A through 8 of the application as filed. No new matter has been added.

With respect to all amendments, Applicant has not dedicated or abandoned any unclaimed subject matter. Moreover, Applicant has not acquiesced to any characterizations of the invention, nor any rejections or objections of the claims, made by the Examiner. Moreover, the Applicant hereby rescinds any prior disclaimer of claim scope, to the extent they exist, made during the prosecution of this application or made during the prosecution of any patent or other related patents/applications, and advises the Examiner that any such previous disclaimers and the cited references that they were made to avoid may need to be revisited.

After entry of this amendment, the pending claims are: claims 2-21.

Petitioners
Ex. 1009, p. 139

REMARKS CONCERNING REJECTIONS UNDER 35 U.S.C. 112

I. REJECTION OF CLAIM 1 UNDER 35 U.S.C. 112, FIRST PARAGRAPH, AS FAILING TO COMPLY WITH THE WRITTEN DESCRIPTION REQUIREMENT

Claim 1 has been cancelled without prejudice. Therefore, the rejection is now moot.

REMARKS CONCERNING DOUBLE PATENTING REJECTIONS

II. REJECTION OF CLAIM 1 ON THE GROUND OF NONSTATUTORY DOUBLE PATENTING AS BEING UNPATENTABLE OVER CLAIMS 29 AND 30 OF U.S. PATENT NO. 8,787,060

The Applicant respectfully requests that the Examiner reconsider this nonstatutory double patenting rejection in light of the amendments in the claims.

III. REJECTION OF CLAIM 1 ON THE GROUND OF NONSTATUTORY DOUBLE PATENTING AS BEING UNPATENTABLE OVER CLAIMS 10 AND 15 OF U.S. PATENT NO. 9,318,160

The Applicant respectfully requests that the Examiner reconsider this nonstatutory double patenting rejection in light of the amendments in the claims.

IV. REJECTION OF CLAIM 1 ON THE GROUND OF NONSTATUTORY DOUBLE PATENTING AS BEING UNPATENTABLE OVER CLAIMS 1 AND 5 OF U.S. PATENT NO. 9,659,601

The Applicant respectfully requests that the Examiner reconsider this nonstatutory double patenting rejection in light of the amendments in the claims.

V. REJECTION OF CLAIM 1 ON THE GROUND OF NONSTATUTORY DOUBLE PATENTING AS BEING UNPATENTABLE OVER CLAIM 1 OF U.S. PATENT NO. 10,290,328

The Applicant respectfully requests that the Examiner reconsider this nonstatutory double patenting rejection in light of the amendments in the claims.

Petitioners
Ex. 1009, p. 140

REMARKS CONCERNING NEW CLAIMS

New claims 2-21 are believed to be patentable

Accordingly, Applicant respectfully requests that the Examiner consider the new claims 2-21 with a view towards allowance.

CONCLUDING REMARKS

By responding in the foregoing remarks only to particular positions asserted by the examiner, the Applicant does not necessarily acquiesce in other positions that have not been explicitly addressed. In addition, the Applicant's arguments for the patentability of a claim should not be understood as implying that no other reasons for the patentability of that claim exist.

In light of the above amendments and remarks, the Applicant respectfully requests that the Examiner reconsider this application with a view towards allowance. The Examiner is invited to call the undersigned attorney at (650) 843-4000, if a telephone call could help resolve any remaining items.

Respectfully submitted,

Date: March 3, 2020

/Jamie J. Zheng/ 51,167

Jamie Zheng (Reg. No.)
MORGAN, LEWIS & BOCKIUS LLP
1400 Page Mill Road
Palo Alto, CA 94304
Phone: (650) 843-4000

Petitioners
Ex. 1009, p. 141

Electronic Patent Application Fee Transmittal

Application Number:	16412308
Filing Date:	14-May-2019
Title of Invention:	MEMORY MODULE WITH BUFFERED MEMORY PACKAGES
First Named Inventor/Applicant Name:	Hyun Lee
Filer:	Jamie Jie Zheng/S. Olivier
Attorney Docket Number:	129980-5070-US01

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension - 2 months with $0 paid	1252	1	600	600
Miscellaneous:				
			Total in USD ($)	**600**

Electronic Acknowledgement Receipt

EFS ID:	38760603
Application Number:	16412308
International Application Number:	
Confirmation Number:	6765
Title of Invention:	MEMORY MODULE WITH BUFFERED MEMORY PACKAGES
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng/S. Olivier
Filer Authorized By:	Jamie Jie Zheng
Attorney Docket Number:	129980-5070-US01
Receipt Date:	03-MAR-2020
Filing Date:	14-MAY-2019
Time Stamp:	20:19:28
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$600
RAM confirmation Number	E202033K19531196
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		129980-5070US01_AMEND.pdf	149233 be426658350d8635962f2d120d50a5df646f389f	yes	10

Multipart Description/PDF files in .zip description

Document Description	Start	End
Amendment/Req. Reconsideration-After Non-Final Reject	1	2
Claims	3	8
Applicant Arguments/Remarks Made in an Amendment	9	10

Warnings:

Information:

2	Fee Worksheet (SB06)	fee-info.pdf	31116 f2186854c484ac54a15e04289218dd1a9ecc81d3	no	2

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Total Files Size (in bytes):	180349

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 16/412,308	Filing Date 05/14/2019	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $100 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $460 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

AMENDMENT		(Column 1)		(Column 2)	(Column 3)			
	03/03/2020	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0		x $100 =	0
	Independent (37 CFR 1.16(h))	* 2	Minus	*** 3	= 0		x $460 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

AMENDMENT		(Column 1)		(Column 2)	(Column 3)			
		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/LINDA A WISE/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed June 5, 2020	
				Application Number	16/412,308
				Filing Date	May 14, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2827
				Examiner Name	Hoang, Huan
Sheet	1	of	11	Attorney Docket Number	129980-5070US01

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		CN 102576565 B	09-30-2015	Netlist, Inc.		

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Examiner Signature		Date Considered	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed June 5, 2020	
				Application Number	16/412,308
				Filing Date	May 14, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2827
				Examiner Name	Hoang, Huan
Sheet	9	of	11	Attorney Docket Number	129980-5070US01

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Examiner Signature		Date Considered	

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Examiner Signature		Date Considered	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed June 5, 2020	
				Application Number	16/412,308
				Filing Date	May 14, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2827
				Examiner Name	Hoang, Huan
Sheet	11	of	11	Attorney Docket Number	129980-5070US01

Examiner Signature		Date Considered	

DB2/ 22684197.4

Electronic Acknowledgement Receipt

EFS ID:	39645986
Application Number:	16412308
International Application Number:	
Confirmation Number:	6765
Title of Invention:	MEMORY MODULE WITH BUFFERED MEMORY PACKAGES
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng/Lamesha Robertson
Filer Authorized By:	Jamie Jie Zheng
Attorney Docket Number:	129980-5070-US01
Receipt Date:	05-JUN-2020
Filing Date:	14-MAY-2019
Time Stamp:	19:03:01
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		129980_5070US01_IDS.pdf	533408 9489f36c0182f650bdb10bf45d10499cf6b86a03	yes	15

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Transmittal Letter	1	4
	Information Disclosure Statement (IDS) Form (SB08)	5	15
Warnings:			
Information:			
	Total Files Size (in bytes):	533408	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronically filed June 5, 2020

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun Lee et al	Confirmation No.:	6765
Serial No.:	16/412,308	Art Unit:	2827
Filed:	May 14, 2019	Examiner:	Hoang, Huan
For:	MEMORY MODULE WITH BUFFERED MEMORY PACKAGES	Attorney Docket No.:	129980-5070US01

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure provisions of 37 C.F.R. §1.56, there is hereby provided certain information which the Examiner may consider material to the examination of the subject U.S. patent application. It is requested that the Examiner make this information of record if it is deemed material to the examination of the application.

1. Enclosures accompanying this Information Disclosure Statement are:

1a. ☒ A list of all patents, publications, applications, or other information submitted for consideration by the office.

1b. A legible copy of:

☐ Each foreign patent;

☐ Each publication or that portion which caused it to be listed on the PTO-1449;

☐ For each cited pending U.S. application, the application specification including the claims, and any drawing of the application, or portion of the application which caused it to be listed on the PTO-1449 including any claims directed to that portion;

☐ all other information or portion which caused it to be listed on the PTO-1449.

1c. ☐ An English language copy of search report(s) from a counterpart foreign application or PCT International Search Report.

1d. ☐ Explanations of relevancy (ATTACHMENT 1(d), hereto) or English language abstracts of the non-English language publications.

2. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(b):

☐ Within three months of the filing date of a national application other than a continued prosecution application under §1.53(d);

☐ Within three months of the date of entry of the national stage as set forth in §1.491 in an international application;

☐ Before the mailing of the first Office action on the merits;

☐ Before the mailing of a first Office action after the filing of a request for continued examination under §1.114.

3. ☒ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(c) after the period specified in 37 C.F.R. §1.97(b), but before the mailing date of any of a final action under 37 C.F.R. §1.113, a notice of allowance under 37 C.F.R. §1.311 or an action that otherwise closes prosecution in the application.

(Check either Item 3a, 3b, 3c or 3d)

3a. ☐ The Certification Statement in Item 5 below is applicable. Accordingly, no fee is required.

3b. ☒ The $240 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5070US01).

3c. ☐ The $120 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

3d. ☐ The $60 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

(Items 3b or 3c to be checked if any reference known for more than 3 months)

4. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(d) after the period specified in 37 C.F.R. §1.97(c), but on or before the date of payment of the issue fee.

(Check Item 4a, and 4b, 4c or 4d)

4a. ☐ The Certification Statement in Item 5 below is applicable.

4b. ☐ The $240 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

4c. ☐ The $120 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

4d. ☐ The $60 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

5. ☐ Certification Statement (applicable if Item 3a or Item 4a is checked)

(Check either Item 5a, 5b, 5c or 5d)

5a. ☐ In accordance with 37 C.F.R. §1.97(e)(1), it is certified that each item of information contained in this information disclosure statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement.

5b. ☐ In accordance with 37 C.F.R. §1.97(e)(2), it is certified that no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 C.F.R. §1.56(c) more than three months prior to the filing of this information disclosure statement.

5c. ☐ Each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

5d. ☐ Pursuant to 37 C.F.R. §1.704(d), each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

6. ☒ Copies of each cited U.S. patent and each U.S. patent application publication are not enclosed pursuant to the USPTO OG Notice dated 05 August 2003 waiving the requirement under 37 C.F.R. 1.98(a)(2)(i) for U.S. patent applications filed after June 30, 2003.

7. ☒ This application is a continuation application under 37 C.F.R. §1.53(b) or (d).

(Check appropriate Items 7a, 7b and/or 7c)

7a. ☐ A Petition to Withdraw from issue under 37 C.F.R. §1.313(b)(5) is concurrently filed herewith.

7b. ☒ Copies of publications listed on Form PTO-1449 from prior application Serial No. 15/602,099, filed on May 22, 2017, 15/095,288, filed on April 11, 2016, 14/337,168, filed on July 21, 2014, and 13/288,850, filed on November 3, 2011, of which this application claims priority under 35 U.S.C. §120, are not being submitted pursuant to 37 C.F.R. §1.98(d).

7c. ☐ Copies of the publications listed on the attached Form PTO-1449 that were not previously cited in prior application Serial No. , filed on , are provided herewith.

8. ☐ This is a Supplemental Information Disclosure Statement. (Check Item 8a)

8a. ☐ This Supplemental Information Disclosure Statement under 37 C.F.R. §1.97(f) supplements the Information Disclosure Statement filed on . A bona fide attempt was made to comply with 37 C.F.R. §1.98, but inadvertent omissions were made. These omissions have been corrected herein. Accordingly, additional time is requested so that this Supplemental Information Disclosure Statement can be considered as if properly filed on .

9. ☐ In accordance with 37 C.F.R. §1.98, a concise explanation of what is presently understood to be the relevance of each non-English language publication is:

(Check Item 9a, 9b, or 9c)

9a. ☐ satisfied because all non-English language publications were cited on the enclosed English language copy of the PCT International Search Report or the search report from a counterpart foreign application indicating the degree of relevance found by the foreign office.

9b. ☐ set forth in the application.

9c. ☐ enclosed as an attachment hereto.

10. ☒ The Commissioner is authorized to charge any additional fee required or credit any overpayment for this Information Disclosure Statement and/or Petition to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5070US01).

11. ☒ No admission is made that the information cited in this Statement is, or is considered to be, material to patentability nor a representation that a search has been made (other than a search report of a foreign counterpart application or PCT International Search Report if submitted herewith). 37 C.F.R. §§1.97(g) and (h).

Respectfully submitted,

Date: June 5, 2020

/ Jamie J. Zheng / 51,167

Jamie J. Zheng (Reg. No.)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed June 8, 2020	
				Application Number	16/412,308
				Filing Date	May 14, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2827
				Examiner Name	Hoang, Huan
Sheet	1	of	11	Attorney Docket Number	129980-5070US01

U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.	Document Number Number - Kind Code	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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FOREIGN PATENT DOCUMENTS

Examiner Initials	Cite No.	Foreign Patent Document Country Code – Number - Kind Code *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T
		CN 102576565 B	09-30-2015	Netlist, Inc.		

NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
		Response, Article 94 3 EPC, EP 18179414.0, 6AUG2019, 23 pgs
		Netlist, Inc., Third Party Observation, EP 3404660, 6AUG2019, 34 pgs
		Office Action, EP 18179414, 2APR2019, 6 pgs
		Patent document filed by third party, EP 18179414, 22FEB2019, 10 pgs

Examiner Signature		Date Considered	

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Examiner Signature		Date Considered	

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		Inter Partes Review of US Patent No. 8,516,185 B2, Case No. IPR2017-00577, Final Written Decision, filed July 5, 2018.
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Examiner Signature		Date Considered	

		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1012, 'Declaration of John J. Kelly Regarding Records of Joint Electron Device Engineering Council JEDEC,' filed December, 22, 2017
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		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1029, 'Respondents' Reply Post-Hearing Brief, Certain Memory Modules and Components Thereof, and Products Containing Same, Inv. No. 337-TA-1023 (June 9, 2017) (excerpts relevant to '185 patent),' filed December, 22, 2017

Examiner Signature		Date Considered	

		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1030, 'High-quality versions of demonstrative graphics included in Respondents' Reply Post-Hearing Brief (Ex.1029),' filed December, 22, 2017
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		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1040, 'Initial Determination, Certain Memory Modules and Components Thereof, and Products Containing Same, Inv. No. 337-TA-1023 (Nov. 14, 2017) (redacted excerpts),' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1041, 'Bruce Jacob et al., Memory System: Cache, DRAM, Disk (2008) (excerpts),' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1042, 'Direct RDRAM datasheet (2000),' filed December, 22, 2017

Examiner Signature		Date Considered	

		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Petition for Review of U.S. Patent No. 9,606,907, filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Preliminary Response, filed April 10, 2018
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00364, Petition for Inter Partes Review of U.S. Patent No. 9,606,907, filed December, 27, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00365, Petition for Inter Partes Review of U.S. Patent No. 9,606,907, filed December, 27, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petition for Inter Partes Review, filed December, 30, 2016
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Patent Owner's Preliminary Response, filed April, 9, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Patent Owner's Response, filed September, 15, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petitioners' Objections to Evidence, filed September, 22, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petitioners Motion to Exclude Certain Inadmissible Testimony of Patent Owners Expert Carl Sechen, filed January, 9, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petitioners Request for Oral Hearing, filed January, 9, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, PO Request for Oral Argument, filed January, 9, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, PO Motion for Observations, filed January, 9, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petitioners' Response to Patent Owner's Motion for Observations, filed January, 23, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, PO's Opposition to Petitioner's Motion to Exclude, filed January, 23, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petitioners' Reply In Support Of Motion to Exclude Certain Inadmissible Testimony Of Patent Owner's Expert Carl Sechen, filed January, 30, 2018

Examiner Signature		Date Considered	

		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petitioners' Updated Exhibit List, filed February, 9, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Patent Owner's Updated Exhibit List, filed February, 9, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Trial Instituted Document, filed May, 15, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, ORDER Trial Hearing, filed January, 25, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Hearing Transcript, filed March, 22, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Final Written Decision, filed May 3, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 1002, 'Excerpts of FH for U.S. Patent 8,756,364,' filed December, 30, 2016
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 1003, 'Declaration of Harold Stone,' filed December, 15, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 1007, 'JEDEC JESD79 publication (June 2000),' filed December, 30, 2016
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 1008, 'JEDEC Declaration for DDR Specification,' filed December, 30, 2016
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 1015, 'Texas Instruments 74LS245 datasheet (2002),' filed December, 30, 2016
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 1017, '2000-03 Samsung CMOS SDRM data sheet,' filed September, 15, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 1019, 'Final Decision [IPR2014-01011],' filed September, 15, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 1020, 'Final Decision [IPR2014-00883],' filed December, 30, 2016
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 1023, 'Gordon_Moore_1965_article,' filed December, 30, 2016

Examiner Signature		Date Considered	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed June 8, 2020	
				Application Number	16/412,308
				Filing Date	May 14, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2827
				Examiner Name	Hoang, Huan
Sheet	8	of	11	Attorney Docket Number	129980-5070US01

		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 1024, 'Deposition Transcript of Carl Sechen (Dec. 8, 2017),' filed December, 15, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 1025, 'Supplemental Declaration of Harold S. Stone (Dec. 15, 2017),' filed December, 15, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 1026, 'Xilinx CoolRunner XPLA3 CPLD product specification (2000),' filed December, 15, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 1027, 'Xilinx Programmable Logic Design Quick Start Handbook (2004),' filed January, 9, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 1028, 'Xilinx TQFP package datasheet (2000),' filed January, 9, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 1029, 'Xilinx VQFP package datasheet (2002),' filed February, 9, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 1030, 'Xilinx CS280 package datasheet (1999),' filed December, 15, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 1031, 'Petitioners Demonstratives,' filed April, 9, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 2001, 'Exhibit 2001,' filed December, 15, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 2002, 'Exhibit 2002,' filed December, 15, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 2003, 'Exhibit 2003,' filed February, 9, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 2004, 'Exhibit 2004,' filed December, 30, 2016
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 2005, 'Exhibit 2005,' filed September, 15, 2017
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Patent Owner's Preliminary Response, filed April, 10, 2017
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Petitioners' Updated Exhibit List, filed June, 21, 2017
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Patent Owner's Response, filed October, 25, 2017

Examiner Signature		Date Considered	

DB2/ 22684197.4

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed June 8, 2020	
				Application Number	16/412,308
				Filing Date	May 14, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2827
				Examiner Name	Hoang, Huan
Sheet	9	of	11	Attorney Docket Number	129980-5070US01

		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Petitioners' Objections to Evidence, filed October, 31, 2017
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Petitioners' Reply to Patent Owner's Response, filed February, 6, 2018
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Patent Owner's Objections to Evidence, filed February, 13, 2018
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Petitioners' Request for Oral Hearing, filed February, 28, 2018
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Patent Owner's Request for Oral Argument, filed February, 28, 2018
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Patent Owner's Motion to Exclude, filed February, 28, 2018
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Petitioners' Opposition to Patent Owner's Motion to Exclude, filed March, 14, 2018
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Patent Owner's Reply to Petitioner's Opposition to Motion to Exclude, filed March, 21, 2018
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Notice of Accord Filing Date, filed January, 10, 2017
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Trial Instituted Document, filed July, 7, 2017
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Order - Request for Oral Argument - 37 CFR 42.70, filed April, 2, 2018
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, EXHIBITS 1003, 'Declaration of Harold S. Stone,' filed January, 5, 2017
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, EXHIBITS 1007, 'JEDEC JESD79 publication (June 2000),' filed January, 5, 2017
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, EXHIBITS 1009, 'TI 74LS245 datasheet (2002),' filed April, 10, 2017
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, EXHIBITS 1010, 'JEDEC Declaration,' filed January, 5, 2017

Examiner Signature		Date Considered	

DB2/ 22684197.4

		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, EXHIBITS 1011, 'IPR2014-01369 08-23-2014 Petition for Inter Partes Review,' filed January, 5, 2017
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, EXHIBITS 1012, 'IPR2014-01029 06-24-2014 Petitioner for Inter Partes Review,' filed April, 10, 2017
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, EXHIBITS 1025, 'US Patent Application Publication 2011/0016250,' filed June, 21, 2017
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, EXHIBITS 1026, 'Netlist's post-hearing brief,' filed June, 21, 2017
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, EXHIBITS 1027, 'Hynix's post-hearing brief,' filed October, 25, 2017
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, EXHIBITS 1028, 'Demonstrative Graphics from hynix's post-hearing brief,' filed October, 25, 2017
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, EXHIBITS 1029, 'Netlist's reply post-hearing brief,' filed October, 25, 2017
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, EXHIBITS 1030, 'hynix's reply post-hearing brief,' filed June, 21, 2017
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, EXHIBITS 1031, 'Demonstrative Graphics from hynix's reply post-hearing brief,' filed June, 21, 2017
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, EXHIBITS 2001, 'Exhibit 2001,' filed June, 21, 2017
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, EXHIBITS 2002, 'Exhibit 2002,' filed June, 21, 2017
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, EXHIBITS 2003, 'Exhibit 2003,' filed October, 25, 2017
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, EXHIBITS 2004, 'Exhibit 2004,' filed October, 25, 2017
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, EXHIBITS 2005, 'Exhibit 2005,' filed December, 30, 2016
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, EXHIBITS 2006, 'Exhibit 2006,' filed December, 30, 2016
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, EXHIBITS 2007, 'Exhibit 2007,' filed December, 30, 2016

Examiner Signature		Date Considered	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed June 8, 2020	
				Application Number	16/412,308
				Filing Date	May 14, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2827
				Examiner Name	Hoang, Huan
Sheet	11	of	11	Attorney Docket Number	129980-5070US01

Examiner Signature		Date Considered	

DB2/ 22684197.4

Electronically filed June 8, 2020

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hoang, Huan	Confirmation No.:	6765
Serial No.:	16/412,308	Art Unit:	2827
Filed:	May 14, 2019	Examiner:	Hoang, Huan
For:	MEMORY MODULE WITH BUFFERED MEMORY PACKAGES	Attorney Docket No.:	129980-5070US01

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure provisions of 37 C.F.R. §1.56, there is hereby provided certain information which the Examiner may consider material to the examination of the subject U.S. patent application. It is requested that the Examiner make this information of record if it is deemed material to the examination of the application.

1. Enclosures accompanying this Information Disclosure Statement are:

1a. ☒ A list of all patents, publications, applications, or other information submitted for consideration by the office.

1b. A legible copy of:

☐ Each foreign patent;

☐ Each publication or that portion which caused it to be listed on the PTO-1449;

☐ For each cited pending U.S. application, the application specification including the claims, and any drawing of the application, or portion of the application which caused it to be listed on the PTO-1449 including any claims directed to that portion;

☐ all other information or portion which caused it to be listed on the PTO-1449.

1c. ☐ An English language copy of search report(s) from a counterpart foreign application or PCT International Search Report.

1d. ☐ Explanations of relevancy (ATTACHMENT 1(d), hereto) or English language abstracts of the non-English language publications.

2. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(b):

☐ Within three months of the filing date of a national application other than a continued prosecution application under §1.53(d);

☐ Within three months of the date of entry of the national stage as set forth in §1.491 in an international application;

☐ Before the mailing of the first Office action on the merits;

☐ Before the mailing of a first Office action after the filing of a request for continued examination under §1.114.

3. ☒ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(c) after the period specified in 37 C.F.R. §1.97(b), but before the mailing date of any of a final action under 37 C.F.R. §1.113, a notice of allowance under 37 C.F.R. §1.311 or an action that otherwise closes prosecution in the application.

(Check either Item 3a, 3b, 3c or 3d)

3a. ☐ The Certification Statement in Item 5 below is applicable. Accordingly, no fee is required.

3b. ☒ The $240 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5070US01).

3c. ☐ The $120 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

3d. ☐ The $60 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

(Items 3b or 3c to be checked if any reference known for more than 3 months)

4. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(d) after the period specified in 37 C.F.R. §1.97(c), but on or before the date of payment of the issue fee.

(Check Item 4a, and 4b, 4c or 4d)

4a. ☐ The Certification Statement in Item 5 below is applicable.

4b. ☐ The $240 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

4c. ☐ The $120 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

4d. ☐ The $60 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

5. ☐ Certification Statement (applicable if Item 3a or Item 4a is checked)

(Check either Item 5a, 5b, 5c or 5d)

5a. ☐ In accordance with 37 C.F.R. §1.97(e)(1), it is certified that each item of information contained in this information disclosure statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement.

5b. ☐ In accordance with 37 C.F.R. §1.97(e)(2), it is certified that no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 C.F.R. §1.56(c) more than three months prior to the filing of this information disclosure statement.

5c. ☐ Each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

5d. ☐ Pursuant to 37 C.F.R. §1.704(d), each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

6. ☒ Copies of each cited U.S. patent and each U.S. patent application publication are not enclosed pursuant to the USPTO OG Notice dated 05 August 2003 waiving the requirement under 37 C.F.R. 1.98(a)(2)(i) for U.S. patent applications filed after June 30, 2003.

7. ☒ This application is a continuation application under 37 C.F.R. §1.53(b) or (d).

(Check appropriate Items 7a, 7b and/or 7c)

7a. ☐ A Petition to Withdraw from issue under 37 C.F.R. §1.313(b)(5) is concurrently filed herewith.

7b. ☒ Copies of publications listed on Form PTO-1449 from prior application Serial No. 15/470,856, filed on March 27, 2017, of which this application claims priority under 35 U.S.C. §120, are not being submitted pursuant to 37 C.F.R. §1.98(d).

7c. ☐ Copies of the publications listed on the attached Form PTO-1449 that were not previously cited in prior application Serial No. , filed on , are provided herewith.

8. ☐ This is a Supplemental Information Disclosure Statement. (Check Item 8a)

8a. ☐ This Supplemental Information Disclosure Statement under 37 C.F.R. §1.97(f) supplements the Information Disclosure Statement filed on . A bona fide attempt was made to comply with 37 C.F.R. §1.98, but inadvertent omissions were made. These omissions have been corrected herein. Accordingly, additional time is requested so that this Supplemental Information Disclosure Statement can be considered as if properly filed on .

9. ☐ In accordance with 37 C.F.R. §1.98, a concise explanation of what is presently understood to be the relevance of each non-English language publication is:

(Check Item 9a, 9b, or 9c)

9a. ☐ satisfied because all non-English language publications were cited on the enclosed English language copy of the PCT International Search Report or the search report from a counterpart foreign application indicating the degree of relevance found by the foreign office.

9b. ☐ set forth in the application.

9c. ☐ enclosed as an attachment hereto.

10. ☒ The Commissioner is authorized to charge any additional fee required or credit any overpayment for this Information Disclosure Statement and/or Petition to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5070US01).

11. ☒ No admission is made that the information cited in this Statement is, or is considered to be, material to patentability nor a representation that a search has been made (other than a search report of a foreign counterpart application or PCT International Search Report if submitted herewith). 37 C.F.R. §§1.97(g) and (h).

Respectfully submitted,

Date: June 8, 2020

/ Jamie J. Zheng / 51,167

Jamie J. Zheng (Reg. No.)
MORGAN, LEWIS & BOCKIUS LLP
1400 Page Mill Road
Palo Alto, CA 94304
(650) 843-4000

Electronic Acknowledgement Receipt

EFS ID:	39658697
Application Number:	16412308
International Application Number:	
Confirmation Number:	6765
Title of Invention:	MEMORY MODULE WITH BUFFERED MEMORY PACKAGES
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng/Lamesha Robertson
Filer Authorized By:	Jamie Jie Zheng
Attorney Docket Number:	129980-5070-US01
Receipt Date:	08-JUN-2020
Filing Date:	14-MAY-2019
Time Stamp:	17:15:36
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		129980_5070US01_IDS.pdf	533390 55ae58ce6e1e53b289555eb6044e25ff267ba07c	yes	15

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Information Disclosure Statement (IDS) Form (SB08)	5	15
	Transmittal Letter	1	4
Warnings:			
Information:			
	Total Files Size (in bytes):	533390	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/412,308	05/14/2019	Hyun Lee	129980-5070-US01	6765

79141 7590 06/09/2020
Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304

EXAMINER
HOANG, HUAN

ART UNIT	PAPER NUMBER
2827	

NOTIFICATION DATE	DELIVERY MODE
06/09/2020	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

padocketingdepartment@morganlewis.com
vskliba@morganlewis.com

Office Action Summary	Application No. 16/412,308	Applicant(s) Lee, Hyun	
	Examiner HUAN HOANG	Art Unit 2827	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 03 March 2020.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☑ This action is **FINAL.** 2b) ☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 2-21 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 2-21 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

DETAILED ACTION

Notice of Pre-AIA or AIA Status

1. The present application is being examined under the pre-AIA first to invent provisions.

The Amendment filed on 03/03/2020 has been received and entered.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on nonstatutory double patenting provided the reference application or patent either is shown to be

commonly owned with the examined application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. See MPEP § 717.02 for applications subject to examination under the first inventor to file provisions of the AIA as explained in MPEP § 2159. See MPEP §§ 706.02(l)(1) - 706.02(l)(3) for applications not subject to examination under the first inventor to file provisions of the AIA. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO Internet website contains terminal disclaimer forms which may be used. Please visit www.uspto.gov/patent/patents-forms. The filing date of the application in which the form is filed determines what form (e.g., PTO/SB/25, PTO/SB/26, PTO/AIA/25, or PTO/AIA/26) should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp.

3. Claims 2-21 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-4, 6, 7, 10 and 11 of U.S. Patent No. 10,290,328. Although the claims at issue are not identical, they are not patentably distinct from each other because it would have been obvious to one of ordinary skill in the art to recognize that the memory module of claims 2-10 and the memory module of claims 1-4, 6, 7, 10 and 11 of the patent are identical in structure; therefore, the differences of two sets of claims are only functional limitations.

Regarding claims 2 and 8: Claims 1 and 13 of the patent recite a memory module operable in a computer system to communicate with a system memory controller via a command/address bus and a data bus, comprising:

a register device configurable to receive input command/address signals from the system memory controller via the command/address bus and to output control signals in response to the input command/address signals (claim 1, lines 4-8 and claim 13, lines 4-7), the control signals including buffered command/address signals and data path control signals; and

a plurality of DRAM packages, each respective DRAM package comprising (claim 1, lines 9-12 and claim 13, lines 8-10):

terminals including control terminals coupled to the register device and data terminals to be coupled to a respective section of the data bus (claim 1, lines 13-15 and claim 13, lines 11-14), the control terminals including first control terminals and second control terminals;

stacked array dies (claim 1, line 16 and claim 13, line 15); and

a control die (claim 1, line 17 and claim 13, line 16) coupled between the stacked array dies and the terminals of the respective DRAM package, the control die including data buffers (claim 6, line 2 and claim 15, line 2) and a data path control circuit (claim 3, line 2 and claim 14, line 2; and wherein the control die is configurable to:

receive the buffered command/address signals via the first control terminals and the data path control signals via the second control terminals;

pass at least some of the buffered command/address signals through the control die to the stacked array dies, the buffered command/address signals including chip-select signals that are provided to respective array dies of the stacked array dies; and

control the data buffers in response to the data path control signals to buffer data signals communicated between a selected array die of the stacked array dies and the respective section of the data bus, the selected array die having received one of the chip select signals that is different from any of the other ones of the chip select signals (claim 18).

Regarding claim 3: Claim 3 and claim 13 of the patent recite the memory module of claim 2, wherein the register device is configurable to decode the input command/address signals and to generate the data path control signals in accordance with the input command/address signals (claim 3, lines 2-4, claim 10, line 2 and claim 13, lines 4-7).

Regarding claim 4: Claim 1 and claim 13 of the patent recite the memory module of claim 2, wherein the data buffers are configurable to selectively isolate one or more array dies of the stacked array dies (claim 1, line 33 and claim 13, line 28).

Regarding claim 5: Claim 1 and claim 13 of the patent recite the memory module of claim 2, wherein the control die does not secondarily buffer the buffered command/address signals.

Regarding claim 6: Claim 4 and claim 17 of the patent recite the memory module of claim 2, wherein the data path control circuit is configurable to control a command/address time slot for the buffered command/address signals passing through the control die.

Regarding claim 7: Claim 2 of the patent recites the memory module of claim 2, wherein the data path control circuit is configurable to control a data bus time slot for the data signals.

Regarding claim 9: Claim 1, 6, 13 and 15 recite the memory module of claim 2, further comprising die interconnects including first die interconnects coupled to the data buffers and second die interconnects coupled to the control terminals, each of the first die interconnects being coupled to one or more of the stacked array dies.

Regarding claim 10: Claims 11 and claim 13 of the patent recite the memory module of claim 9, wherein the data buffers include drivers coupled to respective ones of the first die interconnects, the drivers including a first driver coupled to one or more first array dies via a first die interconnect and a second driver and coupled to one or more second array dies via a second die interconnect, the first driver having a first driver size corresponding to a first capacitive load associated with the one or more first array dies and the first die interconnect, the second driver having a second driver size corresponding to a second capacitive load associated with the one or more second array dies and the second die interconnect.

Regarding claims 11-21: It would have been obvious to one of ordinary skill in the art to recognize that the memory module of claims 10-21 and the memory module of claims 1-4, 6, 7, 10 and 11 are identical in structure; therefore, the differences between two sets of claims are only functional limitations, for example, the memory module of claims 1-4, 6, 7, 10 and 11 of the patent is operable in any one of a plurality of modes including a first mode and a second mode as recited in claim 11.

4. Claims 2-21 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-11, 14 and 15 of U.S. Patent No. 9,659,601. Although the claims at issue are not identical, they are not patentably distinct from each other because it would have been obvious to one of ordinary skill in the art to recognize that the memory module of claims 2-21 and the memory module of claims 1-11, 14 and 15 of the patent are identical in structure, the difference between two sets of claims are only functional limitations (see the rejections of claims 2-21 above).

5. Claims 2-21 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 10-20 of U.S. Patent No. 9,318,160. Although the claims at issue are not identical, they are not patentably distinct from each other because it would have been obvious to one of ordinary skill in the art to recognize that the memory module of claims 2-21 and the memory module of claims 10-20 of the patent are identical in structure, the difference between two sets of claims are only functional limitations.

6. Claims 2-21 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 29-34 of U.S. Patent No. 8,787060. Although the claims at issue are not identical, they are not patentably distinct from each other because it would have been obvious to one of ordinary skill in the art to recognize that the memory module of claims 2-21 and the memory module of claims 29-34 of the patent are identical in structure, the difference between two sets of claims are only functional limitations.

Response to Arguments

7. Applicant's arguments with respect to claims 2-21 have been considered but are moot because the arguments do not apply to any of the references being used in the current rejection.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to HUAN HOANG whose telephone number is (571)272-1779. The examiner can normally be reached on 7:30AM-4:00PM M-F.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, AMIR ZARABIAN can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see https://ppair-my.uspto.gov/pair/PrivatePair. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/HUAN HOANG/
Primary Examiner, Art Unit 2827

Notice of References Cited	Application/Control No. 16/412,308	Applicant(s)/Patent Under Reexamination Lee, Hyun	
	Examiner HUAN HOANG	Art Unit 2827	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-7685364-B2	03-2010	Shaeffer; Ian	G11C11/4076	711/115
*	B	US-10290328-B2	05-2019	Lee; Hyun	G11C7/1084	1/1
	C					
	D					
	E					
	F					
	G					
	H					
	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/412,308	Lee, Hyun
	Examiner	**Art Unit**
	HUAN HOANG	2827

CPC - Searched*		
Symbol	**Date**	**Examiner**
G11C 5/066, G11C 5/06, G11C 7/1057, G11C 7/1094, G11C 7/12	09/29/2019	HH
Above Updated	06/04/2020	HH

CPC Combination Sets - Searched*		
Symbol	**Date**	**Examiner**

US Classification - Searched*			
Class	**Subclass**	**Date**	**Examiner**
365	63	09/29/2019	HH
Above	Updated	06/04/2020	HH

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	**Date**	**Examiner**
EAST (text search)	09/29/2019	HH
Assignee and Inventor search	09/29/2019	HH
EAST (text search)	06/04/2020	HH
Assignee and Inventor search	06/04/2020	HH

Interference Search			
US Class/CPC Symbol	**US Subclass/CPC Group**	**Date**	**Examiner**

/HUAN HOANG/ Primary Examiner, Art Unit 2827	

Petitioners
Ex. 1009, p. 193

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/412,308	Lee, Hyun
	Examiner	**Art Unit**
	HUAN HOANG	2827

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/29/2019	06/04/2020							
	1	✓	-							
	2		✓							
	3		✓							
	4		✓							
	5		✓							
	6		✓							
	7		✓							
	8		✓							
	9		✓							
	10		✓							
	11		✓							
	12		✓							
	13		✓							
	14		✓							
	15		✓							
	16		✓							
	17		✓							
	18		✓							
	19		✓							
	20		✓							
	21		✓							

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L3	35,346	(G11C5/066 or G11C7/12 or G11C5/06 or G11C7/1057 or G11C7/1084).cpc. 365/063,63.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/04 10:04
L4	2,941	3 and (command address) with register	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/04 10:05
L5	209	4 and (dram dynamic adj ram dynamic adj random) with package	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/04 10:06
L6	78	5 and (die dice ic integrated adj circuit) with stack$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/04 10:07
L7	62	6 and control$4 near5 (die dice ic integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/04 10:08
L8	30	6 and control$4 near5 (die dice ic integrated adj circuit) with buffer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/04 10:08
L9	1	6 and control$4 near5 (die dice ic integrated adj circuit) with buffer with chip adj (select$3 enabl$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/04 10:09
L10	2,402,521	netlist.as. lee.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/04 10:18
L11	8,222	10 and (command address) with register	US-PGPUB; USPAT; USOCR;	OR	ON	2020/06/04 10:18

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
L12	97	11 and (dram dynamic adj ram dynamic adj random) with package	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/04 10:19
L13	48	12 and (die dice ic integrated adj circuit) with stack$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/04 10:19
L15	22	13 and control$4 near5 (die dice ic integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/04 10:19
L16	13	15 and control$4 near5 (die dice ic integrated adj circuit) with buffer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/04 10:20
L17	0	16 and control$4 near5 (die dice ic integrated adj circuit) with buffer with chip adj (select$3 enabl$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/04 10:20
L18	9,756	(dram dynamic adj ram dynamic adj random) with package	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/04 10:22
L19	1,842	18 and (command address) with register	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/04 10:23
L20	406	19 and (die dice ic integrated adj circuit) with stack$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/04 10:23
L21	231	20 and control$4 near5 (die dice ic integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/04 10:23

L22	1	21 and control$4 near5 (die dice ic integrated adj circuit) with buffer with chip adj (select$3 enabl$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/04 10:24
S1	113	"10290328" "9659601" "9318160" "8787060"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/02 09:09
S2	82	S1 and register	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/02 09:10
S3	79	S1 and register and buffer$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/02 10:05
S4	2	"20130264592".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/03 08:22
S5	113	"10290328" "9659601" "9318160" "8787060"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/03 13:34
S6	8	S5 and register and buffer$3 and conduit	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/03 13:54
S7	2	S5 and register and buffer$3 with conduit	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/06/03 13:55

EAST Search History (Interference)

<This search history is empty>

6/4/2020 10:38:21 AM
C:\Users\hhoang1\Documents\EAST\Workspaces\164123081.wsp

Doc Code: DIST.E.FILE **Document Description: Electronic Terminal Disclaimer - Filed**	PTO/SB/26 U.S. Patent and Trademark Office Department of Commerce

Electronic Petition Request	**TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT**
Application Number	16412308
Filing Date	14-May-2019
First Named Inventor	Hyun Lee
Attorney Docket Number	129980-5070-US01
Title of Invention	MEMORY MODULE WITH BUFFERED MEMORY PACKAGES

☒ Filing of terminal disclaimer does not obviate requirement for response under 37 CFR 1.111 to outstanding Office Action

☒ This electronic Terminal Disclaimer is not being used for a Joint Research Agreement.

Owner	Percent Interest
Netlist, Inc.	100%

The owner(s) with percent interest listed above in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of prior patent number(s)

8787060

9318160

9659601

10290328

as the term of said prior patent is presently shortened by any terminal disclaimer. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the prior patent are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the owner does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the prior patent, "as the term of said prior patent is presently shortened by any terminal disclaimer," in the event that said prior patent later:
- expires for failure to pay a maintenance fee;
- is held unenforceable;
- is found invalid by a court of competent jurisdiction;
- is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
- has all claims canceled by a reexamination certificate;
- is reissued; or
- is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

(●) Terminal disclaimer fee under 37 CFR 1.20(d) is included with Electronic Terminal Disclaimer request.

( ) I certify, in accordance with 37 CFR 1.4(d)(4), that the terminal disclaimer fee under 37 CFR 1.20(d) required for this terminal disclaimer has already been paid in the above-identified application.

Applicant claims the following fee status:

( ) Small Entity

( ) Micro Entity

(●) Regular Undiscounted

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

THIS PORTION MUST BE COMPLETED BY THE SIGNATORY OR SIGNATORIES

I certify, in accordance with 37 CFR 1.4(d)(4) that I am:

(●) An attorney or agent registered to practice before the Patent and Trademark Office who is of record in this application

Registration Number 51167

( ) A sole inventor

( ) A joint inventor; I certify that I am authorized to sign this submission on behalf of all of the inventors as evidenced by the power of attorney in the application

( ) A joint inventor; all of whom are signing this request

Signature	/Jamie J. Zheng /
Name	Jamie J. Zheng

*Statement under 37 CFR 3.73(b) is required if terminal disclaimer is signed by the assignee (owner).
Form PTO/SB/96 may be used for making this certification. See MPEP § 324.

Electronic Patent Application Fee Transmittal

Application Number:	16412308
Filing Date:	14-May-2019
Title of Invention:	MEMORY MODULE WITH BUFFERED MEMORY PACKAGES
First Named Inventor/Applicant Name:	Hyun Lee
Filer:	Jamie Jie Zheng
Attorney Docket Number:	129980-5070-US01

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
STATUTORY OR TERMINAL DISCLAIMER	1814	1	160	160
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**160**

Doc Code: DISQ.E.FILE
Document Description: Electronic Terminal Disclaimer – Approved

Application No.: 16412308

Filing Date: 14-May-2019

Applicant/Patent under Reexamination: Lee

Electronic Terminal Disclaimer filed on September 9, 2020

☒ APPROVED

This patent is subject to a terminal disclaimer

☐ DISAPPROVED

Approved/Disapproved by: Electronic Terminal Disclaimer automatically approved by EFS-Web

U.S. Patent and Trademark Office

Electronic Acknowledgement Receipt

EFS ID:	40511162
Application Number:	16412308
International Application Number:	
Confirmation Number:	6765
Title of Invention:	MEMORY MODULE WITH BUFFERED MEMORY PACKAGES
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	129980-5070-US01
Receipt Date:	09-SEP-2020
Filing Date:	14-MAY-2019
Time Stamp:	19:31:08
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$160
RAM confirmation Number	E202099J31069122
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Terminal Disclaimer-Filed (Electronic)	eTerminal-Disclaimer.pdf	34976 7649e5961539427a109469f0a0109e5865fb ddc8	no	3
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30542 f2349ae351637c198552035143a2a465ac28 2778	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	65518		

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronically filed September 9, 2020

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun Lee	Confirmation No.:	6765
Serial No.:	16/412,308	Art Unit:	2827
Filed:	May 14, 2019	Examiner:	Hoang, Huan
For:	*Memory Module With Buffered Memory Packages*	Attorney Docket No.:	129980-5070-US01

RESPONSE TO FINAL OFFICE ACTION & INTERVIEW SUMMARY

Mail Stop: AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The enclosed Amendment is in response to the Final Office Action dated June 9, 2020 for the above identified patent application.

The Commissioner is hereby authorized to charge any required fee(s) to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5070-US01).

Petitioners
Ex. 1009, p. 206

McKesson Statement

In view of *McKesson Information Solutions v. Bridge Medical* (Fed. Cir. 2007), Applicant wishes to inform the Examiner that the prosecution history of the following US Patent Application(s) may contain information relevant to the pending application:

(1) U.S. Application Serial No. 15/470,856, filed March 27, 2017.

(2) U.S. Application Serial No. 13/970.606, filed August 20, 2013. This application issued as U.S. Patent No. 9,606,907.

The Examiner is encouraged to review the art made of record, office action(s) and the notice(s) of allowance, if any, in the above-mentioned application(s), all of which are available on PAIR.

Petitioners
Ex. 1009, p. 207

Electronic Acknowledgement Receipt

EFS ID:	40512220
Application Number:	16412308
International Application Number:	
Confirmation Number:	6765
Title of Invention:	MEMORY MODULE WITH BUFFERED MEMORY PACKAGES
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	129980-5070-US01
Receipt Date:	09-SEP-2020
Filing Date:	14-MAY-2019
Time Stamp:	19:35:08
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		129980-5070-US01_Amend.pdf	143916 17045cce7c62fbbef5a811f91f2ce0c5af03f38d	yes	10

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Applicant Arguments/Remarks Made in an Amendment	9	10
	Claims	4	8
	Specification	3	3
	Response After Final Action	1	2
Warnings:			
Information:			
	Total Files Size (in bytes):	143916	

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

REMARKS

This amendment responds to the final office action mailed June 9, 2020. In the final office action, the Examiner:

- rejected claims 2-21 on the ground of nonstatutory double patenting as being unpatentable over claims 1-4, 6, 7, 10 and 11 of U.S. Patent No. 10,290,328;
- rejected claims 2-21 on the ground of nonstatutory double patenting as being unpatentable over claims 1-11, 14 and 15 of U.S. Patent No. 9,659,601;
- rejected claims 2-21 on the ground of nonstatutory double patenting as being unpatentable over claims 10-20 of U.S. Patent No. 9,318,160; and
- rejected claims 2-21 on the ground of nonstatutory double patenting as being unpatentable over claims 29-34 of U.S. Patent No. 8,787,060.

REMARKS CONCERNING CLAIMS

Claims 2 and 11 have been amended for clarity of wording and to correct minor issues.

No new matter has been added.

Entry of the amendments is respectfully requested.

With respect to all amendments, Applicant has not dedicated or abandoned any unclaimed subject matter. Moreover, Applicant has not acquiesced to any characterizations of the invention, nor any rejections or objections of the claims, made by the Examiner. Moreover, the Applicant hereby rescinds any prior disclaimer of claim scope, to the extent they exist, made during the prosecution of this application or made during the prosecution of any patent or other related patents/applications, and advises the Examiner that any such previous disclaimers and the cited references that they were made to avoid may need to be revisited.

After entry of this amendment, the pending claims are: claims 2-21.

Petitioners
Ex. 1009, p. 210

REMARKS CONCERNING DOUBLE PATENTING REJECTIONS

Applicant submits herewith a terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d), which should overcome any actual or provisional rejection of claims 2-21 based on the nonstatutory obviousness-type double patenting ground over:

claims 1-4, 6, 7, 10 and 11 of U.S. Patent No. 10,290,328;
claims 1-11, 14 and 15 of U.S. Patent No. 9,659,601;
claims 10-20 of U.S. Patent No. 9,318,160; and/or
claims 29-34 of U.S. Patent No. 8,787,060.

Applicant's filing of the terminal disclaimer is for the sole purpose of advancing prosecution. It should not be understood as implying that Applicant agrees with the rejection of claims 2-21 on the ground of nonstatutory double patenting made in the Office Action.

CONCLUDING REMARKS

By responding in the foregoing remarks only to particular positions asserted by the examiner, the Applicant does not necessarily acquiesce in other positions that have not been explicitly addressed.

In light of the above amendments and remarks, the Applicant respectfully requests that the Examiner reconsider this application with a view towards allowance. The Examiner is invited to call the undersigned attorney at (650) 843-4000, if a telephone call could help resolve any remaining items.

Respectfully submitted,

Date: September 9, 2020

/ Jamie Zheng / 51,167

Jamie Zheng (Reg. No.)
MORGAN, LEWIS & BOCKIUS LLP
1400 Page Mill Road
Palo Alto, CA 94304
Phone: (650) 843-4000

Petitioners
Ex. 1009, p. 211

Amendments to the Claims

The following listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Cancelled)

2. (Currently Amended) A memory module operable in a computer system to communicate with a system memory controller via a command/address bus and a data bus, comprising:

a register device configurable to receive input command/address signals from the system memory controller via the command/address bus and to output control signals in response to the input command/address signals, the control signals including buffered command/address signals and data path control signals; and

a plurality of DRAM packages, each respective DRAM package comprising:

terminals including control terminals coupled to the register device and data terminals to be coupled to a respective section of the data bus, the control terminals including first control terminals and second control terminals;

stacked array dies; and

a control die coupled between the stacked array dies and the terminals of the respective DRAM package, the control die including data buffers and a data path control circuit; and

wherein the control die is configurable to:

receive the buffered command/address signals via the first control terminals and the data path control signals via the second control terminals;

[[pass]] provide at least some of the buffered command/address signals ~~through the control die~~ to the stacked array dies, ~~the buffered command/address signals~~ including providing respective chip-select signals ~~that are provided~~ to respective array dies of the stacked array dies; and

control the data buffers in response to the data path control signals to buffer data signals communicated between a selected array die of the stacked array dies and the respective section of the data bus, the selected array die having received one of the chip select signals that is different from any of the other ones of the chip select signals.

Petitioners
Ex. 1009, p. 212

3. (Previously Presented) The memory module of claim 2, wherein the register device is configurable to decode the input command/address signals and to generate the data path control signals in accordance with the input command/address signals.

4. (Previously Presented) The memory module of claim 2, wherein the data buffers are configurable to selectively isolate one or more array dies of the stacked array dies.

5. (Previously Presented) The memory module of claim 2, wherein the control die does not secondarily buffer the buffered command/address signals.

6. (Previously Presented) The memory module of claim 2, wherein the data path control circuit is configurable to control a command/address time slot for the buffered command/address signals passing through the control die.

7. (Previously Presented) The memory module of claim 2, wherein the data path control circuit is configurable to control a data bus time slot for the data signals.

8. (Previously Presented) The memory module of claim 2, wherein the buffered command/address signals include more chip select signals than the input command/address signals.

9. (Previously Presented) The memory module of claim 2, further comprising die interconnects including first die interconnects coupled to the data buffers and second die interconnects coupled to the control terminals, each of the first die interconnects being coupled to one or more of the stacked array dies.

10. (Previously Presented) The memory module of claim 9, wherein the data buffers include drivers coupled to respective ones of the first die interconnects, the drivers including a first driver coupled to one or more first array dies via a first die interconnect and a second driver and coupled to one or more second array dies via a second die interconnect, the first driver having a first driver size corresponding to a first capacitive load associated with the one or more first array dies and the first die interconnect, the second driver having a second driver size corresponding to a second capacitive load associated with the one or more second array dies and the second die interconnect.

Petitioners
Ex. 1009, p. 213

11. (Currently Amended) A memory module operable in a computer system to communicate with a system memory controller via a command/address bus and a data bus, comprising:

a register device configurable to receive input command/address signals from the system memory controller via the command/address bus, to buffer the input command/address signals, and to output control signals in response to the input command/address signals, the control signals including buffered command/address signals; and

a plurality of DRAM packages, each respective DRAM package comprising:

terminals including control terminals coupled to the register device and data terminals to be coupled to a respective section of the data bus, the control terminals including first control terminals and second control terminals;

stacked array dies; and

a control die coupled between the stacked array dies and the terminals of the respective DRAM package, the control die including data buffers and a data path control circuit; and

wherein the memory module is operable in any one of a plurality of modes including a first mode and a second mode;

wherein, during the first mode, the register device is configurable to generate data path control signals in response to receiving the input command/address signals, the control signals further include the data path control signals, and the control die is configurable to:

receive the buffered command/address signals via the first control terminals and the data path control signals via the second control terminals; and

[[pass]] provide at least some of the buffered command/address signals ~~through the control die~~ to the stacked array dies, ~~the buffered command/address signals~~ including providing respective chip-select signals ~~that are provided~~ to respective array dies of the stacked array dies;

wherein, during the second mode, the control die is configurable to:

receive the buffered command/address signals via the first control terminals;

generate data path control signals in response to the buffered command/address signals; and

provide secondarily buffered command/address signals to the stacked array dies, ~~the secondarily buffered command/address signals~~ including providing respective chip-select signals ~~that are provided~~ to respective array dies of the stacked array dies; and

Petitioners
Ex. 1009, p. 214

wherein, during the first mode or the second mode, the ~~control die is further~~ data path control circuit is configured to control the data buffers in response to the data path control signals ~~circuit~~ to buffer data signals communicated between a selected array die of the stacked array dies and the respective section of the data bus, the selected array die having received one of the chip select signals that is different from any of the other ones of the chip select signals.

12. (Previously Presented) The memory module of claim 11, wherein, during the second mode, the control die is configurable to generate data path control signals after decoding the buffered command/address signals.

13. (Previously Presented) The memory module of claim 12, wherein the secondarily buffered command/address signals include more chip select signals than the buffered command/address signals.

14. (Previously Presented) The memory module of claim 11, wherein the data buffers are configurable to selectively isolate one or more array dies of the stacked array dies.

15. (Previously Presented) The memory module of claim 11, wherein, during the first mode, the control die does not buffer at least some of the buffered command/address signals.

16. (Previously Presented) The memory module of claim 11, wherein the data path control circuit is configurable to control a command/address time slot for the buffered command/address signals passing through the control die.

17. (Previously Presented) The memory module of claim 11, wherein the data path control circuit is configurable to control a data bus time slot for the data signals.

18. (Previously Presented) The memory module of claim 11, further comprising die interconnects including first die interconnects coupled to the data buffers and second die interconnects coupled to the control terminals, each of the first die interconnects being coupled to one or more of the stacked array dies.

19. (Previously Presented) The memory module of claim 11, wherein the data buffers include drivers coupled to respective ones of the first die interconnects, the drivers including a first

Petitioners
Ex. 1009, p. 215

driver coupled to one or more first array dies via a first die interconnect and a second driver and coupled to one or more second array dies via a second die interconnect, the first driver having a first driver size corresponding to a first capacitive load associated with the one or more first array dies and the first die interconnect, the second driver having a second driver size corresponding to a second capacitive load associated with the one or more second array dies and the second die interconnect.

20. (Previously Presented) The memory module of claim 11, wherein the control die does not receive data path control signals from the register device via the second control terminals during the second mode.

21. (Previously Presented) The memory module of claim 11, wherein, during the first mode, the register device is configurable to perform rank multiplication, and wherein, during the second mode, the control die is configurable to perform rank multiplication.

Amendments to the Specification

Please revise the specification as follows:

Please amend paragraph numbers **[0092]** as follows:

[0092] The 3DS-DIMM proposal can also be compared to the HyperCloud™ (HC) DIMM architecture of Netlist, Inc. An example of the HCDIMM architecture 602 is illustrated in FIG. [[68]] 6B. Further details and embodiments of the HCDIMM architecture is disclosed in U.S. Pat. Nos. 7,289,386, 7,532,537, 7,619,912, and 7,636,274, each of which is incorporated in its entirety by reference herein. One of the main topological differences between the 3DS-DIMM and HCDIMM architectures is that while the 3DS-DIMM architecture uses a control die 722 to buffer the data signals and to decode command/address signals from the 3DS register, certain configurations of the HCDIMM architecture include a plurality of isolation devices (ID), each of which includes data buffers, but no decoding capability. Unlike the HCDIMM architecture, since the command/address signal needs to pass through the control die 722 in the 3DS DRAM package 720, the 3DSDIMM proposal presents the same shortcoming (b) of the controller die described above. The data path control signals are generated by the register device (RD) 612 in the HCDIMM architecture 602, while the data path control signals are generated by the control die 722 in the 3DS DRAM. This aspect of the 3DS-DIMM architecture creates timing critical control paths in 3DS-DIMM architecture.

Petitioners
Ex. 1009, p. 217

PTO/SB/06 (09-11)
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 16/412,308	Filing Date 05/14/2019	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $100 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $460 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

AMENDMENT	09/09/2020	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0		x $100 =	0
	Independent (37 CFR 1.16(h))	* 2	Minus	*** 3	= 0		x $460 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/DORIAN EVANS/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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NOTICE OF ALLOWANCE AND FEE(S) DUE

79141 7590 09/17/2020
Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304

EXAMINER
HOANG, HUAN

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 09/17/2020

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/412,308	05/14/2019	Hyun Lee	129980-5070-US01	6765

TITLE OF INVENTION: MEMORY MODULE WITH BUFFERED MEMORY PACKAGES

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0.00	$0.00	$1000	12/17/2020

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

79141 7590 09/17/2020
Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)

(Signature)

(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/412,308	05/14/2019	Hyun Lee	129980-5070-US01	6765

TITLE OF INVENTION: MEMORY MODULE WITH BUFFERED MEMORY PACKAGES

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0.00	$0.00	$1000	12/17/2020

EXAMINER	ART UNIT	CLASS-SUBCLASS
HOANG, HUAN	2827	365-063000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1_____
2_____
3_____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑Issue Fee ❑Publication Fee (if required) ❑Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

❑ Electronic Payment via EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/412,308	05/14/2019	Hyun Lee	129980-5070-US01	6765

79141 7590 09/17/2020
Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304

EXAMINER
HOANG, HUAN

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 09/17/2020

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 16/412,308	Applicant(s) Lee, Hyun	
	Examiner HUAN HOANG	Art Unit 2827	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to Response to final office action filed on 09/09/20.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 2-21 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☑ Notice of References Cited (PTO-892)
2. ☑ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☑ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/HUAN HOANG/
Primary Examiner, Art Unit 2827

Petitioners
Ex. 1009, p. 223

DETAILED ACTION

Notice of Pre-AIA or AIA Status

1. The present application is being examined under the pre-AIA first to invent provisions.

Information Disclosure Statement

2. The IDS filed on 06/08/2020 is the same as the IDS filed on 06/05/2020; therefore, only the IDS filed on 06/05/2020 has been considered.

Terminal Disclaimer

3. The terminal disclaimer filed on 09/09/20 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of US Patent Nos. 8,787,060, 9,318,160, 9,659,601 and 10,290,328 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to HUAN HOANG whose telephone number is (571)272-1779. The examiner can normally be reached on 7:30AM-4:00PM M-F.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an

interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, AMIR ZARABIAN can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see https://ppair-my.uspto.gov/pair/PrivatePair. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/HUAN HOANG/
Primary Examiner, Art Unit 2827

Notice of References Cited	Application/Control No. 16/412,308	Applicant(s)/Patent Under Reexamination Lee, Hyun	
	Examiner HUAN HOANG	Art Unit 2827	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-20140192583-A1	07-2014	Rajan; Suresh Natarajan	G11C5/06	365/63
	B					
	C					
	D					
	E					
	F					
	G					
	H					
	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/412,308	Lee, Hyun
	Examiner	**Art Unit**
	HUAN HOANG	2827

CPC - Searched*		
Symbol	**Date**	**Examiner**
G11C 5/066, G11C 5/06, G11C 7/1057, G11C 7/1094, G11C 7/12	09/29/2019	HH
Above Updated	06/04/2020	HH
Above Updated	09/12/2020	HH

CPC Combination Sets - Searched*		
Symbol	**Date**	**Examiner**

US Classification - Searched*			
Class	**Subclass**	**Date**	**Examiner**
365	63	09/29/2019	HH
Above	Updated	06/04/2020	HH
Above	Updated	09/12/2020	HH

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	**Date**	**Examiner**
EAST (text search)	09/29/2019	HH
Assignee and Inventor search	09/29/2019	HH
EAST (text search)	06/04/2020	HH
Assignee and Inventor search	06/04/2020	HH
EAST (text search)	09/12/2020	HH
Assignee and Inventor search	09/12/2020	HH

/HUAN HOANG/ Primary Examiner, Art Unit 2827	

Petitioners
Ex. 1009, p. 227

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/412,308	Lee, Hyun
	Examiner	**Art Unit**
	HUAN HOANG	2827

Interference Search			
US Class/CPC Symbol	**US Subclass/CPC Group**	**Date**	**Examiner**
	EAST (US-PGPUB)	09/12/2020	HH

/HUAN HOANG/ Primary Examiner, Art Unit 2827	

Petitioners
Ex. 1009, p. 228

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/412,308	Lee, Hyun
	Examiner	**Art Unit**
	HUAN HOANG	2827

CPC

Symbol					Type	Version
G11C	/	5	/	066	F	2013-01-01
G11C	/	5	/	06	I	2013-01-01
G11C	/	7	/	1057	I	2013-01-01
G11C	/	7	/	1084	I	2013-01-01
G11C	/	7	/	12	I	2013-01-01

CPC Combination Sets

Symbol					Type	Set	Ranking	Version
	/		/					

NONE (Assistant Examiner) (Date)		**Total Claims Allowed:** 20	
/HUAN HOANG/ Primary Examiner, Art Unit 2827 (Primary Examiner) (Date)	12 September 2020	O.G. Print Claim(s) 1	O.G. Print Figure 7

U.S. Patent and Trademark Office

Part of Paper No.: 20200912

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/412,308	Lee, Hyun
	Examiner	**Art Unit**
	HUAN HOANG	2827

INTERNATIONAL CLASSIFICATION				
CLAIMED				
G11C	/	5	/	06

NON-CLAIMED				
	/		/	

US ORIGINAL CLASSIFICATION	
CLASS	**SUBCLASS**

CROSS REFERENCES(S)						
CLASS	**SUBCLASS (ONE SUBCLASS PER BLOCK)**					

NONE (Assistant Examiner) (Date)		**Total Claims Allowed:** 20	
/HUAN HOANG/ Primary Examiner, Art Unit 2827 (Primary Examiner) (Date)	12 September 2020	O.G. Print Claim(s) 1	O.G. Print Figure 7

U.S. Patent and Trademark Office

Part of Paper No.: 20200912

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/412,308	Lee, Hyun
	Examiner	**Art Unit**
	HUAN HOANG	2827

☑ Claims renumbered in the same order as presented by applicant ☐ CPA ☑ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	2		11		20										
	3		12		21										
	4		13												
	5		14												
	6		15												
	7		16												
	8		17												
	9		18												
	10		19												

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 20	
/HUAN HOANG/ Primary Examiner, Art Unit 2827 (Primary Examiner)	12 September 2020 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 7

U.S. Patent and Trademark Office

Part of Paper No.: 20200912

Bibliographic Data

Application No: 16/412,308

Foreign Priority claimed: ○ Yes ◉ No

35 USC 119 (a-d) conditions met: ☐ Yes ☑ No ☐ Met After Allowance

Verified and Acknowledged: /HUAN HOANG/ (Examiner's Signature) [ ] (Initials)

Title: MEMORY MODULE WITH BUFFERED MEMORY PACKAGES

FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
05/14/2019 **RULE**	365	2827	129980-5070-US01

APPLICANTS

NETLIST, INC., Irvine, CA,

INVENTORS

Hyun Lee, Ladera Ranch, CA, UNITED STATES

CONTINUING DATA

This application is a CON of 15602099 05/22/2017 PAT 10290328

15602099 is a CON of 15095288 04/11/2016 PAT 9659601

15095288 is a CON of 14337168 07/21/2014 PAT 9318160

14337168 is a CON of 13288850 11/03/2011 PAT 8787060

13288850 has PRO of 61409893 11/03/2010

FOREIGN APPLICATIONS

IF REQUIRED, FOREIGN LICENSE GRANTED**

05/22/2019

STATE OR COUNTRY

UNITED STATES

ADDRESS

Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304
UNITED STATES

FILING FEE RECEIVED

$2,080

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed June 5, 2020	
				Application Number	16/412,308
				Filing Date	May 14, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2827
				Examiner Name	Hoang, Huan
Sheet	1	of	11	Attorney Docket Number	129980-5070US01

U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.	Document Number Number - Kind Code	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		5,784,705	07-21-1998	Leung	
		5,905,401	05-18-1999	Sher	
		6,070,217	05-30-2000	Connolly et al.	
		6,683,372 B1	01-27-2004	Wong et al.	
		6,704,910 B2	03-09-2004	Hong	
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		7,289,386 B2	10-30-2007	Bhakta et al.	
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		2005/0281096 A1	12-22-2005	Bhakta et al.	
		2006/0117152 A1	06-01-2006	Amidi et al.	
		2006/0262586 A1	11-23-2006	Solomon et al.	
		2006/0277355 A1	12-07-2006	Ellsberry et al.	
		2008/0025137 A1	01-31-2008	Rajan et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials	Cite No.	Foreign Patent Document Country Code – Number - Kind Code *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T
		CN 102576565 B	09-30-2015	Netlist, Inc.		

NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
		Response, Article 94 3 EPC, EP 18179414.0, 6AUG2019, 23 pgs
		Netlist, Inc., Third Party Observation, EP 3404660, 6AUG2019, 34 pgs
		Office Action, EP 18179414, 2APR2019, 6 pgs
		Patent document filed by third party, EP 18179414, 22FEB2019, 10 pgs

Examiner Signature		Date Considered	

DB2/ 22684197.4

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.H/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed June 5, 2020	
				Application Number	16/412,308
				Filing Date	May 14, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2827
				Examiner Name	Hoang, Huan
Sheet	2	of	11	Attorney Docket Number	129980-5070US01

		Observations by third parties, EP 18179414.0, 22FEB2019, 1 pg
		Patent Document filed by a third party, 20FEB2019, 10 pgs
		Netlist, Inc., Observations by third parties, EP 3404660, 20FEB2019, 46 pgs
		Reply to Written Opinion prepared by the EPO, EP 18179414.0, 17JAN2019, 20 pgs
		Netlist, Inc., Information on Search Strategy, EP 18179414, 23OCT2018, 1 pg
		European Search Report, EP 18179414, 23OCT2018, 3 pgs
		European Search Opinion, EP 18179414, 23OCT2018, 3 pgs
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, PAPER 14, 'Patent Owner's Response,' filed October 19,2018
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1047, 'Certified translation of the Examination Decision issued by the State Intellectual Property Office of the P.R.C. (dated 5/30/18),' filed February 11,2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1048, 'Certified translation of the Preliminary Opinion issued by the German Patent and Trademark Office (dated 1/8/19),' filed February 11,2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, PAPER 19, 'Petitioners' Request for Oral Argument,' filed February 19,2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, PAPER 21, 'Patent Owner Objections To Reply Evidence,' filed February 19,2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, PAPER 20, 'Patent Owner Request For Oral Argument,' filed February 19,2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, PAPER 22, 'Patent Owner Motion To Exclude,' filed February 19,2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, PAPER 23, 'Corrected Petitioners' Reply to Patent Owner's Response,' filed February 20,2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, PAPER 28, 'Order - Trial Hearing,' filed March 22,2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, PAPER 29, 'Termination Decision Document,' filed June 27,2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, PAPER 30, 'Record of Oral Hearing,' filed June 27,2019
		Netlist, Inc., Examination Decision of Request for Invalidation, CN201080039043.0, 30MAY2018, 43 pgs.

Examiner Signature		Date Considered	

DB2/ 22684197.4

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.H/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed June 5, 2020	
				Application Number	16/412,308
				Filing Date	May 14, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2827
				Examiner Name	Hoang, Huan
Sheet	3	of	11	Attorney Docket Number	129980-5070US01

		Inter Partes Review of US Patent No. 8,516,185 B2, Case No. IPR2017-00577, Record of Oral Hearing, filed June 19, 2018.
		Inter Partes Review of US Patent No. 8,516,185 B2, Case No. IPR2017-00577, Final Written Decision, filed July 5, 2018.
		Inter Partes Review of US Patent No. 7,532,537 B2, Case No. IPR2017-00667, Final Written Decision, filed July 18, 2018
		Inter Partes Review of US Patent No. 7,532,537 B2, Case No. IPR2017-00668, Final Written Decision, filed July 18, 2018.
		Inter Partes Review of US Patent No. 9,606,907 B2, Case No. IPR2018-00362, ORDER, *Conduct of the Proceedings*, filed August 2, 2018
		Inter Partes Review of US Patent No. 9,606,907 B2, Case No. IPR2018-00362, and Case No. IPR2018-00363, Decision Granting Institution of *Inter Partes* Review, filed August 6, 2018
		Inter Partes Review of US Patent No. 9,606,907 B2, Case No. IPR2018-00362, and Case No. IPR2018-00363, EXHIBIT 3001, 'email from Mehran Arjomand,' filed July 30, 2018
		Inter Partes Review of US Patent No. 9,606,907 B2, Case No. IPR2018-00362, and Case No. IPR2018-00363, EXHIBIT 3001, 'email from Michael D. Hatcher,' filed July 30, 2018
		Inter Partes Review of US Patent No.9,606,907 B2, Case No. IPR2018-00364, and Case No. IPR2018-00365, Decision Granting Institution of *Inter Partes* Review, filed June 29, 2018
		Inter Partes Review of US Patent No.9,606,907 B2, Case No. IPR2018-00364, Patent Owner's Objections to Petition Evidence, filed August 20, 2018
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Patent Owner's Preliminary Response, filed April, 9, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1003, 'Declaration of Dr. Harold Stone,' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1009, 'JEDEC Standard Double Data Rate DDR SDRAM Specification, JESD79 June 2000,' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1010, 'JEDEC Standard 21-C, DDR SDRAM Registered DIMM Design Specification January 2002,' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1011, 'JEDEC Standard DDR2 SDRAM Specification, JESD79-2B January 2005,' filed December, 22, 2017

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed June 5, 2020	
				Application Number	16/412,308
				Filing Date	May 14, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2827
				Examiner Name	Hoang, Huan
Sheet	4	of	11	Attorney Docket Number	129980-5070US01

		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1012, 'Declaration of John J. Kelly Regarding Records of Joint Electron Device Engineering Council JEDEC,' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1022, 'Decision Denying Institution of Inter Partes Review of U.S. Patent No. 8,516,185, SanDisk Corp. v. Netlist, Inc., IPR2014-01029, Paper No. 11 Dec. 16, 2014,' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1023, 'Decision Denying Institution of Inter Partes Review of U.S. Patent No. 8,516,185, Smart Modular Techs. Inc. v. Netlist, Inc., IPR2014-01369, Paper No. 12 Mar. 9, 2015,' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1024, 'Excerpts from the Hearing in Certain Memory Modules and Components Thereof, and Products Containing Same, Inv. No. 337-TA-1023 May 8, 2017,' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1025, 'Complainant Netlist, Inc.'s Initial Post-Hearing Brief, Certain Memory Modules and Components Thereof, and Products Containing Same, Inv. No. 337-TA-1023 May 30, 2017 excerpts relevant to '185 patent,' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1026, 'Respondents' Post-Hearing Brief, Certain Memory Modules and Components Thereof, and Products Containing Same, Inv. No. 337-TA-1023 May 30, 2017 excerpts relevant to '185 patent,' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1027, 'High-quality versions of demonstrative graphics included in Respondents' Post-Hearing Brief (Ex.1026),' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1028, 'Complainant Netlist Inc.'s Reply Post-Hearing Brief, Certain Memory Modules and Components Thereof, and Products Containing Same, Inv. No. 337-TA-1023 (June 9, 2017) (excerpts relevant to '185 patent),' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1029, 'Respondents' Reply Post-Hearing Brief, Certain Memory Modules and Components Thereof, and Products Containing Same, Inv. No. 337-TA-1023 (June 9, 2017) (excerpts relevant to '185 patent),' filed December, 22, 2017

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed June 5, 2020	
				Application Number	16/412,308
				Filing Date	May 14, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2827
				Examiner Name	Hoang, Huan
Sheet	5	of	11	Attorney Docket Number	129980-5070US01

		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1030, 'High-quality versions of demonstrative graphics included in Respondents' Reply Post-Hearing Brief (Ex.1029),' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1031, 'Institution of Inter Partes Review of U.S. Patent No. 8,516,185, SK hynix Inc. et al. v. Netlist, Inc., IPR2017-00577, Paper No. 8 (July 7, 2017),' filed December, 22, 2017.
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1032, 'Final Written Decision, Diablo Techs., Inc. v. Netlist, Inc., IPR2014-00882, Paper No. 33 (Dec. 14, 2015),' filed December, 22, 2017.
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1033, 'Netlist, Inc. v. Diablo Techs., Inc., No. 2016-1742 (Fed. Cir. July 25, 2017),' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1034, 'Netlist's Infringement Claim Chart for U.S. Patent No. 9,606,907 June 14, 2017,' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1035, 'Stone, H.S. Microcomputer Interfacing, Reading, MA: Addison Wesley, 1982,' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1039, 'Intel E7525 Memory Controller Hub (MCH) Chipset Datasheet (June 2004),' filed December, 22, 2017
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed June 5, 2020	
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				First Named Inventor	Hyun Lee
				Art Unit	2827
				Examiner Name	Hoang, Huan
Sheet	6	of	11	Attorney Docket Number	129980-5070US01

		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Petition for Review of U.S. Patent No. 9,606,907, filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Preliminary Response, filed April 10, 2018
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00364, Petition for Inter Partes Review of U.S. Patent No. 9,606,907, filed December, 27, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00365, Petition for Inter Partes Review of U.S. Patent No. 9,606,907, filed December, 27, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petition for Inter Partes Review, filed December, 30, 2016
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Patent Owner's Preliminary Response, filed April, 9, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Patent Owner's Response, filed September, 15, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petitioners' Objections to Evidence, filed September, 22, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petitioners Motion to Exclude Certain Inadmissible Testimony of Patent Owners Expert Carl Sechen, filed January, 9, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petitioners Request for Oral Hearing, filed January, 9, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, PO Request for Oral Argument, filed January, 9, 2018
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		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petitioners' Response to Patent Owner's Motion for Observations, filed January, 23, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, PO's Opposition to Petitioner's Motion to Exclude, filed January, 23, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petitioners' Reply In Support Of Motion to Exclude Certain Inadmissible Testimony Of Patent Owner's Expert Carl Sechen, filed January, 30, 2018

Examiner Signature		Date Considered	

DB2/ 22684197.4

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed June 5, 2020	
				Application Number	16/412,308
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				Art Unit	2827
				Examiner Name	Hoang, Huan
Sheet	7	of	11	Attorney Docket Number	129980-5070US01

		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petitioners' Updated Exhibit List, filed February, 9, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Patent Owner's Updated Exhibit List, filed February, 9, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Trial Instituted Document, filed May, 15, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, ORDER Trial Hearing, filed January, 25, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Hearing Transcript, filed March, 22, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Final Written Decision, filed May 3, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 1002, 'Excerpts of FH for U.S. Patent 8,756,364,' filed December, 30, 2016
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 1003, 'Declaration of Harold Stone,' filed December, 15, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 1007, 'JEDEC JESD79 publication (June 2000),' filed December, 30, 2016
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 1008, 'JEDEC Declaration for DDR Specification,' filed December, 30, 2016
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 1015, 'Texas Instruments 74LS245 datasheet (2002),' filed December, 30, 2016
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 1017, '2000-03 Samsung CMOS SDRM data sheet,' filed September, 15, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 1019, 'Final Decision [IPR2014-01011],' filed September, 15, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 1020, 'Final Decision [IPR2014-00883],' filed December, 30, 2016
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 1023, 'Gordon_Moore_1965_article,' filed December, 30, 2016

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DB2/ 22684197.4

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed June 5, 2020	
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				Art Unit	2827
				Examiner Name	Hoang, Huan
Sheet	8	of	11	Attorney Docket Number	129980-5070US01

		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 1024, 'Deposition Transcript of Carl Sechen (Dec. 8, 2017),' filed December, 15, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 1025, 'Supplemental Declaration of Harold S. Stone (Dec. 15, 2017),' filed December, 15, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 1026, 'Xilinx CoolRunner XPLA3 CPLD product specification (2000),' filed December, 15, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 1027, 'Xilinx Programmable Logic Design Quick Start Handbook (2004),' filed January, 9, 2018
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		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 1029, 'Xilinx VQFP package datasheet (2002),' filed February, 9, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 1030, 'Xilinx CS280 package datasheet (1999),' filed December, 15, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 1031, 'Petitioners Demonstratives,' filed April, 9, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 2001, 'Exhibit 2001,' filed December, 15, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 2002, 'Exhibit 2002,' filed December, 15, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 2003, 'Exhibit 2003,' filed February, 9, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 2004, 'Exhibit 2004,' filed December, 30, 2016
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 2005, 'Exhibit 2005,' filed September, 15, 2017
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Patent Owner's Preliminary Response, filed April, 10, 2017
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Petitioners' Updated Exhibit List, filed June, 21, 2017
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Patent Owner's Response, filed October, 25, 2017

Examiner Signature		Date Considered	

DB2/ 22684197.4

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed June 5, 2020	
				Application Number	16/412,308
				Filing Date	May 14, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2827
				Examiner Name	Hoang, Huan
Sheet	9	of	11	Attorney Docket Number	129980-5070US01

		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Petitioners' Objections to Evidence, filed October, 31, 2017
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Petitioners' Reply to Patent Owner's Response, filed February, 6, 2018
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Patent Owner's Objections to Evidence, filed February, 13, 2018
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Petitioners' Request for Oral Hearing, filed February, 28, 2018
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Patent Owner's Request for Oral Argument, filed February, 28, 2018
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Patent Owner's Motion to Exclude, filed February, 28, 2018
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Petitioners' Opposition to Patent Owner's Motion to Exclude, filed March, 14, 2018
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Patent Owner's Reply to Petitioner's Opposition to Motion to Exclude, filed March, 21, 2018
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Notice of Accord Filing Date, filed January, 10, 2017
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Trial Instituted Document, filed July, 7, 2017
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Order - Request for Oral Argument - 37 CFR 42.70, filed April, 2, 2018
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, EXHIBITS 1003, 'Declaration of Harold S. Stone,' filed January, 5, 2017
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, EXHIBITS 1007, 'JEDEC JESD79 publication (June 2000),' filed January, 5, 2017
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, EXHIBITS 1009, 'TI 74LS245 datasheet (2002),' filed April, 10, 2017
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, EXHIBITS 1010, 'JEDEC Declaration,' filed January, 5, 2017

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		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, EXHIBITS 1011, 'IPR2014-01369 08-23-2014 Petition for Inter Partes Review,' filed January, 5, 2017
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, EXHIBITS 1012, 'IPR2014-01029 06-24-2014 Petitioner for Inter Partes Review,' filed April, 10, 2017
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, EXHIBITS 1025, 'US Patent Application Publication 2011/0016250,' filed June, 21, 2017
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, EXHIBITS 1026, 'Netlist's post-hearing brief,' filed June, 21, 2017
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, EXHIBITS 1027, 'Hynix's post-hearing brief,' filed October, 25, 2017
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, EXHIBITS 1028, 'Demonstrative Graphics from hynix's post-hearing brief,' filed October, 25, 2017
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, EXHIBITS 1029, 'Netlist's reply post-hearing brief,' filed October, 25, 2017
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, EXHIBITS 1030, 'hynix's reply post-hearing brief,' filed June, 21, 2017
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, EXHIBITS 1031, 'Demonstrative Graphics from hynix's reply post-hearing brief,' filed June, 21, 2017
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, EXHIBITS 2001, 'Exhibit 2001,' filed June, 21, 2017
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, EXHIBITS 2002, 'Exhibit 2002,' filed June, 21, 2017
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, EXHIBITS 2003, 'Exhibit 2003,' filed October, 25, 2017
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, EXHIBITS 2004, 'Exhibit 2004,' filed October, 25, 2017
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, EXHIBITS 2005, 'Exhibit 2005,' filed December, 30, 2016
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, EXHIBITS 2006, 'Exhibit 2006,' filed December, 30, 2016
		Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, EXHIBITS 2007, 'Exhibit 2007,' filed December, 30, 2016

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DB2/ 22684197.4

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				Art Unit	2827
				Examiner Name	Hoang, Huan
Sheet	11	of	11	Attorney Docket Number	129980-5070US01

Examiner Signature	/HUAN HOANG/	Date Considered	09/12/2020

DB2/ 22684197.4

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	35,970	(G11C5/066 or G11C7/12 or G11C5/06 or G11C7/1057 or G11C7/1084).cpc. 365/063,63.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/12 10:51
L2	1,913	1 and register with (command address) with control$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/12 10:53
L3	384	2 and stack$3 with (die dice chip ic integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/12 10:56
L4	29	3 and (dram sdram dynamic adj ram dynamic adj random) near3 package	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/12 10:57
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L7	15	6 and chip adj2 (select enabl$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/12 11:14
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L11	7	9 and stack$3 with (die dice chip ic integrated adj circuit) with package	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/12 11:21
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L13	19	12 and (dram sdram dynamic adj ram dynamic adj random) near3 packages	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/09/12 11:22
L14	14	13 and stack$3 with (die dice chip ic integrated adj circuit) with package	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/12 11:23
L15	107,152	(memory storage) and register with (command address) with control$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/12 11:25
L16	21	("20020112119" | "20030070052" | "20050281096" | "20060117152" | "20060262586" | "20060277355" | "20080025137" | "5784705" | "5905401" | "6070217" | "6683372" | "6704910" | "6721860" | "7024518" | "7289386" | "7334150" | "7532537" | "8081536" |	US-PGPUB; USPAT	OR	ON	2020/09/12 11:25

		"8130560" | "8417870" | "8756364").PN.				
L19	88,398	15 16	US-PGPUB; USPAT	OR	ON	2020/09/12 11:39
L20	25,370	19 and register with control$4 adj3 signal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/12 11:40
L21	553	20 and stack$3 with (die dice chip ic integrated adj circuit) with package	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/09/12 11:40
L22	32	20 and (dram sdram dynamic adj ram dynamic adj random) near3 packages	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/09/12 11:41
L23	16	21 and 22	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/09/12 11:41
L24	2,430,810	netlist.as. lee.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/09/12 11:44
L25	5,156	24 and memory with module with controller	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/09/12 11:44
L26	84	25 and register with control adj signal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/09/12 11:45
L27	1	26 and dram with package	US-PGPUB; USPAT; USOCR; FPRS;	OR	OFF	2020/09/12 11:45

			EPO; JPO; DERWENT; IBM_TDB			
L29	19	25 and register with (address command) with register with data adj3 signal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/09/12 11:47
L30	2	29 and stack$3 with (die dice)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/09/12 11:48

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L31	0	(memory and module and register and data and path and dram and package and stack$3 and die and buffer and chip and select and communicat$3).clm.	US-PGPUB; USPAT	OR	OFF	2020/09/12 11:55
L32	2	(memory and module and register and data and path and dram and package and stack$3 and die and buffer and chip and select).clm.	US-PGPUB; USPAT	OR	OFF	2020/09/12 11:56
L33	0	(memory and module and register and address and command and path and dram and package and stack$3 and die and buffer and communicat$3).clm.	US-PGPUB; USPAT	OR	OFF	2020/09/12 11:57

9/12/2020 11:58:19 AM

Receipt date: 09/09/2020

OK TO ENTER: /H.H/

09/11/2020

Electronically filed September 9, 2020

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun Lee	Confirmation No.:	6765
Serial No.:	16/412,308	Art Unit:	2827
Filed:	May 14, 2019	Examiner:	Hoang, Huan
For:	*Memory Module With Buffered Memory Packages*	Attorney Docket No.:	129980-5070-US01

RESPONSE TO FINAL OFFICE ACTION & INTERVIEW SUMMARY

Mail Stop: AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The enclosed Amendment is in response to the Final Office Action dated June 9, 2020 for the above identified patent application.

The Commissioner is hereby authorized to charge any required fee(s) to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5070-US01).

Petitioners
Ex. 1009, p. 248

McKesson Statement

In view of *McKesson Information Solutions v. Bridge Medical* (Fed. Cir. 2007), Applicant wishes to inform the Examiner that the prosecution history of the following US Patent Application(s) may contain information relevant to the pending application:

(1) U.S. Application Serial No. 15/470,856, filed March 27, 2017.

(2) U.S. Application Serial No. 13/970.606, filed August 20, 2013. This application issued as U.S. Patent No. 9,606,907.

The Examiner is encouraged to review the art made of record, office action(s) and the notice(s) of allowance, if any, in the above-mentioned application(s), all of which are available on PAIR.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed June 8, 2020	
				Application Number	16/412,308
				Filing Date	May 14, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2827
				Examiner Name	Hoang, Huan
Sheet	1	of	11	Attorney Docket Number	129980-5070US01

U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.	Document Number Number - Kind Code	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		5,784,705	07-21-1998	Leung	
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Examiner Initials	Cite No.	Foreign Patent Document Country Code - Number - Kind Code *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T
		CN 102576565 B	09-30-2015	Netlist, Inc.		

NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
		Response, Article 94 3 EPC, EP 18179414.0, 6AUG2019, 23 pgs
		Netlist, Inc., Third Party Observation, EP 3404660, 6AUG2019, 34 pgs
		Office Action, EP 18179414, 2APR2019, 6 pgs
		Patent document filed by third party, EP 18179414, 22FEB2019, 10 pgs

Examiner Signature		Date Considered	

DB2/ 22684197.4

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed June 8, 2020	
				Application Number	16/412,308
				Filing Date	May 14, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2827
				Examiner Name	Hoang, Huan
Sheet	2	of	11	Attorney Docket Number	129980-5070US01

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		Netlist, Inc., Observations by third parties, EP 3404660, 20FEB2019, 46 pgs
		Reply to Written Opinion prepared by the EPO, EP 18179414.0, 17JAN2019, 20 pgs
		Netlist, Inc., Information on Search Strategy, EP 18179414, 23OCT2018, 1 pg
		European Search Report, EP 18179414, 23OCT2018, 3 pgs
		European Search Opinion, EP 18179414, 23OCT2018, 3 pgs
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		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1047, 'Certified translation of the Examination Decision issued by the State Intellectual Property Office of the P.R.C. (dated 5/30/18),' filed February 11,2019
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		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, PAPER 19, 'Petitioners' Request for Oral Argument,' filed February 19,2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, PAPER 21, 'Patent Owner Objections To Reply Evidence,' filed February 19,2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, PAPER 20, 'Patent Owner Request For Oral Argument,' filed February 19,2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, PAPER 22, 'Patent Owner Motion To Exclude,' filed February 19,2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, PAPER 23, 'Corrected Petitioners' Reply to Patent Owner's Response,' filed February 20,2019
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, PAPER 28, 'Order - Trial Hearing,' filed March 22,2019
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Examiner Signature		Date Considered	

DB2/ 22684197.4

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed June 8, 2020	
				Application Number	16/412,308
				Filing Date	May 14, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2827
				Examiner Name	Hoang, Huan
Sheet	3	of	11	Attorney Docket Number	129980-5070US01

		Inter Partes Review of US Patent No. 8,516,185 B2, Case No. IPR2017-00577, Record of Oral Hearing, filed June 19, 2018.
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Examiner Signature		Date Considered	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed June 8, 2020	
				Application Number	16/412,308
				Filing Date	May 14, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2827
				Examiner Name	Hoang, Huan
Sheet	4	of	11	Attorney Docket Number	129980-5070US01

		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1012, 'Declaration of John J. Kelly Regarding Records of Joint Electron Device Engineering Council JEDEC,' filed December, 22, 2017
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		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1023, 'Decision Denying Institution of Inter Partes Review of U.S. Patent No. 8,516,185, Smart Modular Techs. Inc. v. Netlist, Inc., IPR2014-01369, Paper No. 12 Mar. 9, 2015,' filed December, 22, 2017
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Examiner Signature		Date Considered	

DB2/ 22684197.4

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed June 8, 2020	
				Application Number	16/412,308
				Filing Date	May 14, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2827
				Examiner Name	Hoang, Huan
Sheet	5	of	11	Attorney Docket Number	129980-5070US01

		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1030, 'High-quality versions of demonstrative graphics included in Respondents' Reply Post-Hearing Brief (Ex.1029),' filed December, 22, 2017
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Examiner Signature		Date Considered	

DB2/ 22684197.4

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed June 8, 2020	
				Application Number	16/412,308
				Filing Date	May 14, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2827
				Examiner Name	Hoang, Huan
Sheet	6	of	11	Attorney Docket Number	129980-5070US01

		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Petition for Review of U.S. Patent No. 9,606,907, filed December, 22, 2017
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		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00364, Petition for Inter Partes Review of U.S. Patent No. 9,606,907, filed December, 27, 2017
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		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petition for Inter Partes Review, filed December, 30, 2016
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Patent Owner's Preliminary Response, filed April, 9, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Patent Owner's Response, filed September, 15, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petitioners' Objections to Evidence, filed September, 22, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petitioners Motion to Exclude Certain Inadmissible Testimony of Patent Owners Expert Carl Sechen, filed January, 9, 2018
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		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, PO Request for Oral Argument, filed January, 9, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, PO Motion for Observations, filed January, 9, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petitioners' Response to Patent Owner's Motion for Observations, filed January, 23, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, PO's Opposition to Petitioner's Motion to Exclude, filed January, 23, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petitioners' Reply In Support Of Motion to Exclude Certain Inadmissible Testimony Of Patent Owner's Expert Carl Sechen, filed January, 30, 2018

Examiner Signature		Date Considered	

DB2/ 22684197.4

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed June 8, 2020	
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				First Named Inventor	Hyun Lee
				Art Unit	2827
				Examiner Name	Hoang, Huan
Sheet	7	of	11	Attorney Docket Number	129980-5070US01

		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petitioners' Updated Exhibit List, filed February, 9, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Patent Owner's Updated Exhibit List, filed February, 9, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Trial Instituted Document, filed May, 15, 2017
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		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Hearing Transcript, filed March, 22, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Final Written Decision, filed May 3, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 1002, 'Excerpts of FH for U.S. Patent 8,756,364,' filed December, 30, 2016
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 1003, 'Declaration of Harold Stone,' filed December, 15, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 1007, 'JEDEC JESD79 publication (June 2000),' filed December, 30, 2016
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		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBITS 1020, 'Final Decision [IPR2014-00883],' filed December, 30, 2016
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Examiner Signature		Date Considered	

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Sheet	8	of	11	Attorney Docket Number	129980-5070US01

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Examiner Signature		Date Considered	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed June 8, 2020	
				Application Number	16/412,308
				Filing Date	May 14, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2827
				Examiner Name	Hoang, Huan
Sheet	9	of	11	Attorney Docket Number	129980-5070US01

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed June 8, 2020	
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				Filing Date	May 14, 2019
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				Art Unit	2827
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Sheet	10	of	11	Attorney Docket Number	129980-5070US01

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				Art Unit	2827
				Examiner Name	Hoang, Huan
Sheet	11	of	11	Attorney Docket Number	129980-5070US01

Examiner Signature		Date Considered	

DB2/22684197.4

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/412,308	05/14/2019	Hyun Lee	129980-5070-US01	6765

79141 7590 11/23/2020
Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304

EXAMINER
HOANG, HUAN

ART UNIT	PAPER NUMBER
2827	

NOTIFICATION DATE	DELIVERY MODE
11/23/2020	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

padocketingdepartment@morganlewis.com
vskliba@morganlewis.com

Corrected ***Notice of Allowability***	**Application No.** 16/412,308	**Applicant(s)** Lee, Hyun	
	Examiner HUAN HOANG	**Art Unit** 2827	**AIA (FITF) Status** No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to the Response filed on 09/09/20.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 2-21 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☑ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☑ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/HUAN HOANG/
Primary Examiner, Art Unit 2827

Petitioners
Ex. 1009, p. 262

DETAILED ACTION

Notice of Pre-AIA or AIA Status

1. The present application is being examined under the pre-AIA first to invent provisions.

Information Disclosure Statement

2. The document “KIM et al., "A Quantitative Analysis of Performance Benefits of 30 Die Stacking on Mobile and Embedded Soc” in the information disclosure statement filed 08/21/2019 fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 because it does not provide the publication date. It has been placed in the application file, but the information referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609.05(a).

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to HUAN HOANG whose telephone number is (571)272-1779. The examiner can normally be reached on 7:30AM-4:00PM M-F.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, AMIR ZARABIAN can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see https://ppair-my.uspto.gov/pair/PrivatePair. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/HUAN HOANG/
Primary Examiner, Art Unit 2827

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed August 21, 2019	
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Sheet	1	of	14	Attorney Docket Number	129980-5070US01

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Examiner Signature		Date Considered	

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.L./

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NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
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				Application Number	16/412,308
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				First Named Inventor	Hyun Lee
				Art Unit	2827
				Examiner Name	To be assigned
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				Art Unit	2827
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Sheet	6	of	14	Attorney Docket Number	129980-5070US01

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				Examiner Name	To be assigned
Sheet	7	of	14	Attorney Docket Number	129980-5070US01

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Sheet	8	of	14	Attorney Docket Number	129980-5070US01

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		Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Exhibit 2001, "Declaration of Professor Carl Sechen," filed February 22, 2016
		International Search Report and Written Opinion, International Application No. PCT/US14/48517, filed July 28, 2014, dated October 27, 2014
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		Notice of Allowance, U.S. Pat. Appl. No. 13/970,606, filed August 20, 2013, dated June 27, 2016
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		Inter Partes Review Case No. 2014-00882, Patent Owner Response, filed May 8, 2015
		Inter Partes Review Case No. 2014-00882, Petitioner Diablo Technologies, Inc.'s Reply to Patent Owner Netlist, Inc.'s Response, filed June 19, 2015
		Inter Partes Review Case No. 2014-00882, Petitioner's Request for Oral Argument, filed July 1, 2015
		Inter Partes Review Case No. 2014-00882, Patent Owner's Request for Oral Argument, filed July 3,2015
		Inter Partes Review Case No. 2014-00882, Order - Request for Oral Argument - 37 C.F.R. 42.70, filed July 10, 2015
		Inter Partes Review Case No. 2014-00882, Record of Oral Hearing, filed November 16, 2015
		Inter Partes Review Case No. 2014-00882, Final Written Decision 35 USC 318 and 37 CFR 42.73, filed December 14, 2015
		Inter Partes Review Case No. 2014-00882, Netlist Inc.'s Notice of Appeal, filed February 10, 2016
		Inter Partes Review Case No. 2014-00882, Exhibit 1022, 'Professor Carl Sechen Deposition Transcript,' filed June,19,2015
		Inter Partes Review Case No. 2014-00882, Exhibit 1023, 'Dr. Srinivasan Jagannathan Supplemental Declaration,' filed June 19,2015
		Inter Partes Review Case No. 2014-00882, Exhibit 2002, 'Declaration of Professor Carl Sechen,' filed May 8,2015
		Inter Partes Review Case No. 2014-00882, Exhibit 2003, 'Transcript of Videotaped Deposition of Srinivasan Jagannathan, Ph. D,' filed May 8,2015
		Microsoft Computer Dictionary, Fifth Edition, Microsoft Press, p. 334, 2002
		Jacob, Bruce, et al. "Memory Systems - Cache, DRAM, Disk," Elsevier Inc. 2008, Chapters 7 and 10

Examiner Signature		Date Considered	

DB2/ 36616000.1

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.H./

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed August 21, 2019	
				Application Number	16/412,308
				Filing Date	May 14, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2827
				Examiner Name	To be assigned
Sheet	13	of	14	Attorney Docket Number	129980-5070US01

		U.S. District Court Northern District of California, Case No. 4.13-cn-05889-YGR, Netlist Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Joint Claim Construction and Prehearing Statement Pursuant to Patent L. T. 4-3, filed August 27, 2014, in 28 pages
		Excerpts from the Authoritative Dictionary of IEEE Standard Terms, Seventh Edition, Standards Information Network, IEEE Press (2000), pp. 349-411
		\Excerpts from the Authoritative Dictionary of IEEE Standard Terms, Seventh Edition, Standards Information Network, IEEE Press (2000), pp. 133-265
		Selected Entries in Oxford English Dictionary, Oxford University Press 2014, http://www.oed.com/view/Entry/175039?redirectedFrom=selectively#eid
		Web search results from the Oxford English Dictionary, Oxford University Press 2014, http://www.oed.com/search?searchType=dictionary&q=select& _searchBin=Search
		Inter Partes Review Case No. 2014-00883, Patent Owner Response, filed May 8, 2015
		Inter Partes Review Case No. 2014-00883, Petitioner Diablo Technologies, Inc.'s Reply to Patent Owner Netlist, Inc.'s Response, filed June 19, 2015
		Inter Partes Review Case No. 2014-00883, Petitioner's Request for Oral Argument, filed July 1, 2015
		Inter Partes Review Case No. 2014-00883, Patent Owner's Request for Oral Hearing, filed July 3, 2015
		Inter Partes Review Case No. 2014-00883, Order - Request for Oral Argument - 37 C.F.R. 42.70, filed July 10, 2015
		Inter Partes Review Case No. 2014-00883, Record of Oral Hearing, filed November 16, 2015
		Inter Partes Review Case No. 2014-00883, Final Written Decision - 35 USC 318 and 37 CFR 42.73, filed December 14, 2015
		Inter Partes Review Case No. 2014-00883, Netlist Inc.'s Notice of Appeal, filed February 10, 2016
		Inter Partes Review Case No. 2014-00883, Exhibit 1025, 'Professor Carl Sechen Deposition Transcript,' filed June 19,2015
		Inter Partes Review Case No. 2014-00883, Exhibit 1026, 'Dr. Srinivasan Jagannathan Supplemental Declaration,' filed June 19,2015
		Inter Partes Review Case No. 2014-01011, Patent Owner Response, filed May 8, 2015
		Inter Partes Review Case No. 2014-01011, Petitioner Diablo Technologies, Inc.'s Reply to Patent Owner Netlist, Inc.'s Response, filed June 19, 2015
		Inter Partes Review Case No. 2014-01011, Petitioner's Request for Oral Argument, filed July 1, 2015
		Inter Partes Review Case No. 2014-01011, Patent Owner's Request for Oral Hearing, filed July 3, 2015
		Inter Partes Review Case No. 2014-01011, Order - Request for Oral Argument - 37 C.F.R. 42.70, filed July 10, 2015

Examiner Signature		Date Considered	

DB2/ 36616000.1

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.H/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed August 21, 2019	
				Application Number	16/412,308
				Filing Date	May 14, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2827
				Examiner Name	To be assigned
Sheet	14	of	14	Attorney Docket Number	129980-5070US01

		Inter Partes Review Case No. 2014-01011, Record of Oral Hearing, filed November 16, 2015
		Inter Partes Review Case No. 2014-01011, Final Written Decision - 35 USC 318 and 37 CFR 42.73, filed December 14, 2015
		Inter Partes Review Case No. 2014-01011, Netlist Inc.'s Notice of Appeal, filed February 10, 2016
		Inter Partes Review Case No. 2014-01011, Exhibit 1027, 'Professor Carl Sechen Deposition Transcript,' filed June 19,2015
		Inter Partes Review Case No. 2014-01011, Exhibit 1028, 'Dr. Srinivasan Jagannathan Supplemental Declaration,' filed June 19,2015

Examiner Signature	/HUAN HOANG/	Date Considered	11/19/2020

DB2/ 36616000.1

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.H/

Electronically filed December 16, 2020

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun Lee	Confirmation No.:	6765
Serial No.:	16/412,308	Art Unit:	2827
Filed:	May 14, 2019	Examiner:	Hoang, Huan
For:	*Memory Module With Buffered Memory Packages*	Attorney Docket No.:	129980-5070-US01

AMENDMENT UNDER 37 C.F.R. § 1.312

Mail Stop: AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The enclosed Amendment is filed under 37 C.F.R. § 1.312 for the above identified patent application, and is filed after a Notice of Allowance dated September 17, 2020 and a Corrected Notice of Allowability dated November 23, 2020.

The Commissioner is hereby authorized to charge any required fee(s) to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5070-US01).

Petitioners
Ex. 1009, p. 279

Amendments to the Claims

The following listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Cancelled)

2. (Previously Presented) A memory module operable in a computer system to communicate with a system memory controller via a command/address bus and a data bus, comprising:

a register device configurable to receive input command/address signals from the system memory controller via the command/address bus and to output control signals in response to the input command/address signals, the control signals including buffered command/address signals and data path control signals; and

a plurality of DRAM packages, each respective DRAM package comprising:

terminals including control terminals coupled to the register device and data terminals to be coupled to a respective section of the data bus, the control terminals including first control terminals and second control terminals;

stacked array dies; and

a control die coupled between the stacked array dies and the terminals of the respective DRAM package, the control die including data buffers and a data path control circuit; and

wherein the control die is configurable to:

receive the buffered command/address signals via the first control terminals and the data path control signals via the second control terminals;

provide at least some of the buffered command/address signals to the stacked array dies, including providing respective chip-select signals to respective array dies of the stacked array dies; and

control the data buffers in response to the data path control signals to buffer data signals communicated between a selected array die of the stacked array dies and the respective section of the data bus, the selected array die having received one of the chip select signals that is different from any of the other ones of the chip select signals.

Petitioners
Ex. 1009, p. 280

3. (Previously Presented) The memory module of claim 2, wherein the register device is configurable to decode the input command/address signals and to generate the data path control signals in accordance with the input command/address signals.

4. (Previously Presented) The memory module of claim 2, wherein the data buffers are configurable to selectively isolate one or more array dies of the stacked array dies.

5. (Previously Presented) The memory module of claim 2, wherein the control die does not secondarily buffer the buffered command/address signals.

6. (Previously Presented) The memory module of claim 2, wherein the data path control circuit is configurable to control a command/address time slot for the buffered command/address signals passing through the control die.

7. (Previously Presented) The memory module of claim 2, wherein the data path control circuit is configurable to control a data bus time slot for the data signals.

8. (Previously Presented) The memory module of claim 2, wherein the buffered command/address signals include more chip select signals than the input command/address signals.

9. (Previously Presented) The memory module of claim 2, further comprising die interconnects including first die interconnects coupled to the data buffers and second die interconnects coupled to the control terminals, each of the first die interconnects being coupled to one or more of the stacked array dies.

10. (Previously Presented) The memory module of claim 9, wherein the data buffers include drivers coupled to respective ones of the first die interconnects, the drivers including a first driver coupled to one or more first array dies via a first die interconnect and a second driver and coupled to one or more second array dies via a second die interconnect, the first driver having a first driver size corresponding to a first capacitive load associated with the one or more first array dies and the first die interconnect, the second driver having a second driver size corresponding to a second capacitive load associated with the one or more second array dies and the second die interconnect.

Petitioners
Ex. 1009, p. 281

11. (Previously Presented) A memory module operable in a computer system to communicate with a system memory controller via a command/address bus and a data bus, comprising:

a register device configurable to receive input command/address signals from the system memory controller via the command/address bus, to buffer the input command/address signals, and to output control signals in response to the input command/address signals, the control signals including buffered command/address signals; and

a plurality of DRAM packages, each respective DRAM package comprising:

terminals including control terminals coupled to the register device and data terminals to be coupled to a respective section of the data bus, the control terminals including first control terminals and second control terminals;

stacked array dies; and

a control die coupled between the stacked array dies and the terminals of the respective DRAM package, the control die including data buffers and a data path control circuit; and

wherein the memory module is operable in any one of a plurality of modes including a first mode and a second mode;

wherein, during the first mode, the register device is configurable to generate data path control signals in response to receiving the input command/address signals, the control signals further include the data path control signals, and the control die is configurable to:

receive the buffered command/address signals via the first control terminals and the data path control signals via the second control terminals; and

provide at least some of the buffered command/address signals to the stacked array dies, including providing respective chip-select signals to respective array dies of the stacked array dies;

wherein, during the second mode, the control die is configurable to:

receive the buffered command/address signals via the first control terminals;

generate data path control signals in response to the buffered command/address signals; and

provide secondarily buffered command/address signals to the stacked array dies, including providing respective chip-select signals to respective array dies of the stacked array dies; and

Petitioners
Ex. 1009, p. 282

wherein, during the first mode or the second mode, the data path control circuit is configured to control the data buffers in response to the data path control signals to buffer data signals communicated between a selected array die of the stacked array dies and the respective section of the data bus, the selected array die having received one of the chip select signals that is different from any of the other ones of the chip select signals.

12. (Previously Presented) The memory module of claim 11, wherein, during the second mode, the control die is configurable to generate data path control signals after decoding the buffered command/address signals.

13. (Previously Presented) The memory module of claim 12, wherein the secondarily buffered command/address signals include more chip select signals than the buffered command/address signals.

14. (Previously Presented) The memory module of claim 11, wherein the data buffers are configurable to selectively isolate one or more array dies of the stacked array dies.

15. (Previously Presented) The memory module of claim 11, wherein, during the first mode, the control die does not buffer at least some of the buffered command/address signals.

16. (Previously Presented) The memory module of claim 11, wherein the data path control circuit is configurable to control a command/address time slot for the buffered command/address signals passing through the control die.

17. (Previously Presented) The memory module of claim 11, wherein the data path control circuit is configurable to control a data bus time slot for the data signals.

18. (Previously Presented) The memory module of claim 11, further comprising die interconnects including first die interconnects coupled to the data buffers and second die interconnects coupled to the control terminals, each of the first die interconnects being coupled to one or more of the stacked array dies.

19. (Currently Amended) The memory module of claim 18[[11]], wherein the data buffers include drivers coupled to respective ones of the first die interconnects, the drivers including a

Petitioners
Ex. 1009, p. 283

first driver coupled to one or more first array dies via a first die interconnect among the first die interconnects and a second driver and coupled to one or more second array dies via a second die interconnect among the first die interconnects, the first driver having a first driver size corresponding to a first capacitive load associated with the one or more first array dies and the first die interconnect, the second driver having a second driver size corresponding to a second capacitive load associated with the one or more second array dies and the second die interconnect.

20. (Previously Presented) The memory module of claim 11, wherein the control die does not receive data path control signals from the register device via the second control terminals during the second mode.

21. (Previously Presented) The memory module of claim 11, wherein, during the first mode, the register device is configurable to perform rank multiplication, and wherein, during the second mode, the control die is configurable to perform rank multiplication.

Petitioners
Ex. 1009, p. 284

REMARKS

This amendment is filed after the Notice of Allowance dated September 17, 2020 and the Corrected Notice of Allowability dated November 23, 2020, which allowed claims 2-21.

Claim 19 has been amended. No new matter is added. The amendments address minor issues of clarity and should not require additional search or examination.

In the Corrected Notice of Allowability dated November 23, 2020, the Examiner notes that the document by KIM et al, "A Quantitative Analysis of Performance Benefits of 30 Die Stacking on Mobile and Embedded Soc" in the information disclosure statement filed 08/21/2019 (the "IDS") fails to comply with the provisions of 37 CFR 1.97 and MPEP § 609 because it does not provide the publication date. Applicant apologizes for the clerical error of leaving out the publication date of the document in the IDS. As Applicant considers whether to resubmit the document, Applicant determines that the document has a publication date in March, 2011, which is after the priority date (November 3, 2010) of the present application. Furthermore, the information in the document is not relevant to the claims in the present application. Therefore, Applicant decides not to resubmit the document.

The Examiner is invited to call the undersigned attorney at (650) 521-4828, if a telephone call could help resolve any remaining items.

Respectfully submitted,

Date: December 16, 2020

/ Jamie Zheng / 51,167

Jamie Zheng (Reg. No.)
MORGAN, LEWIS & BOCKIUS LLP
1400 Page Mill Road
Palo Alto, CA 94304
Phone: (650) 843-4000

Petitioners
Ex. 1009, p. 285

PART B - FEE(S) TRANSMITTAL

Electronically filed December 16, 2020

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(Depositor's name)

(Signature)

(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTY'S DOCKET NO.	CONFIRMATION NO.
16/412,308	05/14/2019	Hyun Lee	129980-5070-US01	6765

TITLE OF INVENTION **MEMORY MODULE WITH BUFFERED MEMORY PACKAGES**

APPLN. TYPE	ENTITY STATUS	ISSUE FEE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	1000	0	1000	12/17/2020

EXAMINER	ART UNIT	CLASS-SUB CLASS
HOANG, HUAN	2827	365-063000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47) attached. **Use of a Customer Number is required.**

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1. **Morgan, Lewis & Bockius LLP**
2.
3.

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: NETLIST, INC.

(B) RESIDENCE: (CITY and STATE OR COUNTRY) Irvine, CA

Please check the appropriate assignee category or categories (will not be printed on the patent) ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

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☐ Advanced Order - # of Copies _____

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5. **Change in Small Entity Status** (from status indicated above)

☐ a. Applicant certifying micro entity status. See 37 CFR 1.29.

NOTE: Absent a valid certification of Micro Entity (see form PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

☐ Applicant asserting small entity status. See 37 CFR 1.27.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

☐ Applicant changing to regular undiscounted fee status.

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NOTE: This form must be sign in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature: / Jamie J. Zheng / Date: December 16, 2020

Printed Name: Jamie J. Zheng Registration No. 51,167

Electronic Acknowledgement Receipt

EFS ID:	41410069
Application Number:	16412308
International Application Number:	
Confirmation Number:	6765
Title of Invention:	MEMORY MODULE WITH BUFFERED MEMORY PACKAGES
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	129980-5070-US01
Receipt Date:	16-DEC-2020
Filing Date:	14-MAY-2019
Time Stamp:	23:42:11
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		129980-5070-US01_312_Amendment.pdf	129795 cf2abe51739ae99cd02ef7a5aa441bcb3a458f79	yes	7

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment after Notice of Allowance (Rule 312)	1	1
	Claims	2	6
	Applicant Arguments/Remarks Made in an Amendment	7	7

Warnings:

Information:

2	Issue Fee Payment (PTO-85B)	129980-5070-US01_Issue_Fee.pdf	110484 9d796162cf76f90b54503a0aabbaec5eb3733605	no	1

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PART B - FEE(S) TRANSMITTAL

Electronically filed December 16, 2020

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(Depositor's name)

(Signature)

(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTY'S DOCKET NO.	CONFIRMATION NO.
16/412,308	05/14/2019	Hyun Lee	129980-5070-US01	6765

TITLE OF INVENTION **MEMORY MODULE WITH BUFFERED MEMORY PACKAGES**

APPLN. TYPE	ENTITY STATUS	ISSUE FEE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	1000	0	1000	12/17/2020

EXAMINER	ART UNIT	CLASS-SUB CLASS
HOANG, HUAN	2827	365-063000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47) attached. **Use of a Customer Number is required.**

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1. **Morgan, Lewis & Bockius LLP**
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3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

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(A) NAME OF ASSIGNEE: NETLIST, INC.

(B) RESIDENCE: (CITY and STATE OR COUNTRY) Irvine, CA

Please check the appropriate assignee category or categories (will not be printed on the patent) ☐ Individual ☒ Corporation or other private group entity ☐ Government

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5. **Change in Small Entity Status** (from status indicated above)

☐ a. Applicant certifying micro entity status. See 37 CFR 1.29.

NOTE: Absent a valid certification of Micro Entity (see form PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

☐ Applicant asserting small entity status. See 37 CFR 1.27.

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☐ Applicant changing to regular undiscounted fee status.

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NOTE: This form must be sign in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature: / Jamie J. Zheng / Date: December 16, 2020

Printed Name: Jamie J. Zheng Registration No. 51,167

Electronic Patent Application Fee Transmittal

Application Number:	16412308
Filing Date:	14-May-2019
Title of Invention:	MEMORY MODULE WITH BUFFERED MEMORY PACKAGES
First Named Inventor/Applicant Name:	Hyun Lee
Filer:	Jamie Jie Zheng/S. Olivier
Attorney Docket Number:	129980-5070-US01

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	1000	1000

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**1000**

Electronic Acknowledgement Receipt

EFS ID:	41347554
Application Number:	16412308
International Application Number:	
Confirmation Number:	6765
Title of Invention:	MEMORY MODULE WITH BUFFERED MEMORY PACKAGES
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	129980-5070-US01
Receipt Date:	17-DEC-2020
Filing Date:	14-MAY-2019
Time Stamp:	01:21:01
Application Type:	Utility under 35 USC 111(a)

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Payment was successfully received in RAM	$1000
RAM confirmation Number	E2020BG221344364
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The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	129980-5070US01_Issue_Fee.pdf	110484 dfc2c00eb6d57fedc1ad82b7c286cffad55f6ef6	no	1
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30470 71d272279fcbdb942a9f68f56e0e340f5d650922	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	140954		

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/412,308	05/14/2019	Hyun Lee	129980-5070-US01	6765

79141 7590 12/28/2020
Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304

EXAMINER
HOANG, HUAN

ART UNIT	PAPER NUMBER
2827	

NOTIFICATION DATE	DELIVERY MODE
12/28/2020	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

padocketingdepartment@morganlewis.com
vskliba@morganlewis.com

Response to Rule 312 Communication	Application No.	Applicant(s)	
	16/412,308	Lee, Hyun	
	Examiner	**Art Unit**	**AIA (FITF) Status**
	HUAN HOANG	2827	No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

1. ☑ The amendment filed on 16 December 2020 under 37 CFR 1.312 has been considered, and has been:
   a) ☑ entered.
   b) ☐ entered as directed to matters of form not affecting the scope of the invention.
   c) ☐ disapproved because the amendment was filed after the payment of the issue fee.
   Any amendment filed after the date the issue fee is paid must be accompanied by a petition under 37 CFR 1.313(c)(1) and the required fee to withdraw the application from issue.
   d) ☐ disapproved. See explanation below.
   e) ☐ entered in part. See explanation below.

/HUAN HOANG/
Primary Examiner, Art Unit 2827

Receipt date: 12/16/2020

APPROVED: /H.H/

12/19/2020

Electronically filed December 16, 2020

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun Lee	Confirmation No.:	6765
Serial No.:	16/412,308	Art Unit:	2827
Filed:	May 14, 2019	Examiner:	Hoang, Huan
For:	*Memory Module With Buffered Memory Packages*	Attorney Docket No.:	129980-5070-US01

AMENDMENT UNDER 37 C.F.R. § 1.312

Mail Stop: AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The enclosed Amendment is filed under 37 C.F.R. § 1.312 for the above identified patent application, and is filed after a Notice of Allowance dated September 17, 2020 and a Corrected Notice of Allowability dated November 23, 2020.

The Commissioner is hereby authorized to charge any required fee(s) to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5070-US01).

Petitioners
Ex. 1009, p. 296

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed August 21, 2019	
				Application Number	16/412,308
				Filing Date	May 14, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2827
				Examiner Name	To be assigned
Sheet	4	of	14	Attorney Docket Number	129980-5070US01

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NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
		U.S. Application No. 12/422,912, (Attorney Docket No. NETL044A)
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Examiner Signature		Date Considered	

DB2/ 36616000.1

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.H/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				Electronically filed August 21, 2019	
				Application Number	16/412,308
				Filing Date	May 14, 2019
				First Named Inventor	Hyun Lee
				Art Unit	2827
				Examiner Name	To be assigned
Sheet	2	of	14	Attorney Docket Number	129980-5070US01

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Change(s) applied to document, /S.D./ 11/18/2020

Examiner Signature		Date Considered	

DB2/ 36616000.1

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.H/

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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/412,308	01/26/2021	10902886	129980-5070-US01	6765

79141 7590 01/06/2021
Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

NETLIST, INC., Irvine, CA;
Hyun Lee, Ladera Ranch, CA;

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