US 20110193226A1

(19) United States

(12) Patent Application Publication

(10) Pub. No.: US 2011/0193226 A1

(43) Pub. Date: Aug. 11, 2011

Kirby et al.

(54) MICROELECTRONIC DEVICES WITH THROUGH-SUBSTRATE INTERCONNECTS AND ASSOCIATED METHODS OF MANUFACTURING

(75) Inventors: **Kyle K. Kirby**, Eagle, ID (US); **Kunal R. Parekh**, Boise, ID (US); **Sarah A. Niroumand**, Boise, ID (US)

(73) Assignee: **MICRON TECHNOLOGY, INC.**, Boise, ID (US)

(21) Appl. No.: **12/701,800**

(22) Filed: **Feb. 8, 2010**

Publication Classification

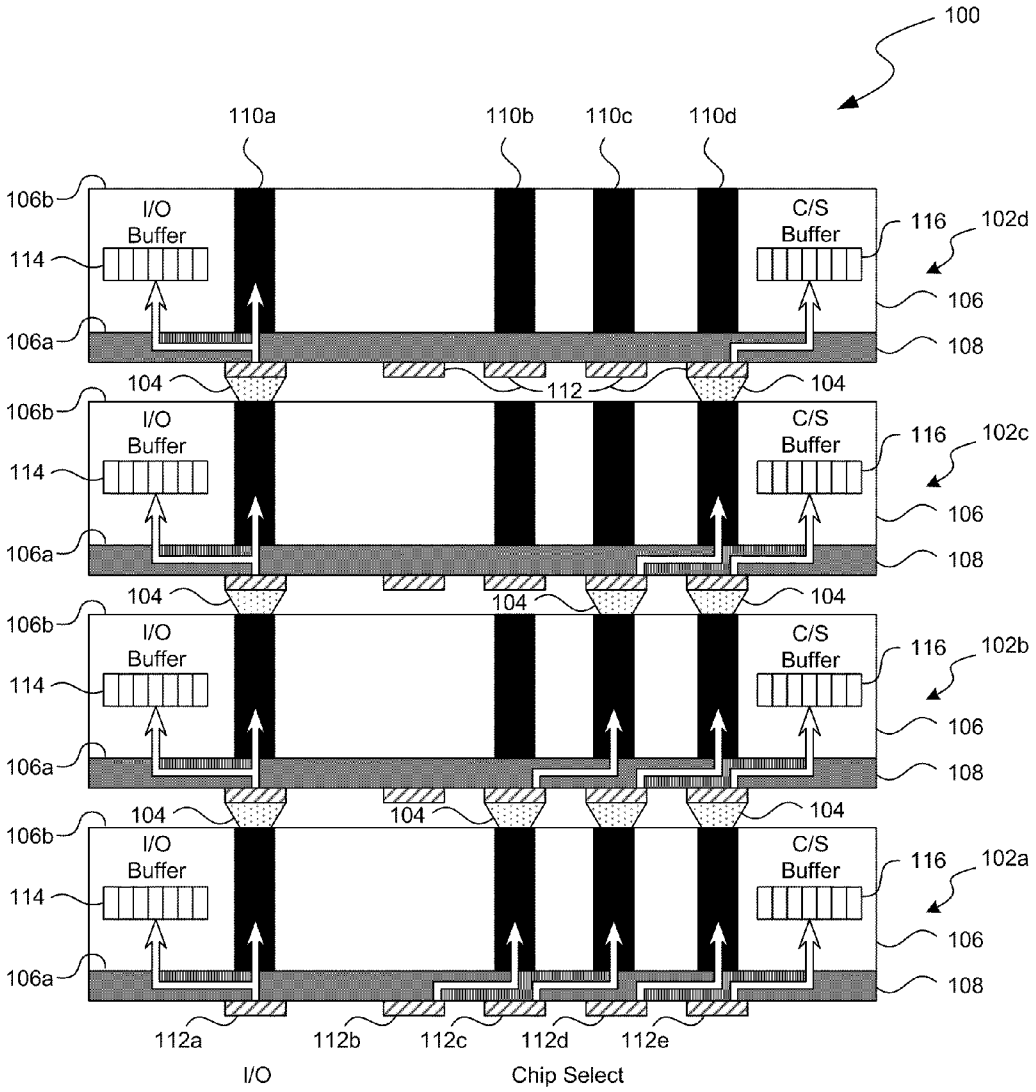
(51) **Int. Cl.**

H01L 23/48	(2006.01)
H01L 21/768	(2006.01)
H01L 23/488	(2006.01)

(52) **U.S. Cl.** **257/738**; 257/774; 438/667; 438/613; 257/E21.585; 257/E23.011; 257/E23.023

(57) **ABSTRACT**

Microelectronic devices with through-substrate interconnects and associated methods of manufacturing are disclosed herein. In one embodiment, a semiconductor device includes a semiconductor substrate carrying first and second metallization layers. The second metallization layer is spaced apart from the semiconductor substrate with the first metallization layer therebetween. The semiconductor device also includes a conductive interconnect extending at least partially through the semiconductor substrate. The first metallization layer is in electrical contact with the conductive interconnect via the second metallization layer.



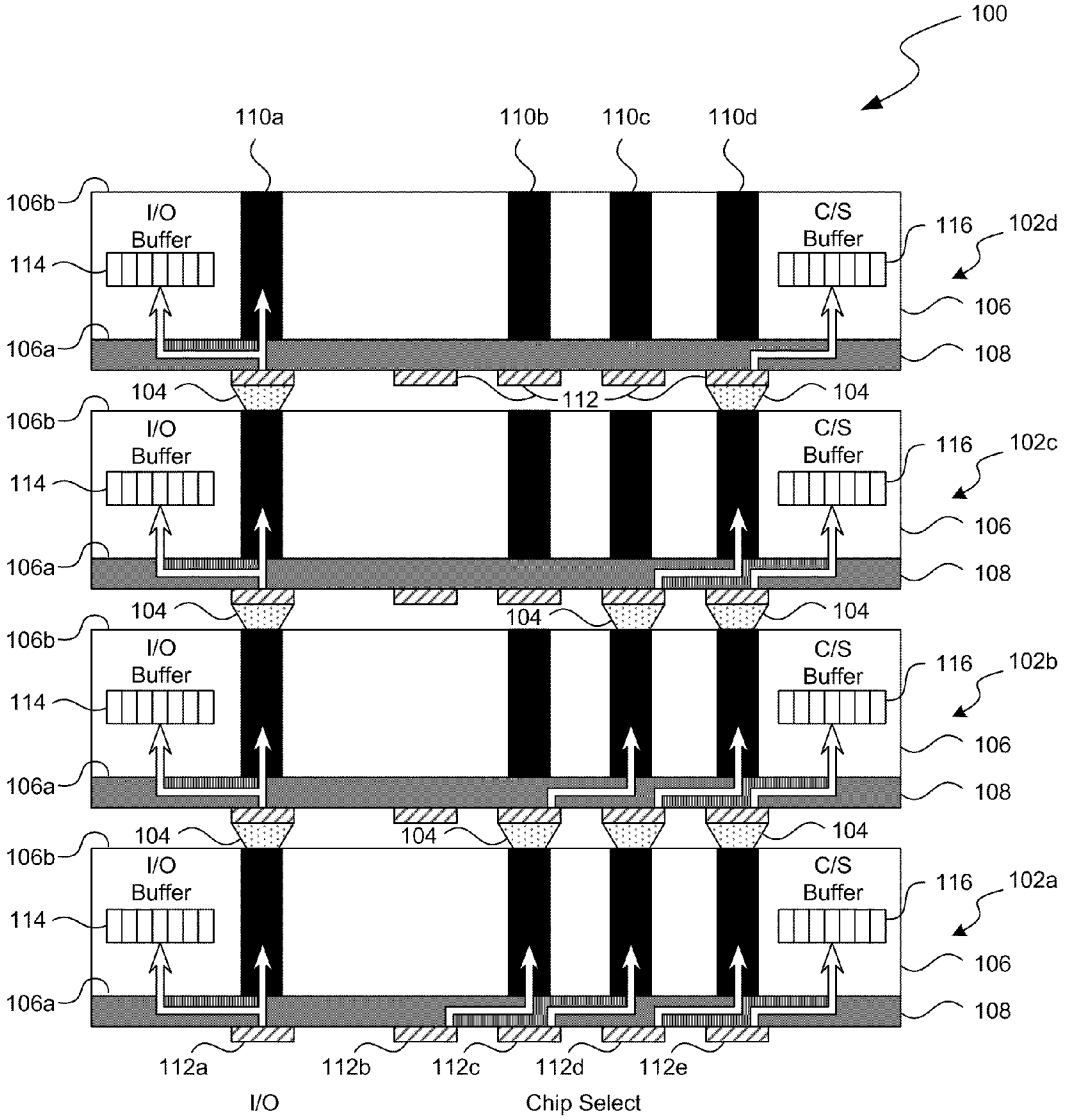

100
110a
110b
110c
110d
106b
I/O Buffer
C/S Buffer
114
116
102d
106
106a
108
104
112
102c
102b
102a
112a
112b
112c
112d
112e
I/O
Chip Select

FIG. 1

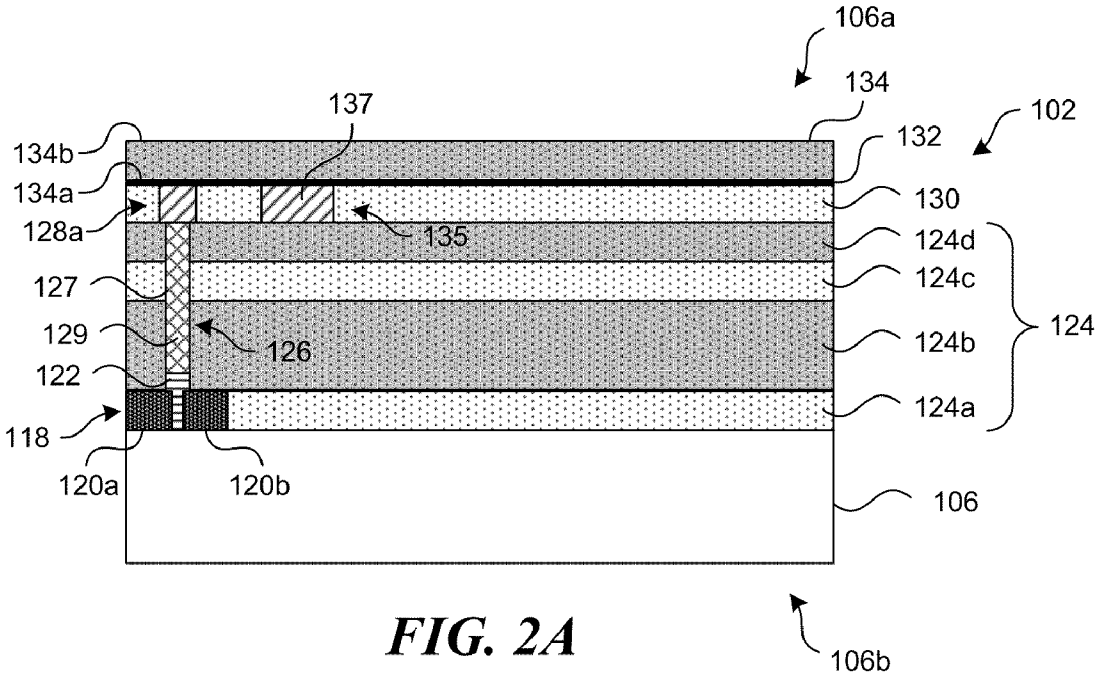

106a
134
137
102
134b
132
134a
130
128a
135
124d
127
124c
129
126
124b
124
122
124a
118
120a
120b
106
106b

FIG. 2A

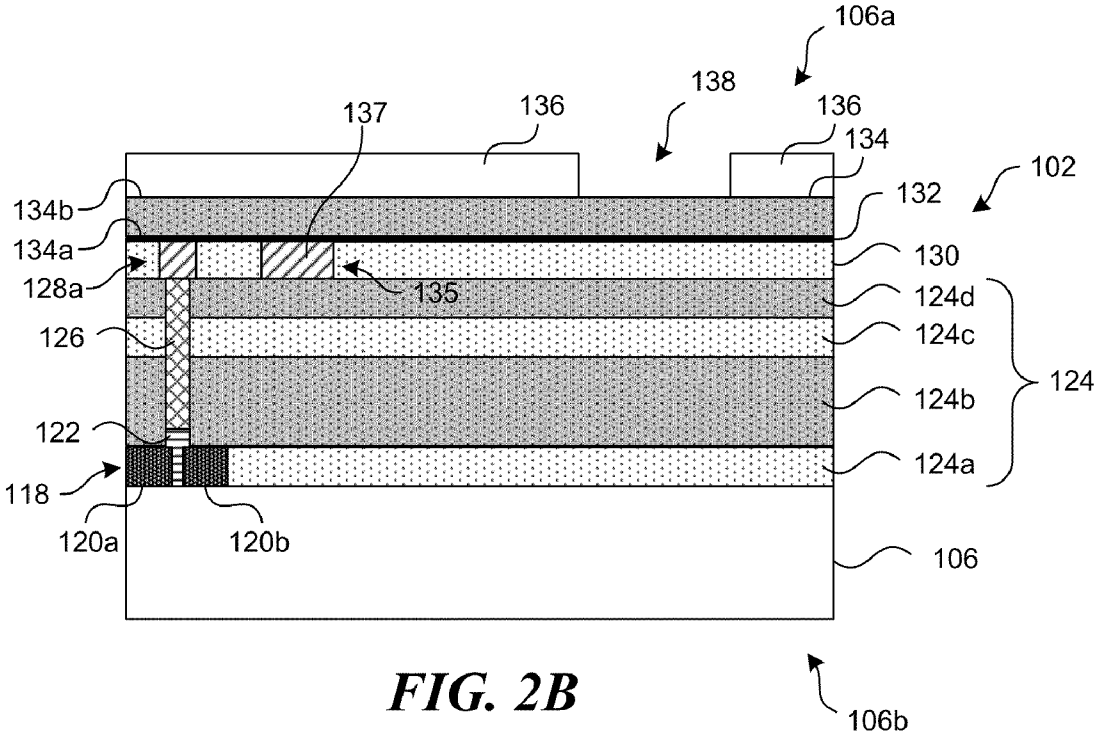

106a
138
137
136
136
134
102
134b
132
134a
130
128a
135
124d
126
124c
124b
124
122
124a
118
120a
120b
106
106b

FIG. 2B

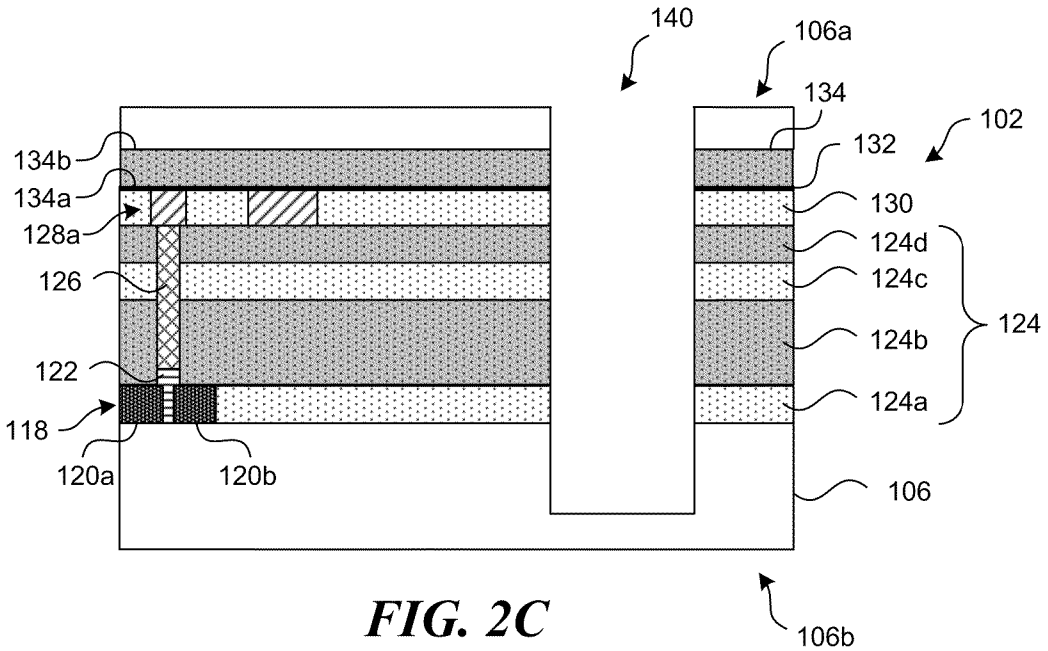

140
106a
134
102
134b
132
134a
130
128a
124d
126
124c
124
124b
122
124a
118
120a
120b
106
106b

FIG. 2C

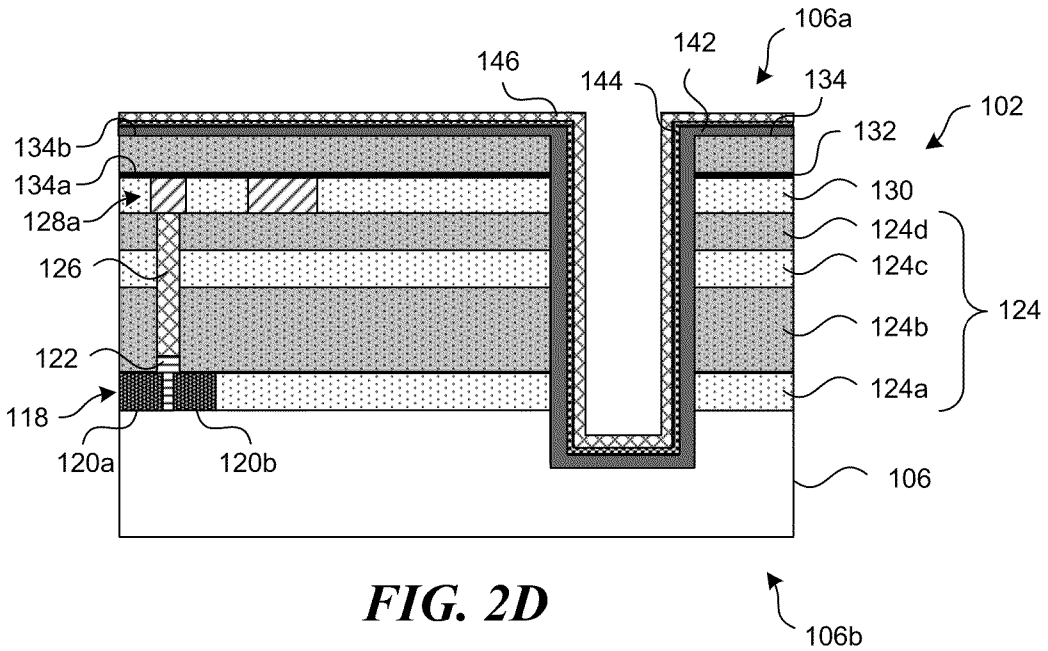

106a
142
146
144
134
102
134b
132
134a
130
128a
124d
126
124c
124
124b
122
124a
118
120a
120b
106
106b

FIG. 2D

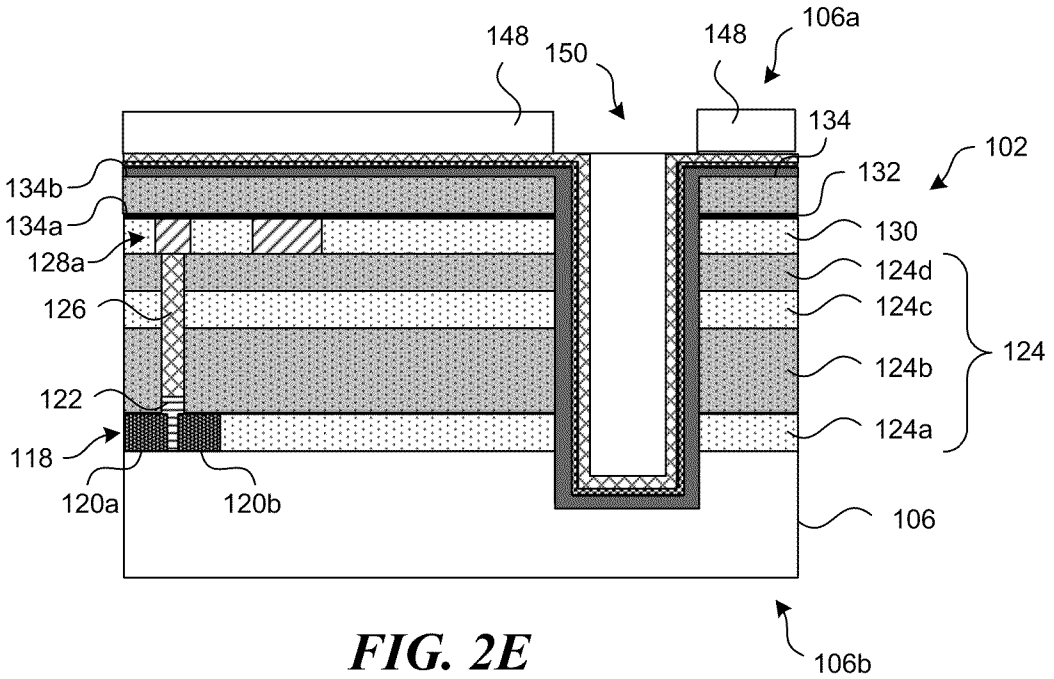

148
150
148
106a
134
102
134b
132
134a
130
128a
124d
126
124c
124
124b
122
124a
118
120a
120b
106
106b

FIG. 2E

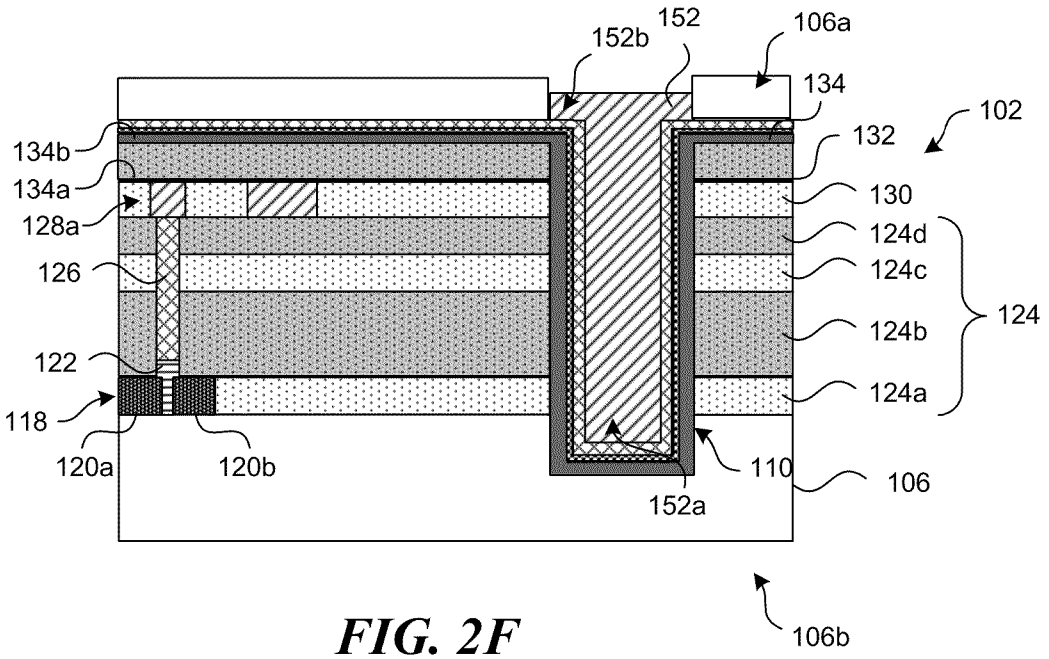

152b
152
106a
134
102
134b
132
134a
130
128a
124d
126
124c
124
124b
122
124a
118
120a
120b
110
106
152a
106b

FIG. 2F

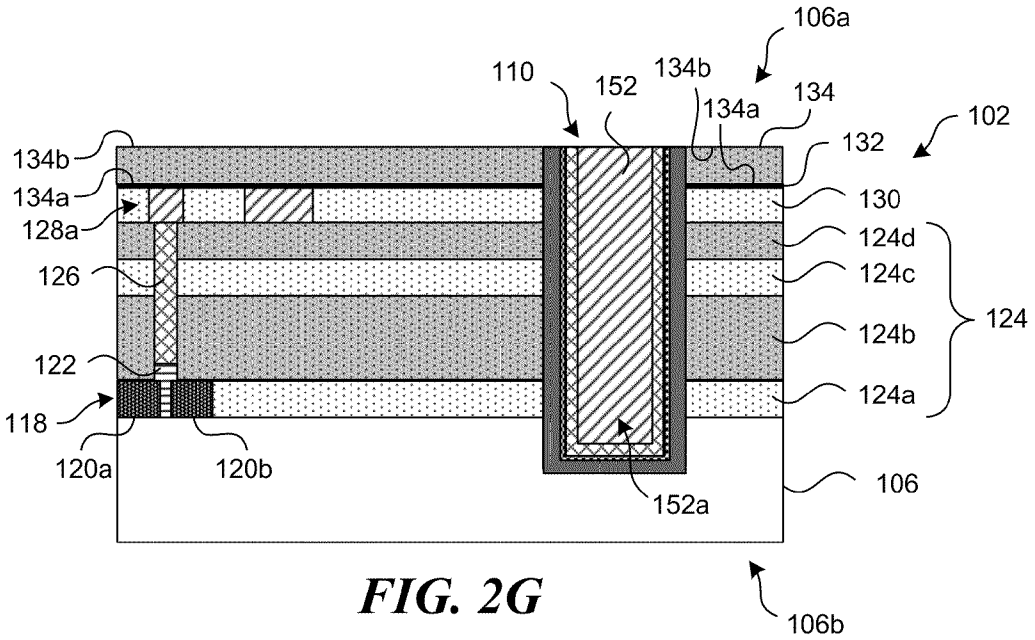

106a
110
152
134b
134a
134
102
132
134b
134a
128a
130
124d
126
124c
124
124b
122
124a
118
120a
120b
106
152a
106b

FIG. 2G

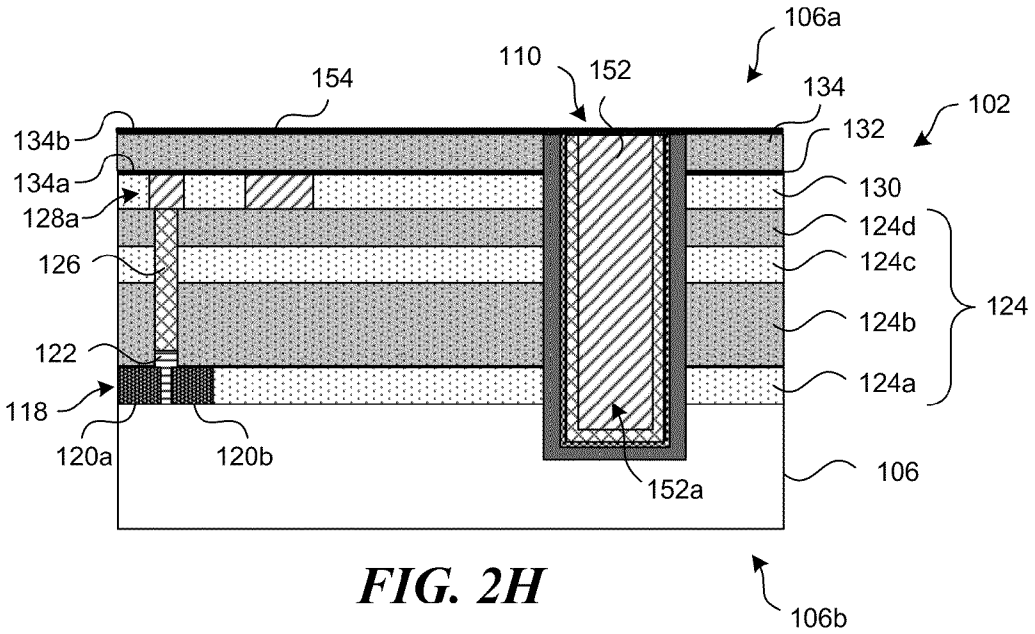

106a
110
152
154
134
102
132
134b
134a
128a
130
124d
126
124c
124
124b
122
124a
118
120a
120b
106
152a
106b

FIG. 2H

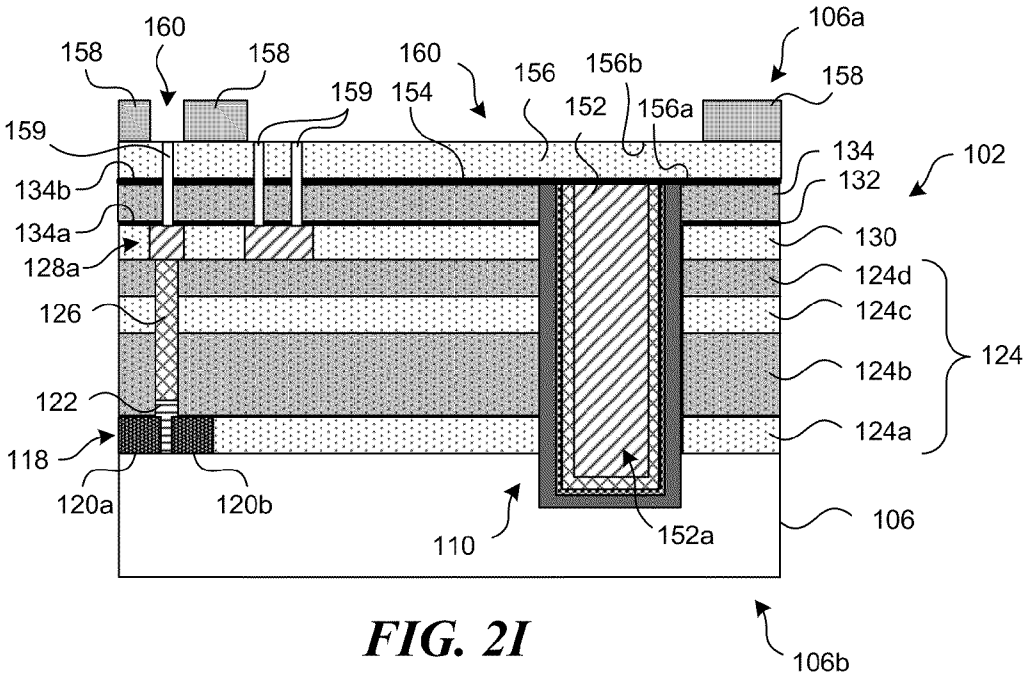

106a
160
158
158
160
156
156b
158
159
154
152
156a
159
134
102
134b
132
134a
130
128a
124d
126
124c
124
124b
122
124a
118
120a
120b
110
152a
106
106b

FIG. 2I

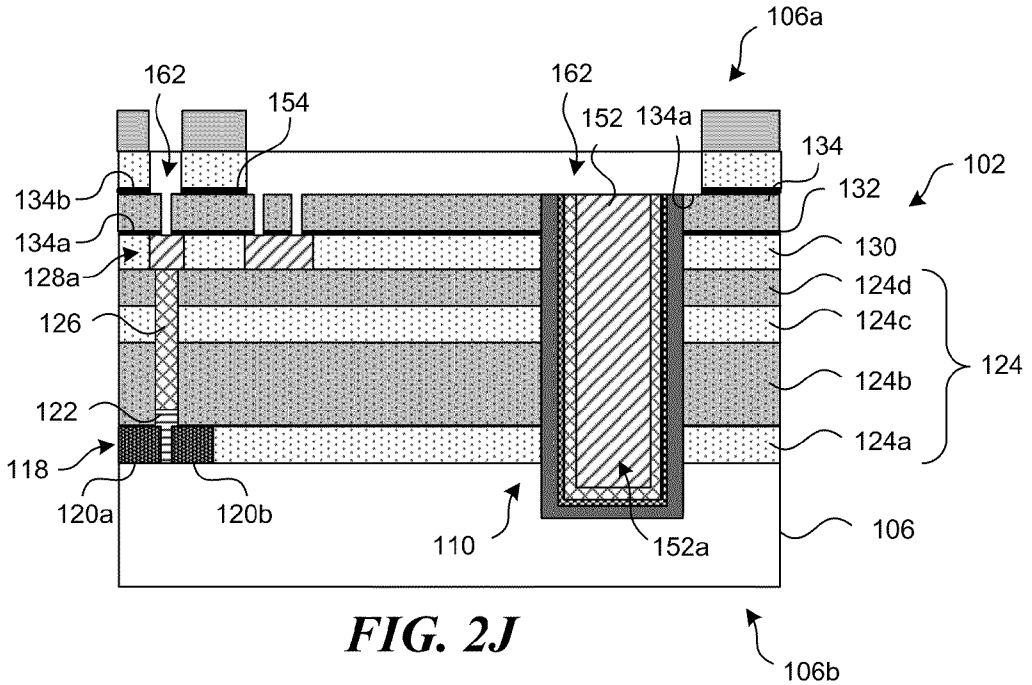

106a
162
162
154
152
134a
134
102
134b
132
134a
130
128a
124d
126
124c
124
124b
122
124a
118
120a
120b
110
152a
106
106b

FIG. 2J

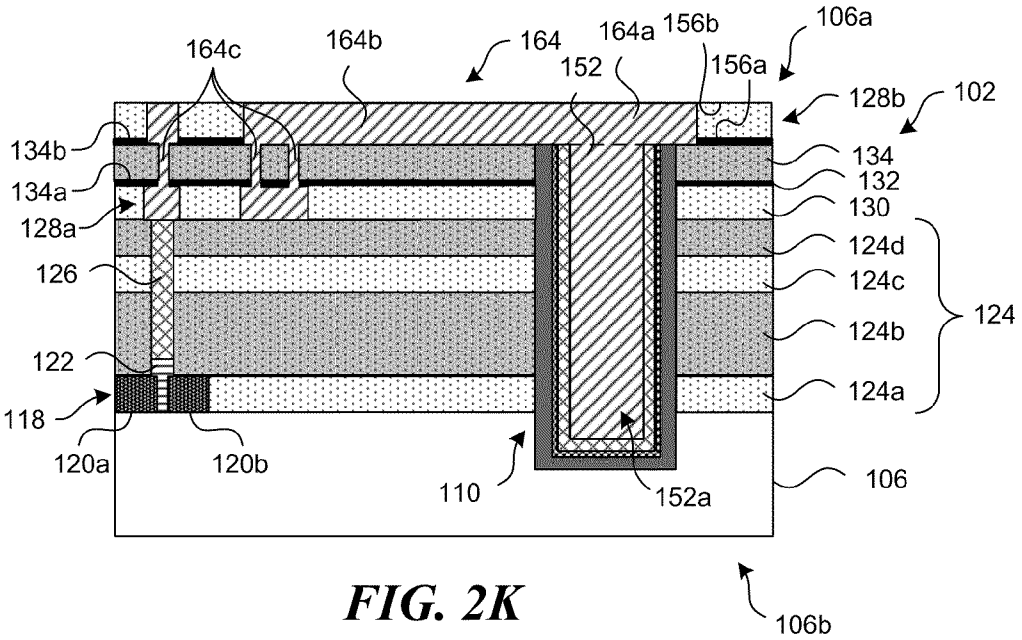

164c
164b
164
164a
156b
106a
152
156a
128b
102
134b
134
134a
132
128a
130
124d
126
124c
124
124b
122
124a
118
120a
120b
110
152a
106
106b

FIG. 2K

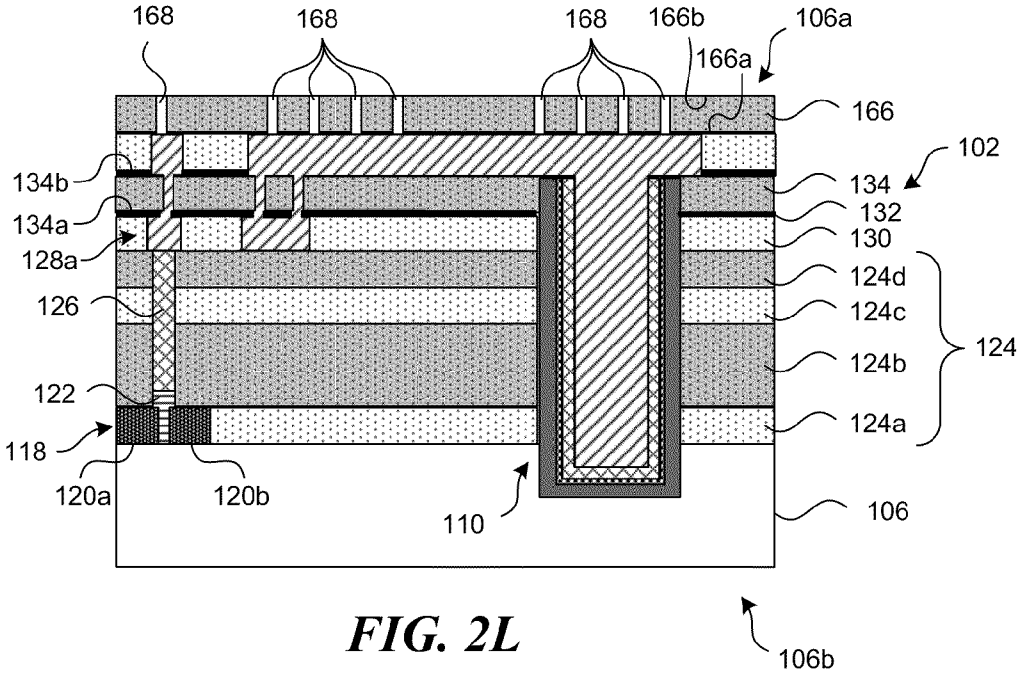

168
168
168
166b
106a
166a
166
102
134b
134
134a
132
128a
130
124d
126
124c
124
124b
122
124a
118
120a
120b
110
106
106b

FIG. 2L

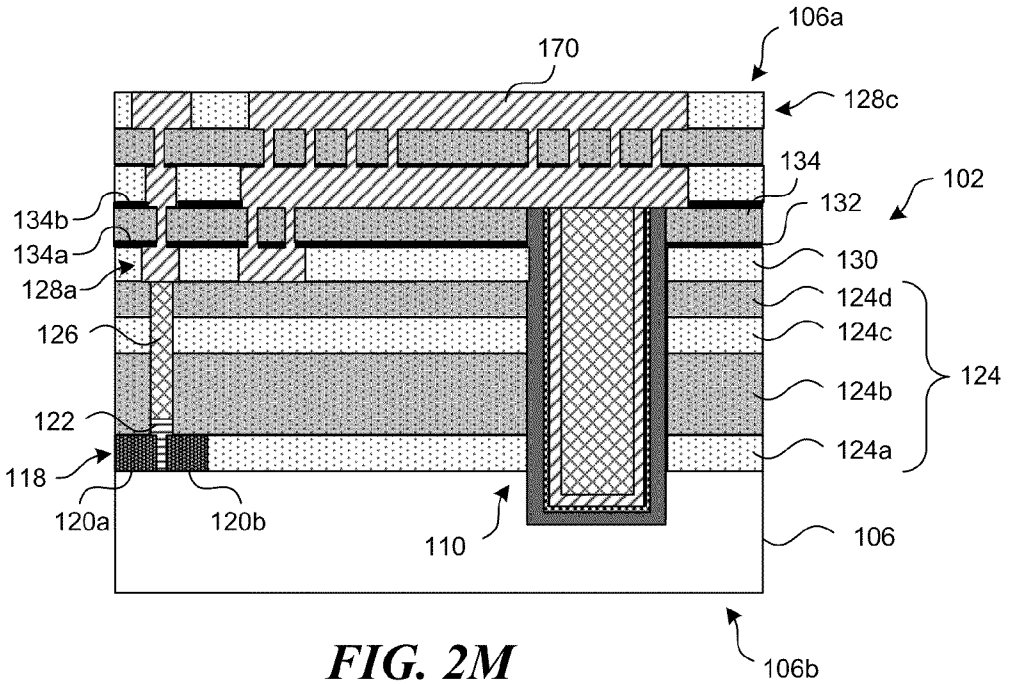

106a
170
128c
134
102
134b
132
134a
130
128a
124d
126
124c
124
124b
122
124a
118
120a
120b
110
106
106b

FIG. 2M

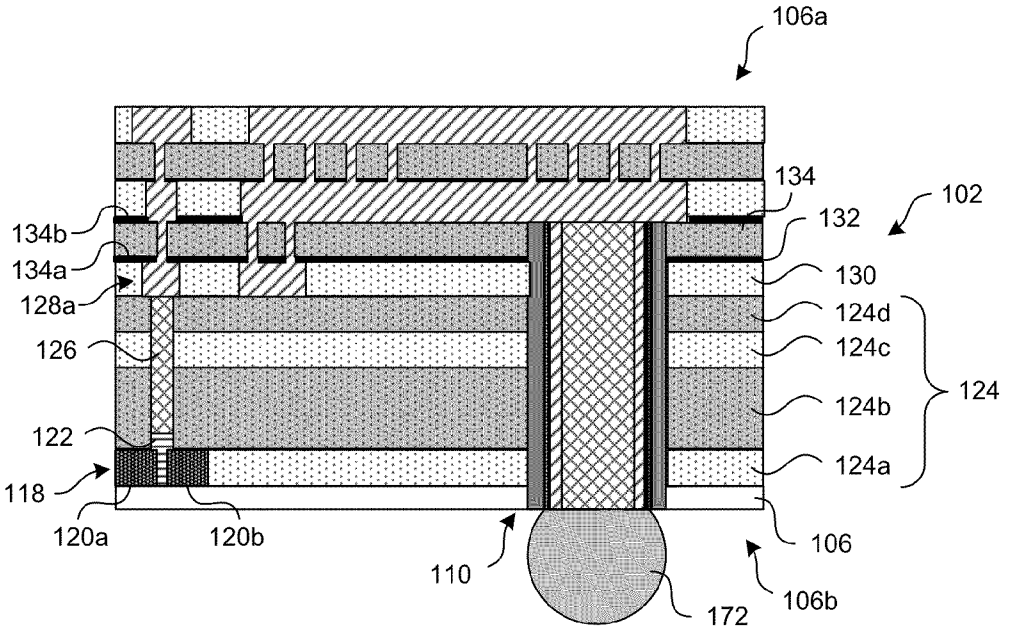

106a
134
102
134b
132
134a
130
128a
124d
126
124c
124
124b
122
124a
118
120a
120b
106
110
106b
172

FIG. 2N

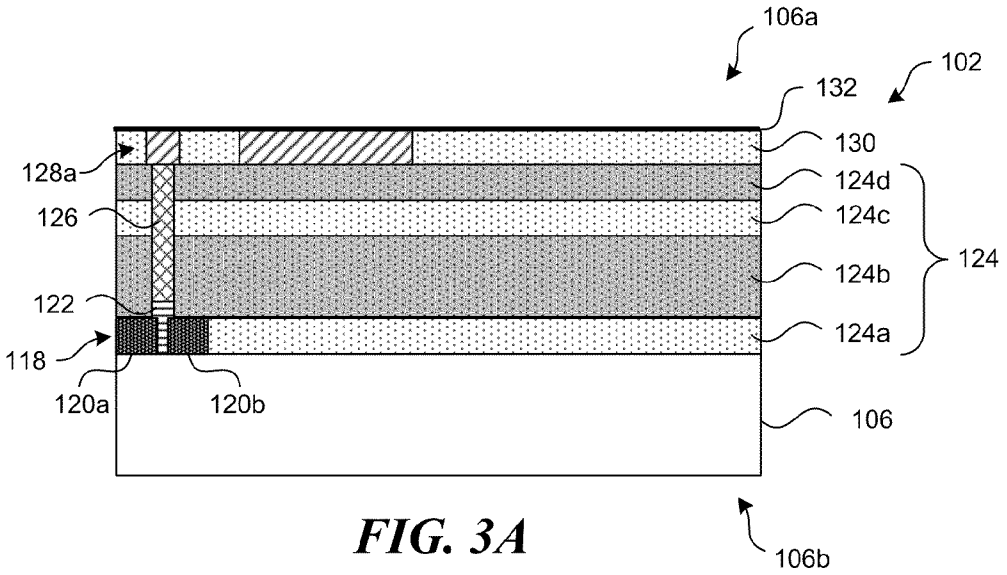

106a
102
132
130
128a
124d
126
124c
124
124b
122
124a
118
120a
120b
106
106b

FIG. 3A

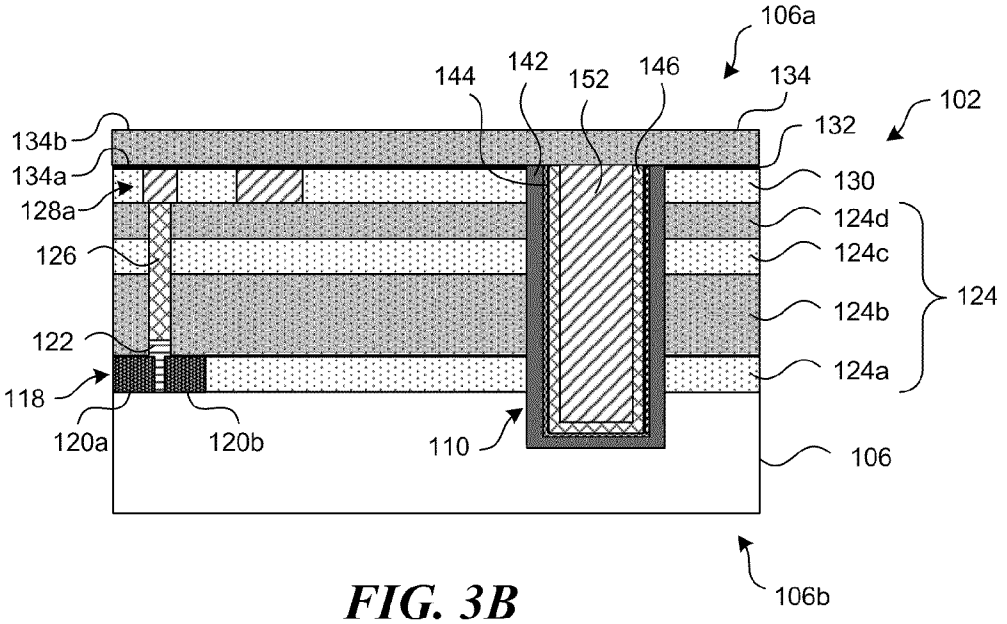

106a
144
142
152
146
134
102
134b
132
134a
130
128a
124d
126
124c
124
124b
122
124a
118
120a
120b
110
106
106b

FIG. 3B

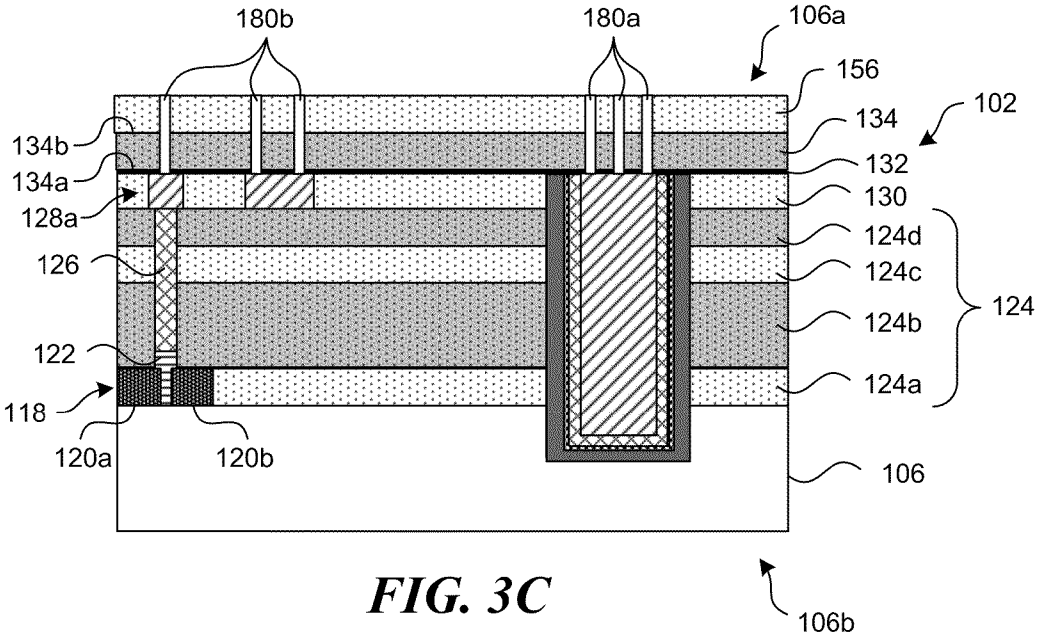

180b
180a
106a
156
134
102
134b
134a
132
128a
130
124d
126
124c
124
124b
122
124a
118
120a
120b
106
106b

FIG. 3C

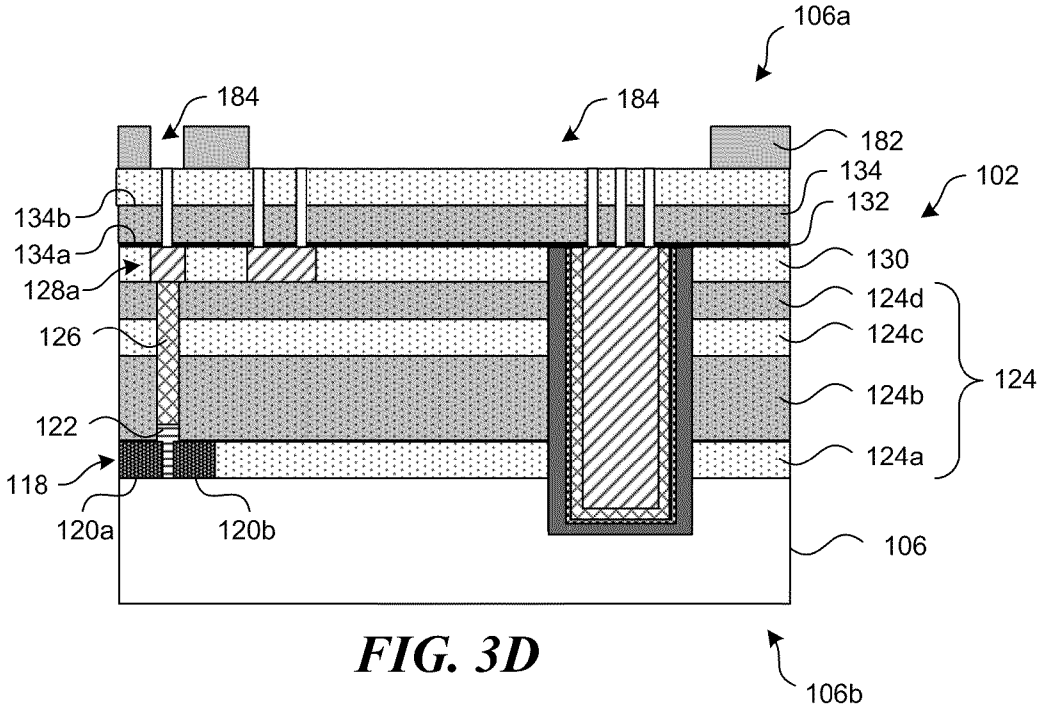

106a
184
184
182
134
102
134b
132
134a
130
128a
124d
126
124c
124
124b
122
124a
118
120a
120b
106
106b

FIG. 3D

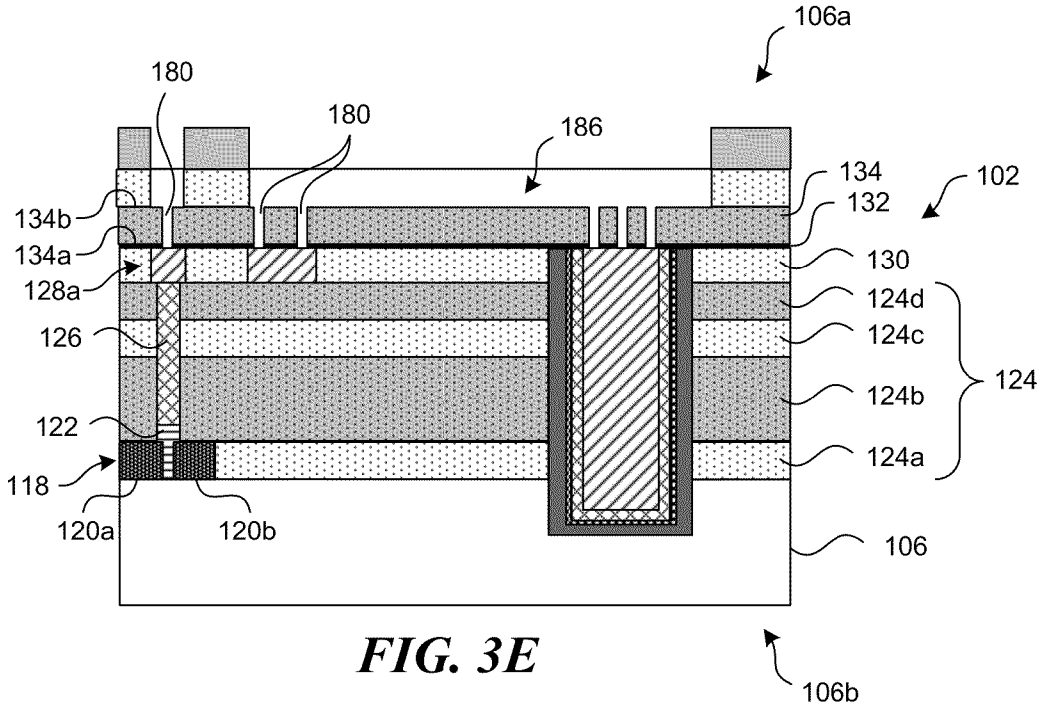

106a
180
180
186
134
102
132
134b
134a
130
128a
124d
126
124c
124
124b
122
124a
118
120a
120b
106
106b

FIG. 3E

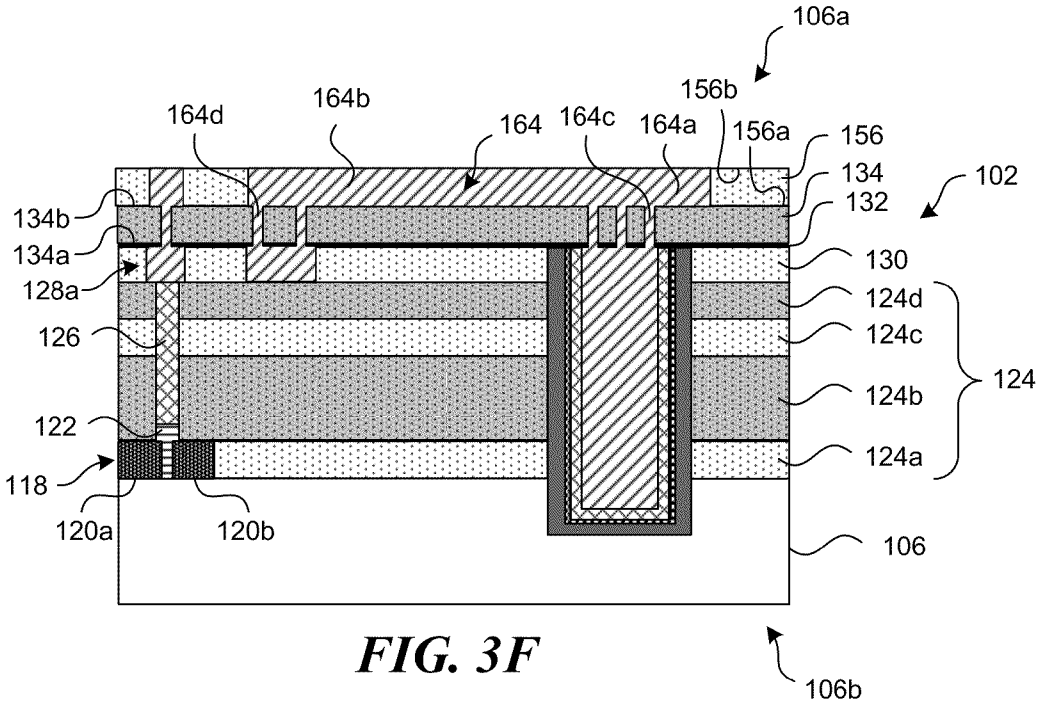

106a
156b
164d
164b
164
164c
164a
156a
156
134
102
132
134b
134a
130
128a
124d
126
124c
124
124b
122
124a
118
120a
120b
106
106b

FIG. 3F

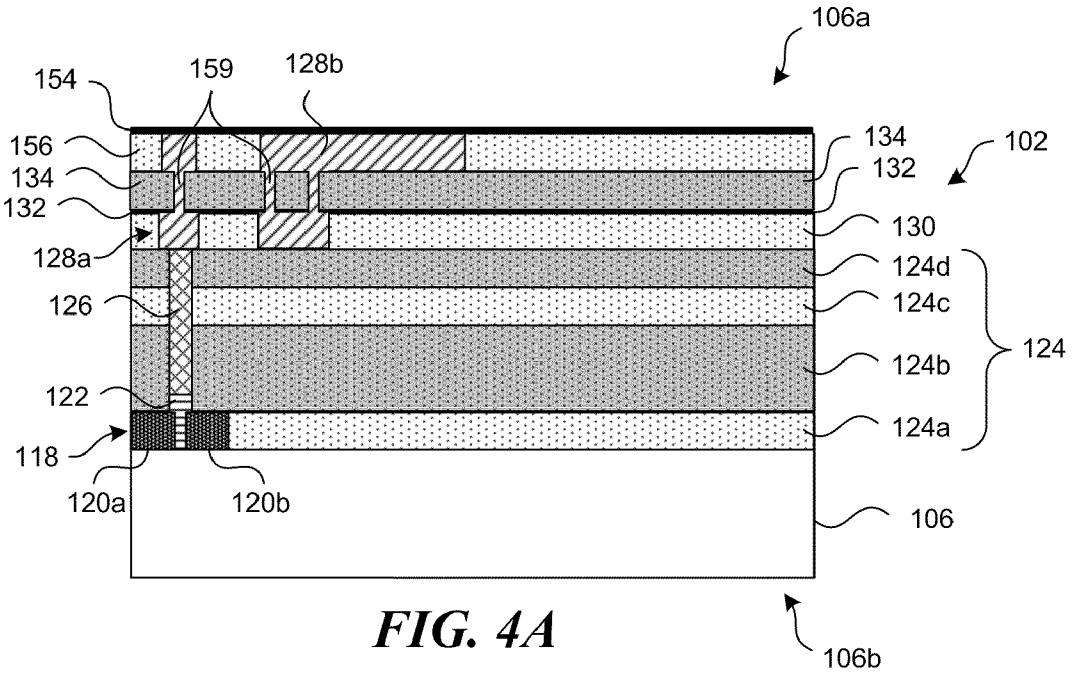

106a
154
159
128b
156
134
132
128a
126
122
118
120a
120b
134
132
102
130
124d
124c
124
124b
124a
106
106b

FIG. 4A

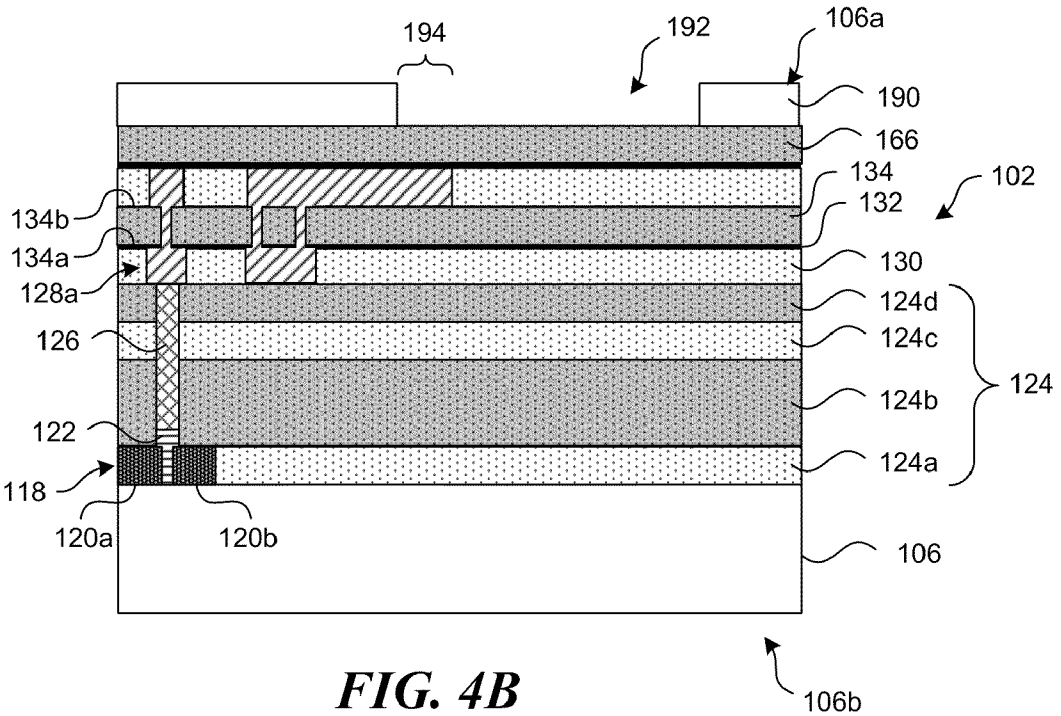

194
192
106a
190
166
134
132
102
134b
134a
128a
126
122
118
120a
120b
130
124d
124c
124
124b
124a
106
106b

FIG. 4B

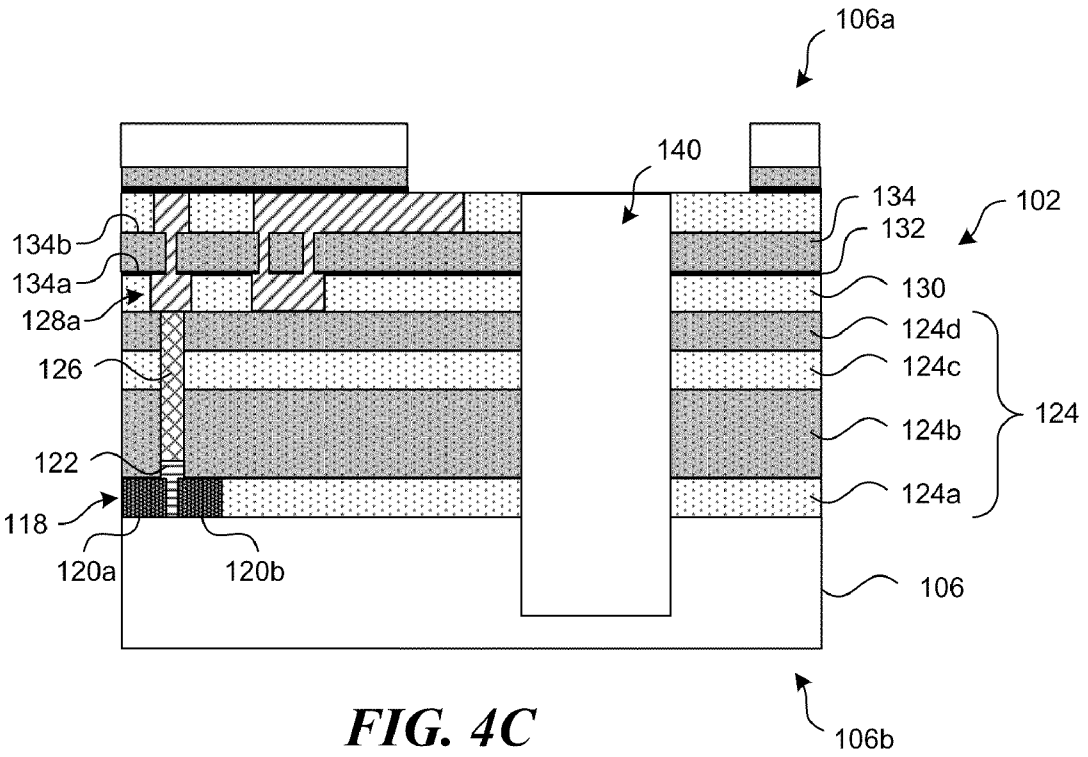

106a
140
134
102
132
134b
134a
130
128a
124d
126
124c
124
124b
122
124a
118
120a
120b
106
106b

FIG. 4C

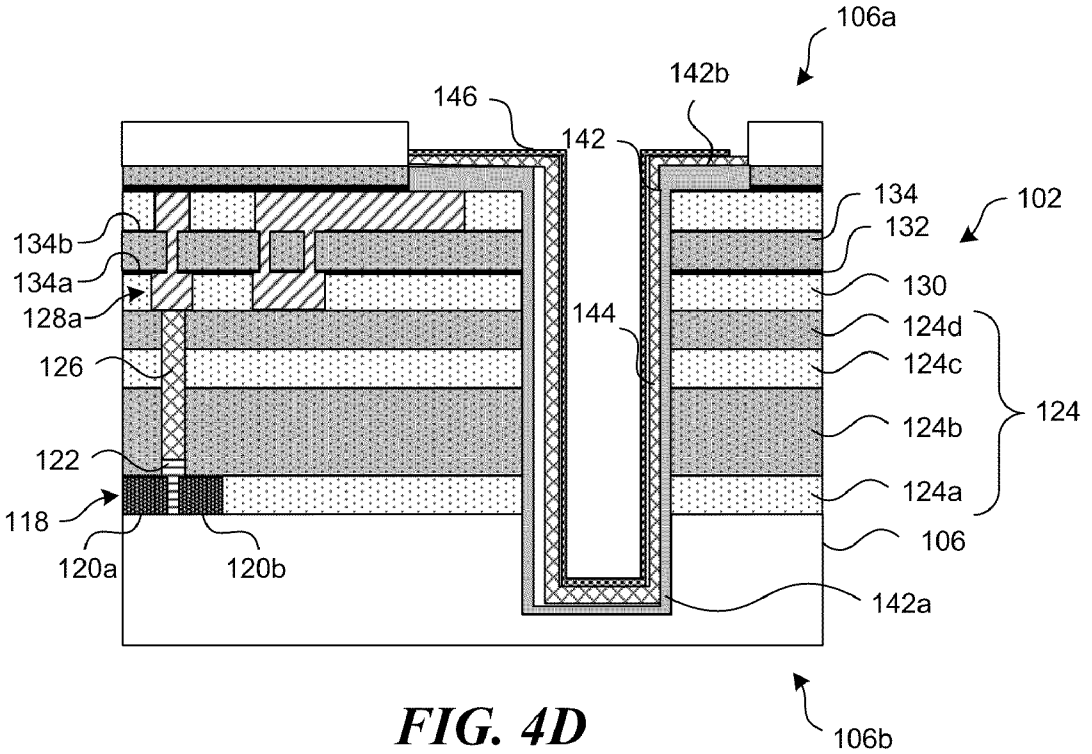

106a
142b
146
142
134
102
132
134b
134a
130
128a
144
124d
126
124c
124
124b
122
124a
118
106
120a
120b
142a
106b

FIG. 4D

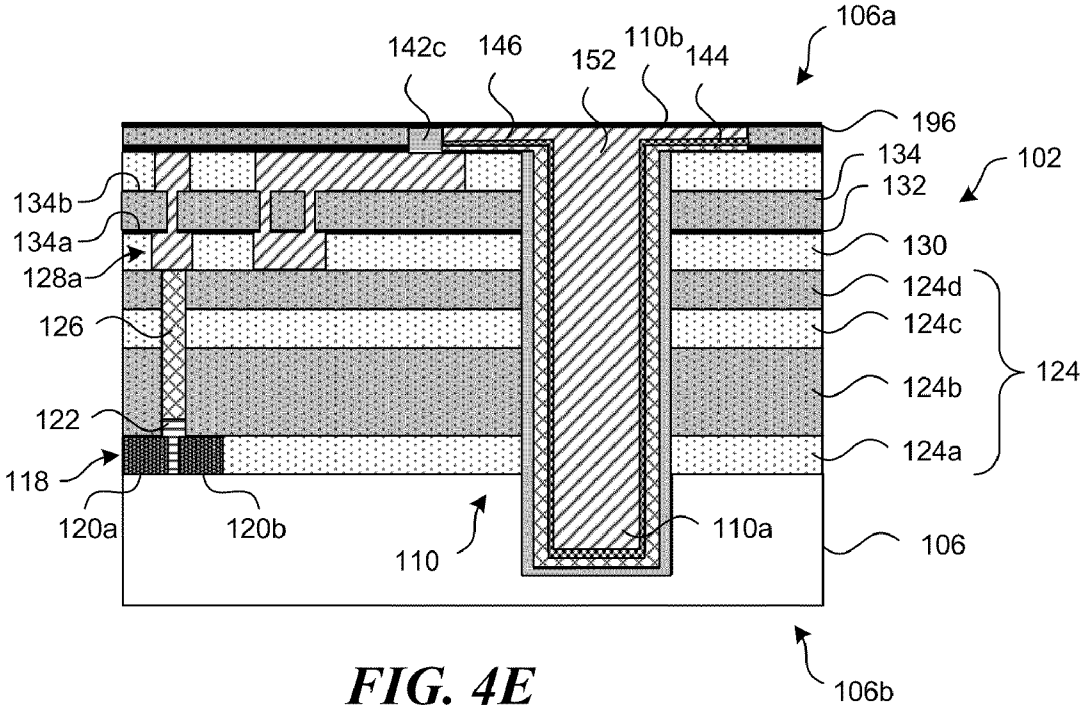

106a
142c
146
152
110b
144
196
134
102
132
134b
134a
128a
130
124d
126
124c
124
124b
122
124a
118
120a
120b
110
110a
106
106b

FIG. 4E

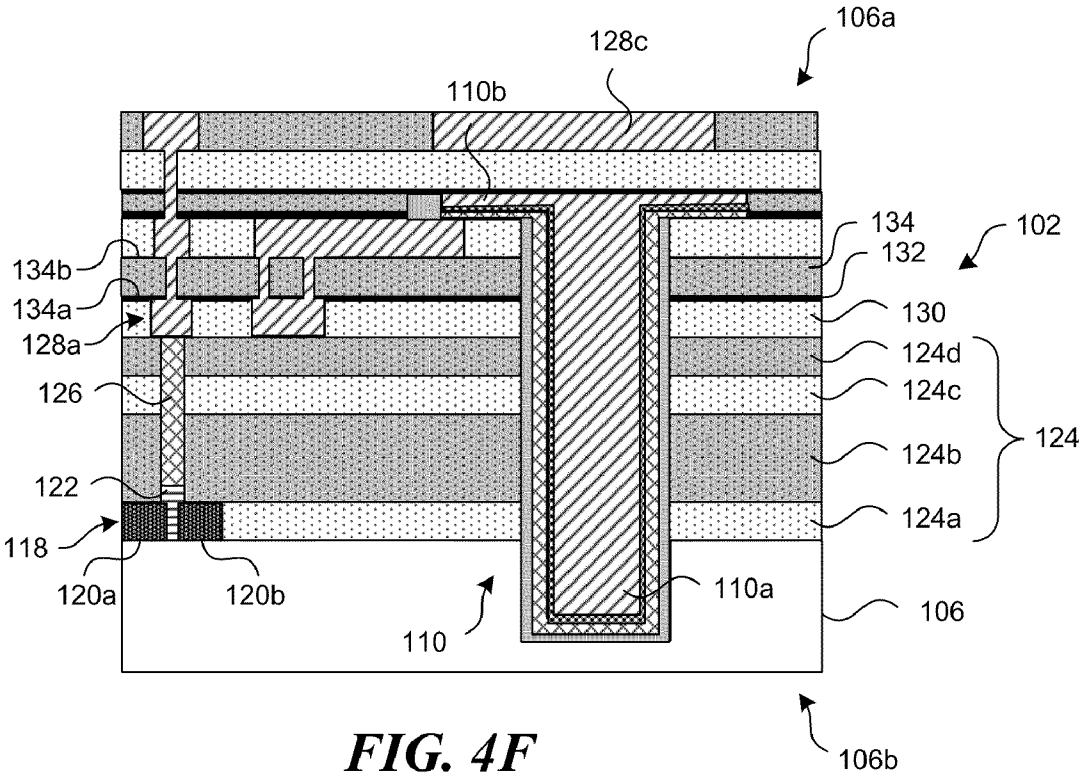

106a
128c
110b
134
102
132
134b
134a
130
128a
124d
126
124c
124
124b
122
124a
118
120a
120b
110a
106
110
106b

FIG. 4F

MICROELECTRONIC DEVICES WITH THROUGH-SUBSTRATE INTERCONNECTS AND ASSOCIATED METHODS OF MANUFACTURING

TECHNICAL FIELD

[0001] The present technology is directed generally to microelectronic devices with through-substrate interconnects and associated methods of manufacturing.

BACKGROUND

[0002] Semiconductor dies typically include a plurality of integrated circuits, bond-pads coupled to the integrated circuits, and metal routing layers for routing electrical signals between the bond-pads and external contacts. Fabricating and packaging such semiconductor dies include forming interconnects to electrically couple the bond-pads and/or metal routing layers to externally devices (e.g., a lead frame, a printed circuit board, etc.).

[0003] In some applications, the interconnects extend completely through or through a significant portion of the semiconductor dies (commonly referred to as "through-substrate interconnects"). One conventional process for forming through-substrate interconnects can include forming deep vias on the front and/or back side of a die in alignment with corresponding bond-pads. The vias are then filled with a conductive material (e.g., copper). Solder balls and/or other external electrical contacts are subsequently attached to the through-substrate interconnects.

[0004] The through-substrate interconnects may be formed (1) prior to integrating processing (commonly referred to as a "via-first" process), or (2) after the integration processing has been substantially completed (commonly referred to as a "via-last" process). However, both the via-first and via-last processes have certain drawbacks, as discussed in more detail later. Accordingly, several improvements to the process of through-substrate formation may be desirable.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] FIG. **1** is a schematic cross-sectional view of a microelectronic package with stacked dies in accordance with embodiments of the technology.

[0006] FIGS. **2**A-**2**N are schematic cross-sectional views of a portion of a semiconductor substrate undergoing a process useful for forming several embodiments of the semiconductor dies shown in FIG. **1** in accordance with embodiments of the technology.

[0007] FIGS. **3**A-**3**F are schematic cross-sectional views of a portion of a semiconductor substrate undergoing a process useful for forming several embodiments of the semiconductor dies shown in FIG. **1** in accordance with additional embodiments of the technology.

[0008] FIGS. **4**A-**4**F are schematic cross-sectional views of a portion of a semiconductor substrate undergoing a process useful for forming several embodiments of the semiconductor dies shown in FIG. **1** in accordance with yet additional embodiments of the technology.

DETAILED DESCRIPTION

[0009] Several embodiments of the present technology are described below with reference to processes for forming through vias and conductive routing layers in semiconductor substrates. Many details of certain embodiments are described below with reference to semiconductor dies. The term "semiconductor substrate" is used throughout to include a variety of articles of manufacture, including, for example, individual integrated circuit dies, imager dies, sensor dies, and/or dies having other semiconductor features.

[0010] Several of the processes described below may be used to form through vias and conductive routing layers in an individual die or in a plurality of dies, on a wafer or portion of a wafer. The wafer or wafer portion (e.g., wafer form) can include an unsingulated wafer or wafer portion, or a repopulated carrier wafer. The repopulated carrier wafer can include an adhesive material (e.g., a flexible adhesive) surrounded by a generally rigid frame having a perimeter shape that is comparable to that of an unsingulated wafer and can include singulated elements (e.g., dies) surrounded by the adhesive.

[0011] Many specific details of certain embodiments are set forth in FIGS. **1**-**4**F and the following text to provide a thorough understanding of these embodiments. Several other embodiments can have configurations, components, and/or processes different from those described below. A person skilled in the relevant art, therefore, will appreciate that additional embodiments may be practiced without several of the details of the embodiments shown in FIGS. **1**-**4**F.

[0012] FIG. **1** is a schematic cross-sectional view of a portion of a microelectronic package **100** in accordance with embodiments of the technology. As shown in FIG. **1**, the microelectronic package **100** can include a plurality of semiconductor dies **102** stacked in series with a plurality of conductive couplers **104** (e.g., solder balls). Four semiconductor dies **102** (identified individually as first, second, third, and fourth semiconductor dies **102***a*-**102***d*, respectively) are shown in FIG. **1** for illustration purposes. In other embodiments, the microelectronic package **100** can include any other desired number of semiconductor dies **102** coupled to one another with wirebonds, solder balls, conductive tapes, and/or other suitable electrical connectors.

[0013] The semiconductor dies **102** can individually include a semiconductor substrate **106** carrying a signal routing structure **108** proximate to a first side **106***a* of the semiconductor substrate **106**, a plurality of bond-pads **112** (identified individually as first to fifth bond-pads **112***a*-**112***e*, respectively) on the signal routing structure **108**, and a plurality of through-substrate interconnects **110** (identified individually as first to fourth interconnects **110***a*-**110***d*, respectively) extending between the first side **106***a* and a second side **106***b* of the semiconductor substrate **106**. The semiconductor dies **102** can also include an input/output ("I/O") buffer **114** associated with the first through-substrate interconnect **110***a* and a chip-select ("C/S") buffer **116** associated with the second, third, and fourth through-substrate interconnects **110***b*-**110***d*.

[0014] The through-substrate interconnects **110** can be selectively connected to certain metallization layers (not shown in FIG. **1**) in the signal routing structures **108** for carrying electrical signals between the first and second sides **106***a* and **106***b* of the semiconductor dies **102**. Details of several embodiments of a process for forming the signal routing structures **108** and the through-substrate interconnects **110** are discussed in more detail below with reference to FIGS. **2**A-**4**F.

[0015] The conductive couplers **104** can interface with corresponding bond-pads **112** based on a desired signal routing scheme. As shown in FIG. **1**, not all of the bond-pads **112** are electrically coupled to one of the conductive couplers **104**.

For example, the first through-substrate interconnect **110***a* of the first semiconductor die **102***a* is electrically coupled via the conductive couplers **104** and the first bond-pad **112***a* of the first semiconductor die **102***a*. In contrast, the second bond-pad **112***b* of all the semiconductor dies **102**, the third bond-pad **112***c* of the third semiconductor die **102***c*, and the third and fourth bond-pads **112***c* and **112***d* of the fourth semiconductor die **102***d* are not electrically coupled to any of the conductive couplers **104**. Instead, the signal routing structure **108** routes a chip-select signal (and/or other suitable signals) received at the second bond-pad **112***b* of the first semiconductor die **102***a* to the C/S buffer **116** of the fourth semiconductor die **102***d* via the second through-substrate interconnect **110***b* of the first semiconductor die **102***a*, the third through-substrate interconnect **110***c* of the second semiconductor die **102***b*, and the fourth through-substrate interconnect **110***d* of the third semiconductor die **102***c*.

[0016] In operation, the electrically coupled first through-substrate interconnect **110***a* of the semiconductor dies **102** forms an electrical path for carrying input/output signals to all the semiconductor dies **102**. The signal routing structures **108** of the individual semiconductor dies **102** route the input/output signals to the individual I/O buffers **114** of the semiconductor dies **102** from the electrical path. The signal routing structure **108** can also route a chip-select signal (and/or other suitable signals) to a selected semiconductor die **102** to enable processing the input/output signals received at the I/O buffer **114** at a selected semiconductor die **102**. For example, the signal routing structure **108** routes a chip-select signal received at the fifth bond-pad **112***e* to the C/S buffer **116** of the first semiconductor die **102***a* to enable the first semiconductor die **102***a* to process the received input/output signals. In another example, the signal routing structure **108** can also route a chip-select signal received at the fourth bond-pad **112***d* to the second semiconductor die **102***b* via the fourth through-substrate interconnect **110***d* of the first semiconductor die **102***a*.

[0017] In accordance with conventional techniques, the through-substrate interconnects **110** may be formed based on a via-first process or a via-last process. However, the inventors have recognized that both the via-first and via-last processes have certain drawbacks. For example, the via-last process may not adequately accommodate routing the chip-select signals because such modification may significantly add cost and/or complexity to the manufacturing process. For example, techniques that may be used to route signals at the last metallization layer can include (1) controlling the formation (or the lack of formation) of conductive bumps to an adjacent semiconductor die **102**; (2) routing the signals back down to the lower metallization layers; (3) adding control gates (e.g., MOSFET) to the signal routing structure **108**; (4) patterning each of the semiconductor dies **102** differently; and (5) adding a redistribution layer (not shown) on the semiconductor dies **102**.

[0018] The inventors also recognized that the via-first process may negatively impact the electrical reliability of the semiconductor dies **102** because the electrical contacts between the signal routing structures **108** and integrated circuits (not shown) in the semiconductor dies **102** may be damaged during formation of the signal routing structures **108**. Several embodiments of a process for addressing at least some of the foregoing drawbacks of the via-first and via-last processes are discussed below with reference to FIGS. **2**A-**2**N.

[0019] FIGS. **2**A-**2**N are schematic cross-sectional views of a portion of a semiconductor substrate **106** undergoing a process for forming several embodiments of the semiconductor dies **102** shown in FIG. **1** in accordance with embodiments of the technology. In the following description, similar processing operations may utilize generally similar processing techniques. As a result, suitable techniques for performing the processing operations (e.g., patterning a deposited material, removing portions of dielectric materials, depositing a conductive material, etc.) are described only once for brevity.

[0020] As shown in FIG. **2**A, the process can include forming an integrated circuit **118** in and/or on the first side **106***a* of the semiconductor substrate **106**. In the illustrated embodiment, the integrated circuit **118** is shown schematically as a field-effect transistor having a source **120***a*, a drain **120***b*, and a gate **122** for illustration purposes. In other embodiments, the integrated circuit **118** can also include vertical transistors, three-dimensional transistors, capacitors, and/or other suitable electrical components forming a dynamic random access memory (DRAM) and/or other suitable electronic devices.

[0021] The process can include forming an insulator **124** on the semiconductor substrate **106**. In the illustrated embodiment, the insulator **124** includes four layers of silicon oxide, silicon nitride, and/or other suitable dielectrics (identified individually as first to fourth insulation materials **124***a*-**124***d*, respectively). In other embodiments, the insulator **124** can also include another desired number of dielectric and/or other suitable insulation materials. Techniques for forming the insulator **124** can include thermal oxidation, chemical vapor deposition ("CVD"), atomic layer deposition ("ALD"), spin-on glass, and/or other suitable techniques.

[0022] The process can also include forming a conductive link **126** in the insulator **124** that is electrically connected to the integrated circuit **118**. In one embodiment, forming the conductive link **126** includes patterning the insulator **124** with photolithography and/or other suitable techniques, and removing a portion of the patterned insulator **124** to form an aperture **127** via wet etching, dry etching, reactive ion etching, and/or other suitable techniques. The aperture **127** may then be filled with a conductive material **129** (e.g., copper, aluminum, gold, and/or other suitable conductive materials) via physical vapor deposition (PVD), CVD, ALD, electroplating, and/or other suitable techniques. In other embodiments, forming the conductive link **126** may include other processing operations in addition to or in lieu of the foregoing operations.

[0023] The process can include forming the first metallization layer **128***a* by forming a first dielectric **130** on the insulator **124**, patterning the first dielectric **130** according to a desired metal routing profile, removing a portion of the first dielectric **130** to form trenches, channels, and/or other openings **135** in the first dielectric **130**, and depositing a conductive material **137** (e.g., copper, aluminum, gold, and/or other suitable conductive materials) in the openings **135**. The process can then include forming a first barrier **132** (e.g., BLOK provided by Applied Materials, Inc., Santa Clara, Calif.) on the first metallization layer **128***a* and depositing a second dielectric **134** (e.g., silicon oxide) on the first barrier **132**. The second dielectric **134** includes a first surface **134***a* proximate to the first barrier **132** and a second surface **134***b* opposite the first surface **134***a*.

[0024] After forming the first metallization layer **128***a*, FIGS. **2**B-**2**H illustrate a through-substrate interconnect formation process module (hereinafter referred to as the "TSV

module") for forming a through-substrate interconnect **110** (FIG. **1**) in the semiconductor substrate **106**. As shown in FIG. **2**B, the TSV module can include depositing a first photoresist **136** on the second dielectric **134** via spin coating and/or other suitable techniques. The first photoresist **136** can then be patterned to form a first opening **138**. As used herein, the term "photoresist" generally refers to a material that can be chemically modified when exposed to electromagnetic radiation. The term encompasses both positive photoresist that is configured to be soluble when activated by the electromagnetic radiation and negative photoresist that is configured to be insoluble when activated by light.

[0025] As shown in FIG. **2**C, the TSV module can include forming an interconnect aperture **140** in the semiconductor substrate **106**. The interconnect aperture **140** can be formed by removing material from the first dielectric **130**, the first barrier **132**, the second dielectric **134**, the insulator **124**, and at least a portion of the semiconductor substrate **106** via the opening **138** in a continuous operation. In other embodiments, forming the interconnect aperture **140** can include a first material removal operation (e.g., using wet etching) to remove a portion of the first dielectric **130**, the first barrier **132**, the second dielectric **134**, and the insulator **124**, and a second material removal operation (e.g., using reactive ion etching) to remove a portion of the semiconductor substrate **106**.

[0026] As shown in FIG. **2**D, the TSV module can further include removing the first photoresist **136** and sequentially forming an aperture insulator **142**, an aperture barrier **144**, and a seed material **146** in the interconnect aperture **140**. The aperture insulator **142** can include silicon oxide, silicon nitride, and/or other suitable insulation materials formed via thermal oxidation, CVD, ALD, and/or other suitable techniques. The aperture barrier **144** can include tantalum (Ta), tungsten (W), titanium nitride (TiN), and/or other suitable barrier materials formed via pulsed chemical vapor deposition ("pCVD"), ionic physical vapor deposition ("iPVD"), ALD, and/or other suitable techniques. The seed material **144** can include copper, tungsten, and/or other suitable conductive materials deposited via pCVD, iPVD, ALD, and/or other suitable techniques.

[0027] As shown in FIG. **2**E, the TSV module can also include depositing a second photoresist **148** on the seed material **146**. The second photoresist **148** can then be patterned to form a second opening **150**. As shown in FIG. **2**F, the TSV module can include filling the interconnect aperture **140** with a first conductive material **152** via the second opening **150** to form the through-substrate interconnect **110**. The first conductive material **152** includes a first portion **152***a* in the interconnect aperture **140** and a second portion **152***b* extending beyond the second dielectric **134**. The first conductive material **152** can include copper, aluminum, tungsten, gold, and/or alloys of the foregoing constituents. In particular embodiments, the first conductive material **152** includes electrolytic copper introduced into the interconnect aperture **140**. The electrolytic copper has an enhanced purity when compared to electrolessly disposed materials, and when compared to solder. For example, the first conductive material **152** can be at least 90% copper and in some cases 99% copper. The second photoresist **148** may then be removed.

[0028] As shown in FIG. **2**G, the second portion **152***b* (FIG. **2**F) of the first conductive material **152** can be subsequently removed such that the first portion **152***a* of the first conductive material **152** is generally planar with the second surface **134***b* of the second dielectric **134**. Techniques for removing the second portion **152***b* of the first conductive material **152** can include chemical-mechanical polishing ("CMP"), electrochemical-mechanical polishing ("ECMP"), and/or other suitable techniques. As shown in FIG. **2**H, the TSV module can optionally include depositing a second barrier **154** (e.g., BLOK provided by Applied Materials, Inc., Santa Clara, Calif.) on the second surface **134***b* of the second dielectric **134** and the first portion **152***a* of the first conductive material **152**. In other embodiments, depositing the second barrier **154** may be omitted.

[0029] Even though the TSV module discussed above includes depositing and patterning the second photoresist **148**, in certain embodiments, the second photoresist **148** may be omitted. Instead, the TSV module can include depositing the first conductive material **152** with the first portion **152***a* in the interconnect aperture **140** and the second portion **152***b* substantially covering the second surface **134***b* of the second dielectric **134**. Subsequently, at least a part of the second portion **152***b* may be removed to yield the through-substrate interconnect **110** as shown in FIG. **2**G.

[0030] Following the TSV module, the process can include forming a second metallization layer. As shown in FIG. **2**I, the process can include forming a third dielectric **156** on the optional second barrier **154**. The third dielectric **156** includes a first surface **156***a* proximate to the optional second barrier **154** and a second surface **156***b* opposite the first surface **156***a*. Then, a plurality of first vias **159** to the first metallization layer **128***a* may be formed through the third dielectric **156**, the optional second barrier **154**, and the second dielectric **134**.

[0031] The process can then include depositing a third photoresist **158** on the third dielectric **156** and patterning the third photoresist **158** to form third openings **160** corresponding to a desired routing profile for a second metallization layer **128***b* (not shown). As shown in FIG. **2**J, the process can include removing a portion of the third dielectric **156** and optionally a portion of the second barrier **154** to form openings **162**. The openings **162** expose at least a part of the second surface **134***b* of the second dielectric **134** and the upper surface of the first portion **152***a* of the first conductive material **152**.

[0032] As shown in FIG. **2**K, the process can include filling the openings **162** and first vias **159** with a second conductive material **164** and subsequently removing excess second conductive material **164** external to the openings **162** such that the second conductive material **164** is generally planar with the second surface **156***b* of the third dielectric **156**. In the illustrated embodiment, the second conductive material **164** includes a first portion **164***a*, a second portion **164***b* extending laterally away from the first portion **164***a*, and a third portion **164***c* in the first vias **159**. The first portion **164***a* of the second conductive material **164** is in direct physical contact with the first portion **152***a* of the first conductive material **152** of the through-substrate interconnect **110**. The third portion **164***c* of the second conductive material **164** electrically connects the second portion **164***b* and the first metallization layer **128***a*.

[0033] In one embodiment, the second conductive material **164** includes the same composition (e.g., copper) as the first conductive material **152**. As a result, the first and second conductive materials **152** and **164** may be generally homogeneous (a phantom line is used in FIG. **2**K to show an artificial demarcation between the first and second conductive materials **152** and **164**). In other embodiments, the second conductive material **164** may include a composition at least partially different than the first conductive material **152**. As a result, the

first metallization layer **128***a* is electrically connected to the through-substrate interconnect **110** via the second conductive material **164**.

[0034] After forming the second metallization layer **128***b*, the process can include forming additional metallization layers on the semiconductor substrate **106**. For example, FIGS. **2**L and **2**M illustrate operations of forming a third metallization layer **128***c*. As shown in FIG. **2**L, the process can include depositing a fourth dielectric **166** on the second surface **156***b* of the third dielectric **156** and the second metallization layer **128***b*. The deposited fourth dielectric **166** has a first surface **166***a* proximate to the third dielectric **156** and a second surface **166***b* opposite the first surface **166***a*. The process can then include patterning and removing a portion of the fourth dielectric **166** to form a plurality of second vias **168** extending from the second surface **166***b* of the fourth dielectric **166** to the second metallization layer **128***b*.

[0035] The third metallization layer **128***c* can then be formed following operations generally similar to those described with reference to FIGS. **2**I and **2**J. As shown in FIG. **2**M, the third metallization layer **128***c* includes a third conductive material **170** electrically connected to the second metallization layer **128***b* via the second vias **168**. In the illustrated embodiment, the third conductive material **170** has the same composition (e.g., copper) as the first and second conductive materials **152** and **164**. In other embodiments, the third dielectric material **170** may have a composition different from the first and/or second dielectric materials **152** and **164**.

[0036] In certain embodiments, the process can also include processing the semiconductor substrate **106** to form additional features in and/or on the semiconductor substrate **106**. For example, as shown in FIG. **2**N, a portion of the semiconductor substrate **106** can be removed from the second side **106***b* using a mechanical or chemical-mechanical technique to expose the through-substrate interconnect **110**. A conductive component **172** (e.g., a conductive pillar, a solder ball, a solder bump, a redistribution layer, a through-silicon via stud, and/or other suitable interconnect devices) can then be attached to the through-substrate interconnect **110** for interconnecting with an external component (not shown).

[0037] Even though only first, second and third metallization layers **128***a*, **128***b*, and **128***c* are illustrated in FIGS. **2**A-**2**M, in certain embodiments, the process can include forming four, five, or any desired number of metallization layers by repeating at least some of the operations discussed above with reference to FIGS. **2**L and **2**M. In these embodiments, the through-substrate interconnect **110** may be electrically connected to the second metallization layer **128***b*, the third metallization layer **128***c*, or the N−1 metallization layer (not shown).

[0038] Several embodiments of the foregoing process can reduce the risk of damaging the electrical connection between the first metallization layer **128***a* and the conductive link **126**. The inventors have observed that forming the through-substrate interconnect **110** before forming the first metallization layer **128***a* can result in a defective electrical connection between the first metallization layer **128***a* and the conductive link **126**. Without being bound by theory, it is believed that several operations during the formation of the first metallization layer **128***a* (e.g., deposition of the conductive material, removal of excess conductive material, etc.) may physically weaken and/or damage the electrical connection between the first metallization layer **128***a* and the conductive link **126**. As a result, by forming the through-substrate interconnect **110** subsequent to forming the first metallization layer **128***a*, the risk of creating a defective electrical connection may be lowered.

[0039] Several embodiments of the foregoing process can also be more cost-effective and flexible when compared to conventional techniques. For example, the selection of electrical connection between the through-substrate interconnect **110** and the metallization layers may be postponed until later processing stages than the via-first process. As a result, the number of generic intermediate products (i.e., semiconductor dies with partially formed metallization layers) may be increased to enable a production manager to continue producing the semiconductor dies **102** before making a decision concerning the final connection configuration of the semiconductor dies **102**.

[0040] Even though specific operations are discussed above with reference to FIGS. **2**A-**2**N for forming and connecting the second metallization layer **128***b* to the through-substrate interconnect **110**, in other embodiments, the second metallization layer **128***b* may be formed and connected to the through-substrate interconnect **110** with additional and/or different process operations. For example, FIGS. **3**A-**3**F are schematic cross-sectional views of a portion of a semiconductor substrate undergoing a process useful for forming several embodiments of the semiconductor dies **102** shown in FIG. **1** in accordance with additional embodiments of the technology. As shown in FIG. **3**A, the process can include forming the integrated circuit **118** in and/or on the semiconductor substrate **106**, forming the conductive link **126**, the first metallization layer **128***a*, and the first barrier **132** on the first metallization layer **128***a*, as discussed above with reference to FIG. **2**A.

[0041] Unlike the embodiment shown in FIG. **2**A, the process shown in FIG. **3**B can include utilizing the TSV module, as discussed above with reference to FIGS. **2**B-**2**H, before depositing the second dielectric **134** on the first barrier **132**. Subsequently, the second dielectric **134** may be formed on the first barrier **132** and the through-substrate interconnect **110**. As a result, the through-substrate interconnect **110** may be generally planar with the first barrier **132** and may be in direct contact with the first surface **134***a* of the second dielectric **134**.

[0042] As shown in FIG. **3**C, the process can include depositing the third dielectric **156** on the second dielectric **134**. As a result, the first surface **156***a* of the third dielectric **156** can be in direct contact with the second surface **134***b* of the second dielectric **134**. The process can include forming a plurality of access vias **180** in the second and third dielectrics **134** and **156** through the third dielectric **156**, the second dielectric **134**, and the barrier **132**. The access vias **180** include (1) a first group **180***a* of access vias **180** that generally correspond to the through-substrate interconnect **110**; and (2) a second group **180***b* of access vias **180** that generally correspond to the first metallization layer **128***a*.

[0043] The process can then include depositing a photoresist **182** on the third dielectric **156** and patterning the photoresist **182** to form openings **184** corresponding to a desired routing profile for the second metallization layer **128***b*. As shown in FIG. **3**E, the process can include removing a portion of the third dielectric **156** to form openings **186**. The openings **186** expose at least a part of the second surface **134***b* of the second dielectric **134** and are in communication with at least some of the access vias **180**.

[0044] As shown in FIG. **3**F, the process can include filling the openings **186** and the access vias **180** with the second conductive material **164**. Excess second conductive material **164** external to the openings **186** may then be removed such that the second conductive material **164** is generally planar with the second surface **156***b* of the third dielectric **156**. The second conductive material **164** includes a first portion **164***a*, a second portion **164***b* extending laterally away from the first portion **164***a*, a third portion **164***c* in the first group **180***a* of the access vias **180**, and a fourth portion **164***d* in the second group **180***b* of the access vias **180**. The third portion **164***c* of the second conductive material **164** electrically connects the first portion **164***a* of the second conductive material **164** to the through-substrate interconnect **110**. The fourth portion **164***d* of the second conductive material **164** electrically connects the second portion **164***b* of the second conductive material **164** to the first metallization layer **128***a*. The process can then include forming additional metallization layers and performing subsequent processing as discussed with reference to FIGS. **2**L-**2**N.

[0045] FIGS. **4**A-**4**F are schematic cross-sectional views of a portion of a semiconductor substrate **100** undergoing a process useful for forming several embodiments of the semiconductor dies **102** shown in FIG. **1** in accordance with yet additional embodiments of the technology. As shown in FIG. **4**A, the process can include forming the integrated circuit **118** in and/or on the semiconductor substrate **106**, forming the conductive link **126**, the first metallization layer **128***a*, and the first barrier **132** on the first metallization layer **128***a*, as discussed above with reference to FIG. **2**A. The process can also include forming the second metallization layer **128***b*, as discussed above with reference to FIGS. **2**H-**2**K. The process can then optionally include depositing the second barrier **154** on the second metallization layer **128***b*.

[0046] As shown in FIG. **4**B, the process can include forming the fourth dielectric **166** on the second barrier **154** and depositing a photoresist **190** on the fourth dielectric **166**. The photoresist **190** can then be patterned to form openings **192** corresponding to a portion of the second metallization layer **128***b* and the through-substrate interconnect **110** (not shown). As a result, a portion of the fourth dielectric **166** and the underlying second barrier **154** is exposed in the opening **192** (hereinafter referred to as the exposed portion **194**).

[0047] As shown in FIG. **4**C, the process can include forming the interconnect aperture **140** in the semiconductor substrate **106** and removing the exposed portion **194** (FIG. **4**B). In one embodiment, the interconnect aperture **140** may be formed and the exposed portion **194** may be removed in one continuous operation using a phase-shift mask, leaky-chrome mask, and/or other suitable techniques. In another embodiment, the interconnect aperture **140** may be formed by etching with a first mask (not shown) generally corresponding to the interconnect aperture **140**. The exposed portion **194** may be removed with a second mask (not shown) generally corresponding to the exposed portion **194**. In other embodiments, the exposed portion **194** may be removed via other suitable techniques.

[0048] As shown in FIG. **4**D, the process can include forming the aperture insulator **142** in the interconnect aperture **140**. In the illustrated embodiment, the aperture insulator **142** includes a first portion **142***a* in the interconnect aperture **140** and a second portion **142***b* external to the interconnect aperture **140**. The second portion **142***b* at least partially overlaps and is in direct contact with the second metallization layer **128***b*. In other embodiments, the aperture insulator **142** may only include the first portion **142***a* by using, for example, a photomask generally corresponding to the interconnect aperture **140** that was used when forming the aperture insulator **142**.

[0049] As shown in FIG. **4**E, the process can include at least partially removing the second portion **142***b* of the aperture insulator **142** and exposing the second metallization layer **128***b*. In one embodiment, the second portion **142***b* may be partially removed via a spacer etch. As a result, a part **142***c* of the second portion **142***b* remains on the second metallization layer **128***b*. In other embodiments, the second portion **142***b* may be partially removed via laser ablation and/or other suitable techniques. In further embodiments, the second portion **142***b* may be completely removed.

[0050] The process can then include depositing the aperture barrier **144** and the seed material **146** in the interconnect aperture **140**, as discussed above with reference to FIGS. **2**C. Then, the process can include filling the interconnect aperture **140** with the first conductive material **152**, and removing excess first conductive material **152** from the fourth dielectric **166**.

[0051] As shown in FIG. **4**F, the through-substrate interconnect **110** includes a vertical section **110***a* in the interconnect aperture **140** and a horizontal section **110***b* external to the interconnect aperture **140**. The horizontal section **110***b* extends laterally toward the second metallization layer **128***b* such that at least a portion of the horizontal section **110***b* is in direct contact with a top surface of the second metallization layer **128***b*. The process can optionally include forming a third barrier **196** on the fourth dielectric **166** and the through-substrate interconnect **110**. The process can then include forming additional metallization layers and performing subsequent processing as discussed with reference to FIGS. **2**L-**2**N to yield the semiconductor die **102** shown in FIG. **4**E.

[0052] From the foregoing, it will be appreciated that specific embodiments of the technology have been described herein for purposes of illustration, but that various modifications may be made without deviating from the technology. Many of the elements of one embodiment may be combined with other embodiments in addition to or in lieu of the elements of the other embodiments. Accordingly, the technology is not limited except as by the appended claims.

I/We claim:

1. A semiconductor device, comprising:

a semiconductor substrate;

first and second metallization layers, the second metallization layer being spaced apart from the semiconductor substrate with the first metallization layer therebetween; and

a conductive interconnect extending at least partially through the semiconductor substrate;

wherein the first metallization layer is in electrical contact with the conductive interconnect via the second metallization layer.

2. The semiconductor device of claim **1** wherein:

the semiconductor substrate includes a first side and a second side;

the second metallization layer includes a first portion generally corresponding to the conductive interconnect and a second portion extending laterally from the first portion; and

the semiconductor device also includes:

an insulation between the first side of the semiconductor substrate and the first metallization layer;

an integrated circuit on or in the semiconductor substrate;

a conductive link at least partially in the insulation, the conductive link being between the integrated circuit and the first metallization layer;

a dielectric between the first and second metallization layers; and

the dielectric includes a conductive via directly between the first metallization layer and the second portion of the second metallization layer;

the conductive interconnect includes a first end and a second end, the first end of the conductive interconnect being in direct contact with the first portion of the second metallization layer; and

a solder ball attached to the second end of the conductive interconnect at the second side of the semiconductor substrate.

3. The semiconductor device of claim **1** wherein:

the semiconductor substrate includes a first side and a second side;

the second metallization layer includes a first portion generally corresponding to the conductive interconnect and a second portion extending laterally from the first portion; and

the semiconductor device also includes:

an insulation between the first side of the semiconductor substrate and the first metallization layer;

an integrated circuit on or in the semiconductor substrate;

a conductive link at least partially in the insulation, the conductive link extending between the integrated circuit and the first metallization layer; and

a dielectric between the first and second metallization layers;

the conductive interconnect includes a first end and a second end opposite the first end;

the dielectric includes a first conductive via and a second conductive via spaced apart from the first conductive via, the first conductive via being directly between the first metallization layer and the second portion of the second metallization layer, the second conductive via being directly between the first portion of the second metallization layer and the first end of the conductive interconnect; and

a solder ball attached to the second end of the conductive interconnect at the second side of the semiconductor substrate.

4. The semiconductor device of claim **1** wherein:

the semiconductor substrate includes a first side and a second side;

the second metallization layer includes a first metallization surface opposite a second metallization surface; and

the semiconductor device also includes:

an insulation between the first side of the semiconductor substrate and the first metallization layer;

an integrated circuit on or in the semiconductor substrate;

a conductive link at least partially in the insulation, the conductive link being between the integrated circuit and the first metallization layer;

a dielectric between the first and second metallization layers; and

the dielectric includes a conductive via directly between the first metallization layer and the second metallization layer;

the conductive interconnect includes:

an aperture extending at least partially between the first and second sides of the semiconductor substrate;

a first section of a conductive material in the aperture;

a second section of the conductive material external to the aperture;

the second section of the conductive material extending laterally on the first section; and

the second section is in direct contact with at least a portion of the second metallization surface of the second metallization layer; and

a solder ball attached to the second end of the conductive interconnect at the second side of the semiconductor substrate.

5. The semiconductor device of claim **1** wherein:

the semiconductor device also includes a dielectric between the first and second metallization layers; and

the conductive interconnect includes a first end and a second end, the first end of the conductive interconnect being generally planar with the second surface of the dielectric, the second end being opposite the first end.

6. The semiconductor device of claim **1** wherein:

the semiconductor device also includes a dielectric between the first and second metallization layers; and

the conductive interconnect includes a first end and a second end, the first end of the conductive interconnect being in direct contact with the second metallization layer, the second end being opposite the first end.

7. The semiconductor device of claim **1** wherein:

the second metallization layer includes a first portion generally corresponding to the conductive interconnect and a second portion extending laterally from the first portion;

the semiconductor device also includes a dielectric between the first and second metallization layers, the dielectric having a first surface in direct contact with the first metallization layer and a second surface in direct contact with the second portion of the second metallization layer; and

the conductive interconnect includes a first end and a second end, the first end of the conductive interconnect being in direct contact with the first portion of the second metallization layer, the second end being opposite the first end.

8. The semiconductor device of claim **1** wherein:

the first metallization layer includes a first metallization surface proximate to the semiconductor substrate and a second metallization surface opposite the first metallization surface; and

the conductive interconnect includes a first end and a second end, the first end of the conductive interconnect being generally flush with the second metallization surface of the first metallization layer, the second end being opposite the first end.

9. The semiconductor device of claim **1** wherein:

the semiconductor device also includes a dielectric between the first and second metallization layers, the dielectric having a first surface in direct contact with the first metallization layer and a second surface opposite the first surface, the second surface being in direct contact with the second metallization layer;

the dielectric includes a first conductive via and a second conductive via spaced apart from the first conductive via;

the first conductive via is directly between the first metallization layer and the second metallization layer; and

the second conductive via is directly between the second metallization layer and the conductive interconnect.

10. The semiconductor device of claim **1** wherein the conductive interconnect includes:

an aperture extending at least partially in the semiconductor substrate;

a first section of a conductive material in the aperture;

a second section of the conductive material external to the aperture; and

the second section of the conductive material extending laterally from the aperture and is in direct contact with the second metallization layer.

11. A semiconductor device, comprising:

a semiconductor substrate;

a plurality of metal routing layers carried by the semiconductor substrate, the plurality of metal routing layers including 1, 2, . . . , N (N is a positive integer greater than 3) metal routing layers; and

a conductive interconnect extending at least partially through the semiconductor substrate, the conductive interconnect including an end proximate to the metal routing layers;

wherein the end of the conductive interconnect extends beyond or is generally flush with at least the first metal routing layer.

12. The semiconductor device of claim **11** wherein the end of the conductive interconnect extends beyond or is generally flush with the N−2 metal routing layer.

13. The semiconductor device of claim **11** wherein:

the end of the conductive interconnect extends beyond or is generally flush with the N−2 metal routing layer; and

the N−1 metal routing layer electrically connects the N−2 metal routing layer to the conductive interconnect.

14. The semiconductor device of claim **11** wherein the end of the conductive interconnect is in direct contact with the N−1 metal routing layer.

15. The semiconductor device of claim **11**, further comprising a conductive via between the end of the conductive interconnect and the N−1 metal routing layer.

16. The semiconductor device of claim **11** wherein the end of the conductive interconnect includes a first section and a second section extending laterally from the first section, the second section being in direct contact with the N−1 metal routing layer.

17. A method for fabricating a semiconductor device, comprising:

forming a first metallization layer on a semiconductor substrate;

forming an interconnect aperture at least partially in the semiconductor substrate after the first metallization layer is formed;

filling the interconnect aperture with a conductive material; and

forming a second metallization layer on the first metallization layer, the second metallization layer being in electrical contact with the conductive material in the interconnect aperture.

18. The method of claim **17** wherein:

forming an interconnect aperture includes:

depositing a first dielectric on the first metallization layer;

patterning the first dielectric and forming an opening generally corresponding to the interconnect aperture; and

etching the first dielectric and the semiconductor substrate via the opening;

filling the interconnect aperture includes:

introducing a first conductive material in the interconnect aperture; and

removing excess first conductive material external to the interconnect aperture; and

forming a second metallization layer includes:

depositing a second dielectric on the first dielectric and the conductive material in the interconnect aperture;

patterning the deposited second dielectric based on a desired profile of the second metallization layer; and

forming a via and a depression in the patterned second dielectric, the via exposing at least a portion of the first metallization layer, the depression exposing at least a portion of the first conductive material in the interconnect aperture; and

filling the via and the depression with a second conductive material, the second conductive material having a first portion in direct contact with the first conductive material in the interconnect aperture and a second portion in the via in direct contact with the first metallization layer.

19. The method of claim **17** wherein:

forming an interconnect aperture includes:

patterning the semiconductor substrate with the first metallization layer and forming an opening generally corresponding to the interconnect aperture; and

etching the semiconductor substrate via the opening;

filling the interconnect aperture includes:

introducing a first conductive material in the interconnect aperture; and

removing excess first conductive material external to the interconnect aperture; and

forming a second metallization layer includes:

depositing a first dielectric on the first metallization layer and the first conductive material in the interconnect aperture;

forming a first via and a second via in the first dielectric, the first via exposing at least a portion of the first metallization layer, the second via exposing at least a portion of the first conductive material in the interconnect aperture;

depositing a second dielectric on the first dielectric;

patterning the deposited second dielectric based on a desired profile of the second metallization layer;

forming a depression in the patterned second dielectric, the depression generally corresponding the to desired profile of the second metallization layer; and

filling the first and second vias and the depression with a second conductive material.

20. The method of claim **17** wherein:

forming a second metallization layer includes:

depositing a first dielectric on the first metallization layer;

patterning the first dielectric based on a desired profile of the second metallization layer;

forming a via and a depression in the first dielectric, the depression generally corresponding to the desired profile of the second metallization layer; and

filling the via and the depression with a first conductive material; and

forming an interconnect aperture includes:

depositing a second dielectric on the second metallization layer and the first dielectric;

patterning the second dielectric and forming an opening generally corresponding to the interconnect aperture and at least a portion of the second metallization layer;

etching the first and second dielectrics and the semiconductor substrate via the opening;

depositing an insulation material in the interconnect aperture and on the second metallization layer;

removing at least a portion of the insulation material on the second metallization layer; and

filling the interconnect aperture with a second conductive material via the opening, at least a portion of the second conductive material being in direct contact with the second metallization layer.

21. The method of claim **17** wherein:

the conductive material is a first conductive material; and

forming a second metallization layer includes:

depositing a dielectric on the conductive material in the interconnect aperture;

forming a depression in the dielectric, the depression exposing at least a portion of the conductive material in the interconnect aperture; and

filling the depression with a second conductive material, the second conductive material having a first portion in direct contact with the first conductive material in the interconnect aperture and a second portion extending laterally from the first portion.

22. The method of claim **17** wherein:

the conductive material is a first conductive material; and

forming a second metallization layer includes:

depositing a dielectric on the first metallization layer and the first conductive material in the interconnect aperture;

forming a first via and a second via in the dielectric, the first via exposing at least a portion of the first metallization layer, the second via exposing at least a portion of the first conductive material in the interconnect aperture; and

filling the first and second vias with a second conductive material.

23. The method of claim **17** wherein:

the conductive material is a first conductive material; and

forming an interconnect aperture includes:

depositing a dielectric on the second metallization layer;

forming the interconnect aperture through the dielectric and the semiconductor substrate;

exposing at least a portion of the second metallization layer; and

depositing a second conductive material in the interconnect aperture and onto the exposed portion of the second conductive material.

24. A method for fabricating a semiconductor device, comprising:

forming a first, second, . . . , and N^{th} metallization layers on a semiconductor substrate, N being a positive integer not less than 3;

forming an interconnect aperture at least partially in the semiconductor substrate at least after the first metallization layer is formed; and

filling the interconnect aperture with a conductive material, the conductive material being in electrical contact with at least one of the metallization layers.

25. The method of claim **24** wherein forming an interconnect aperture includes forming the interconnect aperture at least partially in the semiconductor substrate after the N−2 metallization layer is formed.

26. The method of claim **24** wherein:

forming an interconnect aperture includes forming the interconnect aperture at least partially in the semiconductor substrate after the N−2 metallization layer is formed; and

forming a first, second, . . . , and N^{th} metallization layers includes forming the N−1 metallization layer after filling the interconnect aperture with the conductive material.

27. The method of claim **24** wherein:

forming an interconnect aperture includes forming the interconnect aperture at least partially in the semiconductor substrate after the N−2 metallization layer is formed;

forming a first, second, . . . , and N^{th} metallization layers includes forming the N−1 metallization layer after filling the interconnect aperture with the conductive material; and

the method further includes directly contacting the N−1 metallization layer with the conductive material in the interconnect aperture.

28. The method of claim **24** wherein:

forming an interconnect aperture includes forming the interconnect aperture at least partially in the semiconductor substrate after the N−2 metallization layer is formed;

forming a first, second, . . . , and N^{th} metallization layers includes forming the N−1 metallization layer after filling the interconnect aperture with the conductive material; and

the method further includes forming a conductive via directly between the N−1 metallization layer and the conductive material in the interconnect aperture.

29. The method of claim **24** wherein:

forming an interconnect aperture includes forming the interconnect aperture at least partially in the semiconductor substrate after the N−1 metallization layer is formed; and

filling the interconnect aperture includes filling the interconnect aperture with the conductive material with a first portion in direct contact with the N−1 metallization layer and a second portion in the interconnect aperture.

30. The method of claim **24** wherein:

forming an interconnect aperture includes forming the interconnect aperture at least partially in the semiconductor substrate after the N−1 metallization layer is formed;

the method further includes exposing at least a portion of the N−1 metallization layer; and

filling the interconnect aperture includes introducing the interconnect aperture into the interconnect aperture and onto the exposed portion of the N−1 metallization layer.

* * * * *