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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
95/000,546	05/11/2010	7289386	19473-0052RX1	8688

79141 7590 02/25/2015
The Law Office of Jamie Zheng, Ph.D Esq.
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EXAMINER
PEIKARI, BEHZAD

ART UNIT	PAPER NUMBER
3992	

MAIL DATE	DELIVERY MODE
02/25/2015	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
95/000,577	10/20/2010	7289386	17730-3	7888

79141 7590 02/25/2015
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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

GOOGLE INC.
'546 Requester,[1] Respondent, and Cross-Appellant

and

SMART MODULAR TECHNOLOGIES
'577 Requester and Respondent
v.

NETLIST, INC.
Patent Owner, Appellant, and Cross-Respondent

Appeal 2014-007777
Inter partes Reexamination Control 95/000,546 & 95/000,577[2]
United States Patent 7,289,386
Technology Center 3900

Before JOHN A. JEFFERY, KEVIN F. TURNER, and STANLEY M. WEINBERG, *Administrative Patent Judges*.

JEFFERY, *Administrative Patent Judge*.

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[1] Because this appeal involves two different requesters from respective *inter partes* reexamination proceedings that were merged, we refer to (1) Google Inc., the Requester in the 95/000,546 proceeding, as "the '546 Requester," and (2) SMART Modular Technologies, the Requester from the 95/000,577 proceeding, as "the '577 Requester."

[2] These two reexamination proceedings were merged on March 3, 2011.

DECISION ON APPEAL

Patent Owner appeals under 35 U.S.C. §§ 134 and 315 the Examiner's decision to reject claims 38, 48, and 56–58. Claims 1–37, 39–47, 49–55, 59, and 60 were cancelled. The '546 Requester cross-appeals under 35 U.S.C. §§ 134 and 315 the Examiner's decision declining to reject claims 56–58 on other grounds.[2]

We have jurisdiction under 35 U.S.C. §§ 134 and 315, and we heard the appeal on November 19, 2014.[3] We affirm.

STATEMENT OF THE CASE

This proceeding arose from a first request for *inter partes* reexamination filed on behalf of the '546 Requester, on May 11, 2010, of United States Patent 7,289,386 ("the '386 patent"), issued to Bhakta et al. on October 30, 2007. This proceeding was assigned Control No. 95/000,546.

A second request for *inter partes* reexamination was filed on behalf of the '577 Requester on October 20, 2010, and was assigned Control No. 95/000,577. These two proceedings were merged on March 3, 2011.

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[2] Although the '546 Requester appeals the Examiner's decision declining to adopt the proposed (1) anticipation rejection of claims 1–9, 11, and 12 ("Issue 8") and (2) § 112 rejection of claims 45 and 46 ("Issue 16") on page 3 of the Cross Appeal Brief filed October 1, 2013, these claims were cancelled, thus rendering these issues moot. *Accord* Ans. 1 (noting this cancellation); Patent Owner's Respondent Brief in Cross Appeal, filed November 1, 2013, at 7 (noting this mootness). Accordingly, only the Examiner's decision declining to reject claims 38 and 56–58 on the grounds identified in connection with Issues 34, 37, and 38 on page 3 of '546 Requester's cross-appeal brief are before us in the cross-appeal.

[3] Throughout this opinion, we refer to the transcript of this oral hearing filed February 6, 2015 ("Tr.").

The '386 patent relates to computer system memory modules. In one aspect, a memory module can be fabricated using less expensive, lower-density memory devices, yet simulate a virtual module with more expensive, higher-density devices. To this end, plural double-data-rate (DDR) dynamic random-access memory (DRAM) devices have at least one attribute, such as the number of ranks of such devices or the memory density per rank, whose value is characterized as different from its actual value. *See generally* '386 patent, col. 4, ll. 47–63; col. 9, l. 23–col. 12, l. 11. Claim 56 illustrates the invention and is reproduced below with our emphasis:

> 56. A memory module connectable to a computer system, the memory module comprising:
>
> a printed circuit board;
>
> a plurality of memory devices coupled to the printed circuit board, the plurality of memory devices having a first number of memory devices; and
>
> a logic element coupled to the printed circuit board, the logic element receiving a set of input control signals from the computer system, the set of input control signals corresponding to a second number of memory devices smaller than the first number of memory devices, the logic element generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of memory devices, wherein the plurality of memory devices are arranged in a first number of ranks, and the set of input control signals corresponds to a second number of ranks of memory modules, the second number of ranks less than the first number of ranks, wherein the logic element further responds to a first command signal from the computer system by generating a second command signal transmitted to the

> plurality of memory devices, the first command signal corresponding to the second number of ranks and the second command signal corresponding to the first number of ranks,
>
> wherein the plurality of memory devices is a plurality of double-data-rate (DDR) dynamic random-access memory (DRAM) devices, wherein the plurality of memory devices has at least one attribute selected from a group consisting of: a number of row address bits per DDR DRAM device, a number of column address bits per DDR DRAM device, a number of DDR DRAM devices, a data width per DDR DRAM device, a memory density per DDR DRAM device, a number of ranks of DDR DRAM devices, and a memory density per rank, the memory module further comprising an electrically erasable programmable read-only non-volatile memory device storing data accessible to the computer system, *wherein the data characterizes the plurality of memory devices as having at least one value of the at least one attribute that is different from an actual value of the at least one attribute of the plurality of memory devices.*

RELATED PROCEEDINGS

This appeal is said to be related to various pending proceedings. First, the parties inform us that three co-pending litigations have been stayed: one of which (*Google v. Netlist*)[4] was stayed pending the present reexamination and two others (*Netlist, Inc. v. Inphi Corp*. and *Netlist v. Google*) stayed pending the reexaminations (Control Nos. 95/000,578, 95/000,579, 95/001,339, 95/001,381, and 95/001,337) of three other related patents. PO App. Br. 4; '577 TPR Resp. Br. 1; '546 TPR Resp. Br. 1 (accepting Patent

[4] The full citations of the related proceedings are found in the parties' respective statements and are omitted here for brevity.

Owner's statement of the status of related proceedings).[5] The '386 patent is also said to be related to U.S. Patent 7,864,627 that is being re-examined (95/001,758). PO App. Br. 4; '577 TPR Resp. Br. 1. The '577 Requester's related proceedings statement is similar to that of Patent Owner, but adds *Netlist Inc. v. MetaRAM Inc.*, which is said to be closed in the U.S. District Court for the District of Delaware. '577 TPR Resp. Br. 1.

Two of the above-noted reexaminations (95/001,337 and 95/001,381) were involved in earlier appeals where we rendered decisions. *See Inphi Corp. v. Netlist, Inc.*, No. 2013-009044 (PTAB Jan. 16, 2014) (affirming the Examiner's decision declining to adopt various proposed rejections in part); *see also Inphi Corp. v. Netlist, Inc.*, No. 2013-009066 (PTAB Jan. 16, 2014), *reh'g denied* (PTAB Aug. 13, 2014) (affirming the Examiner's decision declining to adopt various proposed rejections).

THE APPEALED REJECTIONS AND PROPOSED REJECTIONS

Patent Owner appeals the Examiner's adopting the following proposed rejections:

[5] Throughout this opinion, we refer to (1) the Right of Appeal Notice mailed June 21, 2013 ("RAN"); (2) Patent Owner's Appeal Brief filed October 2, 2013 ("PO App. Br."); (3) the '546 Requester's Respondent Brief filed November 1, 2013 ("'546 TPR Resp. Br."); (4) the '577 Requester's Respondent Brief filed November 4, 2013 ("'577 TPR Resp. Br."); (5) the Examiner's Answer mailed February 24, 2014 ("Ans.") (incorporating the RAN by reference); (6) the '546 Requester's Cross Appeal Brief filed October 1, 2013 ("'546 TPR App. Br."); and (7) Patent Owner's Respondent Brief in Cross Appeal filed November 1, 2013 ("PO Resp. Br.").

Claims 38, 48, and 56–58 under 35 U.S.C. § 103(a) as obvious over Amidi (US 2006/0117152 A1; June 1, 2006) and "JEDEC standards".[6] RAN 14, 28, 37–38. ("Issue 29").

Claims 38, 48, and 56–58[7] under 35 U.S.C. § 103(a) as obvious over Amidi and Dell (US 6,446,184 B2; Sept. 3, 2002). RAN 14, 29, 37–38. ("Issue 31").

The '546 Requester cross-appeals the Examiner's declining to reject the claims as follows:[8]

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[6] The Examiner indicates that "JEDEC Standards" refers collectively to three different JEDEC documents, namely (1) *Double Data Rate (DDR) SDRAM Specification*, JEDEC Standard No. 79C (Mar. 2003) ("JEDEC 79C"); (2) *Design Specification for PC2100 and PC I600 DDR SDRAM Registered DIMM JEDEC Standard No. 21-C*, Rev. 1.3, Rel. 11b (Jan. 2002) ("JEDEC 21C"); and (3) JEDEC Standard, *Definition of the SSTV16859 2.5v 13-bit to 26-bit SSTL_2 Registered Buffer for Stacked DDR DIMM Applications*, JESD 82-4B, JEDEC Solid State Tech. Ass'n (2003) ("JEDEC 82-4B"). RAN 6. *Accord* '577 TPR Resp. Br. 2 n.3.

[7] Although the Examiner's statement of the rejection includes cancelled claims 45 and 46 (RAN 14, 29), we nonetheless omit those claims here for clarity. We also include claim 48 in this rejection despite the Examiner's omitting this claim from the rejection. *See* RAN 14, 29. Our presumption that the Examiner intended to reject claim 48 over Amidi and Dell is consistent with that of the parties. *See* PO App. Br. 8 (including claim 48 in this rejection); '577 TPR Resp. Br. 2 (same); '546 TPR Resp. Br. 2 (accepting Patent Owner's statement of the issues to be reviewed on appeal). *Accord* Tr. 8–9, 15–16 (confirming the presumption that the Examiner intended to reject claim 48 over Amidi and Dell due to the Examiner's incorporating by reference claim charts that include claim 48).

[8] Although the '546 Requester cross-appeals the Examiner's declining to reject (1) claims 1–9, 11, and 12 as anticipated by Amidi ("Issue 8") and (2) claims 45 and 46 under § 112 ("Issue 16") ('546 TPR App. Br. 3–8)—these

Claims 38 and 56–58 under 35 U.S.C. § 103(a) as obvious over Amidi and "JEDEC specifications."[9] RAN 15, 30, 39. ("Issue 34").

Claims 56–58 under 35 U.S.C. § 112(a) as overly broad. RAN 15, 31–32, 39. ("Issue 37").

Claims 56–58 under 35 U.S.C. § 112(b) as not directed to the subject matter that the inventors regard as their invention. RAN 15, 32, 39. ("Issue 38").[10]

THE OBVIOUSNESS REJECTION OVER AMIDI AND "JEDEC STANDARDS" ("ISSUE 29")

The Examiner finds that Amidi and the JEDEC standards collectively teach or suggest all recited limitations of independent claim 56 for the reasons indicated in Section VI.C of the '577 Requester's Comments filed February 13, 2012, and the claim chart of Exhibit CC-F, which the Examiner incorporates by reference. RAN 14, 28. The Examiner also incorporates by

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claims were cancelled, thus rendering these issues moot. *Accord* PO Resp. Br. 7 (noting this point). Accordingly, we omit those moot issues here for clarity and brevity.

[9] The Examiner indicates that "JEDEC specifications" refers collectively to two different JEDEC documents, namely JEDEC 79C and JEDEC 21C. RAN 6.

[10] Although page 2 of the '546 Requester's Notice of Cross Appeal filed August 2, 2013, characterizes both Issues 37 and 38 as pertaining to rejections under § 112(a), the Examiner indicates that Issue 38 pertains to a proposed rejection under § 112(b)—not § 112(a) as is the case for Issue 37. RAN 15, 32. *Accord* '546 TPR Comments filed Jan. 2, 2013, at 3–4 (distinguishing the proposed § 112 rejections of claims 56–58 as under § 112(a) and (b), respectively). Accordingly, we adopt the Examiner's undisputed characterization here.

reference pages 3 to 8 of the '577 Requester's comments filed January 2, 2013 in connection with this rejection. RAN 38. Both Requesters concur with the Examiner's findings and conclusions. *See* '546 TPR Resp. Br. 3–7; *see also* '577 TPR Resp. Br. 5–13.

Patent Owner argues that the Examiner's reliance on information stored in Amidi's SPD 414[11] in paragraph 40 is flawed, for Amidi is said to say nothing about the content of this information, let alone that it characterizes plural memory devices as having an attribute different from their actual attributes as claimed. PO App. Br. 8–9. According to Patent Owner, ordinarily skilled artisans would understand that Amidi's SPD holds information that characterizes accurately the memory devices' attributes for the Basic Input/Output System (BIOS) during power-up so that the computer system can operate properly. *Id.* at 12–13. Characterizing these attributes inaccurately by altering the SPD's data is said to result in various memory-operation problems, including data collisions during back-to-back adjacent read commands. *Id.* at 13–16. Because Amidi is said to provide no solution to these problems, Patent Owner reasons that skilled artisans would consider Amidi's SPD as characterizing the memory devices as they actually are. *Id.* The JEDEC standards are also said to be deficient in this regard. *Id.* at 17.

[11] Although Amidi does not define the acronym "SPD," it nonetheless refers to a serial presence detect EEPROM device that stores data accessible by the computer system. *See* Declaration of Nader Bagherzadeh (dated Oct. 26, 2011), Ex. OTH-F, filed Nov. 1, 2013 ("Bagherzadeh Decl.") ¶ 43.

ISSUE

Under § 103, has the Examiner erred in rejecting claim 56 by finding that Amidi and the JEDEC standards would have collectively taught or suggested a memory module comprising an electrically erasable programmable read-only non-volatile memory device storing data accessible to a computer system, where the data characterizes plural memory devices as having at least one value of at least one of the recited attributes that is different from an actual value of the at least one attribute ("the attribute limitation")[12]?

ANALYSIS

We begin by noting that the point of Amidi's invention is to simulate a two-rank memory module by using a four-rank module on one memory socket as the Requesters indicate. *See* '546 TPR Resp. Br. 4 (citing Amidi ¶ 62; claim 20); '577 TPR Resp. Br. 5–8 (citing Amidi ¶¶ 40–41, 62; claim 23). The dispute before us, however, hinges on the SPD's role in this simulation, namely whether Amidi at least suggests that the information that it provides to the BIOS characterizes memory-device attribute values differently from their actual values as claimed. On this record, we find that the weight of the evidence favors the Examiner's position in this regard.

As shown in Amidi's Figure 4A, memory module 400 includes, among other things, SPD 414—an interface EEPROM that holds information regarding the memory module for BIOS during the power-up

[12] For brevity, we adopt the '577 Requester's label (the "attribute limitation") to refer to this disputed limitation in claim 56. *See* '577 TPR Resp. Br. 3.

sequence. Amidi ¶¶ 37, 40. Amidi's memory module also includes a complex programmable logic device (CPLD) 410 that emulates a two-rank memory module on the four-rank memory module 400. Amidi ¶¶ 37, 41. To this end, the CPLD determines which of the four ranks to activate based on address and command signals using the algorithms in Figures 5 and 7. Amidi ¶¶ 41, 43–44, 62.

To be sure, Amidi is short on specifics regarding the SPD's role in this emulation apart from the single sentence in paragraph 40 indicating that the SPD holds information *regarding the memory module* for BIOS during power-up. But our emphasis above highlights the fact that although this information's content is undisclosed, it nonetheless pertains to the memory module of which the SPD is a part—the very module configured to emulate a module with a different number of ranks as the '546 Requester indicates. *See* '546 TPR Resp. Br. 4–6 (citing Declaration of Dr. Christoforos Kozyrakis filed Nov. 1, 2013 ("Kozyrakis Decl.") ¶ 18(f); Bagherzadeh Decl. ¶¶ 28, 89). Dr. Bagherzadeh emphasizes this point in his supplemental declaration, noting that because the information on Amidi's SPD describes what the system's memory controller *expects*—not what it actually *has*—skilled artisans would understand that the memory module detects information that characterizes the memory devices' configuration differently from their actual configuration. Declaration of Nader Bagherzadeh, Ph.D. (dated Jan. 1, 2012) filed Jan. 2, 2013 ("Supp. Bagherzadeh Decl.") ¶¶ 4–6.

To be sure, Dr. Sechen opines that there is *no absolute requirement* at boot-up for Amidi's SPD to provide information characterizing what the computer system expects as Dr. Bagherzadeh declares. Supplemental

Declaration of Dr. Carl Sechen (dated Dec. 3, 2012), filed Oct. 2, 2013 ("Supp. Sechen Decl.") ¶ 27. But even assuming, without deciding, that this is the case, the lack of an absolute requirement in Amidi does not obviate Amidi at least *suggesting* that the SPD provide such information at boot-up for proper operation, particularly in view of Amidi's memory module emulation function—a memory module of which the SPD is a part as noted above. *Accord* '546 TPR Resp. Br. 5 (citing Kozyrakis Decl. ¶¶ 16–17, 18(f); Bagherzadeh Decl. ¶¶ 28, 45, 89–90).

On the other hand, Dr. Sechen declares that skilled artisans would not have modified Amidi's SPD to store data characterizing the memory devices as having an attribute different from an actual attribute, and that such an alteration would render Amidi inoperable due to data collisions during back-to-back adjacent read commands that cross device boundaries. Supp. Sechen Decl. ¶¶ 18, 22–30. Although we appreciate Dr. Sechen's insights in this regard, claim 56 does not require performing back-to-back adjacent reads as the '546 Requester indicates. *See* '546 TPR Resp. Br. 7. Therefore, Patent Owner's arguments in this regard (PO App. Br. 13–15) are not commensurate with the scope of the claim.

But even if the claim required performing such back-to-back reads (which it does not), whether Amidi is sufficiently enabled to deal with those reads is immaterial to the obviousness analysis as both Requesters correctly indicate. '546 TPR Resp. Br. 7; '577 TPR Resp. Br. 11–12. It is well settled that published subject matter is prior art for all that it teaches in obviousness determinations—even if the reference itself is not enabling. *See In re Antor Media Corp.*, 689 F.3d 1282, 1292 (Fed. Cir. 2012) (citing

Symbol Techs. Inc. v. Opticon Inc., 935 F.2d 1569, 1578 (Fed. Cir. 1991)). To be sure, the prior art must enable skilled artisans to make and use the claimed invention to render that invention obvious. *In re Kumar*, 418 F.3d 1361, 1368-69 (Fed. Cir. 2005). But this requirement is not based solely on the prior art references themselves, but also those references considered together with the knowledge of ordinarily skilled artisans. *In re Paulsen*, 30 F.3d 1475, 1480-81 (Fed. Cir. 1994) (citations and internal quotation marks omitted). Cited references, therefore, do not have to explain every detail to render a claimed invention obvious because the references speak to those skilled in the art. *Id.* at 1480.

Here, there is no persuasive evidence on this record to prove that the Examiner's modification to Amidi would have been beyond the level of ordinarily skilled artisans. Nor is there persuasive evidence on this record to rebut Amidi's presumption of operability apart from conclusory statements as the '577 Requester indicates. '577 TPR Resp. Br. 12 (citing *In re Sasse*, 629 F.2d 675 (CCPA 1980)).

Nor has Patent Owner persuasively rebutted Dr. Bagherzadeh's countervailing statement that even if timing problems arise in Amidi resulting from such an implementation, skilled artisans would nonetheless be able to solve such problems without undue experimentation by, for example, configuring a memory controller to use the appropriate timing sequences without requiring the SPD to describe the memory devices' configuration accurately. Supp. Bagherzadeh Decl. ¶ 6. Although this statement lacks

corroborating evidence which tends to weaken its probative value,[13] Dr. Sechen's countervailing statements in this regard suffer from the same weakness. On this particular problem-resolution issue, then, the contradictory expert declarations are in counterpoise: no declaration is more or less persuasive than the other. But what we can say is that no persuasive evidence has been shown on this record to rebut the Examiner's position that is premised on what would have been obvious to ordinarily skilled artisans in light of Amidi's disclosure, presumption of operability, and its teachings considered in light of the JEDEC standards.

Patent Owner's argument that Dell places Amidi's limited disclosure of the SPD "in proper context for one of ordinary skill in the art" (PO App. Br. 12) is likewise unavailing. As the '577 Requester indicates, the Examiner did not cite Dell in this particular rejection, let alone for teaching the disputed attribute limitation. '577 TPR Resp. Br. 10–11. Rather, Dell was cited in an alternative obviousness rejection of claim 56 ("Issue 31"). Nevertheless, to the extent that Dell has some relevance to the Examiner's rejection based solely on Amidi and the JEDEC standards ("Issue 29") at least with respect to setting forth the state of the art (*see* Tr. 11:8–15), we find Patent Owner's arguments in this regard unpersuasive.

According to Patent Owner, Dell's SPD device provides the actual—not expected—configuration at boot-up, namely the "original" or initial SPD data in steps 202 to 204 in Figure 2. PO App. Br. 12. But after boot-up,

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[13] *Accord* PO App. Br. 17 (arguing that Paragraph 6 of Dr. Bagherzadeh's declaration (1) is conclusory regarding skilled artisans' addressing timing problems in implementing Amidi's invention, and (2) lacks analysis as to how that would be done).

Dell is said to place information about a requested operating mode or function provided by the computer system in a different (volatile) memory, rather than the non-volatile memory of the SPD device. *Id.* (citing Dell, col. 7, ll. 5–65). Patent Owner reasons that this knowledge would have placed Amidi's limited disclosure of the SPD device in proper context for ordinarily skilled artisans, namely that it would provide the actual configuration during power up. PO App. Br. 12 (citing Supp. Sechen Decl. ¶ 27). *Accord* Tr. 10–11.

But even assuming, without deciding, that the initial SPD data from Dell's non-volatile memory provides actual configuration data during boot-up as Patent Owner contends, Dell at least suggests that this functionality is a *preferred embodiment*—not an absolute requirement. Notably, Dell's "volatile memory 26 can be used to store the new PD data because, when power is removed, it will be *preferred* to effect a start up sequence with the 'original' or initial PD data in the EEPROM 30." Dell, col. 7, ll. 16–19 (emphasis added). Simply put, a preference is not a requirement and, as Requesters indicate, Dell reasonably suggests such a preferred embodiment. '577 TPR Resp. Br. 10 (noting this preferred embodiment)[14]; '546 TPR Resp. Br. 8. Although Dell prefers to preserve the original PD data, Dell nonetheless describes alternative techniques in that regard *while using the*

[14] *Accord* Tr. 22:4–7 (MR. HEAFEY [counsel for the '577 Requester]: "I would agree that Dell would suggest that modified information could be stored in the nonvolatile memory. . . . There are *embodiments* of Dell where *the nonvolatile memory stores data as the BIOS is expecting*.") (emphasis added).

non-volatile memory 30 for the modified PD data, and then re-writing the original PD data back to that memory. Dell, col. 7, ll. 23–28.

Based on these teachings, then, skilled artisans would understand that Dell (1) effects a start-up sequence with the "original" or initial PD data in non-volatile memory as a preferred embodiment, and (2) can store modified PD data in that non-volatile memory—the same memory used to provide the data at start-up. Even assuming, without deciding, that this modified PD data storage can be temporary and used for other purposes as Dr. Sechen declares (Supp. Sechen Decl. ¶¶ 40, 42), Dell nevertheless suggests that the non-volatile memory is used to provide data at start-up and can also store data that is different from actual device memory characteristics for the reasons noted above and those indicated by Requesters. *See* '546 TPR Resp. Br. 8–9; Tr. 22:3–12.

Therefore, to the extent that Dell reflects the state of the art to inform skilled artisans regarding the information that Amidi's SPD can provide, we agree with Requesters at least to the extent that providing data that is different from actual device memory characteristics via Amidi's SPD would have at least been an obvious variation.

Lastly, to the extent that Patent Owner argues that the JEDEC standards do not teach or suggest the disputed attribute limitation (PO App. Br. 17), such arguments do not persuasively rebut the Examiner's principal reliance on Amidi in that regard, and the relatively limited purpose for which the JEDEC standards were cited. *See* RAN 28 (incorporating claim chart of Ex. CC-F of the Comments filed Feb. 13, 2012 by reference); *see also* Claim

Chart CC-F, at 43 (referring to claim 38 in connection with claim 56's attribute limitation), 25–28 (claim 38)).

Therefore, we are not persuaded that the Examiner erred in rejecting claim 56 as obvious over Amidi and the JEDEC standards, as well as claims 38, 48, 57, and 58 not argued separately with particularity.

Because our decision is dispositive regarding patentability of these claims based on these references, we need not reach the merits of the Examiner's alternative obviousness rejection of claims 38 and 56–58 over Amidi and Dell ("Issue 31"). RAN 14, 29, 38. *See In re Gleave*, 560 F.3d 1331, 1338 (Fed. Cir. 2009).

THE CROSS-APPEAL

THE PROPOSED OBVIOUSNESS REJECTION OVER AMIDI AND "JEDEC SPECIFICATIONS" ("ISSUE 34")

The Examiner declines to reject claims 38 and 56–58 as obvious over Amidi and "JEDEC *specifications*" because this proposed rejection is said to have "already been addressed in Issue 29," namely the obviousness rejection over Amidi and "JEDEC *standards*." RAN 15, 30, 39 (emphases added). These standards are said to incorporate all teachings of the JEDEC specifications. RAN 30.

The '546 Requester argues that the proposed rejection of claims 38 and 56–58 over Amidi and JEDEC standards should also be treated as an adoption of the rejection of those claims over Amidi and JEDEC specifications. '546 TPR App. Br. 8. According to the '546 Requester, this

issue should be "preserved" in the event the '577 Requester ceases to participate or the '577 proceeding terminates before the '546 proceeding. *Id.*

Patent Owner argues that not only did the '546 Requester fail to appeal this issue as to claims 56–58, the attempt to "preserve" the issue on appeal is improper and fails to present any reasons for adopting the proposed rejection. PO Resp. Br. 8. Patent Owner adds that the '546 Requester's equating the two rejections is likewise improper, for the two rejections rely on different evidence, namely the Bagherzadeh and Kozyrakis declarations, respectively. PO Resp. Br. 8–10.

ISSUE

Has the Examiner erred in declining to reject claims 38 and 56–58 as obvious over Amidi and JEDEC specifications?

ANALYSIS

We begin by noting, as does Patent Owner (PO Resp. Br. 8–9), that the '546 Requester's Notice of Cross Appeal filed August 2, 2013, on page 2 limits unambiguously the cross-appeal of the Examiner's non-adoption of the obviousness rejection over Amidi and JEDEC specifications ("Issue 34") *solely to claim 38*. The '546 Requester's Cross-Appeal Brief, however, adds claims 56–58 in connection with this issue. *See* '546 TPR App. Br. 8.

But as Patent Owner indicates, this belated inclusion of claims 56–58 in the '546 Requester's cross-appeal brief is beyond the scope of the cross-appeal of Issue 34 that was limited solely to claim 38 in the Notice of Cross Appeal. Because claims 56–58 were not identified in the Notice of Cross

Appeal in connection with this issue—a regulatory requirement[15]—the '546 Requester apparently did not intend to cross-appeal the Examiner's non-adoption of the obviousness rejection of those claims over Amidi and JEDEC specifications. That the '546 Requester's Notice of Appeal specifically identified claims 56–58 in connection with *other* cross-appealed issues (e.g., Issues 21, 22, 27, 37, and 38) tends to suggest that these claims were intended to be omitted from the cross-appeal of the proposed obviousness rejection pertaining to Issue 34. Accordingly, any arguments pertaining to claims 56–58 in connection with the proposed obviousness rejection pertaining to Issue 34 are untimely and, therefore, deemed to be waived.[16]

In any event, we find unavailing the '546 Requester's contention that the Examiner's obviousness rejection of claims 38 and 56–58 over Amidi and "JEDEC *standards*" should also be treated as an adoption of the rejection of those claims over Amidi and "JEDEC *specifications*." '546 TPR App. Br. 8. To be sure, the cited "JEDEC *specifications*" refers to two documents that are a subset of the three documents collectively referred to as "JEDEC *standards*" as noted previously. RAN 6. But as Patent Owner indicates, the two rejections are not the same, for they rely on different evidence, namely the Bagherzadeh and Kozyrakis declarations, respectively. PO Resp. Br. 8–9. Moreover, these rejections are based on different

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[15] *See* 37 C.F.R. § 41.61(c) ("The notice of appeal or cross appeal in the proceeding *must* identify the appealed claim(s) . . . .") (emphasis added).
[16] *Accord Artsana USA, Inc. v. Kolcraft Enter. Inc.*, No. 2013-008706, 2013 WL 6490306, at *4 (PTAB Dec. 6, 2013) (non-precedential) (dismissing the appeal of claims 3 and 4 that were omitted from the Notice of Appeal).

combinations of prior art references (four total cited references versus three total cited references)—a distinction that further establishes that these rejections constitute different grounds of rejection despite citing three identical references. *See In re McDaniel*, 293 F.3d 1379, 1384 (Fed. Cir. 2002) (noting that obviousness rejection that added a prior art reference (Grot) to a combination of other prior art references did not share a common ground of rejection with claims rejected as obvious over those other references).

Therefore, to the extent that the '546 Requester's "preservation" argument is based on the notion that the proposed obviousness rejection over Amidi and "JEDEC *specifications*" is equivalent to the Examiner's rejection over Amidi and "JEDEC *standards*," we disagree.

Therefore, we are not persuaded that the Examiner erred in declining to reject claims 38 and 56–58 over Amidi and "JEDEC specifications."[17]

THE PROPOSED § 112(A) REJECTION ("ISSUE 37")

We also sustain the Examiner's decision declining to adopt the proposed rejection of claims 56–58 under § 112(a) as allegedly overly broad. RAN 15, 31–32, 39. Independent claim 56 was narrowed via Patent

[17] To the extent that the '546 Requester contends that the Examiner's action in this regard is improper procedurally, such a matter is petitionable—not appealable—and, therefore, not before us. *See* Tr. 42:1–8; 45:10–20; *see also In re Watkinson*, 900 F.2d 230, 232-33 (Fed. Cir. 1990) (noting that the Board has no jurisdiction for matters within the Examiner's discretion and not tantamount to a rejection of claims).

Owner's amendment filed December 4, 2012, to add the words "electrically erasable programmable" before the term "read-only non-volatile memory device." *See* PO Resp. Br. 10–11 (noting this amendment). Therefore, claims 56–58 are narrower than they were before that amendment and, as such, the 112(a) overbreadth rejection was not proposed *responsive to that amendment* as the Examiner indicates. RAN 32. Patent Owner's point in this regard is well taken. PO Resp. Br. 11–12 (citing MPEP § 2658(II), 2258(II)).

The '546 Requester's attempt to tie the proposed overbreadth rejection to the alleged limited scope of enablement in paragraphs 18, 22, and 23 of Dr. Sechen's Supplemental Declaration of December 3, 2012 ('546 TPR App. Br. 10) is unavailing. Not only are the particular issues raised by the '546 Requester pertaining to the invention's enabled implementations to address back-to-back read problems unrelated to the amendment language, but the particular cited paragraphs of that declaration pertain to Amidi's perceived shortcomings in connection with the claimed invention as Patent Owner indicates. PO Resp. Br. 11–13. Nevertheless, to the extent that these cited paragraphs of Dr. Sechen's Supplemental Declaration somehow can be considered as directed to the '386 patent as the '546 Requester seems to suggest, the proposed § 112(a) issues are simply not germane to the above-noted narrowing amendment to claim 56, let alone responsive to that amendment as the Examiner and Patent Owner indicate.

Therefore, we are not persuaded that the Examiner erred in declining to reject claims 56–58 as overly broad under § 112(a).

THE PROPOSED § 112(B) REJECTION ("ISSUE 38")

For similar reasons, we also sustain the Examiner's decision declining to reject claims 56–58 under § 112(b) as allegedly not directed to the subject matter that the inventors regard as their invention. RAN 15, 32, 39. Here again, the proposed § 112(b) issues pertaining to the invention's enabled implementations to address back-to-back read problems are unrelated to the amendment language, and the particular cited paragraphs of that declaration pertain to Amidi's perceived shortcomings in connection with the claimed invention as Patent Owner indicates. PO Resp. Br. 11–13. In short, the '546 Requester's proposed 112(b) rejection is simply not germane to the above-noted narrowing amendment to claim 56, let alone responsive to that amendment as the Examiner and Patent Owner indicate. RAN 32; PO Resp. Br. 11–13.

Therefore, we are not persuaded that the Examiner erred in declining to reject claims 56–58 under § 112(b).

CONCLUSION

The Examiner did not err in rejecting claims 38, 48, and 56–58 under § 103 as obvious over Amidi and "JEDEC standards." Nor did the Examiner err in declining to reject (1) claims 38 and 56–58 as obvious over Amidi and "JEDEC specifications" and (2) claims 56–58 under § 112(a) and (b). Accordingly, we affirm those decisions.

We do not reach the Examiner's alternative obviousness rejection of claims 38 and 56–58 over Amidi and Dell.

DECISION

The Examiner's decision rejecting claims 38, 48, and 56–58 is affirmed, as is the Examiner's decision declining to reject those claims on other grounds as noted in the preceding section of this opinion.

Requests for extensions of time in this *inter partes* reexamination proceeding are governed by 37 C.F.R. § 1.956. *See* 37 C.F.R. § 41.79.

In the event neither party files a request for rehearing within the time provided in 37 C.F.R. § 41.79, and this decision becomes final and appealable under 37 C.F.R. § 41.81, a party seeking judicial review must timely serve notice on the Director of the United States Patent and Trademark Office. *See* 37 C.F.R. §§ 90.1 and 1.983.

AFFIRMED

peb

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