3.11.5.8 – GDDR4 Specific SGRAM Functions

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GRAPHICS DOUBLE DATA RATE (GDDR4) SGRAM SPECIFICATION

(From JEDEC Board Ballot JCB-06-007, formulated under the cognizance of the JC42.3 Sub-Committee on DRAM Parametrics.)

Release 1.0, November 2005

SCOPE

This document defines the Graphics Double Data Rate 4 (GDDR4) Synchronous Graphics Random Access Memory (SGRAM) specification, including features, functionality, package, and pin assignments. This scope may be expanded in future to also include other higher density devices.

The purpose of this Specification is to define the minimum set of requirements for JEDEC standard compatible 256 Mb through 1 Gb x32 GDDR4 SGRAM devices. System designs based on the required aspects of this specification will be supported by all GDDR4 SGRAM vendors providing JEDEC standard compatible devices. Some aspects of the GDDR4 standard such as AC timings and capacitance values were not standardized. Features such as Parity and Boundary scan are optional. GDDR4 supports both 4 bank and 8 bank addressing. This specification is written using 8 banks and a full complement of address bits. The addressing table should be consulted for addressing specifics. In all cases, vendor datasheets should be consulted for specifics.

This specification was created based on the DDR specification (JESD79) and some aspects of the GDDR3 specification (JESD21C). Each aspect of the changes for high speed operation were considered and balloted. The accumulation of these ballots were then incorporated to prepare this GDDR4 SGRAM specification, replacing whole sections and incorporating the changes into Functional Description and Operation.

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GDDR4 SGRAM SPECIFICATION

256 Mb = 8M x 32 (2M x 32 x 4 banks); 512 Mb = 16M x 32 (2M x 32 x 8 banks)
1 Gb = 32M x 32 (4M x 32 x 8 banks)

FEATURES

- Double-data rate architecture; two data transfers per clock cycle
- Single ended READ strobe (RDQS) per byte
- Single ended WRITE strobe (WDQS) per byte
- Differential clock inputs (CK and CK#)
- Commands entered on each positive CK edge; data and data mask referenced to both edges of RDQS/WDQS
- 4 or 8 internal banks for concurrent operation
- Data mask (DM) for masking WRITE data
- Burst Length: 8 only
- Multiplexed addressing
- Auto Precharge option for each burst access
- Auto Refresh and Self Refresh Modes
- On-die termination (ODT)
- Calibrated output drive
- Programmable offset for both driver and termination
- POD-15 (or POD-18) compatible inputs
- VDD and VDDQ: 1.5 +/- 0.045 V
- VDD and VDDQ: 1.8 +/- 0.09 V (optional)
- Parity and Boundary Scan (both optional)

FUNCTIONAL DESCRIPTION

The GDDR4 SGRAM is a high speed CMOS, dynamic random-access memory internally configured as either four or eight banks. These devices contain the following number of bits:

256 Mb has 268,435,456 bits and quad-banks
512 Mb has 536,870,912 bits and eight-banks
1 Gb has 1,073,741,824 bits and eight banks

The GDDR4 SGRAM uses a double data rate architecture to achieve high speed operation. The double data rate architecture is essentially an 8n prefetch architecture with an interface designed to transfer two data words per clock cycle over four clock cycles at the I/O pins. A single read or write access for the GDDR4 SGRAM effectively consists of an 8n data transfer every four clock cycles at the internal DRAM core and eight corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

Uni-directional data strobes are transmitted externally, along with data, for use in data capture at the receiver. RDQS is a strobe transmitted by the GDDR4 SGRAM during READs. WDQS is the data strobe sent by the memory controller during WRITEs. RDQS is edge-aligned with data for READs and WDQS is center aligned with data for WRITEs.

The GDDR4 SGRAM operates from a differential clock (CK and CK# the crossing of the CK going high and CK# going low will be referred to as the positive edge of CK). Commands (address and control signals) are registered at the positive edge of CK. Address is received on two consecutive rising edges of CK. Input data is registered at both edges of WDQS, and output data is referenced to both edges of RDQS, as well as to both edges of CK.

Read and write accesses to the GDDR4 SGRAM are burst oriented; accesses start at a selected location and continue for a total of eight locations. The start address is restricted to multiples of 8. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command and the next clock edge are used to select the bank and the row to be accessed. The address bits registered coincident with the READ or WRITE command and the next clock edge are used to select the bank and the starting column location for the burst access.

This specification includes all features and functionality required for JEDEC GDDR4 SGRAM devices. Users benefit from knowing that any system design based on the required aspects of the specification are supported by all GDDR4 SGRAM vendors; conversely users seeking to use any superset specifications bear the responsibility to verify support with individual vendors.

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INITIALIZATION

GDDR4 SGRAMs must be powered up and initialized in a predefined manner as shown in Figure 1. Operational procedures other than those specified may result in undefined operation.

The Mode Register and Extended Mode Registers do not have default values except EMR[A3:A2] and EMR3[A5]. If they are not programmed during initialization, it may lead to unspecified operation.

1	Apply Power to VDD
2	Apply power to VDDQ at same time or after power is applied to VDD
3	Apply VREF at same time or after power is applied to VDDQ
4	After power is stable, provide stable clock signals
5	Assert and hold RESET low
6	Wait a minimum of 200µs
7	Set CKE# and A0 to the desired address & command on die termination settings, then bring RESET High to latch in the logic state of CKE# and A0. t_{ATS} and t_{ATH} must be met during this procedure. See Table 1 for the values and logic states for CKE# and A0
8	Bring CKE# low after t_{ATH} is satisfied
9	Wait at least 200µs referenced from the beginning of t_{ATS}
10	Issue at least 2 NOP commands
11	Issue a PRECHARGE ALL command followed by NOP commands until t_{RP} is satisfied
12	Issue MRS commands to the mode register and the 3 extended mode registers in any order. t_{MRD} must be met during this procedure
13	Issue two AUTO REFRESH commands
14	After t_{RFC} is satisfied from the second AUTO REFRESH command and t_{DL} is satisfied, the device is ready for operation

Figure 1: GDDR4 Initialization Sequence

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Table 1 Address and Control Termination Values

VALUE OHMS	CKE#	A0
60	L	H
120	H	H
240	H	L
RFU	L	L

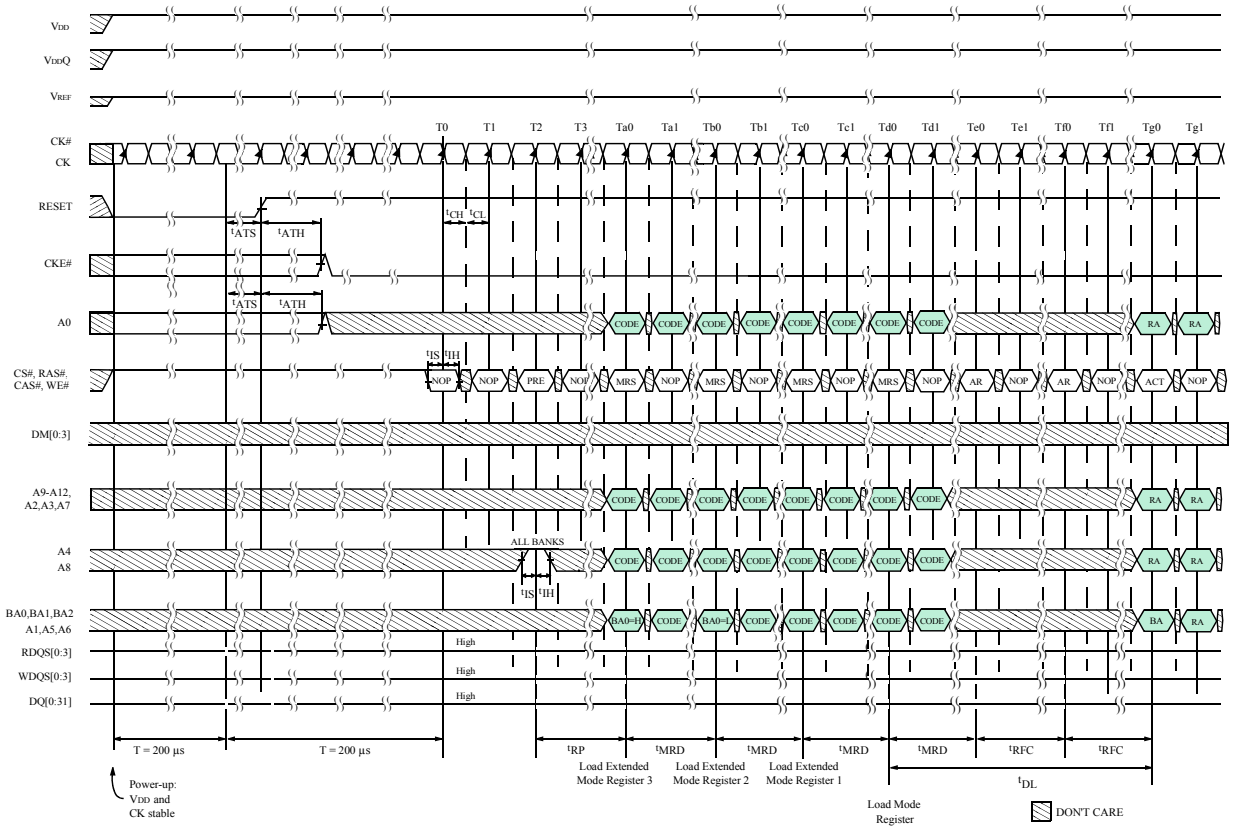

Figure 2: GDDR4 SGRAM Initialization

REGISTER DEFINITION

MODE REGISTER (MR)

The Mode Register is used to define the specific mode of operation of the GDDR4 SGRAM. This includes the definition of Write Latency, Write Recovery, DLL Reset, Test Mode and CAS latency as shown in Figure 3.

The Mode Register is programmed via the MODE REGISTER SET (MRS) command (with BA0=0, BA1=0 and BA2=0) and will retain the stored information until it is reprogrammed or the device loses power (except bit A8, which is self-clearing).

Reprogramming the mode register will not alter the contents of the memory. The Mode Register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time t_{MRD} before initiating any subsequent operation. Violating either of these requirements will result in unspecified operation. Reserved states should not be used, as unknown operation or incompatibility with future versions may result. RFU bits are reserved for future use and must be programmed to 0.

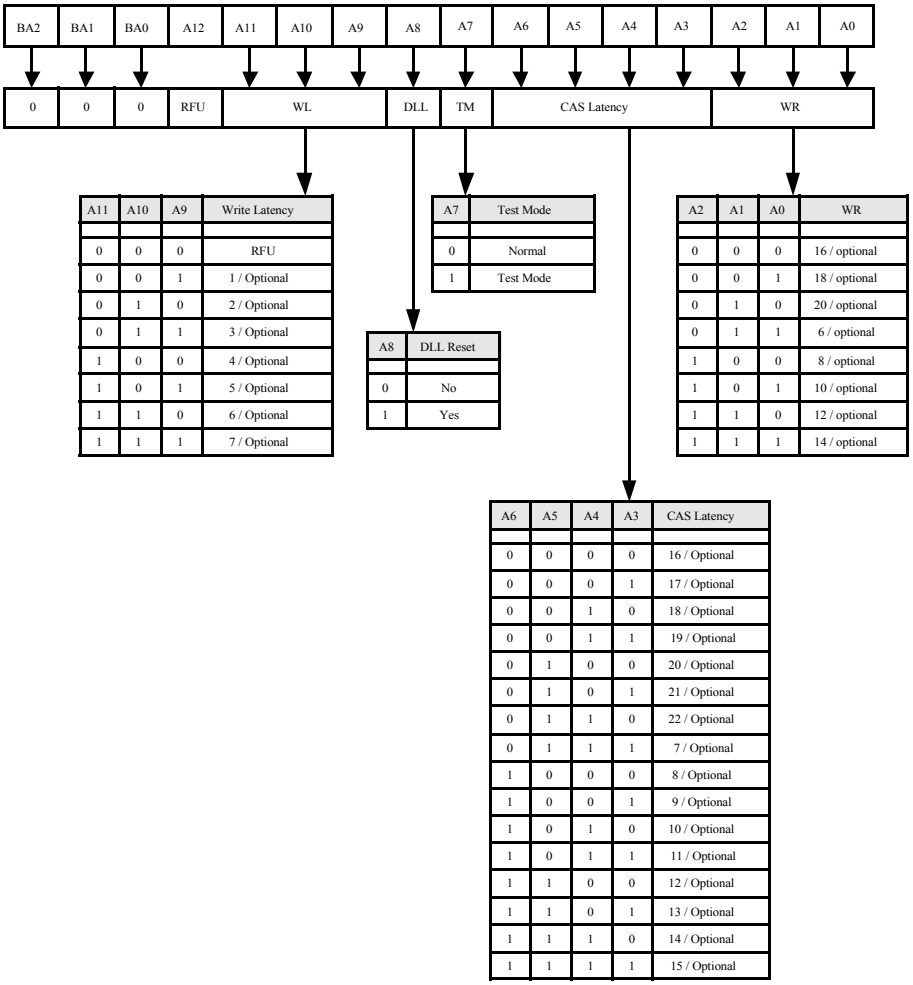

Figure 3: Mode Register Definition

Burst Length

Read and write accesses to the GDDR4 SGRAM are burst-oriented, with the burst length fixed at 8 and thus not programmable in the MRS as with many other DRAMs. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block. The block is uniquely selected by A3–Ai (where Ai is the most significant column address bit for a given configuration) as the GDDR4 SGRAM has a fixed burst length of 8. Also GDDR4 SGRAM has a fixed start address of 000 within the block, thus A2-A0 does not select the access order within a burst and must be set to zero.

Table 2 Burst Order

Burst Length	Starting Column Address	Order of Access within a burst
		Type = Sequential
8	A2 A1 A0	
	0 0 0	0 - 1 - 2 - 3 - 4 - 5 - 6 - 7

CAS Latency

The READ latency, or CAS latency, is the delay between the registration of a READ command and the availability of the first piece of output data. The latency is set using bits A3-A6 and values of 7-22 are supported in the specification. Vendor specifications should be checked for value(s) of CAS latency supported.

If a READ command is registered at clock edge n, and the latency is *m* clocks, the data will be available nominally coincident with clock edge *n* + *m*.

WRITE Latency

The WRITE latency (WL) is the delay, in clock cycles, between the registration of a WRITE command and the availability of the first bit of input data. The latency can be set from 1 to 7 clocks depending on the operating frequency and desired current draw. When the write latencies are set to small values (i.e. 1,2,... clocks), the input receivers never turn off, in turn, raising the operating power. When the WRITE latency is set to higher values (i.e. ... 6, 7 clocks) the input receivers turn on when the WRITE command is registered. Refer to vendor datasheets for value(s) of WL supported and the specific value(s) of WL where the input receivers are always on or only turn on when the WRITE command is registered.

If a WRITE command is registered at clock edge *n*, and the latency is *m* clocks, the data will be registered nominally coincident with clock edge *n* + *m*.

WRITE Recovery (WR)

WR must be programmed into bits A0-A2 with a value greater than or equal to RU{tWR/tCK}, where RU stands for round up, tWR is the analog value from the vendor datasheet and tCK is the operating clock cycle time. The WR register bits are not a required function and may be implemented at the discretion of the memory manufacturer.

Test Mode

The normal operating mode is selected by issuing a MODE REGISTER SET command with bit A7 set to zero, and bits A0–A6 and A8–A12 set to the desired values. Test Mode is initiated by issuing a MODE REGISTER SET command with bit A7 set to one, and bits A0–A7 and A9–A12 set to the desired values. Test mode functions are specific to each DRAM vendor and their exact function are hidden from the user.

DLL Reset

The normal operating mode is selected by issuing a MODE REGISTER SET command with bit A8 set to zero, and bits A0-A7 and A9-A12 set to the desired values. A DLL reset is initiated by issuing a MODE REGISTER SET command with bit A8 set to one, and bits A0-A7 and A9-A12 set to the desired values. When a DLL Reset is complete the GDDR4 SGRAM Reset bit, A8 of the mode register is self clearing (i.e. automatically set to a zero by the GDDR4 SGRAM).

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EXTENDED MODE REGISTER (EMR)

The Extended Mode Register controls functions beyond those controlled by the Mode Register; these additional functions include output drive strength selection, control of DBI, preamble selection and Vendor ID as shown in Figure 4.

The Extended Mode Register is programmed via the MODE REGISTER SET (MRS) command (with BA0=1, BA1=0 and BA2=0) and will retain the stored information until it is reprogrammed or the device loses power. The Extended Mode Register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time t_{MRD} before initiating any subsequent operation. Violating either of these requirements will result in unspecified operation.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result. RFU bits are reserved for future use and must be programmed to 0.

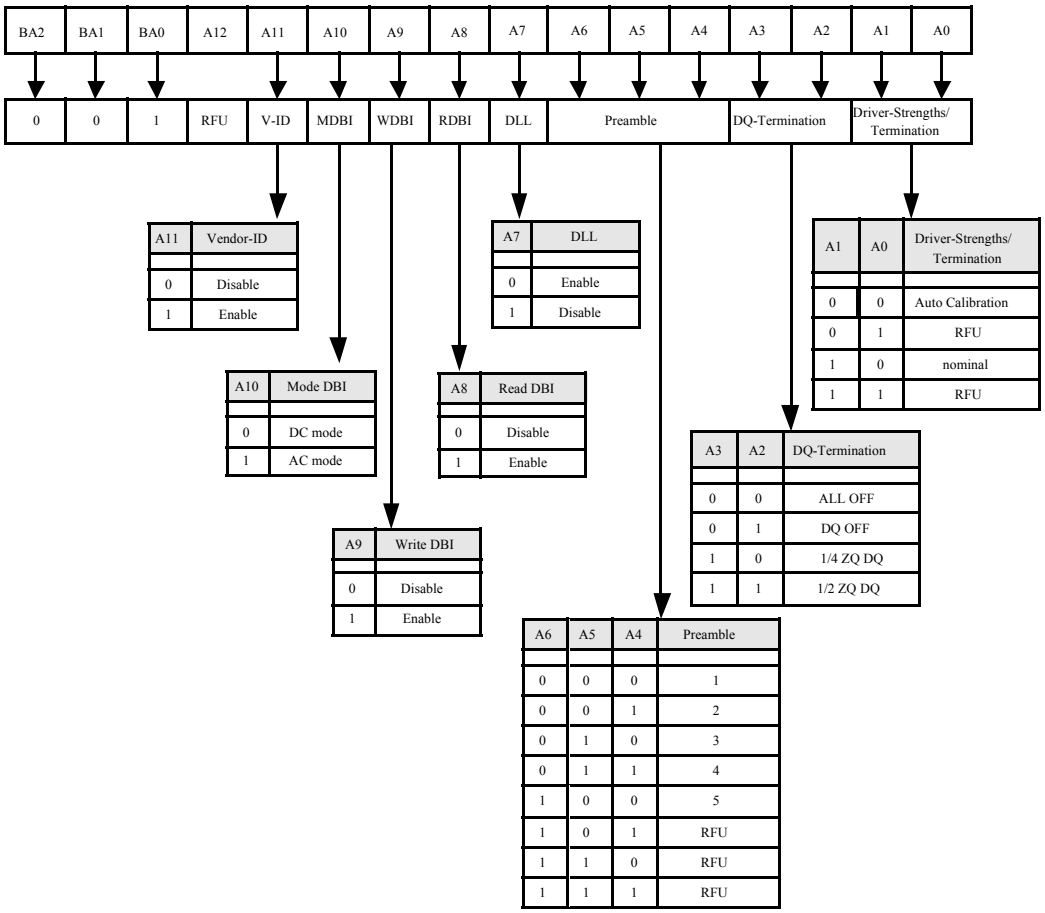

Figure 4: Extended Mode Register Definition

DRIVER Strengths/Termination

The Data Driver Impedance, DZ, is used to determine the value of the data drivers impedance. The Auto Calibration option enables the Auto-Calibration functionality of the DRAM which controls the Pulldown-, Pullup-Driver Strength and the Termination over process, temperature and voltage changes. The nominal option enables the factory setting for the Pulldown, Pullup-Driver-Strength and for the Termination. The design target for the factory setting is 40Ohm Pulldown, 60Ohm Pullup-Driver-Strength and 60/120Ohm for DQ-Termination, 60/120/240Ohm for CMD/ADD-Termination with nominal process, voltage and temperature conditions. With the nominal option enabled, Driver-Strength and Termination is expected to change with process, voltage and temperature variations. AC timings are only guaranteed with Auto Calibration.

DQ Termination

DQ Termination is used in combination with Driver Strengths/Termination setting to define the value for the on-die termination for the DQ, DM, and WDQS pins.

GDDR4 SGRAM's DQ Termination supports values of 1/4 ZQ or 1/2 ZQ intended for a single- or dual-loaded system. DQ Termination is set with bits A2 and A3 during an MRS command to EMR. The ZQ value is controlled by the EMR Driver Strengths/Termination setting.

The DQ Termination setting is also used to turn off the on-die termination on a GDDR4 SGRAM. If A3 & A2 is set 00, all DQ, DM, WDQS and Command/Address terminators on the device are disabled. If A3 & A2 is set 01 all DQ, DM, WDQS Terminations are switched off but Command/Address terminators are still enabled. GDDR4 adds a mode where only the DQS termination is on (see EMR3 LPTERM). The LPTERM mode is only valid if A3 & A2 is set to either 10 or 11.

To assure that address/command termination is enabled during initialization, the GDDR4 SGRAM automatically sets EMR bits A3 & A2 and EMR3 bit A5 to a default setting during the 200 us window after power/clock stabilization. The default setting for EMR[A3:A2] is either 01, 10 or 11, and for EMR3[A5] is 0.

Preamble

The READ and WRITE preamble in GDDR4 SGRAMs is programmable using bits A4 - A6. Values of 1-5 t_{CK} are specified. Additional cycles of preamble may be required to attain the desired frequency. It is recommended that Controller manufacturers support all values. Manufacturer datasheets should be consulted as the maximum number of preamble cycles over clock frequency which is supported by the GDDR4 SGRAM for Read commands is vendor specific and will be defined by each vendor's specification.

DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power-up initialization and upon returning to normal operation after disabling the DLL for debugging or evaluation as well as low power operation. (When the device exits self refresh mode in normal operation, the DLL is enabled automatically.) Any time the DLL is enabled, t_{DL} must be met before a READ command can be issued.

DBI

Data Bus Inversion (DBI) for READ and WRITE is selected independently using bit A8 for read and bit A9 for write. The mode of DBI is selected using bit A10. For more details on DBI see DBI in the Operation section.

Vendor ID

Vendor ID is used to identify the manufacture of the GDDR4 SGRAM. For more details on Vendor ID see Section entitled VENDOR ID, PARITY & SCAN for more details.

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EXTENDED MODE REGISTER 2 (EMR2)

The Extended Mode Register 2 controls functions beyond those controlled by the Mode Register and Extended Mode Register; these additional functions include the offset for both the driver and termination and t_{RAS} as shown in Figure 5.

The Extended Mode Register 2 is programmed via the MODE REGISTER SET (MRS) command (with BA0=0, BA0=1 and BA2=0) and will retain the stored information until it is reprogrammed or the device loses power. The Extended Mode Register 2 must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time t_{MRD} before initiating any subsequent operation. Violating either of these requirements will result in unspecified operation.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result. RFU bits are reserved for future use and must be programmed to 0.

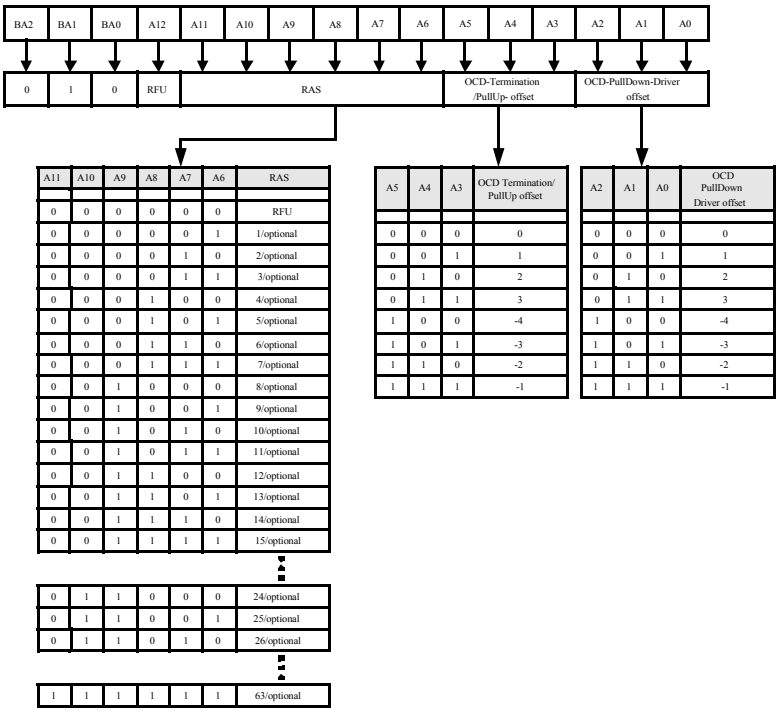

Figure 5: Extended Mode Register 2 Definition

RAS

RAS must be programmed into bits A6-A11 with a value greater than or equal to RU{tRAS/tCK}, where RU stands for round up, tRAS is the analog value from the vendor datasheet and tCK is the operating clock cycle time.

If the DRAM vendor does not support the Mode Register definition of tRAS in clock cylces, the Mode Register settings will be ignored. In that case, the valid analog tRAS timing is given with the DRAM vendor datasheet. If the DRAM vendor supports the clock cycle definition of tRAS, it is mandatory to support all optional clock cycles.

OCD PullDown Driver and Termination PullUp Driver offset

GDDR4 SGRAM adds the ability to add or subtract offsets from both the Driver and Terminator. See section entitled DRIVER & TERMINATION for more details.

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EXTENDED MODE REGISTER 3 (EMR)

The Extended Mode Register 3 controls functions beyond those controlled by the Mode Register, Extended Mode Register and Extended Mode Register 2; these additional functions include LPTERM and Parity as shown in Figure 6.

The Extended Mode Register 3 is programmed via the MODE REGISTER SET (MRS) command (with BA0=1, BA1=1 and BA2=0) and will retain the stored information until it is reprogrammed or the device loses power. The Extended Mode Register 3 must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time t_{MRD} before initiating any subsequent operation. Violating either of these requirements will result in unspecified operation.

If the user activates bits in the Extended Mode Register 3 in an optional field, either the optional field is activated (if option is implemented in the device) or no action is taken by the device (if option is not implemented). Reserved states should not be used, as unknown operation or incompatibility with future versions may result. RFU bits are reserved for future use and must be programmed to 0.

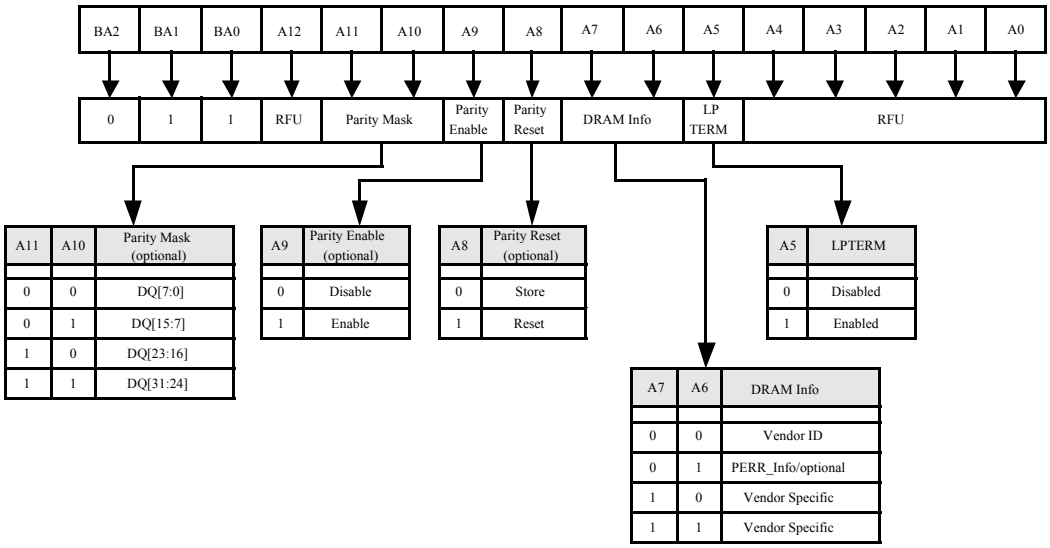

Figure 6: Extended Mode Register 3 Definition

LPTERM

GDDR4 SGRAM adds a low power mode which reduces power consumed for I/O termination by disabling the termination for a subset of the pins. See Section entitled DRIVER & TERMINATION for more details.

DRAM Info

DRAM info is used to select either Parity info or Vendor ID info to be output.

Parity

Parity is an optional feature of GDDR4 SGRAMs. Parity is enabled using bit A9. Parity is stored and reset using bit A8. A mask which selects which bits to monitor can be used by selecting bits A10 - A11. Parity Mask, Parity Enable and Partiy Reset are optional features. If the Parity feature is implemented all Parity Mode Register Bits must be supported. See the Section entitled VENDOR ID, PARITY & SCAN for more details.

COMMAND & ADDRESS

Addressing

GDDR4 SGRAMs use a multiplexed address scheme to reduce pins required on the GDDR4 SGRAM as shown in Table 3. The addresses should be provided to the GDDR4 SGRAM in two parts that are latched into the memory with two consecutive clock edges. Command protocols incorporating signals such as CS#, RAS#, CAS# and WE# should be issued at the first rising edge of the clock and half of the addresses will be registered along with command inputs. Following this cycle, the remaining half of the addresses will be registered at the next rising edge of the clock.

Table 3 Address Pairs

Clock								
First	BA2	BA1	BA0	A12	A11	A10	A9	A8
Second	A6	A5	A1	A2	A3	A0	A7	A4

The commands such as ACTIVE, READ, READ with autoprecharge, WRITE, WRITE with autoprecharge, Precharge, Precharge all, MODE REGISTER SET, Auto-refresh and Self-refresh require two consecutive clocks to fulfill a single task. Only NOP command can be registered at single clock cycle. The clock reference for the AC timing is defined as the first rising edge of the clock.

It is prohibited to issue any other command at the second clock cycle which has been reserved for the second half of the addresses for the preceding command.

GDDR4 addressing includes support for 8Mx32, 16Mx32 and 32Mx32 GDDR4 SGRAM. For both the 32Mx32 and the 16Mx32, two addressing options are allowed (2KB or 4KB page size). 8Mx32 GDDR4 SGRAMs are quad-bank and 16Mx32 and 32Mx32 GDDR4 SGRAMs are eight-bank devices.

Table 4 Addressing Scheme

	8Mx32	16Mx32		32Mx32	
Row address	A0~A11	A0~A10	A0~A11	A0~A11	A0~A12
Column address	A0~A7,A9	A0~A7,A9,A10	A0~A7,A9	A0~A7,A9,A10	A0~A7,A9
Bank address	BA0~BA1	BA0~BA2	BA0~BA2	BA0~BA2	BA0~BA2
Autoprecharge	A8	A8	A8	A8	A8
Refresh	4K/32ms	4K/32ms	8K/32ms	8K/32ms	16K/32ms
Refresh period	7.8us	7.8us	3.9us	3.9us	1.9us

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Commands

Table 5 Truth Table - Commands

NAME (FUNCTION)	CKE#		CS#	RAS#	CAS#	WE#	ADDR	NOTES
	Previous cycle	Current cycle						
DESELECT (NOP)	L	X	H	X	X	X	X	1, 7, 9
NO OPERATION (NOP)	L	X	L	H	H	H	X	1, 7
ACTIVE (Select bank & activate row)	L	L	L	L	H	H	Bank/Row	1, 3, 10
READ (Select bank and column, & start READ burst)	L	L	L	H	L	H	Bank/Col	1, 4, 10
WRITE (Select bank and column, & start WRITE burst)	L	L	L	H	L	L	Bank/Col	1, 4, 10
PRECHARGE (Deactivate row in bank or banks)	L	L	L	L	H	L	Code	1, 4, 5, 10
AUTO REFRESH	L	L	L	L	L	H	X	1, 6
SELF REFRESH ENTRY	L	H	L	L	L	H	X	1, 6
SELF REFRESH EXIT	H	L	H	X	X	X	X	1, 6
			L	H	H	H	X	1, 6
POWER DOWN ENTRY	L	H	H	X	X	X	X	1
			L	H	H	H	X	1
POWER DOWN EXIT	H	L	H	X	X	X	X	1
			L	H	H	H	X	1
MODE REGISTER SET	L	L	L	L	L	L	Op-Code	1, 2, 10
DATA TERMINATOR DISABLE	L	L	H	H	L	H	X	1, 8

Notes:
1) H = Logic High Level; L = Logic Low Level; X = Don't care.
2) BA0–BA2 select either the mode register or the extended mode register (BA0 = 0, BA1 = 0, BA2=0 select the mode register; BA0 = 1, BA1 = 0, BA2 = 0 select extended mode register; BA0 = 0, BA1 = 1, BA2 = 0 select extended mode register 2; BA0 = 1, BA1 = 0, BA2 = 0 select extended mode register 3; other combinations of BA0–BA2 are reserved). A0–A12 provide the op-code to be written to the selected mode register.
3) BA0–BA2 provide bank address and A0–A11 provide row address.
4) BA0–BA2 provide bank address; A0–A7 and A9-A12 provide column address; A8 HIGH enables the auto precharge feature (nonpersistent), and A8 LOW disables the auto precharge feature.
5) A8 LOW: BA0–BA2 determine which bank is precharged.
A8 HIGH: all banks are precharged and BA0–BA2 are "Don't Care."
6) Internal refresh counter controls row addressing; all inputs and I/Os are "Don't Care" except for CKE#.
7) DESELECT and NOP are functionally interchangeable.
8) Used for bus snooping when the DQ termination is set to ZQ/2 in the EMRS and cannot be used during power-down or self refresh.
9) The decode of the DESELECT command excludes the DATA TERMINATOR DISABLE command.
10) Address is received on two consecutive rising edges of CK

Table 6 Truth Table - DM Operations

FUNCTION	DM	DQ	NOTES
Write Enable	L	Valid	1
Write Inhibit	H	X	1

Notes:
1) Used to mask write data, provided coincident with the corresponding data.

OPERATION

Deselect (NOP)

The DESELECT function (CS# HIGH) prevents new commands from being executed by the GDDR4 SGRAM. The GDDR4 SGRAM is effectively deselected. Operations already in progress are not affected.

No Operation (NOP)

The NO OPERATION (NOP) command is used to instruct the selected GDDR4 SGRAM to perform a NOP (CS# LOW). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

MODE REGISTER SET

The mode registers are loaded via inputs A0–A12. See mode register descriptions in the Register Definition section. The MODE REGISTER SET command can only be issued when all banks are idle, and a subsequent executable command cannot be issued until t_{MRD} is met.

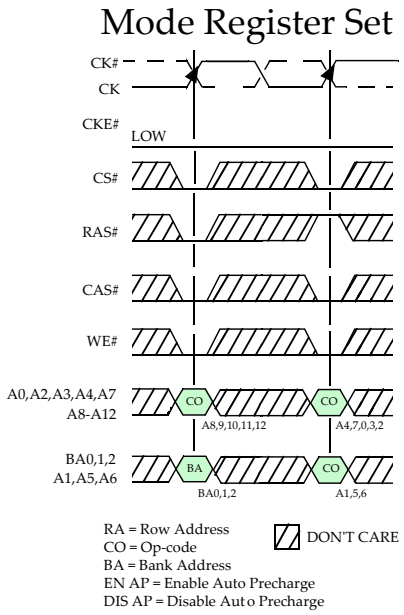

Figure 7: MRS Command

Activation

Before any READ or WRITE commands can be issued to a bank in the GDDR4 SGRAM, a row in that bank must be "opened". This is accomplished by the ACTIVE command (see Figure 8): BA0 -BA2 select the bank, and the address inputs select the row to be activated. Once a row is open, a READ or WRITE command could be issued to that row, subject to the t_{RCD} specification.

A subsequent ACTIVE command to another row in the same bank can only be issued after the previous row has been closed. The minimum time interval between two successive ACTIVE commands on the same bank is defined by t_{RC}.

A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between two successive ACTIVE commands on different banks is defined by t_{RRD}. Figure 9 shows the t_{RCD} and t_{RRD} definition.

The row remains active until a PRECHARGE command (or READ or WRITE command with Auto Precharge) is issued to the bank.

A PRECHARGE command (or READ or WRITE command with Auto Precharge) must be issued before opening a different row in the same bank.

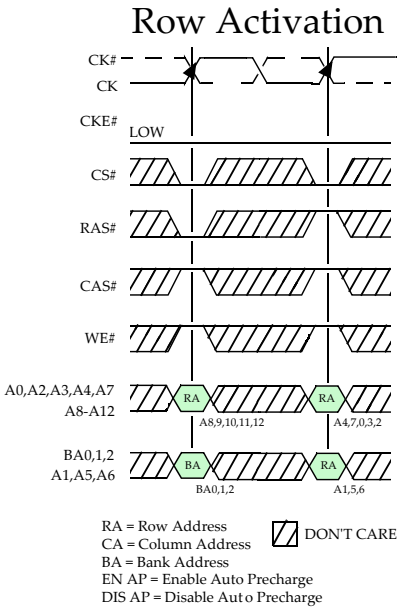

Figure 8: ACTIVE command

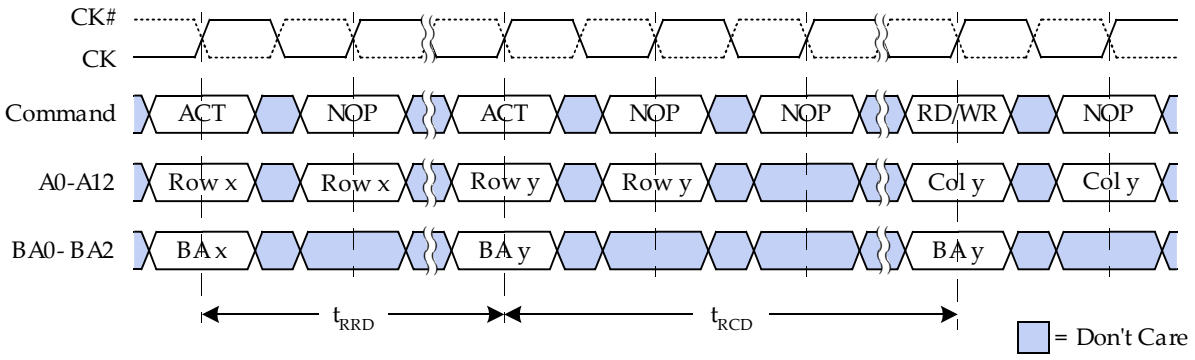

Figure 9: Bank Activation Command Cycle

Data Terminator Disable

Bus snooping for READ commands other than CS# is used to control the on-die termination in the dual load configuration. See Section DRIVER & TERMINATION for more details on GDDR4 SGRAM Termination.

Bank Restrictions

For eight bank GDDR4 devices, there may be a need to limit the number of activates in a rolling window to ensure that the instantaneous current supplying capability of the devices is not exceeded. To reflect the true capability of the DRAM instantaneous current supply, the parameter t_{FAW} (four activate window) is defined. No more than 4 banks may be activated in a rolling t_{FAW} window. Converting to clocks is done by dividing t_{FAW} (ns) by t_{CK} (ns) and rounding up to next integer value. As an example of the rolling window, if (t_{FAW}/t_{CK}) rounds up to 10 clocks, and an activate command is issued in clock N, no more than three further activate commands may be issued in clocks N+1 through N+9.

It is also acceptable and preferable that GDDR4 SGRAMs have no restrictions on the number of banks activated.

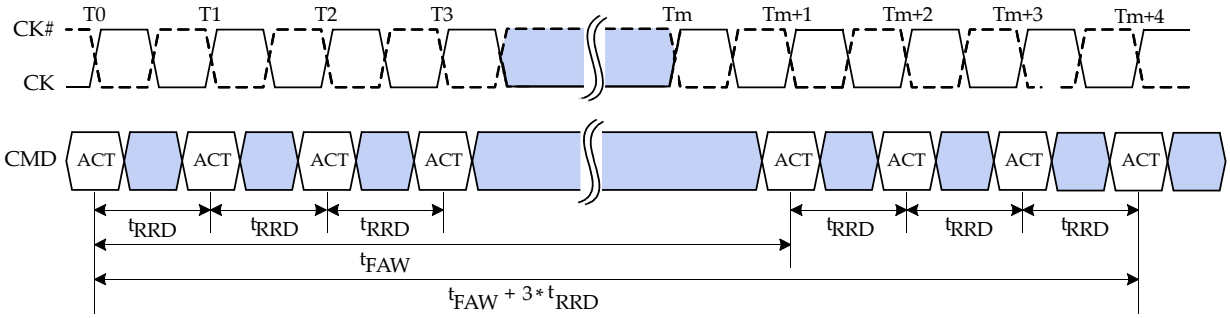

Figure 10: tFAW

READ

READ burst is initiated with a READ command. as shown in Figure 11. The starting column and bank addresses are provided with the READ command and the following clock cycle, and auto precharge is either enabled or disabled for that access with the A8 pin. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst after t_{RAS} min has been met or after the number of clock cycles programmed in EMR2 for RAS depending on the implementation choice per DRAM vendor.

During READ bursts, the first valid data-out element from the starting column address will be available following the CAS latency after the READ command. Each subsequent data-out appears on the DQ pin in phase with the RDQS signal in a source synchronous manner. The GDDR4 SGRAM drives the output data edge aligned to RDQS. And all outputs, i.e. DQs and RDQS, are also edge aligned to the clock. Prior to the first valid RDQS rising edge, a cycle is driven and specified as the READ preamble. The single preamble consists of a half cycle High followed by a half cycle of Low driven by the GDDR4 SGRAM. For the multi-cycle preamble it should be set in extended mode register. The cycle on RDQS consisting of a half cycle Low coincident with the last data-out element followed by a half cycle High is known as the read postamble, and it will be driven by the SGRAM. The SGRAM toggles RDQS only when it is driving valid data on the bus. Upon completion of a burst, assuming no other command has been initiated; the DQs and RDQS will be in a Hi-Z state.

Data from any READ burst may be concatenated with data from a subsequent READ command. A continuous flow of data can be maintained. The first data element from the new burst follows the last element of a completed burst. The new READ command should be issued at least 4 cycles after the first READ command. A PRECHARGE can also be issued to the SGRAM with the same timing restriction as the new READ command if t_{RAS} is met. A WRITE can be issued any time after a READ command as long as the bus turn around time is met. READ data cannot be truncated.

The data inversion flag is driven on the DM signal to identify whether the data is true or inverted data. If DM is HIGH, the data is inverted, and if LOW not inverted. READ Data Inversion can be programmed as a Disable (A8=0) or Enable (A8=1) in the EMRS.

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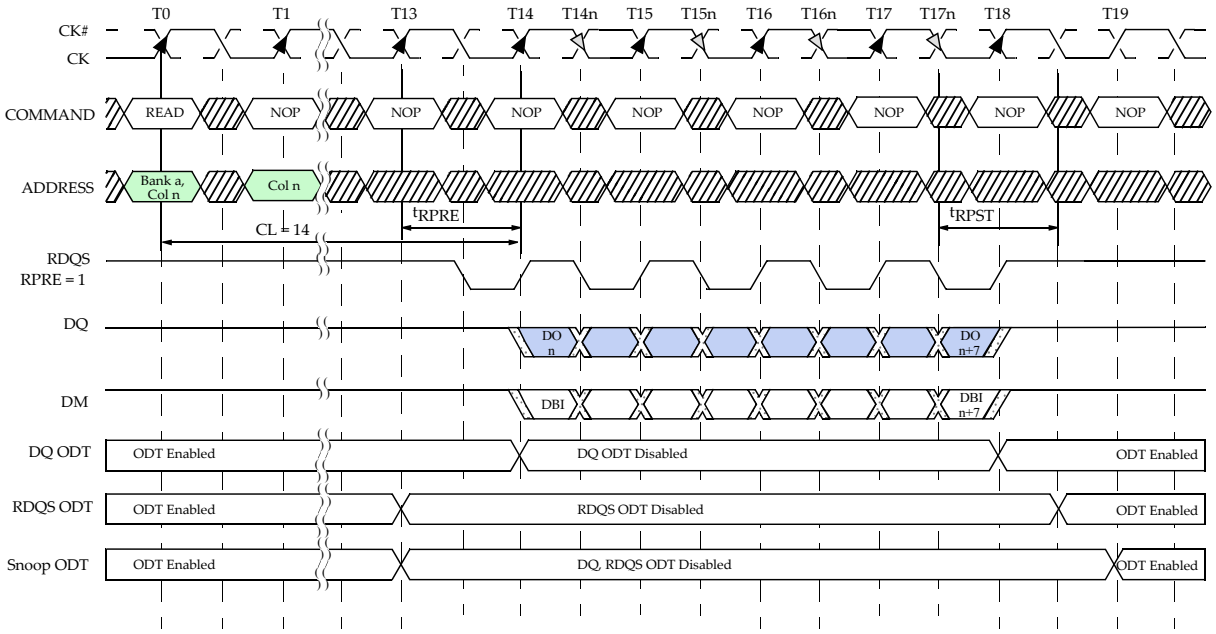
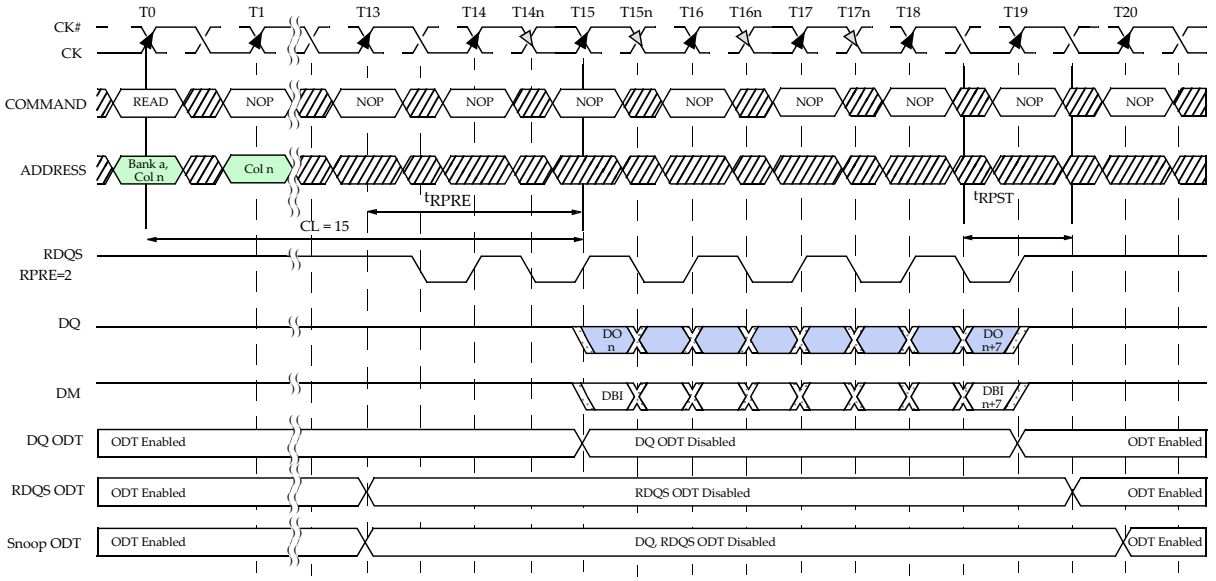
Figure 11: READ Command





Note: RPRE=2 case is shown for an example. Actual supported RPRE numbers will be found in EMRS standard.

Figure 12: Byte Lane READ Timing

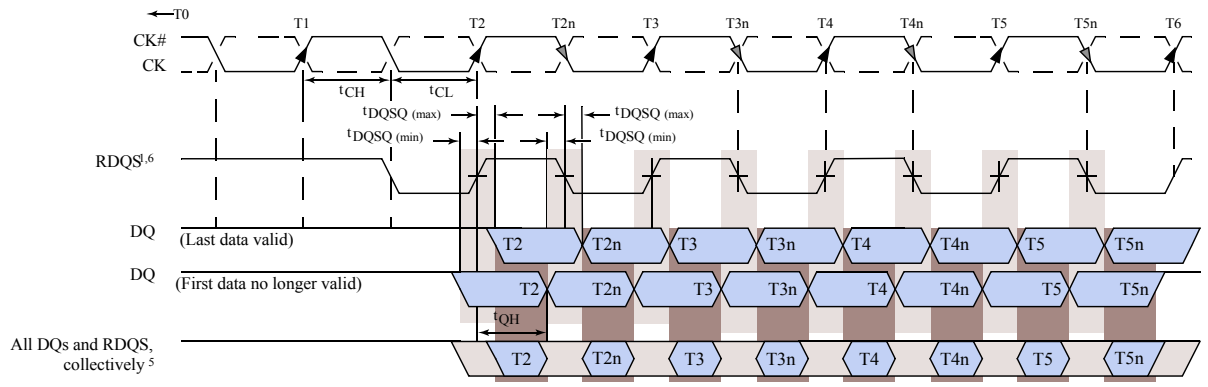


Figure 13: Byte Lane to CK/CK#

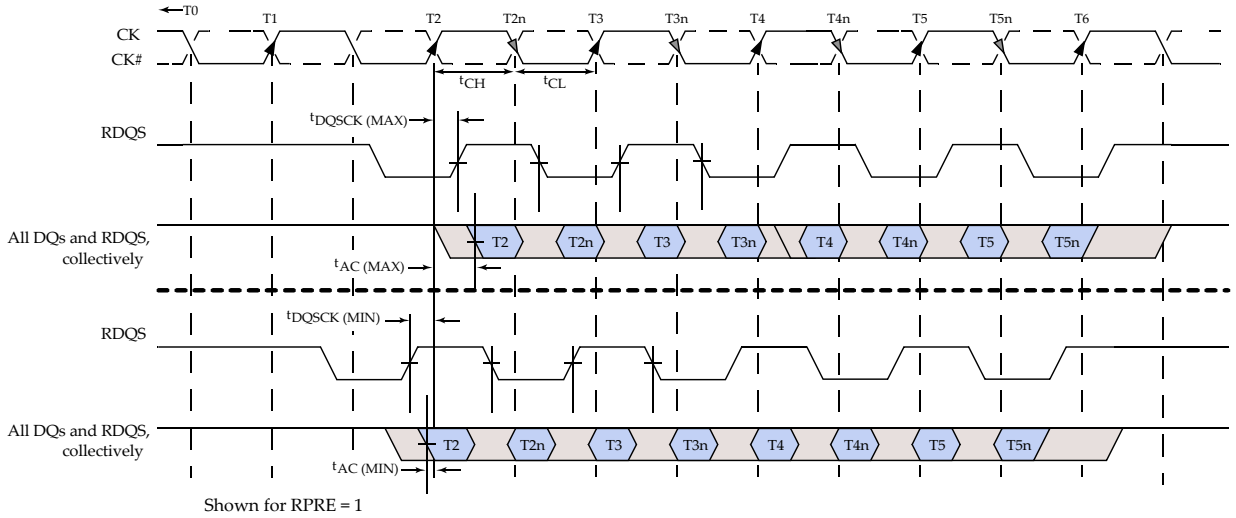
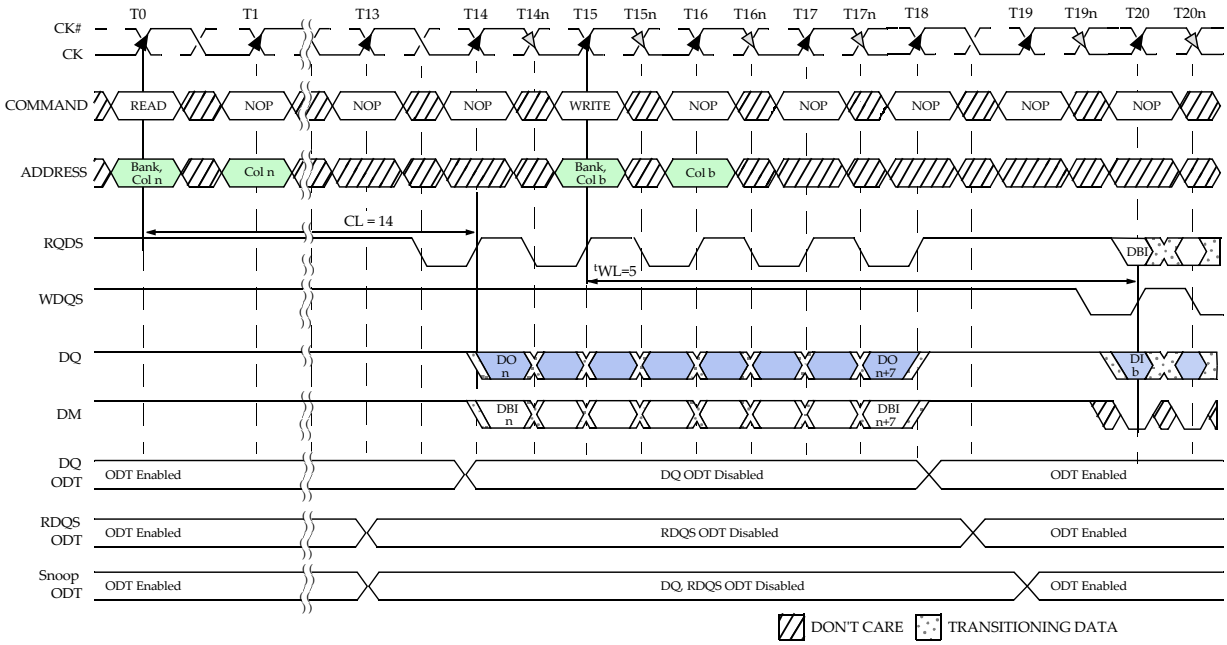


Figure 14: READ to WRITE



Notes:
1. DO *n* = data-out from column *n*.
2. DI *b* = data-in from column *b*.
3. Seven subsequent elements of data-out appear in the programmed order following DO *n*.
4. Data-in elements are applied following DI *b* in the programmed order.
5. Shown with nominal t_{AC}, and t_{DQSQ}.
6. t_{DQSS} in nominal case. RDQS will start driving HIGH one half-clock cycle prior to the first falling edge of RDQS.

READ and DLL Off Mode

The GDDR4 uses a DLL to synchronize the byte lane to the clock. Although the DLL provides accurate clocking of data out, it requires a minimum operating frequency to function properly. The EXTENDED MODE REGISTER provides an avenue to turn the DLL off for running at lower frequencies.

The GDDR4 devices default into the DLL off mode upon power-up. The device enters the DLL on mode of operation if and when the DLL is enabled, via a MODE REGISTER SET Command to the Extended Mode Register. Once in the DLL on mode, the device remains in that mode until powered down or turned off via the EXTENDED MODE REGISTER.

With the DLL off mode the output, DQ and DQS transitions may or may not align with CK and CK# transitions, depending on clock frequency and CAS Latency settings.

The burst READ operation is a bit different from the standard DLL on mode. The time frame from the READ command to first data out is defined by the CAS latency minus one plus $t_{AC\ (DLL\ Off)}$. Data moves from the DRAM cell to the sense amp and is held in a buffer waiting for the appropriate clock cycle. The data will fire from the buffer $t_{AC(DLL\ off)}$ after the clock edge prior to the programmed CAS latency.

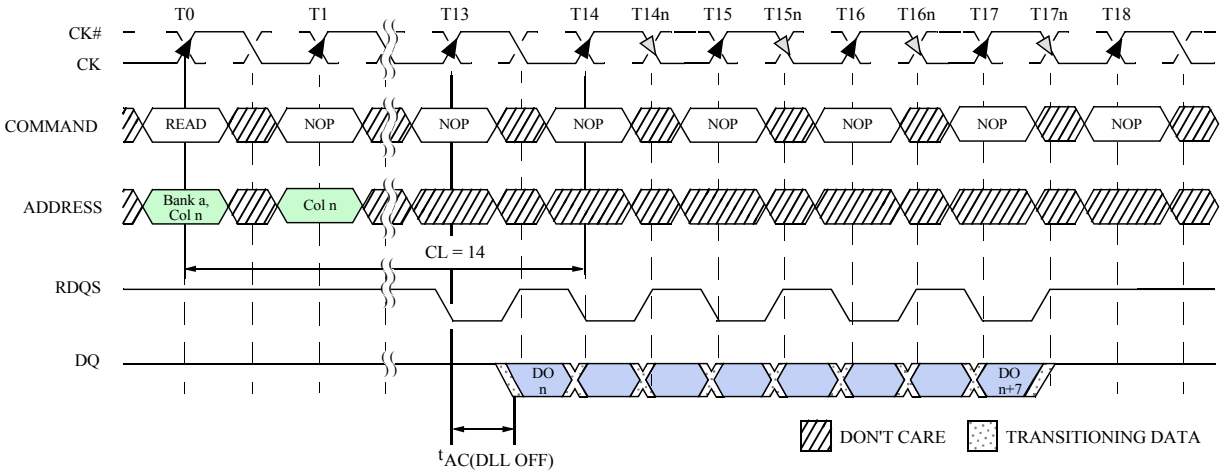


Figure 15: DLL Off Timing

WRITE

WRITE bursts are initiated with a WRITE command (see Figure 16). The starting column and bank addresses are provided with the WRITE command and the following clock cycle, and auto precharge is either enabled or disabled for that access with the A8 pin. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst or after t_{RAS} min is met or after the number of clock cycles programmed in EMR2 for RAS depending on the implementation choice per DRAM vendor.

During WRITE bursts, the first valid data-in element will be registered on the rising edge of WDQS following the write latency and subsequent data elements will be registered on successive edges of WDQS. Prior to the first valid WDQS edge a cycle or cycles is/are needed and specified as the WRITE Preamble. The cycle on WDQS following the last data-in element is known as the write postamble and must be driven high by the controller it can not be left to float high using the on die termination.

A valid strobe edge is defined as a strobe edge associated with data. The time between the WRITE command and the first valid edge of WDQS (t_{DQSS}) is specified relative to the write latency and the number of write preamble (WL - #preamble - 0.25CK and WL - #preamble + 0.25CK), where WPRE is the number of write preamble set in the extended mode register. All of the WRITE diagrams show the nominal case, and where the two extreme cases (i.e., t_{DQSS} [MIN] and t_{DQSS} [MAX]) might not be intuitive, they have also been included. Upon completion of a burst, assuming no other commands have been initiated, the DQs will remain High and any additional input data will be ignored. Data for any WRITE burst may not be truncated with a subsequent WRITE command. The new WRITE command can be issued on any positive edge of clock following the previous WRITE command assuming the previous burst has been completed. The new WRITE command should be issued at least 4 cycles after the first WRITE command. Data for any WRITE burst cannot be truncated by a subsequent PRECHARGE command. After the PRECHARGE command, a subsequent command to the same bank cannot be issued until t_{RP} is met.

The data inversion flag receives the RDQS signal to identify whether to store the true or inverted data. If RDQS is HIGH, the data will be stored after inversion inside the GDDR4 SGRAM and not inverted when it recognizes RDQS as LOW. WRITE Data Inversion can be programmed as an Disable(A9=0) or Enable (A9=1) in the EMRS.

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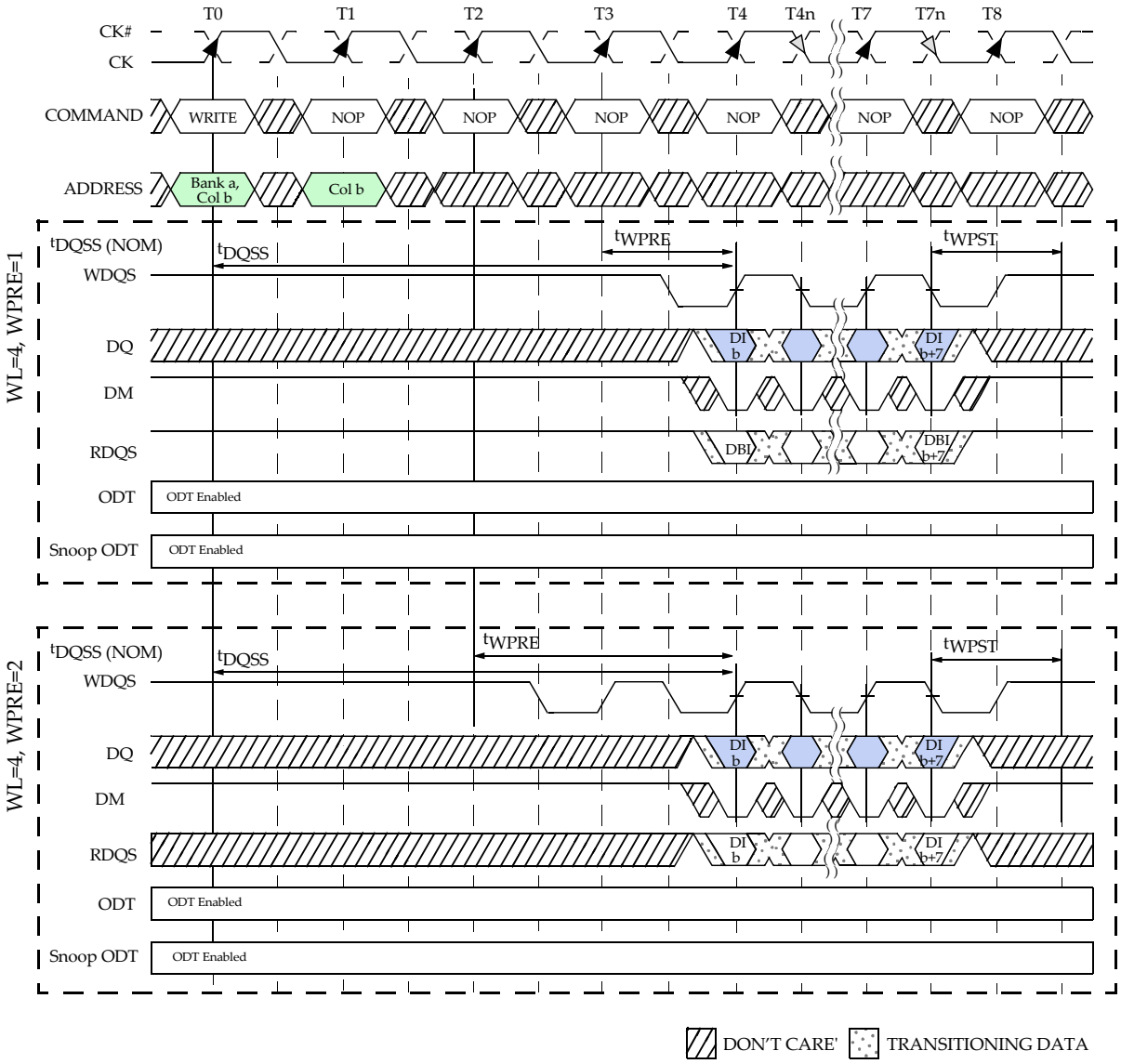
Figure 16: WRITE Command



Note: WPRE=2 case is shown as an example. Actual supported WPRE values are found in the EMR.

Figure 17: WRITE Capture

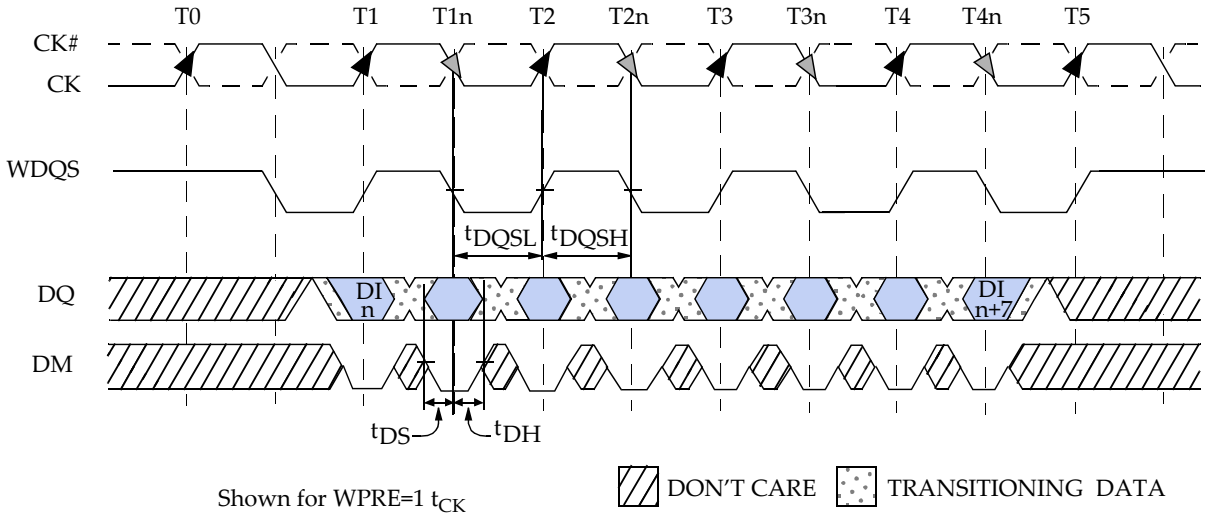
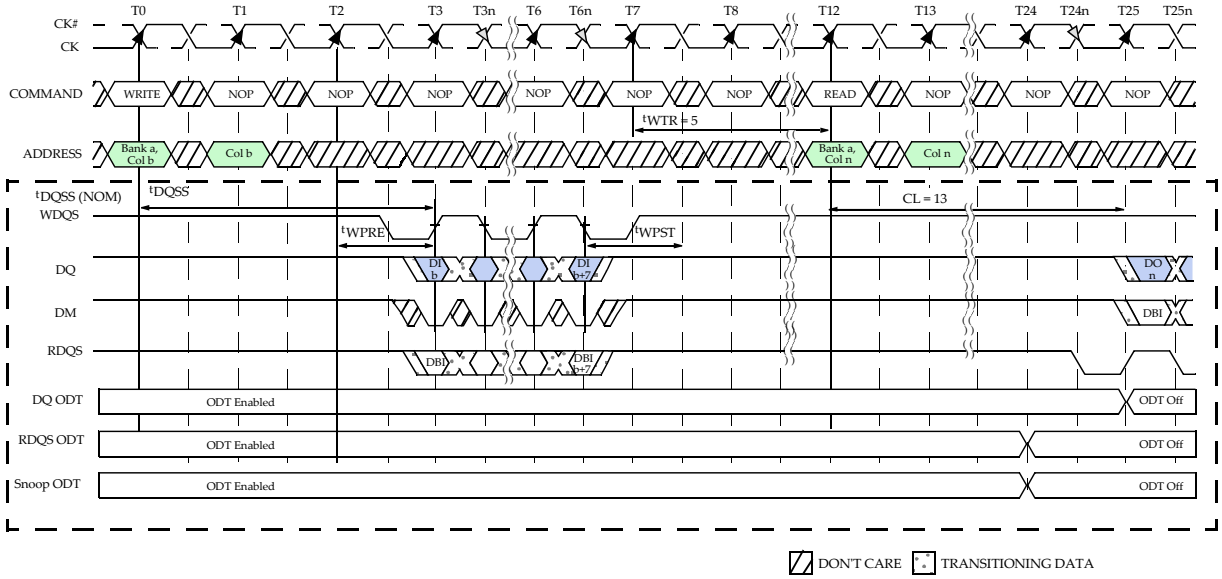


Figure 18: WRITE to READ



1. DI *b* = data-in for column *b*.
2. Seven subsequent elements of data-in are applied in the specified order following DI *b*.
3. t_{WTR} is referenced from the first positive CK edge after the last written data.
4. The READ and WRITE commands are to the same device. However, the READ and WRITE commands may be to different devices, in which case t_{WTR} is not required and the READ command could be applied earlier.
5. A8 is LOW with the WRITE command (auto precharge is disabled).
6. WRITE latency is set to 3.
7. The 8n prefetch architecture requires a 5-clock WRITE to READ turnaround time (t_{WTR}).

PRECHARGE

The PRECHARGE command (see Figure 19) is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (t_{RP}) after the PRECHARGE command is issued.

Input A8 determines whether one or all banks are to be precharged. In case where only one bank is to be precharged, inputs BA0-BA2 select the bank. Otherwise BA0-BA2 are treated as "Don't Care".

Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE command being issued. A PRECHARGE command will be treated as a NOP if there is no open row in that bank, or if the previously open row is already in the process of precharging.

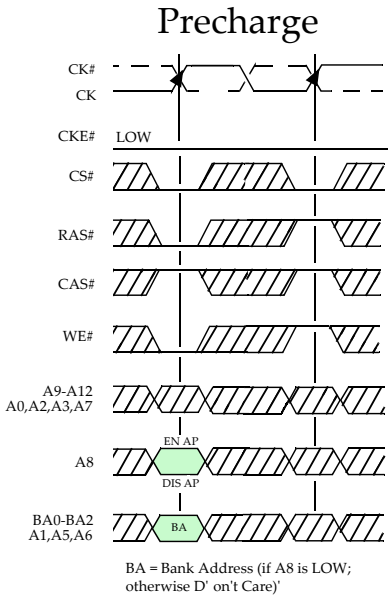


Figure 19: PRECHARGE command

AUTO PRECHARGE

Auto Precharge is a feature which performs the same individual bank precharge function as described above, but without requiring an explicit command. This is accomplished by using A8 (A8 = High), to enable Auto Precharge in conjunction with a specific READ or WRITE command. A precharge of the bank / row that is addressed with the READ or WRITE command is automatically performed upon completion of the read or write burst. Auto Precharge is non persistent in that it is either enabled or disabled for each individual READ or WRITE command.

Auto Precharge ensures that a precharge is initiated at the earliest valid stage within a burst. The user must not issue another command to the same bank until the precharing time (t_{RP}) is completed. This is determined as if an explicit PRECHARGE command was issued at the earliest possible time, as described for each burst type in the Operation section of this specification.

AUTO REFRESH

AUTO REFRESH command (see Figure 20) is used during normal operation of the GDDR4 SGRAM. This command is non persistent, so it must be issued each time a refresh is required.

The refresh addressing is generated by the internal refresh controller. The GDDR4 SGRAM requires AUTO REFRESH commands at an average periodic interval of t_{REFI}. The values of t_{REFI} for different densities are listed in Table 4.

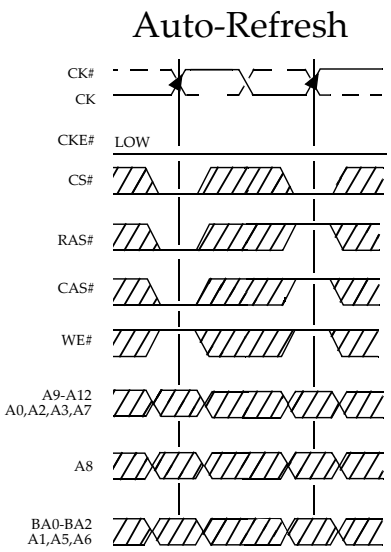


Figure 20: AUTO REFRESH command

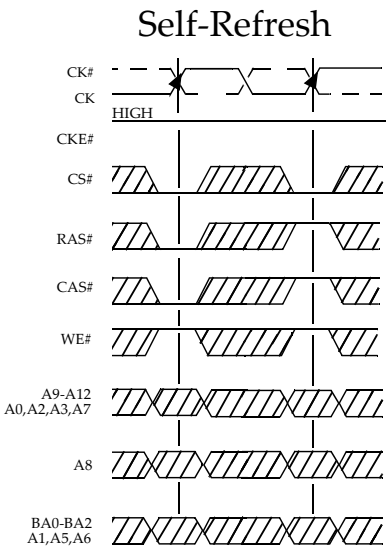


Figure 21: SELF REFRESH command

SELF REFRESH

The SELF REFRESH command (see Figure 21) can be used to retain data in the GDDR4 SGRAM, even if the rest of the system is powered down. When in the self refresh mode, the GDDR4 SGRAM retains data without external clocking.

The SELF REFRESH command is initiated like an AUTO REFRESH command except CKE# is disabled(HIGH). The DLL is automatically disabled upon entering SELF REFRESH and is automatically enabled and reset upon exiting SELF REFRESH. The on-die termination is also disabled upon entering Self Refresh except for CKE# and enabled upon exiting Self Refresh. (t_{XSRD} must be met before a read-like command, i.e, Read, Read with Auto Precharge, Data Terminator Disable can be issued, t_{XSNR} must be met before a non-read-like command can be issued.) Input signals except CKE# are "Don't Care" during SELF REFRESH.

The procedure for exiting self refresh (see Figure 22) requires a sequence of commands. First, CK and CK# must be stable prior to CKE# going back LOW. Once CKE# is LOW, the GDDR4 SGRAM must have NOP commands issued for t_{XSNR} because time is required for the completion of any internal refresh in progress.

A simple algorithm for meeting both refresh and DLL requirements and output calibration is to apply NOPs for t_{XSRD} cycles before applying any other command to allow the DLL to lock and the output drivers to recalibrate.

If the GDDR4 device enters SELF REFRESH with the DLL disabled the GDDR4 device will exit SELF REFRESH with the DLL disabled.

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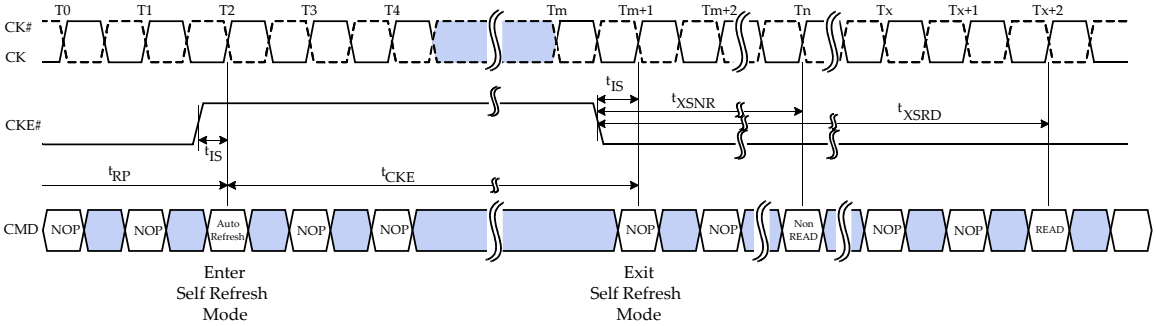

Figure 22: Self Refresh Entry and Exit

Note:
1. Device must be in the "All banks idle" state prior to entering Self Refresh mode.
2. Minimum CKE# pulse width must satisfy t_{CKE}.
3. After issuing Self Refresh command, two more NOPs should be issued.

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Power-Down

GDDR4 SGRAMs require CKE# to be active at all times that an access is in progress: from the issuing of a READ or WRITE command until completion of the burst. For READs, a burst completion is defined when the Read Postamble is satisfied; For WRITEs, a burst completion is defined when the write postamble is satisfied.

Figure 23 shows Power-down entry and exit. Power-down is entered when CKE# is registered HIGH. If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any banks, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CK, CK#, RESET and CKE#. However, power-down duration is limited by the refresh requirements of the device. While in power-down, CKE# and RESET must be HIGH and a stable clock signal must be maintained at the inputs of the GDDR4 SGRAM, while all other input signals are "Don't Care."

The power-down state is synchronously exited when CKE# is registered LOW (in conjunction with a NOP or DESELECT command). A valid executable command may be applied t_{PDEX} cycles later.

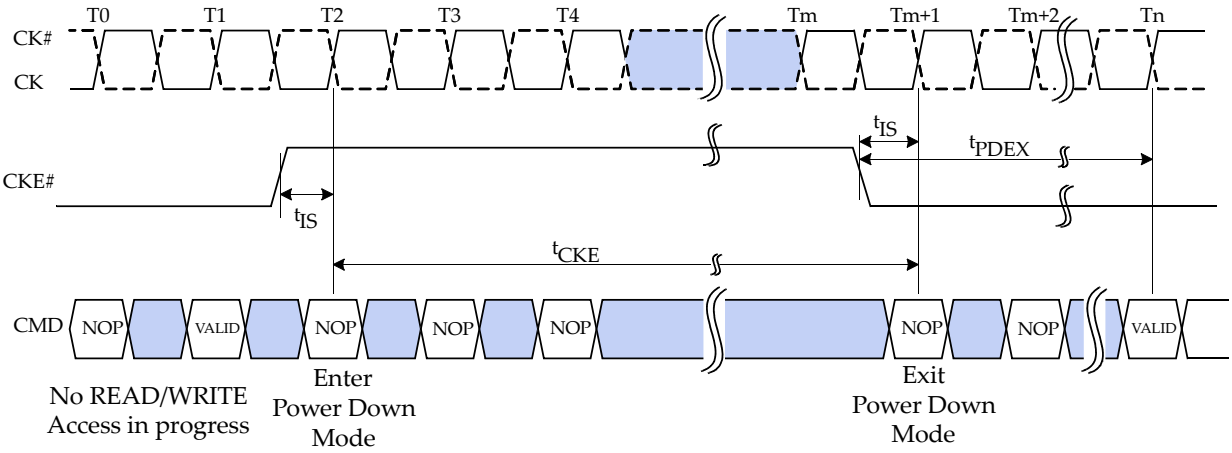

Figure 23: Power-Down Entry and Exit

Note:
1. Minimum CKE# pulse width must satisfy t_{CKE}.
2. After issuing Power Down command, two more NOPs should be issued.

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Table 7 Truth Table – CKE#

CKE#*n-1*	CKE#*n*	CURRENT STATE	COMMAND*n*	ACTION*n*	NOTES
H	H	Power-Down	X	Maintain Power-Down	
H	H	Self Refresh	X	Maintain Self Refresh	
H	L	Power-Down	DESELECT or NOP	Exit Power-Down	
H	L	Self Refresh	DESELECT or NOP	Exit Self Refresh	5
L	H	All Banks Idle	DESELECT or NOP	Precharge Power-Down Entry	
L	H	Bank(s) Active	DESELECT or NOP	Active Power-Down Entry	
L	H	All Banks Idle	AUTO REFRESH	Self Refresh Entry	
L	L		See Table 8		1-3

Notes
1. CKE#*n* is the logic state of CKE# at clock edge *n*; CKE#*n-1* was the state of CKE# at the previous clock edge.
2. Current state is the state of the GDDR4 SGRAM immediately prior to clock edge n.
3. COMMANDn is the command registered at clock edge *n*, and ACTION*n* is a result of COMMAND*n*.
4. All states and sequences not shown are illegal or reserved.
5. DESELECT or NOP commands should be issued on any clock edges occurring during the t_{XSRD} period. A minimum of t_{DL} is needed for the DLL to lock before applying a READ command if the DLL was disabled.

Table 8 Truth Table – Current State Bank *n* – Command To Bank *n*

CURRENT STATE	CS#	RAS#	CAS#	WE#	COMMAND/ACTION	NOTES
Any	H	X	X	X	DESELECT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
	L	L	H	H	ACTIVE (select and activate row)	
Idle	L	L	L	H	AUTO REFRESH	4
	L	L	L	L	MODE REGISTER SET	4
Row Active	L	H	L	H	READ (select column and start READ burst)	6
	L	H	L	L	WRITE (select column and start WRITE burst)	6
	L	L	H	L	PRECHARGE (deactivate row in bank or banks)	5
Read (Auto Precharge Disabled)	L	H	L	H	READ (select column and start new READ burst)	6
	L	H	L	L	WRITE (select column and start WRITE burst)	6, 8
	L	L	H	L	PRECHARGE (only after the READ burst is complete	5
Write (Auto Precharge Disabled)	L	H	L	H	READ (select column and start READ burst)	6, 7
	L	H	L	L	WRITE (select column and start new WRITE burst)	6
	L	L	H	L	PRECHARGE (only after the WRITE burst is complete)	5, 7

Notes
1. This table applies when CKE#*n-1* was LOW and CKE#*n* is LOW (see Table 7) and after t_{XSNR} has been met (if the previous state was self refresh).
2. This table is bank-specific, except where noted (i.e., the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state). Exceptions are covered in the notes below.
3. Current state definitions:
   Idle: The bank has been precharged, and t_{RP} has been met.
   Row Active: A row in the bank has been activated, and t_{RCD} has been met. No data bursts/accesses and no register accesses are in progress.
   Read: A READ burst has been initiated, with auto precharge disabled.

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Write: A WRITE burst has been initiated, with auto precharge disabled.

4. The following states must not be interrupted by a command issued to the same bank. COMMAND INHIBIT or NOP commands, or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and Table 8, and according to Table 9.
   Precharging: Starts with registration of a PRECHARGE command and ends when t_{RP} is met. Once t_{RP} is met, the bank will be in the idle state.
   Row Activating: Starts with registration of an ACTIVE command and ends when t_{RCD} is met. Once t_{RCD} is met, the bank will be in the "row active" state.
   Read w/Auto-Precharge Enabled: Starts with registration of a READ command with auto precharge enabled and ends when t_{RP} has been met. Once t_{RP} is met, the bank will be in the idle state.
   Write w/Auto-Precharge Enabled: Starts with registration of a WRITE command with auto precharge enabled and ends when t_{RP} has been met. Once t_{RP} is met, the bank will be in the idle state.
5. The following states must not be interrupted by any executable command; COMMAND INHIBIT or NOP commands must be applied on each positive clock edge during these states.
   Refreshing: Starts with registration of an AUTO REFRESH command and ends when t_{RC} is met. Once t_{RC} is met, the GDDR4 SGRAM will be in the all banks idle state.
   Accessing Mode Register: Starts with registration of a MODE REGISTER SET command and ends when t_{MRD} has been met. Once t_{MRD} is met, the GDDR4 SGRAM will be in the all banks idle state.
   Precharging All: Starts with registration of a PRECHARGE ALL command and ends when t_{RP} is met. Once t_{RP} is met, all banks will be in the idle state.
   READ or WRITE: Starts with the registration of the ACTIVE command and ends the last valid data nibble.
6. All states and sequences not shown are illegal or reserved.
7. Not bank-specific; requires that all banks are idle, and bursts are not in progress.
8. May or may not be bank-specific; if multiple banks are to be precharged, each must be in a valid state for precharging.
9. Reads or Writes listed in the Command/Action column include Reads or Writes with auto precharge enabled and Reads or Writes with auto precharge disabled.
10. Requires appropriate DM masking.
11. A WRITE command may be applied after the completion of the READ burst

Table 9 Truth Table – Current State Bank *n* – Command To Bank *m*

CURRENT STATE	CS#	RAS#	CAS#	WE#	COMMAND/ACTION	NOTES
Any	H	X	X	X	DESELECT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	X	X	X	X	Any Command Otherwise Allowed to Bank m	
Row Activating, Active, or Precharging	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	6
	L	H	L	L	WRITE (select column and start WRITE burst)	6
	L	L	H	L	PRECHARGE	
Read (Auto Precharge Disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	6
	L	H	L	L	WRITE (select column and start WRITE burst)	6
	L	L	H	L	PRECHARGE	
Write (Auto Precharge Disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	6, 7
	L	H	L	L	WRITE (select column and start new WRITE burst)	6
	L	L	H	L	PRECHARGE	
Read (With Auto Precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	6
	L	H	L	L	WRITE (select column and start WRITE burst)	6
	L	L	H	L	PRECHARGE	
Write (With Auto Precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	6
	L	H	L	L	WRITE (select column and start new WRITE burst)	6
	L	L	H	L	PRECHARGE	

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Notes
1. This table applies when CKE#*n-1* was LOW and CKE#*n* is LOW (see Table 8) and after t_{XSNR} has been met (if the previous state was self refresh).
2. This table describes alternate bank operation, except where noted (i.e., the current state is for bank *n* and the commands shown are those allowed to be issued to bank *m*, assuming that bank *m* is in such a state that the given command is allowable). Exceptions are covered in the notes below.
3. Current state definitions:

Idle: The bank has been precharged, and t_{RP} has been met.
Row Active: A row in the bank has been activated, and t_{RCD} has been met. No data bursts/accesses and no register accesses are in progress.
Read: A READ burst has been initiated, with auto precharge disabled.
Write: A WRITE burst has been initiated, with auto precharge disabled.
Read with Auto Precharge Enabled: See following text
Write with Auto Precharge Enabled: See following text

3a. The read with auto precharge enabled or write with auto precharge enabled states can each be broken into two parts: the access period and the precharge period. For read with auto precharge, the precharge period is defined as if the same burst was executed with auto precharge disabled and then followed with the earliest possible PRECHARGE command that still accesses all of the data in the burst. For write with auto precharge, the precharge period begins when t_{WR} ends, with t_{WR} measured as if auto precharge was disabled. The access period starts with registration of the command and ends where the precharge period (or t_{RP}) begins. During the precharge period of the read with auto precharge enabled or write with auto precharge enabled states, ACTIVE, PRECHARGE, READ and WRITE commands to the other bank may be applied. In either case, all other related limitations apply (e.g., contention between read data and write data must be avoided).

3b. The minimum delay from a READ or WRITE command with auto precharge enabled, to a command to a different bank is summarized below.

Table 10 Minimum Delay Between Commands to Different Banks with Auto Precharge Enabled

From Command	To Command	Minimum delay (with concurrent auto precharge)
WRITE with AUTO PRECHARGE	READ or READ with AUTO PRECHARGE	$[WL + (BL/2)]\ t_{CK} + t_{WTR}$
	WRITE or WRITE with AUTO PRECHARGE	$(BL/2)\ t_{CK}$
	PRECHARGE	$1\ t_{CK}$
	ACTIVE	$1\ t_{CK}$
READ with AUTO PRECHARGE	READ or READ with AUTO PRECHARGE	$(BL/2) * t_{CK}$
	WRITE or WRITE with AUTO PRECHARGE	$[CL + (BL/2) + 1 - WL] * t_{CK}$
	PRECHARGE	$1\ t_{CK}$
	ACTIVE	$1\ t_{CK}$

CL = CAS latency (CL) rounded up to the next integer
BL = Burst length
WL = WRITE latency

4. AUTO REFRESH and MODE REGISTER SET commands may only be issued when all banks are idle.
5. All states and sequences not shown are illegal or reserved.
6. READs or WRITEs listed in the Command/Action column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
7. Requires appropriate DM masking.

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READ and WRITE DBI

The GDDR4 Data Bus Inversion (DBI) logic reduces the AC power (DBIac) as shown in the flow chart in Figure 24a for READs. The GDDR4 DBI logic reduces the AC power as shown in the flow chart in Figure 25a for WRITEs. GDDR4 DBI logic reduces the DC power (DBIdc) as shown in the flow chart in Figure b for READs. The GDDR4 DBI logic reduces the DC power as shown in the flow chart in Figure b for WRITEs.

The mapping of the DBI flag for READs and WRITEs are as follows:

Table 11 DBI Flag mapping for READ

Data	DBI Flag
DQ[7:0]	DM[0]
DQ[15:8]	DM[1]
DQ[23:16]	DM[2]
DQ[31:24]	DM[3]

Table 12 DBI Flag mapping for WRITE

Data	DBI Flag
DQ[7:0]	RDQS[0]
DQ[15:8]	RDQS[1]
DQ[23:16]	RDQS[2]
DQ[31:24]	RDQS[3]

Note: When the DBI Flag equals 1 the Data is inverted

The timing diagram in Figure 26a shows the READ timing of the DM and the read data DQ. The timing diagram in Figure 26b shows the WRITE timing of the RDQS and the write data DQ.

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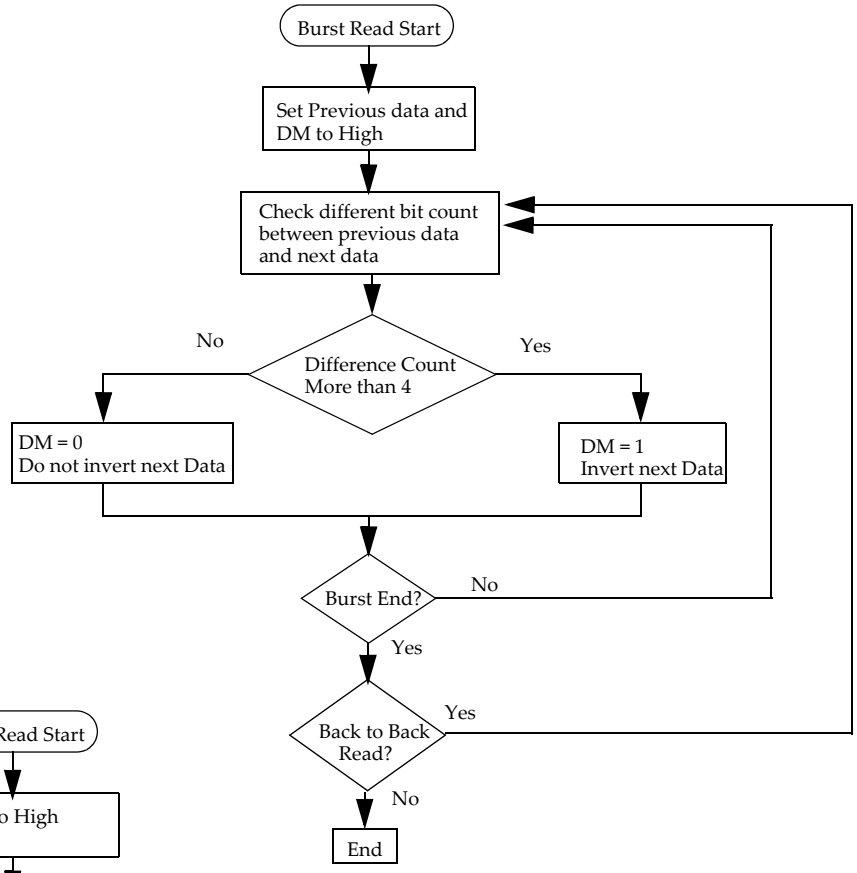
Figure 24: a Flow Chart READ DBIac



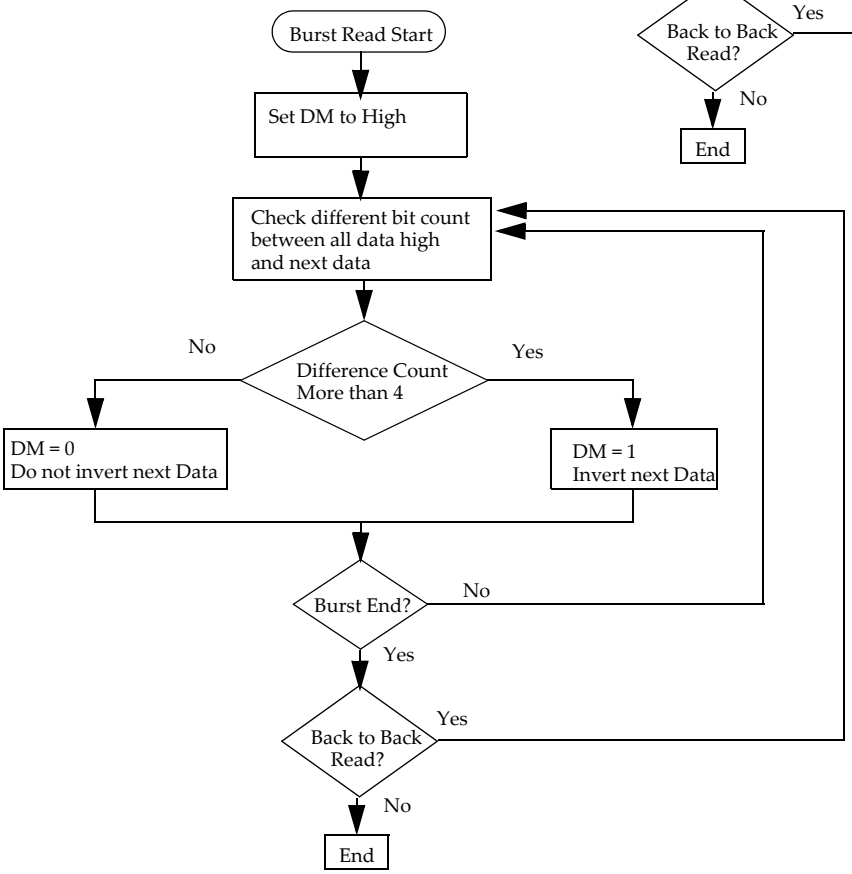
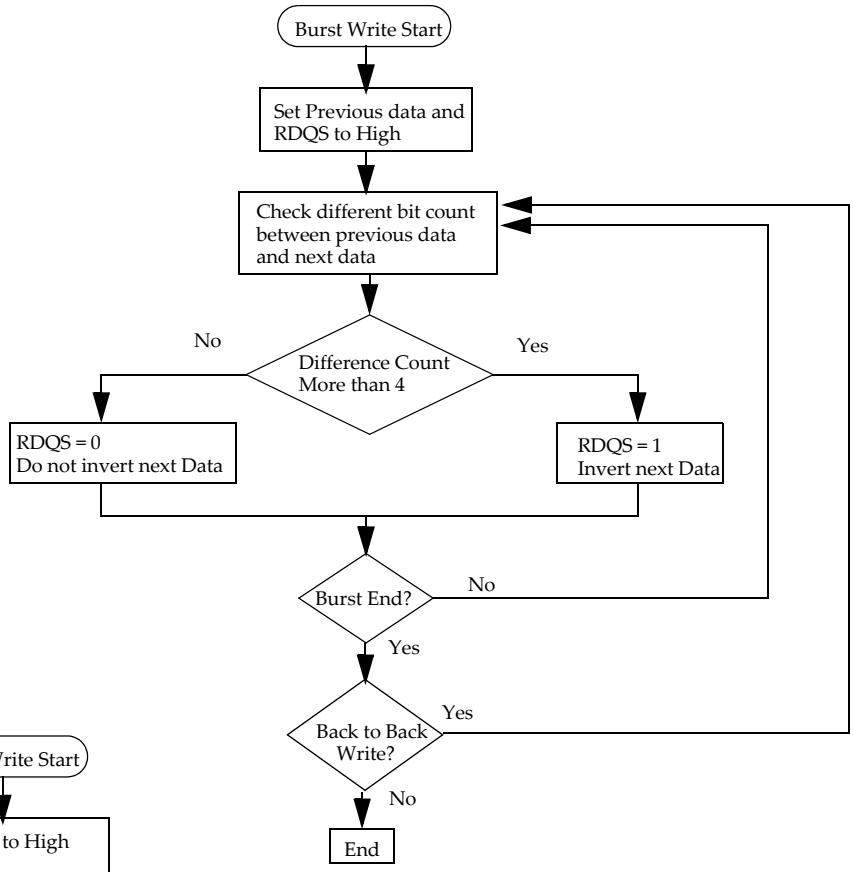


Figure24: b Flow Chart READ DBIdc

Figure 25: a
Flow Chart
WRITE DBIac



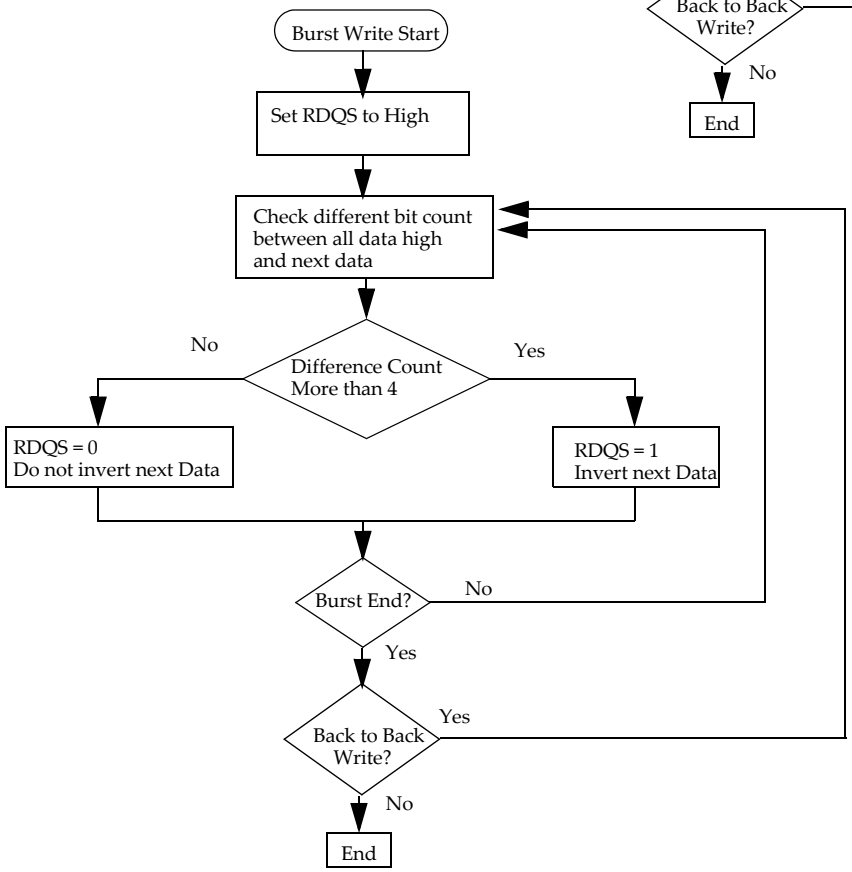


Figure 25: b
Flow Chart
WRITE DBIdc

Figure 26: a) READ DBI Timing

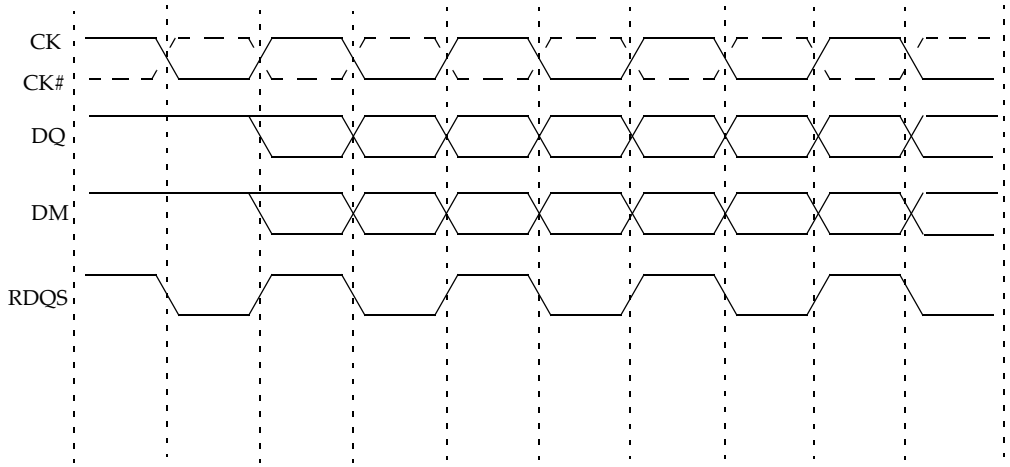


Figure 26: b) WRITE DBI Timing

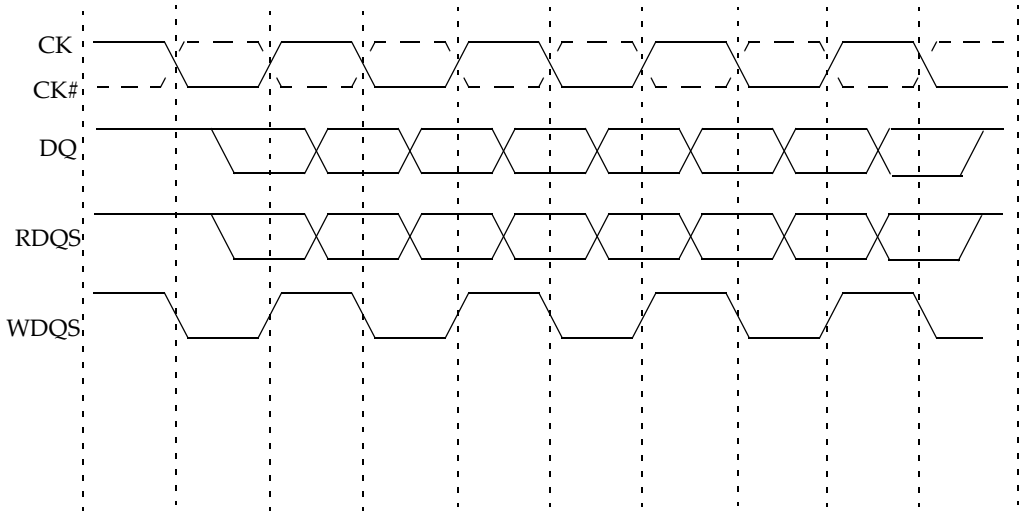


Figure 27: a) Block Diagram For READS

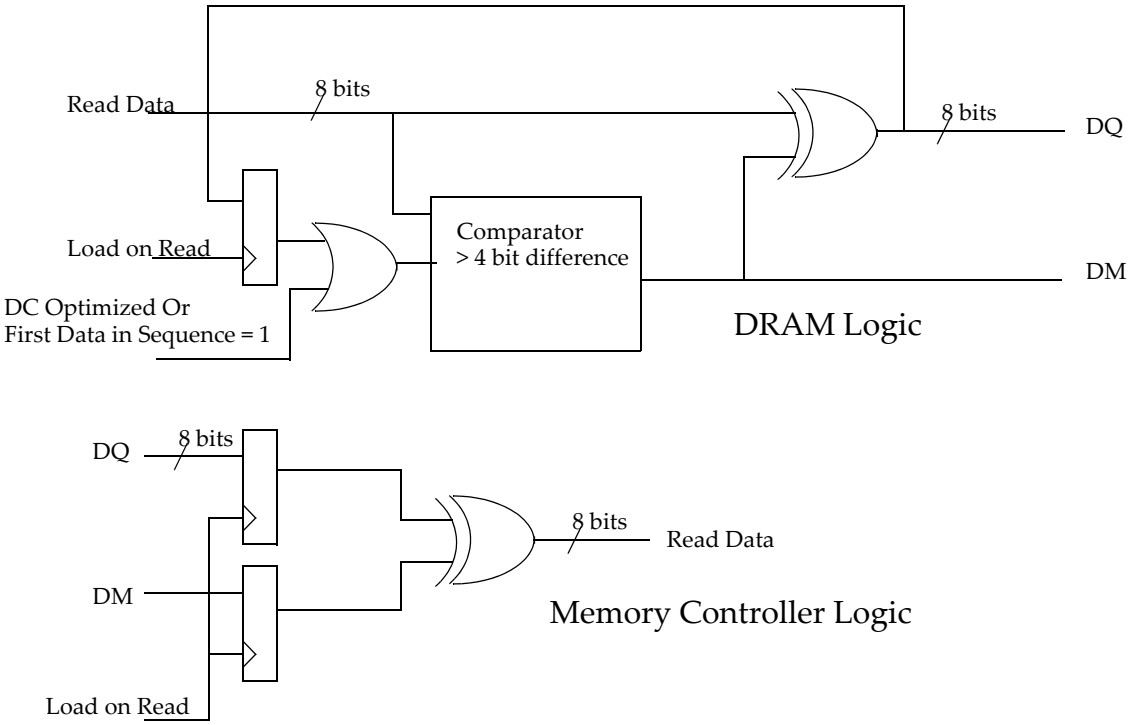
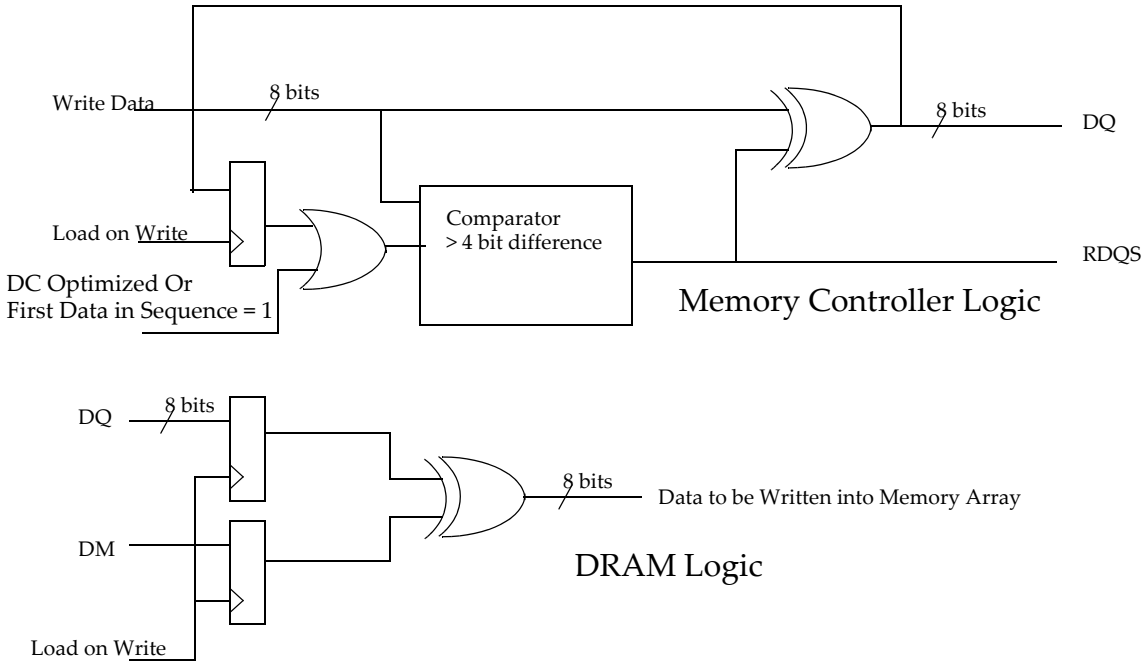


Figure 27: b) Block Diagram For WRITES



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CLOCKING, DATA CAPTURE & TRAINING

Data Capture

The Data Strobe (DQS) functionality for GDDR4 SGRAMs includes both a uni-directional, single-ended read strobe per byte, and a uni-directional, single-ended write strobe per byte.

Write Data Strobe (WDQS) is center-aligned with Write Data and Read Data Strobe(RDQS) is edge-aligned with Read Data. WDQS0 is assigned to DQ0~DQ7 and DM0, WDQS1; DQ8~DQ15 and DM1, WDQS2; DQ16~DQ23 and DM2, WDQS3; DQ24~DQ31 and DM3. RDQS0 is assigned to DQ0~DQ7, RDQS1; DQ8~DQ15, RDQS2; DQ16~DQ23, RDQS3; DQ24~DQ31.

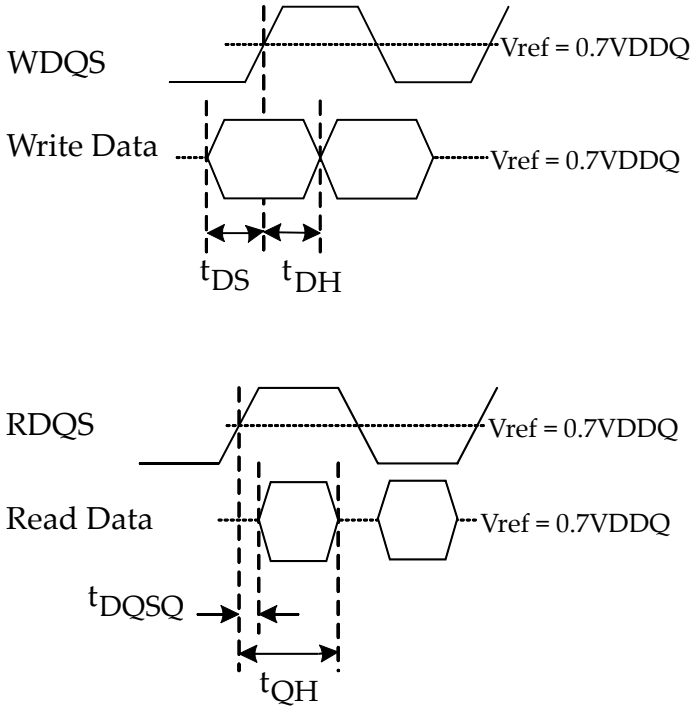

Figure 28: WDQS and RDQS

Data Training

GDDR4 includes a training scheme that uses normal WRITE and READ operations for data training. Before starting data training, the GDDR4 SGRAM must be powered up and initialized in a predefined manner to prevent undefined operations. READ data training is started by going through step 1~ step 8 sequentially. After the READ data training is completed, the WRITE data training can be started or vice versa. The preferred manner is READ data training first and then WRITE data training.

t_{CKL} is defined as the low speed clock frequency used to train READs and is specified by the user. t_{CKL} may not violate the t_{CK} specification. t_{SHFC} is the Stable High Frequency Clock that has been trained.

READ Data Training Sequence

Step1:

The GDDR4 SGRAM must be initialized properly and set to the low speed clock frequency.

Step2:

Issue a WRITE command to load the data pattern at $t_{CKL.}$ The Memory Contoller Logic defines the data pattern for the training. During the WRITE, REFRESH commands can be used if required.

Step 3:

After completing the WRITE at t_{CKL}, the clock frequency is then changed to the target frequency. A DLL reset is required after changing the frequency. The READ command must occur within 10ms to prevent data loss in case there is no REFRESH command.

Step 4.

The controller needs to select a DQ(or Byte) to be trained and set a minimum delay.

Step 5.

Issue normal READ commands. During normal READ operation, REFRESH commands can be issued if required.

Step 6.

After the READ command is issued, if the delay step is not Max. then go to Step 5. Repeat Step 5 and Step 6 until all of the delay steps are scanned.

Step 7.

If all DQs(or Byte) are not checked, then go to Step 4. Repeat Step 4 to Step 7 until all the DQs are scanned.

Step 8.

If all completed, then END of READ data training

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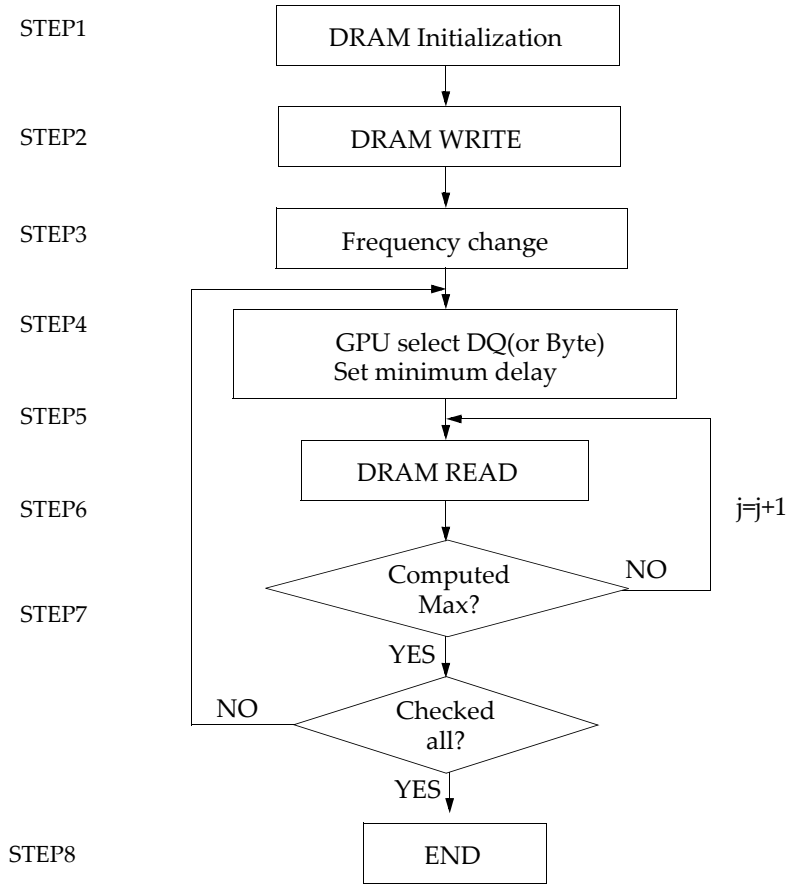

Figure 29: Read Data Training Flowchart

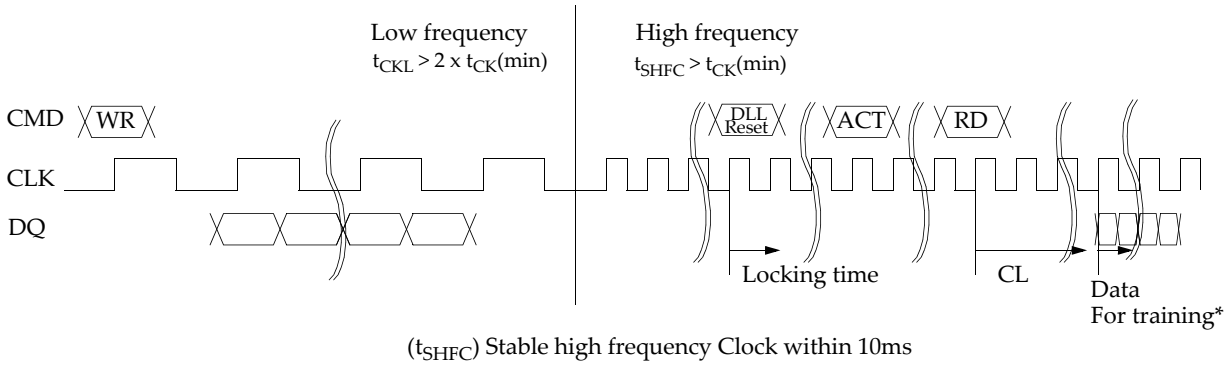

Figure 30: Read Data Training Timing Diagram

WRITE Data Training Sequence

The WRITE data training procedure is almost the same as the READ data training procedure. WRITE data training does not require the frequency change that is required in READ data training. To make sure the WRITE completes correctly, the low speed clock frequency is selected for the WRITE operation during the READ data training. Whereas WRITE data training case does not require such a frequency change because read data is already trained.

Step 1.

START of WRITE data training

Step 2.

The controller needs to select a DQ(or Byte) to be trained, and then set minimum delay.

Step 3.

Issue WRITE command and then READ the data for the validation. During the WRITE and READ operations, REFRESH commands can be issued if required.

Step 4.

Increase a delay step. If the step is not Max. then go to Step 1. Repeat Steps 3~4 until scan all the delay steps.

Step 5.

If all DQ(or Byte) is not checked, go to Step 2. Repeat Steps 2~5 until scan all DQs(or bytes)

Step 6.

END of WRITE data training

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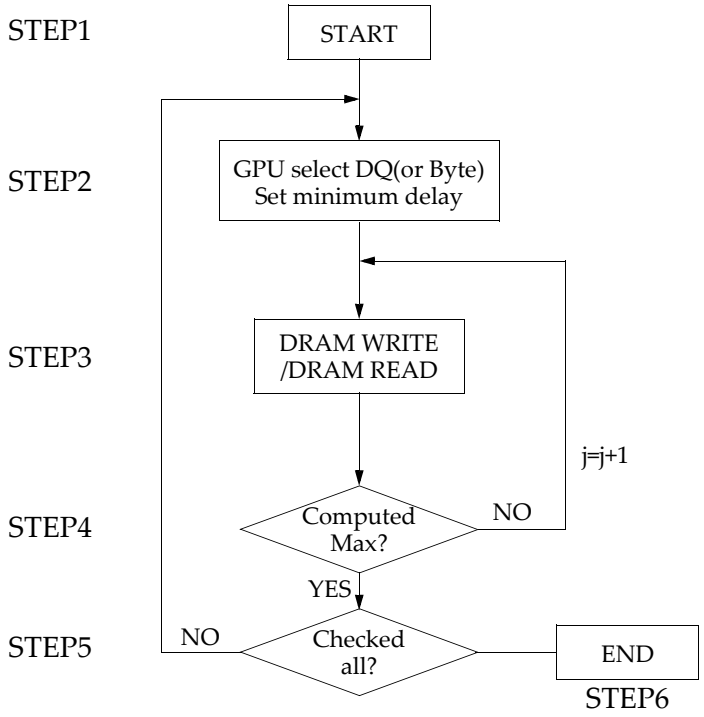

Figure 31: WRITE Data Training Flowchart

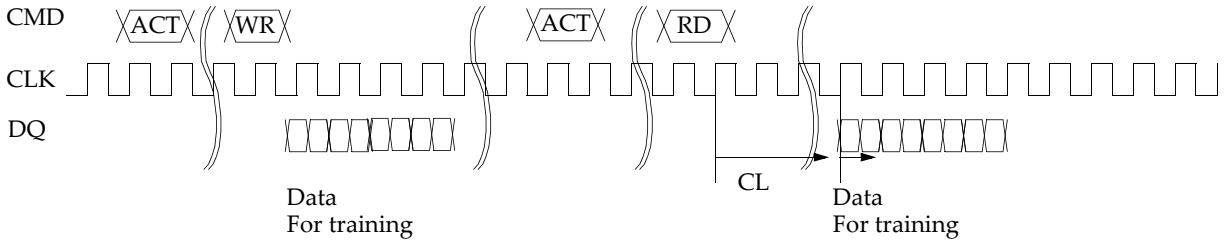

Figure 32: DRAM WRITE Data Training Timing Diagram

Changing Clock Frequency

Clock Frequency Change Sequence - AREF commands

Step 1) Wait until all commands have finished, all banks are idle.

Step 2) Only NOP or DESELECT or AREF commands may be issued (must meet setup/hold relative to clock while clock is changing) to GDDR4 SGRAM for the entire sequence unless stated to do otherwise. AREF commands must fulfill AREF burst requirements.

Step 3) If new clock period is between the range of $t_{CK\ (Max\ DLL\ Off)}$ to $_{tCK\ (Min\ DLL\ Off)}$, then turn DLL off via EMRS register write.

Step 4) Change the clock frequency and wait until clock is stabilized.

Step 5) If new clock period is smaller than $_{tCK(Max\ DLL\ On)}$, then turn DLL on via EMRS register write.

Step 6) If the DLL is enabled, then complete steps 6a and 6b:

6a) Reset the DLL by writing to the MRS register.

6b) Wait t_{DL} clock cycles before issuing any commands to the GDDR4 SGRAM.

Step 7) GDDR4 SGRAM is ready for normal operation.

Clock Frequency Change Sequence - NOP/DESELECT commands

Step 1) Wait until all commands have finished, all banks are idle.

Step 2) Send NOP or DESELECT (must meet setup/hold relative to clock while clock is changing) to GDDR4 SGRAM for the entire sequence unless stated to do otherwise. The user must take are of AREF requirements.

Step 3) If new clock period is between the range of $t_{CK(Max\ DLL\ Off)}$ to $t_{CK\ (Min\ DLL\ Off)}$, then turn DLL off via EMRS register write.

Step 4) Change the clock frequency and wait until clock is stabilized.

Step 5) If new clock period is smaller than $t_{CK(Max\ DLL\ On)}$, then turn DLL on via EMRS register write.

Step 6) If the DLL is enabled, then complete steps 6a and 6b:

6a) Reset the DLL by writing to the MRS register.

6b) Wait t_{DL} clock cycles before issuing any commands to the GDDR4 SGRAM.

Step 7) GDDR4 SGRAM is ready for normal operation.

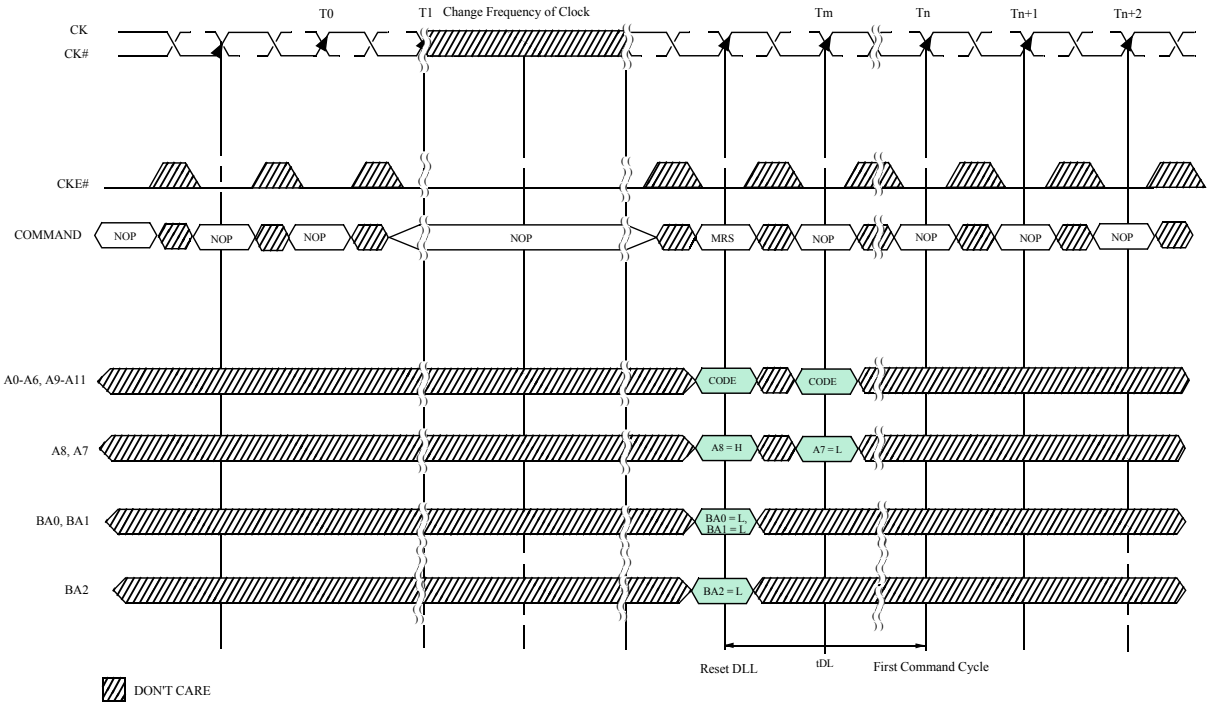

Figure 33: DLL is on and new frequency range DLL is on

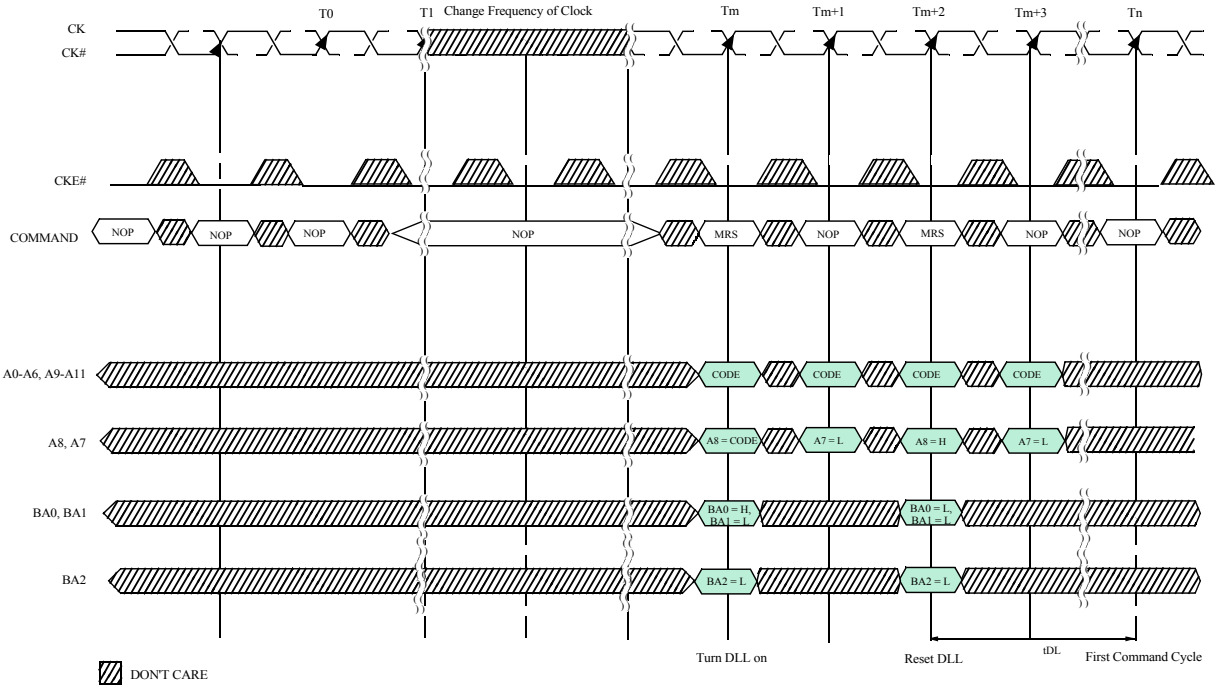

Figure 34: DLL is off and new frequency range DLL is on

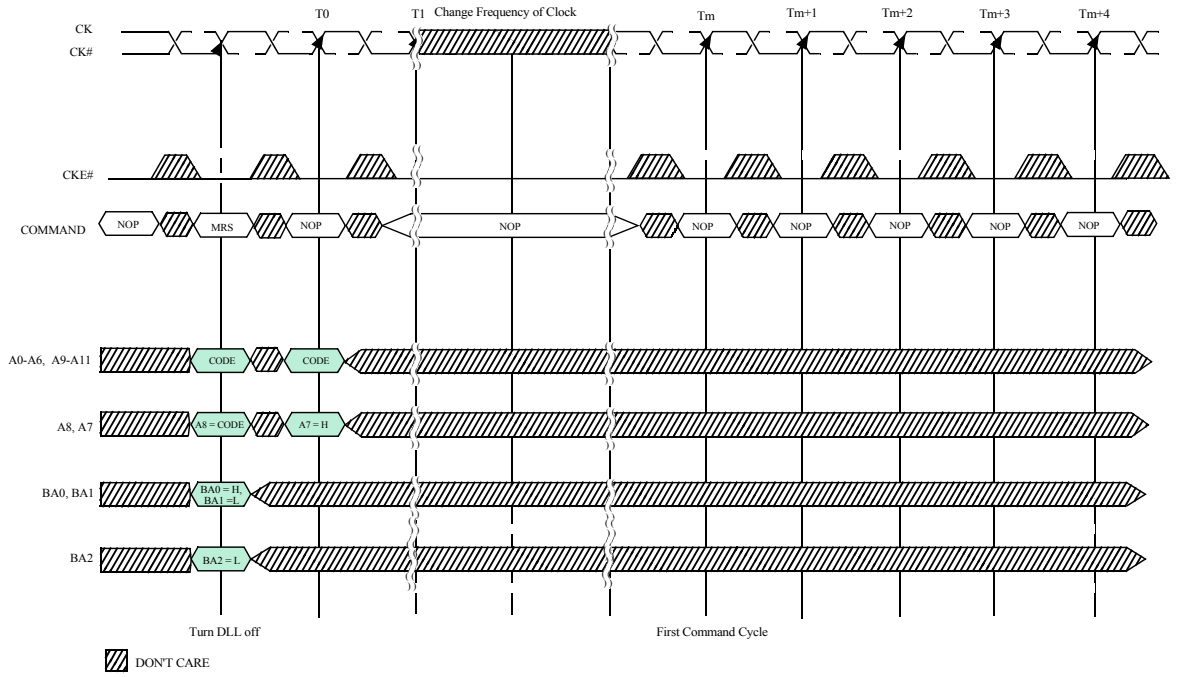

Figure 35: DLL is on and new frequency range DLL is off

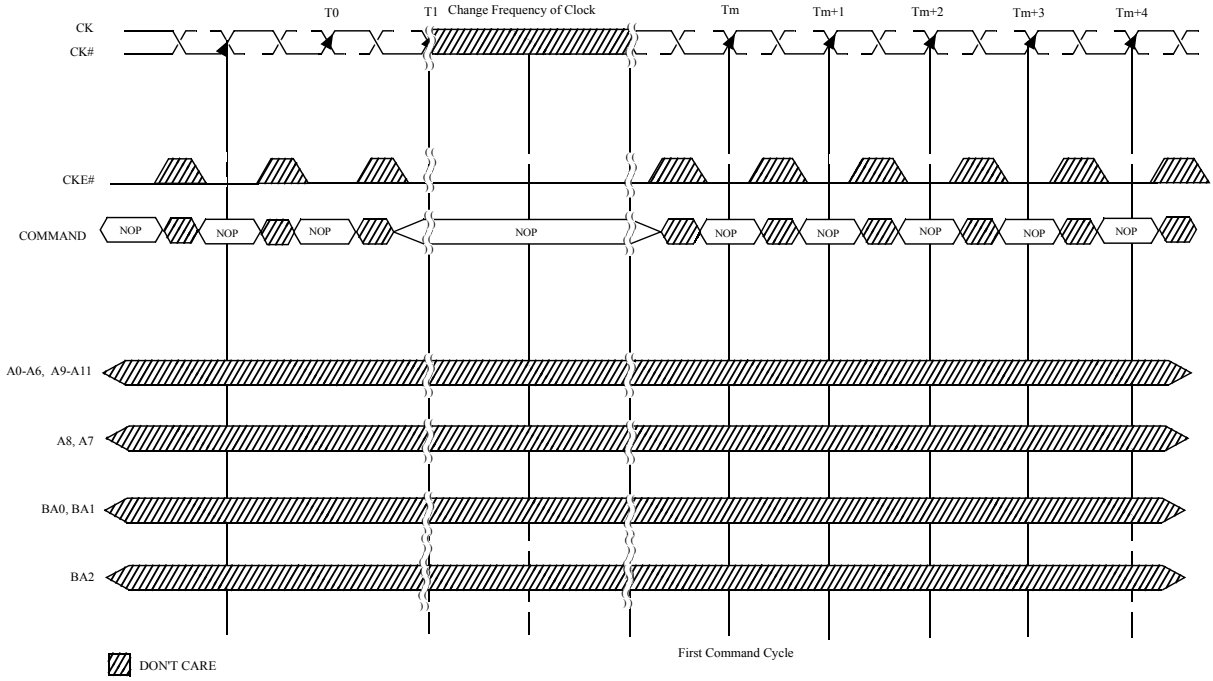

Figure 36: DLL is off and new frequency range DLL is off

DRIVER & TERMINATION

Programmable Impedance Output Buffer and Active Terminator

GDDR4 SGRAM uses a programmable impedance output buffer. This enables a user to match the driver impedance to the system. To adjust the impedance, an external precision resistor (RQ) is connected between the ZQ pin and Vss. The value of the resistor must be six times the desired driver impedance. For example, a 240ohm resistor is required for an output impedance of 40ohm. To ensure that output impedance is one-sixth the value of RQ (within 10 percent), the range of RQ is 210ohm to 270ohm (35ohm–45ohm output impedance). RESET, CK and CK# are not internally terminated. CK and CK# need to be terminated on the system using external one percent resistors to Vdd.

The output impedance is updated during all AUTO REFRESH commands to compensate for variations in supply voltage and temperature. The output impedance updates are transparent to the system. Impedance updates do not affect device operation, and all data sheet timing and current specifications are met during an update.

The device will power up with an output impedance set to nominal, close to 40ohm. To guarantee optimum output driver impedance after power-up, the GDDR4 SGRAM needs 350 cycles after the clock is applied and stable to calibrate the impedance. The user may operate the part with fewer than 350 clock cycles, but optimal output impedance is not guaranteed.

The value of RQ is also used to calibrate the internal address/command termination resistors. The termination values are selectable at power up using CKE# and A0 with values of 60, 120 and 240ohm supported.

The value of RQ is used to calibrate the internal DQ termination resistors. The two termination values that are selectable are 1/4 of RQ and 1/2 of RQ.

Impedance Control

GDDR4 SGRAM output driver impedance and termination impedance are programmable through EMRS. The offset impedance step values may be non-linear and will vary across suppliers and across the yield distribution and across temperature. The offsets are only applied to the DQ, DQM, RDQS and WDQS signals. No programmability is provided for the address and command signals. With negative offset steps the Driver Strength will be decreased and the Ron will be increased. With positive offset steps the Driver Strength will be increased and Ron will be decreased. With negative offset steps the Termination value will be increased. With positive offset steps the Termination value will be decreased. The Termination offset steps will also be applied to the Pullup Driver Strength settings. IV curves and AC timings are only guaranteed with zero offset.

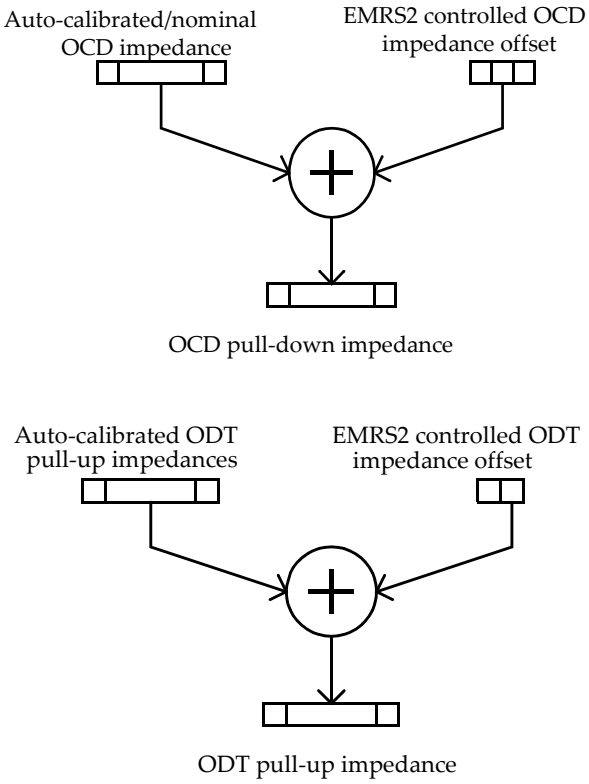

Figure 37: Offsets

Data Terminator Disable

(BUS SNOOPING FOR READ COMMANDS)

Bus snooping for READ commands is used to control the on-die termination in the dual load configuration. The GDDR4 SGRAM will disable the on-die termination when a READ command is detected, regardless of the state of CS#, when the ODT for the DQ pins are set for dual loads. The on-die termination is disabled x clocks after the READ command where x equals CL - 1 and stays off for a duration of BL + 2. In a two-rank system, both DRAM devices snoop the bus for READ commands to either device and both will disable the on-die termination if a READ command is detected. The on-die terminations for all other pins on the device are always on for both a single-rank system and a dual-rank system.

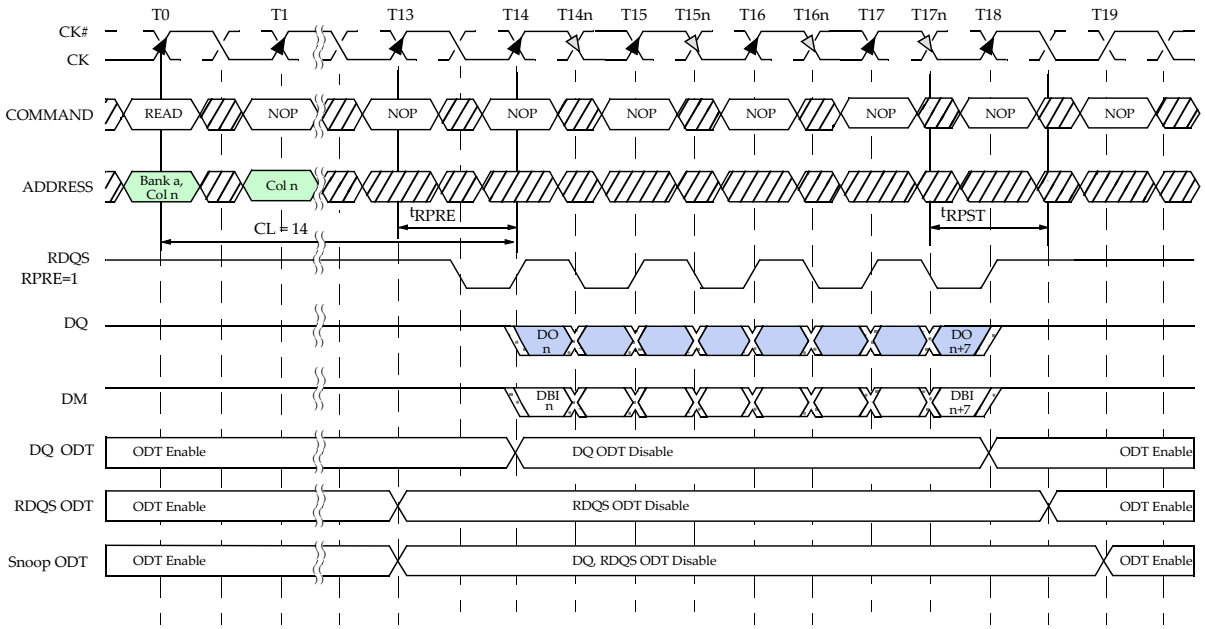

Figure 38: Data Terminator Disable Timing

Notes
1. DO n = data-out from column n.
2. Three subsequent elements of data-out appear in the specified order following DO n.
3. Shown with nominal t_{AC} and t_{DQSQ}.
4. RDQS will start driving high one-half clock cycle prior to the first falling edge.
5. The Data Terminators are disabled starting at CL - 1 and the duration is BL + 2.
6. READs to either rank disable both ranks' termination regardless of the logic level of CS#.

LPTERM

As GDDR4 SGRAM gains adoption in mobile applications there is a desire from users to support a mode where terminations can be disabled on the memory for the majority of the signals while maintaining termination on the strobes for proper clocking of the interface. The intent is the GDDR4 SGRAM would be operated at a slower condition possibly with the DLL disabled while still meeting the AC timings of the DRAM.

This feature is available during normal operation but requires the memory controller to meet the device specifications by operating at a reduced frequency. Absolute frequencies supported by the GDDR4 SGRAM are vendor specific.

Control of the Low power mode is accomplished through the mode register field defined in Table 13. The Low Power Termination mode can only be enabled when DQ termination is enabled in the ZQ/2 or ZQ/4 mode.

Table 13 Low Power Termination Control

	LPTERM
0	Disabled
1	Enabled

Table 14 defines the termination states for each signal group. The value EMRS[Termination] is meant to reference the value defined in the EMRS register for the state of ODT termination for actual termination impedance.

Table 14 Termination Support

Signal Group	LPTERM Disabled	LPTERM Enabled
CLK, CLK#	N/A	N/A
Address	Enabled	Disabled
RAS#, CAS#, WE#, CS#,	Enabled	Disabled
CKE#	Enabled	Disabled
RDQS[3:0]	EMRS[Termination]	Disabled
WDQS[3:0]	EMRS[Termination]	EMRS[Termination]
DQ[31:0], DM[3:0]	EMRS[Termination]	Disabled

OPERATING CONDITIONS

Absolute Maximum Ratings

Voltage on Vdd Supply
Relative to Vss..... -0.5V to +2.5V
Voltage on VddQ Supply
Relative to Vss ..... -0.5V to +2.5V
Voltage on Vref and Inputs
Relative to Vss ..... -0.5V to +2.5V
Voltage on I/O Pins
Relative to Vss ..... -0.5V to VddQ +0.5V
Storage Temperature (plastic) ..... -55°C to +150°C
Short Circuit Output Current 50mA

*Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 15 Capacitance

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Delta Input/Output Capacitance: DQs, DQS, DM	DCio			pF	
Delta Input Capacitance: Command and Address	DCi_1			pF	
Delta Input Capacitance: CK, CK#	DCi_2			pF	
Input/Output Capacitance: DQs, DQS, DM	Cio			pF	
Input Capacitance: Command and Address	Ci_1			pF	
Input Capacitance: CK, CK#	Ci_2			pF	
Input Capacitance: CKE#	Ci_3			pF	

Table 16 Thermal Characteristics

Parameter	Description	Value	Units	Notes
Theta_JA	Thermal resistance junction to ambient		$^oC/W$	1,2,3,5
TJ_MAX	Maximum operating junction temperature		^oC	4
TC_MAX	Maximum operating case temperature		^oC	4
Theta_JC	Thermal resistance from junction to case		$^oC/W$	1,6
Theta_JB	Thermal resistance junction to board		$^oC/W$	1,2,6

Notes:
1. Measurement procedures for each parameter must follow standard procedures defined in the current JEDEC JESD-51 standard.
2. Theta_JA and Theta_JB must be measured with the high effective thermal conductivity test board defined in JESD51-7
3. Airflow information must be documented for Theta_JA.
4. TJ_MAX and TC_MAX are documented for normal operation in this table. These are not intended to reflect reliability limits.
5. Theta_JA should only be used for comparing the thermal performance of single packages and not for system related junction temperature prediction.
6. Theta_JB and Theta_JC are derived through a package thermal simulation.
7. Values are guaranteed by design but not tested in production

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AC & DC Characteristics

All GDDR4 SGRAMs are designed for 1.5V typical voltage supplies but may optionally support 1.8V typical voltage supplies. The GDDR4 SGRAM vendor may restrict VDD and VDDQ combinations. The supported VDD and VDDQ will be vendor specific. The interface of GDDR4 with 1.5V VDDQ will follow the POD15 specification and GDDR4 SGRAMs with 1.8V VDDQ will follow the POD18 specification.

Table 17 DC Operating Conditions

		POD15			POD18				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Note**
Device Supply Voltage	VDD	1.455	1.5	1.545	1.710	1.8	1.890	V	1
Output Supply Voltage	VDDQ	1.455	1.5	1.545	1.710	1.8	1.890	V	1
Reference Voltage	VREF	0.69 * VDDQ		0.71 * VDDQ	0.69 * VDDQ		0.71 * VDDQ	V	2
DC Input Logic HIGH Voltage	VIH (DC)	VREF + 0.12			VREF + 0.15			V	
DC Input Logic LOW Voltage	VIL (DC)			VREF - 0.12			VREF - 0.15	V	
Input Leakage Current Any Input 0V <= V_{IN} <= VDD (All other pins not under test = 0V)	Il				-5		5	µs	
Output Leakage Current (DQs are disabled; 0V <= Vout <= VDDQ)	Ioz				-5		5	µs	
Output Logic LOW Voltage	VOL (DC)			0.62			0.76	V	

Notes:
1. GDDR4 SGRAM is designed to tolerate PCB designs with separate VDD and VDDQ power regulators.
2. AC noise in the system is estimated at 50mV pk-pk for the purpose of DRAM design

Table 18 AC Operating Conditions

		POD15			POD18				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Note**
AC Input Logic HIGH Voltage	VIH (AC)	VREF + 0.200			VREF + 0.250			V	
AC Input Logic LOW Voltage	VIL (AC)			VREF - 0.200			VREF - 0.250	V	

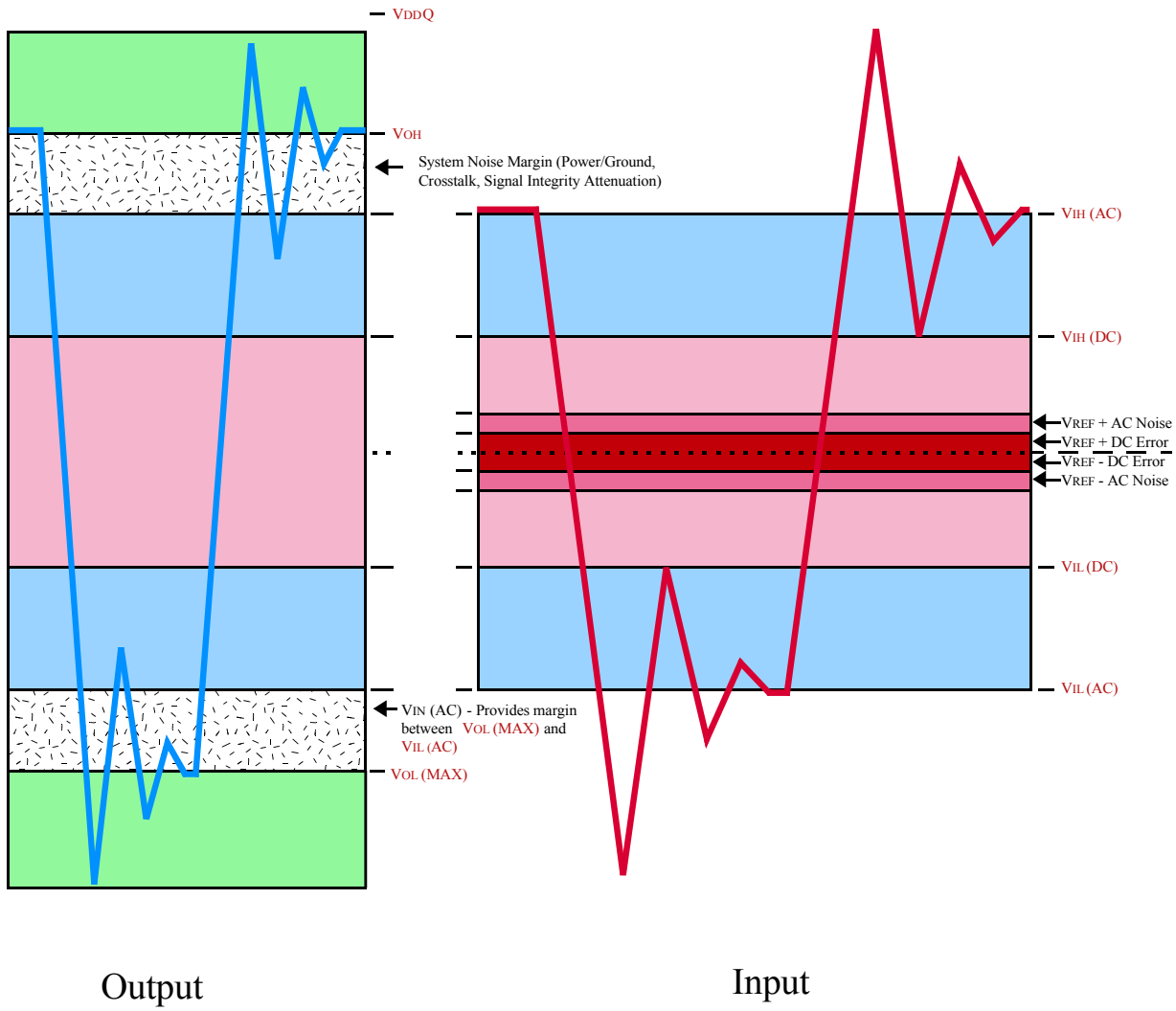

Figure 39: Voltage Waveform

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Table 19 Clock Input Operating Conditions

		POD15		POD18			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Note**
Clock Input Mid-Point Voltage ; CK and CK#	VMP (DC)	VREF - 100mV	VREF + 100mV	1.16	1.36	V	1,2,3
Clock Input Differential Voltage ; CK and CK#	VID (DC)	0.22		0.22	VDDQ	V	2,4
Clock Input Differential Voltage ; CK and CK#	VID (AC)	0.400		0.5	VDDQ + 0.5	V	4
Clock Input Voltage Level; CK and CK#	VIN	0.350	VDDQ + 0.3	0.42	VDDQ + 0.3	V	
Clock Input Crossing Point Voltage ; CK and CK#	VIX (AC)	VREF - 0.12	VREF + 0.12	VREF - 0.15	VREF + 0.15	V	3

Notes :
1. This provides a minimum of 0.95V to a maximum of 1.15V, and is always 70% of VDDQ with POD15
2. For AC operations, all DC clock requirements must be satisfied as well.
3. The value of VIX is expected to equal 70% VDDQ for the transmitting device and must track variations in the DC level of the same.
4. VID is the magnitude of the difference between the input level in CK and the input level on CK#. The input reference level for signals other than CK and CK# is VREF.
5. The CK and CK# input reference level (for timing referenced to CK and CK#) is the point at which CK and CK# cross.
6. CK and CK# input slew rate must be greater than 3V/ns for VDDQ = 1.5V (typ) or greater than 4V/ns for VDDQ = 1.8V (typ)

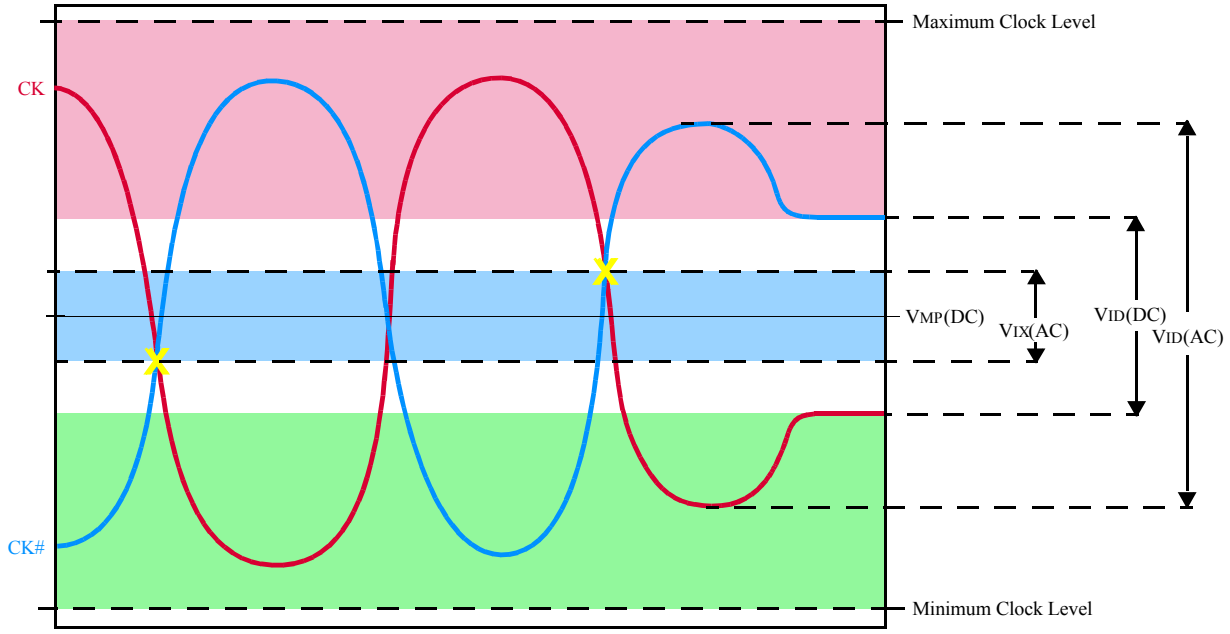

Figure 40: Clock Input Waveform

Table 20 IDD SPECIFICATIONS AND CONDITIONS

PARAMETER/CONDITION	SYMBOL	NOTES
OPERATING CURRENT: One bank; Active Precharge; t_{RC} (MIN); t_{CK}= t_{CK} (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; Address and control inputs changing once per clock cycle;	IDD0	23
OPERATING CURRENT: One bank; Active Read Precharge; Burst = 8; t_{RC} (MIN); t_{CK} = t_{CK} (MIN); I(OUT) = 0mA; Address and control inputs changing once per clock cycle; CL = CL(min)	IDD1	23
PRECHARGE POWER-DOWN STANDBY CURRENT: All banks idle; Power-down mode; t_{CK} = t_{CK} (MIN); CKE# = HIGH	IDD2P	
IDLE STANDBY CURRENT: CS# = HIGH; All banks idle; t_{CK} = t_{CK} (MIN); CKE# = LOW; inputs changing once per clock cycle	IDD2N	
ACTIVE POWER-DOWN STANDBY CURRENT: One bank active; Power-down mode; t_{CK} = t_{CK} (MIN); CKE# = HIGH	IDD3P	
ACTIVE STANDBY CURRENT: CS# = HIGH; CKE# = LOW; One bank; Active Precharge; t_{RC} = t_{RAS} (MAX); t_{CK} = t_{CK} (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	IDD3N	23
OPERATING CURRENT: Burst = 8; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; t_{CK} = t_{CK} (MIN); Iout = 0mA	IDD4R	
OPERATING CURRENT: Burst = 8; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; t_{CK} = t_{CK} (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; WL = WL(max)	IDD4W	
AUTO REFRESH CURRENT: t_{RC} = t_{RFC}(min); All banks active	IDD5	23
SELF REFRESH CURRENT: CKE# = HIGH	IDD6	
OPERATING CURRENT: Four Bank Interleave; Burst = 8; Reads; Addr/control inputs changing once per clock cycle; t_{CK} = t_{CK} (MIN); DQ, DM, and DQS inputs changing twice per clock cycle; CL=CL(min)	IDD7	

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Table 21 AC TIMINGS

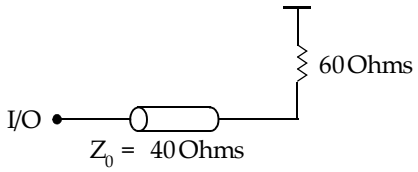
PARAMETER		SYMBOL	MIN	MAX	UNIT	NOTES
Access window of RDQS from CK/CK#		t_{AC}			ns	
		$t_{AC(DLL\ off)}$			ns	
Clock high-level width		t_{CH}			t_{CK}	30
Clock low-level width		t_{CL}			t_{CK}	30
Clock cycle time	DLL on	t_{CK}		2.0	ns	9, 32, 38
	DLL off		6.0	20.0	ns	10, 32, 38
Write Latency		t_{WL}			t_{CK}	41
DQ and DM input setup time		t_{DS}			ns	26, 31
DQ and DM input hold time		t_{DH}			ns	26, 31
Active termination setup time		t_{ATS}				
Active termination setup time		t_{ATH}				
Vendor ID on		t_{WRIDON}	0	30	ns	
Vendor ID off		$t_{WRIDOFF}$	0	30	ns	
WDQS input high-level width		t_{DQSH}			t_{CK}	
WDQS input low-level width		t_{DQSL}			t_{CK}	
RDQS - DQ skew		t_{DQSQ}			ns	26
RDQS output access time from CK/CK#		t_{DQSCK}			ns	
DQ / RDQS output hold time from RDQS		t_{QH}			ns	25, 26
Data hold skew factor		t_{QHS}			ns	25, 26
Write command to 1st WDQS latching transition		t_{DQSS}			t_{CK}	
RDQS falling edge to CK setup time		t_{DSS}			t_{CK}	
RDQS falling edge hold time from CK		t_{DSH}			t_{CK}	
Half strobe period		t_{HP}			ns	33
DQ & RDQS high-impedance time from CK/CK#		t_{HZ}			ns	19
DQ & RDQS low-impedance time from CK/CK#		t_{LZ}			ns	19
Address and control input setup time		t_{IS}			ns	17
Address and control input hold time		t_{IH}			ns	17
Address and control input pulse width		t_{IPW}			ns	42
MODE REGISTER SET command period		t_{MRD}			t_{CK}	
DLL enable to READ command delay		t_{DL}			ns	
ACTIVE to PRECHARGE command period		t_{RAS}			ns	34
ACTIVE to ACTIVE command period		t_{RC}			ns	

Table 21 AC TIMINGS

PARAMETER	SYMBOL			UNIT	NOTES
		MIN	MAX		
AUTO REFRESH command period	t_{RFC}			ns	
REFRESH to REFRESH command interval	t_{REFC}			µs	
Average periodic refresh interval	t_{REFI}			µs	
ACTIVE to READ or WRITE delay	t_{RCDRD}			ns	
	t_{RCDWR}			ns	
PRECHARGE command period	t_{RP}			ns	
RDQS Read preamble	t_{RPRE}			t_{CK}	
RDQS Read postamble	t_{RPST}			t_{CK}	
ACTIVE bank A to ACTIVE bank B delay	t_{RRD}			ns	
Column address to column address delay	t_{CCD}			t_{CK}	
Exit Power-down	t_{PDIX}			t_{CK}	
Write preamble	t_{WPRE}			t_{CK}	21, 22
Write preamble setup time	t_{WPRES}			ns	20, 35
Write postamble	t_{WPST}			t_{CK}	
WRITE recovery time	t_{WR}			ns	
Internal write to Read command delay	t_{WTR}			t_{CK}	
Bank restriction rolling window	t_{FAW}			ns	
Exit Self refresh to non-READ command	t_{XSNR}			t_{CK}	
Exit SELF REFRESH to READ command	t_{XSRD}			t_{CK}	
CKE# min. pulse width (high and low pulse width)	t_{CKE}			t_{CK}	
Auto precharge write recovery + precharge time	t_{DAL}			t_{CK}	

1. All voltages referenced to VSS.
2. Tests for AC timing may be conducted at nominal supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage and temperature range specified.
3. Outputs measured with equivalent load (vendor specific) terminated with 60ohms to VDDQ.

Timing Reference Load



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4. All parameters assume proper device initialization.
5. AC and DC input and output voltage levels are defined in the section for Electrical Characteristics and AC/DC operating conditions.
6. AC timing and Idd tests may use a Vil-to-Vih swing of up to 1.0V in the test environment, but input timing is still referenced to Vref (or to the crossing point for CK/CK#), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 3 V/ns for VDDQ = 1.5V (typ) or 4V/ns for VDDQ = 1.8V (typ) in the range between Vil(AC) and Vih(AC).
7. The AC and DC input level specifications are a pseudo open drain design for improved high-speed signaling.
8. Vref is expected to equal 70 percent of VddQ for the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise on Vref may not exceed ±2 percent of the DC value. Thus, from 70% of VddQ, Vref is allowed ±25mV for DC error and an additional ±25mV for AC noise.
9. GDDR4 SGRAMs are required to support a minimum clock frequency of 500MHz for normal DLL-on operation, regardless of the speed bin of the device.
10. If users need operation below 500MHz, they should use the DLL-off mode of the device.
11. Vid is the magnitude of the difference between the input level on CK and the input level on CK#.
12. The value of Vix is expected to equal 70 percent of VddQ for the transmitting device and must track variations in the DC level of the same.
13. Idd is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time at minimum CAS latency and does not include the on-die termination current. Outputs are open during Idd measurements.
14. Enables on-chip refresh and address counters.
15. Idd specifications are tested after the device is properly initialized.
16. The CK/CK# input reference level (for timing referenced to CK/CK#) is the point at which CK and CK# cross; the input reference level for signals other than CK/CK# is Vref.
17. Command/Address input slew rate = 3 V/ns for VDDQ = 1.5V (typ) and 4 V/ns for VDDQ = 1.8V (typ). If the slew rate is less than 3 V/ns when VDDQ = 1.5V (or 4 V/ns when VDDQ = 1.8V) timing is no longer referenced to the midpoint but to the Vil(AC) maximum and Vih(AC) minimum points.
18. Inputs are not recognized as valid until Vref stabilizes. Exception: during the period before Vref stabilizes, MF, CKE# <= 0.3 x VddQ is recognized as LOW.
19. t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (HZ) or begins driving (LZ).
20. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.
21. This is not a device limit. The device will operate with a negative value, but system performance could be degraded due to bus turnaround.
22. It is recommended that WDQS be valid (HIGH or LOW) on or before the WRITE command.
23. MIN (t_{RC} or t_{RFC}) for Idd measurements is the smallest multiple of t_{CK} that meets the minimum absolute value for the respective parameter. t_{RAS} (MAX) for Idd measurements is the largest multiple of t_{CK} that meets the maximum absolute value for t_{RAS}.
24. The I/O capacitance per DQS and DQ byte/group will not differ by more than this maximum amount for any given device.
25. $t_{QH} = t_{HP} - t_{QHS}$, where t_{HP} = minimum half clock period for any given cycle and is defined by clock high or clock low (t_{CL}, t_{CH}). t_{QHS} accounts for 1) the pulse duration distortion of on-chip clock circuits; and 2) the worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are, separately, due to data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers.
26. Referenced to each output group: RDQS0 with DQ0–DQ7, RDQS1 with DQ8–DQ15, RDQS2 with DQ16–DQ23, and RDQS with DQ24–DQ31.
27. This limit is actually a nominal value and does not result in a fail value. CKE# is LOW during REFRESH command period (t_{RFC} [MIN]) else CKE# is HIGH (e.g., during standby).
28. The DC values define where the input slew rate requirements are imposed, and the input signal must not violate these levels in order to maintain a valid level. The inputs require the AC value to be achieved during signal transition edge, and the driver should achieve the same slew rate through the AC values.
29. The input capacitance per pin group will not differ by more than this maximum amount for any given device.
30. CK and CK# input slew rate must be greater than 3 V/ns for VDDQ = 1.5V (typ) or greater than 4 V/ns for VDDQ = 1.8V (typ).
31. DQ and DM input slew rates must not deviate from WDQS by more than 10 percent. If the DQ/DM/WDQS slew rate is less than 3 V/ns for VDDQ = 1.5V and 4 V/ns for VDDQ = 1.8V, timing is no longer referenced to the midpoint but to the Vil(AC) maximum and Vih(AC) minimum points.
32. The clock is allowed up to ±90ps of jitter. Each timing parameter is allowed to vary by the same amount.

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33. t_{HP} (MIN) is the lesser of t_{DQSL} minimum and t_{DQSH} minimum actually applied to the device CK and CK# inputs, collectively during bank active.
34. For READs and WRITEs with auto precharge the GDDR4 device will hold off the internal PRECHARGE command until t_{RAS} (MIN) has been satisfied.
35. The last rising edge of WDQS after the write postamble must be driven high by the controller. WDQS cannot be pulled high by the on-die termination alone. For the read postamble the GDDR4 will drive the last rising edge of the read postamble.
36. The voltage levels used are derived from the referenced test load. In practice, the voltage levels obtained from a properly terminated bus will provide significantly different voltage values.
37. Vih overshoot: Vih (MAX) = VddQ + 0.5V for a pulse width <= 500ps and the pulse width cannot be greater than 1/3 of the cycle rate. Vil undershoot: Vil (MIN) = 0.0V for a pulse width <= 500ps and the pulse width cannot be greater than 1/3 of the cycle rate.
38. The DLL must be reset when changing the frequency, followed by t_{DL}.
39. Junction temperature is a function of total device power dissipation and device mounting environment. Measured per SEMI G38-87.
40. The thermal resistance data is based on a number of samples from multiple lots and should be viewed as a typical number. These parameters are not tested in production.
41. The WRITE latency can be set from 1 to 7 clocks but can never be less than 2ns for latencies of 1 and 2 clocks. When the WRITE latency is set to small values (i.e. 1, 2,... clocks), the input buffers are always on, reducing the latency but adding power. When the WRITE latency is set to larger values (i.e. ..., 6, 7 clocks) the input buffers are turned on during the WRITE commands for lower power operation and can never be less than 5ns. Vendor specifications should be checked for value(s) of WL supported and the specific value(s) of WL where the input receivers are always on or only turn on when the WRITE command is registered.
42. The t_{IPW} parameter defines the min pulse width for command/address. This is used to tell the input receiver designer the max bandwidth to design to.
43. AC characteristics should be guaranteed for operation up to the maximum operating case temperature (TC_MAX) specified in Table 16.

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1.5V I/O Driver Values

The Driver and Termination impedances are derived from the following test conditions under worst case process corners:

1. Nominal 1.5V (VDD/VDDQ)
2. Power the GDDR4 device and calibrate the output drivers and termination to eliminate process variation at 25 °C.
3. Reduce temperature to 10 °C recalibrate.
4. Reduce temperature to 0 °C and take the fast corner measurement.
5. Raise temperature to 75 °C and recalibrate
6. Raise temperature to 85 °C and take the slow corner measurement
7. Reiterate 2 to 6 with VDD/VDDQ 1.455V
8. Reiterate 2 to 6 with VDD/VDDQ 1.545V
9. All obtained Driver and Termination IV characteristics have to be bounded by the specified MIN and MAX IV characteristics

Table 22 1.5V I/O Impedances

Pull-Down Characteristic at 40 ohms		
Voltage (V)	MIN(mA)	MAX(mA)
0.1	2.25	2.75
0.2	4.50	5.50
0.3	6.75	8.25
0.4	9.00	11.00
0.5	11.25	13.75
0.6	13.50	16.50
0.7	15.75	19.25
0.8	18.00	22.00
0.9	20.25	24.75
1.0	22.50	27.50
1.1	24.75	30.25
1.2	27.00	33.00
1.3	29.25	35.75
1.4	31.50	38.50
1.5	33.75	41.25

Pull-Up/Termination Characteristic at 60 ohms		
Voltage (V)	MIN(mA)	MAX(mA)
0.1	-1.50	-1.83
0.2	-3.00	-3.67
0.3	-4.50	-5.50
0.4	-6.00	-7.33
0.5	-7.50	-9.17
0.6	-9.00	-11.00
0.7	-10.50	-12.83
0.8	-12.00	-14.67
0.9	-13.50	-16.50
1.0	-15.00	-18.33
1.1	-16.50	-20.17
1.2	-18.00	-22.00
1.3	-19.50	-23.83
1.4	-21.00	-25.67
1.5	-22.50	-27.50

Note:
1. These targeted values are for the designer and do not need to meet these values but it is recommended that designs fit these curves.

1.8V I/O Driver Values

The Driver and Termination impedances are derived from the following test conditions under worst case process corners:

1. Nominal 1.8V (VDD/VDDQ)
2. Power the GDDR4 device and calibrate the output drivers and termination to eliminate process variation at 25 °C.
3. Reduce temperature to 10 °C recalibrate.
4. Reduce temperature to 0 °C and take the fast corner measurement.
5. Raise temperature to 75 °C and recalibrate
6. Raise temperature to 85 °C and take the slow corner measurement
7. Reiterate 2 to 6 with VDD/VDDQ 1.710V
8. Reiterate 2 to 6 with VDD/VDDQ 1.890V
9. All obtained Driver and Termination IV characteristics have to be bounded by the specified MIN and MAX IV characteristics

Table 23 1.8V I/O Impedances

Pull-Down Characteristic at 40 ohms		
Voltage (V)	MIN(mA)	MAX(mA)
0.1	2.25	2.75
0.2	4.50	5.50
0.3	6.75	8.25
0.4	9.00	11.00
0.5	11.25	13.75
0.6	13.50	16.50
0.7	15.75	19.25
0.8	18.00	22.00
0.9	20.25	24.75
1.0	22.50	27.50
1.1	24.75	30.25
1.2	27.00	33.00
1.3	29.25	35.75
1.4	31.50	38.50
1.5	33.75	41.25
1.6	36.00	44.00
1.7	38.25	46.75
1.8	40.50	49.50

Pull-Up/Termination Characteristic at 60 ohms		
Voltage (V)	MIN(mA)	MAX(mA)
0.1	-1.50	-1.83
0.2	-3.00	-3.67
0.3	-4.50	-5.50
0.4	-6.00	-7.33
0.5	-7.50	-9.17
0.6	-9.00	-11.00
0.7	-10.50	-12.83
0.8	-12.00	-14.67
0.9	-13.50	-16.50
1.0	-15.00	-18.33
1.1	-16.50	-20.17
1.2	-18.00	-22.00
1.3	-19.50	-23.83
1.4	-21.00	-25.67
1.5	-22.50	-27.50
1.6	-24.00	-29.34
1.7	-25.50	-31.17
1.8	-27.00	-33.00

Note: These values are target values for the design. The design does not need to meet these values but it is recommended that the design fits these curves.

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POD I/O SYSTEM

The POD I/O system is optimized for small systems with data rates exceeding 2.0 Gbps. The system allows a single Master device to control one, two or four slave devices. The POD driver uses a 40 Ohm output impedance that drives into a 60 Ohm equivalent terminator tied to VDDQ. Single, dual and quad load systems are shown as follows:

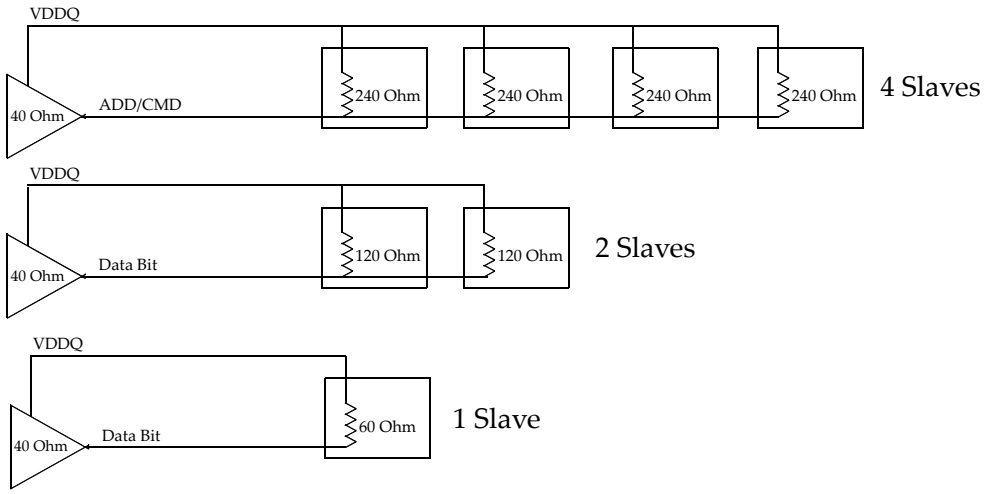

Figure 41: System Configurations

The POD Master I/O cell is comprised of a 40 Ohm driver and a terminator of 60 Ohms. The Master POD cell's terminator is disabled when the output driver is enabled. The basic cell is shown in Figure 42.

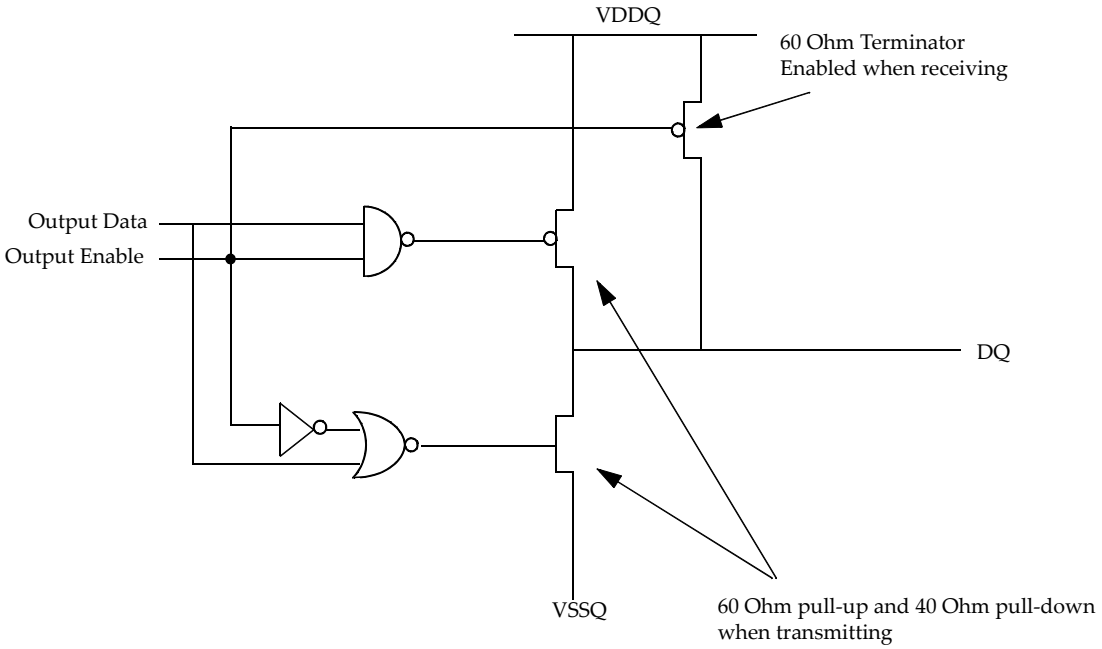

Figure 42: Master I/O Cell

The POD Slave I/O cell is comprised of a 40 ohm driver and programmable terminator of 60, 120 or 240 ohms. The Slave POD cell's terminator is disabled when the output driver is enabled or any other Slave output driver is enabled. The basic cell is shown in Figure 43.

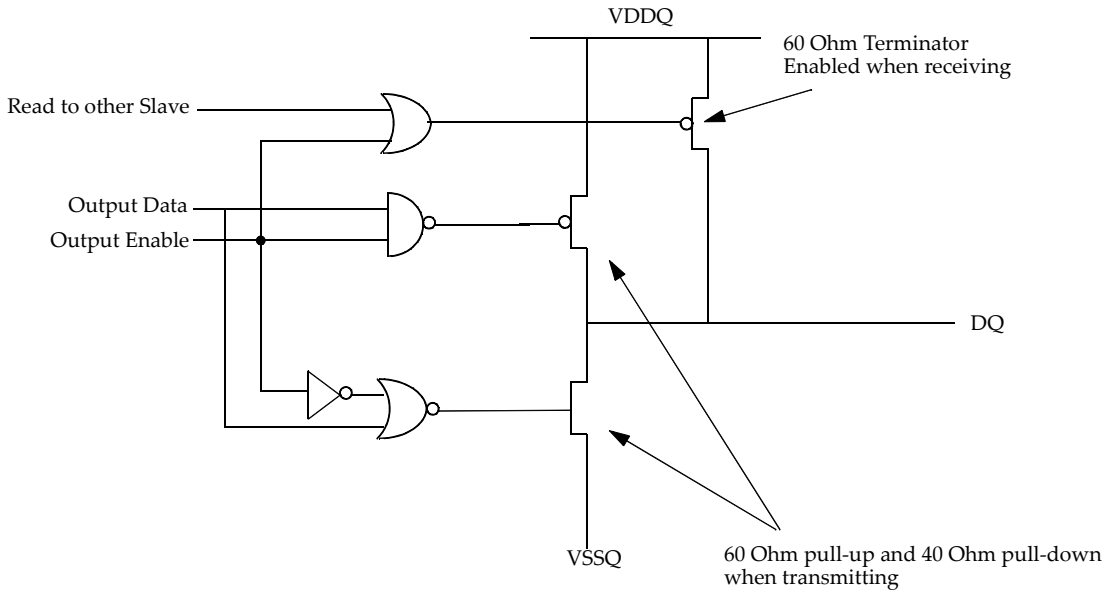

Figure 43: Slave I/O Cell

The POD Master and Slave I/O cells are intended to have their driver and terminators combined together to minimize the area needed to implement the cell and reduce input capacitance. This is possible by using six 240 Ohm driver/terminator sub cells that are connected in parallel. The combinations used are as follows.

Table 24 POD I/O Sub Cells

# of 240 ohm Sub Cells Enabled	Resulting Impedance	Use
1	240 Ohms	4 Slave loads
2	120 Ohms	2 Slave loads
4	60 Ohms	1 Slave load or Master driver or terminator
6	40 Ohms	Master or Slave Driver

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To ensure that the target impedance is achieved the POD I/O cell is designed to be calibrated to an external 1% precision resistor.

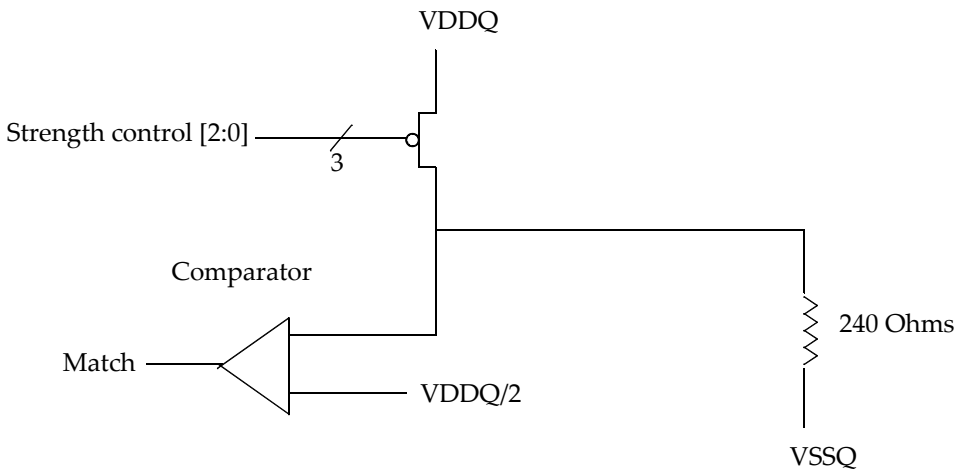
The following procedure may be used to calibrate the cell:

1.) First calibrate the PMOS device against a 240 Ohm resister to VSS via the ZQ pin as illustrated in Figure 44.

- Set Strength Control to minimum setting
- Increase drive strength until comparator detects data bit is greater than VDDQ/2
- PMOS device is calibrated to 240 Ohms

2.) Then calibrate the NMOS device against the calibrated 240 Ohm PMOS device as illustrate in Figure 45

- Set Strength Control to minimum setting
- Increase drive strength until comparator detects data bit is less than VDDQ/2
- NMOS device is now calibrated to 240 Ohms



When Match PMOS leg is calibrated to 240 ohms

Figure 44: PMOS Calibration

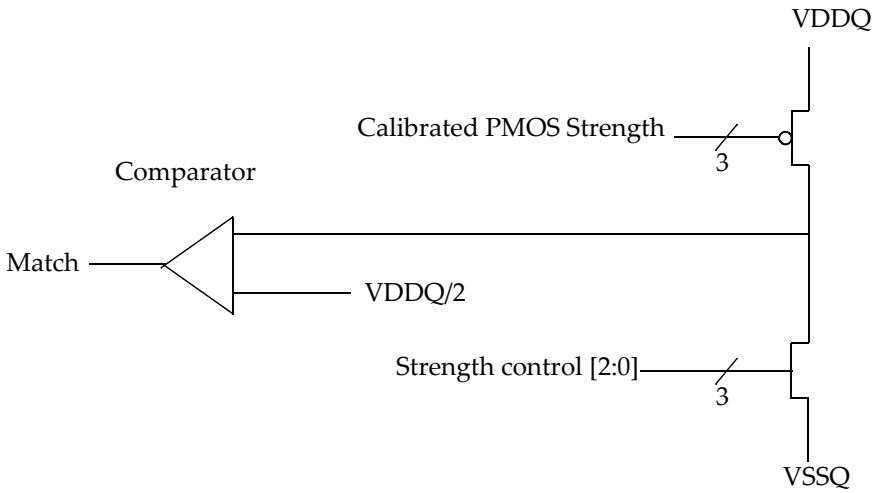


Figure 45: NMOS Calibration

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PACKAGE SPECIFICATION

Ball-out

1	2	3	4	5	6	7	8	9	10	11	12
V_{DDQ}	V_{DD}	V_{SS}	ZQ			A		MF	V_{SS}	V_{DD}	V_{DDQ}
V_{SSQ}	DQ0	DQ1	V_{SSQ}			B		V_{SSQ}	DQ9	DQ8	V_{SSQ}
V_{DDQ}	DQ2	DQ3	V_{DDQ}			C		V_{DDQ}	DQ11	DQ10	V_{DDQ}
V_{SSQ}	WDQS0	RDQS0	V_{SSQ}			D		V_{SSQ}	RDQS1	WDQS1	V_{SSQ}
V_{DDQ}	DQ4	DM0	V_{DDQ}			E		V_{DDQ}	DM1	DQ12	V_{DDQ}
V_{DD}	DQ6	DQ5	V_{SSQ}			F		V_{SSQ}	DQ13	DQ14	V_{DD}
V_{SS}	V_{SSQ}	DQ7	CAS#			G		CS#	DQ15	V_{SSQ}	V_{SS}
V_{DDQ}	RAS#	CKE#	BA0 A1			H		BA1 A5	WE#	RFM	V_{DDQ}
V_{SS}	RFU	PERR#	VREFC			J		VREFD / NC	CK#	CK	V_{SS}
V_{DD}	A10 A0	A12 A2	V_{SS}			K		V_{SS}	BA2 A6	A8 A4	V_{DD}
V_{SS}	V_{SSQ}	DQ25	A11 A3			L		A9 A7	DQ17	V_{SSQ}	V_{SS}
V_{DD}	DQ24	DQ27	V_{SSQ}			M		V_{SSQ}	DQ19	DQ16	V_{DD}
V_{DDQ}	DQ26	DM3	V_{DDQ}			N		V_{DDQ}	DM2	DQ18	V_{DDQ}
V_{SSQ}	WDQS3	RDQS3	V_{SSQ}			P		V_{SSQ}	RDQS2	WDQS2	V_{SSQ}
V_{DDQ}	DQ28	DQ29	V_{DDQ}			R		V_{DDQ}	DQ21	DQ20	V_{DDQ}
V_{SSQ}	DQ30	DQ31	V_{SSQ}			T		V_{SSQ}	DQ23	DQ22	V_{SSQ}
V_{DDQ}	V_{DD}	V_{SS}	SEN			V		RESET	V_{SS}	V_{DD}	V_{DDQ}

GDDR4 SGRAM x33 Ballout Using MO-207
(Variation DR-2 with Note 22 Applied)

Note: Top View, MF = LOW

Signals

Table 25 Ball-out Description

FBGA BALL-OUT	SYMBOL	TYPE	DESCRIPTION
J10, J11	CK, CK#	Input	Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#.
H3	CKE#	Input	Clock Enable: CKE# LOW activates and CKE# HIGH deactivates the internal clock, input buffers, and output drivers. Taking CKE# HIGH provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any bank). CKE# is synchronous for POWER-DOWN entry and exit, and for SELF REFRESH entry. CKE# is asynchronous for SELF REFRESH exit and for disabling the outputs. CKE# must be maintained LOW throughout read and write accesses. Input buffers (excluding CK, CK#, and CKE#) are disabled during POWER- DOWN. Input buffers (excluding CKE#) are disabled during SELF REFRESH.
G9	CS#	Input	Chip Select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
H2, G4, H10	RAS#, CAS#,WE#	Input	Command Inputs: RAS#, CAS#, and WE# (along with CS#) define the command being entered.
E(3, 10), N(3,10)	DM0–DM3	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on the rising and falling edges of WDQS. DM is used as the flag for READ DBI
Multiplexed with Address H(4, 9), K10	BA0–BA2	Input	Bank Address Inputs: BA0, BA1 and BA2 define to which bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
Multiplexed with Bank Address H(4, 9), K10 Multiplexed with other address K(2, 3, 11), L(4, 9)	A0–A12	Input	Address Inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A8) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A8 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A8 LOW, bank selected by BA0-BA2) or all banks (A8 HIGH). The address inputs also provide the op-code during a MODE REGISTER SET command. BA0-BA2 define which mode register (mode register or specific extended mode register) is loaded during the MODE REGISTER SET command.
B(2, 3), C(2, 3), E2, F(2, 3), G3	DQ0–7	I/O	Data Input/Output
B(10, 11), C(10, 11), E11, F(10,11), G10	DQ8–15	I/O	Data Input/Output
L10, M(10, 11), N11, R(10, 11), T(10, 11)	DQ16–23	I/O	Data Input/Output

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Table 25 Ball-out Description

FBGA BALL-OUT	SYMBOL	TYPE	DESCRIPTION
L3, M(2, 3) N2, R(2, 3), T(2, 3)	DQ24–31	I/O	Data Input/Output
D(3, 10), P(3, 10)	RDQS(0–3)	Output	READ Data Strobe: Output with read data. RDQS is edge-aligned with read data. RDQS is used as the flag for WRITE DBI.
D(2, 11), P(2, 11)	WDQS(0–3)	Input	WRITE Data strobe: Input with write data. WDQS is center-aligned to the input data.
J2	RFU		Reserved for Future Use
A(1, 12), C(1, 4, 9, 12), (E1, 4, 9, 12), H(1,9), N(1, 4, 9, 12), R(1, 4, 9, 12), V(1, 12)	VddQ	Supply	DQ Power Supply: +1.5V ±0.045V or +1.8V ±0.09V. Isolated on the die for improved noise immunity.
B(1, 4, 9, 12), D(1, 4, 9, 12), F(4,9), G(2, 11), L(2, 11), M(4,9), P(1, 4, 9, 12), T(1, 4, 9, 12)	VssQ	Supply	DQ Ground: Isolated on the die for improved noise immunity.
A(2, 11), F(1, 12), K(1, 12) M(1, 12), V(2,11)	Vdd	Supply	Power Supply: +1.5V ±0.045V or +1.8V ±0.09V
A(3, 10), G(1, 12), J(1, 12), K(4, 9), L(1,12), V(3,10)	Vss	Supply	Ground.
J(4, 9)	Vref	Supply	Reference Voltage.
J3	PERR#	Output	Parity error
A9	MF	Reference	Mirror Function for clamshell mounting of DRAMs
H11	RFM		When the MF ball is tied LOW, RFM receiver is disabled and it recommended to be driven to a static LOW state. However, either static HIGH or floating state on this pin will not cause any problem for the GDDR4 SGRAM. When the MF ball is tied HIGH, RAS(H2) becomes RFM due to mirror function and the receiver is disabled. It is recommended to be driven to a static LOW state. However, either static HIGH or floating state on this pin will not cause any problem. for the GDDR4 SGRAM
A4	ZQ	Reference	External Reference Pin for autocalibration
V4	SEN	Input	Scan enable. Must tie to the ground when not in use.
V9	RESET	Input	Reset Pin. The RESET pin is a VDDQ CMOS input.

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Mirror Function

The GDDR4 SGRAM provides a mirror function (MF) ball to change the physical location of the control lines and all address lines assisting in routing devices back to back. The MF ball will affect RAS#, CAS#, WE#, CS# ,CKE#, A0, A1, A2, A3, A4, A5, A6, A7, A8, A9, A10, A11, A12, BA0, BA1 and BA2, and only detects a DC input. The MF ball should be tied directly to VSS or VDD depending on the control line orientation desired.

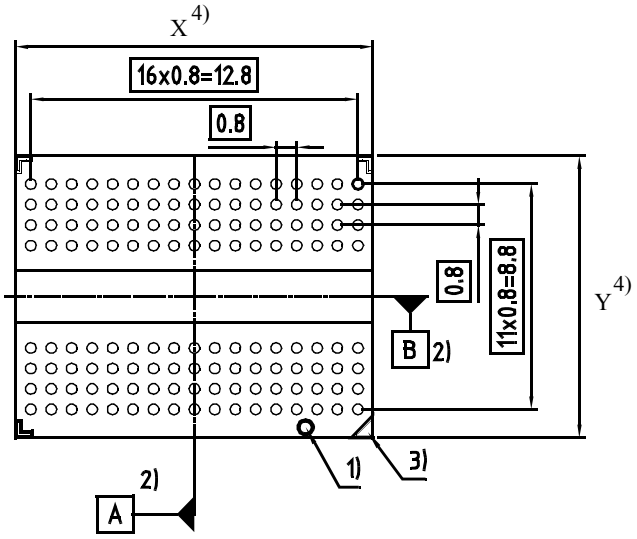
Table 26 illustrates the pin location in relation to the polarity of the MF pin. The MF pin may not transition under/during normal operation. MF can only transition when either the RESET or SEN pins are asserted.

Table 26 Mirror Function Signal Mapping

PIN	MF LOGIC STATE	
	LOW	HIGH
RAS#	H2	H11
CAS#	G4	G9
WE#	H10	H3
CS#	G9	G4
CKE#	H3	H10
A0/A10	K2	K11
A1/BA0	H4	H9
A2/A12	K3	K10
A3/A11	L4	L9
A4/A8	K11	K2
A5/BA1	H9	H4
A6/BA2	K10	K3
A7/A9	L9	L4

Package Dimensions

Figure 46: X-Y Dimensions



1) Bad Unit Marking (BUM) - position and shape preliminary
2) Middle of Package
3) Package Orientation Mark A1
4) X and Y are vendor specific

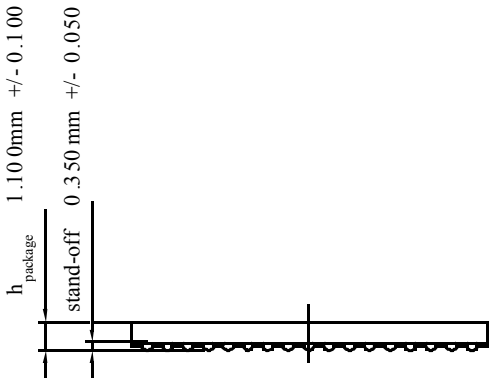


Figure 47: Package Height

Table 27 Package Height Parameter

	Nominal	Variation
hpackage	1.100 mm	+/- 0.100 mm
stand-off	0.350 mm	+/- 0.050 mm

Note 1) The GDDR4 package height specification is compliant to MO-207, DR-2 applying Note 22.

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VENDOR ID, PARITY & SCAN

Vendor ID

The Manufacturers Vendor ID Code, V, is selected by issuing a MODE REGISTER SET command to EMRS (1) with bit A11 set to 1, and bits A0-A10 and A12 set to the desired values. The DRAM Info command of EXTENDED MODE REGISTER SET 3 must also be set to Vendor ID by setting bits A6 and A7 to 0. When the Vendor ID function is enabled the GDDR4 SGRAM will provide its manufacturers vendor ID code on DQ[3:0] and revision identification on DQ[7:4]. The code will be driven onto the DQ bus after the EMRS that set A11 to 1. The DQ bus will be continuously driven until an EMRS write sets A11 back to 0. The DQ bus will be in a Hi-Z state after $t_{WRIDOFF}$ max. The code can be sampled by the controller after waiting t_{WRIDON} max and before $t_{WRIDOFF}$ min.

Table 28 Vendor IDs

VENDOR	DQ(3:0)
Reserved	0
Samsung	1
Infineon	2
Elpida	3
Etron	4
Nanya	5
Hynix	6
Mosel	7
Winbond	8
ESMT	9
Reserved	A
Reserved	B
Reserved	C
Reserved	D
Reserved	E
Micron	F

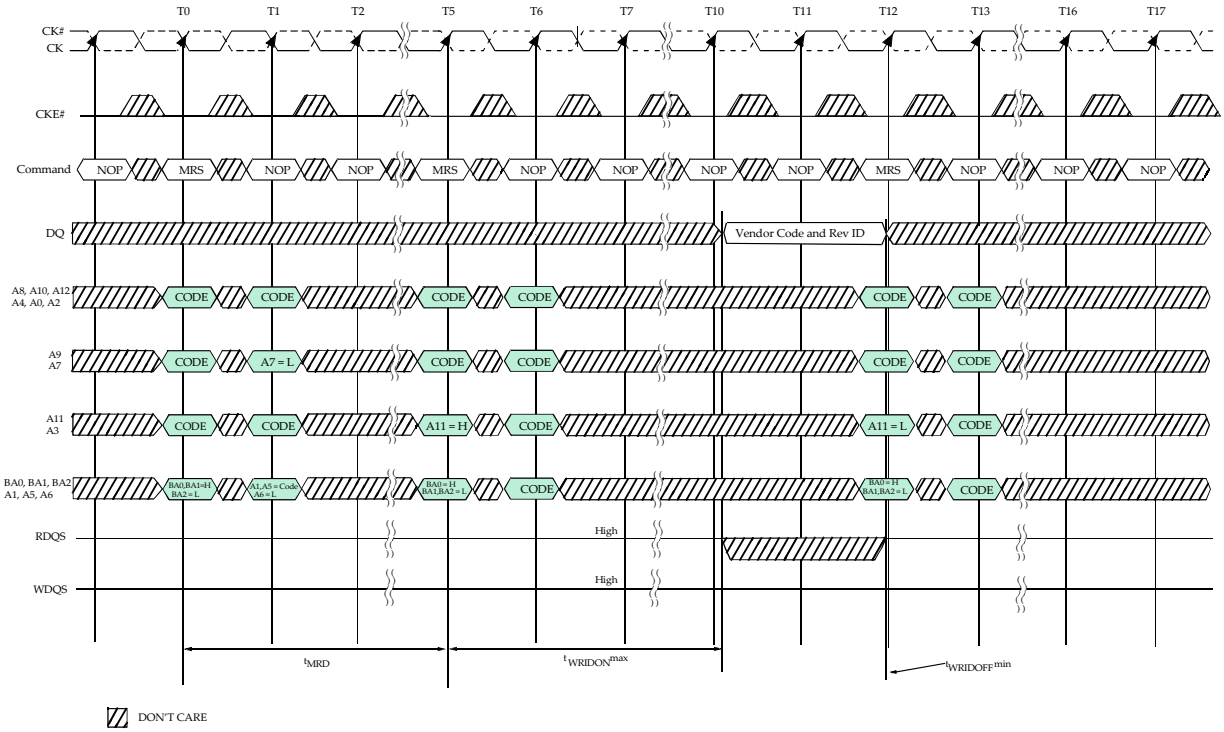

Figure 48: Vendor ID Timing

Note
1. Address is received on two consecutive rising edges of CK

Parity

GDDR4 SGRAM adds an optional parity feature that allows the controller to determine when the DRAM receivers are not capturing the intended data. This feature is available during normal operation and can be used to identify failures and help isolate problems during system validation and failure analysis.

Control of the parity feature is accomplished through the following mode register fields:

Table 29 Parity Mode

	PARITY
0	Disabled
1	Enabled

Table 30 Parity Mask

	PMASK
00	DQ[7:0]
01	DQ[15:9]
10	DQ[23:16]
11	DQ[31:24]

Table 31 Parity Reset

	PRST
0	Store
1	Clear

The Parity feature is enabled when PARITY is set to the Enabled value. When PARITY is set to Disabled, the feature is not available. Devices not supporting this feature will only support the Disabled mode. When PARITY is enabled, the PMASK field selects which byte group the GDDR4 SGRAM will check for EVEN PARITY. To support identification of the bits that failed, the GDDR4 SGRAM stores the value received on DQ[31:0] in a register called PERR_INFO at the time of the first failure. The controller can read back this information on the DQ pins using the same data path defined for accessing the Vendor ID of the GDDR4 SGRAM. Setting PRST to Clear resets the logic that looks for the first error to store in the PERR_INFO register. When PRST is set to store the PERR_INFO register maintains its first captured error information. It is not necessary to set the PRST field back to the Store setting after selecting the Clear state. This field self resets back to the Store value after a Clear is recognized by the GDDR4 SGRAM, i.e. self clearing.

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Table 32 DRAM Information

	INFO
00	Vendor ID
01	PERR_INFO
10	Reserved
11	Reserved

Calculating Even Parity

When PARITY is set to Enabled, the controller is required to send EVEN parity data to the GDDR4 SGRAM for the byte selected by the PMASK setting during WRITE cycles. The GDDR4 SGRAM calculates parity for each DQ in the selected byte by computing the bit-wise XOR of these 8 bits and if ODD parity is detected will drive the PERR# pin to a LOW state t_{PD} later. The timing of t_{PD} is vendor specific.

Example:

PARITY = enabled
PMASK = DQ{7:0]
PERR# = DQ[7] xor DQ[6] xor DQ[5] xor DQ[4] xor DQ[3] xor DQ[2] xor DQ[1] xor DQ[0]

Figure 49 shows the timing diagram for the Parity feature. Refer to WRITE timing figures for more detailed signaling requirements. In this example, parity errors were detected for bit times d0, d2, d4, and d6. If PRST was cleared prior to this bit stream, then PERR_INFO would have stored the value of the DQ bus at bit time d0.

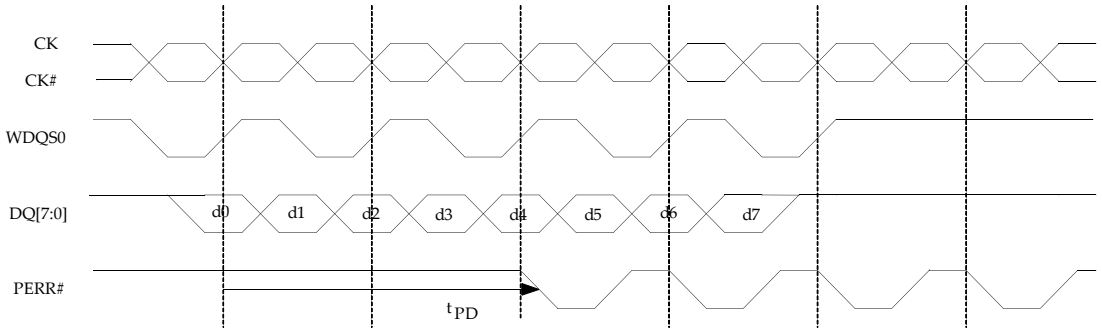

Figure 49: Parity Timing

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Boundary Scan

The GDDR4 incorporates a modified boundary scan test mode as an optional feature. This mode doesn't operate in accordance with IEEE Standard 1149.1-1990. To save the current GDDR4 ball-out, this mode will scan the parallel data input and output the scanned data through WDQS0 pin controlled by an add-on pin, SEN which is located at V-4 of 136 ball package. For normal device operation, i.e. other than boundary scan, it is required that device re-initialization occur through device power-off and then power-on.

Disabling the scan feature

It is possible to operate the GDDR4 without using the boundary scan feature. SEN (at V-4 of 136-ball package) should be tied LOW(VSS) to prevent the device from entering the boundary scan mode. The other pins which are used for scan mode, RESET, MF, WDQS0 and CS# will be operating as normal when SEN is deasserted.

Figure 50: Internal Block Diagram (Reference Only)

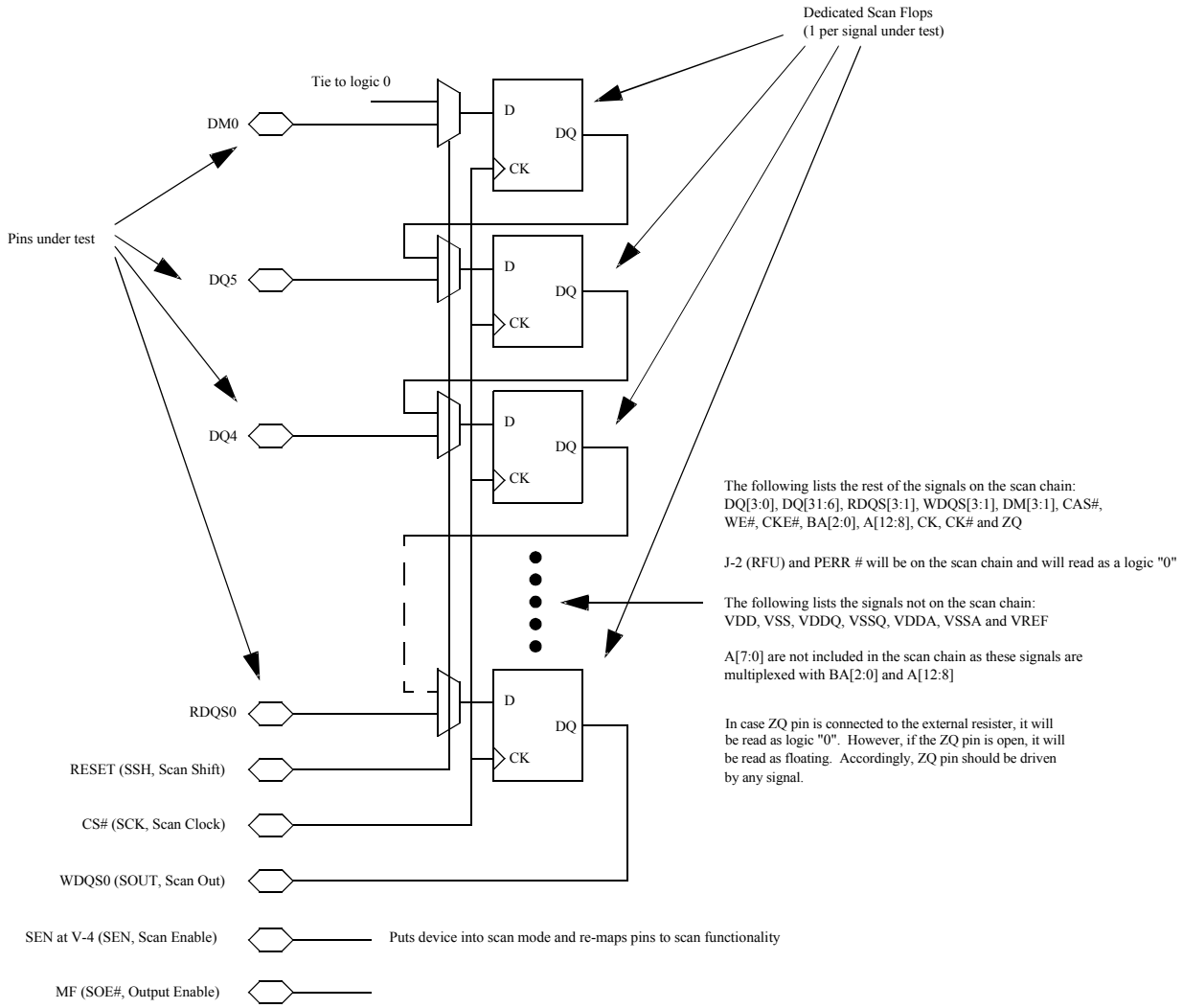

Table 33 Boundary Scan Exit Order

BIT#	BALL	BIT#	BALL	BIT#	BALL	BIT#	BALL	BIT#	BALL	BIT#	BALL
1	D-3	13	E-10	25	K-10	37	T-3	49	K-2	61	E-3
2	C-2	14	F-10	26	M-11	38	T-2	50	L-4		
3	C-3	15	E-11	27	L-10	39	R-3	51	J-3		
4	B-2	16	G-10	28	N-11	40	R-2	52	J-2		
5	B-3	17	F-11	29	M-10	41	P-3	53	H-2		
6	A-4	18	H-9	30	N-10	42	P-2	54	H-3		
7	B-10	19	H-10	31	P-11	43	N-3	55	H-4		
8	B-11	20	H-11	32	P-10	44	M-3	56	G-4		
9	C-10	21	J-11	33	R-11	45	N-2	57	F-2		
10	C-11	22	J-10	34	R-10	46	L-3	58	G-3		
11	D-10	23	L-9	35	T-11	47	M-2	59	E-2		
12	D-11	24	K-11	36	T-10	48	K-3	60	F-3		

Note:
1. When the device is in scan mode, mirror function is disabled and none of the pins are remapped
2. Since the other input of the MUX for DM0 is tied to GND, the device will continuously output zeros after scanning bit# 61, if the chip stays in scan shift mode.

Table 34 Scan Pin Description

PACKAGE BALL	SYMBOL	NORMAL FUNCTION	TYPE	DESCRIPTION
V-9	SSH	RESET	Input	Scan Shift. Capture the data input from the pad at logic LOW and shift the data on the chain at logic HIGH.
F-9	SCK	CS#	Input	Scan Clock. Not a true clock, could be a single pulse or series of pulses. All scan inputs will be referenced to rising edge of the scan clock.
D-2	SOUT	WDQS0	Output	Scan Output.
V-4	SEN	RFU	Input	Scan Enable. Logic HIGH enables scan mode. Scan mode is disabled at logic LOW. Must be tied to GND when not in use.
A-9	SOE#	MF	Input	Scan Output Enable. Enables (registered LOW) and disables (registered HIGH) SOUT data. This pin will be tied to VDD or GND through a resistor (typically 1KW) for normal operation. Tester needs to overdrive this pin to guarantee the required input logic level in scan mode.

Note :
1. When SEN is asserted, no commands are to be executed by the GDDR4. This applies to both user commands and manufacturing commands which may exist while RESET is deasserted.
2. All scan functionality is valid only after the appropriate power-up and initialization sequence. (CKE# and A0 to set the ODT of the C/A)
3. In scan mode, the ODT for the address and control lines set to a nominal termination value of ZQ. The ODT for DQ's will be disabled. It is not necessary for the termination to be calibrated.
4. In a double-load clam-shell configuration, SEN will be asserted to both devices. Two separate SOE#'s should be provided to the top and bottom devices to access the scanned output. When either of the devices is in scan mode, SOE# for the device not being scanned will be disabled.

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Table 35 Scan DC Electrical Characteristics and Operating Conditions

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage	VIH(DC)	VREF+0.15	-	V	1, 2
Input Low (Logic 0) Voltage	VIL(DC)	-	VREF-0.15	V	1, 2

Note:
1. The parameter applies only when SEN is asserted.
2. All voltages referenced to GND.

Figure 51: Scan Capture Timing

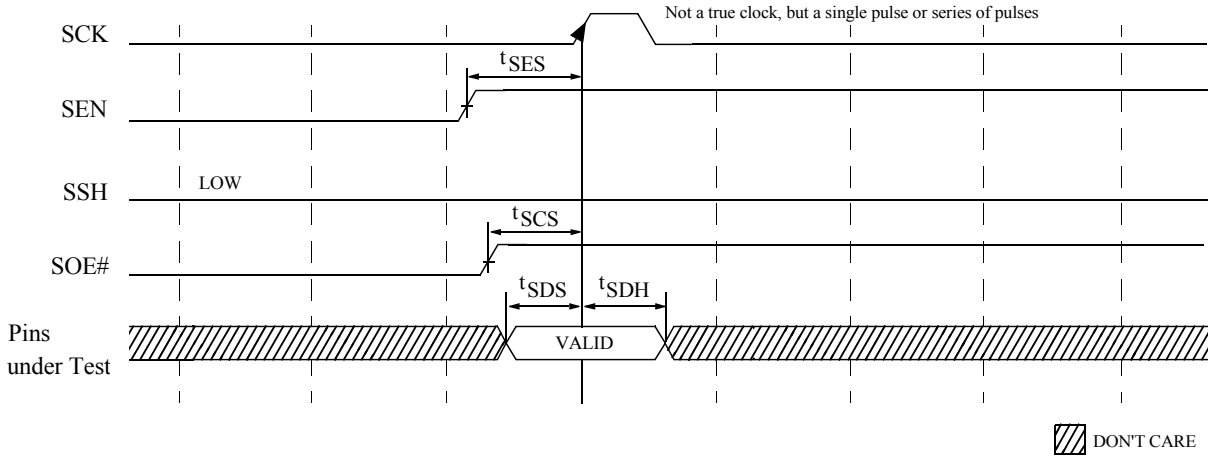


Figure 52: Scan Shift Timing

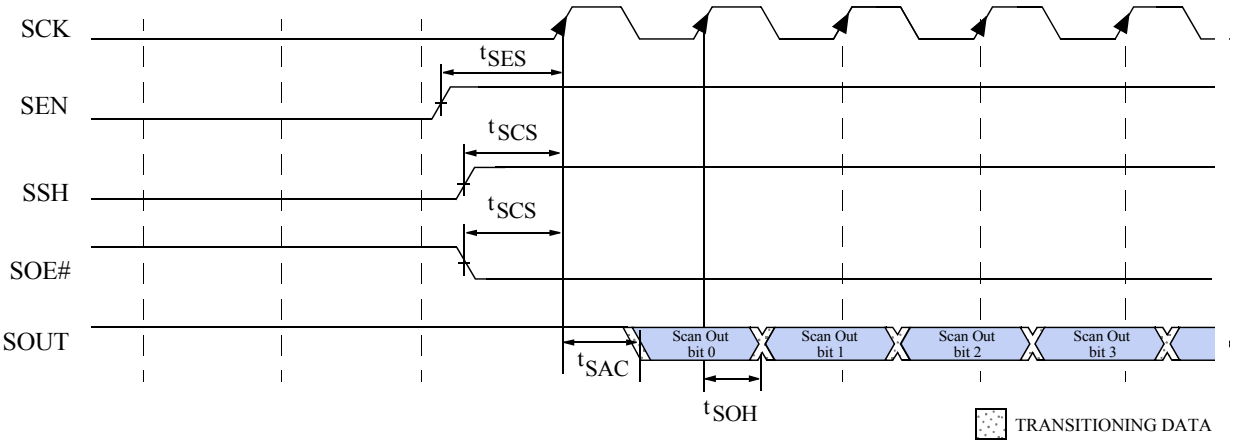
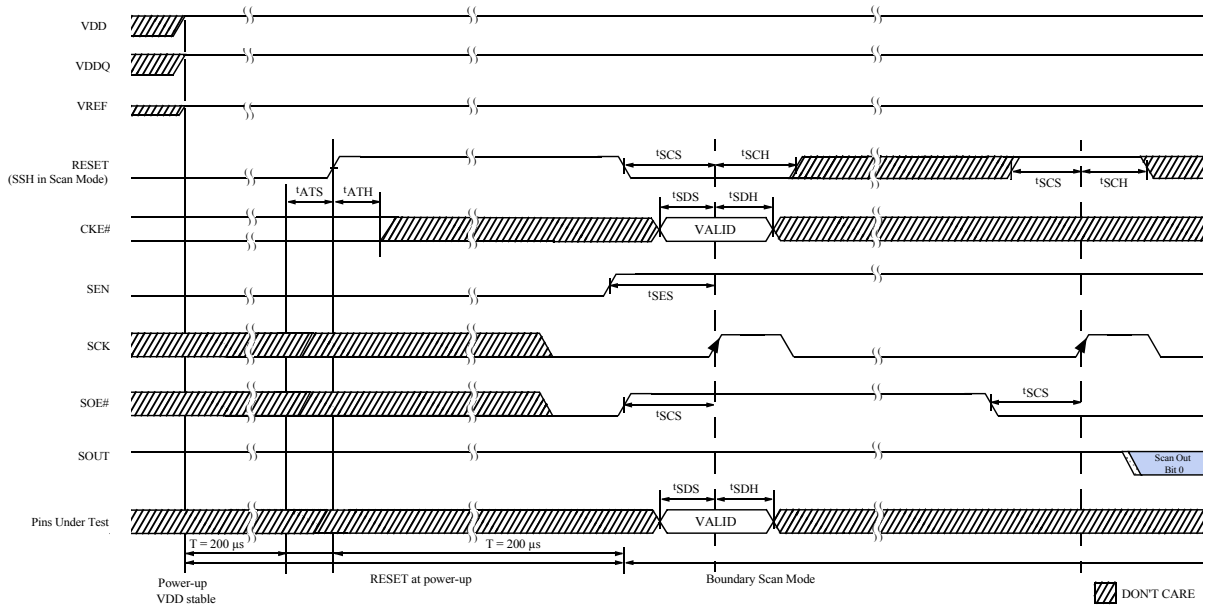


Table 36 Scan AC Electrical Characteristics

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Clock					
Clock cycle time	t_{SCK}	40	-	ns	1
Scan Command Time					
Scan enable setup time	t_{SES}	20	-	ns	1, 2
Scan enable hold time	t_{SEH}	20	-	ns	1
Scan command setup time for SSH, SOE# and SOUT	t_{SCS}	14	-	ns	1
Scan command hold time for SSH, SOE# and SOUT	t_{SCH}	14	-	ns	1
Scan Capture Time					
Scan capture setup time	t_{SDS}	10	-	ns	1
Scan capture hold time	t_{SDH}	10	-	ns	1
Scan Shift Time					
Scan clock to valid scan output	t_{SAC}	-	6	ns	1
Scan clock to scan output hold	t_{SOH}	1.5	-	ns	1

Note:
1. The parameter applies only when SEN is asserted.
2. Scan Enable should be issued earlier than other scan commands by 6ns.

Figure 53: Scan Initialization Sequence



Note : To set the pre-defined ODT for C/A, a boundary scan mode should be issued after an appropriate ODT initialization sequence with A0 and CKE# signals