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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NETL.071C3
	Application Number	
Title of Invention	MEMORY MODULE WITH PACKAGES OF STACKED MEMORY CHIPS	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
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Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Hyun		Lee	

Residence Information (Select One) ● US Residency Non US Residency Active US Military Service

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All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

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Customer Number	79141		
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Application Information:

Title of the Invention	MEMORY MODULE WITH PACKAGES OF STACKED MEMORY CHIPS		
Attorney Docket Number	NETL.071C3	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	8	Suggested Figure for Publication (if any)	

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Filing By Reference :

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

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☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

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When referring to the current application, please leave the application number blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Continuation of	15095288	2016-04-11
Prior Application Status	Patented		Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15095288	Continuation of	14337168	2014-07-21	9318160	2016-04-19

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Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14337168	Continuation of	13288850	2011-11-03	8787060	2014-07-22
Prior Application Status	Expired				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)		
13288850	Claims benefit of provisional	61409893	2010-11-03		
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This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

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Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)

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Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Authorization to Permit Access:

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If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application.

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application.

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Applicant 1 Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

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If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor :

If the Applicant is an Organization check here. ☒

Organization Name	Netlist, Inc.

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Title of Invention	MEMORY MODULE WITH PACKAGES OF STACKED MEMORY CHIPS	

Mailing Address Information For Applicant:

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Country i	US	Postal Code	92618
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Email Address			

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Signature	/Jamie J. Zheng/			Date (YYYY-MM-DD)	2017-05-22
First Name	Jamie	Last Name	Zheng	Registration Number	51167

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3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

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MEMORY MODULE WITH PACKAGES OF STACKED MEMORY CHIPS

RELATED APPLICATION

[0001] This application is a continuation application of U.S. Pat. App. No. 15/095,288, filed April 11, 2016, to be issued as U.S. Pat. No. 9,659,601 on May 23, 2017, which is a continuation of U.S. Pat. App. No. 14/337,168, filed July 21, 2014, now U.S. Pat. No. 9,318,160, which is a continuation of U.S. Pat. App. No. 13/288,850, filed November 3, 2011, now U.S. Pat. No. 8,787,060, which claims the benefit of priority under 35 U.S.C. § 119(e) of U.S. Provisional Patent Application No. 61/409,893, filed November 03, 2010, and entitled "ARCHITECTURE FOR MEMORY MODULE WITH PACKAGES OF THREE-DIMENSIONAL STACKED (3DS) MEMORY CHIPS." The disclosure of each of the above applications is hereby incorporated by reference in its entirety.

BACKGROUND

Technical Field

[0002] The present disclosure relates to memory devices and memory modules. More specifically, the present disclosure relates to systems and methods for reducing the load of drivers of memory packages included on the memory modules.

Description of the Related Art

[0003] Memory modules may include a number of memory packages. Each memory package may itself include a number of array dies that are packaged together. Each array die may include an individual semiconductor chip that includes a number of memory cells. The memory cell may serve as the basic building block of computer storage representing a single bit of data.

[0004] FIGS. 1A and 1B schematically illustrate examples of existing memory package designs currently used or proposed to be used to provide the dynamic random-access memory of memory modules. FIG. 1A schematically illustrates a memory package 100 with three array dies 110 and a control die 130. The control die 130 is configured to

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respond to signals received by the memory package 100 by sending appropriate control signals to the array dies 110 and includes a driver 134 for driving data signals to each of the array dies 110 via a corresponding die interconnect 120. Further, the control die 130 includes a driver 140 for driving command and/or address signals to each of the array dies 110 via another corresponding die interconnect 142. For simplicity, FIG. 1A shows only a single driver 134, die interconnect 120, driver 140, and die interconnect 142. However, additional drivers and die interconnects may be included for each bit the memory package 100 is designed to support. Thus, a 16-bit memory may include 16 pairs of drivers and die interconnects for the data signals and other similar drivers and die interconnects for the command and/or address signals. Each array die 110 also includes a chip select port 144, with the chip select ports 144 of the array dies 110 configured to receive corresponding chip select signals to enable or select the array dies for data transfer. The array dies 110 are configured to transfer data (e.g. read or write) to or from the selected memory cells identified by the command, address, and chip select signals via the die interconnects.

[0005] In some cases, the control die 130 may include memory cells and therefore, also serve as an array die. Thus, as can be seen from FIG. 1A, the control die 130 may also include a chip select port 144. Alternatively, the control die 130 and the array dies 110 may be distinct elements and the control die 130 may not include any memory cells.

[0006] FIG. 1B schematically illustrates an example of a memory package 150 that includes four array dies 160 and a control die 170 that does not include memory cells. As can be seen in FIG. 1B, each array die 160 includes a chip select port 174. However, because the control die 170 does not also serve as an array die, the control die 170 does not include a chip select port. As with memory package 100, memory package 150 includes a driver 184 that drives data signals to each of the array dies 160 along a corresponding die interconnect 182. Further, the memory package 150 includes a driver 186 for driving command and/or address signals to each of the array dies 160 via another die interconnect 188.

[0007] Generally, a load exists on each of the drivers 134, 140, 184, and 186 by virtue of

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the drivers being in electrical communication with the corresponding die interconnects and the corresponding circuitry of the array dies. Thus, to drive a signal along a die interconnect, a driver typically must be large enough to overcome the load on the driver. However, generally a larger driver not only consumes more space on the control die, but also consumes more power.

SUMMARY

[0008] In certain embodiments, a memory module is operable in a computer system to communicate with a system memory controller via a command/address bus and a data bus. The memory module comprises a register device coupled to the command/address bus, and a plurality of DRAM packages coupled to the data bus and to the register device via a set of module control lines. Each respective DRAM package comprises stacked array dies and a control die. The control die includes data signal conduits and control signal conduits. In response to the memory module receiving a set of command/address signals from the system memory controller, the register device outputs control signals, and the control die configures the data signal conduits in accordance with the control signals to enable respective bits of one or more data signals to be communicated between a selected die among the stacked dies and the system memory controller.

[0009] In certain embodiments, the register device receives command/address signals from the system memory controller via the command/address bus and outputs the control signals in response to the input command/address signals. The each respective DRAM package further comprises control terminals coupled to the module control lines via which the each respective DRAM package receives the control signals from the register device, and data terminals coupled to a respective section of the data bus via which the each respective DRAM package communicates with the system memory controller the respective bits of the one or more data signals associated with the command/address signals.

[0010] In certain embodiments, the each respective DRAM package further comprises die interconnects including first die interconnects coupled to the data signal conduits and second die interconnects coupled to the control signal conduits, at least one of the first die

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interconnects is coupled to at least two of the stacked array dies. In certain embodiments, the control signals include chip-select signals, and the control signal conduits include chip-select conduits for receiving the chip select signals and providing respective ones of the chip select signals to respective ones of the stacked array dies. The selected array die receives one of the chip select signals that is different from any of the other ones of the chip select signals.

[0011] In certain embodiments, the control die configures the data signal conduits to control data bus time slots for the respective bits of the one or more data signals. In certain embodiments, the control signals include command/address signals, and the control die includes command/address buffers to control the timing of the command/address signals in the control signals.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] Throughout the drawings, reference numbers are re-used to indicate correspondence between referenced elements. The drawings are provided to illustrate certain example embodiments of the inventive subject matter described herein and not to limit the scope thereof.

[0013] FIGS. 1A and 1B schematically illustrate examples of existing memory package designs.

[0014] FIG. 2 schematically illustrates an example embodiment of a memory package in accordance with the present disclosure.

[0015] FIG. 3 schematically illustrates another example embodiment of a memory package in accordance with the present disclosure.

[0016] FIG. 4 schematically illustrates an example embodiment of a driver structure of a control die in accordance with the present disclosure.

[0017] FIG. 5 presents a flowchart for an example embodiment of a load optimization process.

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[0018] FIGS. 6A and 6B schematically illustrate an example of a Load Reduction Dual In-line Memory Module (LRDIMM) and a HyperCloud™ Dual In-line Memory Module (HCDIMM) architecture respectively.

[0019] FIG. 7 schematically illustrates an example of a Three-Dimensional Structure Dual In-line Memory Module (3DS-DIMM) architecture.

[0020] FIG. 8 schematically illustrates an example embodiment of a memory module architecture in accordance with the present disclosure.

DETAILED DESCRIPTION OF SPECIFIC EMBODIMENTS

[0021] In addition to the below, the following U.S. patents are incorporated in their entirety by reference herein: U.S. Patent Nos. 7,289,386, 7,286,436, 7,442,050, 7,375,970, 7,254,036, 7,532,537, 7,636,274, 7,630,202, 7,619,893, 7,619,912, 7,811,097. Further, the following U.S. patent applications are incorporated in their entirety by reference herein: U.S. Patent Application Nos. 12/422,912, 12/422,853, 12/577,682, 12/629,827, 12/606,136, 12/874,900, 12/422,925, 12/504,131, 12/761,179, and 12/815,339.

[0022] Certain embodiments of the present disclosure reduce the size of drivers that are configured to drive a signal, such as a data signal, along a die interconnect to one or more array dies. Further, certain embodiments of the present disclosure reduce the power consumption of the drivers.

[0023] In certain embodiments, reducing one or both of driver size and driver power consumption may be accomplished by increasing the number of die interconnects and reducing the number of array dies that are in electrical communication with each die interconnect. For example, instead of one die interconnect in electrical communication with four array dies, there may be two die interconnects, each in electrical communication with a different pair of the four array dies.

[0024] In certain embodiments, determining the number of die interconnects and the number of array dies in electrical communication with each die interconnect is based, at

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least in part, on a load of each array die and a load of the die interconnect that is in electrical communication with one or more of the array dies.

[0025] In some embodiments, the load contribution from a die interconnect may be negligible compared to the load contribution from the array dies. In such embodiments, determining the number of die interconnects and the number of array dies in electrical communication with each die interconnect may be based, at least in part, on a load of each array die without considering the load of the die interconnect. However, as the physical size of a memory package shrinks, the load of a die interconnect becomes a non-negligible value relative to the load of the array dies. Thus, as memory packages become physically smaller, it becomes more important to consider the load of the die interconnect in determining the number of die interconnects and the number of array dies in electrical communication with each die interconnect. Advantageously, certain embodiments of the present disclosure account for both the loads of the array dies and the loads of the die interconnects on a conduit (e.g., driver) in determining the number of die interconnects to be used and the number of array dies in electrical communication with each die interconnect.

[0026] FIG. 2 schematically illustrates an example embodiment of a memory package 200 in accordance with the present disclosure. One example of a memory package that includes array dies and a control die is the Hybrid Memory Cube (HMC). Examples of an HMC compatible with certain embodiments described herein are described by the IDF2011 Intel Developer Forum website, http://www.intel.com/idf/index.htm, which includes presentations and papers from the IDF2011 Intel Developer Forum including the keynote address given by Justin Rattner on September 15, 2011. Additional examples of an HMC compatible with certain embodiments described herein are described by the Hybrid Memory Cube Consortium website, http://www.hybridmemorycube.org. The memory package 200 can include any type of memory package. For example, the memory package 200 may be a DRAM package, a SDRAM package, a flash memory package, or a DDR SDRAM package (e.g., DDR3, DDR4), to name a few. A memory module (not shown) may include one or more memory packages in accordance with the memory package 200. Further, the memory package 200 may include input/output

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terminals (not shown) that are configured to be placed in electrical communication with circuitry of the memory module to transmit signals between the memory package 200 and a Memory Control Hub (MCH) (not shown).

[0027] The memory package 200 may include a plurality of array dies 210 (e.g., array dies 210a-210d). The plurality of array dies 210 may be sealed within the memory package 200. Further, circuitry of the array dies 210 may be in electrical communication with the input/output terminals of the memory package 200. Although generally referred to as array dies herein, the array dies 210 may also be called slave dies or slave chips. Each of the array dies 210a-210d may include circuitry (e.g., memory cells) (not shown) for storing data. Examples of array dies compatible with certain embodiments described herein are described by the existing literature regarding the Hybrid Memory Cube (e.g., as cited above). As illustrated in FIG. 2, the plurality of array dies 210 may be arranged in a stack configuration known as a three-dimensional structure (30S). Examples of 30S compatible with certain embodiments described herein are described by the existing literature regarding the Hybrid Memory Cube (e.g., as cited above). However, the structure or layout of the plurality of array dies 210 is not limited as such, and other structures are possible in accordance with the present disclosure. For example, the plurality of array dies 210 may be arranged in a planar structure, or in a structure that combines 30S with a planar structure. Moreover, while the memory package 200 is illustrated as including four array dies, the memory package 200 is not limited as such and may include any number of array dies. For example, as illustrated in FIG. 3, the memory package 200 may include eight array dies. As further examples, the memory package 200 may include three or sixteen array dies.

[0028] Each of the array dies 210 may include one or more data ports (not shown). The data ports enable electrical communication and data transfer between the corresponding memory circuitry of the array dies 210 and a communication pathway (e.g., a die interconnect).

[0029] In the example schematically illustrated in FIG. 2, the memory package 200 includes a plurality of die interconnects 220 (e.g., die interconnects 220a, 220b). For

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example, certain versions of HMC have been reported to have 512 data ports per die, with the corresponding bits of each die all connected to a single die interconnect (e.g., TSV). Examples of die interconnects include, but are not limited to, through-silicon vias (TSV), conducting rods, wire bonds, and pins. (See e.g., U.S. Patent Nos. 7,633,165 and 7,683,459.) Each of these die interconnects 220 may be coupled to, or in electrical communication with at least one data port of at least one of the array dies 210. In certain embodiments, at least one of the die interconnects 220 is in electrical communication with at least one data port from each of at least two array dies 210 without being in electrical communication with a data port from at least one array die 210, which may be in electrical communication with a different die interconnect 220.

[0030] For example, die interconnect 220a may be in electrical communication with a data port from array die 210a and a data port from array die 210b (as illustrated by the darkened circles in FIG. 2) and not in electrical communication with any data ports from array die 210c or any data ports from array die 210d. The data ports of array dies 210a and 210b in electrical communication with the die interconnect 220a can be corresponding to the same data bit (e.g., 00). Other die interconnects (not shown) can be in electrical communication with other data ports corresponding to other data bits (e.g., 01, 02, ...) of array dies 210a and 210b. These other die interconnects can be electrically isolated from the corresponding data ports of array dies 210c and 210d.

[0031] However, continuing this example, the die interconnect 220b may be in electrical communication with a data port from array die 210c and a data port from array die 210d (as illustrated by the darkened circles in FIG. 2) (e.g., corresponding to the same data bit, e.g., 00) without being in electrical communication with any data ports from array die 210a and array die 210b. Other die interconnects (not shown) can be in electrical communication with other data ports corresponding to other data bits (e.g., 01, 02, ...) of array dies 210c and 210d. Despite not being in electrical communication with any data ports from array die 210a and 210b, in some implementations, the die interconnect 220b may pass through the array dies 210a and 210b (as illustrated by the unfilled circles) e.g., through through-holes or vias of array dies 210a and 210b. For some implementations, each of the array dies 210 may be in electrical communication with corresponding die

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interconnects 220, without any of the die interconnects 220 being in electrical communication with all of the array dies 210. Where existing systems may utilize a single die interconnect to be in electrical communication with the corresponding data ports of each array die (e.g., the data ports corresponding to the same bit), certain embodiments described herein utilize multiple die interconnects to provide electrical communication to the corresponding data ports of the array dies (e.g., the data ports corresponding to the same data bit) with none of the multiple die interconnects in electrical communication with data ports of all the array dies.

[0032] In addition to the plurality of array dies 210, the memory package 200 includes a control die 230, which may also be called a master die. Examples of master dies compatible with certain embodiments described herein are described by the existing literature regarding the Hybrid Memory Cube (e.g., as cited above). In some embodiments, the control die 230 may be one of the array dies 210. Alternatively, the control die 230 may be a modified version of one of the array dies 210. Thus, in some implementations, memory package 200 may include four dies or chips instead of the five illustrated in FIG. 2. Further, in some embodiments, the control die 230 may comprise a logic layer (e.g., the logic layer of an HMC).

[0033] The control die 230 may include a number of data conduits 232, which includes data conduits 232a and 232b. Each of these data conduits 232 may be configured to transmit a data signal to a single die interconnect 220. For example, the data conduit 232a may be configured to transmit a data signal to the die interconnect 220a without transmitting the data signal to the die interconnect 220b. Conversely, the data conduit 232b may be configured to transmit the data signal to the die interconnect 220b without transmitting the data signal to the die interconnect 220a (e.g., data conduit 232b is electrically isolated from die interconnect 220a and data conduit 232a is electrically isolated from die interconnect 220b).

[0034] In some embodiments, the data conduits 232 may also include one or more drivers 234 as schematically illustrated by FIG. 2. The drivers 234 may be configured to drive the data signals along the corresponding die interconnects 220. In some embodiments, a

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single data conduit 232 or driver 234 may be in electrical communication with multiple die interconnects 220, each of which may be in electrical communication with different array dies 210.

[0035] Each of the data conduits 232 may be configured to receive the data signal from a common source. For instance, the data conduit 232a and the data conduit 232b may each receive a substantially similar, if not identical, data signal from the same signal source (e.g. the data signal corresponding to the same data bit). The source of the data signal may include a data path, a driver, a latch, a pin, or any other construct that may provide a data signal to a data conduit.

[0036] The data conduits 232 may each be subject to a load. Although not limited as such, this load may be measured as a capacitive load, such as a parasitic capacitance. The load on each of the data conduits 232 may include at least a load of the die interconnect 220 to which the data conduit 232 is coupled or connected as well as a load of each array die 210 with which the die interconnect 220 is in electrical communication via a data port of the die interconnect 220. Thus, for example, the load of the data conduit 232a may include loads of the die interconnect 220a, the array die 210a, and the array die 210b. Similarly, the load of the data conduit 232b may include loads of the die interconnect 220b, the array die 210c, and the array die 210d.

[0037] Generally, a load that would be on a data conduit that was in electrical communication with a die interconnect that was in electrical communication with at least one data port of each of the array dies 210 can be considered the maximum load for a data conduit. This maximum load is the load of a data conduit of a memory package that does not implement the teachings of this disclosure, but is in accordance with conventional configurations.

[0038] In some implementations, the difference between the load of the data conduit 232a and the load of the data conduit 232b is less than the maximum load for a data conduit as described above. Thus, in some cases, there may exist a degree of balance or equalization between the loads of the data conduits 232a, 232b. In some implementations, the difference between the load of the data conduit 232a and the load of the data conduit

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232b is zero or substantially zero. In some embodiments, the length of each die interconnect 220, and the number of array dies 210 in electrical communication with each die interconnect 220 may be selected to maintain the difference between the load of the data conduit 232a and the load of the data conduit 232b to be at or below a threshold load difference. For example, suppose that the load of each array die 210 is 1, the load of each segment of the die interconnects 220 is 0.25, and that the threshold load difference is 0.5. Using the configuration schematically illustrated in FIG. 2, the load on the data conduit 232a in this example is 2.5 and the load on the data conduit 232b in this example is 3. Thus, in this example, the difference between the load of the data conduit 232a and the load of the data conduit 232b is at the threshold load difference value of 0.5. However, an alternative configuration that places the die interconnect 220a in electrical communication with only the array die 210a, and the die interconnect 220b in electrical communication with the array dies 210b-210d would not satisfy the threshold load difference value of 0.5 of the above example. In the alternative configuration, the load on the data conduit 232a would be 1.25 and the load on the data conduit 232b would be 4. Thus, in the alternative configuration, the difference between the load of the data conduit 232a and the load of the data conduit 232b is 2.75, which is above the threshold load difference value of 0.5.

[0039] For certain embodiments, the load of each data conduit is less than the maximum load as described above. Thus, in some cases, the load of the data conduit 232a is less than the maximum load and the load of the data conduit 232b is less than the maximum load. Further, in many implementations, the combined load of the data conduit 232a and the data conduit 232b is less than the maximum load of a single data conduit. In other words, it is possible to design the data conduit 232a and the data conduit 232b to reduce the overall load compared to a single data conduit that is in electrical communication with a die interconnect that is in electrical communication with at least one data port of each of the array dies 210. By reducing the overall load compared to the single data conduit, it is possible in many cases to reduce power consumption. Further, it is possible in many cases to maintain signal quality (e.g. maintain signal amplitude, maintain low signal distortion, etc.) while reducing power consumption. Advantageously, in a number of embodiments, by using multiple data conduits instead of a single data conduit, the

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speed of the memory package 200 can be increased. In some cases, this speed increase can include a reduced latency in accessing array dies 210 and/or operating the memory package 200 at a higher clock frequency.

[0040] Each of the die interconnects 220 may include any type of conducting material. For example, the die interconnects 220 may include copper, gold, or a conductive alloy, such as a copper/silver alloy. Further, the die interconnects 220 may include any type of structure for enabling electrical communication between the data conduits 232 and the data ports of the array dies 210. For example, the die interconnects 220 may include a wire, a conducting rod, or a conducting trace, to name a few. Moreover, the die interconnects 220 may use vias, or through-silicon vias (TSVs) to couple with or to electrically communicate with an array die. For instance, die interconnect 220a may be connected with data ports of the array dies 210a and 210b using vias (illustrated by the filled or darkened circles). Examples of TSVs which may be used with the present disclosure are described further in U.S. Patent Nos. 7,633,165 and 7,683,459.

[0041] In addition, the die interconnects 220 may use via holes to pass through an array die that is not configured to be in electrical communication with the die interconnect. For instance, die interconnect 220b may pass through array dies 210a and 210b using TSVs that do not electrical communication between the die interconnect 220b and data ports of the array dies 210a and 210b (illustrated by the unfilled circles). In this way, the array dies 210a, 210b are not responsive to the data signals being transmitted by the die interconnect 220b. However, the die interconnect 220b may be connected with at least one data port of each of the array dies 210c and 210d using a via (illustrated by the filled or darkened circles). In cases where the die interconnect passes through an array die that is not configured to be in electrical communication with the die interconnect, the TSV may include an insulator or an air gap between the die interconnect and the array die circuitry that is large enough to prevent electrical communication between the die interconnect and the array die circuitry. In certain embodiments, the TSV for array dies that are configured to be in electrical communication with the die interconnect and for array dies that are not configured to be in electrical communication with the die interconnect may be configured the same. However, in such cases, electrical connections

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leading from the TSV of the array dies that are not configured to be in electrical communication with the die interconnect may not exist or may be stubs. These stubs are not configured to provide electrical communication with the memory cells of the array die.

[0042] Although FIG. 2 illustrates a single pair of data conduits 232 corresponding to a single pair of die interconnects 220, this is only to simplify the drawing figure. The memory package 200 may generally include as many additional data conduits and corresponding die interconnects as the number of bits the memory package 200 is designed or configured to support per memory address. Thus, if, for example, the memory package 200 is configured to be a 16-bit memory, the memory package 200 may include 16 pairs of data conduits 232 and 16 pairs of corresponding die interconnects 220. Similarly, if the memory package 200 is configured as a 32-or 64-bit memory, the memory package 200 may include 32 or 64 pairs of data conduits 232 and 32 or 64 pairs of corresponding die interconnects 220. Generally, the data conduits and die interconnects for each bit are configured identically. Thus, for the memory package 200, each data conduit is configured to be in electrical communication with a die interconnect that is configured to be in electrical communication with a pair of the array dies 210. However, it is possible that, in some embodiments, the data conduits and die interconnects of different bits may be configured differently.

[0043] In certain embodiments, the same die interconnects and the same corresponding data conduits may be used to transfer data both to and from the array dies 210. In such embodiments, the die interconnects may be bi-directional. In alternative embodiments, separate die interconnects and corresponding data conduits may be used to transfer data to the array dies 210 and data from the array dies 210 to the control die 230. Thus, such embodiments may include double the number of die interconnects and data conduits as embodiments that use the same die interconnect to transfer data to and from an array die.

[0044] In some embodiments, the control die 230 may include additional command/address conduits 240 and die interconnects 242, which may be in electrical communication with at least one port of each of the array dies 210. For simplicity, FIG. 2

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shows only a single such conduit 240 and die interconnect 242. The command/address conduits 240 are configured to provide corresponding signals to the die interconnects 242. These signals may be command signals, address signals, or may serve as both command and address signals (e.g., may include a memory cell address and a write command or a read command) either simultaneously or based on a determining criterion, such as the edge of a clock signal. The command die 230 may include a command/address conduit 240 and corresponding die interconnect 242 for each bit of the command/address signals that the memory package 200 is configured to support. The number of bits of the command/address signals may be the same or may be different from the number of data bits of the memory package 200.

[0045] In addition, in certain embodiments, the control die 230 may include a plurality of chip select conduits 250 (e.g., chip select conduits 250a-250d as shown in FIG. 2). Further, the control die 230 may include corresponding die interconnects 252 (e.g., die interconnects 252a-252d) with one die interconnect 252 in electrical communication with one chip select conduit 250 and one array die 210. Each of the die interconnects 252 may be in electrical communication with a different array die 210. For example, the die interconnect 252a may be in electrical communication with the array die 210a and the die interconnect 252b may be in electrical communication with the array die 210b. Each of the chip select conduits 250 may be configured to provide a chip select signal to a corresponding array die 210 via a corresponding die interconnect 252.

[0046] In some embodiments, the control die 230 may include additional drivers that are configured to drive the chip select signals along the die interconnects 252. Alternatively, the chip select signals may be driven by drivers that are external to the control die 230. For example, a register (not shown) that is part of a memory module that includes the memory package 200 may determine the chip select signals and drive the chip select signals to the array dies 210. As a second example, the chip select signals may be provided by an MCH. In some embodiments, the control die 230 may determine the array die 210 to select based on, for example, an address signal. In such embodiments, the control die may generate the chip select signals.

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[0047] FIG. 3 schematically illustrates another example embodiment of a memory package 300 in accordance with the present disclosure. In certain embodiments, some or all of the embodiments described above with respect to the memory package 200 may be applicable to the memory package 300. However, for ease of illustration and to simplify discussion, certain elements are omitted in FIG. 3, such as the chip select conduits. Nevertheless, it should be understood that the memory package 300 can include the same or similar elements as described above with respect to the memory package 200, including, for example, the chip select conduits.

[0048] The memory package 300 may include a plurality of array dies 310 (e.g., array dies 310a-310h). In the implementation illustrated in FIG. 3, the memory package includes eight array dies. However, as stated earlier, the memory package 300 may include more or fewer array dies. Each of the array dies 310 may include one or more ports (not shown) that enable electrical communication between the circuitry of the array dies 310 and one or more die interconnects 320. Each of these die interconnects 320 may be coupled to, or in electrical communication with at least one port of at least one of the array dies 310. As with the memory package 200, in certain embodiments, at least one of the die interconnects 320 is in electrical communication with at least one port from each of at least two array dies 310 without being in electrical communication with a port from at least one array die 310, which may be in electrical communication with a different die interconnect 320.

[0049] In addition to the plurality of array dies 310, the memory package 300 includes a control die 330. In some embodiments, the control die 330 may include a number of conduits 332 (e.g., conduits 332a-332f). Each of these conduits 332 may be configured to transmit a signal to a single die interconnect 320.

[0050] Further, implementations of the conduits 332 may include one or more drivers 334 (e.g., drivers 334a-334f). Each of the drivers 334 may be configured to drive a signal along a corresponding die interconnect 320. For instance, the driver 334a of the conduit 332a may be configured to drive a signal along the die interconnect 320a to one or more of the array dies 310a and 310b. As a second example, the driver 334b of the conduit

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332b may be configured to drive a signal along the die interconnect 320b to one or more of the array dies 310c and 310d. Although the die interconnect 320b may pass through the array dies 310a and 310b, because the die interconnect 320b, in the example illustrated in FIG. 3, is not configured to be in electrical communication with the array dies 310a and 310b, the driver 334b does not drive the signal to the array dies 310a and 310b.

[0051] In some embodiments, the signal can be a data signal, a command or address signal, a chip select signal, a supply voltage signal, or a ground voltage signal, to name a few. Further, as the signal is not limited to a data signal, in some embodiments, the conduits 332 may include conduits configured to provide signals other than data signals to the die interconnects 320. For example, the conduits may include conduits configured to provide a command or address signal, a chip select signal, a supply voltage signal, or a ground voltage signal to one or more die interconnects. Consequently, in some embodiments, the drivers 334 may be configured to drive signals other than data signals.

[0052] Generally, the signal that each of the drivers 334 drive to the corresponding die interconnects 320 is from a common source. Thus, each of the drivers 334, in certain embodiments, is driving the same signal to each corresponding die interconnect 320.

[0053] The size of the drivers 334 is generally related to the load on the driver 334. In certain embodiments, the load on each driver 334 corresponds to the load of the respective conduit 332. Although not limited as such, the load may be measured as a capacitive load, such as a parasitic capacitance.

[0054] The load on each of the conduits 332 may include at least the loads of the die interconnect 320 with which the conduit 332 is coupled or connected as well as the loads of each array die 310 with which the die interconnect 320 is in electrical communication via a port of the die interconnect 320. Thus, for example, the loads of the conduit 332a may include the loads of the die interconnect 320a, the array die 310a, and the array die 310b. Similarly, the loads of the conduit 332b may include the loads of the die interconnect 320b, the array die 310c, and the array die 310d. The loads of both conduits 332a and 332b include a load of two array dies 310 because the corresponding die

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interconnects 320 are each configured to be in electrical communication with two array dies 310. On the other hand, the load of the conduit 332c, which may include the loads of the die interconnect 320c and the array die 310e, includes a load of one array die 310e because the corresponding die interconnect 320c is configured to be in electrical communication with only one array die 310.

[0055] As previously described with respect to FIG. 2, a load that would be on a conduit that was in electrical communication with a die interconnect that was in electrical communication with at least one port of each of the array dies 310 can be considered the maximum load for a conduit. This maximum load is the load of a conduit of a memory package that does not implement the teachings of this disclosure, but is used in accordance with conventional configurations.

[0056] In some implementations, the difference between the loads of any pair of the conduits 332 is less than the maximum load for a conduit as described above. For instance, the difference between the load of the conduit 332a and the load of the conduit 332b is less than the maximum load. As a second example, the difference between the load of the conduit 334f and anyone of the conduits 334a334e is less than the maximum load. Thus, in some cases, the load on each of the conduits 332 may be, at least partially balanced or equalized to reduce or minimize the difference between the load of any pair of the conduits 332. In some implementations, the difference between the load of a pair of the conduits 332 is zero or substantially zero. In some embodiments, the length of each die interconnect 320, and the number of array dies 310 in electrical communication with each die interconnect 320 may be selected to maintain the difference between the load of any pair of the conduits 332 to be at or below a threshold load difference.

[0057] For certain embodiments, the load of each conduit is less than the maximum load as described above. Thus, for example, the load of the conduit 332a, the load of the conduit 332b, and the load of the conduit 332c are each less than the maximum load defined above.

[0058] In certain embodiments, the load associated with each of the array dies 310 may be substantially equivalent. For example, the load of the array die 310a may be

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substantially equal to the load of the array die 310h. Thus, the load contribution from the array dies 310 for a specific conduit 332 may be measured as a multiple of the array dies that are in electrical communication with a die interconnect 320 corresponding to a specific conduit 332. For example, assuming that the load of each of the array dies 310 is 'L', then the contribution of the load from the array dies 310 to the conduit 332a would be 2L because the die interconnect 320a corresponding to the conduit 332a is in electrical communication with two array dies 310, array dies 310a and 310b. In alternative embodiments, the load of each of the array dies 310a may differ. For example, the load of array die 310a may be L and the load of the array die 310b may be 1.25L.

[0059] Similar to the array dies 310, in some embodiments, a die interconnect 320 can be considered to comprise a plurality of segments, with each segment of a die interconnect 320 contributing a substantially equivalent load to the load of the die interconnect 320. In this case, the segment of the die interconnect 320 may refer to the portion of the die interconnect between two successive or adjacent dies (array die-to-array die, master die-to-array die, or both) along the die interconnect 320. Further, the segment may be defined as a portion of the die interconnect 320 between the dies exclusive of a portion of the dies. For example, one segment of the die interconnect 320a may extend from the top of the array die 310a to the bottom of the array die 310b. Alternatively, the segment may be defined to include at least a portion of at least one of the array dies 310. For example, one segment of the die interconnect 320a may extend from the center of array die 310a to the center of array die 310b. As a second example, one segment of the die interconnect 320a may extend from the top of the control die 330 to the top of the array die 310a, and therefore may include a portion of the die interconnect 320a extending from the bottom of the array die 310a to the top of the array die 310a. In some implementations, the segments are substantially equal in length to each other. Moreover, the load contribution of each segment may be substantially equal to each other. Alternatively, the segments may be unequal in length and/or may each contribute a different load to the total load of a die interconnect 320. Further, in some cases, the load contribution of a segment of the die interconnect 320 that is in electrical communication with a port of an array die 310 may differ from the load contribution of a segment of the die interconnect 320 that is not in electrical communication with a port of an array die 310.

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[0060] In some cases, the load contribution of each segment of the die interconnect 320 may be measured as a fraction of the load contribution from an array die 310. For example, the load of one segment of the die interconnect 320a may be equivalent to one quarter of the load of an array die 310. Thus, for example, the load of the conduit 332a may be 2.5L assuming a load contribution of L per array die 310 (two in this case) in electrical communication with the die interconnect 320a and a load contribution of 0.25L per segment (two in this case) of the die interconnect 320a. As a second example, the load of the conduit 332f may be 3L assuming the same load values as the previous example and a load contribution from one array die 310h and eight die interconnect 320f segments. Table 1 specifies the capacitive load values for each conduit 332 assuming, as with the previous two examples, that the load of each of the array dies 310 is L, and that the load of each segment of the die interconnects 320 is 0.25L. Table 1 also specifies the deviation in load from the conduits having the highest load value, which in this example are conduits 332b and 332f.

TABLE 1

Conduit	Number of Array Dies	Number of Die Interconnect Segments	Capacitive Load	Deviation from Maximum Load
332a	2	2	2.5L	0.5
332b	2	4	3L	0
332c	1	5	2.25L	0.75
332d	1	6	2.5L	0.5
332e	1	7	2.75L	0.25
332f	1	8	3L	0

[0061] As can be seen from Table 1, the maximum load of any conduit 332, using the example values previously described, is 3L, or rather three times the load of a single array die 310. Assuming the same example values, the load of a conduit in electrical communication with a die interconnect that itself is in electrical communication with each array die 310 would be 10L. Thus, certain embodiments of the present disclosure enable a reduction in the load of the conduits 332. Consequently, in some embodiments, the drivers 334 may each be smaller than a single driver that is configured to drive a signal from a conduit along a single die interconnect that is in electrical communication with a port from each of the array dies 310. Moreover, the drivers 334 may include smaller transistor sizes than a single driver that is configured to drive a signal to each of

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the array dies 110.

[0062] As can be seen from Table 1, conduits 332b and 332f have the largest capacitive load of the group of conduits, which is 3L. Conduit 332 has the smallest capacitive load of the group of conduits, which is 2.25L and which is a deviation of only 0.75 from the maximum load. Thus, in some embodiments, each of the drivers 334 may be substantially similar in size. In certain implementations, the drivers 334 may vary in size based on the total capacitive load on each conduit 332. Thus, the driver 334f may be larger than the driver 334e. Alternatively, each driver 334 may be substantially equal and may be configured based on the drivers 334 with the largest load, which are drivers 334b and 334f in the example illustrated in FIG. 3 and Table 1.

[0063] In some embodiments, the capacitive load of each conduit 332 or driver 334 can be calculated using formula (1).

$$CL = AD + {}^{S}/_{M}$$

[0064] In formula (1), CL represents the capacitive load of a conduit 332 or driver 334, AD represents the number of array dies 310 in electrical communication with a die interconnect 320 that is in electrical communication with the conduit 332 and/or driver 334, S represents the number of die interconnect segments of the die interconnect 320, and M represents the ratio of the load of an array die 310 to the load of a segment of a die interconnect 320. Thus, using formula (1) and the example values described above, the load of the driver 332a, for example, can be calculated with the following values: AD=2, for two array dies 310; S=2, for the two segments of the die interconnect 320a; and M=4, for the ratio of the load of an array die 310, L, to the load of a segment of the die interconnect 320a, 0.25L. Therefore, as can be seen from Table 1, the capacitive load of the driver 332a is 2.5L where L is the load of a single array die.

[0065] In some cases, the load on each conduit 332 and/or driver 334 may be evenly balanced. In other words, the load on each conduit 332 and/or driver 334 may be substantially the same. To achieve a balanced load, each of the conduits 332 may be in electrical communication with a combination of array dies 310 and die interconnect 320

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segments that results in a load that is substantially equivalent to the loads of the other conduits 332. In certain embodiments, the load of the conduits 332 is balanced despite each conduit 332 being in electrical communication with a different subset of the array dies 310. However, in alternative embodiments, the load of each conduit 332 and/or driver 334 may differ. This difference in the load of the conduits 332 and/or drivers 334 may be a design decision (e.g. to maintain a specific number of drivers). Alternatively, or in addition, the load difference between conduits 332 and/or drivers 334 may occur because the loads of the array dies 310 and the die interconnect segments 320 do not allow for perfect or substantially even load balancing.

[0066] As previously stated, in some embodiments the loads of the conduits 332 and/or drivers 334 may be balanced to minimize the difference between any pair of conduits 332 and/or drivers 334. For example, as illustrated in FIG. 3, a driver in electrical communication with a longer die interconnect, which may consequently include more die interconnect segments, is likely to obtain a larger load contribution from the die interconnect than a driver in electrical communication with a shorter die interconnect (e.g., compare driver 334f to 334a). Thus, the driver in electrical communication with the longer die interconnect may be in electrical communication with fewer array dies than the driver in electrical communication with the shorter die interconnect (e.g. compare driver 334f to 334a). The selection of die interconnect length and the selection of array dies to place in electrical communication with the die interconnects may therefore be dependent on the load of each segment of the die interconnects 320 and the loads of the array dies 310.

[0067] Alternatively, or in addition, the loads of the conduits 332 and/or drivers 334 may be balanced to reduce the maximum load of each conduit 332 and/or driver 334. Further, in some embodiments, the maximum load of each conduit 332 and/or driver 334 may be reduced to maintain the load of each conduit 332 and/or driver 334 to be at or below a threshold load difference.

[0068] Although not illustrated in FIG. 3, each of the conduits 332 may include one or more additional drivers configured to drive a signal received from an array die via a

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corresponding die interconnect 320. The additional drivers may drive the signal to a processor, a register, a latch, or any other component or device that mayor may not be part of a memory module that includes the memory package 300. In some implementations, one or more of the die interconnects 320 are configured to be bi-directional, thereby enabling a signal to be driven to the array dies 310 via the die interconnect 320, and to enable a signal received from the array dies 310 along the same die interconnect 320 to be transmitted to a corresponding conduit 332 of the control die 330. Alternatively, the memory package 300 comprises one or more die interconnects 320 that are configured to enable a signal to be driven to the array dies 310 without enabling a signal to be received from the array dies 310 (e.g., the die interconnects 320 may not be bidirectional). In certain embodiments where one or more of the die interconnects 320 are not bi-directional, the memory package 300 may include additional die interconnects (not shown) that are in electrical communication with the one or more additional conduits or drivers and that are configured to enable a signal from the array dies 310 to be transmitted to the one or more additional conduits or drivers.

[0069] In addition to the drivers 334 of the control die 330, the memory package 300 may include one or more pre-drivers 340. A pre-driver 340, shown schematically in FIG. 3, may be large enough to drive a signal (e.g., a data signal) to any of the drivers 332 and subsequently, to any of the array dies 310. Thus, using the same example values as described above in relation to Table 1, a load of the pre-driver 340 may be at least 10l, which is the load of a conduit in electrical communication with a die interconnect that is in electrical communication with a port from each of the array dies 310. In some embodiments, the memory package 300 may include any number of additional drivers and/or latches for buffering and/or driving the signal to any of the array dies 310.

[0070] Just as the memory package 300 may include a pre-driver 340 for providing a signal to the conduits 332, the memory package 300 may include a post-driver (not shown) for driving an output signal from the control die 330. This post-driver may drive the output signal to additional latches and/or drivers. In some embodiments, the post-driver may drive the signal from the memory package 300 to a bus or other electrical path that is in electrical communication with the memory package 300.

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[0071] FIG. 4 illustrates an example embodiment of a driver structure 400 of a control die (e.g. control die 230) in accordance with the present disclosure. The driver structure 400 is configured for a single data bit. Thus, a control die for a 32-bit memory package will generally include at least 32 instances of the driver structure 400, one per bit. In some embodiments, the control die 230 may include the driver structure 400 in place of the combination of drivers 232a and 232b. Similarly, in certain embodiments, the control die 330 may include a structure similar to the driver structure 400 in place of the drivers 334. In such embodiments, the driver structure 400 would be modified to enable a signal (e.g., data signal) to be driven to the six conduits 332.

[0072] The driver structure 400 can include an input/output port 402 configured to receive or send a signal, such as a data signal. Signals received at the input/output port 402 can be provided to the drivers 404a and 404b. In turn, these drivers 404a and 404b can drive the signal to conduits 406a and 406b respectively, which are in electrical communication with corresponding die interconnects. Each of the die interconnects may be in electrical communication with different array dies in accordance with certain embodiments described herein.

[0073] In some embodiments, the driver structure 400 is bi-directional. In such embodiments, operation of the drivers 404a and 404b, and 408a and 408b may be controlled or enabled by a control signal (e.g., a directional control signal). This control signal, in some cases, may correspond to one or more of a command/address signal (e.g., read/write) and a chip select signal. In some implementations, the drivers 404a and 404b may drive a signal to the array die corresponding to the chip select signal, and not to array dies that do not correspond to a chip select signal. For example, suppose the conduit 406a is in electrical communication with array dies one and two (not shown), and that the conduit 406b is in electrical communication with array dies three and four (not shown). If a chip select signal is received corresponding to array die two, then in some implementations, driver 404a may be configured to drive a signal along a die interconnect in electrical communication with the conduit 406a to array die one and two. In this example, the driver 404b would not drive the signal because the chip select signal does not correspond to either array die three or array die four.

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[0074] In some embodiments, the drivers 404a and 404b may drive a signal to all of the array dies. For example, assume the memory package that includes the driver structure 400 also includes four array dies. If the die interconnect in electrical communication with the conduit 406a is in electrical communication with two of the array dies, and if the die interconnect in electrical communication with the conduit 406b is in electrical communication with the other two array dies, then the drivers 404a and 404b may drive a signal to all four of the array dies of this example.

[0075] Similar to the input/output port 402, the conduits 406a and 406b can be configured to receive a signal from the die interconnects that are in electrical communication with the conduits 406a and 406b. In turn, the signal received at one of the conduits 406a and 406b can be provided to drivers 408a and 408b respectively. The drivers 408a and 408b can each be configured to drive a signal received from a respective data conduit 406a and 406b to the input/output port 402 and to another component that may be in electrical communication with the input/output port 402, such as a MCH.

[0076] In some embodiments, one or more chip selects, as illustrated in FIG. 2, may be used to select, determine, or enable the array die that communicates the signal to or from one or more of the conduits 406a and 406b and the drivers 408a and 408b. Similarly, in some embodiments, the chip select may select, determine, or enable the array die to receive and/or respond to the signal driven by the drivers 404a and 404b to the array dies.

[0077] It should be noted that the driver structure 400 is a non-limiting example for arranging drivers in a control die. Other driver structures are possible. For example, instead of the drivers 404a and 408a being in electrical communication with the same conduit 406a, each of the drivers 404a and 408a can be in electrical communication with a separate conduit and consequently a separate die interconnect. In such an example, the drivers 404a and 408a may still be in electrical communication with the same input/output port 402, or each driver may be in electrical communication with a separate port, the driver 404a in electrical communication with an input port, and the driver 408a in communication with an output port.

[0078] FIG. 5 presents a flowchart for an example embodiment of a load optimization

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process 500. In certain embodiments, the load optimization process 500 may be performed, at least in part, by one or more computing systems. Further, the process 500, in some embodiments, may be used to optimize one or more loads in a memory package (e.g. memory package 200 or memory package 300). Optimizing the loads in the memory package can include optimizing the load on one or more conduits and/or drivers. As previously described with respect to FIGS. 2 and 3, the memory package can include a plurality of array dies, a plurality of die interconnects, and a control die. Furthermore, the control die can include a plurality of drivers, each of which may be configured to drive a signal along a die interconnect.

[0079] In some implementations, the process 500 can comprise selecting a first subset of array dies and a second subset of array dies from a plurality of array dies (e.g., array dies 310), as shown in operational block 502. Generally, the first subset of array dies and the second subset of array dies may be exclusive of one another. Thus, the first subset of array dies does not include any array dies from the second subset of array dies and vice versa. However, in some cases there may be some overlap between the first subset of array dies and the second subset of array dies. Further, in some cases, at least one of the subsets of array dies includes more than one array die. For instance, the first subset of array dies may include two array dies, and the second subset of array dies may include one array die, which, depending on the embodiment, mayor may not be included in the first subset of array dies.

[0080] Further, the first subset of array dies and the second subset of array dies may be selected to balance a load on a first driver and a load on a second driver based, at least in part, on the loads of the array dies 310 and on the loads of the die interconnect segments from a first and a second die interconnect. The first die interconnect may be in electrical communication with the first driver and the second die interconnect may be in electrical communication with the second driver. In some embodiments, the first subset of array dies and the second subset of array dies are selected to balance a load on a first conduit and a load on a second conduit. The load on each driver and/or conduit may be calculated using formula (1) as previously described above. In some embodiments, the first subset of array dies and the second subset of array dies may be selected to balance a load on a

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first driver and a load on a second driver based, at least in part, on the loads of the array dies 310 without considering the loads of the die interconnect segments from the first die interconnect and the second die interconnect.

[0081] The process 500 further comprises forming electrical connections between the first die interconnect and the first subset of array dies in an operational block 504. The process 500 further comprises forming electrical connections between the second die interconnect and the second subset of array dies in an operational block 506. Forming the electrical connections places the die interconnects in electrical communication with the respective subsets of array dies. In some embodiments, forming the electrical connections can comprise forming electrical connections between the die interconnects and at least one port from each array die of the respective subsets of array dies.

[0082] The process 500 further comprises selecting a driver size for a first driver at block 508 and selecting a driver size for a second driver at block 510. Selecting the driver size can be based, at least in part, on the calculated load on the driver. Generally, the greater the load on the driver, the larger the driver is selected to drive a signal along, for example, a die interconnect. The size of the driver may be adjusted by the selection of the transistor size and/or number of transistors included in the driver. A larger driver often consumes more power than a smaller driver. Thus, in certain embodiments, balancing the loads on the drivers to reduce the load on each driver can reduce the power consumption of a memory package.

[0083] In some embodiments, the size of the first driver and the size of the second driver are both less than the size sufficient for a driver to drive a signal along a die interconnect to each of the array dies 310 (e.g., with less than a predetermined or threshold signal degradation). The threshold signal degradation can be based on anyone or more characteristics of a signal. For example, the threshold signal degradation can be based on the amplitude of the signal, the frequency of the signal, the noise distortion included in or introduced into the signal, or the shape of the signal, to name a few.

[0084] The process 500 further comprises forming electrical connections between the first die interconnect and the first driver in an operational block 512. Similarly, the

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process 500 further comprises forming electrical connections between the second die interconnect and the second driver in an operational block 514. Forming the electrical connections places the die interconnects in electrical communication with the respective drivers. In some embodiments, forming the electrical connections can comprise forming electrical connections between the die interconnects and a data conduit that includes the respective driver.

[0085] Advantageously, certain embodiments of the present disclosure reduce the load on each conduit and on each corresponding driver. In certain embodiments, reducing the load on a driver may increase the speed of data transfer between the array dies and other components in a computer system (e.g. a MCH or a processor). Further, reducing the load on a driver may result in reduced power consumption by the driver and consequently, by the memory package. In addition, certain embodiments of the present disclosure may minimize current switching noise.

Operational Modes

[0086] A proposed three-dimensional stacking (3DS) standard for dual in-line memory modules (DIMMs) being considered by the Joint Electron Devices Engineering Council (JEDEC) addresses three major shortcomings in the current JEDEC registered DIMM (RDIMM) and JEDEC load reduced DIMM (LRDIMM) standards (an example LRDIMM structure 600 is schematically illustrated in FIG. 6A). These shortcomings include: a) The DIMM density limitation due to the fixed number of chip-select signals received by the DIMM from the system memory controller. b) The performance loss due to the increased load on the data bus as the DIMM density (e.g., the number of DRAM devices and number of ranks) increases. c) The upper bound of the DIMM density due to the physical DIMM form factor.

[0087] Further, the LRDIMM structure 600 may have timing issues due to signals passing through a single memory buffer 601. In addition, the increased size of the data path of the LRDIMM architecture 600, compared to the HCDIMM architecture 602, an example of which is schematically illustrated in FIG. 68, may result in more latency and signal integrity issues.

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[0088] FIG. 7 schematically illustrates an example memory module 700 that has previously been proposed for the 3DS-DIMM standard. The proposed 3DS Dual In-line Memory Module (3DS-DIMM) schematically illustrated in FIG. 7 attempts to address the above shortcomings using two components, a 3DS register 712 and a controller die 722. In some implementations, the 3DS-DIMM 700 includes the 3DS register 712 (also known as an enhanced DDR3 register). The 3DS register 712 may include a DDR3 JEDEC standard register with a "rank multiplication" circuit, which increases the number of the output chip-select signals for selecting an array die 710 by decoding one or more higher-order row or column address bits with the incoming chip-select signals from the system controller. The 3DS Register 712 can also include a command/address buffer, a register operational code buffer (RC word buffer), and rank multiplication logic (e.g., supporting rank multiplication of 1-to-2, 1-to-4, and/or 1-to-8). The 3DS register addresses shortcoming (a) of the JEDEC RDIMM and LRDIMM listed above.

[0089] Another component of the proposed 3DS-DIMM is a 3DS dynamic random-access memory (DRAM) package 720. The 3DS DRAM package 720 includes a plurality of stacked DDR DRAM chips 724 or array dies. The 3DS DRAM package 720 has a data I/O load that is equivalent to the data I/O load of a single-die DRAM package, regardless of the actual number of DRAM dies in the 3DS DRAM package 720. The 3DS DRAM package 720 may comprise a plurality of array dies (e.g., 2, 4 or 8 DDR DRAM dies) and a controller die 722. The controller die 722 may include data buffers, a data path timing controller, a secondary command/address buffer, a programmable secondary 1-to-2 rank decoder, and a data path signal (e.g., DDT, DDT, RTT) controller. Examples of such memory packages include HMC. The 3DS DRAM package 720 addresses the shortcomings (b) and (c) of the JEDEC RDIMM and LRDIMM listed above. However, there are deficiencies in the proposed 3DS-DIMM standard as described below.

[0090] The JEDEC DDR3 RDIMM standard contains two major components: a DDR3 register and a plurality of DRAM packages each comprising one or more DRAM chips or dies. The DDR3 register serves as a command/address signal buffer and as a command/control decoder. This DDR3 register holds a set of register control (RC) words, which a computer system configures to ensure the proper operation of the RDIMM. The

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DDR3 register contains a phase-lock-loop (PLL), which functions as a clock synchronizer for each RDIMM. The DDR3 register outputs a set of buffered command/address signals to all the DRAM packages on the RDIMM, but the data signals are directly fed to the DRAM packages from the system memory controller.

[0091] In contrast to the JEDEC DDR3 RDIMM standard, the 3DS-DIMM proposal requires the DRAM package 720 to include the controller die 722 that controls all data paths timing and operations. This arrangement of the DRAM package reduces the load on the data bus, however, it presents three significant shortcomings: 1) The command/address buffer in the 3DS DRAM package introduces clock cycle latency since it needs to provide clock synchronous operation to the DRAM dies in the package. 2) The data path control circuit (e.g., DDT, read/write data direction) in the control die becomes very complicated to support semi-synchronous (flyby) data path control among all 3DS DRAM packages that are on a DIMM. 3) The variations in the DRAM die timing characteristics within each 3DS DRAM package would be likely to require resynchronization of the data signals during the read/write operations, which increases the read/write latency and the read-to-write and write-to-read turn around time.

[0092] The 3DS-DIMM proposal can also be compared to the HyperCloud™ (HC) DIMM architecture of Netlist, Inc. An example of the HCDIMM architecture 602 is illustrated in FIG. 68. Further details and embodiments of the HCDIMM architecture is disclosed in U.S. Pat. Nos. 7,289,386, 7,532,537, 7,619,912, and 7,636,274, each of which is incorporated in its entirety by reference herein. One of the main topological differences between the 3DS-DIMM and HCDIMM architectures is that while the 3DS-DIMM architecture uses a control die 722 to buffer the data signals and to decode command/address signals from the 3DS register, certain configurations of the HCDIMM architecture include a plurality of isolation devices (ID), each of which includes data buffers, but no decoding capability. Unlike the HCDIMM architecture, since the command/address signal needs to pass through the control die 722 in the 3DS DRAM package 720, the 3DSDIMM proposal presents the same shortcoming (b) of the controller die described above. The data path control signals are generated by the register device (RD) 612 in the HCDIMM architecture 602, while the data path control signals are

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generated by the control die 722 in the 3DS DRAM. This aspect of the 3DS-DIMM architecture creates timing critical control paths in 3DS-DIMM architecture.

[0093] In certain embodiments described herein, a memory module architecture is proposed that includes a set of device components that support JEDEC 3DS operation with the benefit of RDIMM and HCDIMM architectures (see, e.g., FIG. 8). This set of device components may comprise two components: a register device 812 (RD), which in some embodiments may be the same or similar RD component as used in HCDIMM architectures, and a plurality of array dies 824, such as a DDR DRAM Stack Package (DDSP). The DDSP may comprise a DRAM control die that can include command/address buffers and a data path control circuit. Certain embodiments of the architecture described herein differs from the 3DS-DIMM architecture in that instead of the controller die of the 3DS-DIMM (which provides a secondary address buffer, and a second rank multiplication decoder), certain embodiments described herein use an "ID+" die as a control die 822, which can provide both selective isolation and address pass-through. Selective isolation refers generally to a driver corresponding to an array die driving a signal to the array die in response to a corresponding chip select signal while additional drivers corresponding to additional array dies maintain a previous state (e.g. do not drive the signal). For example, assuming that the memory package 300 implements selective isolation, if a chip select signal is received that corresponds to a selection of array die 310b, then the driver 334a will drive a signal along the die interconnect 320a to the array die 310b, and the remaining drivers (e.g., drivers 334b-334f) will maintain their state (e.g., not drive the signal). Address pass-through is described in further detail below.

[0094] The data path control circuit of certain embodiments may have at least two operational modes: mode-C (HCDIMM/RDIMM Compatible mode) and mode-3DS (3DS DIMM compatible mode). In mode-C, the array dies 824 (e.g. a DDSP) receive the data path control signals from the register device 812, which can be configured to control a command/address time slot and a data bus time slot. In mode-3DS, the control die 822 internally generates the data path control signals to ensure the proper operation of the data path.

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[0095] The control die 822 of certain embodiments enables the memory module 800 to work as either a 3DS-DIMM, a RDIMM, or a HCDIMM. However, the memory module 800 may comprise a set of optional control input pins (in addition to the package pins that are included in 3DS-DRAM packages) which in mode-C receive the data path control signals from the register device 812.

[0096] As previously mentioned, FIG. 8 schematically illustrates an example embodiment of a memory module architecture 800 in accordance with the present disclosure. Advantageously, certain embodiments of the memory module architecture 800 address the shortcomings described above without adding complexity or latency, and without causing performance loss. The memory module architecture 800 includes a memory control hub 802 (also known as a memory controller hub, a memory control handler, or a northbridge) and a memory module 810. As schematically illustrated in FIG. 8, the memory control hub 802 may communicate directly with one or more components of the memory module 810. Alternatively, the memory control hub 802 may communicate with one or more intermediary system components (not shown), which in turn communicate with one or more components of the memory module 810. In some embodiments, the memory control hub 802 may be integrated with another component of the computer system, such as a Central Processing Unit (CPU).

[0097] Further, in some embodiments, the memory control hub 802 may communicate with one or more memory modules. Each of the memory modules may be similar or substantially similar to the memory module 810. Alternatively, some of the memory modules may differ from memory module 810 in configuration, type, or both. For example, some of the memory modules may be capable of operating at different frequencies, may include a different amount of storage capability, or may be configured for different purposes (e.g. graphics versus nongraphics memory). Although in some cases a system may include memory modules capable of operating at different frequencies, each memory module may be configured to operate at the same frequency when used in a specific device. In certain implementations, the memory control hub 802 may set the operating frequency for the one or more memory modules.

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[0098] The memory module 810 may include a register device 812, which is configured to receive command, address, or command and address signals from the memory control hub 802. For the purpose of simplifying discussion, and not to limit these signals, the signals will be referred to herein as command/address signals.

[0099] In some embodiments, the register device 812 receives the command/address signals via a command/address bus 814. The command/address bus 814, although illustrated as a single line, may include as many lines or signal conduits as the number of bits of the command/address signal.

[0100] Further, the register device 812 may generate data path control signals, which can be provided to a control die 822, or isolation device, of a memory package 820 via one or more data path control lines 816. In certain embodiments, the control dies 822 can include some or all of the embodiments described above with respect to the control dies 230 and 330. Moreover, in certain embodiments, the memory packages 820 can include some or all of the embodiments described above with respect to the memory package 200 and 300. In general, the memory module 812 may include one or more memory packages 820.

[0101] In certain embodiments, each control die 822, or isolation device, may be capable of address pass-through. Address pass-through, in some cases, enables the control die 822 to provide an address signal to one or more array dies 824 without decoding the address signal. This is possible, in some implementations, because the address signal received by the control die 822 is not encoded.

[0102] Some implementations of the control dies 822 include a plurality of command/address buffers (not shown). These buffers may comprise latches. In certain embodiments, the buffers are configured to hold command/address signals to control the timing of command/address signals. In some cases, controlling the timing of the command/address signals may reduce or slow signal degradation. In some implementations, the control dies 822 include a plurality of data buffers, which may control the timing of data signals to reduce or slow signal degradation. Further, the control dies 822 may include a data path control circuit (not shown) that is configured to

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control command/address time slots and data bus time slots. Controlling the command/address time slots and the data bus time slots enables the control dies 822 to reduce or prevent signal collisions caused by multiple memory packages 820 sharing the data path control lines 816 and the data bus 818. In some implementations, the data path control circuit may be separate from the control die 822.

[0103] Each of the control dies 822 may be configured to receive data signals from the memory control hub 802 via the data bus 818. Further, the control dies 822 may provide data signals to the memory control hub 802 via the data bus 818. The control dies 822 may also receive data path control signals and/or command/address signals from the register device 812 via the data path control lines 816.

[0104] As illustrated in FIG. 8, each memory package 820 may include one or more array dies 824 operatively coupled to the control die 822. The array dies 824 may be configured to receive data signals from the control die 822. As with the array dies 210 and 310, the array dies 824 may include any type of Random Access Memory (RAM) die. For example, the array dies 824 may include DDR DRAM, SDRAM, flash memory, or SRAM, to name a few. Further, if the memory module 810 is utilized for graphics, the array dies 824 may include GDDR SDRAM or any other type of graphics memory. In addition, the array dies 824 may be configured in a stack arrangement as illustrated in FIG. 8. Alternatively, the array dies 824 may be arranged in a planar configuration or a hybrid configuration utilizing both a planar and a stack arrangement.

[0105] In some embodiments, the memory module 810 is selectively configurable into two operational modes. In the first operational mode, the register device 812 generates data path control signals provided to the control dies 822 via the data path control lines 816. The control dies 822 may decode command/address signals included with the data path control signals generated by the register device 812. In some implementations, the control dies 822 use the data path control signals to operate the data path control circuits of the control dies 822.

[0106] In the second operational mode, the control dies 822 may operate the data path control circuits to provide command/address signals to the array dies 824 without

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decoding the command/address signals. In this mode, the control dies 822 may use address pass-through to provide received address signals to the array dies 824.

[0107] Other operational modes may also be possible. In some embodiments, the data path control signals generated by the register device 812 may include decoded command/address signals that are decoded from command/address signals received from the memory control hub 802 via the command/address bus 814.

[0108] In some embodiments, the register device 812 may be configured to perform rank multiplication. In addition, or alternatively, the control dies 822 may be configured to perform rank multiplication. Embodiments of rank multiplication are described in greater detail in U.S. Patent Nos. 7,289,386 and 7,532,537, each of which are incorporated in their entirety by reference herein. In such embodiments, the register device 812 can generate additional chip select signals that are provided to the array dies 824. For instance, if the memory control hub 802 is configured to recognize a single array die 824 per memory package 820, but there exists four array dies 824 per memory package 820, the memory control hub 802 may not provide the correct number of chip select signals to access a specific memory location of the plurality of array dies 824 is memory package 820. Thus, to access the specific memory location, the register device 812 can determine the array die that includes the specific memory location to be accessed based on the command/address signals received from the memory control hub 802 and can generate the correct chip select signal to access the array die that includes the specific memory location. In certain embodiments, when the memory module 810 is operating in the second operation module as described above, the memory module 810 does not perform rank multiplication.

Terminology

[0109] Unless the context clearly requires otherwise, throughout the description and the claims, the words "comprise," "comprising," and the like are to be construed in an inclusive sense, as opposed to an exclusive or exhaustive sense; that is to say, in the sense of "including, but not limited to." The term "coupled" is used to refer to the connection between two elements, the term refers to two or more elements that may be either directly

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connected, or connected by way of one or more intermediate elements. Additionally, the words "herein," "above," "below," and words of similar import, when used in this application, shall refer to this application as a whole and not to any particular portions of this application. Where the context permits, words in the above Detailed Description using the singular or plural number may also include the plural or singular number respectively. The word "or" in reference to a list of two or more items covers all of the following interpretations of the word: any of the items in the list, all of the items in the list, and any combination of the items in the list.

[0110] The above detailed description of embodiments of the invention is not intended to be exhaustive or to limit the invention to the precise form disclosed above. While specific embodiments of, and examples for, the invention are described above for illustrative purposes, various equivalent modifications are possible within the scope of the invention, as those skilled in the relevant art will recognize. For example, while processes or blocks are presented in a given order, alternative embodiments may perform routines having steps, or employ systems having blocks, in a different order, and some processes or blocks may be deleted, moved, added, subdivided, combined, and/or modified. Each of these processes or blocks may be implemented in a variety of different ways. Also, while processes or blocks are at times shown as being performed in series, these processes or blocks may instead be performed in parallel, or may be performed at different times.

[0111] The teachings of the invention provided herein can be applied to other systems, not necessarily the system described above. The elements and acts of the various embodiments described above can be combined to provide further embodiments.

[0112] Conditional language used herein, such as, among others, "can," "might," "may," "e.g.," and the like, unless specifically stated otherwise, or otherwise understood within the context as used, is generally intended to convey that certain embodiments include, while other embodiments do not include, certain features, elements and/or states. Thus, such conditional language is not generally intended to imply that features, elements and/or states are in any way required for one or more embodiments or that one or more embodiments necessarily include logic for deciding, with or without author input or

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prompting, whether these features, elements and/or states are included or are to be performed in any particular embodiment.

[0113] While certain embodiments of the inventions have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the disclosure. Indeed, the novel methods and systems described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the methods and systems described herein may be made without departing from the spirit of the disclosure. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the disclosure.

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WHAT IS CLAIMED IS:

1. A memory module operable in a computer system to communicate with a system memory controller via a command/address bus and a data bus, comprising:

a register device to receive command/address signals from the system memory controller via the command/address bus and to output control signals in response to the input command/address signals, the control signals including chip-select signals; and

a plurality of DRAM packages coupled to the register device via a set of module control lines, each respective DRAM package comprising:

control terminals coupled to the module control lines via which the each respective DRAM package receives the control signals from the register device, and data terminals coupled to a respective section of the data bus via which the each respective DRAM package communicates with the system memory controller respective bits of one or more data signals associated with the command/address signals;

stacked array dies;

a control die including data signal conduits coupled to the data terminals and control signal conduits coupled to the control terminals, the control signal conduits including chip-select conduits for receiving the chip select signals and providing respective ones of the chip select signals to respective ones of the stacked array dies; and

die interconnects including first die interconnects coupled to the data signal conduits and second die interconnects coupled to the control signal conduits, at least one of the first die interconnects is coupled to at least two of the stacked array dies; and

wherein the control die configures the data signal conduits in accordance with the control signals to enable the respective bits of the one or more data signals to be communicated between a selected die among the stacked dies and the system memory controller, the selected die having received one of the chip select signals that is different from any of the other ones of the chip select signals.

2. The memory module of claim 1, wherein the control die configures the data signal conduits to control data bus time slots for the respective bits of the one or more data signals.

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3. The memory module of claim 1, wherein the control die includes a data path control circuit that configures the data signal conduits in accordance with the control signals.

4. The memory module of claim 1, wherein the control signals include command/address signals, wherein the control die includes command/address buffers to control the timing of the command/address signals in the control signals.

5. The memory module of claim 4, wherein the command/address buffers comprise latches.

6. The memory module of claim 1, wherein the data signal conduits include data buffers to control the timing of the respective bits of the one or more data signals.

7. The memory module of claim 6, wherein control die configures the data signal conduits to control data bus time slots for the respective bits of the one or more data signals.

8. The memory module of claim 1, wherein the array dies include DDR DRAM, SDRAM, flash memory, or SRAM.

9. The memory module of claim 1, wherein the control dies is configured to decode the control signals to obtain command/address signals for providing to the array dies.

10. The memory module of claim 1, wherein the control signals include decoded command/address signals, and wherein the control die is configured to pass the command/address signals through to the stacked array dies.

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MEMORY MODULE WITH PACKAGES OF STACKED MEMORY CHIPS

ABSTRACT OF THE DISCLOSURE

A memory module is operable in a computer system to communicate with a system memory controller via a command/address bus and a data bus. The memory module comprises a register device coupled to the command/address bus, and a plurality of DRAM packages coupled to the data bus and to the register device via a set of module control lines. Each respective DRAM package comprises stacked array dies and a control die. The control die includes data signal conduits and control signal conduits. In response to the memory module receiving a set of command/address signals from the system memory controller, the register device outputs control signals, and the control die configures the data signal conduits in accordance with the control signals to enable respective bits of one or more data signals to be communicated between a selected die among the stacked dies and the system memory controller.

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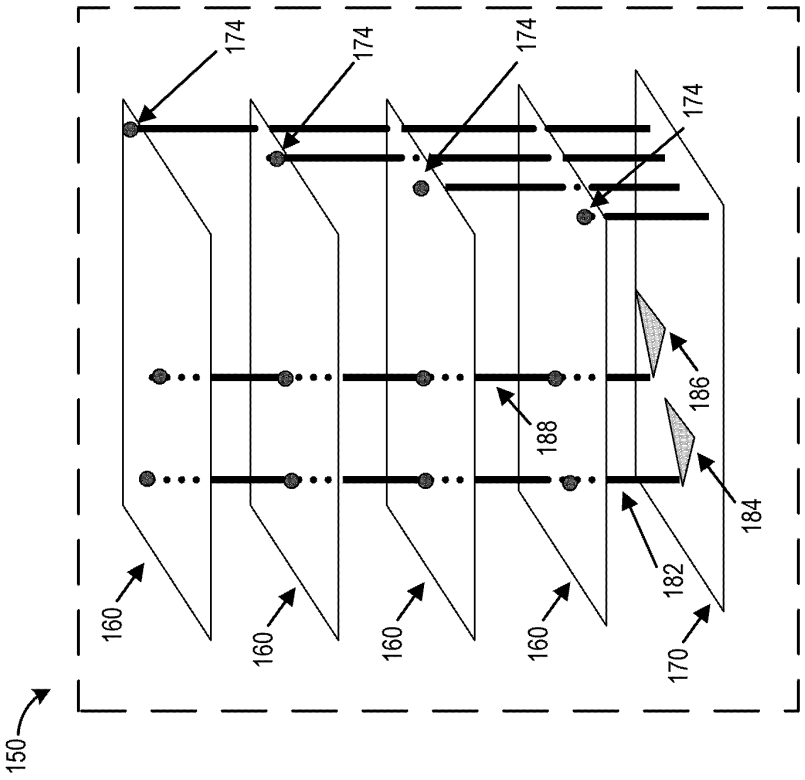

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FIG. 1B

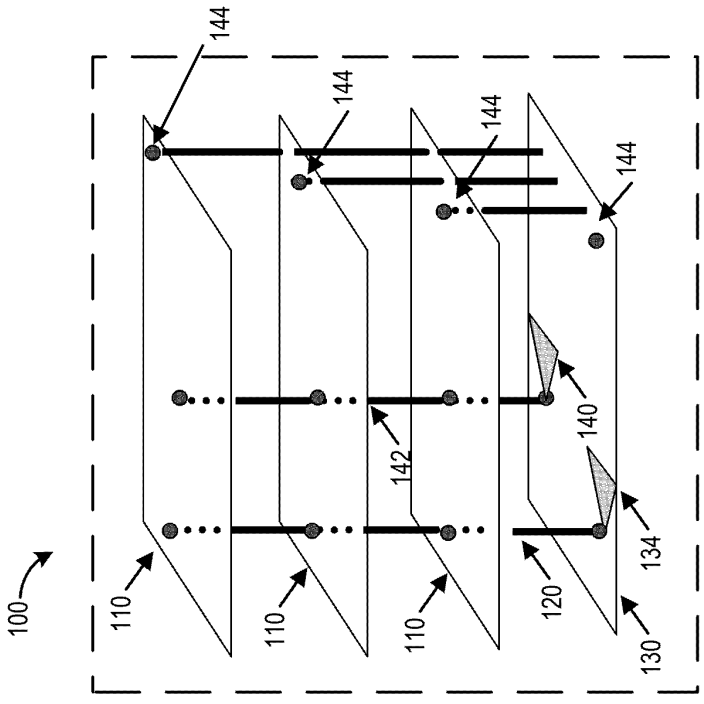

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FIG. 1A

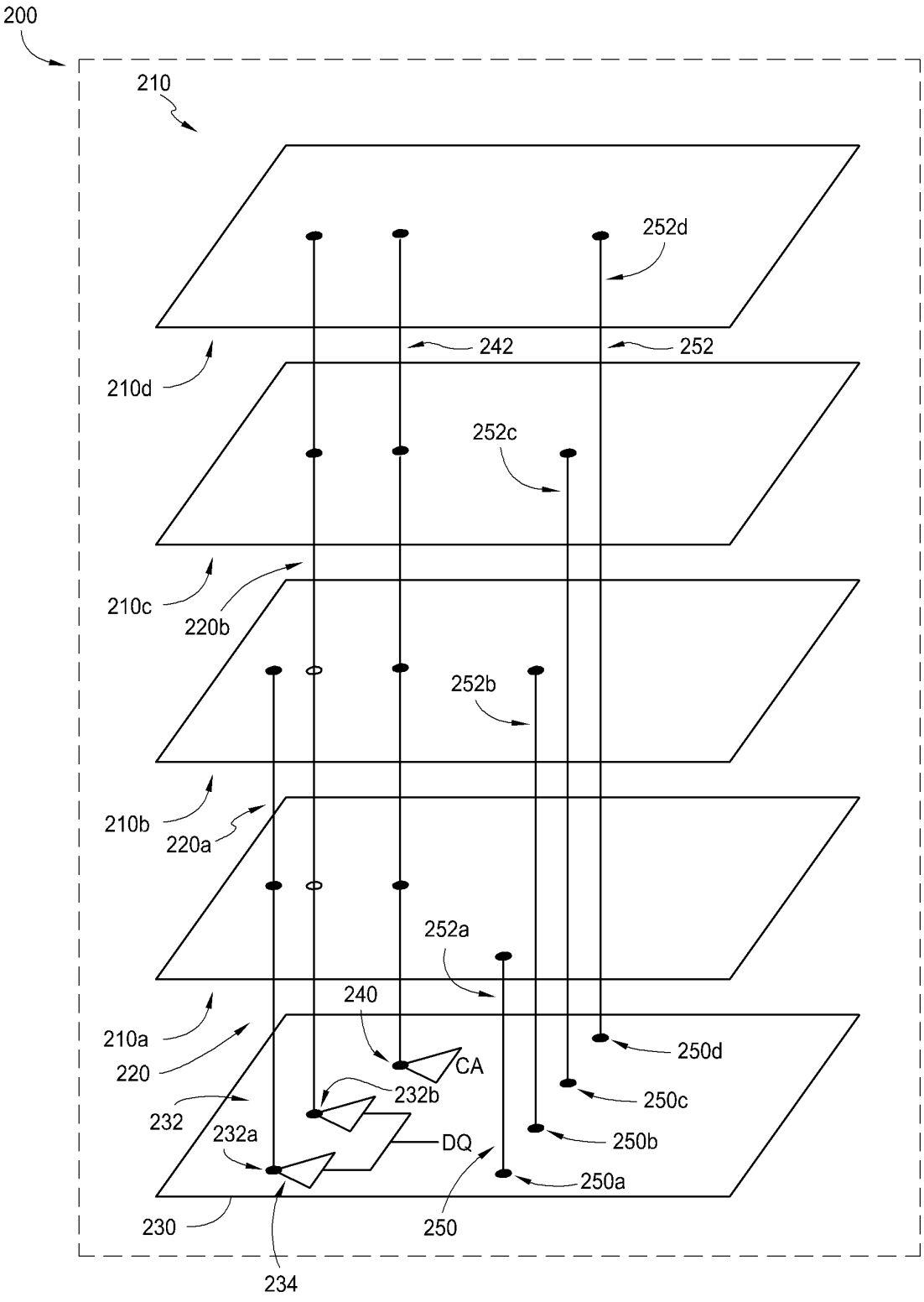

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FIG. 2

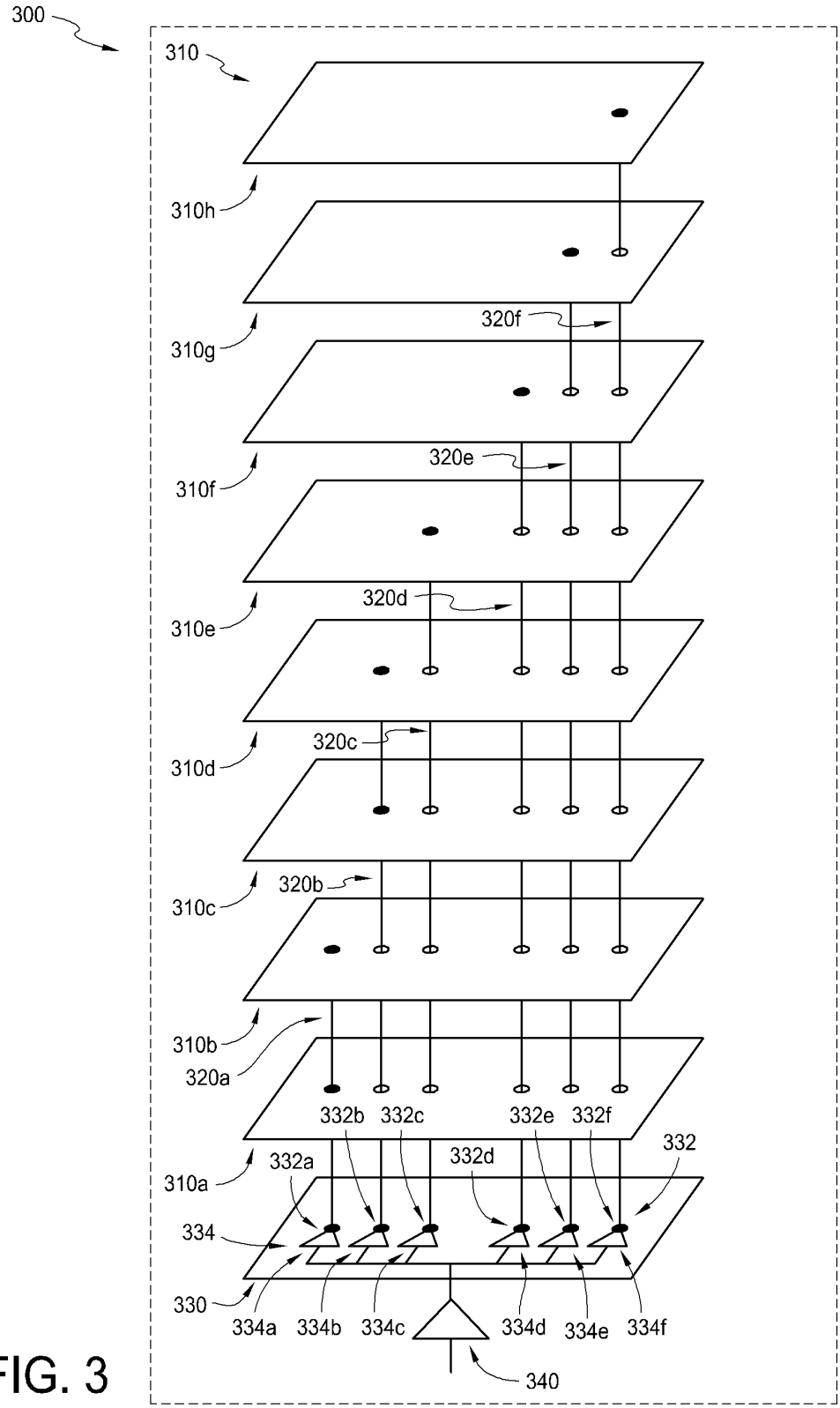

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FIG. 3

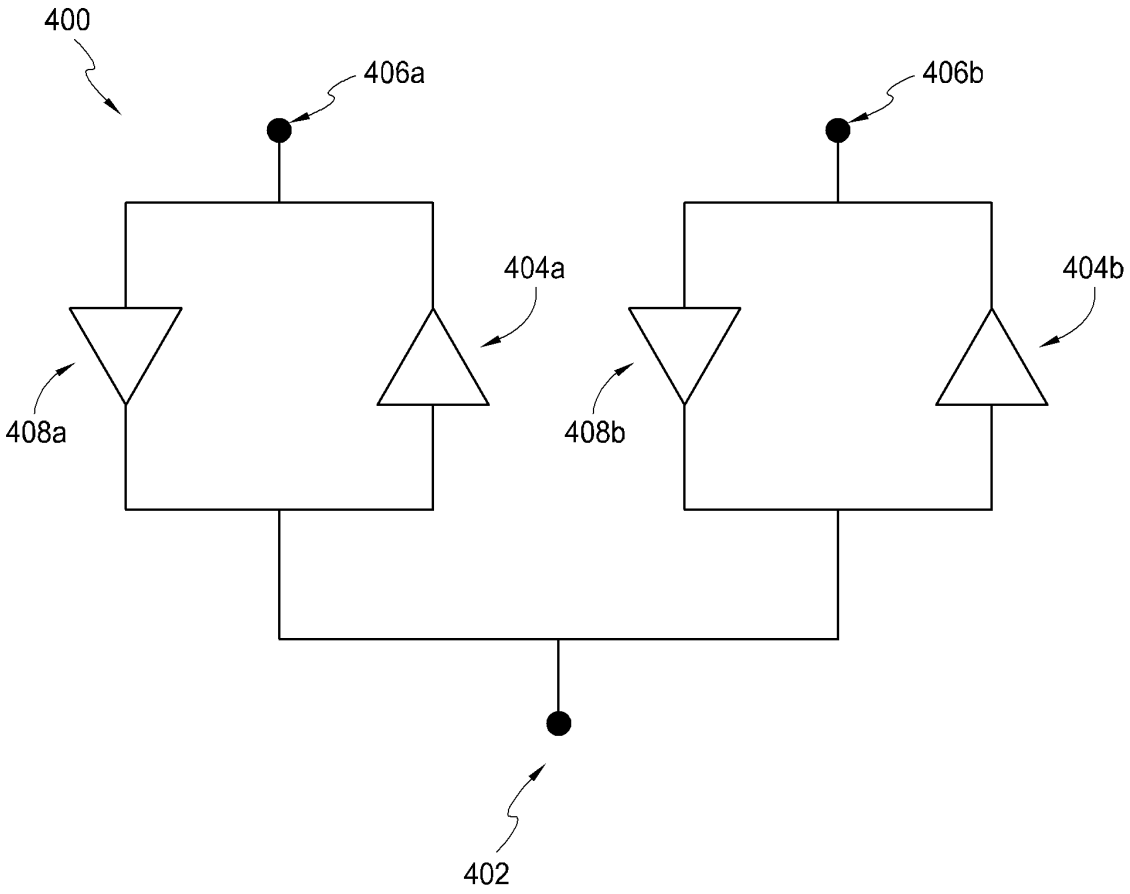


FIG. 4

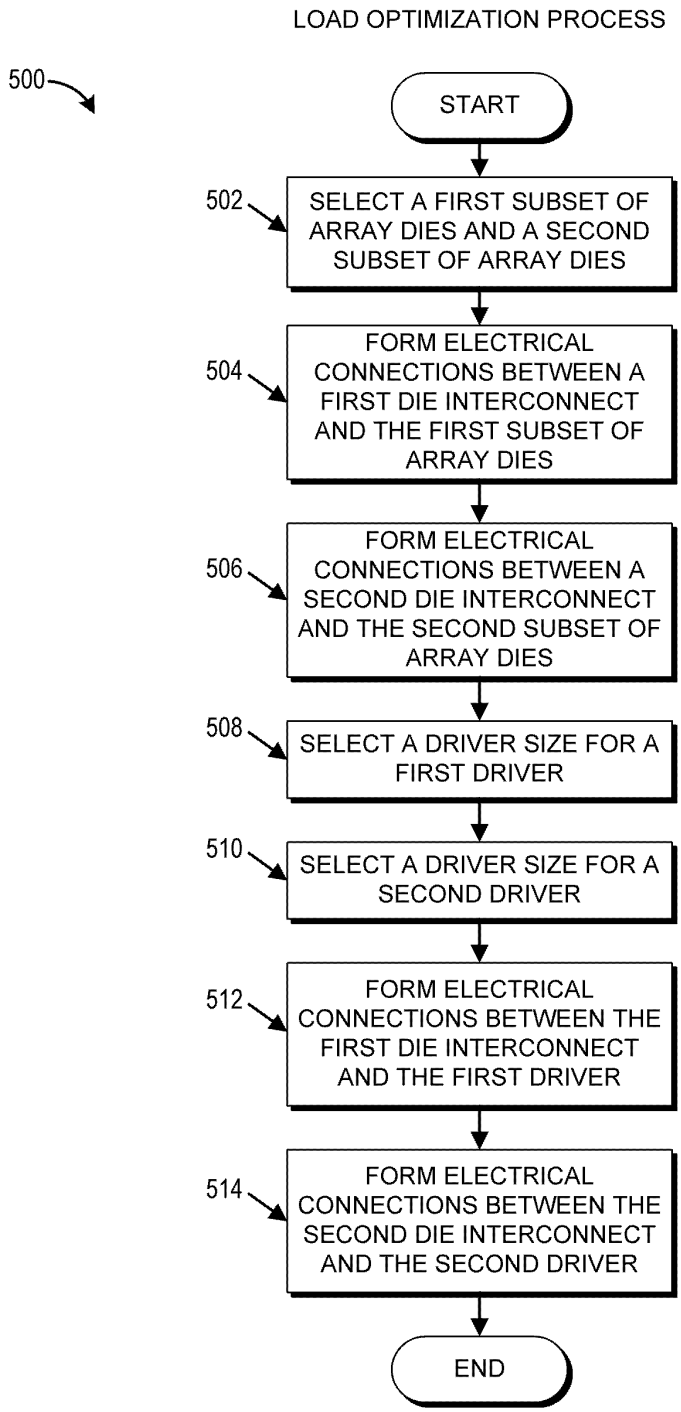

LOAD OPTIMIZATION PROCESS
500
START
502
SELECT A FIRST SUBSET OF ARRAY DIES AND A SECOND SUBSET OF ARRAY DIES
504
FORM ELECTRICAL CONNECTIONS BETWEEN A FIRST DIE INTERCONNECT AND THE FIRST SUBSET OF ARRAY DIES
506
FORM ELECTRICAL CONNECTIONS BETWEEN A SECOND DIE INTERCONNECT AND THE SECOND SUBSET OF ARRAY DIES
508
SELECT A DRIVER SIZE FOR A FIRST DRIVER
510
SELECT A DRIVER SIZE FOR A SECOND DRIVER
512
FORM ELECTRICAL CONNECTIONS BETWEEN THE FIRST DIE INTERCONNECT AND THE FIRST DRIVER
514
FORM ELECTRICAL CONNECTIONS BETWEEN THE SECOND DIE INTERCONNECT AND THE SECOND DRIVER
END

FIG. 5

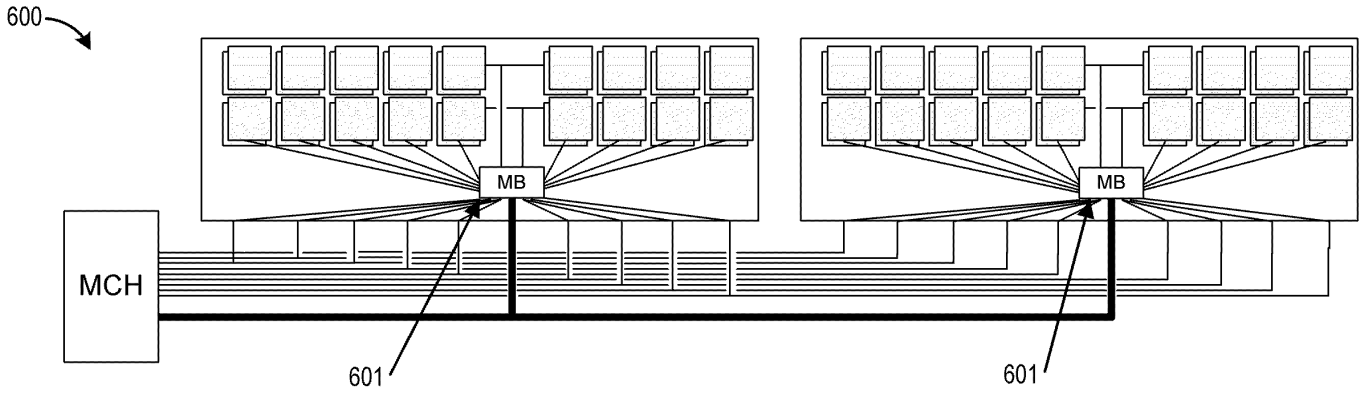


FIG. 6A

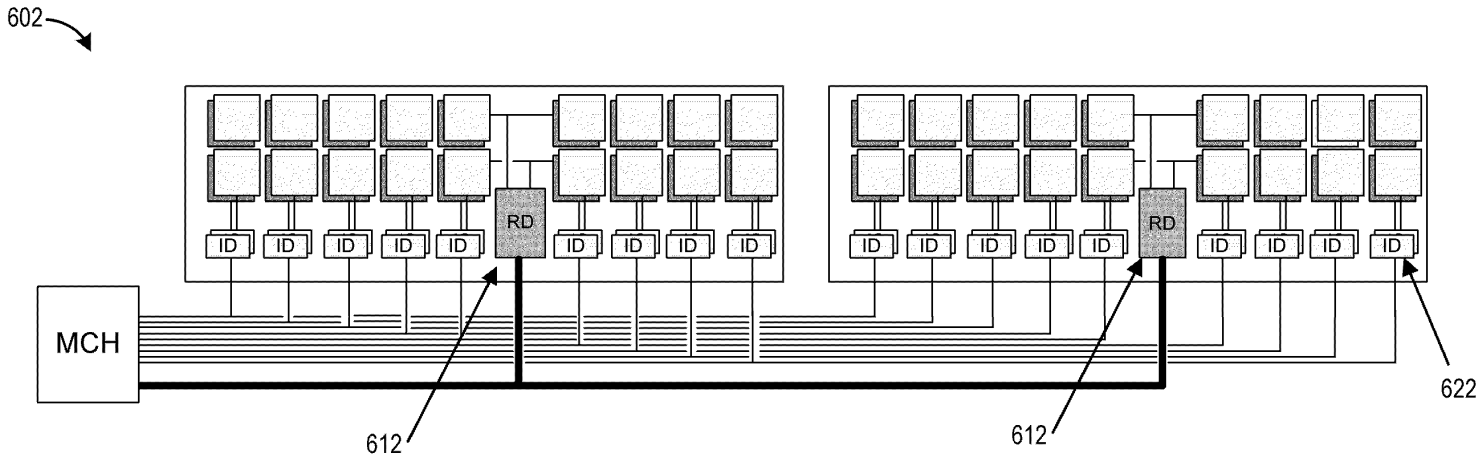


FIG. 6B

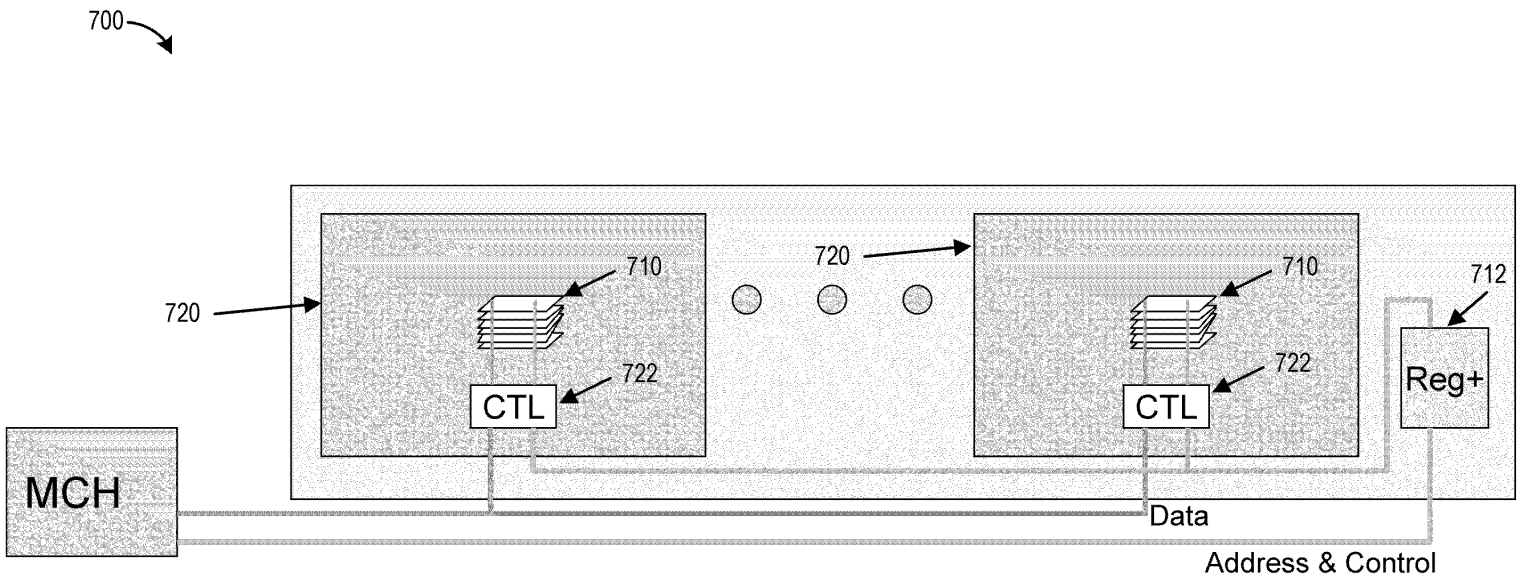

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CTL
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Reg+
MCH
Data
Address & Control

FIG. 7

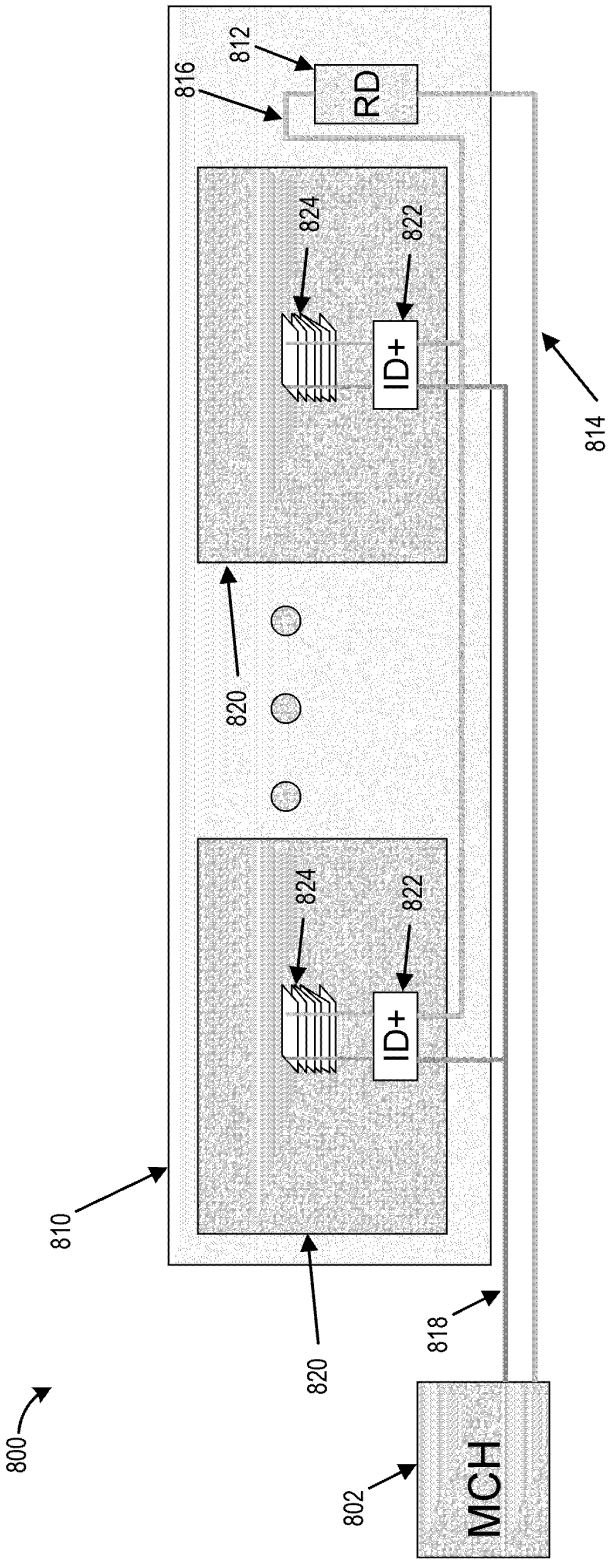


FIG. 8

Customer No. 79141
Attorney Docket No.: NETL.071C1

COMBINED DECLARATION AND ASSIGNMENT FOR UTILITY OR DESIGN APPLICATION

Title of Invention	MEMORY PACKAGE WITH OPTIMIZED DRIVER LOAD AND METHOD OF OPERATION

DECLARATION

As a below named inventor, I hereby declare that:

This declaration is directed to:

☐ The attached application, or

■ United States application or PCT international application number 14/337,168 filed on July 21, 2014.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

Note to Inventor: 37 C.F.R. § 1.63(c) states: "A person may not execute an oath or declaration for an application unless that person has reviewed and understands the contents of the application, including the claims, and is aware of the duty to disclose to the Office all information known to the person to be material to patentability as defined in § 1.56."

First Inventor (Legal Name): Hyun Lee

Signature: _____ Date: 3/2/2016

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	MEMORY MODULE WITH PACKAGES OF STACKED MEMORY CHIPS
First Named Inventor/Applicant Name:	Hyun Lee
Filer:	Jamie Jie Zheng
Attorney Docket Number:	N3044.10015US05

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY APPLICATION FILING	1011	1	280	280
UTILITY SEARCH FEE	1111	1	600	600
UTILITY EXAMINATION FEE	1311	1	720	720
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1600**

Electronic Acknowledgement Receipt

EFS ID:	29281502
Application Number:	15602099
International Application Number:	
Confirmation Number:	1757
Title of Invention:	MEMORY MODULE WITH PACKAGES OF STACKED MEMORY CHIPS
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	N3044.10015US05
Receipt Date:	22-MAY-2017
Filing Date:	
Time Stamp:	23:50:27
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$1600
RAM confirmation Number	052317INTEFSW23570400
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	2017-05-22_Appl_Data_Sheet_NETL071C3.pdf	1819477 48d892f2cfbf4f61e1bae8ea24d43b4c343a7849	no	7
Warnings:					
Information:					
2		2017-05-22_Specification_NETL071C3.pdf	756490 2c765dd83d5452fa72cc6c6b23c6bce930264c1a	yes	39
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Specification		1	36	
	Claims		37	38	
	Abstract		39	39	
Warnings:					
Information:					
3	Drawings-only black and white line drawings	2017-05-22_Drawings_NETL071C3.pdf	674388 3221d1d55f8a60dcd90de02cad04dc116652e6ed	no	8
Warnings:					
Information:					
4	Oath or Declaration filed	2016-03-02_Declaration_NETL071C1.pdf	89942 80b31bbb5e8c04a45c6fbdb128d9c8a6172462e5	no	1
Warnings:					
The page size in the PDF is too large. The pages should be 8.5 x 11 or A4. If this PDF is submitted, the pages will be resized upon entry into the Image File Wrapper and may affect subsequent processing					
Information:					

5	Fee Worksheet (SB06)	fee-info.pdf	34946 daa9ed4d0adf9bfbea4602d18a2dbd2899f8c640	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	3375243	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 15/602,099

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	600
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720
TOTAL CLAIMS (37 CFR 1.16(i))	10 minus 20 =	*			OR	x 80 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1 minus 3 =	*				x 420 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1600

APPLICATION AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)		RATE($)	ADDITIONAL FEE($)
Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
15/602,099	05/22/2017	2827	1600	NETL.071C3	10	1

CONFIRMATION NO. 1757

FILING RECEIPT

79141
Jamie J. Zheng, Ph.D Esq.
MASCHOFF BRENNAN
1389 Center Drive
Suite 300
Park City, UT 84098

Date Mailed: 06/01/2017

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Hyun Lee, Ladera Ranch, CA;

Applicant(s)

Netlist, Inc., Irvine, CA;

Power of Attorney: None

Domestic Priority data as claimed by applicant

This application is a CON of 15/095,288 04/11/2016 PAT 9659601
which is a CON of 14/337,168 07/21/2014 PAT 9318160
which is a CON of 13/288,850 11/03/2011 PAT 8787060
which claims benefit of 61/409,893 11/03/2010

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: No

Permission to Access Search Results: No

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 05/30/2017

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 15/602,099**

Projected Publication Date: 09/07/2017

Non-Publication Request: No

Early Publication Request: No

Title

MEMORY MODULE WITH PACKAGES OF STACKED MEMORY CHIPS

Preliminary Class

365

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

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The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

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United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/602,099	05/22/2017	Hyun Lee	N3044.10015US05	1757

79141 7590 07/27/2017

Jamie J. Zheng, Ph.D Esq.
MASCHOFF BRENNAN
1389 Center Drive
Suite 300
Park City, UT 84098

EXAMINER
HOANG, HUAN

ART UNIT	PAPER NUMBER
2827	

NOTIFICATION DATE	DELIVERY MODE
07/27/2017	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

d@mabr.com
bisraelsen@mabr.com

Office Action Summary	Application No. 15/602,099	Applicant(s) LEE, HYUN	
	Examiner HUAN HOANG	Art Unit 2827	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05/22/17*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-10* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-10* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *05/22/17* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of 35 U.S.C. 112(b):
(b) CONCLUSION.—The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention.

The following is a quotation of 35 U.S.C. 112 (pre-AIA), second paragraph:
The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 9 is rejected under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor, or for pre-AIA the applicant regards as the invention.

Claim 9 recites the limitation "the control dies" in line 1. There is insufficient antecedent basis for this limitation in the claim.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the “right to exclude” granted by a patent

and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on nonstatutory double patenting provided the reference application or patent either is shown to be commonly owned with the examined application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. See MPEP § 717.02 for applications subject to examination under the first inventor to file provisions of the AIA as explained in MPEP § 2159. See MPEP §§ 706.02(l)(1) - 706.02(l)(3) for applications not subject to examination under the first inventor to file provisions of the AIA. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO Internet website contains terminal disclaimer forms which may be used. Please visit www.uspto.gov/patent/patents-forms. The filing date of the application in which the form is filed determines what form (e.g., PTO/SB/25, PTO/SB/26,

PTO/AIA/25, or PTO/AIA/26) should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp.

Claims 1-10 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1, 5-7 and 12-15 of U.S. Patent No. 9,659,601. Although the claims at issue are not identical, they are not patentably distinct from each other because claims 1-10 are anticipated by claims 1, 5-7 and 12-15 of the patent.

Regarding claim 1: Claim 1 of the patent recites a memory module operable in a computer system to communicate with a system memory controller via a command/address bus and a data bus, comprising:

a register device to receive command/address signals from the system memory controller via the command/address bus and to output control signals in response to the input command/address signals (claim 1, lines 3-6), the control signals including chip-select signals (claim 5); and

a plurality of DRAM packages coupled to the register device via a set of module control lines, each respective DRAM package comprising:

control terminals coupled to the module control lines via which the each respective DRAM package receives the control signals from the register device, and data terminals coupled to a respective section of the data bus via which the each respective DRAM package communicates with the system memory controller respective

bits of one or more data signals associated with the command/address signals (claim 1, lines 9-13);

stacked array dies (claim 1, line 12);

a control die including data signal conduits coupled to the data terminals and control signal conduits coupled to the control terminals, the control signal conduits including chip-select conduits for receiving the chip select signals and providing respective ones of the chip select signals to respective ones of the stacked array dies (claim 5 of the patent); and

die interconnects including first die interconnects coupled to the data signal conduits and second die interconnects coupled to the control signal conduits, at least one of the first die interconnects is coupled to at least two of the stacked array dies (claim 1, lines 19-23); and

wherein the control die configures the data signal conduits in accordance with the control signals to enable the respective bits of the one or more data signals to be communicated between a selected die among the stacked dies and the system memory controller, the selected die having received one of the chip select signals that is different from any of the other ones of the chip select signals (claim 1, lines 24-34).

Regarding claim 2: Claim 1 of the patent recites the memory module of claim 1, wherein the control die configures the data signal conduits to control data bus time slots for the respective bits of the one or more data signals (claim 1, lines 24-34 and claim 6).

Regarding claim 3: Claim 1 of the patent recites the memory module of claim 1, wherein the control die includes a data path control circuit (first and second drivers) that configures the data signal conduits in accordance with the control signals.

Regarding claim 4: Claim 7 of the patent recites the memory module of claim 1, wherein the control signals include command/address signals, wherein the control die includes command/address buffers to control the timing of the command/address signals in the control signals.

Regarding claim 5: Claim 12 recites the memory module of claim 4, wherein the command/address buffers comprise latches.

Regarding claim 6: Claim 7 recites the memory module of claim 1, wherein the data signal conduits include data buffers to control the timing of the respective bits of the one or more data signals.

Regarding claim 7: Claim 8 of the patent recites the memory module of claim 6, wherein control die configures the data signal conduits to control data bus time slots for the respective bits of the one or more data signals.

Regarding claim 8: Claim 13 of the patent recites the memory module of claim 1, wherein the array dies include DDR DRAM, SDRAM, flash memory, or SRAM.

Regarding 9: Claim 14 of the patent recites the memory module of claim 1, wherein the control dies is configured to decode the control signals to obtain command/address signals for providing to the array dies.

Regarding claim 10: Claim 15 recites the memory module of claim 1, wherein the control signals include decoded command/address signals, and wherein the control die is configured to pass the command/address signals through to the stacked array dies.

4. Claims 1-10 rejected on the ground of nonstatutory double patenting as being unpatentable over claims 10-20 of U.S. Patent No. 9,318,160. Although the claims at issue are not identical, they are not patentably distinct from each other because it would have been obvious to one of ordinary skill in the art to recognize that there are chip-select conduits for receiving the chip select signals in claim 5 of the patent and the array dies include DDR DRAM.

5. Claims 1-10 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 29-34 of U.S. Patent No. 8,787,060. Although the claims at issue are not identical, they are not patentably distinct from each other because it would have been obvious to one of ordinary skill in the art to recognize that claims 1-10 recites all the limitations similar to those of the claims 29-34 of the patent and the memory module of claims 1-10 of the instant application and the memory module of claims 29-34 of the patent are identical in structure; therefore, the array dies include DDR RAM.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to HUAN HOANG whose telephone number is (571)272-1779. The examiner can normally be reached on Tues-Fri 8:30AM-7:00PM.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/HUAN HOANG/
Primary Examiner, Art Unit 2827

Notice of References Cited	Application/Control No. 15/602,099	Applicant(s)/Patent Under Reexamination LEE, HYUN	
	Examiner HUAN HOANG	Art Unit 2827	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-9,659,601 B2	05-2017	Lee; Hyun	G11C5/06	1/1
*	B	US-9,318,160 B2	04-2016	Lee; Hyun	G11C5/06	1/1
*	C	US-8,787,060 B2	07-2014	Lee; Hyun	G11C5/06	365/51
	D	US-				
	E	US-				
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15602099	LEE, HYUN
	Examiner	Art Unit
	HUAN HOANG	2827

CPC- SEARCHED		
Symbol	Date	Examiner
G11C 5/066, G11C 5/06, G11C 7/1057, G11C 7/1084, G11C 7/12	7/22/17	HH

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
365	63	7/22/17	HH

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

SEARCH NOTES		
Search Notes	Date	Examiner
EAST (text search)	7/22/17	HH

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

	/HUAN HOANG/ Primary Examiner.Art Unit 2827

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	19117	(g11c5/066 g11c5/06 g11c7/1057 g11c7/1084 g11c7/12).cpc. 365/63.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2017/07/22 16:43
L3	208	1 and register with address$3 with (chip adj select chip-select cs ce)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2017/07/22 16:45
L4	169	3 and (dram dynamic adj ram dynamic adj random)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2017/07/22 16:45
L5	39	4 and (dram dynamic adj ram dynamic adj random) with (die dice ic integrated adj circuit)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2017/07/22 16:46
L6	21	5 and stack$3 with (die dice ic integrated adj circuit)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2017/07/22 16:46
L7	18	6 and (die ic integrated adj circuit) with (chip-select chip adj select ce cs)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2017/07/22 16:51
L8	6	7 and conduit	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2017/07/22 16:59
L9	8	5 and (dram dynamic adj ram dynamic adj random) with stack$3 with (die dice ic integrated adj circuit)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2017/07/22 17:44
L10	8	9 and interconnect$3	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2017/07/22 17:45
L11	8	10 and control$4 with (die ic integrated adj circuit)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2017/07/22 17:45
L12	8	10 and control$4 near3 (die ic integrated adj circuit)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2017/07/22 17:45
S1	9317	(memory stor$3) and register with address$3 with (chip adj seclect$3 cs ce chip-select)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2017/07/22 09:27
S2	2460	S1 and (dynamic adj ram dynamic adj random adj access dram)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2017/07/22 09:28
S3	108	S2 and stack$3 with (die dice ic integrated adj circuit)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2017/07/22 09:30
S4	74	S3 and control$4 with (die dice ic integrated adj circuit)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2017/07/22 09:30
S5	29	S4 and (die dice ic integrated adj	US-PGPUB;	OR	ON	2017/07/22

		circuit) with interconnect$3	USPAT; EPO; JPO; DERWENT			09:31
S6	11	S4 and (die dice ic integrated adj circuit) with interconnect$3 with data	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2017/07/22 09:32

EAST Search History (Interference)

< This search history is empty>

7/ 22/ 2017 5:49:02 PM

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15602099	LEE, HYUN
	Examiner	Art Unit
	HUAN HOANG	2827

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	07/22/2017								
	1	✓								
	2	✓								
	3	✓								
	4	✓								
	5	✓								
	6	✓								
	7	✓								
	8	✓								
	9	✓								
	10	✓								

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/602,099	05/22/2017	Hyun Lee	N3044.10015US05

CONFIRMATION NO. 1757

79141
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PUBLICATION NOTICE

OC000000093912214

Title:MEMORY MODULE WITH PACKAGES OF STACKED MEMORY CHIPS

Publication No.US-2017-0256291-A1
Publication Date:09/07/2017

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Public Records Division. The Public Records Division can be reached by telephone at (571) 272-3150 or (800) 972-6382, by facsimile at (571) 273-3250, by mail addressed to the United States Patent and Trademark Office, Public Records Division, Alexandria, VA 22313-1450 or via the Internet.

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Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Netlist, Inc.
App. No.	:	15/095,288
Filed	:	July 27, 2017
For	:	Memory Module with Packages of Stacked Memory Chips
Examiner	:	HOANG, HUAM
Art Unit	:	2827
Conf. No.	:	1751
Docket No.	:	N3044.10015US05

CERTIFICATE OF EFS WEB TRANSMISSION

I hereby certify that this correspondence and any other attachment noted on the Automated Acknowledgement Receipt, is being transmitted from within the Pacific Time zone to the Commissioner for Patents via the EFS Web Server on:

December 27, 2017

(Date)

/Jamie J. Zheng/

Jamie J. Zheng, Reg. No. 51167

AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This submission is in response to the Non-Final Office Action dated July 27, 2017 for the above-identified patent application.

Applicant hereby petitions for a 2-month extension of time to respond to the above-referenced Office Action.

The Commissioner is hereby authorized to charge any required fee(s) to Deposit Account No. 50-5394.

AMENDMENTS to the CLAIMS begin on Page 2 of this paper.

REMARKS begin on Page 8 of this paper.

IN THE CLAIMS:

1. **(Currently Amended)** A memory module operable in a computer system to communicate with a system memory controller via a command/address bus and a data bus, comprising:

a register device configured to receive command/address signals from the system memory controller via the command/address bus and to output control signals in response to the input command/address signals, the control signals including chip-select signals; and

a plurality of DRAM packages coupled to the register device and configured to receive the control signals via a set of module control lines, each respective DRAM package comprising:

control terminals coupled to corresponding signal lines in the set of module control lines ~~via which the each respective DRAM package receives the control signals from the register device~~, and data terminals coupled to a respective section of the data bus ~~via which the each respective DRAM package communicates with the system memory controller respective bits of one or more data signals associated with the command/address signals~~;

stacked array dies;

a control die including data signal conduits coupled to the data terminals and control signal conduits coupled to the control terminals, the control signal conduits including chip-select conduits for receiving the chip select signals and providing respective ones of the chip select signals to respective ones of the stacked array dies; and

die interconnects including first die interconnects coupled to the data signal conduits and second die interconnects coupled to the control signal conduits, each of at least ~~one~~ a subset of the first die interconnects is coupled to at least two of the stacked array dies; and

wherein the control die is configured to control ~~configures~~ the data signal conduits in accordance with the control signals to enable the each respective DRAM package to communicate a respective set of bits of ~~the~~ one or more data signals ~~to be communicated~~ between a selected die among the stacked dies and the system memory controller, the

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selected die having received one of the chip select signals that is different from any of the other ones of the chip select signals.

2. **(Currently Amended)** The memory module of claim 1, wherein the control die ~~configures~~ is configured to control the data signal conduits so as to control one or more data bus time slots for the respective set of bits of the one or more data signals.

3. **(Currently Amended)** The memory module of claim 1, wherein the control die includes a data path timing controller configured to control timing of the respective set of bits of the one or more data signals ~~control circuit that configures the data signal conduits~~ in accordance with the control signals.

4. **(Currently Amended)** The memory module of claim 1, wherein the control signals include command/address signals, wherein the control die includes command/address buffers to control the timing of the command/address signals ~~in the control signals~~.

5. **(Original)** The memory module of claim 4, wherein the command/address buffers comprise latches.

6. **(Currently Amended)** The memory module of claim 1, wherein the data signal conduits include data buffers configured to control the timing of the respective set of bits of the one or more data signals.

7. **(Currently Amended)** The memory module of claim 6, wherein control die is configured to control ~~configures~~ the data signal conduits so as to control data bus time slots for the respective set of bits of the one or more data signals.

8. **(Original)** The memory module of claim 1, wherein the array dies include DDR DRAM, SDRAM, flash memory, or SRAM.

9. **(Currently Amended)** The memory module of claim 1, wherein the control die ~~dies~~ is configured to decode the control signals to obtain command/address signals for providing to the array dies.

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10. **(Original)** The memory module of claim 1, wherein the control signals include decoded command/address signals, and wherein the control die is configured to pass the command/address signals through to the stacked array dies.

11. **(New)** The memory module of claim 1, wherein the data signal conduits include a first data signal conduit having a first total capacitive load and a second data signal conduit having a second total capacitive load that is different from the first total capacitive load, and wherein the first data signal conduit includes a first driver having a first driver size corresponding to the first total capacitive load, and the second data signal conduit includes a second driver having a second driver size corresponding to the second total capacitive load, the second driver size being different from the first driver size.

12. **(New)** The memory module of claim 1, wherein the data signal conduits include a first data signal conduit coupled to a first subset of the stacked array dies and a second data signal conduit coupled to a second subset of the stacked array dies, wherein the first data signal conduit has a first total capacitive load and the second data signal conduit has a second total capacitive load that is substantially the same as the first total capacitive load.

13. **(New)** A memory module operable in a computer system to communicate with a system memory controller via a command/address bus and a data bus, comprising:

a register device configured to receive input command/address signals from the system memory controller via the command/address bus and to output control signals in response to the input command/address signals; and

a plurality of DRAM packages coupled to the register device to receive the control signals via a set of module control lines, each DRAM package comprising:

control terminals coupled to corresponding signal lines in the set of module control lines, and data terminals coupled to a section of the data bus corresponding to the each DRAM package;

stacked array dies;

a control die including data signal conduits coupled to the data terminals and control signal conduits coupled to the control terminals; and

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die interconnects including first die interconnects coupled to the data signal conduits and second die interconnects coupled to the control signal conduits, each of the first die interconnects is coupled to at least one of the stacked array dies; and

wherein the control die is configured to control the data signal conduits in accordance with the control signals to enable the each respective DRAM package to communicate a respective set of bits of one or more data signals between a selected die among the stacked dies and the system memory controller;

wherein the data signal conduits include a first data signal conduit having a first total capacitive load and a second data signal conduit having a second total capacitive load that is different from the first total capacitive load, and wherein the first data signal conduit includes a first driver having a first driver size corresponding to the first total capacitive load, and the second data signal conduit includes a second driver having a second driver size corresponding to the second total capacitive load, the second driver size being different from the first driver size.

14. **(New)** The memory module of claim 13, wherein the control die includes a data path timing controller configured to control timing of the respective set of bits of the one or more data signals.

15. **(New)** The memory module of claim 13, wherein the data signal conduits include data buffers configured to control the timing of the respective set of bits of the one or more data signals.

16. **(New)** The memory module of claim 13, wherein the array dies include DDR DRAM, SDRAM, flash memory, or SRAM.

17. **(New)** The memory module of claim 13, wherein the control die is configured to decode the control signals to obtain command/address signals for providing to the array dies.

18. **(New)** The memory module of claim 13, wherein the control signals include chip-select signals and the control signal conduits include chip-select conduits for receiving the chip select signals and providing respective ones of the chip select signals to respective ones of the stacked array dies, and wherein the selected die has received one of

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the chip select signals that is different from any of the other ones of the chip select signals

19. (**New**) A memory module operable in a computer system to communicate with a system memory controller via a command/address bus and a data bus, comprising:

a register device configured to receive input command/address signals from the system memory controller via the command/address bus and to output control signals in response to the input command/address signals; and

a plurality of DRAM packages coupled to the register device to receive the control signals via a set of module control lines, each DRAM package comprising:

control terminals coupled to corresponding signal lines in the set of module control lines, and data terminals coupled to a section of the data bus corresponding to the each DRAM package;

stacked array dies;

a control die including data signal conduits coupled to the data terminals and control signal conduits coupled to the control terminals; and

die interconnects including first die interconnects coupled to the data signal conduits and second die interconnects coupled to the control signal conduits, each of the first die interconnects is coupled to at least one of the stacked array dies; and

wherein the control die is configured to control the data signal conduits in accordance with the control signals to enable the each respective DRAM package to communicate a respective set of bits of one or more data signals between a selected die among the stacked dies and the system memory controller;

wherein the data signal conduits include a first data signal conduit coupled to a first subset of the stacked array dies and a second data signal conduit coupled to a second subset of the stacked array dies, wherein the first data signal conduit has a first total capacitive load and the second data signal conduit has a second total capacitive load that is substantially the same as the first total capacitive load;

wherein the control signals include chip-select signals and the control signal conduits include chip-select conduits for receiving the chip select signals and providing respective ones of the chip select signals to respective ones of the stacked array dies, and wherein the selected die has received one of the chip select signals that is different from any of the other ones of the chip select signals; and

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wherein the control die includes a data path timing controller configured to control timing of the respective set of bits of the one or more data signals in accordance with the control signals.

20. **(New)** The memory module of claim 19, wherein the control die is configured to decode the control signals to obtain command/address signals for providing to the array dies.

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REMARKS

This amendment responds to the Non-Final Office Action dated July 27, 2017. In the Office Action, the Examiner:

- rejected claim 9 under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), second paragraph; and
- rejected claims 1-10 on the ground of nonstatutory double patenting as being unpatentable over claims of U.S. Patent No. 9,659,601, U.S. Patent No. 9,318,160, and U.S. Patent No. 8,787,060.

I. CLAIM AMENDMENT

Claims 1-4, 6-7 and 9 are amended for clarity and to correct minor issues. New claims 11-20 are presented. Support for the new claims can be found throughout the specification and drawings of the present application, for example, in paragraphs [0062]-[0065]. Thus, no new matter is added.

II. REJECTION OF CLAIMS 1-10 ON THE GROUND OF NONSTATUTORY DOUBLE PATENTING

Applicant files herewith a Terminal Disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) to overcome the nonstatutory double patenting rejection of claims 1-10.

III. NEW CLAIMS

New claims 11-20 are believed to be patentable.

Applicant submits that claims 1-20 are in condition for allowance, and respectfully requests such action. The Examiner is invited to call the undersigned at (650) 521-4828 if such phone call would help resolve any remaining issues.

Respectfully submitted,

Date: December 27, 2017

/Jamie J. Zheng/ 51167

Jamie J. Zheng (Reg. No.)

Customer No. 79141

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Ex. 1008, p. 87

PTO/AIA/26 (04-14)
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TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT	Docket Number (Optional) N3044.10015US05

In re Application of: Hyun Lee

Application No.: 15/602,099

Filed: May 22, 2017

For: MEMORY MODULE WITH PACKAGES OF STACKED MEMORY CHIPS

The applicant, Netlist, Inc., owner of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of **prior patent** No. 8,787,060 as the term of said **prior patent** is presently shortened by any terminal disclaimer. The applicant hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the **prior patent** are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the applicant does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the **prior patent**, "as the term of said **prior patent** is presently shortened by any terminal disclaimer," in the event that said **prior patent** later:

expires for failure to pay a maintenance fee;
is held unenforceable;
is found invalid by a court of competent jurisdiction;
is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
has all claims canceled by a reexamination certificate;
is reissued; or
is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

Check either box 1 or 2 below, if appropriate.

1. ☐ The undersigned is the applicant. If the applicant is an assignee, the undersigned is authorized to act on behalf of the assignee.

I hereby acknowledge that any willful false statements made are punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

2. ☑ The undersigned is an attorney or agent of record. Reg. No. 51167

/Jaime J. Zheng/ — Signature
2017-12-27 — Date

Jaime J. Zheng — Typed or printed name

Attorney — Title
949-202-1901 — Telephone Number

☑ Terminal disclaimer fee under 37 CFR 1.20(d) included.

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TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT	Docket Number (Optional) N3044.10015US05

In re Application of: Hyun Lee

Application No.: 15/602,099

Filed: May 22, 2017

For: MEMORY MODULE WITH PACKAGES OF STACKED MEMORY CHIPS

The applicant, Netlist, Inc., owner of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of **prior patent** No. 9,318,160 as the term of said **prior patent** is presently shortened by any terminal disclaimer. The applicant hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the **prior patent** are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

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expires for failure to pay a maintenance fee;
is held unenforceable;
is found invalid by a court of competent jurisdiction;
is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
has all claims canceled by a reexamination certificate;
is reissued; or
is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

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/Jaime J. Zheng/ — Signature
2017-12-27 — Date

Jaime J. Zheng — Typed or printed name

Attorney — Title
949-202-1901 — Telephone Number

☑ Terminal disclaimer fee under 37 CFR 1.20(d) included.

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TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT

Docket Number (Optional)
N3044.10015US05

In re Application of: Hyun Lee

Application No.: 15/602,099

Filed: May 22, 2017

For: MEMORY MODULE WITH PACKAGES OF STACKED MEMORY CHIPS

The applicant, Netlist, Inc., owner of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of **prior patent** No. 9,659,601 as the term of said **prior patent** is presently shortened by any terminal disclaimer. The applicant hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the **prior patent** are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

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2. ☑ The undersigned is an attorney or agent of record. Reg. No. 51167

/Jaime J. Zheng/ — Signature
2017-12-27 — Date

Jaime J. Zheng — Typed or printed name

Attorney — Title
949-202-1901 — Telephone Number

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Electronic Patent Application Fee Transmittal

Application Number:	15602099
Filing Date:	22-May-2017
Title of Invention:	MEMORY MODULE WITH PACKAGES OF STACKED MEMORY CHIPS
First Named Inventor/Applicant Name:	Hyun Lee
Filer:	Jamie Jie Zheng/Maria Nadal
Attorney Docket Number:	N3044.10015US05

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension - 2 months with $0 paid	1252	1	600	600
Miscellaneous:				
STATUTORY OR TERMINAL DISCLAIMER	1814	1	160	160
		Total in USD ($)		**760**

Electronic Acknowledgement Receipt

EFS ID:	31348480
Application Number:	15602099
International Application Number:	
Confirmation Number:	1757
Title of Invention:	MEMORY MODULE WITH PACKAGES OF STACKED MEMORY CHIPS
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng/Maria Nadal
Filer Authorized By:	Jamie Jie Zheng
Attorney Docket Number:	N3044.10015US05
Receipt Date:	27-DEC-2017
Filing Date:	22-MAY-2017
Time Stamp:	19:41:40
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$760
RAM confirmation Number	122817INTEFSW19495700
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	N3044-10015US05_POA.pdf	293274 df3ef8cd1f1da5e8d3fc6a4710e163fe92d3ebde	no	5
Warnings:					
Information:					
2		N3044-100US05_RESPONSE_FOA.pdf	158634 4df969dd2f9f4aab5769d33a6a06d6325cf550bb	yes	8
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Response After Final Action		1	1	
	Claims		2	7	
	Applicant Arguments/Remarks Made in an Amendment		8	8	
Warnings:					
Information:					
3	Terminal Disclaimer Filed	N3044-10015US15_TERMINAL_DISCLAIMERS.pdf	241782 55d163a7c74accd48dfd859a9d4881c6651a9c09	no	3
Warnings:					
Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	32633 bd8ceea41176c2c17d8c02afc32e0290c67db2e6	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	726323		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B or equivalent) to identify the application to which the Power of Attorney directed, in accordance with 37 CFR 1.5. If the Power of Attorney by Applicant form is not accompanied by this transmittal form or an equivalent, the Power of Attorney will not be recognized in the application.

Application Number	15/602,099
Filing Date	May 22, 2017
First Named Inventor	Hyun Lee
Title	MEMORY MODULE WITH PACKAGES OF STACKED MEMORY CHIPS
Art Unit	2827
Examiner Name	Huan Hoang
Attorney Docket Number	N3044.10015US05

SIGNATURE of Applicant or Patent Practitioner

Signature	/Jaime J. Zheng/	2017-12-27 **Date**	2017-12-27
Name	Jaime J. Zheng	**Telephone**	(435) 252-1360
Registration Number	51167		

MASCHOFF BRENNAN, PLLC
1389 Center Drive, SUITE 300
PARK CITY, UTAH 84098, USA

GENERAL POWER OF ATTORNEY BY APPLICANT FOR UNITED STATES PATENT

I hereby revoke all previous powers of attorney given in the application referenced in the attached transmittal letter (form PTO/AIA/82A or equivalent).

I hereby appoint the practitioner associated with the following Customer Number :

79141

as my/our attorney or agent, and to transact all business in the United States Patent and Trademark Office in connection with the application referenced in the attached transmittal letter (form PTO/AIA/82A or equivalent).

Please recognize or change the **correspondence address** for the application referenced in the attached transmittal letter to the address associated with the above-mentioned **Customer Number**.

I am the Applicant:

- ☐ Inventor or Joint Inventor
- ☐ Legal Representative of a Deceased or Legally Incapacitated Inventor
- ■ Assignee or Person to Whom the Inventor is Under an Obligation to Assign
- ☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is currently being filed in this document)

SIGNATURE of Applicant for Patent

Signature		Date: January 9, 2013
Name	Gail Sasaki	
Title	Vice President and Chief Financial Officer	
Company	Netlist, Inc.	

Note: Signature - this form must be signed by the Applicant or a person authorized to act on behalf of Applicant.

Submit multiple forms for more than one signature
Total of ___ forms are submitted.

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STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: Hyun Lee

Application No./Patent No.: 15/602,099 Filed/Issue Date: 05/22/2017

Titled: Memory Module with Packages of Stacked Memory Chips

Netlist, Inc., a corporation

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☑ The assignee of the entire right, title, and interest.

2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):

☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

A. ☑ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 042475, Frame 0107, or for which a copy thereof is attached.

B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

2. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

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STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

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5. From: _____ To: _____

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6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☑ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Jamie J. Zheng/	2017-12-27
Signature	Date
Jaime J. Zheng	51167
Printed or Typed Name	Title or Registration Number

15/602,099	MEMORY MODULE WITH PACKAGES OF STACKED MEMORY CHIPS	N3044.10015US05 12-27-2017::15:18:04

Patent Assignment Abstract of Title

Total Assignments: 1

Application #: 15602099 **Filing Dt:** 05/22/2017 **Patent #:** NONE **Issue Dt:**

PCT #: NONE **Intl Reg #:** **Publication #:** US20170256291 **Pub Dt:** 09/07/2017

Inventor: Hyun Lee

Title: MEMORY MODULE WITH PACKAGES OF STACKED MEMORY CHIPS

Assignment: 1

Reel/Frame: 042475 / 0107 **Received:** 05/23/2017 **Recorded:** 05/23/2017 **Mailed:** 05/24/2017 **Pages:** 3

Conveyance: ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS).

Assignor: LEE, HYUN **Exec Dt:** 12/15/2011

Assignee: NETLIST, INC.
175 TECHNOLOGY, #150
IRVINE, CALIFORNIA 92618

Correspondent: JAMIE J. ZHENG/ MASCHOFF BRENNAN
1389 CENTER DRIVE
SUITE 300
PARK CITY, UT 84098

Search Results as of: 12/27/2017 15:17:49 PM

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If you have any comments or questions concerning the data displayed, contact OPR / Assignments at 571-272-3350

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 15/602,099	Filing Date 05/22/2017	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)		
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

		(Column 1)		(Column 2)	(Column 3)		
	12/27/2017	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
AMENDMENT	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0	X $80 =	0
AMENDMENT	Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X $420 =	0
AMENDMENT	☐ Application Size Fee (37 CFR 1.16(s))						
AMENDMENT	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)		
		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
AMENDMENT	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
AMENDMENT	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
AMENDMENT	☐ Application Size Fee (37 CFR 1.16(s))						
AMENDMENT	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/CHRISTINE MOLLISH/

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Alexandria, Virginia 22313-1450
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/602,099	05/22/2017	Hyun Lee	N3044.10015US05

CONFIRMATION NO. 1757

POA ACCEPTANCE LETTER

79141
Jamie J. Zheng, Ph.D Esq.
MASCHOFF BRENNAN
1389 Center Drive
Suite 300
Park City, UT 84098

OC00000096367385

Date Mailed: 12/29/2017

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 12/27/2017.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/qtran/

Application Number	Application/Control No.	Applicant(s)/Patent under Reexamination	
	15/602,099	LEE, HYUN	

Document Code - DISQ	Internal Document – DO NOT MAIL

TERMINAL DISCLAIMER	☒ APPROVED	☐ DISAPPROVED
Date Filed : 12/27/17	This patent is subject to a Terminal Disclaimer	

Approved/Disapproved by:
Felicia D. Roberts 8,787,060

U.S. Patent and Trademark Office

Application Number	Application/Control No.	Applicant(s)/Patent under Reexamination	
	15/602,099	LEE, HYUN	

Document Code - DISQ	Internal Document – DO NOT MAIL

TERMINAL DISCLAIMER	☐ APPROVED	☒ DISAPPROVED
Date Filed : 12/27/17	This patent is subject to a Terminal Disclaimer	

Approved/Disapproved by:

Felicia D. Roberts - 2 TDs disapproved with this filing date (9,318,160 and 9,659,601):

The disclaimer fee under 37 CFR 1.20(d) has not been submitted, nor is there any pre authorization in the application to charge to a deposit account. (See FP 14.24 and 14.26.07)

Note: The signing attorney is not an authorized person listed under the deposit number in the RAM system.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/602,099	05/22/2017	Hyun Lee	N3044.10015US05	1757

79141 7590 02/26/2018

Jamie J. Zheng, Ph.D Esq.
MASCHOFF BRENNAN
1389 Center Drive
Suite 300
Park City, UT 84098

EXAMINER
HOANG, HUAN

ART UNIT	PAPER NUMBER
2827	

NOTIFICATION DATE	DELIVERY MODE
02/26/2018	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

d@mabr.com
bisraelsen@mabr.com

Office Action Summary	Application No. 15/602,099	Applicant(s) LEE, HYUN	
	Examiner HUAN HOANG	Art Unit 2827	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/27/17*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-10* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-10* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

The amendment filed on 12/27/17 has been received and entered.

Terminal Disclaimer

1. The terminal disclaimer filed on 12/27/17 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of US Patent No. 8,787,060 has been reviewed and is accepted. The terminal disclaimer has been recorded.

2. The terminal disclaimer filed on 12/27/17 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of US 9,318,160 and 9,659,601 have been reviewed and is NOT accepted.

The disclaimer fee under 37 CFR 1.20(d) has not been submitted, nor is there any pre authorization in the application to charge to a deposit account. (See FP 14.24 and 14.26.07)

Note: The signing attorney is not an authorized person listed under the deposit number in the RAM system.

Double Patenting

3. Claims 1-10 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1, 5-7 and 12-15 of U.S. Patent No. 9,659,601. Although the claims at issue are not identical, they are not patentably distinct from each other because claims 1-10 are anticipated by claims 1, 5-7 and 12-15 of the patent.

Regarding claim 1: Claim 1 of the patent recites a memory module operable in a computer system to communicate with a system memory controller via a command/address bus and a data bus, comprising:

a register device to receive command/address signals from the system memory controller via the command/address bus and to output control signals in response to the input command/address signals (claim 1, lines 3-6), the control signals including chip-select signals (claim 5); and

a plurality of DRAM packages coupled to the register device via a set of module control lines, each respective DRAM package comprising:

control terminals coupled to the module control lines via which the each respective DRAM package receives the control signals from the register device, and data terminals coupled to a respective section of the data bus via which the each respective DRAM package communicates with the system memory controller respective bits of one or more data signals associated with the command/address signals (claim 1, lines 9-13);

stacked array dies (claim 1, line 12);

a control die including data signal conduits coupled to the data terminals and control signal conduits coupled to the control terminals, the control signal conduits including chip-select conduits for receiving the chip select signals and providing respective ones of the chip select signals to respective ones of the stacked array dies (claim 5 of the patent); and

die interconnects including first die interconnects coupled to the data signal conduits and second die interconnects coupled to the control signal conduits, at least one of the first die interconnects is coupled to at least two of the stacked array dies (claim 1, lines 19-23); and

wherein the control die configures the data signal conduits in accordance with the control signals to enable the respective bits of the one or more data signals to be communicated between a selected die among the stacked dies and the system memory controller, the selected die having received one of the chip select signals that is different from any of the other ones of the chip select signals (claim 1, lines 24-34).

Regarding claim 2: Claim 1 of the patent recites the memory module of claim 1, wherein the control die configures the data signal conduits to control data bus time slots for the respective bits of the one or more data signals (claim 1, lines 24-34 and claim 6).

Regarding claim 3: Claim 1 of the patent recites the memory module of claim 1, wherein the control die includes a data path control circuit (first and second drivers) that configures the data signal conduits in accordance with the control signals.

Regarding claim 4: Claim 7 of the patent recites the memory module of claim 1, wherein the control signals include command/address signals, wherein the control die

includes command/address buffers to control the timing of the command/address signals in the control signals.

Regarding claim 5: Claim 12 recites the memory module of claim 4, wherein the command/address buffers comprise latches.

Regarding claim 6: Claim 7 recites the memory module of claim 1, wherein the data signal conduits include data buffers to control the timing of the respective bits of the one or more data signals.

Regarding claim 7: Claim 8 of the patent recites the memory module of claim 6, wherein control die configures the data signal conduits to control data bus time slots for the respective bits of the one or more data signals.

Regarding claim 8: Claim 13 of the patent recites the memory module of claim 1, wherein the array dies include DDR DRAM, SDRAM, flash memory, or SRAM.

Regarding 9: Claim 14 of the patent recites the memory module of claim 1, wherein the control dies is configured to decode the control signals to obtain command/address signals for providing to the array dies.

Regarding claim 10: Claim 15 recites the memory module of claim 1, wherein the control signals include decoded command/address signals, and wherein the control die is configured to pass the command/address signals through to the stacked array dies.

4. Claims 1-10 rejected on the ground of nonstatutory double patenting as being unpatentable over claims 10-20 of U.S. Patent No. 9,318,160. Although the claims at issue are not identical, they are not patentably distinct from each other because it would have been obvious to one of ordinary skill in the art to recognize that there are chip-

select conduits for receiving the chip select signals in claim 5 of the patent and the array dies include DDR DRAM.

Response to Arguments

5. Applicant's arguments filed 12/27/17 have been fully considered but they are not persuasive.

The double patenting rejections are maintained because two Terminal Disclaimers are disapproved.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HUAN HOANG whose telephone number is (571)272-1779. The examiner can normally be reached on Tues-Fri 8:30AM-7:00PM.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/HUAN HOANG/
Primary Examiner, Art Unit 2827

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15602099	LEE, HYUN
	Examiner	Art Unit
	HUAN HOANG	2827

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	07/22/2017	02/20/2018							
	1	✓	✓							
	2	✓	✓							
	3	✓	✓							
	4	✓	✓							
	5	✓	✓							
	6	✓	✓							
	7	✓	✓							
	8	✓	✓							
	9	✓	✓							
	10	✓	✓							

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/602,099	05/22/2017	Hyun Lee	129980-5070US	1757

79141 7590 05/31/2018

Morgan Lewis Bockius LLP / Jamie Zheng Ph.D.
1400 Page Mill Road
Palo Alto, CA 94304

EXAMINER
HOANG, HUAN

ART UNIT	PAPER NUMBER
2827	

NOTIFICATION DATE	DELIVERY MODE
05/31/2018	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

padocketingdepartment@morganlewis.com
vskliba@morganlewis.com

Applicant-Initiated Interview Summary	Application No.	Applicant(s)	
	15/602,099	LEE, HYUN	
	Examiner	Art Unit	
	HUAN HOANG	2827	

All participants (applicant, applicant's representative, PTO personnel):

(1) *HUAN HOANG*. (3)_____.

(2) *JAMIE J. ZHENG*. (4)_____.

Date of Interview: *23 May 2018*.

Type: ☒ Telephonic ☐ Video Conference
☐ Personal [copy given to: ☐ applicant ☐ applicant's representative]

Exhibit shown or demonstration conducted: ☐ Yes ☒ No.
If Yes, brief description: _____.

Issues Discussed ☐101 ☐112 ☐102 ☐103 ☒Others
(For each of the checked box(es) above, please describe below the issue and detailed description of the discussion)

Claim(s) discussed: *11-20*.

Identification of prior art discussed: *N/A*.

Substance of Interview
(For each issue discussed, provide a detailed description and indicate if agreement was reached. Some topics may include: identification or clarification of a reference or a portion thereof, claim interpretation, proposed amendments, arguments of any applied references etc...)

Applcant's representative, Ms. Jamie J. Zheng, called the Examiner to notify that claims 11-20 had not been addressed in the last Office Action. The Exmaniner will consider to send a Letter Restarting Period for Response to correct the last Office Action.

Applicant recordation instructions: The formal written reply to the last Office action must include the substance of the interview. (See MPEP section 713.04). If a reply to the last Office action has already been filed, applicant is given a non-extendable period of the longer of one month or thirty days from this interview date, or the mailing date of this interview summary form, whichever is later, to file a statement of the substance of the interview

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

☒ Attachment

/HUAN HOANG/ Primary Examiner, Art Unit 2827	

Summary of Record of Interview Requirements

Manual of Patent Examining Procedure (MPEP), Section 713.04, Substance of Interview Must be Made of Record
A complete written statement as to the substance of any face-to-face, video conference, or telephone interview with regard to an application must be made of record in the application whether or not an agreement with the examiner was reached at the interview.

Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews
Paragraph (b)

In every instance where reconsideration is requested in view of an interview with an examiner, a complete written statement of the reasons presented at the interview as warranting favorable action must be filed by the applicant. An interview does not remove the necessity for reply to Office action as specified in §§ 1.111, 1.135. (35 U.S.C. 132)

37 CFR §1.2 Business to be transacted in writing.
All business with the Patent or Trademark Office should be transacted in writing. The personal attendance of applicants or their attorneys or agents at the Patent and Trademark Office is unnecessary. The action of the Patent and Trademark Office will be based exclusively on the written record in the Office. No attention will be paid to any alleged oral promise, stipulation, or understanding in relation to which there is disagreement or doubt.

The action of the Patent and Trademark Office cannot be based exclusively on the written record in the Office if that record is itself incomplete through the failure to record the substance of interviews.

It is the responsibility of the applicant or the attorney or agent to make the substance of an interview of record in the application file, unless the examiner indicates he or she will do so. It is the examiner's responsibility to see that such a record is made and to correct material inaccuracies which bear directly on the question of patentability.

Examiners must complete an Interview Summary Form for each interview held where a matter of substance has been discussed during the interview by checking the appropriate boxes and filling in the blanks. Discussions regarding only procedural matters, directed solely to restriction requirements for which interview recordation is otherwise provided for in Section 812.01 of the Manual of Patent Examining Procedure, or pointing out typographical errors or unreadable script in Office actions or the like, are excluded from the interview recordation procedures below. Where the substance of an interview is completely recorded in an Examiners Amendment, no separate Interview Summary Record is required.

The Interview Summary Form shall be given an appropriate Paper No., placed in the right hand portion of the file, and listed on the "Contents" section of the file wrapper. In a personal interview, a duplicate of the Form is given to the applicant (or attorney or agent) at the conclusion of the interview. In the case of a telephone or video-conference interview, the copy is mailed to the applicant's correspondence address either with or prior to the next official communication. If additional correspondence from the examiner is not likely before an allowance or if other circumstances dictate, the Form should be mailed promptly after the interview rather than with the next official communication.

The Form provides for recordation of the following information:
- Application Number (Series Code and Serial Number)
- Name of applicant
- Name of examiner
- Date of interview
- Type of interview (telephonic, video-conference, or personal)
- Name of participant(s) (applicant, attorney or agent, examiner, other PTO personnel, etc.)
- An indication whether or not an exhibit was shown or a demonstration conducted
- An identification of the specific prior art discussed
- An indication whether an agreement was reached and if so, a description of the general nature of the agreement (may be by attachment of a copy of amendments or claims agreed as being allowable). Note: Agreement as to allowability is tentative and does not restrict further action by the examiner to the contrary.
- The signature of the examiner who conducted the interview (if Form is not an attachment to a signed Office action)

It is desirable that the examiner orally remind the applicant of his or her obligation to record the substance of the interview of each case. It should be noted, however, that the Interview Summary Form will not normally be considered a complete and proper recordation of the interview unless it includes, or is supplemented by the applicant or the examiner to include, all of the applicable items required below concerning the substance of the interview.

A complete and proper recordation of the substance of any interview should include at least the following applicable items:
1) A brief description of the nature of any exhibit shown or any demonstration conducted,
2) an identification of the claims discussed,
3) an identification of the specific prior art discussed,
4) an identification of the principal proposed amendments of a substantive nature discussed, unless these are already described on the Interview Summary Form completed by the Examiner,
5) a brief identification of the general thrust of the principal arguments presented to the examiner,
   (The identification of arguments need not be lengthy or elaborate. A verbatim or highly detailed description of the arguments is not required. The identification of the arguments is sufficient if the general nature or thrust of the principal arguments made to the examiner can be understood in the context of the application file. Of course, the applicant may desire to emphasize and fully describe those arguments which he or she feels were or might be persuasive to the examiner.)
6) a general indication of any other pertinent matters discussed, and
7) if appropriate, the general results or outcome of the interview unless already described in the Interview Summary Form completed by the examiner.

Examiners are expected to carefully review the applicant's record of the substance of an interview. If the record is not complete and accurate, the examiner will give the applicant an extendable one month time period to correct the record.

Examiner to Check for Accuracy

If the claims are allowable for other reasons of record, the examiner should send a letter setting forth the examiner's version of the statement attributed to him or her. If the record is complete and accurate, the examiner should place the indication, "Interview Record OK" on the paper recording the substance of the interview along with the date and the examiner's initials.

Office Action Summary	Application No. 15/602,099	Applicant(s) LEE, HYUN	
	Examiner HUAN HOANG	Art Unit 2827	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *1* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/27/17*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-20* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-20* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *05/23/18* .

4) ☐ Other: _____.

The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

1. In response to applicant's telephone call on 05/23/18 regarding the last Office action, the following corrective action is taken.

The period for reply of 1 MONTHS set in said Office Action is restarted to begin with the mailing date of this letter.

The amendment filed on 12/27/17 has been received and entered.

Terminal Disclaimer

2. The terminal disclaimer filed on 12/27/17 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of US Patent No. 8,787,060 has been reviewed and is accepted. The terminal disclaimer has been recorded.

3. The terminal disclaimers filed on 12/27/17 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of US 9,318,160 and 9,659,601 have been reviewed and are NOT accepted.

The disclaimer fee under 37 CFR 1.20(d) has not been submitted, nor is there any pre authorization in the application to charge to a deposit account. (See FP 14.24 and 14.26.07)

Note: The signing attorney is not an authorized person listed under the deposit number in the RAM system.

Double Patenting

4. Claims 1-20 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1, 5-7 and 12-15 of U.S. Patent No. 9,659,601. Although the claims at issue are not identical, they are not patentably distinct from each other because claims 1-10 are anticipated by claims 1, 5-7 and 12-15 of the patent.

Regarding claim 1: Claim 1 of the patent recites a memory module operable in a computer system to communicate with a system memory controller via a command/address bus and a data bus, comprising:

a register device configured to receive command/address signals from the system memory controller via the command/address bus and to output control signals in response to the input command/address signals (claim 1, lines 3-6), the control signals including chip-select signals (claim 5); and

a plurality of DRAM packages coupled to the register device and configured to receive the control signals via a set of module control lines, each respective DRAM package comprising:

control terminals coupled to corresponding signal lines in the set of module control lines;

stacked array dies (claim 1, line 14);

a control die including data signal conduits coupled to the data terminals and control signal conduits coupled to the control terminals, the control signal conduits including chip-select conduits for receiving the chip select signals and providing respective ones of the chip select signals to respective ones of the stacked array dies (claim 5 of the patent); and

die interconnects including first die interconnects coupled to the data signal conduits and second die interconnects coupled to the control signal conduits, each of at least a subset of the first die interconnects is coupled to at least two of the stacked array dies (claim 1, lines 19-23); and

wherein the control die is configured to control the data signal conduits in accordance with the control signals to enable the each respective DRAM package to communicate a respective set of bits of one or more data signals between a selected die among the stacked dies and the system memory controller, the selected die having received one of the chip select signals that is different from any of the other ones of the chip select signals (claim 1, lines 24-34).

Regarding claim 2: Claim 1 of the patent recites the memory module of claim 1, wherein the control die is configured to control the data signal conduits so as to control on or more data bus time slots for the respective set of bits of the one or more data signals (claim 1, lines 24-34 and claim 6).

Regarding claim 3: Claim 1 of the patent recites the memory module of claim 1, wherein the control die includes a data path timing controller configured to control timing

of the respective set of bits of the one or more data signals in accordance with the control signals.

Regarding claim 4: Claim 7 of the patent recites the memory module of claim 1, wherein the control signals include command/address signals, wherein the control die includes command/address buffers to control the timing of the command/address signals.

Regarding claim 5: Claim 12 recites the memory module of claim 4, wherein the command/address buffers comprise latches.

Regarding claim 6: Claim 7 recites the memory module of claim 1, wherein the data signal conduits include data buffers configured to control the timing of the respective set of bits of the one or more data signals.

Regarding claim 7: Claim 8 of the patent recites the memory module of claim 6, wherein control die is configured to control the data signal conduits so as to control data bus time slots for the respective set of bits of the one or more data signals.

Regarding claim 8: Claim 13 of the patent recites the memory module of claim 1, wherein the array dies include DDR DRAM, SDRAM, flash memory, or SRAM.

Regarding 9: Claim 14 of the patent recites the memory module of claim 1, wherein the control die is configured to decode the control signals to obtain command/address signals for providing to the array dies.

Regarding claim 10: Claim 15 recites the memory module of claim 1, wherein the control signals include decoded command/address signals, and wherein the control die is configured to pass the command/address signals through to the stacked array dies.

Regarding claims 11-20: Claims 1, 5-7 and 12-15 of the patent recites the memory module of claim 11-20 except for the data signal conduits including a first data signal conduit having a first total capacitive load and a second data signal conduit having a second total capacitive load that is different from the first total capacitive load, and the first data signal conduit including a first driver having a first driver size corresponding to the first total capacitive load, and the second data signal conduit including a second driver having a second driver size corresponding to the second total capacitive load, the second driver size being different from the first driver size. It would have been obvious to one of ordinary skill in the art to recognize that each data signal conduit has a total capacitive load and a driver size.

Claims 1-20 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 10-20 of U.S. Patent No. 9,318,160. Although the claims at issue are not identical, they are not patentably distinct from each other because it would have been obvious to one of ordinary skill in the art to recognize that there are chip-select conduits for receiving the chip select signals in claim 5 of the patent and the array dies include DDR DRAM and it would have been obvious to one of ordinary skill in the art to recognize that each data signal conduit has a total capacitive load and a driver size.

Response to Arguments

5. Applicant's arguments filed 12/27/17 have been fully considered but they are not persuasive.

The double patenting rejections are maintained because two Terminal Disclaimers have been disapproved.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HUAN HOANG whose telephone number is (571)272-1779. The examiner can normally be reached on Tues-Fri 8:30AM-7:00PM.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an

interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/HUAN HOANG/
Primary Examiner, Art Unit 2827

Applicant-Initiated Interview Summary	Application No.	Applicant(s)	
	15/602,099	LEE, HYUN	
	Examiner	Art Unit	
	HUAN HOANG	2827	

All participants (applicant, applicant's representative, PTO personnel):

(1) *HUAN HOANG*. (3)_____.

(2) *JAMIE J. ZHENG*. (4)_____.

Date of Interview: *23 May 2018*.

Type: ☒ Telephonic ☐ Video Conference
☐ Personal [copy given to: ☐ applicant ☐ applicant's representative]

Exhibit shown or demonstration conducted: ☐ Yes ☒ No.
If Yes, brief description: _____.

Issues Discussed ☐101 ☐112 ☐102 ☐103 ☒Others
(For each of the checked box(es) above, please describe below the issue and detailed description of the discussion)

Claim(s) discussed: *11-20*.

Identification of prior art discussed: *N/A*.

Substance of Interview
(For each issue discussed, provide a detailed description and indicate if agreement was reached. Some topics may include: identification or clarification of a reference or a portion thereof, claim interpretation, proposed amendments, arguments of any applied references etc...)

Applcant's representative, Ms. Jamie J. Zheng, called the Examiner to notify that claims 11-20 had not been addressed in the last Office Action. The Exmaniner will consider to send a Letter Restarting Period for Response to correct the last Office Action.

Applicant recordation instructions: The formal written reply to the last Office action must include the substance of the interview. (See MPEP section 713.04). If a reply to the last Office action has already been filed, applicant is given a non-extendable period of the longer of one month or thirty days from this interview date, or the mailing date of this interview summary form, whichever is later, to file a statement of the substance of the interview

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

☒ Attachment

/HUAN HOANG/ Primary Examiner, Art Unit 2827	

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Summary of Record of Interview Requirements

Manual of Patent Examining Procedure (MPEP), Section 713.04, Substance of Interview Must be Made of Record
A complete written statement as to the substance of any face-to-face, video conference, or telephone interview with regard to an application must be made of record in the application whether or not an agreement with the examiner was reached at the interview.

Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews
Paragraph (b)

In every instance where reconsideration is requested in view of an interview with an examiner, a complete written statement of the reasons presented at the interview as warranting favorable action must be filed by the applicant. An interview does not remove the necessity for reply to Office action as specified in §§ 1.111, 1.135. (35 U.S.C. 132)

37 CFR §1.2 Business to be transacted in writing.
All business with the Patent or Trademark Office should be transacted in writing. The personal attendance of applicants or their attorneys or agents at the Patent and Trademark Office is unnecessary. The action of the Patent and Trademark Office will be based exclusively on the written record in the Office. No attention will be paid to any alleged oral promise, stipulation, or understanding in relation to which there is disagreement or doubt.

The action of the Patent and Trademark Office cannot be based exclusively on the written record in the Office if that record is itself incomplete through the failure to record the substance of interviews.

It is the responsibility of the applicant or the attorney or agent to make the substance of an interview of record in the application file, unless the examiner indicates he or she will do so. It is the examiner's responsibility to see that such a record is made and to correct material inaccuracies which bear directly on the question of patentability.

Examiners must complete an Interview Summary Form for each interview held where a matter of substance has been discussed during the interview by checking the appropriate boxes and filling in the blanks. Discussions regarding only procedural matters, directed solely to restriction requirements for which interview recordation is otherwise provided for in Section 812.01 of the Manual of Patent Examining Procedure, or pointing out typographical errors or unreadable script in Office actions or the like, are excluded from the interview recordation procedures below. Where the substance of an interview is completely recorded in an Examiners Amendment, no separate Interview Summary Record is required.

The Interview Summary Form shall be given an appropriate Paper No., placed in the right hand portion of the file, and listed on the "Contents" section of the file wrapper. In a personal interview, a duplicate of the Form is given to the applicant (or attorney or agent) at the conclusion of the interview. In the case of a telephone or video-conference interview, the copy is mailed to the applicant's correspondence address either with or prior to the next official communication. If additional correspondence from the examiner is not likely before an allowance or if other circumstances dictate, the Form should be mailed promptly after the interview rather than with the next official communication.

The Form provides for recordation of the following information:
- Application Number (Series Code and Serial Number)
- Name of applicant
- Name of examiner
- Date of interview
- Type of interview (telephonic, video-conference, or personal)
- Name of participant(s) (applicant, attorney or agent, examiner, other PTO personnel, etc.)
- An indication whether or not an exhibit was shown or a demonstration conducted
- An identification of the specific prior art discussed
- An indication whether an agreement was reached and if so, a description of the general nature of the agreement (may be by attachment of a copy of amendments or claims agreed as being allowable). Note: Agreement as to allowability is tentative and does not restrict further action by the examiner to the contrary.
- The signature of the examiner who conducted the interview (if Form is not an attachment to a signed Office action)

It is desirable that the examiner orally remind the applicant of his or her obligation to record the substance of the interview of each case. It should be noted, however, that the Interview Summary Form will not normally be considered a complete and proper recordation of the interview unless it includes, or is supplemented by the applicant or the examiner to include, all of the applicable items required below concerning the substance of the interview.

A complete and proper recordation of the substance of any interview should include at least the following applicable items:
1) A brief description of the nature of any exhibit shown or any demonstration conducted,
2) an identification of the claims discussed,
3) an identification of the specific prior art discussed,
4) an identification of the principal proposed amendments of a substantive nature discussed, unless these are already described on the Interview Summary Form completed by the Examiner,
5) a brief identification of the general thrust of the principal arguments presented to the examiner,
   (The identification of arguments need not be lengthy or elaborate. A verbatim or highly detailed description of the arguments is not required. The identification of the arguments is sufficient if the general nature or thrust of the principal arguments made to the examiner can be understood in the context of the application file. Of course, the applicant may desire to emphasize and fully describe those arguments which he or she feels were or might be persuasive to the examiner.)
6) a general indication of any other pertinent matters discussed, and
7) if appropriate, the general results or outcome of the interview unless already described in the Interview Summary Form completed by the examiner.

Examiners are expected to carefully review the applicant's record of the substance of an interview. If the record is not complete and accurate, the examiner will give the applicant an extendable one month time period to correct the record.

Examiner to Check for Accuracy

If the claims are allowable for other reasons of record, the examiner should send a letter setting forth the examiner's version of the statement attributed to him or her. If the record is complete and accurate, the examiner should place the indication, "Interview Record OK" on the paper recording the substance of the interview along with the date and the examiner's initials.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15602099	LEE, HYUN
	Examiner	Art Unit
	HUAN HOANG	2827

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	07/22/2017	02/20/2018	05/23/2018						
	1	✓	✓	✓						
	2	✓	✓	✓						
	3	✓	✓	✓						
	4	✓	✓	✓						
	5	✓	✓	✓						
	6	✓	✓	✓						
	7	✓	✓	✓						
	8	✓	✓	✓						
	9	✓	✓	✓						
	10	✓	✓	✓						
	11			✓						
	12			✓						
	13			✓						
	14			✓						
	15			✓						
	16			✓						
	17			✓						
	18			✓						
	19			✓						
	20			✓						

Electronically filed July 2, 2018

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun Lee	Confirmation No.:	1757
Serial No.:	15/602,099	Art Unit:	2827
Filed:	May 22, 2017	Examiner:	Hoang, Huan
For:	*Memory Module With Packages Of Stacked Memory Chips*	Attorney Docket No.:	129980-5070-US
		Date:	July 2, 2018

RESPONSE TO FINAL OFFICE ACTION & INTERVIEW SUMMARY

Mail Stop: AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
Sir:

The enclosed Amendment is in response to the Final Office Action dated May 31, 2018 for the above identified patent application.

The Commissioner is hereby authorized to charge any required fee(s) to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5070-US).

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Amendments to the Claims

The following listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously Presented) A memory module operable in a computer system to communicate with a system memory controller via a command/address bus and a data bus, comprising:

a register device configured to receive command/address signals from the system memory controller via the command/address bus and to output control signals in response to the input command/address signals, the control signals including chip-select signals; and

a plurality of DRAM packages coupled to the register device and configured to receive the control signals via a set of module control lines, each respective DRAM package comprising:

control terminals coupled to corresponding signal lines in the set of module control lines, and data terminals coupled to a respective section of the data bus;

stacked array dies;

a control die including data signal conduits coupled to the data terminals and control signal conduits coupled to the control terminals, the control signal conduits including chip-select conduits for receiving the chip select signals and providing respective ones of the chip select signals to respective ones of the stacked array dies; and

die interconnects including first die interconnects coupled to the data signal conduits and second die interconnects coupled to the control signal conduits, each of at least a subset of the first die interconnects is coupled to at least two of the stacked array dies; and

wherein the control die is configured to control the data signal conduits in accordance with the control signals to enable the each respective DRAM package to communicate a respective set of bits of one or more data signals between a selected die among the stacked dies and the system memory controller, the selected die having received one of the chip select signals that is different from any of the other ones of the chip select signals.

2. (Previously Presented) The memory module of claim 1, wherein the control die is configured to control the data signal conduits so as to control one or more data bus time slots for the respective set of bits of the one or more data signals.

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3. (Previously Presented) The memory module of claim 1, wherein the control die includes a data path timing controller configured to control timing of the respective set of bits of the one or more data signals in accordance with the control signals.

4. (Previously Presented) The memory module of claim 1, wherein the control signals include command/address signals, wherein the control die includes command/address buffers to control the timing of the command/address signals.

5. (Original) The memory module of claim 4, wherein the command/address buffers comprise latches.

6. (Previously Presented) The memory module of claim 1, wherein the data signal conduits include data buffers configured to control the timing of the respective set of bits of the one or more data signals.

7. (Previously Presented) The memory module of claim 6, wherein control die is configured to control the data signal conduits so as to control data bus time slots for the respective set of bits of the one or more data signals.

8. (Original) The memory module of claim 1, wherein the array dies include DDR DRAM, SDRAM, flash memory, or SRAM.

9. (Previously Presented) The memory module of claim 1, wherein the control die is configured to decode the control signals to obtain command/address signals for providing to the array dies.

10. (Original) The memory module of claim 1, wherein the control signals include decoded command/address signals, and wherein the control die is configured to pass the command/address signals through to the stacked array dies.

11. (Previously Presented) The memory module of claim 1, wherein the data signal conduits include a first data signal conduit having a first total capacitive load and a second data signal conduit having a second total capacitive load that is different from the first total capacitive load, and wherein the first data signal conduit includes a first driver having a first driver size corresponding to the first total capacitive load, and the second data signal conduit includes a

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second driver having a second driver size corresponding to the second total capacitive load, the second driver size being different from the first driver size.

12. (Previously Presented) The memory module of claim 1, wherein the data signal conduits include a first data signal conduit coupled to a first subset of the stacked array dies and a second data signal conduit coupled to a second subset of the stacked array dies, wherein the first data signal conduit has a first total capacitive load and the second data signal conduit has a second total capacitive load that is substantially the same as the first total capacitive load.

13. (Previously Presented) A memory module operable in a computer system to communicate with a system memory controller via a command/address bus and a data bus, comprising:

a register device configured to receive input command/address signals from the system memory controller via the command/address bus and to output control signals in response to the input command/address signals; and

a plurality of DRAM packages coupled to the register device to receive the control signals via a set of module control lines, each DRAM package comprising:

control terminals coupled to corresponding signal lines in the set of module control lines, and data terminals coupled to a section of the data bus corresponding to the each DRAM package;

stacked array dies;

a control die including data signal conduits coupled to the data terminals and control signal conduits coupled to the control terminals; and

die interconnects including first die interconnects coupled to the data signal conduits and second die interconnects coupled to the control signal conduits, each of the first die interconnects is coupled to at least one of the stacked array dies; and

wherein the control die is configured to control the data signal conduits in accordance with the control signals to enable the each respective DRAM package to communicate a respective set of bits of one or more data signals between a selected die among the stacked dies and the system memory controller;

wherein the data signal conduits include a first data signal conduit having a first total capacitive load and a second data signal conduit having a second total capacitive load that is

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different from the first total capacitive load, and wherein the first data signal conduit includes a first driver having a first driver size corresponding to the first total capacitive load, and the second data signal conduit includes a second driver having a second driver size corresponding to the second total capacitive load, the second driver size being different from the first driver size.

14. (Previously Presented) The memory module of claim 13, wherein the control die includes a data path timing controller configured to control timing of the respective set of bits of the one or more data signals.

15. (Previously Presented) The memory module of claim 13, wherein the data signal conduits include data buffers configured to control the timing of the respective set of bits of the one or more data signals.

16. (Previously Presented) The memory module of claim 13, wherein the array dies include DDR DRAM, SDRAM, flash memory, or SRAM.

17. (Previously Presented) The memory module of claim 13, wherein the control die is configured to decode the control signals to obtain command/address signals for providing to the array dies.

18. (Previously Presented) The memory module of claim 13, wherein the control signals include chip-select signals and the control signal conduits include chip-select conduits for receiving the chip select signals and providing respective ones of the chip select signals to respective ones of the stacked array dies, and wherein the selected die has received one of the chip select signals that is different from any of the other ones of the chip select signals.

19. (Previously Presented) A memory module operable in a computer system to communicate with a system memory controller via a command/address bus and a data bus, comprising:

a register device configured to receive input command/address signals from the system memory controller via the command/address bus and to output control signals in response to the input command/address signals; and

a plurality of DRAM packages coupled to the register device to receive the control signals via a set of module control lines, each DRAM package comprising:

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control terminals coupled to corresponding signal lines in the set of module control lines, and data terminals coupled to a section of the data bus corresponding to the each DRAM package;

stacked array dies;

a control die including data signal conduits coupled to the data terminals and control signal conduits coupled to the control terminals; and

die interconnects including first die interconnects coupled to the data signal conduits and second die interconnects coupled to the control signal conduits, each of the first die interconnects is coupled to at least one of the stacked array dies; and

wherein the control die is configured to control the data signal conduits in accordance with the control signals to enable the each respective DRAM package to communicate a respective set of bits of one or more data signals between a selected die among the stacked dies and the system memory controller;

wherein the data signal conduits include a first data signal conduit coupled to a first subset of the stacked array dies and a second data signal conduit coupled to a second subset of the stacked array dies, wherein the first data signal conduit has a first total capacitive load and the second data signal conduit has a second total capacitive load that is substantially the same as the first total capacitive load;

wherein the control signals include chip-select signals and the control signal conduits include chip-select conduits for receiving the chip select signals and providing respective ones of the chip select signals to respective ones of the stacked array dies, and wherein the selected die has received one of the chip select signals that is different from any of the other ones of the chip select signals; and

wherein the control die includes a data path timing controller configured to control timing of the respective set of bits of the one or more data signals in accordance with the control signals.

20. (Previously Presented) The memory module of claim 19, wherein the control die is configured to decode the control signals to obtain command/address signals for providing to the array dies.

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REMARKS

This amendment responds to the final office action mailed May 31, 2018. In the final office action, the Examiner:

A. rejected claims 1-20 on the ground of nonstatutory double patenting as being unpatentable over claims 1, 5-7 and 12-15 of U.S. Patent No. 9,659,601; and

B. rejected claims 1-20 on the ground of nonstatutory double patenting as being unpatentable over claims 10-20 of U.S. Patent No. 9,318,160.

A. Rejection of claims 1-20 on the ground of nonstatutory double patenting as being unpatentable over claims 1, 5-7 and 12-15 of U.S. Patent No. 9,659,601

A terminal disclaimer is being filed concurrently with this response to address this nonstatutory double patenting rejection.

Applicant respectfully requests that these rejections be withdrawn.

B. Rejection of claims 1-20 on the ground of nonstatutory double patenting as being unpatentable over claims 10-20 of U.S. Patent No. 9,318,160

A terminal disclaimer is being filed concurrently with this response to address this nonstatutory double patenting rejection.

Applicant respectfully requests that these rejections be withdrawn.

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CONCLUDING REMARKS

By responding in the foregoing remarks only to particular positions asserted by the examiner, the Applicant does not necessarily acquiesce in other positions that have not been explicitly addressed. In addition, the Applicant's arguments for the patentability of a claim should not be understood as implying that no other reasons for the patentability of that claim exist.

In light of the above amendments and remarks, the Applicant respectfully requests that the Examiner reconsider this application with a view towards allowance. The Examiner is invited to call the undersigned attorney at (650) 843-4000, if a telephone call could help resolve any remaining items.

Respectfully submitted,

Date: July 2, 2018

/Jamie J. Zheng/ 51,167

Jaime J. Zheng (Reg. No.)

MORGAN, LEWIS & BOCKIUS LLP
1400 Page Mill Road
Palo Alto, CA 94304
Phone: (650) 843-4000

Petitioners
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Electronic Acknowledgement Receipt

EFS ID:	33068121
Application Number:	15602099
International Application Number:	
Confirmation Number:	1757
Title of Invention:	MEMORY MODULE WITH PACKAGES OF STACKED MEMORY CHIPS
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	129980-5070US
Receipt Date:	02-JUL-2018
Filing Date:	22-MAY-2017
Time Stamp:	19:08:05
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		129980_5070US_AMD.pdf	137062 dea9ed0472bc6d5115939e9555cd9a9f02ab06d8	yes	8

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Response After Final Action	1	1
	Claims	2	6
	Applicant Arguments/Remarks Made in an Amendment	7	8
Warnings:			
Information:			
	Total Files Size (in bytes):	137062	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc Code: DIST.E.FILE Document Description: Electronic Terminal Disclaimer - Filed	PTO/SB/26 U.S. Patent and Trademark Office Department of Commerce

Electronic Petition Request	**TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT**
Application Number	15602099
Filing Date	22-May-2017
First Named Inventor	Hyun Lee
Attorney Docket Number	129980-5070US
Title of Invention	MEMORY MODULE WITH PACKAGES OF STACKED MEMORY CHIPS

☒ Filing of terminal disclaimer does not obviate requirement for response under 37 CFR 1.111 to outstanding Office Action

☒ This electronic Terminal Disclaimer is not being used for a Joint Research Agreement.

Owner	Percent Interest
NETLIST, INC.	100%

The owner(s) with percent interest listed above in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of prior patent number(s)

9318160

9659601

as the term of said prior patent is presently shortened by any terminal disclaimer. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the prior patent are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the owner does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the prior patent, "as the term of said prior patent is presently shortened by any terminal disclaimer," in the event that said prior patent later:
- expires for failure to pay a maintenance fee;
- is held unenforceable;
- is found invalid by a court of competent jurisdiction;
- is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
- has all claims canceled by a reexamination certificate;
- is reissued; or
- is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

(•) Terminal disclaimer fee under 37 CFR 1.20(d) is included with Electronic Terminal Disclaimer request. ( ) I certify, in accordance with 37 CFR 1.4(d)(4), that the terminal disclaimer fee under 37 CFR 1.20(d) required for this terminal disclaimer has already been paid in the above-identified application.	
Applicant claims the following fee status: ( ) Small Entity ( ) Micro Entity (•) Regular Undiscounted I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.	
THIS PORTION MUST BE COMPLETED BY THE SIGNATORY OR SIGNATORIES I certify, in accordance with 37 CFR 1.4(d)(4) that I am: (•) An attorney or agent registered to practice before the Patent and Trademark Office who is of record in this application Registration Number 51167 ( ) A sole inventor ( ) A joint inventor; I certify that I am authorized to sign this submission on behalf of all of the inventors as evidenced by the power of attorney in the application ( ) A joint inventor; all of whom are signing this request	
Signature	/Jamie J. Zheng/
Name	Jamie J. Zheng

*Statement under 37 CFR 3.73(b) is required if terminal disclaimer is signed by the assignee (owner).
Form PTO/SB/96 may be used for making this certification. See MPEP § 324.

Electronic Patent Application Fee Transmittal

Application Number:	15602099
Filing Date:	22-May-2017
Title of Invention:	MEMORY MODULE WITH PACKAGES OF STACKED MEMORY CHIPS
First Named Inventor/Applicant Name:	Hyun Lee
Filer:	Jamie Jie Zheng
Attorney Docket Number:	129980-5070US

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
STATUTORY OR TERMINAL DISCLAIMER	1814	1	160	160
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**160**

Doc Code: DISQ.E.FILE
Document Description: Electronic Terminal Disclaimer – Approved

Application No.: 15602099

Filing Date: 22-May-2017

Applicant/Patent under Reexamination: Lee

Electronic Terminal Disclaimer filed on July 2, 2018

☒ APPROVED

This patent is subject to a terminal disclaimer

☐ DISAPPROVED

Approved/Disapproved by: Electronic Terminal Disclaimer automatically approved by EFS-Web

U.S. Patent and Trademark Office

Electronic Acknowledgement Receipt

EFS ID:	32996671
Application Number:	15602099
International Application Number:	
Confirmation Number:	1757
Title of Invention:	MEMORY MODULE WITH PACKAGES OF STACKED MEMORY CHIPS
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	129980-5070US
Receipt Date:	02-JUL-2018
Filing Date:	22-MAY-2017
Time Stamp:	19:11:29
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$160
RAM confirmation Number	070318INTEFSW00006205500310
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Terminal Disclaimer-Filed (Electronic)	eTerminal-Disclaimer.pdf	33608 64ae57ab3cde05453ac6b9b77f97e074089b6e9c	no	2
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30335 9b97ede7b8762600ae3583cddb59fa8ac9511586	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	63943		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 15/602,099	Filing Date 05/22/2017	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $80 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $420 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

AMENDMENT	07/02/2018	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0		x $100 =	0
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0		x $460 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $ 0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $ 0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/RENEE HAWKINS/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

79141 7590 08/01/2018
Morgan Lewis Bockius LLP / Jamie Zheng Ph.D.
1400 Page Mill Road
Palo Alto, CA 94304

EXAMINER
HOANG, HUAN

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 08/01/2018

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/602,099	05/22/2017	Hyun Lee	129980-5070US	1757

TITLE OF INVENTION: MEMORY MODULE WITH PACKAGES OF STACKED MEMORY CHIPS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0	$0	$1000	11/01/2018

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PTOL-85 (Rev. 02/11)

Petitioners
Ex. 1008, p. 147

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

79141 7590 08/01/2018
Morgan Lewis Bockius LLP / Jamie Zheng Ph.D.
1400 Page Mill Road
Palo Alto, CA 94304

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/602,099	05/22/2017	Hyun Lee	129980-5070US	1757

TITLE OF INVENTION: MEMORY MODULE WITH PACKAGES OF STACKED MEMORY CHIPS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0	$0	$1000	11/01/2018

EXAMINER	ART UNIT	CLASS-SUBCLASS
HOANG, HUAN	2827	365-063000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ Applicant certifying micro entity status. See 37 CFR 1.29 — NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ❑ Applicant asserting small entity status. See 37 CFR 1.27 — NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ❑ Applicant changing to regular undiscounted fee status. — NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Petitioners
Ex. 1008, p. 148

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/602,099	05/22/2017	Hyun Lee	129980-5070US	1757

79141 7590 08/01/2018

Morgan Lewis Bockius LLP / Jamie Zheng Ph.D.
1400 Page Mill Road
Palo Alto, CA 94304

EXAMINER	
HOANG, HUAN	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 08/01/2018

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 02/11)

Petitioners
Ex. 1008, p. 149

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 15/602,099	Applicant(s) LEE, HYUN	
	Examiner HUAN HOANG	Art Unit 2827	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the Response filed on 07/02/18*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-20*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☒ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/HUAN HOANG/
Primary Examiner, Art Unit 2827

Petitioners
Ex. 1008, p. 151

The present application is being examined under the pre-AIA first to invent provisions.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The application has been amended as follows:

In the claims:

Claim 1, line 4, replace "command/address signals" insert –input command/address signals--.

Note: The amendment to claim 1 is to provide proper antecedent basis for "the input command/address signals" in claim 1, lines 5-6.

Terminal Disclaimer

2. The terminal disclaimer filed on 07/02/18 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of the full statutory term of prior patent numbers 9,318,160 and 9,659,601 has been reviewed and is accepted. The terminal disclaimer has been recorded.

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to HUAN HOANG whose telephone number is (571)272-1779. The examiner can normally be reached on Tues-Fri 8:30AM-7:00PM.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/HUAN HOANG/
Primary Examiner, Art Unit 2827

OK TO ENTER: /H.H/

07/17/2018

Electronically filed July 2, 2018

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun Lee	Confirmation No.:	1757
Serial No.:	15/602,099	Art Unit:	2827
Filed:	May 22, 2017	Examiner:	Hoang, Huan
For:	*Memory Module With Packages Of Stacked Memory Chips*	Attorney Docket No.:	129980-5070-US
		Date:	July 2, 2018

RESPONSE TO FINAL OFFICE ACTION & INTERVIEW SUMMARY

Mail Stop: AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
Sir:

The enclosed Amendment is in response to the Final Office Action dated May 31, 2018 for the above identified patent application.

The Commissioner is hereby authorized to charge any required fee(s) to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5070-US).

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15602099	LEE, HYUN
	Examiner	Art Unit
	HUAN HOANG	2827

CPC- SEARCHED		
Symbol	Date	Examiner
G11C 5/066, G11C 5/06, G11C 7/1057, G11C 7/1084, G11C 7/12	7/22/17	HH
Above Updated	07/17/18	HH

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
365	63	7/22/17	HH
Above	Updated	07/17/18	HH

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

SEARCH NOTES		
Search Notes	Date	Examiner
EAST (text search)	7/22/17	HH
EAST (text search)	07/17/18	HH
Inventor search	07/17/18	HH

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
	EAST (US-PGPUB)	07/17/18	HH

	/HUAN HOANG/ Primary Examiner.Art Unit 2827

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

BIB DATA SHEET

CONFIRMATION NO. 1757

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
15/602,099	05/22/2017	365	2827	129980-5070US

APPLICANTS
Netlist, Inc., Irvine, CA;

INVENTORS
Hyun Lee, Ladera Ranch, CA;

**** CONTINUING DATA ***************************
This application is a CON of 15/095,288 04/11/2016 PAT 9659601
which is a CON of 14/337,168 07/21/2014 PAT 9318160
which is a CON of 13/288,850 11/03/2011 PAT 8787060
which claims benefit of 61/409,893 11/03/2010

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****
05/30/2017

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /HUAN HOANG/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		CA	8	10	1

ADDRESS
Morgan Lewis Bockius LLP / Jamie Zheng Ph.D.
1400 Page Mill Road
Palo Alto, CA 94304
UNITED STATES

TITLE
MEMORY MODULE WITH PACKAGES OF STACKED MEMORY CHIPS

FILING FEE RECEIVED		
1600	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	24063	(G11C5/066 or G11C7/12 or G11C7/1084 or G11C5/06 or G11C7/1057).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/07/17 17:06
L2	29581	(G11C5/066 or G11C7/12 or G11C7/1084 or G11C5/06 or G11C7/1057).cpc. 365/063,63.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/07/17 17:07
L3	168	2 and register with address$3 with chip adj select$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/07/17 17:08
L4	122	3 and (dynamic adj ram dram)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/07/17 17:19
L5	15	4 and stack$3 with (die dice integrated adj circuit ic)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/07/17 17:19
L6	2123220	netlist.as. lee.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/07/17 17:22
L7	124	6 and register with address$3 with chip adj select$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/07/17 17:22
L9	79	7 and (dynamic adj ram dram)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/07/17 17:23
L10	18	9 and stack$3 with (die dice integrated adj circuit ic)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/07/17 17:24
L11	18	10 and interconnect$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/07/17 17:24
L12	2424	register with (command address$3) with chip adj select$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/07/17 17:27
L13	1175	12 and (dynamic adj ram dram)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/07/17 17:27

L14	61	12 and (dynamic adj ram dram) with control$3 adj3 line	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/07/17 17:29
L15	61	12 and (dynamic adj ram dram) with control$4 adj3 line	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/07/17 17:29
L16	3	15 and stack$3 with (die dice integrated adj circuit ic)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/07/17 17:29

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L17	2	(memory and module and controller and command and address and bus and control and signal and dram and package and stack$3 and die and conduit and interconnect$3).clm.	US-PGPUB; USPAT	OR	ON	2018/07/17 17:31
L18	4	(memory and module and controller and command and address and array and control and signal and dram and package and stack$3 and die and conduit and interconnect$3).clm.	US-PGPUB; USPAT	OR	ON	2018/07/17 17:32
L19	0	(memory and module and controller and command and address and array and control and signal and dram and package and stack$3 and die and capacitive and interconnect$3).clm.	US-PGPUB; USPAT	OR	ON	2018/07/17 17:33

7/17/2018 5:33:40 PM

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15602099	LEE, HYUN
	Examiner	**Art Unit**
	HUAN HOANG	2827

CPC						
Symbol					**Type**	**Version**
G11C		5	/	066	F	2013-01-01
G11C		5	/	06	I	2013-01-01
G11C		7	/	1057	I	2013-01-01
G11C		7	/	1084	I	2013-01-01
G11C		7	/	12	I	2013-01-01
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CPC Combination Sets							
Symbol				**Type**	**Set**	**Ranking**	**Version**
			/				
			/				

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	20	
/HUAN HOANG/ Primary Examiner.Art Unit 2827	07/17/2018	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15602099	LEE, HYUN
	Examiner	**Art Unit**
	HUAN HOANG	2827

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION	
CLASS	SUBCLASS	CLAIMED	NON-CLAIMED
365	63	G 1 1 C 5 / 06 (2006.01.01)	

CROSS REFERENCE(S)					
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	20	
/HUAN HOANG/ Primary Examiner.Art Unit 2827	07/17/2018	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15602099	LEE, HYUN
	Examiner	**Art Unit**
	HUAN HOANG	2827

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☒ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		17												
	2		18												
	3		19												
	4		20												
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	7														
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	9														
	10														
	11														
	12														
	13														
	14														
	15														
	16														

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 20	
/HUAN HOANG/ Primary Examiner.Art Unit 2827 (Primary Examiner)	07/17/2018 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 2

REQUEST FOR CONTINUED EXAMINATION (RCE) TRANSMITTAL

Address to:
Mail Stop RCE
Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Electronically filed	October 29, 2018
Application Number	15/602,099
Filing Date	May 22, 2017
First Named Inventor	Hyun Lee
Art Unit	2827
Examiner Name	Hoang, Huan
Attorney Docket No.	129980-5070US

This is a Request for Continued Examination (RCE) under 37 C.F.R. § 1.114 of the above-identified application. Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application.

1. Submission required under 37 C.F.R. § 1.114

NOTE: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

a. ☐ Previously submitted. If a final Office Action is outstanding, any amendments filed after the final Office Action may be considered as a submission.
   - i. ☐ Request for non-entry of amendment: Please **do not** entered the amendment submitted on _____
   - ii. ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed _____
   - iii. ☐ Other _____

b. ☒ Enclosed
   - i. ☐ Amendment/Reply
   - ii. ☐ Affidavit(s)/Declaration(s)
   - iii. ☒ Information Disclosure Statement (IDS)
   - iv. ☐ Other _____

2. Miscellaneous

a. ☐ Suspension of action on the above-identified application is requested under 37 C.F.R. § 1.103(c) for a period of _____ months. (Period of suspension shall not exceed 3 months; Fee under 37 C.F.R. § 1.17(i) required)

b. ☐ Other _____

3. Fees — The RCE fee under 37 C.F.R. § 1.17(e) is required by 37 C.F.R. § 1.114 when the RCE is filed.

a. ☒ The Director is hereby authorized to charge the following fees, any underpayment of fees, or credit any overpayments, to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5070US).
   - i. ☒ (1st request) RCE fee required under 37 C.F.R. § 1.17(e)(1), estimated to be $1300 (large entity) or $650 (small entity)
   - ii. ☐ (2nd or subsequent request) RCE fee required under 37 C.F.R. § 1.17(e)(2), estimated to be $1900 (large entity) or $950 (small entity)
   - iii. ☐ Extension of time fee required under 37 C.F.R. §§ 1.136 and 1.17, estimated to be $ for a month(s) extension, the request for which is being made herewith
   - iv. ☐ Other _____

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

Name (Print/Type)	Gary S. Williams	*Registration No. (Attorney/Agent)*	31,066
Signature		*Date*	October 29, 2018

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, or by facsimile transmitted to fax no. 1-703- to the U.S. Patent and Trademark Office on the date indicated below.

Name (Print/Type)		*Registration No. (Attorney/Agent)*	
Signature		*Date*	

DB2/ 35058353.1

PTO/SB/08a/b(07-09)
Approved for use through 7/31/2012. 0MB 0651-0031
US Patent & Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless ii contains a valid 0MB control number.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet | 1 | of | 18

Complete if Known	
Application Number	15/602,099
Filing Date	May 22, 2017
First Named Inventor	Hyun Lee
Art Unit	2827
Examiner Name	Hoang, Huan
Attorney Docket Number	129980-5070-US

USP ATENT DOCUMENTS					
Examiner Initials*	Cite No. 1	Document Number Number-Kind Code 2 (ifknown)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1.	2002/0038405 Al	03-28-2002	Leddige, M. et al.	
	2.	2009/0296503 A 1	12-03-2009	Chu, M. et al.	
	3.	2011/0085408 A 1	04-14-2011	Solomon, J. et al.	
	4.	2008/0162790 Al	07-03-2008	IM	

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.1	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T'
	5.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Related Matters, filed April 28, 2015	
	6.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Patent Owner Response to Petition, filed February 22, 2016	
	7.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner1s Objections to Evidence, filed February 29, 2016	
	8.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner1s Reply, filed May 19, 2016	
	9.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner Request for Oral Argument, filed June 2, 2016	
	10.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, PATENT OWNER MOTION FOR OBSERVATIONS, filed June 2, 2016	
	11.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, PATENT OWNER REQUEST FOR ORAL ARGUMENT, filed June 2, 2016	
	12.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, ORDER Trial Hearing, filed June 8, 2016	
	13.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Patent Owner1s SUBMISSION ON PROPRIETY OF PETITIONER REPLY, filed June 9, 2016	
	14.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner1s Response to Motion for Observations, filed June 10, 2016	
	15.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner1s Response to Netlist1s Submission, filed June 13, 2016	
	16.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Patent Owner1s Objections to Petitioner1s Demonstrative Exhibits, filed June 23, 2016	
	17.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Patent Owner1s Demonstrative Exhibits, filed June 24, 2016	

EXAMINER **DATE CONSIDERED**

• EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicanl. 1 Applicant's unique citation designation number (optional). 2 See Kinds Codes of USPTO Patents Documents at www.,Jsplo.GGv or MPEP 901.04.3 Enter Office that issued the document, by the two-letter code (WIPO Standard ST. 3). 4 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5 Kind of document by the appropriate symbols as indicated on the document and WIPO Standard ST. 16 if possible. 6 Applicant is to place a check mark here if English language Translation is attached.

PTO/SB/08a/b(07-09)
Approved for use through 7/31/2012. 0MB 0651-0031
US Patent & Trademark Office; U.S. DEPARTMENT OF COMMERCE
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet | 2 | of | 18

Complete if Known	
Application Number	15/602,099
Filing Date	May 22, 2017
First Named Inventor	Hyun Lee
Art Unit	2827
Examiner Name	Hoang, Huan
Attorney Docket Number	129980-5070-US

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[6]
	18.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner1s Updated Exhibit List, filed June 24, 2016	
	19.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Supplemental Declaration of Dr. Jagannathan, filed May 19, 2016	
	20.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, May 10, 2016 Deposition of Carl Sechen, filed May 19, 2016	
	21.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner1s Demonstrative Exhibits, filed June 24, 2016	
	22.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 2001, "Declaration of Professor Carl Sechen," filed February 22, 2016	
	23.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 2002, "Videotaped Deposition of Srinivasan Jagannathan, Ph.Don February 12, 2016," filed February 22, 2016	
	24.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 2003, "Videotaped Deposition of Srinivasan Jagannathan, Ph.Don April 20, 2015," filed February 22, 2016	
	25.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 2007, "Deposition of Dr. Srinivasan Jagannathan on May 25, 2016," filed June 2, 2016	
	26.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Patent Owner Response to Petition, filed February 22, 2016	
	27.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Petitioner1s Objections to Evidence, filed February 29, 2016	
	28.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Petitioner1s Reply, filed May 19, 2016	
	29.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Petitioner Request for Oral Argument, filed June 2, 2016	
	30.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, PATENT OWNER MOTION FOR OBSERVATIONS, filed June 2, 2016	
	31.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, PATENT OWNER REQUEST FOR ORAL ARGUMENT, filed June 2, 2016	
	32.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Patent Owner1s SUBMISSION ON PROPRIETY OF PETITIONER REPLY, filed June 9, 2016	
	33.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Petitioner1s Response to Motion for Observations, filed June 10, 2016	
	34.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Petitioner1s Response to Patent Owner1s Submission, filed June 13, 2016	

EXAMINER **DATE CONSIDERED**

• EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicanl. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patents Documents at www.,Jsplo.GGv or MPEP 901.04.[3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST. 3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document and WIPO Standard ST. 16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

PTO/SB/08a/b(07-09)
Approved for use through 7/31/2012. 0MB 0651-0031
US Patent & Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet | 3 | of | 18

Complete if Known	
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Filing Date	May 22, 2017
First Named Inventor	Hyun Lee
Art Unit	2827
Examiner Name	Hoang, Huan
Attorney Docket Number	129980-5070-US

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[6]
	35.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Patent Owner1s Objections to Petitioner1s Demonstrative Exhibits, filed June 23, 2016	
	36.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Patent Owner1s Demonstrative Exhibits, filed June 24, 2016	
	37.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Petitioner1s Updated Exhibit List, filed June 24, 2016	
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	40.	International Search Report and Written Opinion, International Application No. PCT/US14/48517, filed July 28, 2014, dated October 27, 2014	
	41.	Inter Partes Review Case No. IPR2014-01029, Petitioner's Request for Rehearing pursuant to 37 C.F.R. § 42.71, filed on January 15, 2015.	
	42.	Inter Partes Review Case No. IPR2014-01029, Decision Denying Request for Rehearing, Issued on March 3, 2015.	
	43.	Inter Partes Review Case No. IPR2014-01369, Decision Denying Institution oflnter Partes Review 37 C.F.R. § 42.108, issued March 9, 2014.	
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Complete if Known	
Application Number	15/602,099
Filing Date	May 22, 2017
First Named Inventor	Hyun Lee
Art Unit	2827
Examiner Name	Hoang, Huan
Attorney Docket Number	129980-5070-US

US PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (If known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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	10.	Inter Partes Review Case No. 2014-00882, Petitioner's Request for Oral Argument, filed July 1, 2015	
	11.	Inter Partes Review Case No. 2014-00882, Patent Owner's Request for Oral Argument, filed July 3,2015	
	12.	Inter Partes Review Case No. 2014-00882, Order - Request for Oral Argument - 37 C.F.R. 42.70, filed July 10, 2015	
	13.	Inter Partes Review Case No. 2014-00882, Record of Oral Hearing, filed November 16, 2015	
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	16.	Inter Partes Review Case No. 2014-00882, Exhibit 1022, 'Professor Carl Sechen Deposition Transcript,' filed June,19,2015	
	17.	Inter Partes Review Case No. 2014-00882, Exhibit 1023, 'Dr. Srinivasan Jagannathan Supplemental Declaration,' filed June 19,2015	
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Application Number	15/602,099
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First Named Inventor	Hyun Lee
Art Unit	2827
Examiner Name	Hoang, Huan
Attorney Docket Number	129980-5070-US

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First Named Inventor	Hyun Lee
Art Unit	2827
Examiner Name	Hoang, Huan
Attorney Docket Number	129980-5070-US

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Examiner Initials*	Cite No.1	Document Number Number-Kind Code 2 (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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	56.	International Search Report and Written Opinion, International Application No. PCT/US14/48517, filed July 28, 2014, dated October 27, 2014	
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	70.	Inter Partes Review Case No. IPR2014-01029, Petition for Inter Partes Review of U.S. Patent No. 8,516,185, filed on June 24, 2014.	
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	72.	Inter Partes Review Case No. IPR2014-01029, Supplemental Petition for Inter Partes Review of U.S. Patent No. 8,516,185, filed on July 23, 2014.	
	73.	Inter Partes Review Case No. IPR2014-01029, Patent Owner's Preliminary Response pursuant to 37 C.F.R. § 42.107, filed on October 17, 2014.	
	74.	Inter Partes Review Case No. IPR2014-01029, Decision Denying Institution of Inter Partes Review 37 C.F.R. § 42.108, issued December 16, 2014.	
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First Named Inventor	Hyun Lee
Art Unit	2827
Examiner Name	Hoang, Huan
Attorney Docket Number	129980-5070-US

NON PATENT LITERATURE DOCUMENTS			
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	79.	Inter Partes Review Case No. IPR2014-00882, Corrected Petition for Inter Partes Review of U.S. Patent No. 7,881,150, filed on July 8, 2014.	
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	90.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-01011, Patent Owner's Preliminary Response Pursuant to 37 C.F.R. § 42.107, filed October 7, 2014	
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Sheet | 11 | of | 18

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	104.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Exhibits G-1 to G-6 to "Diablo Technologies, Inc.'s Invalidity Contentions," dated June 6, 2014.	
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First Named Inventor	Hyun Lee
Art Unit	2827
Examiner Name	Hoang, Huan
Attorney Docket Number	129980-5070-US

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	109.	Non-final office action, U.S. Patent Application No. 13/288,850, October 11, 2013, 24 pages	
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Art Unit	2827
Examiner Name	Hoang, Huan
Attorney Docket Number	129980-5070-US

US PATENT DOCUMENTS

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	22.	Inter Partes Review of U.S. Patent No. 8756364, Case No. IPR2017-00549, Petition for Inter Partes Review, filed December 30, 2016	
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	Art Unit	2827
(Multiple sheets *used when necessary)*	Examiner	Hoang, Huan
SHEET 17 OF 18	Attorney Docket No.	129980-5070-US

U.S. PATENT APPLICATIONS					
Examiner Initials	Cite No.	Document Number *Number - Kind Code (if known)* Example: 1,234,567 B1	Filing Date MM-DD-YYYY	Name of Patentee or Applicant	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
	54	12/422,912 (Attorney Docket No.NETL.044A)	04-13-2009	Hyun Lee, et al.	
	55	12/422,853 (Attorney Docket No.NETL.045A)	04-13-2009	Hyun Lee, et al.	
	56	12/815,339 (Attorney Docket No.NETL.062A)	06-14-2010	Hyun Lee	

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Foreign Patent Document *Country Code-Number-Kind Code* Example: JP 1234567 A1	Publication Date MM-DD-YYYY	Name of Patentee or Applicant	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear	T1
	57	EP 1 816 570 A2	08-08-2007	Rambus Inc.		
	58	WO 2010-138480	12-02-2010	Rambus Inc.		
	59	WO 2011-049710	04-28-2011	Rambus Inc.		
	60	WO 2011-094437	08-04-2011	Hewlett Packard Development Co.		

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T1
	61	AHMAD et al., "Modeling of peak-to-peak switching noise along a vertical chain of power distribution TSV pairs in a 30 stack of ICs interconnected through TSVs," Norchip Conference, Article Number 5669473, Nov. 15-16, 2010, IEEE Computer Society	
	62	BLACK et al., "Die Stacking (30) Microarchitecture," MICR0-39, 39th Annual IEEE/ACM International Symposium on, Dec. 2006, 469-479, Orlando, FL	
	63	DANESHTALAB et al., "CMIT -A novel cluster-based topology for 30 stacked architectures," 30 Systems Integration Conference (3DIC), 2010 IEEE International, Nov. 16-18, 2010, pp. 1-5	
	64	FUNAYA et al., "Cache partitioning strategies for 3-D stacked vector processors," IEEE 30 System Integration Conference, article no. 5751453, Nov. 16-18, 2010, IEEE Computer Society	
	65	GHOSH et al., "Smart Refresh: An Enhancement Memory Controller Design for Reducing Energy in Conventional and 30 Die-Stacked DRAMs," Microarchitecture, 2007, 40th Annual IEEE/ACM International Symposium, Dec. 1-5, 2007, pp. 134-145.	
	66	KANG et al., "8 Gb 3-D DDR3 DRAM using through-silicon-via technology," IEEE Journal of Solid-State Circuits, v45, n 1, 111-19, Jan. 2010, IEEE, USA	

Examiner Signature	Date Considered

***Examiner:** Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

T[1] - Place a check mark in this area when an English language Translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Application No.	15/602,099
	Filing Date	May 22, 2017
	First Named Inventor	Hyun Lee
	Art Unit	2827
(Multiple sheets *used when necessary)*	Examiner	Hoang, Huan
SHEET 18 OF 18	Attorney Docket No.	129980-5070-US

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T1
	67	KANG et al., "Signal integrity and reliability of a new Multi-Stack Package using a Pressure Conductive Rubber," Electrical Design of Advanced Packaging and Systems Symposium, 214-17, Dec. 2008, Seoul, South Korea	
	68	KAWANO, "A 30 Packaging Technology for High-Density Stacked DRAM," VLSI Technology, Systems and Applications, 2007, 23-25 April 2007, pp. 1-2	
	69	KIM et al., "A Quantitative Analysis of Performance Benefits of 30 Die Stacking on Mobile and Embedded Soc	
	70	KURITA et al., "A 3-D packaging technology with highly-parallel memory/logic interconnect," IEICE Transactions on Electronics, v E92-C, no. 12, pp. 1512-1522, 2009, Maruzen Col, Ltd.	
	71	KURITA et al., "Vertical Integration of Stacked DRAM and High-Speed Logic Device Using SMAFTI Technology," Advanced Packaging, IEEE Transactions, Aug. 2009, Volume 32 Issue 3, pp. 657-665	
	72	"Posts Tagged '30 Stacking'," from Chip Design Mag., http://chipdesignmag.com/lpd/blog/tag/3d-stacking/ (Printed October 13, 2011).	
	73	RUSSELL, Gill, "Intel Micron Hybrid Memory Cube: The Future of Exascale Computing," Bright Side of News. Sept. 19, 2011, <http://www.brightsideofnews.com/news/201l/9/19/intel-micron-hybrid-memory-cube-the-future-of-exascale-computing.aspx> Printed October 13, 2011 in 8 pages.	
	74	LOH, "30-Stacked Memory Architectures for Multi-core Processors," Proceedings of the 35th Annual International Symposium on Computer Architecture (ISCA '08), 453-464, IEEE Computer Society, Washington DC, USA	
	75	VAL, "The 30 interconnection applications for mass memories and microprocessors," Proceedings of the Technical Conference, 1991 International Electronic Packaging Conference, 851-60, vol. 2, 1991, Int. Electron. Packaging Soc, Wheaton, IL, USA, 2008	
	76	WEIS et al., "Design space exploration for 30-stacked DRAMs," Proceedings - Design, Automation and Test in Europe Conference and Exhibition, 2011	
	77	ZHANG et al. "A Customized Design of DRAM Controller for On-Chip 30 DRAM Stacking" Custom Integrated Circuits Conference (CICC), 2010 IEEE, Sept. 19-22 2010, pp. 1-4	
	78	International Search Report and Written Opinion, PCT/US2011/059209, January 31, 2013	

Examiner Signature	Date Considered
***Examiner:** Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

T[1] - Place a check mark in this area when an English language Translation is attached.

Electronically filed October 29, 2018

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun Lee	Confirmation No.:	1757
Serial No.:	15/602,099	Art Unit:	2827
Filed:	May 22, 2017	Examiner:	Hoang, Huan
For:	MEMORY MODULE WITH PACKAGES OF STACKED MEMORY CHIPS	Attorney Docket No.:	129980-5070US

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure provisions of 37 C.F.R. §1.56, there is hereby provided certain information which the Examiner may consider material to the examination of the subject U.S. patent application. It is requested that the Examiner make this information of record if it is deemed material to the examination of the application.

1. Enclosures accompanying this Information Disclosure Statement are:

1a. ☒ A list of all patents, publications, applications, or other information submitted for consideration by the office.

1b. A legible copy of:

☐ Each foreign patent;

☐ Each publication or that portion which caused it to be listed on the PTO-1449;

☐ For each cited pending U.S. application, the application specification including the claims, and any drawing of the application, or portion of the application which caused it to be listed on the PTO-1449 including any claims directed to that portion;

☐ all other information or portion which caused it to be listed on the PTO-1449.

1c. ☐ An English language copy of search report(s) from a counterpart foreign application or PCT International Search Report.

1d. ☐ Explanations of relevancy (ATTACHMENT 1(d), hereto) or English language abstracts of the non-English language publications.

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2. ☒ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(b):

☐ Within three months of the filing date of a national application other than a continued prosecution application under §1.53(d);

☐ Within three months of the date of entry of the national stage as set forth in §1.491 in an international application;

☐ Before the mailing of the first Office action on the merits;

☒ Before the mailing of a first Office action after the filing of a request for continued examination under §1.114.

3. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(c) after the period specified in 37 C.F.R. §1.97(b), but before the mailing date of any of a final action under 37 C.F.R. §1.113, a notice of allowance under 37 C.F.R. §1.311 or an action that otherwise closes prosecution in the application.

(Check either Item 3a, 3b, 3c or 3d)

3a. ☐ The Certification Statement in Item 5 below is applicable. Accordingly, no fee is required.

3b. ☐ The $240 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

3c. ☐ The $120 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

3d. ☐ The $60 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

(Items 3b or 3c to be checked if any reference known for more than 3 months)

4. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(d) after the period specified in 37 C.F.R. §1.97(c), but on or before the date of payment of the issue fee.

(Check Item 4a, and 4b, 4c or 4d)

4a. ☐ The Certification Statement in Item 5 below is applicable.

4b. ☐ The $240 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

4c. ☐ The $120 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

Petitioners
Ex. 1008, p. 182

4d. ☐ The $60 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no.).

5. ☐ Certification Statement (applicable if Item 3a or Item 4a is checked)

(Check either Item 5a, 5b, 5c or 5d)

5a. ☐ In accordance with 37 C.F.R. §1.97(e)(1), it is certified that each item of information contained in this information disclosure statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement.

5b. ☐ In accordance with 37 C.F.R. §1.97(e)(2), it is certified that no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 C.F.R. §1.56(c) more than three months prior to the filing of this information disclosure statement.

5c. ☐ Each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

5d. ☐ Pursuant to 37 C.F.R. §1.704(d), each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

6. ☒ Copies of each cited U.S. patent and each U.S. patent application publication are not enclosed pursuant to the USPTO OG Notice dated 05 August 2003 waiving the requirement under 37 C.F.R. 1.98(a)(2)(i) for U.S. patent applications filed after June 30, 2003.

7. ☒ This application is a continuation application under 37 C.F.R. §1.53(b) or (d).

(Check appropriate Items 7a, 7b and/or 7c)

7a. ☐ A Petition to Withdraw from issue under 37 C.F.R. §1.313(b)(5) is concurrently filed herewith.

7b. ☒ Copies of publications listed on Form PTO-1449 from prior application Serial Nos. **15/095,288**, filed on **April 11, 2016**; **14/337,168**, filed on **July 21, 2014** and **13/288,850**, filed on **November 3, 2011**, of which this application claims priority under 35 U.S.C. §120, are not being submitted pursuant to 37 C.F.R. §1.98(d).

7c. ☐ Copies of the publications listed on the attached Form PTO-1449 that were not previously cited in prior application Serial No. , filed on , are provided

herewith.

8. ☐ This is a Supplemental Information Disclosure Statement. (Check Item 8a)

8a. ☐ This Supplemental Information Disclosure Statement under 37 C.F.R. §1.97(f) supplements the Information Disclosure Statement filed on . A bona fide attempt was made to comply with 37 C.F.R. §1.98, but inadvertent omissions were made. These omissions have been corrected herein. Accordingly, additional time is requested so that this Supplemental Information Disclosure Statement can be considered as if properly filed on .

9. ☐ In accordance with 37 C.F.R. §1.98, a concise explanation of what is presently understood to be the relevance of each non-English language publication is:

(Check Item 9a, 9b, or 9c)

9a. ☐ satisfied because all non-English language publications were cited on the enclosed English language copy of the PCT International Search Report or the search report from a counterpart foreign application indicating the degree of relevance found by the foreign office.

9b. ☐ set forth in the application.

9c. ☐ enclosed as an attachment hereto.

10. ☒ The Commissioner is authorized to charge any additional fee required or credit any overpayment for this Information Disclosure Statement and/or Petition to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5070-US).

11. ☒ No admission is made that the information cited in this Statement is, or is considered to be, material to patentability nor a representation that a search has been made (other than a search report of a foreign counterpart application or PCT International Search Report if submitted herewith). 37 C.F.R. §§1.97(g) and (h).

Respectfully submitted,

Date: October 29, 2018

Gary S. Williams 31,066 (Reg. No.)
MORGAN, LEWIS & BOCKIUS LLP
1400 Page Mill Road
Palo Alto, CA 94304
(650) 843-4000

Petitioners
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INFORMATION DISCLOSURE CITATION Substitute for Form 1449-PTO				*Electronically filed October 29, 2018*	
				Application Number	*15/602,099*
				Filing Date	*May 22, 2017*
				First Named Inventor	*Hyun Lee*
				Art Unit	*2827*
				Examiner Name	*Hoang, Huan*
Sheet	1	of	21	Attorney Docket Number	*129980-5070-US*

PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code[2]	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		6,070,217	05-30-2000	Connolly et al.	
		6,683,372 B1	01-27-2004	Wong et al.	
		6,704,910 B2	03-09-2004	Hong	
		6,721,860 B2	04-13-2004	Klein	
		7,024,518 B2	04-04-2006	Halbert et al.	
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		2006/0277355 A1	12-07-2006	Ellsberry et al.	

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Foreign Patent Document Country Code[3] – Number[4] - Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

NON PATENT LITERATURE DOCUMENTS		
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Patent Owner's Preliminary Response, filed April, 9, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1003, 'Declaration of Dr. Harold Stone,' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1009, 'JEDEC Standard Double Data Rate DDR SDRAM Specification, JESD79 June 2000,' filed December, 22, 2017

Examiner's Signature		Date Considered	

INFORMATION DISCLOSURE CITATION Substitute for Form 1449-PTO				*Electronically filed October 29, 2018*	
				Application Number	***15/602,099***
				Filing Date	***May 22, 2017***
				First Named Inventor	***Hyun Lee***
				Art Unit	***2827***
				Examiner Name	***Hoang, Huan***
Sheet	2	of	21	Attorney Docket Number	***129980-5070-US***

		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1010, 'JEDEC Standard 21-C, DDR SDRAM Registered DIMM Design Specification January 2002,' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1011, 'JEDEC Standard DDR2 SDRAM Specification, JESD79-2B January 2005,' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1012, 'Declaration of John J. Kelly Regarding Records of Joint Electron Device Engineering Council JEDEC,' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1022, 'Decision Denying Institution of Inter Partes Review of U.S. Patent No. 8,516,185, SanDisk Corp. v. Netlist, Inc., IPR2014-01029, Paper No. 11 Dec. 16, 2014,' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1023, 'Decision Denying Institution of Inter Partes Review of U.S. Patent No. 8,516,185, Smart Modular Techs. Inc. v. Netlist, Inc., IPR2014-01369, Paper No. 12 Mar. 9, 2015,' filed December, 22, 2017
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		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1025, 'Complainant Netlist, Inc.'s Initial Post-Hearing Brief, Certain Memory Modules and Components Thereof, and Products Containing Same, Inv. No. 337-TA-1023 May 30, 2017 excerpts relevant to '185 patent,' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1026, 'Respondents' Post-Hearing Brief, Certain Memory Modules and Components Thereof, and Products Containing Same, Inv. No. 337-TA-1023 May 30, 2017 excerpts relevant to '185 patent,' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1027, 'High-quality versions of demonstrative graphics included in Respondents' Post-Hearing Brief (Ex.1026),' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1028, 'Complainant Netlist Inc.'s Reply Post-Hearing Brief, Certain Memory Modules and Components Thereof, and Products Containing Same, Inv. No. 337-TA-1023 (June 9, 2017) (excerpts relevant to '185 patent),' filed December, 22, 2017

Examiner's Signature		Date Considered	

INFORMATION DISCLOSURE CITATION Substitute for Form 1449-PTO				*Electronically filed October 29, 2018*	
				Application Number	***15/602,099***
				Filing Date	***May 22, 2017***
				First Named Inventor	***Hyun Lee***
				Art Unit	***2827***
				Examiner Name	***Hoang, Huan***
Sheet	3	of	21	Attorney Docket Number	***129980-5070-US***

		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1029, 'Respondents' Reply Post-Hearing Brief, Certain Memory Modules and Components Thereof, and Products Containing Same, Inv. No. 337-TA-1023 (June 9, 2017) (excerpts relevant to '185 patent),' filed December, 22, 2017
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		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1031, 'Institution of Inter Partes Review of U.S. Patent No. 8,516,185, SK hynix Inc. et al. v. Netlist, Inc., IPR2017-00577, Paper No. 8 (July 7, 2017),' filed December, 22, 2017.
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1032, 'Final Written Decision, Diablo Techs., Inc. v. Netlist, Inc., IPR2014-00882, Paper No. 33 (Dec. 14, 2015),' filed December, 22, 2017.
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1033, 'Netlist, Inc. v. Diablo Techs., Inc., No. 2016-1742 (Fed. Cir. July 25, 2017),' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1034, 'Netlist's Infringement Claim Chart for U.S. Patent No. 9,606,907 June 14, 2017,' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1035, 'Stone, H.S. Microcomputer Interfacing, Reading, MA: Addison Wesley, 1982,' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1039, 'Intel E7525 Memory Controller Hub (MCH) Chipset Datasheet (June 2004),' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1040, 'Initial Determination, Certain Memory Modules and Components Thereof, and Products Containing Same, Inv. No. 337-TA-1023 (Nov. 14, 2017) (redacted excerpts),' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1041, 'Bruce Jacob et al., Memory System: Cache, DRAM, Disk (2008) (excerpts),' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1042, 'Direct RDRAM datasheet (2000),' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Petition for Review of U.S. Patent No. 9,606,907, filed December, 22, 2017

Examiner's Signature		Date Considered	

INFORMATION DISCLOSURE CITATION Substitute for Form 1449-PTO				*Electronically filed October 29, 2018*	
				Application Number	***15/602,099***
				Filing Date	***May 22, 2017***
				First Named Inventor	***Hyun Lee***
				Art Unit	***2827***
				Examiner Name	***Hoang, Huan***
Sheet	4	of	21	Attorney Docket Number	***129980-5070-US***

		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Preliminary Response, filed April 10, 2018
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00364, Petition for Inter Partes Review of U.S. Patent No. 9,606,907, filed December, 27, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00365, Petition for Inter Partes Review of U.S. Patent No. 9,606,907, filed December, 27, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petition for Inter Partes Review, filed December, 30, 2016
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Patent Owner's Preliminary Response, filed April, 9, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Patent Owner's Response, filed September, 15, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petitioners' Objections to Evidence, filed September, 22, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petitioners Motion to Exclude Certain Inadmissible Testimony of Patent Owners Expert Carl Sechen, filed January, 9, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petitioners Request for Oral Hearing, filed January, 9, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, PO Request for Oral Argument, filed January, 9, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, PO Motion for Observations, filed January, 9, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petitioners' Response to Patent Owner's Motion for Observations, filed January, 23, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, PO's Opposition to Petitioner's Motion to Exclude, filed January, 23, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petitioners' Reply In Support Of Motion to Exclude Certain Inadmissible Testimony Of Patent Owner's Expert Carl Sechen, filed January, 30, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petitioners' Updated Exhibit List, filed February, 9, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Patent Owner's Updated Exhibit List, filed February, 9, 2018
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Trial Instituted Document, filed May, 15, 2017
		Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, ORDER Trial Hearing, filed January, 25, 2018

Examiner's Signature		Date Considered	

INFORMATION DISCLOSURE CITATION Substitute for Form 1449-PTO				*Electronically filed October 29, 2018*	
				Application Number	***15/602,099***
				Filing Date	***May 22, 2017***
				First Named Inventor	***Hyun Lee***
				Art Unit	***2827***
				Examiner Name	***Hoang, Huan***
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				First Named Inventor	***Hyun Lee***
				Art Unit	***2827***
				Examiner Name	***Hoang, Huan***
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				Art Unit	*2827*
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		U.S. District Court Northern District of California, Case No. CV08 04144, Google Inc. v. Netlist, Inc., Defendant Netlist, lnc.'s Opening Claim Construction Brief, filed July 28, 2009 in 21 pages.
		U.S. District Court Northern District of California, Case No. CV08 04144, Google Inc. v. Netlist, Inc., Defendant Netlist, lnc.'s Opposition to Google Inc's Motion for Summary Judgment of Invalidity, filed July 6, 2010 in 13 pages.
		U.S. District Court Northern District of California, Case No. CV08 04144, Google Inc. v. Netlist, Inc., Exhibit A To Joint Claim Construction And Prehearing Statement, filed June 12, 2009 in 2 pages.

Examiner Signature		Date Considered	

INFORMATION DISCLOSURE CITATION Substitute for Form 1449-PTO				*Electronically filed October 29, 2018*	
				Application Number	*15/602,099*
				Filing Date	*May 22, 2017*
				First Named Inventor	*Hyun Lee*
				Art Unit	*2827*
				Examiner Name	*Hoang, Huan*
Sheet	15	of	21	Attorney Docket Number	*129980-5070-US*

		U.S. District Court Northern District of California, Case No. CV08 04144, Google Inc. v. Netlist, Inc., Exhibit B to Joint Claim Construction and Prehearing Statement, filed June 12, 2009 in 36 pages.
		U.S. District Court Northern District of California, Case No. CV08 04144, Google Inc. v. Netlist, Inc., Joint Claim Construction and Prehearing Statement, filed June 12, 2009 in 5 pages.
		U.S. District Court Northern District of California, Case No. CV08 04144, Google Inc. v. Netlist, Inc., Netlist, lnc.'s Answer to Complaint and Counterclaims, filed Nov. 18, 2008 in 9 pages.
		U.S. District Court Northern District of California, Case No. CV08 04144, Google Inc. v. Netlist, Inc., Order Re Claim Construction, filed Nov. 16, 2009 in 1 page.
		U.S. District Court Northern District of California, Case No. CV08 04144, Google Inc. v. Netlist, Inc., Plaintiff Google's Reply to Counterclaims, filed Dec. 8, 2008 in 4 pages.
		U.S. District Court Northern District of California, Case No. CV08 04144, Google Inc. v. Netlist, Inc., Stipulation Re: Additional Agreed-Upon Claim Constructions, filed Oct. 28, 2009 in 3 pages.
		U.S. District Court Northern District of California, Case No. CV08 04144, GOOGLE INC. vs. NETLIST, INC., [Redacted] Google lnc.'s Responsive Claim Construction Brief, filed Aug. 25, 2009 in 30 pages.
		U.S. District Court Northern District of California, Case No. CV08 04144, GOOGLE INC. vs. NETLIST, INC., Amended Exhibit A To Joint Claim Construction And Prehearing Statement, filed Oct. 28, 2009 in 1 page.
		U.S. District Court Northern District of California, Case No. CV08 04144, GOOGLE INC. vs. NETLIST, INC., Appendix 1 To Google's Responsive Claim Construction Brief, filed Nov. 12, 2009 in 4 pages.
		U.S. District Court Northern District of California, Case No. CV08 04144, GOOGLE INC. vs. NETLIST, INC., Attachment 1 to Exhibit B To Joint Claim Construction And Prehearing Statement, filed June 12, 2009 in 7 pages.
		U.S. District Court Northern District of California, Case No. CV08 04144, GOOGLE INC. vs. NETLIST, INC., Attachment 2 To Exhibit B To Joint Claim Construction And Prehearing Statement, filed June 12, 2009 in 12 pages.
		U.S. District Court Northern District of California, Case No. CV08 04144, GOOGLE INC. vs. NETLIST, INC., Complaint for Declaratory Relief, filed Aug. 29, 2008 in 49 pages.

Examiner Signature		Date Considered	

DB2/ 33259060.1

INFORMATION DISCLOSURE CITATION Substitute for Form 1449-PTO				*Electronically filed October 29, 2018*	
				Application Number	*15/602,099*
				Filing Date	*May 22, 2017*
				First Named Inventor	*Hyun Lee*
				Art Unit	*2827*
				Examiner Name	*Hoang, Huan*
Sheet	16	of	21	Attorney Docket Number	*129980-5070-US*

		U.S. District Court Northern District of California, Case No. CV09 05718, Netlist, Inc. vs. Google, Inc., Complaint For Patent Infringement, filed Dec. 4, 2009 in 47 pages.
		U.S. District Court Northern District of California, Case No. CV09 05718, NETLIST, INC. vs. GOOGLE, INC., Defendant Google Inc's Responsive Claim Construction Brief, filed Aug. 4, 2010 in 108 pages.
		U.S. District Court Northern District of California, Case No. CV09 05718, Netlist, Inc. vs. Google, Inc., Exhibit A to Joint Claim Construction and Prehearing Statement under Patent L. R. 4-3, filed June 25, 2010 in 2 pages.
		U.S. District Court Northern District of California, Case No. CV09 05718, Netlist, Inc. vs. Google, Inc., Exhibit B to Joint Claim Construction and Prehearing Statement under Patent L. R. 4-3, filed Jun. 25, 2010 in 23 pages.
		U.S. District Court Northern District of California, Case No. CV09 05718, Netlist, Inc. vs. Google, Inc., Google's Answer to Plaintiff's Complaint for Patent Infringement; and Assertion of Counterclaims, filed Feb. 12, 2010 in 13 pages.
		U.S. District Court Northern District of California, Case No. CV09 05718, Netlist, Inc. vs. Google, Inc., Joint Claim Construction And Prehearing Statement Under Patent Local Rule 4-3, filed June 25, 2010 in 5 pages.
		U.S. District Court Northern District of California, Case No. CV09 05718, Netlist, Inc. vs. Google, Inc., Plaintiff Netlist, lnc.'s Reply Claim Construction Brief, filed Aug. 16, 2010 in 17 pages.
		U.S. District Court Northern District of California, Case No. CV09 05718, Netlist, Inc. vs. Google, Inc., Plaintiff Netlist, lnc.'s Reply to Defendant Google lnc.'s Counterclaim, filed March 8, 2010 in 11 pages.
		U.S. District Court Northern District of California, Case No. CV09 05718, Netlist, Inc. vs. Google, Inc., Plaintiff Netlist, Inc's Opening Claim Construction Brief, filed Jul. 16, 2010 in 162 pages.
		US District Court Civil Docket; Google Inc. v. Netlist Inc.; 4:08cv04144; filed Aug. 29, 2008.
		US District Court Civil Docket; Netlist Inc. v. Google Inc.; 4:09cv5718, filed Dec. 4, 2009 in 10 pages.
		US District Court Civil Docket; Netlist Inc. v. lnphi Corporation; 2:09cv6900; Date filed Sep. 22, 2009.
		Vogt, Pete, "Fully Buffered DIMM (FB-DIMM) Server Memory Architecture: Capacity, Performance, Reliability, and Longevity," Intel, Feb. 18, 2004, 33 pages.

Examiner Signature		Date Considered	

INFORMATION DISCLOSURE CITATION Substitute for Form 1449-PTO				*Electronically filed October 29, 2018*	
				Application Number	*15/602,099*
				Filing Date	*May 22, 2017*
				First Named Inventor	*Hyun Lee*
				Art Unit	*2827*
				Examiner Name	*Hoang, Huan*
Sheet	17	of	21	Attorney Docket Number	*129980-5070-US*

US PATENT APPLICATIONS					
Examiner Initials	Cite No.	Application Number	Filing Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Reexam Appl. No. 95/000,546 for U.S. Pat. No. 7,289,386	05/11/2010	Netlist, Inc.	Entire File History
		Reexam Appl. No. 95/000,577 for U.S. Pat. No. 7,289,386	10/20/2010	Netlist, Inc.	Entire File History
		Reexam Appl. No. 95/000,578 for U.S. Pat. No. 7,619,912	10/20/2010	Netlist, Inc.	Entire File History
		Reexam Appl. No. 95/000,579 for U.S. Pat. No. 7,619,912	10/21/2010	Netlist, Inc.	Entire File History
		Reexam App. No. 95/001,337 for U.S. Pat. No. 7,636,274	06/04/2010	Netlist, Inc.	Entire File History
		Reexam Appl. No. 95/001,381 for U.S. Pat. No. 7,532,537	06/09/2010	Netlist, Inc.	Entire File History
		Reexam Appl. No. 95/001,338; for U.S. Pat. No. 7,532,537	04/19/2010	Netlist, Inc.	Entire File History
		Reexam Appl. No. 95/001,758 for U.S. Pat. No. 7,864,627	09/15/2010	Netlist, Inc.	Entire File History
		Reexam Appl. No. 95/001,339 for U.S. Pat. No. 7,619,912	06/08/2010	Netlist, Inc.	Entire File History

Examiner Signature		Date Considered	

INFORMATION DISCLOSURE CITATION Substitute for Form 1449-PTO				*Electronically filed October 29, 2018*	
				Application Number	*15/602,099*
				Filing Date	*May 22, 2017*
				First Named Inventor	*Hyun Lee*
				Art Unit	*2827*
				Examiner Name	*Hoang, Huan*
Sheet	18	of	21	Attorney Docket Number	*129980-5070-US*

		Reexam Appl. No. 95/002,399 for U.S. Pat. No. 8,250,295	09/15/2010	Netlist, Inc.	Entire File History
		11/075,395	03/07/2005	Netlist, Inc.	Entire Prosecution History
		11/173,175	07/01/2005	Netlist, Inc.	Entire Prosecution History
		11/862,931	09/27/2007	Netlist, Inc.	Entire Prosecution History
		12/577,682	10/12/2009	Netlist, Inc.	Entire Prosecution History
		12/954,492	11/24/2010	Netlist, Inc.	Entire Prosecution History
		12/912,623	10/26/2010	Netlist, Inc.	Entire Prosecution History
		11/335,875	01/19/2006	Netlist, Inc.	Entire Prosecution History
		12/408,652	03/20/2009	Netlist, Inc.	Entire Prosecution History
		12/629,827	12/02/2009	Netlist, Inc.	Entire Prosecution History
		12/955,711	11/29/2010	Netlist, Inc.	Entire Prosecution History
		12/981,380	12/29/2010	Netlist, Inc.	Entire Prosecution History
		13/154,172	06/06/2011	Netlist, Inc.	Entire Prosecution History
		13/287,042	11/01/2011	Netlist, Inc.	Entire Prosecution History
		13/473,413	05/16/2012	Netlist, Inc.	Entire Prosecution History
		13/032,470	02/22/2011	Netlist, Inc.	Entire Prosecution History
		13/287,081	11/01/2011	Netlist, Inc.	Entire Prosecution History
		13/971,231	08/20/2013	Netlist, Inc.	Entire Prosecution History

Examiner Signature		Date Considered	

INFORMATION DISCLOSURE CITATION Substitute for Form 1449-PTO				*Electronically filed October 29, 2018*	
				Application Number	*15/602,099*
				Filing Date	*May 22, 2017*
				First Named Inventor	*Hyun Lee*
				Art Unit	*2827*
				Examiner Name	*Hoang, Huan*
Sheet	19	of	21	Attorney Docket Number	*129980-5070-US*

		12/422,853	04/13/2009	Netlist, Inc.	Entire Prosecution History
		13/412,243	03/05/2012	Netlist, Inc.	Entire Prosecution History
		12/422,925	04/13/2009	Netlist, Inc.	Entire Prosecution History
		13/183,253	07/14/2011	Netlist, Inc.	Entire Prosecution History
		13/745,790	01/19/2013	Netlist, Inc.	Entire Prosecution History
		14/229,844	03/29/2014	Netlist, Inc.	Entire Prosecution History
		12/504,131	07/16/2009	Netlist, Inc.	Entire Prosecution History
		12/761,179	04/15/2010	Netlist, Inc.	Entire Prosecution History
		13/288,850	11/03/2011	Netlist, Inc.	Entire Prosecution History
		13/411,344	03/02/2012	Netlist, Inc.	Entire Prosecution History
		13/952,599	07/27/2013	Netlist, Inc.	Entire Prosecution History

Examiner Signature		Date Considered	

INFORMATION DISCLOSURE CITATION Substitute for Form 1449-PTO				*Electronically filed October 29, 2018*	
				Application Number	*15/602,099*
				Filing Date	*May 22, 2017*
				First Named Inventor	*Hyun Lee*
				Art Unit	*2827*
				Examiner Name	*Hoang, Huan*
Sheet	20	of	21	Attorney Docket Number	*129980-5070-US*

PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code[2]	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		7,024,518 B2	04-04-2006	Halbert et al.	
		9,606,907 B2	03-28-2017	Lee et al.	
		2009/0228631 A1	09-10-2009	Marulkar et al.	

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Foreign Patent Document Country Code[3] – Number[4] - Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
		CN102576565B	09-30-2015	Netlist, Inc.		

NON PATENT LITERATURE DOCUMENTS		
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
		Netlist, Inc., Examination Decision of Request for Invalidation, CN201080039043.0, 30MAY2018, 43 pgs.
		Inter Partes Review of US Patent No. 8,516,185 B2, Case No. IPR2017-00577, Record of Oral Hearing, filed June 19, 2018.
		Inter Partes Review of US Patent No. 8,516,185 B2, Case No. IPR2017-00577, Final Written Decision, filed July 5, 2018.
		Inter Partes Review of US Patent No. 7,532,537 B2, Case No. IPR2017-00667, Final Written Decision, filed July 18, 2018
		Inter Partes Review of US Patent No. 7,532,537 B2, Case No. IPR2017-00668, Final Written Decision, filed July 18, 2018.
		Inter Partes Review of US Patent No. 9,606,907 B2, Case No. IPR2018-00362, ORDER, *Conduct of the Proceedings*, filed August 2, 2018
		Inter Partes Review of US Patent No. 9,606,907 B2, Case No. IPR2018-00362, and Case No. IPR2018-00363, Decision Granting Institution of *Inter Partes* Review, filed August 6, 2018
		Inter Partes Review of US Patent No. 9,606,907 B2, Case No. IPR2018-00362, and Case No. IPR2018-00363, EXHIBIT 3001, 'email from Mehran Arjomand,' filed July 30, 2018

Examiner's Signature		Date Considered	

DB2/ 34183565.1

INFORMATION DISCLOSURE CITATION Substitute for Form 1449-PTO				*Electronically filed October 29, 2018*	
				Application Number	***15/602,099***
				Filing Date	***May 22, 2017***
				First Named Inventor	***Hyun Lee***
				Art Unit	***2827***
				Examiner Name	***Hoang, Huan***
Sheet	21	of	21	Attorney Docket Number	***129980-5070-US***

		Inter Partes Review of US Patent No. 9,606,907 B2, Case No. IPR2018-00362, and Case No. IPR2018-00363, EXHIBIT 3001, 'email from Michael D. Hatcher,' filed July 30, 2018
		Inter Partes Review of US Patent No.9,606,907 B2, Case No. IPR2018-00364, and Case No. IPR2018-00365, Decision Granting Institution of *Inter Partes* Review, filed June 29, 2018
		Inter Partes Review of US Patent No.9,606,907 B2, Case No. IPR2018-00364, Patent Owner's Objections to Petition Evidence, filed August 20, 2018
		Lee, Office Action, US15/470,856, 06OCT2017, 12 pgs.
		Lee, Final Office Action, US15/470,856, 27JUL2018, 52 pgs.

Examiner's Signature		Date Considered	

DB2/ 34183565.1

Electronically filed October 29, 2018

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun Lee	Confirmation No.:	1757
Serial No.:	15/602,099	Art Unit:	2827
Filed:	May 22, 2017	Examiner:	Hoang, Huan
For:	MEMORY MODULE WITH PACKAGES OF STACKED MEMORY CHIPS	Attorney Docket No.:	129980-5070US

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Enclosed for filing in the above-identified application is a Form PTO/SB/08a/b Equivalent listing 475 references. Copies of foreign documents and/or their translation and non-patent literature are submitted on commonly-owned U.S. Pat. App. No. 15/470,856, filed March 27, 2017; 13/970,606, filed August 20, 2013; 12/761,179, filed April 15, 2010, and 12/504,131, filed July 16, 2009, which are accessible via PAIR.

The applicants would appreciate the Examiner initialing and returning the Form PTO/SB/08a/b Equivalent indicating that the information has been considered and made of record herein.

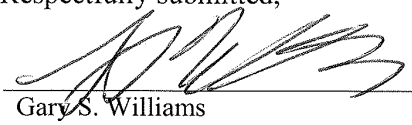
The information contained in this Information Disclosure Statement is not to be construed as a representation that: (i) a complete search has been made; (ii) additional information material to this application does not exist; (iii) the information, protocols, results and the like reported by third parties are accurate or enabling; or (iv) the above information constitutes prior art to the subject invention.

Petitioners
Ex. 1008, p. 206

This Information Disclosure Statement is being filed with the filing of a Request for Continued Examination, and presumably no fee is required. The Commissioner is authorized to charge any required fees to Deposit Account No. 50-0310 (order no. 129980-5070-US).

Respectfully submitted,

Date: October 29, 2018



31,066
(Reg. No.)

Gary S. Williams
MORGAN, LEWIS & BOCKIUS LLP
1400 Page Mill Road
Palo Alto, CA 94304
(650) 843-4000

Petitioners
Ex. 1008, p. 207

Electronic Patent Application Fee Transmittal

Application Number:	15602099
Filing Date:	22-May-2017
Title of Invention:	MEMORY MODULE WITH PACKAGES OF STACKED MEMORY CHIPS
First Named Inventor/Applicant Name:	Hyun Lee
Filer:	Gary Scott Williams/Edith Fuentes
Attorney Docket Number:	129980-5070US

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
RCE- 1ST REQUEST	1801	1	1300	1300
		Total in USD ($)		**1300**

Electronic Acknowledgement Receipt

EFS ID:	34152536
Application Number:	15602099
International Application Number:	
Confirmation Number:	1757
Title of Invention:	MEMORY MODULE WITH PACKAGES OF STACKED MEMORY CHIPS
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Gary Scott Williams/Edith Fuentes
Filer Authorized By:	Gary Scott Williams
Attorney Docket Number:	129980-5070US
Receipt Date:	29-OCT-2018
Filing Date:	22-MAY-2017
Time Stamp:	22:19:48
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$1300
RAM confirmation Number	103018INTEFSW00007857500310
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Continued Examination (RCE)	129980-5070US_RCE.pdf	97823 5919e830ae3975becdd5b3b08f76dca2a4790c7c	no	1
Warnings:					
This is not a USPTO supplied RCE SB30 form.					
Information:					
2		129980-5070US_1st-IDS.pdf	618696 a818ac4f77254d0e49e4a3717374aa4ee5adb8a5	yes	22

Multipart Description/PDF files in .zip description		
Document Description	**Start**	**End**
Information Disclosure Statement (IDS) Form (SB08)	5	22
Transmittal Letter	1	4

Warnings:					
Information:					
3		129980-5070US-2nd-IDS.pdf	354594 a9cdeb67903cca4c7fff9531f0f33380dfd6efdf	yes	23

Multipart Description/PDF files in .zip description		
Document Description	**Start**	**End**
Information Disclosure Statement (IDS) Form (SB08)	3	23
Transmittal Letter	1	2

Warnings:					
Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	30330 22ca6af59fda381e0069e7f18ad896bdfa4a03f6	no	2

Warnings:	
Information:	
Total Files Size (in bytes):	1101443

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

79141 7590 12/26/2018
Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304

EXAMINER
HOANG, HUAN

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 12/26/2018

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/602,099	05/22/2017	Hyun Lee	129980-5070US	1757

TITLE OF INVENTION: MEMORY MODULE WITH PACKAGES OF STACKED MEMORY CHIPS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0.00	$0.00	$1000	03/26/2019

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

Petitioners
Ex. 1008, p. 213

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

79141 7590 12/26/2018
Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/602,099	05/22/2017	Hyun Lee	129980-5070US	1757

TITLE OF INVENTION: MEMORY MODULE WITH PACKAGES OF STACKED MEMORY CHIPS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0.00	$0.00	$1000	03/26/2019

EXAMINER	ART UNIT	CLASS-SUBCLASS
HOANG, HUAN	2827	365-063000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑ Issue Fee ❑ Publication Fee (if required) ❑ Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

❑ Electronic Payment via EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (08-18) Approved for use through 01/31/2020 OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Petitioners
Ex. 1008, p. 214

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/602,099	05/22/2017	Hyun Lee	129980-5070US	1757

79141 7590 12/26/2018

Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304

EXAMINER	
HOANG, HUAN	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 12/26/2018

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 02/11)

Petitioners
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OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 15/602,099	Applicant(s) Lee, Hyun	
	Examiner HUAN HOANG	Art Unit 2827	AIA Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to the RCE filed on 10/29/18.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 1-20 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file areply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☑ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/HUAN HOANG/
Primary Examiner, Art Unit 2827

Petitioners
Ex. 1008, p. 217

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/602,099	Lee, Hyun
	Examiner	**Art Unit**
	HUAN HOANG	2827

CPC						
Symbol					**Type**	**Version**
G11C	/	5	/	066	F	2013-01-01
G11C	/	5	/	06	I	2013-01-01
G11C	/	7	/	1057	I	2013-01-01
G11C	/	7	/	1084	I	2013-01-01
G11C	/	7	/	12	I	2013-01-01

CPC Combination Sets							
Symbol					**Type**	**Set**	**Ranking**	**Version**
	/		/					

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	20	
/HUAN HOANG/ Primary Examiner, Art Unit 2827	17 December 2018	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2

U.S. Patent and Trademark Office — Part of Paper No.: 20181217

Petitioners
Ex. 1008, p. 218

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/602,099	Lee, Hyun
	Examiner	**Art Unit**
	HUAN HOANG	2827

INTERNATIONAL CLASSIFICATION				
CLAIMED				
G11C	/	5	/	06

NON-CLAIMED				
	/		/	

US ORIGINAL CLASSIFICATION	
CLASS	**SUBCLASS**
365	63

CROSS REFERENCES(S)						
CLASS	**SUBCLASS (ONE SUBCLASS PER BLOCK)**					

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	20	
/HUAN HOANG/ Primary Examiner, Art Unit 2827	17 December 2018	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2

U.S. Patent and Trademark Office — Part of Paper No.: 20181217

Petitioners
Ex. 1008, p. 219

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/602,099	Lee, Hyun
	Examiner	**Art Unit**
	HUAN HOANG	2827

☑ Claims renumbered in the same order as presented by applicant ☐ CPA ☑ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		10		19										
	2		11		20										
	3		12												
	4		13												
	5		14												
	6		15												
	7		16												
	8		17												
	9		18												

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	20	
/HUAN HOANG/ Primary Examiner, Art Unit 2827	17 December 2018	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2

Petitioners
Ex. 1008, p. 220

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/602,099	Lee, Hyun
	Examiner	Art Unit
	HUAN HOANG	2827

CPC - Searched*		
Symbol	**Date**	**Examiner**
G11C 5/066, G11C 5/06, G11C 7/1057, G11C 7/1084, G11C 7/12	7/22/17	HH
Above Updated	07/17/18	HH
Above Updated	12/17/2018	HH

CPC Combination Sets - Searched*		
Symbol	**Date**	**Examiner**

US Classification - Searched*			
Class	**Subclass**	**Date**	**Examiner**
365	63	7/22/17	HH
Above	Updated	07/17/18	HH
Above	Updated	12/17/2018	HH

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	**Date**	**Examiner**
EAST (text search)	7/22/17	HH
EAST (text search)	07/17/18	HH
Inventor search	07/17/18	HH
EAST (text search)	12/17/2018	HH
Inventor search	12/17/2018	HH

/HUAN HOANG/ Primary Examiner.Art Unit 2827	

Petitioners
Ex. 1008, p. 221

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/602,099	Lee, Hyun
	Examiner	Art Unit
	HUAN HOANG	2827

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
	EAST (US-PGPUB)	07/17/18	HH
	EAST (US-PGPUB)	12/17/2018	HH

/HUAN HOANG/ Primary Examiner.Art Unit 2827	

Petitioners
Ex. 1008, p. 222

INFORMATION DISCLOSURE CITATION Substitute for Form 1449-PTO				*Electronically filed October 29, 2018*	
				Application Number	*15/602,099*
				Filing Date	*May 22, 2017*
				First Named Inventor	*Hyun Lee*
				Art Unit	*2827*
				Examiner Name	*Hoang, Huan*
Sheet	1	of	21	Attorney Docket Number	*129980-5070-US*

PATENT DOCUMENTS

Examiner Initials	Cite No.	Document Number Number - Kind Code[2]	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		6,070,217	05-30-2000	Connolly et al.	
		6,683,372 B1	01-27-2004	Wong et al.	
		6,704,910 B2	03-09-2004	Hong	
		6,721,860 B2	04-13-2004	Klein	
		7,024,518 B2	04-04-2006	Halbert et al.	
		7,334,150 B2	02-19-2008	Ruckerbauer et al.	
		8,081,536 B1	12-20-2011	Solomon et al.	
		8,130,560 B1	03-06-2012	Rajan et al.	
		8,417,870 B2	04-09-2013	Lee et al.	
		8,756,364 B1	06-17-2014	Bhakta et al.	
		2002/0112119 A1	08-15-2002	Halbert et al.	
		2005/0281096 A1	12-22-2005	Bhakta et al.	
		2006/0117152 A1	06-01-2006	Amidi et al.	
		2006/0277355 A1	12-07-2006	Ellsberry et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials	Cite No.	Foreign Patent Document Country Code[3] – Number[4] - Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Patent Owner's Preliminary Response, filed April, 9, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1003, 'Declaration of Dr. Harold Stone,' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1009, 'JEDEC Standard Double Data Rate DDR SDRAM Specification, JESD79 June 2000,' filed December, 22, 2017

Examiner's Signature		Date Considered	

DB2/ 33227625.1

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.H/

INFORMATION DISCLOSURE CITATION Substitute for Form 1449-PTO				*Electronically filed October 29, 2018*	
				Application Number	*15/602,099*
				Filing Date	*May 22, 2017*
				First Named Inventor	*Hyun Lee*
				Art Unit	*2827*
				Examiner Name	*Hoang, Huan*
Sheet	2	of	21	Attorney Docket Number	*129980-5070-US*

		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1010, 'JEDEC Standard 21-C, DDR SDRAM Registered DIMM Design Specification January 2002,' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1011, 'JEDEC Standard DDR2 SDRAM Specification, JESD79-2B January 2005,' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1012, 'Declaration of John J. Kelly Regarding Records of Joint Electron Device Engineering Council JEDEC,' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1022, 'Decision Denying Institution of Inter Partes Review of U.S. Patent No. 8,516,185, SanDisk Corp. v. Netlist, Inc., IPR2014-01029, Paper No. 11 Dec. 16, 2014,' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1023, 'Decision Denying Institution of Inter Partes Review of U.S. Patent No. 8,516,185, Smart Modular Techs. Inc. v. Netlist, Inc., IPR2014-01369, Paper No. 12 Mar. 9, 2015,' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1024, 'Excerpts from the Hearing in Certain Memory Modules and Components Thereof, and Products Containing Same, Inv. No. 337-TA-1023 May 8, 2017,' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1025, 'Complainant Netlist, Inc.'s Initial Post-Hearing Brief, Certain Memory Modules and Components Thereof, and Products Containing Same, Inv. No. 337-TA-1023 May 30, 2017 excerpts relevant to '185 patent,' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1026, 'Respondents' Post-Hearing Brief, Certain Memory Modules and Components Thereof, and Products Containing Same, Inv. No. 337-TA-1023 May 30, 2017 excerpts relevant to '185 patent,' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1027, 'High-quality versions of demonstrative graphics included in Respondents' Post-Hearing Brief (Ex.1026),' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1028, 'Complainant Netlist Inc.'s Reply Post-Hearing Brief, Certain Memory Modules and Components Thereof, and Products Containing Same, Inv. No. 337-TA-1023 (June 9, 2017) (excerpts relevant to '185 patent),' filed December, 22, 2017

Examiner's Signature		Date Considered	

DB2/ 33227625.1

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.H/

INFORMATION DISCLOSURE CITATION Substitute for Form 1449-PTO				*Electronically filed October 29, 2018*	
				Application Number	*15/602,099*
				Filing Date	*May 22, 2017*
				First Named Inventor	*Hyun Lee*
				Art Unit	*2827*
				Examiner Name	*Hoang, Huan*
Sheet	3	of	21	Attorney Docket Number	*129980-5070-US*

		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1029, 'Respondents' Reply Post-Hearing Brief, Certain Memory Modules and Components Thereof, and Products Containing Same, Inv. No. 337-TA-1023 (June 9, 2017) (excerpts relevant to '185 patent),' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1030, 'High-quality versions of demonstrative graphics included in Respondents' Reply Post-Hearing Brief (Ex.1029),' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1031, 'Institution of Inter Partes Review of U.S. Patent No. 8,516,185, SK hynix Inc. et al. v. Netlist, Inc., IPR2017-00577, Paper No. 8 (July 7, 2017),' filed December, 22, 2017.
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1032, 'Final Written Decision, Diablo Techs., Inc. v. Netlist, Inc., IPR2014-00882, Paper No. 33 (Dec. 14, 2015),' filed December, 22, 2017.
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1033, 'Netlist, Inc. v. Diablo Techs., Inc., No. 2016-1742 (Fed. Cir. July 25, 2017),' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1034, 'Netlist's Infringement Claim Chart for U.S. Patent No. 9,606,907 June 14, 2017,' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1035, 'Stone, H.S. Microcomputer Interfacing, Reading, MA: Addison Wesley, 1982,' filed December, 22, 2017
		Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1039, 'Intel E7525 Memory Controller Hub (MCH) Chipset Datasheet (June 2004),' filed December, 22, 2017
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				Application Number	*15/602,099*
				Filing Date	*May 22, 2017*
				First Named Inventor	*Hyun Lee*
				Art Unit	*2827*
				Examiner Name	*Hoang, Huan*
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				First Named Inventor	*Hyun Lee*
				Art Unit	*2827*
				Examiner Name	*Hoang, Huan*
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				First Named Inventor	*Hyun Lee*
				Art Unit	*2827*
				Examiner Name	*Hoang, Huan*
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				Filing Date	*May 22, 2017*
				First Named Inventor	*Hyun Lee*
				Art Unit	*2827*
				Examiner Name	*Hoang, Huan*
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				Art Unit	*2827*
				Examiner Name	*Hoang, Huan*
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				Art Unit	*2827*
				Examiner Name	*Hoang, Huan*
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				Art Unit	*2827*
				Examiner Name	*Hoang, Huan*
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Examiner Signature		Date Considered	

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.H/

INFORMATION DISCLOSURE CITATION Substitute for Form 1449-PTO				*Electronically filed October 29, 2018*	
				Application Number	*15/602,099*
				Filing Date	*May 22, 2017*
				First Named Inventor	*Hyun Lee*
				Art Unit	*2827*
				Examiner Name	*Hoang, Huan*
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		Non-Final Action mailed August 27, 2010, for Control No. 95/000,546, filed May 11, 2010, 16 pages.
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		Non-Final Action mailed September 27, 2011, for Control No. 95/001,337, filed April 19, 2010, 19 pages.
		Non-Final Action mailed October 4, 2011, for Control No. 95/001,339, filed April 20, 2010, 77 pages. (merged with 95/000,578 and 95/000,579)
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				Art Unit	*2827*
				Examiner Name	*Hoang, Huan*
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		U.S. District Court Northern District of California, Case No. CV08 04144, Google Inc. v. Netlist, Inc., Defendant Netlist, lnc.'s Opening Claim Construction Brief, filed July 28, 2009 in 21 pages.
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INFORMATION DISCLOSURE CITATION Substitute for Form 1449-PTO				*Electronically filed October 29, 2018*	
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				Art Unit	*2827*
				Examiner Name	*Hoang, Huan*
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		U.S. District Court Northern District of California, Case No. CV08 04144, GOOGLE INC. vs. NETLIST, INC., [Redacted] Google lnc.'s Responsive Claim Construction Brief, filed Aug. 25, 2009 in 30 pages.
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				Filing Date	*May 22, 2017*
				First Named Inventor	*Hyun Lee*
				Art Unit	*2827*
				Examiner Name	*Hoang, Huan*
Sheet	16	of	21	Attorney Docket Number	*129980-5070-US*

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				Art Unit	*2827*
				Examiner Name	*Hoang, Huan*
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US PATENT APPLICATIONS					
Examiner Initials	Cite No.	Application Number	Filing Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Reexam Appl. No. 95/000,546 for U.S. Pat. No. 7,289,386	05/11/2010	Netlist, Inc.	Entire File History
		Reexam Appl. No. 95/000,577 for U.S. Pat. No. 7,289,386	10/20/2010	Netlist, Inc.	Entire File History
		Reexam Appl. No. 95/000,578 for U.S. Pat. No. 7,619,912	10/20/2010	Netlist, Inc.	Entire File History
		Reexam Appl. No. 95/000,579 for U.S. Pat. No. 7,619,912	10/21/2010	Netlist, Inc.	Entire File History
		Reexam App. No. 95/001,337 for U.S. Pat. No. 7,636,274	06/04/2010	Netlist, Inc.	Entire File History
		Reexam Appl. No. 95/001,381 for U.S. Pat. No. 7,532,537	06/09/2010	Netlist, Inc.	Entire File History
		Reexam Appl. No. 95/001,338; for U.S. Pat. No. 7,532,537	04/19/2010	Netlist, Inc.	Entire File History
		Reexam Appl. No. 95/001,758 for U.S. Pat. No. 7,864,627	09/15/2010	Netlist, Inc.	Entire File History
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Examiner Signature		Date Considered	

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				Art Unit	*2827*
				Examiner Name	*Hoang, Huan*
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		Reexam Appl. No. 95/002,399 for U.S. Pat. No. 8,250,295	09/15/2010	Netlist, Inc.	Entire File History
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Examiner Signature		Date Considered	

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				Art Unit	*2827*
				Examiner Name	*Hoang, Huan*
Sheet	19	of	21	Attorney Docket Number	*129980-5070-US*

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PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code[2]	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		7,024,518 B2	04-04-2006	Halbert et al.	
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		CN102576565B	09-30-2015	Netlist, Inc.		

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Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
		Netlist, Inc., Examination Decision of Request for Invalidation, CN201080039043.0, 30MAY2018, 43 pgs.
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Examiner's Signature		Date Considered	

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				Art Unit	*2827*
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Examiner's Signature	/HUAN HOANG/	Date Considered	12/17/2018

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

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Complete if Known	
Application Number	15/602,099
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First Named Inventor	Hyun Lee
Art Unit	2827
Examiner Name	Hoang, Huan
Attorney Docket Number	129980-5070-US

USP ATENT DOCUMENTS					
Examiner Initials*	Cite No. 1	Document Number Number-Kind Code 2 (ifknown)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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	3.	2011/0085408 A 1	04-14-2011	Solomon, J. et al.	
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NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.1	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T'
	5.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Related Matters, filed April 28, 2015	
	6.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Patent Owner Response to Petition, filed February 22, 2016	
	7.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner1s Objections to Evidence, filed February 29, 2016	
	8.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner1s Reply, filed May 19, 2016	
	9.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner Request for Oral Argument, filed June 2, 2016	
	10.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, PATENT OWNER MOTION FOR OBSERVATIONS, filed June 2, 2016	
	11.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, PATENT OWNER REQUEST FOR ORAL ARGUMENT, filed June 2, 2016	
	12.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, ORDER Trial Hearing, filed June 8, 2016	
	13.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Patent Owner1s SUBMISSION ON PROPRIETY OF PETITIONER REPLY, filed June 9, 2016	
	14.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner1s Response to Motion for Observations, filed June 10, 2016	
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EXAMINER **DATE CONSIDERED**

• EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicanl. 1 Applicant's unique citation designation number (optional). 2 See Kinds Codes of USPTO Patents Documents at www..Jsplo.GGv or MPEP 901.04.3 Enter Office that issued the document, by the two-letter code (WIPO Standard ST. 3). 4 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5 Kind of document by the appropriate symbols as indicated on the document and WIPO Standard ST. 16 if possible. 6 Applicant is to place a check mark here if English language Translation is attached.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet | 2 | of | 18

Complete if Known	
Application Number	15/602,099
Filing Date	May 22, 2017
First Named Inventor	Hyun Lee
Art Unit	2827
Examiner Name	Hoang, Huan
Attorney Docket Number	129980-5070-US

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[6]
	18.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner1s Updated Exhibit List, filed June 24, 2016	
	19.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Supplemental Declaration of Dr. Jagannathan, filed May 19, 2016	
	20.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, May 10, 2016 Deposition of Carl Sechen, filed May 19, 2016	
	21.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner1s Demonstrative Exhibits, filed June 24, 2016	
	22.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 2001, "Declaration of Professor Carl Sechen," filed February 22, 2016	
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	24.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 2003, "Videotaped Deposition of Srinivasan Jagannathan, Ph.Don April 20, 2015," filed February 22, 2016	
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	27.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Petitioner1s Objections to Evidence, filed February 29, 2016	
	28.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Petitioner1s Reply, filed May 19, 2016	
	29.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Petitioner Request for Oral Argument, filed June 2, 2016	
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	31.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, PATENT OWNER REQUEST FOR ORAL ARGUMENT, filed June 2, 2016	
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	34.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Petitioner1s Response to Patent Owner1s Submission, filed June 13, 2016	

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	42.	Inter Partes Review Case No. IPR2014-01029, Decision Denying Request for Rehearing, Issued on March 3, 2015.	
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	48.	English Translation of the Notice of Grounds for Rejection, Korean Patent Application No. 2012-7004038, dated May 11, 2016	
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US PATENT DOCUMENTS

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	5.	W099/30240	06-17-1999	Intel Corporation		

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	6.	Non-Final Office Action, U.S. Patent Application No. 13/970,606, filed August 20, 2013, dated November 23, 2015	
	7.	Response to Non-Final Office Action, U.S. Patent Application No. 13/970,606, filed August 20, 2013, dated March 23, 2016	
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	10.	Inter Partes Review Case No. 2014-00882, Petitioner's Request for Oral Argument, filed July 1, 2015	
	11.	Inter Partes Review Case No. 2014-00882, Patent Owner's Request for Oral Argument, filed July 3,2015	
	12.	Inter Partes Review Case No. 2014-00882, Order - Request for Oral Argument - 37 C.F.R. 42.70, filed July 10, 2015	
	13.	Inter Partes Review Case No. 2014-00882, Record of Oral Hearing, filed November 16, 2015	
	14.	Inter Partes Review Case No. 2014-00882, Final Written Decision 35 USC 318 and 37 CFR 42.73, filed December 14, 2015	
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Art Unit	2827
Examiner Name	Hoang, Huan
Attorney Docket Number	129980-5070-US

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	16.	Inter Partes Review Case No. 2014-00882, Exhibit 1022, 'Professor Carl Sechen Deposition Transcript,' filed June,19,2015	
	17.	Inter Partes Review Case No. 2014-00882, Exhibit 1023, 'Dr. Srinivasan Jagannathan Supplemental Declaration,' filed June 19,2015	
	18.	Inter Partes Review Case No. 2014-00882, Exhibit 2002, 'Declaration of Professor Carl Sechen,' filed May 8,2015	
	19.	Inter Partes Review Case No. 2014-00882, Exhibit 2003, 'Transcript of Videotaped Deposition of Srinivasan Jagannathan, Ph. D,' filed May 8,2015	
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	23.	Excerpts from the Authoritative Dictionary of IEEE Standard Terms, Seventh Edition, Standards Information Network, IEEE Press (2000), pp. 349-411	
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	25.	Selected Entries in Oxford English Dictionary, Oxford University Press 2014, http://www.oed.com/view/Entry/175039?redirectedFrom=selectively#eid	
	26.	Web search results from the Oxford English Dictionary, Oxford University Press 2014, http://www.oed.com/search?searchType=dictionary&q=select& _searchBin=Search	
	27.	Inter Partes Review Case No. 2014-00883, Patent Owner Response, filed May 8, 2015	
	28.	Inter Partes Review Case No. 2014-00883, Petitioner Diablo Technologies, Inc.'s Reply to Patent Owner Netlist, Inc.'s Response, filed June 19, 2015	
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	32.	Inter Partes Review Case No. 2014-00883, Record of Oral Hearing, filed November 16, 2015	
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First Named Inventor	Hyun Lee
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	36.	Inter Partes Review Case No. 2014-00883, Exhibit 1026, 'Dr. Srinivasan Jagannathan Supplemental Declaration,' filed June 19,2015	
	37.	Inter Partes Review Case No. 2014-01011, Patent Owner Response, filed May 8, 2015	
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Examiner Initials*	Cite No.1	Foreign Patent Document Country Code3-Number4-Kind Code 5 (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T'
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	56.	International Search Report and Written Opinion, International Application No. PCT/US14/48517, filed July 28, 2014, dated October 27, 2014	
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Application Number	15/602,099
Filing Date	May 22, 2017
First Named Inventor	Hyun Lee
Art Unit	2827
Examiner Name	Hoang, Huan
Attorney Docket Number	129980-5070-US

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	58.	Inter Partes Review Case No. IPR2014-01029, Decision Denying Request for Rehearing, Issued on March 3, 2015.	
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Attorney Docket Number	129980-5070-US

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	78.	Inter Partes Review Case No. IPR2014-01369, Exhibit 1014 to Corrected Petition for Inter Partes Review, "Standard Dictionary of Electrical and Electronics Terms," IEEE 1988, filed on September 22, 2014.	
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	98.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Exhibits F.1-F.5 to "Smart Storage Systems, Inc.'s Invalidity Contentions," dated June 6, 2014.	
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	109.	Non-final office action, U.S. Patent Application No. 13/288,850, October 11, 2013, 24 pages	
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	23.	Inter Partes Review of U.S. Patent No. 8756364, Case No. IPR2017-00549, Exhibit 1003, "Declaration of Harold S. Stone," filed December 30, 2016	
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	27.	JEDEC Standard Double Data Rate (DDR) SDRAM Specification, JESD79 (June 2000)	
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	31.	Lee, Office Action, US14/337,168, 22JAN2015, 6 pgs.	
	32.	Lee, Office Action, US14/337,168, 22OCT2015, 7 pgs.	
	33.	Lee, Notice of Allowance, US14/337,168, 10FEB2016, 8 pgs.	
	34.	Lee, Office Action, US13/288,850, 11OCT2013, 14 pgs.	
	35.	Lee, Notice of Allowance, US13/288,850, 26MAR2014, 7 pgs.	
	36.	Texas Instruments SN74LS245 octal bus transceivers with 3-state outputs datasheet, 2002	
	37.	Stone, H.S. Microcomputer Interfacing, Reading, MA: Addison Wesley, 1982	
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	39.	G. Moore, "Cramming more components onto integrated circuits," Electronics, volume 38, no. 8, April 19, 1965	

EXAMINER **DATE CONSIDERED**

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in confonnance and not considered. Include copy of this form with next communication to applicant.' Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patents Documents at 1www.osatc.gc.,1or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST. 3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document and WIPO Standard ST. 16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.H/

PTO/SB/08 E:q.u1valent

INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Application No.	15/602,099
	Filing Date	May 22, 2017
	First Named Inventor	Hyun Lee
	Art Unit	2827
(Multiple sheets *used when necessary)*	Examiner	Hoang, Huan
SHEET 15 OF 18	Attorney Docket No.	129980-5070-US

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number *Number - Kind Code (if known)* Example: 1,234,567 B1	Publication Date MM-DD-YYYY	Name of Patentee or Applicant	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
	1	6,243,283 B1	06-05-2001	Bertin et al.	
	2	6,551,857 B2	04-22-2003	Leedy	
	3	7,098,541 B2	08-29-2006	Adelmann	
	4	7,200,021 B2	04-03-2007	Raghuram	
	5	7,254,036 B2	08-07-2007	Pauley et al.	
	6	7,269,042 B2	09-11-2007	Kinsley et al.	
	7	7,286,436 B2	10-23-2007	Bhakta et al.	
	8	7,289,386 B2	10-30-2007	Bhakta et al.	
	9	7,375,970 B2	05-20-2008	Pauley et al.	
	10	7,442,050 B1	10-28-2008	Bhakta et al.	
	11	7,532,537 B2	05-12-2009	Solomon et al.	
	12	7,619,893 B1	11-17-2009	Yu	
	13	7,619,912 B2	11-17-2009	Bhakta et al.	
	14	7,630,202 B2	12-08-2009	Pauley et al.	
	15	7,633,165 B2	12-15-2009	Hsu et al.	
	16	7,636,274 B2	12-22-2009	Solomon et al.	
	17	7,683,459 B2	03-23-2010	Ma et al.	
	18	7,811,097 B1	10-12-2010	Bhakta et al.	
	19	7,827,348 B2	11-02-2010	Lee et al.	
	20	7,830,692 B2	11-09-2010	Chung et al.	
	21	7,830,645 B2	11-23-2010	Pauley et al.	
	22	7,864,627 B2	01-04-2011	Bhakta et al.	
	23	7,881,150 B2	02-01-2011	Solomon et al.	
	24	7,894,229 B2	02-22-2011	Lahtinen et al.	
	25	7,894,230 B2	02-22-2011	Kim	
	26	7,978,721 B2	07-12-2011	Jeddeloh et al.	
	27	7,990,171 B2	08-02-2011	Chung et al.	
	28	7,999,367 B2	08-16-2011	Kang et al.	

Examiner Signature	Date Considered
***Examiner:** Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

T[1] - Place a check mark in this area when an English language Translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.H/

PTO/SB/08 E:q.u1valent

INFORMATION DISCLOSURE STATEMENT BY APPLICANT		
	Application No.	15/602,099
	Filing Date	May 22, 2017
	First Named Inventor	Hyun Lee
	Art Unit	2827
(Multiple sheets *used when necessary)*	Examiner	Hoang, Huan
SHEET 16 OF 18	Attorney Docket No.	129980-5070-US

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number *Number - Kind Code (if known)* Example: 1,234,567 B1	Publication Date MM-DD-YYYY	Name of Patentee or Applicant	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
	29	8,001,434 B2	08-16-2011	Lee et al	
	30	8,019,589 B2	09-13-2011	Rajan et al.	
	31	8,033,836 B1	10-11-2011	Bhakta et al.	
	32	2006/0233012 A1	10-19-2006	Sekiguchi et al.	
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	35	2008/0094808 A1	01-24-2008	Kanapathippillai et al.	
	36	2008/0025134 A1	01-31-2008	Rajan et al.	
	37	2008/0025137 A1	01-31-2008	Natarajan et al.	
	38	2008/0253085 A1	10-16-2008	Soffer	
	39	2008/0296779 A1	12-04-2008	Matsui et al.	
	40	2009/0070727 A1	03-12-2009	Solomon	
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	43	2010/0020583 A1	01-28-2010	Kang et al.	
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	45	2010/0174858 A1	07-08-2010	Chen et al.	
	46	2011/0006360 A1	01-13-2011	Ikebuchi	
	47	2011/0016250 A1	01-20-2011	Lee et al.	
	48	2011/0016269 A1	01-20-2011	Lee et al.	
	49	2011/0050320 A1	03-03-2011	Gillingham	
	50	2011/0108888 A1	05-12-2011	Or-Bach et al.	
	51	2011/0125982 A1	05-26-2011	Choi et al.	
	52	2011/0156232 A1	06-30-2011	Youn et al.	
	53	2011/0169171 A1	07-14-2011	Marcoux	

Examiner Signature	Date Considered

***Examiner:** Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Application No.	15/602,099
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U.S. PATENT APPLICATIONS

Examiner Initials	Cite No.	Document Number *Number - Kind Code (if known)* Example: 1,234,567 B1	Filing Date MM-DD-YYYY	Name of Patentee or Applicant	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
	54	12/422,912 (Attorney Docket No.NETL.044A)	04-13-2009	Hyun Lee, et al.	
	55	12/422,853 (Attorney Docket No.NETL.045A)	04-13-2009	Hyun Lee, et al.	
	56	12/815,339 (Attorney Docket No.NETL.062A)	06-14-2010	Hyun Lee	

FOREIGN PATENT DOCUMENTS

Examiner Initials	Cite No.	Foreign Patent Document *Country Code-Number-Kind Code* Example: JP 1234567 A1	Publication Date MM-DD-YYYY	Name of Patentee or Applicant	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear	T1
	57	EP 1 816 570 A2	08-08-2007	Rambus Inc.		
	58	WO 2010-138480	12-02-2010	Rambus Inc.		
	59	WO 2011-049710	04-28-2011	Rambus Inc.		
	60	WO 2011-094437	08-04-2011	Hewlett Packard Development Co.		

NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T1
	61	AHMAD et al., "Modeling of peak-to-peak switching noise along a vertical chain of power distribution TSV pairs in a 30 stack of ICs interconnected through TSVs," Norchip Conference, Article Number 5669473, Nov. 15-16, 2010, IEEE Computer Society	
	62	BLACK et al., "Die Stacking (30) Microarchitecture," MICR0-39, 39th Annual IEEE/ACM International Symposium on, Dec. 2006, 469-479, Orlando, FL	
	63	DANESHTALAB et al., "CMIT -A novel cluster-based topology for 30 stacked architectures," 30 Systems Integration Conference (3DIC), 2010 IEEE International, Nov. 16-18, 2010, pp. 1-5	
	64	FUNAYA et al., "Cache partitioning strategies for 3-D stacked vector processors," IEEE 30 System Integration Conference, article no. 5751453, Nov. 16-18, 2010, IEEE Computer Society	
	65	GHOSH et al., "Smart Refresh: An Enhancement Memory Controller Design for Reducing Energy in Conventional and 30 Die-Stacked DRAMs," Microarchitecture, 2007, 40th Annual IEEE/ACM International Symposium, Dec. 1-5, 2007, pp. 134-145.	
	66	KANG et al., "8 Gb 3-D DDR3 DRAM using through-silicon-via technology," IEEE Journal of Solid-State Circuits, v45, n 1, 111-19, Jan. 2010, IEEE, USA	

Examiner Signature	Date Considered

***Examiner:** Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.H/

PTO/SB/08 E:q.u1valent

INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Application No.	15/602,099
	Filing Date	May 22, 2017
	First Named Inventor	Hyun Lee
	Art Unit	2827
(Multiple sheets *used when necessary)*	Examiner	Hoang, Huan
SHEET 18 OF 18	Attorney Docket No.	129980-5070-US

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T1
	67	KANG et al., "Signal integrity and reliability of a new Multi-Stack Package using a Pressure Conductive Rubber," Electrical Design of Advanced Packaging and Systems Symposium, 214-17, Dec. 2008, Seoul, South Korea	
	68	KAWANO, "A 30 Packaging Technology for High-Density Stacked DRAM," VLSI Technology, Systems and Applications, 2007, 23-25 April 2007, pp. 1-2	
	69	KIM et al., "A Quantitative Analysis of Performance Benefits of 30 Die Stacking on Mobile and Embedded Soc	
	70	KURITA et al., "A 3-D packaging technology with highly-parallel memory/logic interconnect," IEICE Transactions on Electronics, v E92-C, no. 12, pp. 1512-1522, 2009, Maruzen Col, Ltd.	
	71	KURITA et al., "Vertical Integration of Stacked DRAM and High-Speed Logic Device Using SMAFTI Technology," Advanced Packaging, IEEE Transactions, Aug. 2009, Volume 32 Issue 3, pp. 657-665	
	72	"Posts Tagged '30 Stacking'," from Chip Design Mag., http://chipdesignmag.com/lpd/blog/tag/3d-stacking/ (Printed October 13, 2011).	
	73	RUSSELL, Gill, "Intel Micron Hybrid Memory Cube: The Future of Exascale Computing," Bright Side of News. Sept. 19, 2011, <http://www.brightsideofnews.com/news/2011/9/19/intel-micron-hybrid-memory-cube-the-future-of-exascale-computing.aspx> Printed October 13, 2011 in 8 pages.	
	74	LOH, "30-Stacked Memory Architectures for Multi-core Processors," Proceedings of the 35th Annual International Symposium on Computer Architecture (ISCA '08), 453-464, IEEE Computer Society, Washington DC, USA	
	75	VAL, "The 30 interconnection applications for mass memories and microprocessors," Proceedings of the Technical Conference, 1991 International Electronic Packaging Conference, 851-60, vol. 2, 1991, Int. Electron. Packaging Soc, Wheaton, IL, USA, 2008	
	76	WEIS et al., "Design space exploration for 30-stacked DRAMs," Proceedings - Design, Automation and Test in Europe Conference and Exhibition, 2011	
	77	ZHANG et al. "A Customized Design of DRAM Controller for On-Chip 30 DRAM Stacking" Custom Integrated Circuits Conference (CICC), 2010 IEEE, Sept. 19-22 2010, pp. 1-4	
	78	International Search Report and Written Opinion, PCT/US2011/059209, January 31, 2013	

Examiner Signature	/HUAN HOANG/	Date Considered	12/17/2018

***Examiner:** Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

T[1] - Place a check mark in this area when an English language Translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.H/

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	30803	(G11C5/066 or G11C7/12 or G11C7/1084 or G11C5/06 or G11C7/1057).cpc. 365/063,63.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/12/17 11:18
L2	171	1 and register with address$3 with chip adj select$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/12/17 11:19
L3	7	2 and (dram dynamic adj ram dynamic adj random) with stack$3 with (die dice ic integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/12/17 11:20
L4	7	3 and die with chip adj select$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/12/17 11:21
L5	2175	register with address$3 with chip adj select$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/12/17 11:28
L6	11	5 and (dram dynamic adj ram dynamic adj random) with stack$3 with (die dice ic integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/12/17 11:28
L7	11	6 and control with (chip die ic integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/12/17 11:32
L8	9	6 and control near3 (chip die ic integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/12/17 11:33
L9	9	8 and capacit$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/12/17 11:39
L10	0	8 and (second another different) adj3 capacit$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/12/17 11:39

L11	2186445	netlist.as. lee.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/12/17 11:40
L12	125	11 and register with address$3 with chip adj select$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/12/17 11:41
L13	9	12 and (dram dynamic adj ram dynamic adj random) with stack$3 with (chip die dice ic integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/12/17 11:42
L14	7	13 and control near3 (chip die ic integrated adj circuit)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/12/17 11:43

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L15	4	(memory and module and system and register and control and dram and package and stack$3 and conduit and communicat$3).clm.	US-PGPUB; USPAT	OR	ON	2018/12/17 11:46
L16	4	(memory and module and system and register and control and dram and package and stack$3 and conduit and interconnect).clm.	US-PGPUB; USPAT	OR	ON	2018/12/17 11:47
L17	0	(memory and module and system and register and control and dram and package and stack$3 and conduit and capacitive).clm.	US-PGPUB; USPAT	OR	ON	2018/12/17 11:48
L18	1	(memory and module and system and register and control and dram and package and stack$3 and conduit and load).clm.	US-PGPUB; USPAT	OR	ON	2018/12/17 11:48

12/ 17/ 2018 11:49:43 AM

Electronically filed March 26, 2019

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun Lee	Confirmation No.:	1757
Serial No.:	15/602,099	Art Unit:	2827
Filed:	May 22, 2017	Examiner:	Hoang, Huan
For:	*Memory Module With Packages Of Stacked Memory Chips*	Attorney Docket No.:	129980-5070-US
		Date:	March 26, 2019

AMENDMENT UNDER 37 CFR 1.312

Mail Stop: AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
Sir:

The enclosed Amendment is in response to the Notice of Allowance dated December 26, 2018 for the above-identified patent application.

The Commissioner is hereby authorized to charge any required fee(s) to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5070-US).

Petitioners
Ex. 1008, p. 264

PART B - FEE(S) TRANSMITTAL

Electronically filed March 26, 2019

Complete and send this form with applicable fee(s), to: Mail
Mail Stop ISSUE FEE
Commissioner of Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571) 273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advanced orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS

MORGAN, LEWIS & BOCKIUS LLP
1400 Page Mill Road
Palo Alto, CA 94304

Note: A certificate of mailing below can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing.

Certificate of Mailing

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)

(Signature)

(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTY'S DOCKET NO.	CONFIRMATION NO.
15/602,099	05/22/2017	Hyun Lee	129980-5070-US	1757

TITLE OF INVENTION **MEMORY MODULE WITH PACKAGES OF STACKED MEMORY CHIPS**

APPLN. TYPE	ENTITY STATUS	ISSUE FEE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	1000	0	1000	03/26/2019

EXAMINER	ART UNIT	CLASS-SUB CLASS
HOANG, HUAN	2827	365-063000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed

1. **Morgan, Lewis & Bockius LLP**
2.
3.

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: NETLIST, INC.

(B) RESIDENCE: (CITY and STATE OR COUNTRY) Irvine, CA

Please check the appropriate assignee category or categories (will not be printed on the patent) ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
☒ Issue Fee
☐ Advanced Order - # of Copies ____

4b. Payment of Fee(s): (**Please first reapply any previously paid issue fee shown above.**)
☐ A check in the amount of the fee(s) enclosed
☐ Payment by credit card. Form PTO-2038 is attached.
☒ The Director is hereby authorized to charge the required fee(s), or credit any overpayment, to Deposit Account Number 50-0310 (order no. 129980-5070-US).

5. **Change in Small Entity Status** (from status indicated above)
☐ a. Applicant certifying micro entity status. See 37 CFR 1.29.
NOTE: Absent a valid certification of Micro Entity (see form PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

☐ Applicant asserting small entity status. See 37 CFR 1.27.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

☐ Applicant changing to regular undiscounted fee status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be sign in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Jamie J. Zheng/ Date: March 26, 2019

Printed Name: Jamie J. Zheng Registration No. 51,167

Electronic Patent Application Fee Transmittal

Application Number:	15602099
Filing Date:	22-May-2017
Title of Invention:	MEMORY MODULE WITH PACKAGES OF STACKED MEMORY CHIPS
First Named Inventor/Applicant Name:	Hyun Lee
Filer:	Jamie Jie Zheng/S. Olivier
Attorney Docket Number:	129980-5070US

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	1000	1000

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1000**

Electronic Acknowledgement Receipt

EFS ID:	35537059
Application Number:	15602099
International Application Number:	
Confirmation Number:	1757
Title of Invention:	MEMORY MODULE WITH PACKAGES OF STACKED MEMORY CHIPS
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	79141
Filer:	Jamie Jie Zheng/S. Olivier
Filer Authorized By:	Jamie Jie Zheng
Attorney Docket Number:	129980-5070US
Receipt Date:	26-MAR-2019
Filing Date:	22-MAY-2017
Time Stamp:	18:56:52
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$1000
RAM confirmation Number	032719INTEFSW00006184500310
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		129980_5070US_Issue_fee_312_AMEND.pdf	155075 7ee7bc297f42fc280fb7638e8c948e82b676e538	yes	8

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Applicant Arguments/Remarks Made in an Amendment	8	8
	Claims	3	7
	Amendment after Notice of Allowance (Rule 312)	2	2
	Issue Fee Payment (PTO-85B)	1	1

Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30186 64a86a225a9b7d8c6898ac450dae08e1ac2429fb	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	185261		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

REMARKS

Applicant appreciates the allowance of claims 1-20 in the Notice of Allowance dated December 26, 2018.

In this amendment, claims 1 and 10 are amended to address minor antecedent basis issues. Claims 12 and 19 are amended for clarity. The amendments should not affect the scope of the claims, as evidenced in paragraphs [0040], [0058], and [0067]-0068]. No new matter is added.

CONCLUDING REMARKS

The Examiner is invited to call the undersigned attorney at (650) 843-4000, if a telephone call could help resolve any remaining items.

Respectfully submitted,

Date: March 26, 2019

/Jamie J. Zheng/ 51,167

Jaime J. Zheng (Reg. No.)

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Phone: (650) 843-4000

Amendments to the Claims

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A memory module operable in a computer system to communicate with a system memory controller via a command/address bus and a data bus, comprising:

a register device configured to receive input command/address signals from the system memory controller via the command/address bus and to output control signals in response to the input command/address signals, the control signals including chip-select signals; and

a plurality of DRAM packages coupled to the register device and configured to receive the control signals via a set of module control lines, each respective DRAM package comprising:

control terminals coupled to corresponding signal lines in the set of module control lines, and data terminals coupled to a respective section of the data bus;

stacked array dies;

a control die including data signal conduits coupled to the data terminals and control signal conduits coupled to the control terminals, the control signal conduits including chip-select conduits for receiving the chip select signals and providing respective ones of the chip select signals to respective ones of the stacked array dies; and

die interconnects including first die interconnects coupled to the data signal conduits and second die interconnects coupled to the control signal conduits, each of at least a subset of the first die interconnects is coupled to at least two of the stacked array dies; and

wherein the control die is configured to control the data signal conduits in accordance with the control signals to enable the each respective DRAM package to communicate a respective set of bits of one or more data signals between a selected die among the stacked dies and the system memory controller, the selected die having received one of the chip select signals that is different from any of the other ones of the chip select signals.

2. (Previously Presented) The memory module of claim 1, wherein the control die is configured to control the data signal conduits so as to control one or more data bus time slots for the respective set of bits of the one or more data signals.

3. (Previously Presented) The memory module of claim 1, wherein the control die includes a data path timing controller configured to control timing of the respective set of bits of the one or more data signals in accordance with the control signals.

4. (Previously Presented) The memory module of claim 1, wherein the control signals include command/address signals, wherein the control die includes command/address buffers to control the timing of the command/address signals.

5. (Original) The memory module of claim 4, wherein the command/address buffers comprise latches.

6. (Previously Presented) The memory module of claim 1, wherein the data signal conduits include data buffers configured to control the timing of the respective set of bits of the one or more data signals.

7. (Previously Presented) The memory module of claim 6, wherein control die is configured to control the data signal conduits so as to control data bus time slots for the respective set of bits of the one or more data signals.

8. (Original) The memory module of claim 1, wherein the array dies include DDR DRAM, SDRAM, flash memory, or SRAM.

9. (Previously Presented) The memory module of claim 1, wherein the control die is configured to decode the control signals to obtain command/address signals for providing to the array dies.

10. (Currently Amended) The memory module of claim 1, wherein the control signals include decoded command/address signals, and wherein the control die is configured to pass the decoded command/address signals through to the stacked array dies.

11. (Previously Presented) The memory module of claim 1, wherein the data signal conduits include a first data signal conduit having a first total capacitive load and a second data signal conduit having a second total capacitive load that is different from the first total capacitive load, and wherein the first data signal conduit includes a first driver having a first driver size

corresponding to the first total capacitive load, and the second data signal conduit includes a second driver having a second driver size corresponding to the second total capacitive load, the second driver size being different from the first driver size.

12. (Currently Amended) The memory module of claim 1, wherein the data signal conduits include a first data signal conduit coupled to a first subset of the stacked array dies and a second data signal conduit coupled to a second subset of the stacked array dies, wherein the first data signal conduit has a first total capacitive load and the second data signal conduit has a second total capacitive load that is balanced with ~~substantially the same as~~ the first total capacitive load.

13. (Previously Presented) A memory module operable in a computer system to communicate with a system memory controller via a command/address bus and a data bus, comprising:

a register device configured to receive input command/address signals from the system memory controller via the command/address bus and to output control signals in response to the input command/address signals; and

a plurality of DRAM packages coupled to the register device to receive the control signals via a set of module control lines, each DRAM package comprising:

control terminals coupled to corresponding signal lines in the set of module control lines, and data terminals coupled to a section of the data bus corresponding to the each DRAM package;

stacked array dies;

a control die including data signal conduits coupled to the data terminals and control signal conduits coupled to the control terminals; and

die interconnects including first die interconnects coupled to the data signal conduits and second die interconnects coupled to the control signal conduits, each of the first die interconnects is coupled to at least one of the stacked array dies; and

wherein the control die is configured to control the data signal conduits in accordance with the control signals to enable the each respective DRAM package to communicate a respective set of bits of one or more data signals between a selected die among the stacked dies and the system memory controller;

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wherein the data signal conduits include a first data signal conduit having a first total capacitive load and a second data signal conduit having a second total capacitive load that is different from the first total capacitive load, and wherein the first data signal conduit includes a first driver having a first driver size corresponding to the first total capacitive load, and the second data signal conduit includes a second driver having a second driver size corresponding to the second total capacitive load, the second driver size being different from the first driver size.

14. (Previously Presented) The memory module of claim 13, wherein the control die includes a data path timing controller configured to control timing of the respective set of bits of the one or more data signals.

15. (Previously Presented) The memory module of claim 13, wherein the data signal conduits include data buffers configured to control the timing of the respective set of bits of the one or more data signals.

16. (Previously Presented) The memory module of claim 13, wherein the array dies include DDR DRAM, SDRAM, flash memory, or SRAM.

17. (Previously Presented) The memory module of claim 13, wherein the control die is configured to decode the control signals to obtain command/address signals for providing to the array dies.

18. (Previously Presented) The memory module of claim 13, wherein the control signals include chip-select signals and the control signal conduits include chip-select conduits for receiving the chip select signals and providing respective ones of the chip select signals to respective ones of the stacked array dies, and wherein the selected die has received one of the chip select signals that is different from any of the other ones of the chip select signals.

19. (Currently Amended) A memory module operable in a computer system to communicate with a system memory controller via a command/address bus and a data bus, comprising:

a register device configured to receive input command/address signals from the system memory controller via the command/address bus and to output control signals in response to the input command/address signals; and

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a plurality of DRAM packages coupled to the register device to receive the control signals via a set of module control lines, each DRAM package comprising:

control terminals coupled to corresponding signal lines in the set of module control lines, and data terminals coupled to a section of the data bus corresponding to the each DRAM package;

stacked array dies;

a control die including data signal conduits coupled to the data terminals and control signal conduits coupled to the control terminals; and

die interconnects including first die interconnects coupled to the data signal conduits and second die interconnects coupled to the control signal conduits, each of the first die interconnects is coupled to at least one of the stacked array dies; and

wherein the control die is configured to control the data signal conduits in accordance with the control signals to enable the each respective DRAM package to communicate a respective set of bits of one or more data signals between a selected die among the stacked dies and the system memory controller;

wherein the data signal conduits include a first data signal conduit coupled to a first subset of the stacked array dies and a second data signal conduit coupled to a second subset of the stacked array dies, wherein the first data signal conduit has a first total capacitive load and the second data signal conduit has a second total capacitive load that is ~~substantially the same as~~ balanced with the first total capacitive load;

wherein the control signals include chip-select signals and the control signal conduits include chip-select conduits for receiving the chip select signals and providing respective ones of the chip select signals to respective ones of the stacked array dies, and wherein the selected die has received one of the chip select signals that is different from any of the other ones of the chip select signals; and

wherein the control die includes a data path timing controller configured to control timing of the respective set of bits of the one or more data signals in accordance with the control signals.

20. (Previously Presented) The memory module of claim 19, wherein the control die is configured to decode the control signals to obtain command/address signals for providing to the array dies.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/602,099	05/22/2017	Hyun Lee	129980-5070US	1757

79141 7590 04/08/2019

Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304

EXAMINER	
HOANG, HUAN	

ART UNIT	PAPER NUMBER
2827	

NOTIFICATION DATE	DELIVERY MODE
04/08/2019	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

padocketingdepartment@morganlewis.com
vskliba@morganlewis.com

Response to Rule 312 Communication	Application No.	Applicant(s)	
	15/602,099	Lee, Hyun	
	Examiner	Art Unit	AIA Status
	HUAN HOANG	2827	No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

1. ☑ The amendment filed on 26 March 2019 under 37 CFR 1.312 has been considered, and has been:
   a) ☑ entered.
   b) ☐ entered as directed to matters of form not affecting the scope of the invention.
   c) ☐ disapproved because the amendment was filed after the payment of the issue fee.
      Any amendment filed after the date the issue fee is paid must be accompanied by a petition under 37 CFR 1.313(c)(1) and the required fee to withdraw the application from issue.
   d) ☐ disapproved. See explanation below.
   e) ☐ entered in part. See explanation below.

/HUAN HOANG/
Primary Examiner, Art Unit 2827

Electronically filed March 26, 2019

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Hyun Lee	Confirmation No.:	1757
Serial No.:	15/602,099	Art Unit:	2827
Filed:	May 22, 2017	Examiner:	Hoang, Huan
For:	*Memory Module With Packages Of Stacked Memory Chips*	Attorney Docket No.:	129980-5070-US
		Date:	March 26, 2019

AMENDMENT UNDER 37 CFR 1.312

Mail Stop: AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
Sir:

The enclosed Amendment is in response to the Notice of Allowance dated December 26, 2018 for the above-identified patent application.

The Commissioner is hereby authorized to charge any required fee(s) to Morgan, Lewis & Bockius LLP Deposit Account No. 50-0310 (order no. 129980-5070-US).

PTO/SB/08a/b(07-09)
Approved for use through 7/31/2012. 0MB 0651-0031
US Patent & Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Papeiwork Reduction Act of 1995, no persons are reauired to respond to a collection of information unless ii contains a valid 0MB control number.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 13 of 18

Complete if Known	
Application Number	15/602,099
Filing Date	May 22, 2017
First Named Inventor	Hyun Lee
Art Unit	2827
Examiner Name	Hoang, Huan
Attorney Docket Number	129980-5070-US

US PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code 2 (if koowo)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1.	4,739,473	1988-04-19	Ng	
	2.	5,313,624	1994-05-17	Harriman	
	3.	5,630,096	1997-05-13	Zuravleff	
	4.	5,905,401	1999-05-18	Sher	
	5.	6,061,754	2000-05-09	Cepulis	
	6.	6,141,245	2000-10-31	Bertin	
Change(s) applied	7.	6,223,650	2001-05-15	~~Johnson~~	Stuck
to document,	8.	6,262,938	2001-07-17	Lee	
/J.H./	9.	6,546,476	2003-04-08	Gillingham	
4/18/2019	10.	6,636,446	2003-10-21	Lee	
	11.	6,704,910	2004-03-09	Hong	
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	21.	2011/0193226 A1	2011-	Kirby et al.	

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T2
	22.	Inter Partes Review of U.S. Patent No. 8756364, Case No. IPR2017-00549, Petition for Inter Partes Review, filed December 30, 2016	
	23.	Inter Partes Review of U.S. Patent No. 8756364, Case No. IPR2017-00549, Exhibit 1003, "Declaration of Harold S. Stone," filed December 30, 2016	
	24.	Inter Partes Review of U.S. Patent No. 8516185, Case No. IPR2017-00577, Petition for Inter Partes Review, filed January 5, 2017	
	25.	Inter Partes Review of U.S. Patent No. 8516185, Case No. IPR2017-00577, Exhibit 1003, "Declaration of Harold S. Stone," filed January 5, 2017	

EXAMINER **DATE CONSIDERED**

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in confonnance and not considered. Include copy of this form with next communication to applicant.' Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patents Documents at 1www.osatc.gc.,.1or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST. 3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document and WIPO Standard ST. 16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.H/

INFORMATION DISCLOSURE CITATION Substitute for Form 1449-PTO				*Electronically filed October 29, 2018*	
				Application Number	*15/602,099*
				Filing Date	*May 22, 2017*
				First Named Inventor	*Hyun Lee*
				Art Unit	*2827*
				Examiner Name	*Hoang, Huan*
Sheet	9	of	21	Attorney Docket Number	*129980-5070-US*

PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code[2]	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		4,249,253	02/03/1981	Gentili et al.	
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		5,572,691	11/05/1996	Koudmani	
		5,630,096	05/13/1997	Zuravleff	
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		6,141,245	10/31/2000	Bertin	
		6,188,641	02/13/2001	Uchida	
		6,205,516	03/20/2001	Usami	
Change(s) applied		6,223,650 05/2001	~~05/15/201~~	~~Johnson~~ Stuck	
to document.		6,262,938	07/17/2001	Lee	
/JH/		6,438,062	08/20/2002	Curtis	
4/18/2019		6,446,158	09/03/2002	Karabatsos	
		6,480,439	11/12/2002	Tokutome et al.	
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		6,553,449	04/22/2003	Dodd et al.	
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		6,636,446	10/21/2003	Lee	
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		6,948,084	09/20/2005	Manapat et al	
		7,093,066	08/15/2006	Klein	

Examiner Signature		Date Considered	

DB2/ 33259060.1

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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/602,099	05/14/2019	10290328	129980-5070US	1757

79141 7590 04/24/2019

Morgan, Lewis & Bockius LLP (PA)(J. Zheng)
1400 Page Mill Road
Palo Alto, CA 94304

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Hyun Lee, Ladera Ranch, CA;
Netlist, Inc., Irvine, CA;

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