I, Julie Carlson, declare as follows:

1. I have personal knowledge of the facts set forth herein, and if called to testify, I could and would competently testify to the same.

2. I have been involved in semiconductor standardization and publication services for over twenty years. For nearly all of this time, I have worked at JEDEC, a standards-setting organization for the microelectronics industry, to edit, publish, and maintain JEDEC business records and standards developed by its numerous committees and subcommittees.

3. I have been involved with the standardization and publication activities of JEDEC continuously since 1997. I was the Manager of Standards and Publications at JEDEC from February 1997 through June 2005. Since June 2005, I have continued to work for JEDEC as a Consultant where my responsibilities include the maintenance and publication of JEDEC documents and standards. In addition, I am familiar with JEDEC's historical record-keeping and publication practices since at least 1992, based on my review of JEDEC's business records since that time and my regular discussions with JEDEC employees and members.

4. For over 50 years, JEDEC has been the global leader in developing and publishing open standards for the microelectronics industry. JEDEC's membership consists of more than 3,000 volunteers representing nearly 300

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member companies, and includes key technical individuals from most device, assembly, system and testing companies. JEDEC publications and standards are adopted worldwide. JEDEC is accredited by ANSI and maintains liaisons with numerous standards bodies throughout the world.

5. Since at least 2000, JEDEC standards have been publicly available for download from the JEDEC website (https://www.jedec.org), where they are cataloged and indexed by keyword and technological subject matter. By 2000, the JEDEC website was publicly available and commonly used by manufactures, companies in the microelectronics industry, and other interested parties to access and obtain standards information pertaining to that industry. Anyone interested can join JEDEC online, at JEDEC.org.

6. This declaration concerns JEDEC STANDARD, DDR3 SDRAM Specification, JESD79-3C (November 2008) (hereinafter, "JESD79-3C Standard"), which is a standard published by JEDEC. I have reviewed the JESD79-3C Standard. The copy of the JESD79-3C Standard attached to this declaration as Exhibits A is identical to the copy of the JESD79-3C Standard in JEDEC's files.

7. The following statements on the public availability of the JESD79-3C Standard as of November 2008 are based on personal knowledge. The development of all JEDEC documents follows the process set forth in JM21: JEDEC Manual of Organization and Procedure. According to that process, the

date on the cover of a JEDEC document is the month the document was finalized, approved by legal, and posted to the website. For the JESD79-3C Standard, the date on the cover (and thus the date it was posted to JEDEC's website) is November 2008.

8. I am familiar with the circulation and publication procedures used by JEDEC. Upon approval of the Board of Directors, the JEDEC publications department prepares documents for publication, and seeks final review and approval to publish from the JEDEC legal department. Once legal approval is received, the JEDEC publications department uploads the approved document to the JEDEC website with a brief description. An email announcement is then sent to the sponsoring committee and any approved resellers. By 2000, JEDEC made its published standards available for download from www.jedec.org, as mentioned above.

9. Based on my personal knowledge of JEDEC's policies, the JESD79-3C Standard was made publicly available in November 2008 for download from the JEDEC website (https://www.jedec.org), consistent with the date on the cover page of the JESD79-3C Standard. My knowledge of the procedures surrounding the creation of the date notation and publication is based on JEDEC's policies and practices as I understand them through my work at JEDEC. I rely on these policies and practices in the course of my work. I have no reason to believe that JEDEC's

typical practice was not followed. I have no reason to believe that the JESD79-3C Standard was not made publicly accessible in November 2008.

10. To further confirm my statements above, I have visited the Internet Archive to look at the first capture of the online catalog at www.jedec.org after November 2008, which occurred on December 7, 2008: <http://web.archive.org/web/20081207190024/http://www.jedec.org/Catalog/display.cfm>. A printout of this capture is attached as Exhibit B and is consistent with my personal recollection of the JEDEC website. As can be seen from this capture on December 7, 2008, the JESD79-3C Standard was cataloged, indexed under the "RAM Memories" technical subject matter and under the keywords "SDRAM" and "DDR3," and was available to the public by that date, consistent with my statements above. *See* Exhibit B at pages 24, 61, 70, 93.

11. Exhibit C is a printout of <http://web.archive.org/web/20081201234333/http://jedec.org/service_members/New_Members/memberco.cfm>, which is a capture on December 1, 2008, of the list of member companies on JEDEC's website as of that date, which is consistent with my personal recollection of JEDEC's membership. All of those member companies would have had access to the JESD79-3C Standard attached as Exhibit A no later than that date.

I, Julie Carlson, do hereby declare and state, that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, under Section 1001 of Title 18 of the United States Code.

Executed on 2021/09/16 Julie D. Carlson

Julie D. Carlson

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Exhibit A

JEDEC STANDARD

DDR3 SDRAM

JESD79-3C

(Revision of Jesd79-3B, April 2008)

NOVEMBER 2008

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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Table 73 —Required time tVAC above VIH(ac) {below VIL(ac)} for valid transition 182

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Ex. 1020, p. 20

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1 Scope

This document defines the DDR3 SDRAM specification, including features, functionalities, AC and DC characteristics, packages, and ball/signal assignments. The purpose of this Specification is to define the minimum set of requirements for JEDEC compliant 512 Mb through 8 Gb for x4, x8, and x16 DDR3 SDRAM devices. This specification was created based on the DDR2 specification (JESD79-2) and some aspects of the DDR specification (JESD79). Each aspect of the changes for DDR3 SDRAM operation were considered and approved by committee ballot(s). The accumulation of these ballots were then incorporated to prepare this JESD79-3 specification, replacing whole sections and incorporating the changes into Functional Description and Operation.

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2 DDR3 SDRAM Package Pinout and Addressing

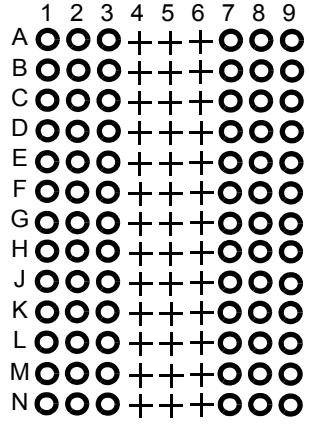
2.1 DDR3 SDRAM x4 Ballout using MO-207

(Top view: see balls through package)

	1	2	3	4	5	6	7	8	9	10	11	
A	NC	NC		NC				NC		NC	NC	
B												
C	NC	NC		NC				NC		NC	NC	
D												
E												
F	NC	VSS	VDD	NC				NC	VSS	VDD	NC	A
G		VSS	VSSQ	DQ0				DM	VSSQ	VDDQ		B
H		VDDQ	DQ2	DQS				DQ1	DQ3	VSSQ		C
J		VSSQ	NC	DQS#				VDD	VSS	VSSQ		D
K		VREFDQ	VDDQ	NC				NC	NC	VDDQ		E
L		NC	VSS	RAS#				CK	VSS	NC		F
M		ODT	VDD	CAS#				CK#	VDD	CKE		G
N		NC	CS#	WE#				A10/AP	ZQ	NC		H
P		VSS	BA0	BA2				A15	VREFCA	VSS		J
R		VDD	A3	A0				A12/BC#	BA1	VDD		K
T		VSS	A5	A2				A1	A4	VSS		L
U		VDD	A7	A9				A11	A6	VDD		M
V	NC	VSS	RESET#	A13				A14	A8	VSS	NC	N
W												
Y												
AA	NC	NC		NC				NC		NC	NC	
AB												
AC	NC	NC		NC				NC		NC	NC	
		1	2	3	4	5	6	7	8	9		

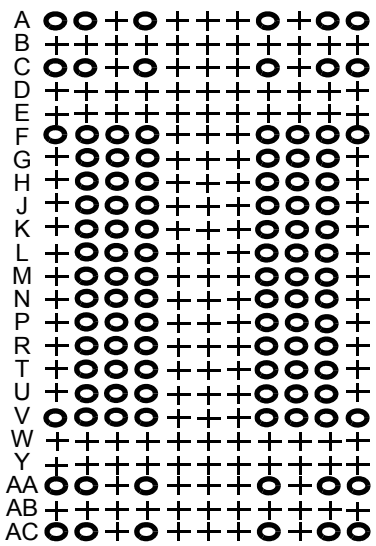
NOTE: Green NC balls indicate mechanical support balls with no internal connection. Any of the support ball locations may or may not be populated with a ball depending upon the DRAM Vendor's actual package size. Therefore, it's recommended to consider landing pad location for all possible support balls based upon maximum DRAM package size allowed in the application.

MO-207 Variation DT-z (x4)



O Populated ball
+ Ball not populated

MO-207 Variation DW-z (x4) with support balls



2 DDR3 SDRAM Package Pinout and Addressing (Cont'd)

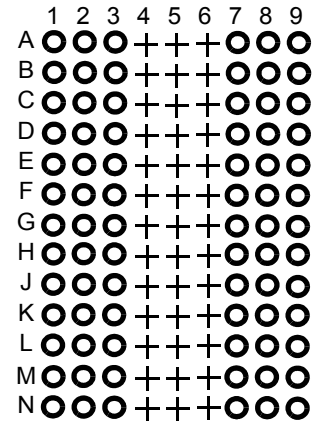
2.2 DDR3 SDRAM x8 Ballout using MO-207

(Top view: see balls through package)

	1	2	3	4	5	6	7	8	9	10	11	
A	NC	NC		NC				NC		NC	NC	
B												
C	NC	NC		NC				NC		NC	NC	
D												
E												
F	NC	VSS	VDD	NC				NU/TDQS#	VSS	VDD	NC	A
G		VSS	VSSQ	DQ0				DM/TDQS	VSSQ	VDDQ		B
H		VDDQ	DQ2	DQS				DQ1	DQ3	VSSQ		C
J		VSSQ	DQ6	DQS#				VDD	VSS	VSSQ		D
K		VREFDQ	VDDQ	DQ4				DQ7	DQ5	VDDQ		E
L		NC	VSS	RAS#				CK	VSS	NC		F
M		ODT	VDD	CAS#				CK#	VDD	CKE		G
N		NC	CS#	WE#				A10/AP	ZQ	NC		H
P		VSS	BA0	BA2				A15	VREFCA	VSS		J
R		VDD	A3	A0				A12/BC#	BA1	VDD		K
T		VSS	A5	A2				A1	A4	VSS		L
U		VDD	A7	A9				A11	A6	VDD		M
V	NC	VSS	RESET#	A13				A14	A8	VSS	NC	N
W												
Y												
AA	NC	NC		NC				NC		NC	NC	
AB												
AC	NC	NC		NC				NC		NC	NC	
		1	2	3	4	5	6	7	8	9		

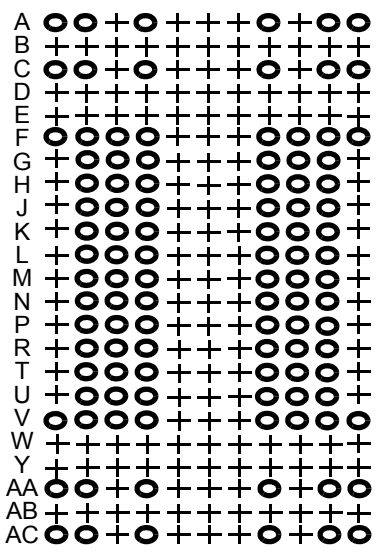
NOTE: Green NC balls indicate mechanical support balls with no internal connection. Any of the support ball locations may or may not be populated with a ball depending upon the DRAM Vendor's actual package size. Therefore, it's recommended to consider landing pad location for all possible support balls based upon maximum DRAM package size allowed in the application.

MO-207 Variation DT-z (x8)



O Populated ball
+ Ball not populated

MO-207 Variation DW-z (x8)
with support balls



2 DDR3 SDRAM Package Pinout and Addressing (Cont'd)

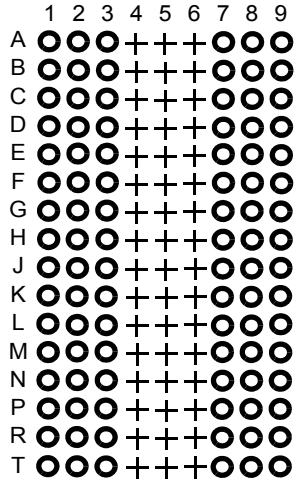
2.3 DDR3 SDRAM x16 Ballout using MO-207

(Top view: see balls through package)

	1	2	3	4	5	6	7	8	9	10	11	
A	NC	NC		NC				NC		NC	NC	A
B												B
C												C
D	NC	VDDQ	DQU5	DQU7				DQU4	VDDQ	VSS	NC	D
E		VSSQ	VDD	VSS				DQSU#	DQU6	VSSQ		E
F		VDDQ	DQU3	DQU1				DQSU	DQU2	VDDQ		F
G		VSSQ	VDDQ	DMU				DQU0	VSSQ	VDD		G
H		VSS	VSSQ	DQL0				DML	VSSQ	VDDQ		H
J		VDDQ	DQL2	DQSL				DQL1	DQL3	VSSQ		J
K		VSSQ	DQL6	DQSL#				VDD	VSS	VSSQ		K
L		VREFDQ	VDDQ	DQL4				DQL7	DQL5	VDDQ		L
M		NC	VSS	RAS#				CK	VSS	NC		M
N		ODT	VDD	CAS#				CK#	VDD	CKE		N
P		NC	CS#	WE#				A10/AP	ZQ	NC		P
R		VSS	BA0	BA2				A15	VREFCA	VSS		R
T		VDD	A3	A0				A12/BC#	BA1	VDD		T
U		VSS	A5	A2				A1	A4	VSS		U
V		VDD	A7	A9				A11	A6	VDD		V
W	NC	VSS	RESET#	A13				A14	A8	VSS	NC	W
Y												Y
AA												AA
AB	NC	NC		NC				NC		NC	NC	AB
		1	2	3	4	5	6	7	8	9		

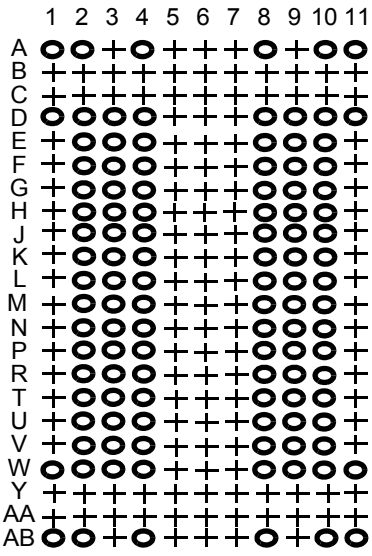
NOTE: Green NC balls indicate mechanical support balls with no internal connection. Any of the support ball locations may or may not be populated with a ball depending upon the DRAM Vendor's actual package size. Therefore, it's recommended to consider landing pad location for all possible support balls based upon maximum DRAM package size allowed in the application.

MO - 207 Variation DU-z (x16)



O Populated ball
+ Ball not populated

MO-207 Variation DY-z (x16)
with support balls



2 DDR3 SDRAM Package Pinout and Addressing (Cont'd)

2.4 Stacked / dual-die DDR3 SDRAM x4 Ballout using MO-207

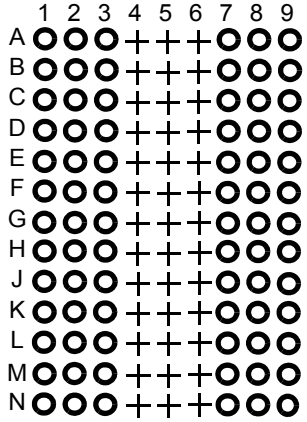
(Top view: see balls through package)

	1	2	3	4	5	6	7	8	9	10	11	
A	NC	NC		NC				NC		NC	NC	
B												
C	NC	NC		NC				NC		NC	NC	
D												
E												
F	NC	VSS	VDD	NC				NC	VSS	VDD	NC	A
G		VSS	VSSQ	DQ0				DM	VSSQ	VDDQ		B
H		VDDQ	DQ2	DQS				DQ1	DQ3	VSSQ		C
J		VSSQ	NC	DQS#				VDD	VSS	VSSQ		D
K		VREFDQ	VDDQ	NC				NC	NC	VDDQ		E
L		ODT1	VSS	RAS#				CK	VSS	CKE1		F
M		ODT0	VDD	CAS#				CK#	VDD	CKE0		G
N		CS1#	CS0#	WE#				A10/AP	ZQ0	ZQ1		H
P		VSS	BA0	BA2				A15	VREFCA	VSS		J
R		VDD	A3	A0				A12/BC#	BA1	VDD		K
T		VSS	A5	A2				A1	A4	VSS		L
U		VDD	A7	A9				A11	A6	VDD		M
V	NC	VSS	RESET#	A13				A14	A8	VSS	NC	N
W												
Y												
AA	NC	NC		NC				NC		NC	NC	
AB												
AC	NC	NC		NC				NC		NC	NC	
		1	2	3	4	5	6	7	8	9		

NOTE 1: Green NC balls indicate mechanical support balls with no internal connection. Any of the support ball locations may or may not be populated with a ball depending upon the DRAM Vendor's actual package size. Therefore, it's recommended to consider landing pad location for all possible support balls based upon maximum DRAM package size allowed in the application.

NOTE 2: This stacked ballout is intended for use only with stacked/dual-die packages, and does not apply to non-stacked/single-die packages. This document (JESD79-3) focuses on non-stacked, single-die devices unless otherwise explicitly stated.

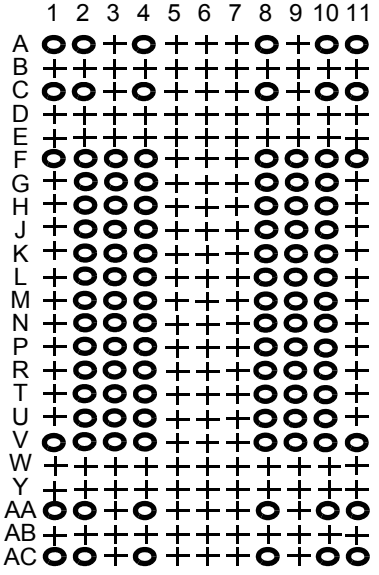
MO-207 Variation DT-z (x4)



O Populated ball

+ Ball not populated

MO-207 Variation DW-z (x4) with support balls



2 DDR3 SDRAM Package Pinout and Addressing (Cont'd)

2.5 Stacked / dual-die DDR3 SDRAM x8 Ballout using MO-207

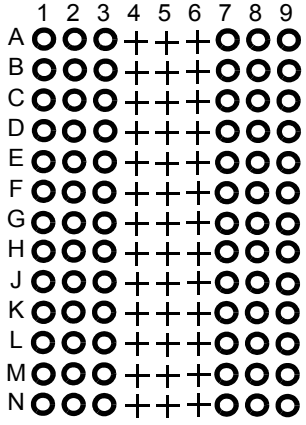
(Top view: see balls through package)

	1	2	3	4	5	6	7	8	9	10	11	
A	NC	NC		NC				NC		NC	NC	
B												
C	NC	NC		NC				NC		NC	NC	
D												
E												
F	NC	VSS	VDD	NC				NU/TDQS#	VSS	VDD	NC	A
G		VSS	VSSQ	DQ0				DM/TDQS	VSSQ	VDDQ		B
H		VDDQ	DQ2	DQS				DQ1	DQ3	VSSQ		C
J		VSSQ	DQ6	DQS#				VDD	VSS	VSSQ		D
K		VREFDQ	VDDQ	DQ4				DQ7	DQ5	VDDQ		E
L		ODT1	VSS	RAS#				CK	VSS	CKE1		F
M		ODT0	VDD	CAS#				CK#	VDD	CKE0		G
N		CS1#	CS0#	WE#				A10/AP	ZQ0	ZQ1		H
P		VSS	BA0	BA2				A15	VREFCA	VSS		J
R		VDD	A3	A0				A12/BC#	BA1	VDD		K
T		VSS	A5	A2				A1	A4	VSS		L
U		VDD	A7	A9				A11	A6	VDD		M
V	NC	VSS	RESET#	A13				A14	A8	VSS	NC	N
W												
Y												
AA	NC	NC		NC				NC		NC	NC	
AB												
AC	NC	NC		NC				NC		NC	NC	
		1	2	3	4	5	6	7	8	9		

NOTE 1: Green NC balls indicate mechanical support balls with no internal connection. Any of the support ball locations may or may not be populated with a ball depending upon the DRAM Vendor's actual package size. Therefore, it's recommended to consider landing pad location for all possible support balls based upon maximum DRAM package size allowed in the application.

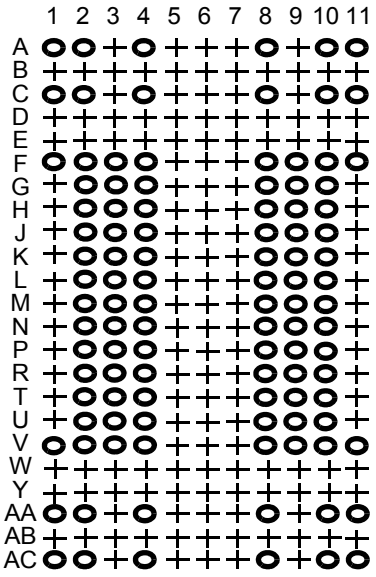
NOTE 2: This stacked ballout is intended for use only with stacked/dual-die packages, and does not apply to non-stacked/single-die packages. This document (JESD79-3) focuses on non-stacked, single-die devices unless otherwise explicitly stated.

MO-207 Variation DT-z (x8)



O Populated ball
+ Ball not populated

MO - 207 Variation DW-z (x8) with support balls



2 DDR3 SDRAM Package Pinout and Addressing (Cont'd)

2.6 Stacked / dual-die DDR3 SDRAM x16 Ballout using MO-207

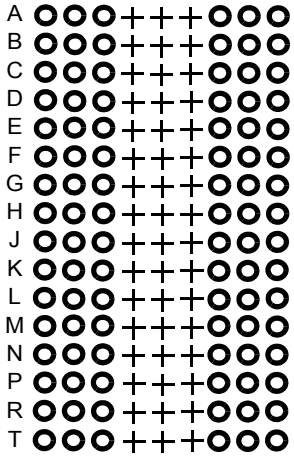
(Top view: see balls through package)

	1	2	3	4	5	6	7	8	9	10	11	
A	NC	NC		NC				NC		NC	NC	A
B												B
C												C
D	NC	VDDQ	DQU5	DQU7				DQU4	VDDQ	VSS	NC	D
E		VSSQ	VDD	VSS				DQSU#	DQU6	VSSQ		E
F		VDDQ	DQU3	DQU1				DQSU	DQU2	VDDQ		F
G		VSSQ	VDDQ	DMU				DQU0	VSSQ	VDD		G
H		VSS	VSSQ	DQL0				DML	VSSQ	VDDQ		H
J		VDDQ	DQL2	DQSL				DQL1	DQL3	VSSQ		J
K		VSSQ	DQL6	DQSL#				VDD	VSS	VSSQ		K
L		VREFDQ	VDDQ	DQL4				DQL7	DQL5	VDDQ		L
M		ODT1	VSS	RAS#				CK	VSS	CKE1		M
N		ODT0	VDD	CAS#				CK#	VDD	CKE0		N
P		CS1#	CS0#	WE#				A10/AP	ZQ0	ZQ1		P
R		VSS	BA0	BA2				A15	VREFCA	VSS		R
T		VDD	A3	A0				A12/BC#	BA1	VDD		T
U		VSS	A5	A2				A1	A4	VSS		U
V		VDD	A7	A9				A11	A6	VDD		V
W	NC	VSS	RESET#	A13				A14	A8	VSS	NC	W
Y												Y
AA												AA
AB	NC	NC		NC				NC		NC	NC	AB
		1	2	3	4	5	6	7	8	9		

NOTE 1: Green NC balls indicate mechanical support balls with no internal connection. Any of the support ball locations may or may not be populated with a ball depending upon the DRAM Vendor's actual package size. Therefore, it's recommended to consider landing pad location for all possible support balls based upon maximum DRAM package size allowed in the application.

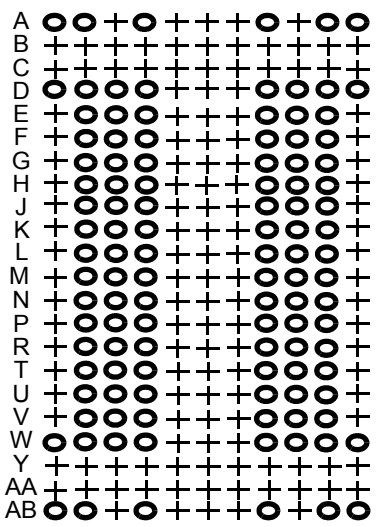
NOTE 2: This stacked ballout is intended for use only with stacked/dual-die packages, and does not apply to non-stacked/single-die packages. This document (JESD79-3) focuses on non-stacked, single-die devices unless otherwise explicitly stated.

MO - 207 Variation DU-z (x16)



O Populated ball
+ Ball not populated

MO - 207 Variation DY-z (x16) with support balls



2 DDR3 SDRAM Package Pinout and Addressing (Cont'd)

2.7 Quad-stacked / Quad-die DDR3 SDRAM x4 Ballout using MO-207

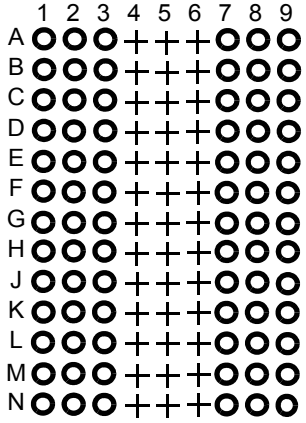
(Top view: see balls through package)

	1	2	3	4	5	6	7	8	9	10	11	
A	NC	NC		NC				NC		NC	NC	
B												
C	NC	NC		NC				NC		NC	NC	
D												
E												
F	NC	VSS	VDD	NC				NC	VSS	VDD	NC	A
G		VSS	VSSQ	DQ0				DM	VSSQ	VDDQ		B
H		VDDQ	DQ2	DQS				DQ1	DQ3	VSSQ		C
J		VSSQ	NC	DQS#				VDD	VSS	VSSQ		D
K		VREFDQ	VDDQ	NC				NC	NC	VDDQ		E
L		ODT1	VSS	RAS#				CK	VSS	CKE1		F
M		ODT0	VDD	CAS#				CK#	VDD	CKE0		G
N		CS1#	CS0#	WE#				A10/AP	ZQ0	ZQ1		H
P		VSS	BA0	BA2				A15	VREFCA	VSS		J
R		CS2#	A3	A0				A12/BC#	BA1	ZQ2		K
T		CS3#	A5	A2				A1	A4	ZQ3		L
U		VDD	A7	A9				A11	A6	VDD		M
V	NC	VSS	RESET#	A13				A14	A8	VSS	NC	N
W												
Y												
AA	NC	NC		NC				NC		NC	NC	
AB												
AC	NC	NC		NC				NC		NC	NC	
		1	2	3	4	5	6	7	8	9		

NOTE 1: Green NC balls indicate mechanical support balls with no internal connection. Any of the support ball locations may or may not be populated with a ball depending upon the DRAM Vendor's actual package size. Therefore, it's recommended to consider landing pad location for all possible support balls based upon maximum DRAM package size allowed in the application.

NOTE 2: This stacked ballout is intended for use only with quad-stacked/quad-die packages, and does not apply to non-stacked/single-die packages. This document (JESD79-3) focuses on non-stacked, single-die devices unless otherwise explicitly stated.

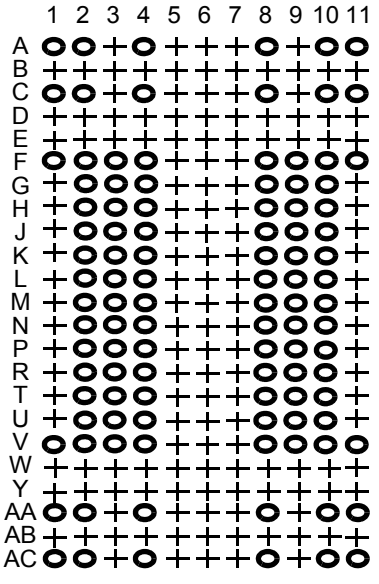
MO-207 Variation DT-z (x4)



O Populated ball

+ Ball not populated

MO-207 Variation DW-z (x4)
with support balls



2 DDR3 SDRAM Package Pinout and Addressing (Cont'd)

2.8 Quad-stacked / Quad-die DDR3 SDRAM x8 Ballout using MO-207

(Top view: see balls through package)

	1	2	3	4	5	6	7	8	9	10	11	
A	NC	NC		NC				NC		NC	NC	
B												
C	NC	NC		NC				NC		NC	NC	
D												
E												
F	NC	VSS	VDD	NC				NU/TDQS#	VSS	VDD	NC	A
G		VSS	VSSQ	DQ0				DM/TDQS	VSSQ	VDDQ		B
H		VDDQ	DQ2	DQS				DQ1	DQ3	VSSQ		C
J		VSSQ	DQ6	DQS#				VDD	VSS	VSSQ		D
K		VREFDQ	VDDQ	DQ4				DQ7	DQ5	VDDQ		E
L		ODT1	VSS	RAS#				CK	VSS	CKE1		F
M		ODT0	VDD	CAS#				CK#	VDD	CKE0		G
N		CS1#	CS0#	WE#				A10/AP	ZQ0	ZQ1		H
P		VSS	BA0	BA2				A15	VREFCA	VSS		J
R		CS2#	A3	A0				A12/BC#	BA1	ZQ2		K
T		CS3#	A5	A2				A1	A4	ZQ3		L
U		VDD	A7	A9				A11	A6	VDD		M
V	NC	VSS	RESET#	A13				A14	A8	VSS	NC	N
W												
Y												
AA	NC	NC		NC				NC		NC	NC	
AB												
AC	NC	NC		NC				NC		NC	NC	
		1	2	3	4	5	6	7	8	9		

NOTE 1: Green NC balls indicate mechanical support balls with no internal connection. Any of the support ball locations may or may not be populated with a ball depending upon the DRAM Vendor's actual package size. Therefore, it's recommended to consider landing pad location for all possible support balls based upon maximum DRAM package size allowed in the application.

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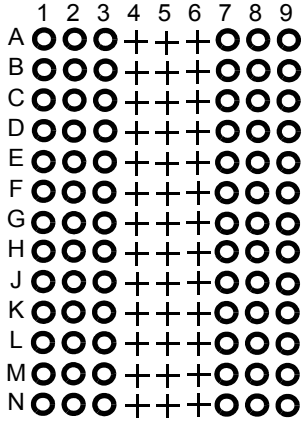
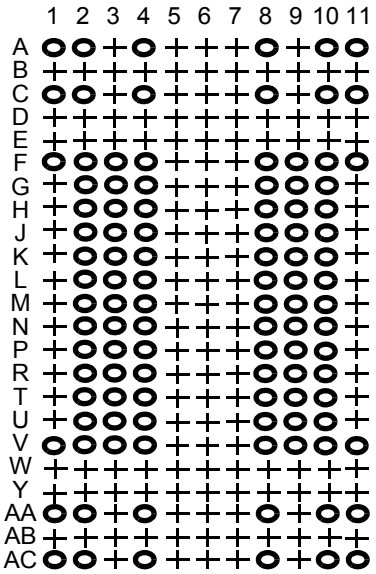
MO-207 Variation DT-z (x8)



O Populated ball
+ Ball not populated

MO - 207 Variation DW-z (x8) with support balls



2 DDR3 SDRAM Package Pinout and Addressing (Cont'd)

2.9 Quad-stacked / Quad-die DDR3 SDRAM x16 Ballout using MO-207

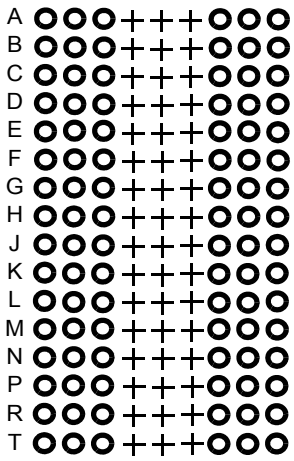
(Top view: see balls through package)

	1	2	3	4	5	6	7	8	9	10	11	
A	NC	NC		NC				NC		NC	NC	
B												
C												
D	NC	VDDQ	DQU5	DQU7				DQU4	VDDQ	VSS	NC	A
E		VSSQ	VDD	VSS				DQSU#	DQU6	VSSQ		B
F		VDDQ	DQU3	DQU1				DQSU	DQU2	VDDQ		C
G		VSSQ	VDDQ	DMU				DQU0	VSSQ	VDD		D
H		VSS	VSSQ	DQL0				DML	VSSQ	VDDQ		E
J		VDDQ	DQL2	DQSL				DQL1	DQL3	VSSQ		F
K		VSSQ	DQL6	DQSL#				VDD	VSS	VSSQ		G
L		VREFDQ	VDDQ	DQL4				DQL7	DQL5	VDDQ		H
M		ODT1	VSS	RAS#				CK	VSS	CKE1		J
N		ODT0	VDD	CAS#				CK#	VDD	CKE0		K
P		CS1#	CS0#	WE#				A10/AP	ZQ0	ZQ1		L
R		VSS	BA0	BA2				A15	VREFCA	VSS		M
T		CS2#	A3	A0				A12/BC#	BA1	ZQ2		N
U		CS3#	A5	A2				A1	A4	ZQ3		P
V		VDD	A7	A9				A11	A6	VDD		R
W	NC	VSS	RESET#	A13				A14	A8	VSS	NC	T
Y												
AA												
AB	NC	NC		NC				NC		NC	NC	
		1	2	3	4	5	6	7	8	9		

NOTE 1: Green NC balls indicate mechanical support balls with no internal connection. Any of the support ball locations may or may not be populated with a ball depending upon the DRAM Vendor's actual package size. Therefore, it's recommended to consider landing pad location for all possible support balls based upon maximum DRAM package size allowed in the application.

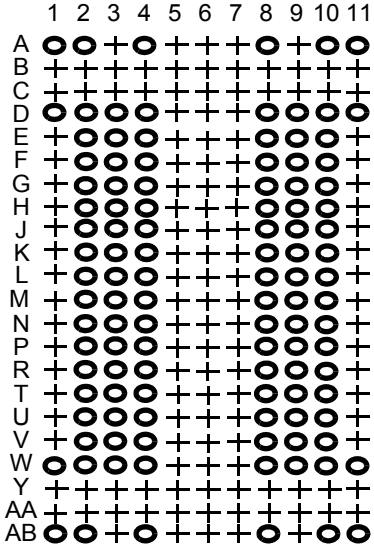
NOTE 2: This stacked ballout is intended for use only with quad-stacked/quad-die packages, and does not apply to non-stacked/single-die packages. This document (JESD79-3) focuses on non-stacked, single-die devices unless otherwise explicitly stated.

MO - 207 Variation DU-z (x16)



O Populated ball
+ Ball not populated

MO - 207 Variation DY-z
(x16) with support balls



2 DDR3 SDRAM Package Pinout and Addressing (Cont'd)
2.9 Quad-stacked / Quad-die DDR3 SDRAM x16 Ballout using MO-207 (Cont'd)

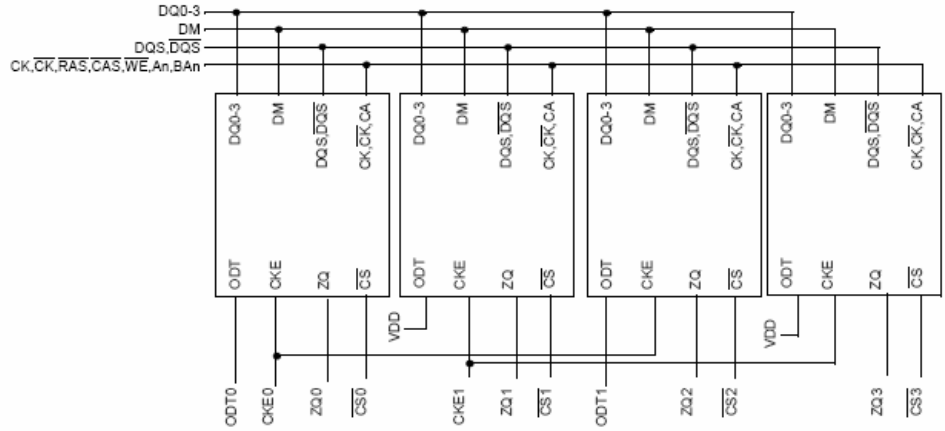


Figure 1 — Qual-stacked / Quad-die DDR3 SDRAM x4 rank association

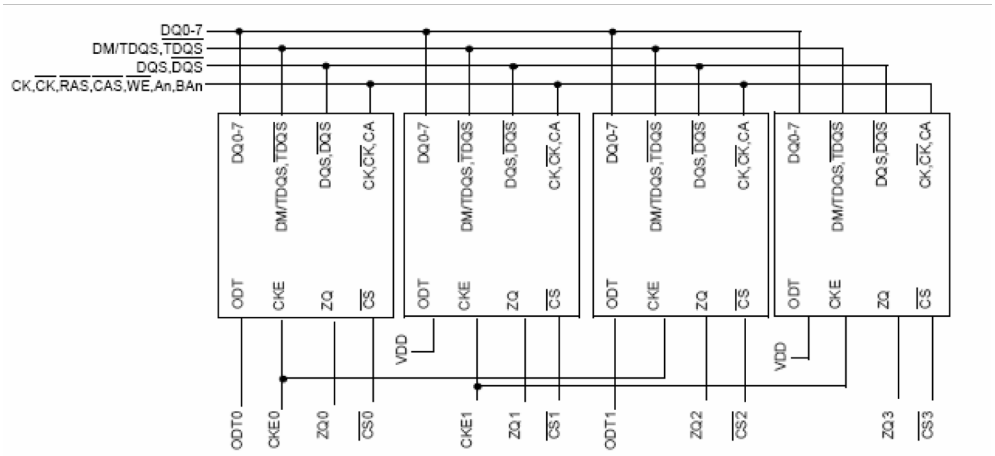


Figure 2 — Qual-stacked / Quad-die DDR3 SDRAM x8 rank association

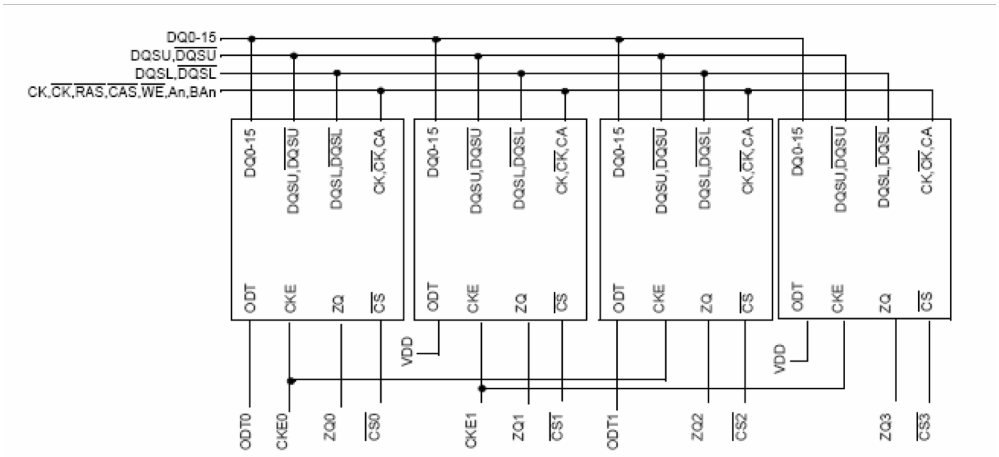


Figure 3 — Qual-stacked / Quad-die DDR3 SDRAM x16 rank association

2 DDR3 SDRAM Package Pinout and Addressing (Cont'd)

2.10 Pinout Description

Table 1 — Input/output functional description

Symbol	Type	Function
CK, CK#	Input	Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#.
CKE, (CKE0), (CKE1)	Input	Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is asynchronous for Self-Refresh exit. After VREFCA and VREFDQ have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, CK#, ODT and CKE, are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS#, (CS0#), (CS1#), (CS2#), (CS3#)	Input	Chip Select: All commands are masked when CS# is registered HIGH. CS# provides for external Rank selection on systems with multiple Ranks. CS# is considered part of the command code.
ODT, (ODT0), (ODT1)	Input	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is only applied to each DQ, DQS, DQS# and DM/TDQS, NU/TDQS# (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x4/x8 configurations. For x16 configuration, ODT is applied to each DQ, DQSU, DQSU#, DQSL, DQSL#, DMU, and DML signal. The ODT pin will be ignored if MR1 and MR2 are programmed to disable RTT.
RAS#. CAS#. WE#	Input	Command Inputs: RAS#, CAS# and WE# (along with CS#) define the command being entered.
DM, (DMU), (DML)	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. For x8 device, the function of DM or TDQS/TDQS# is enabled by Mode Register A11 setting in MR1.
BA0 - BA2	Input	Bank Address Inputs: BA0 - BA2 define to which bank an Active, Read, Write, or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A15	Input	Address Inputs: Provide the row address for Active commands and the column address for Read/ Write commands to select one location out of the memory array in the respective bank. (A10/AP and A12/BC# have additional functions; see below). The address inputs also provide the op-code during Mode Register Set commands.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC#	Input	Burst Chop: A12 / BC# is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
RESET#	Input	Active Low Asynchronous Reset: Reset is active when RESET# is LOW, and inactive when RESET# is HIGH. RESET# must be HIGH during normal operation. RESET# is a CMOS rail-to-rail signal with DC high and low at 80% and 20% of V_{DD}, i.e., 1.20V for DC high and 0.30V for DC low.
DQ	Input / Output	Data Input/ Output: Bi-directional data bus.
DQU, DQL, DQS, DQS#, DQSU, DQSU#, DQSL, DQSL#	Input / Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobes DQS, DQSL, and DQSU are paired with differential signals DQS#, DQSL#, and DQSU#, respectively, to provide differential pair signaling to the system during reads and writes. DDR3 SDRAM supports differential data strobe only and does not support single-ended.

2 DDR3 SDRAM Package Pinout and Addressing (Cont'd)
2.10 Pinout Description (Cont'd)

Table 1 — Input/output functional description (Cont'd)

Symbol	Type	Function
TDQS, TDQS#	Output	Termination Data Strobe: TDQS/TDQS# is applicable for x8 DRAMs only. When enabled via Mode Register A11 = 1 in MR1, the DRAM will enable the same termination resistance function on TDQS/TDQS# that is applied to DQS/DQS#. When disabled via mode register A11 = 0 in MR1, DM/TDQS will provide the data mask function and TDQS# is not used. x4/x16 DRAMs must disable the TDQS function via mode register A11 = 0 in MR1.
NC		No Connect: No internal electrical connection is present.
V_{DDQ}	Supply	DQ Power Supply: 1.5 V +/- 0.075 V
V_{SSQ}	Supply	DQ Ground
V_{DD}	Supply	Power Supply: 1.5 V +/- 0.075 V
V_{SS}	Supply	Ground
V_{REFDQ}	Supply	Reference voltage for DQ
V_{REFCA}	Supply	Reference voltage for CA
ZQ, (ZQ0), (ZQ1), (ZQ2), (ZQ3)	Supply	Reference Pin for ZQ calibration
NOTE: Input only pins (BA0-BA2, A0-A15, RAS#, CAS#, WE#, CS#, CKE, ODT, and RESET#) do not supply termination.		

2 DDR3 SDRAM Package Pinout and Addressing (Cont'd)

2.11 DDR3 SDRAM Addressing

2.11.1 512Mb

Configuration	128Mb x 4	64Mb x 8	32Mb x 16
# of Banks	8	8	8
Bank Address	BA0 - BA2	BA0 - BA2	BA0 - BA2
Auto precharge	A10/AP	A10/AP	A10/AP
BC switch on the fly	A12/BC#	A12/BC#	A12/BC#
Row Address	A0 - A12	A0 - A12	A0 - A11
Column Address	A0 - A9,A11	A0 - A9	A0 - A9
Page size [1]	1 KB	1 KB	2 KB

2.11.2 1Gb

Configuration	256Mb x 4	128Mb x 8	64Mb x 16
# of Banks	8	8	8
Bank Address	BA0 - BA2	BA0 - BA2	BA0 - BA2
Auto precharge	A10/AP	A10/AP	A10/AP
BC switch on the fly	A12/BC#	A12/BC#	A12/BC#
Row Address	A0 - A13	A0 - A13	A0 - A12
Column Address	A0 - A9,A11	A0 - A9	A0 - A9
Page size [1]	1 KB	1 KB	2 KB

2.11.3 2Gb

Configuration	512Mb x 4	256Mb x 8	128Mb x 16
# of Banks	8	8	8
Bank Address	BA0 - BA2	BA0 - BA2	BA0 - BA2
Auto precharge	A10/AP	A10/AP	A10/AP
BC switch on the fly	A12/BC#	A12/BC#	A12/BC#
Row Address	A0 - A14	A0 - A14	A0 - A13
Column Address	A0 - A9,A11	A0 - A9	A0 - A9
Page size [1]	1 KB	1 KB	2 KB

2.11.4 4Gb

Configuration	1Gb x 4	512Mb x 8	256Mb x 16
# of Banks	8	8	8
Bank Address	BA0 - BA2	BA0 - BA2	BA0 - BA2
Auto precharge	A10/AP	A10/AP	A10/AP
BC switch on the fly	A12/BC#	A12/BC#	A12/BC#
Row Address	A0 - A15	A0 - A15	A0 - A14
Column Address	A0 - A9,A11	A0 - A9	A0 - A9
Page size [1]	1 KB	1 KB	2 KB

2 DDR3 SDRAM Package Pinout and Addressing (Cont'd)
2.11 DDR3 SDRAM Addressing (Cont'd)

2.11.5 8Gb

Configuration	2Gb x 4	1Gb x 8	512Mb x 16
# of Banks	8	8	8
Bank Address	BA0 - BA2	BA0 - BA2	BA0 - BA2
Auto precharge	A10/AP	A10/AP	A10/AP
BC switch on the fly	A12/BC#	A12/BC#	A12/BC#
Row Address	A0 - A15	A0 - A15	A0 - A15
Column Address	A0 - A9, A11, A13	A0 - A9, A11	A0 - A9
Page size [1]	2 KB	2 KB	2 KB

NOTE 1. Page size is the number of bytes of data delivered from the array to the internal sense amplifiers when an ACTIVE command is registered. Page size is per bank, calculated as follows:

page size = $2^{COLBITS} * ORG \div 8$
where
COLBITS = the number of column address bits
ORG = the number of I/O (DQ) bits

3 Functional Description

3.1 Simplified State Diagram

This simplified State Diagram is intended to provide an overview of the possible state transitions and the commands to control them. In particular, situations involving more than one bank, the enabling or disabling of on-die termination, and some other events are not captured in full detail.

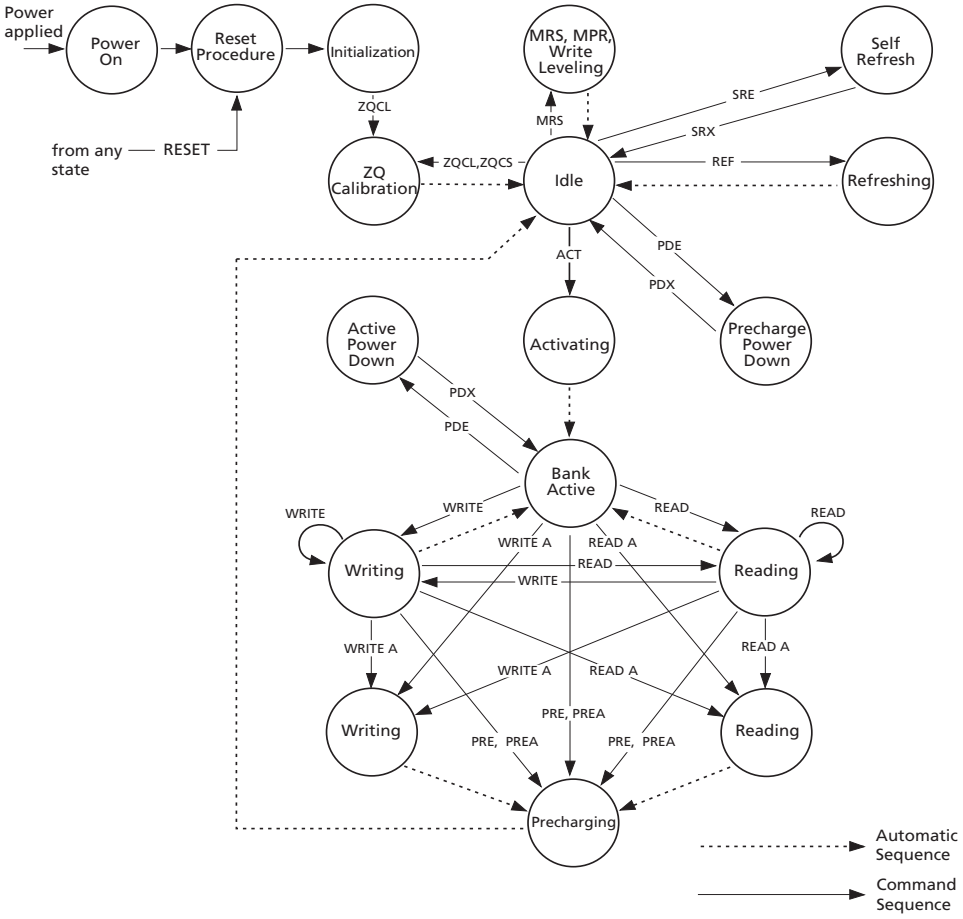


Figure 4 — Simplified State Diagram

Table 2 — State Diagram Command Definitions

Abbreviation	Function	Abbreviation	Function	Abbreviation	Function
ACT	Active	Read	RD, RDS4, RDS8	PDE	Enter Power-down
PRE	Precharge	Read A	RDA, RDAS4, RDAS8	PDX	Exit Power-down
PREA	Precharge All	Write	WR, WRS4, WRS8	SRE	Self-Refresh entry
MRS	Mode Register Set	Write A	WRA, WRAS4, WRAS8	SRX	Self-Refresh exit
REF	Refresh	RESET	Start RESET Procedure	MPR	Multi-Purpose Register
ZQCL	ZQ Calibration Long	ZQCS	ZQ Calibration Short	-	-
NOTE: See "Command Truth Table" on page 33 for more details.					

3.2 Basic Functionality

The DDR3 SDRAM is a high-speed dynamic random-access memory internally configured as an eight-bank DRAM. The DDR3 SDRAM uses a 8n prefetch architecture to achieve high-speed operation. The 8n prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the DDR3 SDRAM consists of a single 8n-bit wide, four clock data transfer at the internal DRAM core and two corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

Read and write operation to the DDR3 SDRAM are burst oriented, start at a selected location, and continue for a burst length of eight or a 'chopped' burst of four in a programmed sequence. Operation begins with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the Active command are used to select the bank and row to be activated (BA0-BA2 select the bank; A0-A15 select the row; refer to "DDR3 SDRAM Addressing" on page 15 for specific requirements). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (via A10), and select BC4 or BL8 mode 'on the fly' (via A12) if enabled in the mode register.

Prior to normal operation, the DDR3 SDRAM must be powered up and initialized in a predefined manner. The following sections provide detailed information covering device reset and initialization, register definition, command descriptions, and device operation.

3 Functional Description (Cont'd)

3.3 RESET and Initialization Procedure

3.3.1 Power-up Initialization Sequence

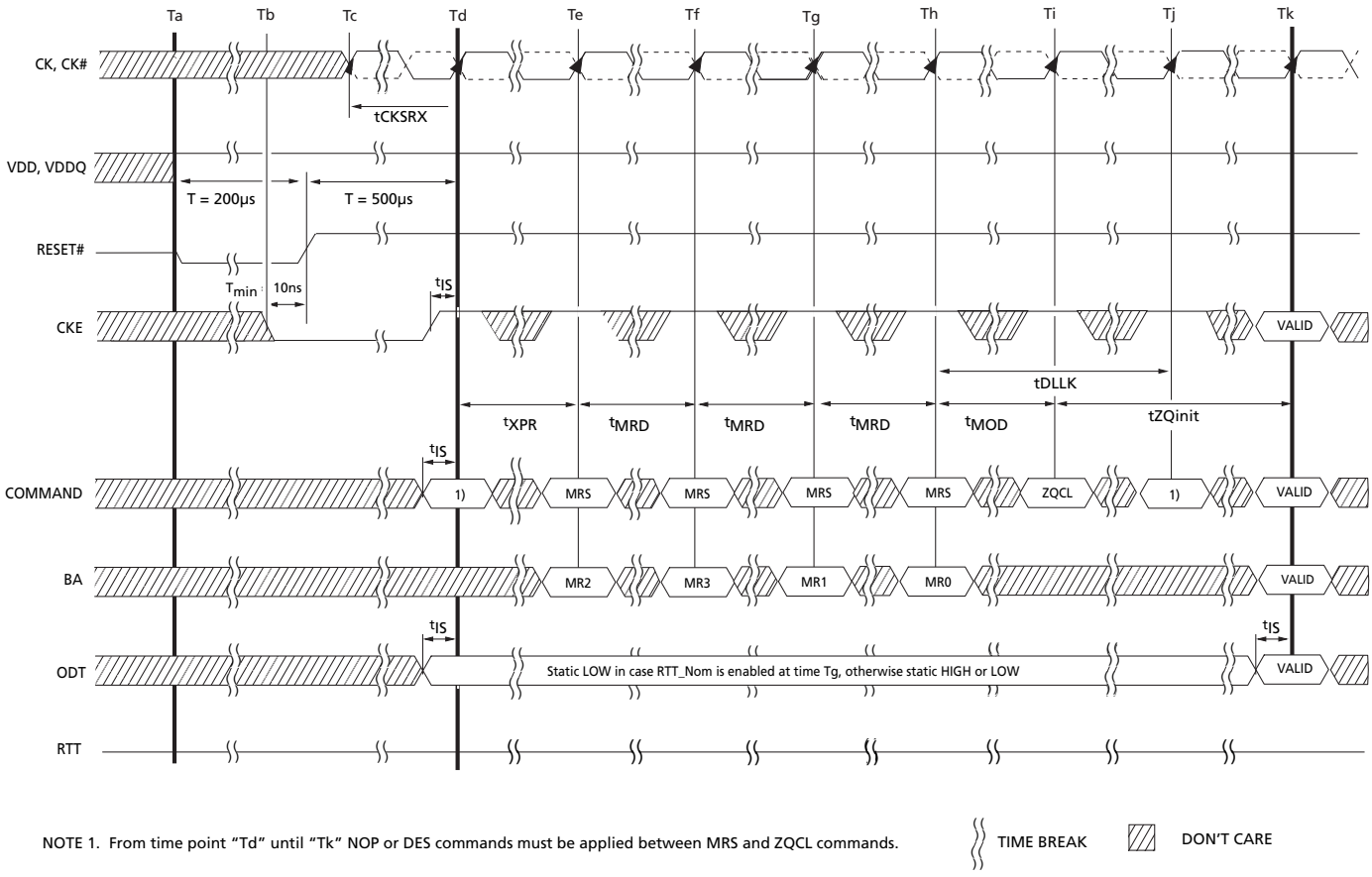
The following sequence is required for POWER UP and Initialization.

1. Apply power (RESET# is recommended to be maintained below 0.2 x VDD; all other inputs may be undefined). RESET# needs to be maintained for minimum 200 us with stable power. CKE is pulled "Low" anytime before RESET# being de-asserted (min. time 10 ns). The power voltage ramp time between 300 mv to VDDmin must be no greater than 200 ms; and during the ramp, VDD > VDDQ and (VDD - VDDQ) < 0.3 volts.
   - VDD and VDDQ are driven from a single power converter output, AND
   - The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side. In addition, VTT is limited to 0.95 V max once power ramp is finished, AND
   - Vref tracks VDDQ/2.

OR

   - Apply VDD without any slope reversal before or at the same time as VDDQ.
   - Apply VDDQ without any slope reversal before or at the same time as VTT & Vref.
   - The voltage levels on all pins other than VDD, VDDQ, VSS, VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side.
2. After RESET# is de-asserted, wait for another 500 us until CKE becomes active. During this time, the DRAM will start internal state initialization; this will be done independently of external clocks.
3. Clocks (CK, CK#) need to be started and stabilized for at least 10 ns or 5 tCK (which is larger) before CKE goes active. Since CKE is a synchronous signal, the corresponding set up time to clock (tIS) must be met. Also, a NOP or Deselect command must be registered (with tIS set up time to clock) before CKE goes active. Once the CKE is registered "High" after Reset, CKE needs to be continuously registered "High" until the initialization sequence is finished, including expiration of tDLLK and tZQinit.
4. The DDR3 SDRAM keeps its on-die termination in high-impedance state as long as RESET# is asserted. Further, the SDRAM keeps its on-die termination in high impedance state after RESET# deassertion until CKE is registered HIGH. The ODT input signal may be in undefined state until tIS before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal may be statically held at either LOW or HIGH. If RTT_NOM is to be enabled in MR1, the ODT input signal must be statically held LOW. In all cases, the ODT input signal remains static until the power up initialization sequence is finished, including the expiration of tDLLK and tZQinit.
5. After CKE is being registered high, wait minimum of Reset CKE Exit time, tXPR, before issuing the first MRS command to load mode register. *(tXPR=max (tXS ; 5 x tCK)*
6. Issue MRS Command to load MR2 with all application settings. (To issue MRS command for MR2, provide "Low" to BA0 and BA2, "High" to BA1.)
7. Issue MRS Command to load MR3 with all application settings. (To issue MRS command for MR3, provide "Low" to BA2, "High" to BA0 and BA1.)
8. Issue MRS Command to load MR1 with all application settings and DLL enabled. (To issue "DLL Enable" command, provide "Low" to A0, "High" to BA0 and "Low" to BA1 – BA2).
9. Issue MRS Command to load MR0 with all application settings and "DLL reset". (To issue DLL reset command, provide "High" to A8 and "Low" to BA0-2).
10. Issue ZQCL command to starting ZQ calibration.
11. Wait for both tDLLK and tZQinit completed.
12. The DDR3 SDRAM is now ready for normal operation.

3.3 RESET and Initialization Procedure (Cont'd)
3.3.1 Power-up Initialization Sequence (Cont'd)



NOTE 1. From time point "Td" until "Tk" NOP or DES commands must be applied between MRS and ZQCL commands.

Figure 5 — Reset and Initialization Sequence at Power-on Ramping

3 Functional Description (Cont'd)
3.3 RESET and Initialization Procedure (Cont'd)

3.3.2 Reset Initialization with Stable Power

The following sequence is required for RESET at no power interruption initialization.

1. Asserted RESET below 0.2 * VDD anytime when reset is needed (all other inputs may be undefined). RESET needs to be maintained for minimum 100 ns. CKE is pulled "LOW" before RESET being de-asserted (min. time 10 ns).
2. Follow Power-up Initialization Sequence steps 2 to 11.
3. The Reset sequence is now completed; DDR3 SDRAM is ready for normal operation.

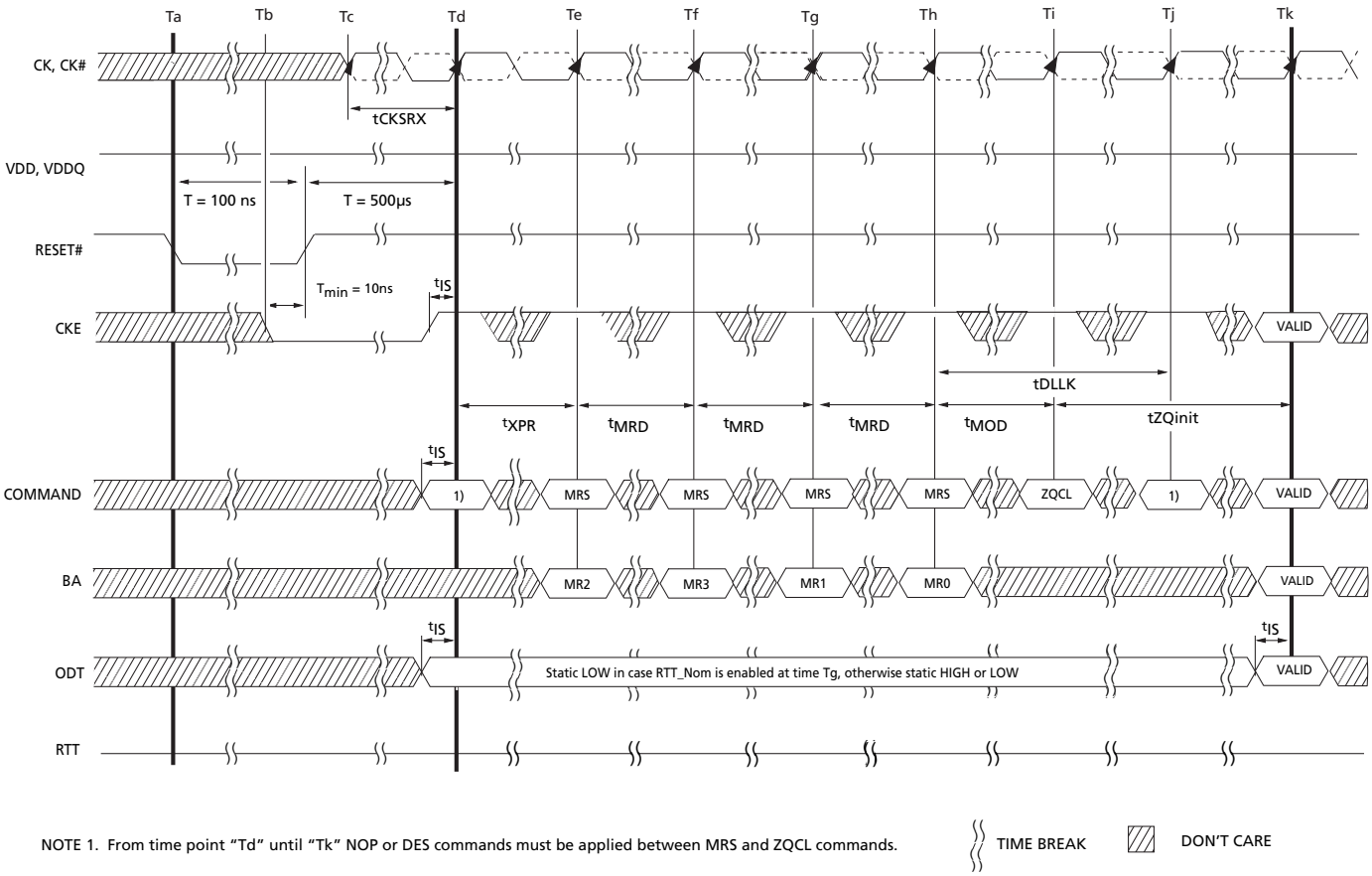


Figure 6 — Reset Procedure at Power Stable Condition

3.4 Register Definition

3.4.1 Programming the Mode Registers

For application flexibility, various functions, features, and modes are programmable in four Mode Registers, provided by the DDR3 SDRAM, as user defined variables and they must be programmed via a Mode Register Set (MRS) command. As the default values of the Mode Registers (MR#) are not defined, contents of Mode Registers must be fully initialized and/or re-initialized, i.e., written, after power up and/or reset for proper operation. Also the contents of the Mode Registers can be altered by re-executing the MRS command during normal operation. When programming the mode registers, even if the user chooses to modify only a sub-set of the MRS fields, all address fields within the accessed mode register must be redefined when the MRS command is issued. MRS command and DLL Reset do not affect array contents, which means these commands can be executed any time after power-up without affecting the array contents.

The mode register set command cycle time, tMRD is required to complete the write operation to the mode register and is the minimum time required between two MRS commands shown in Figure 7 .

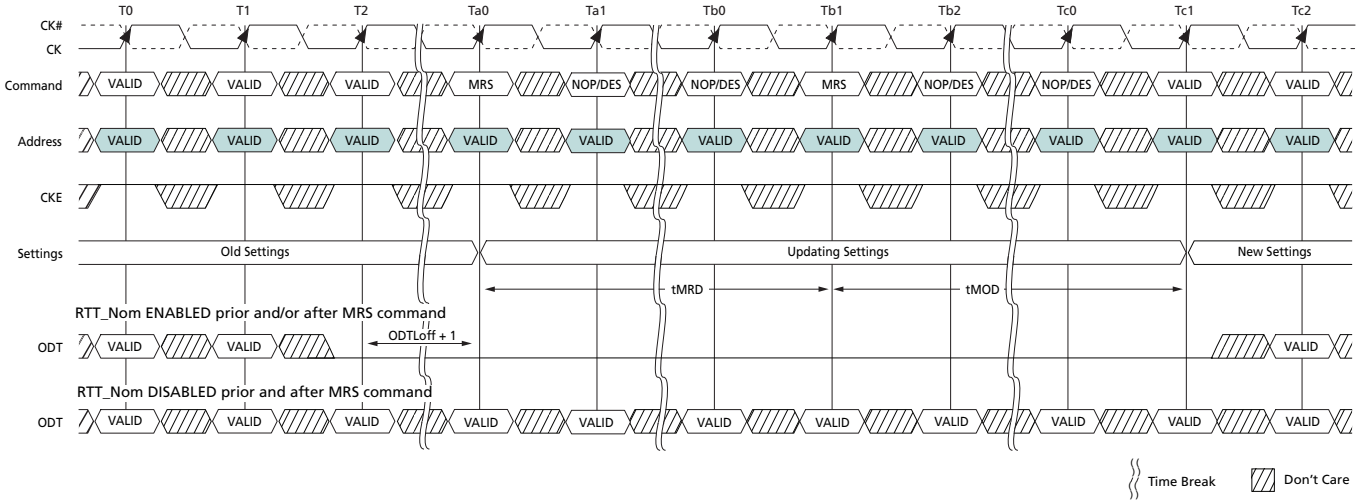


Figure 7 — tMRD Timing

The MRS command to Non-MRS command delay, tMOD, is required for the DRAM to update the features, except DLL reset, and is the minimum time required from an MRS command to a non-MRS command excluding NOP and DES shown in Figure 8.

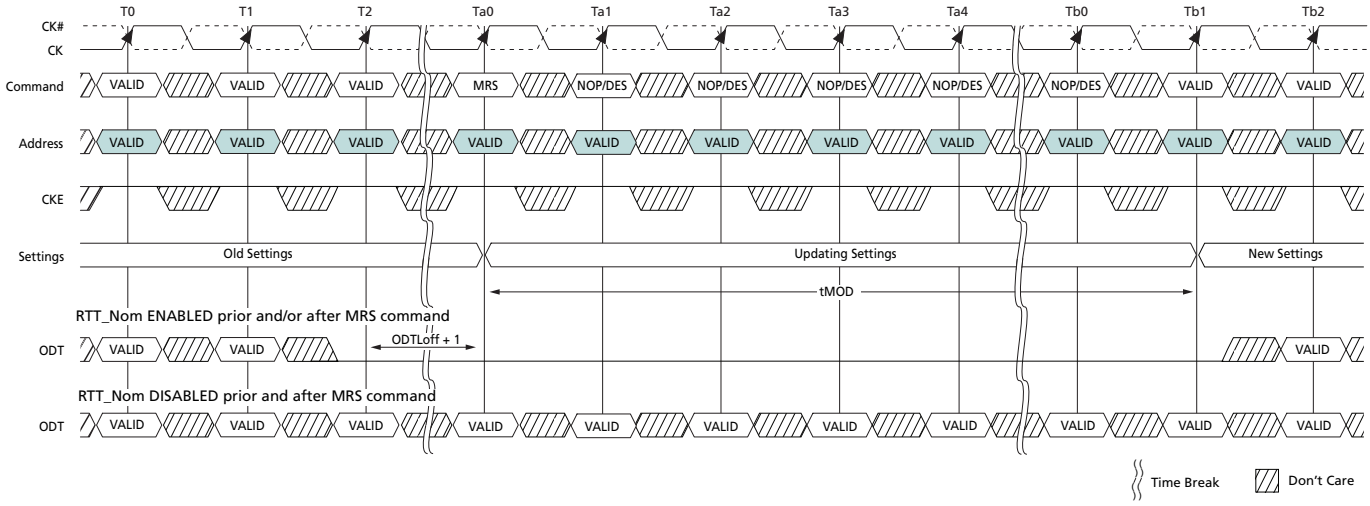


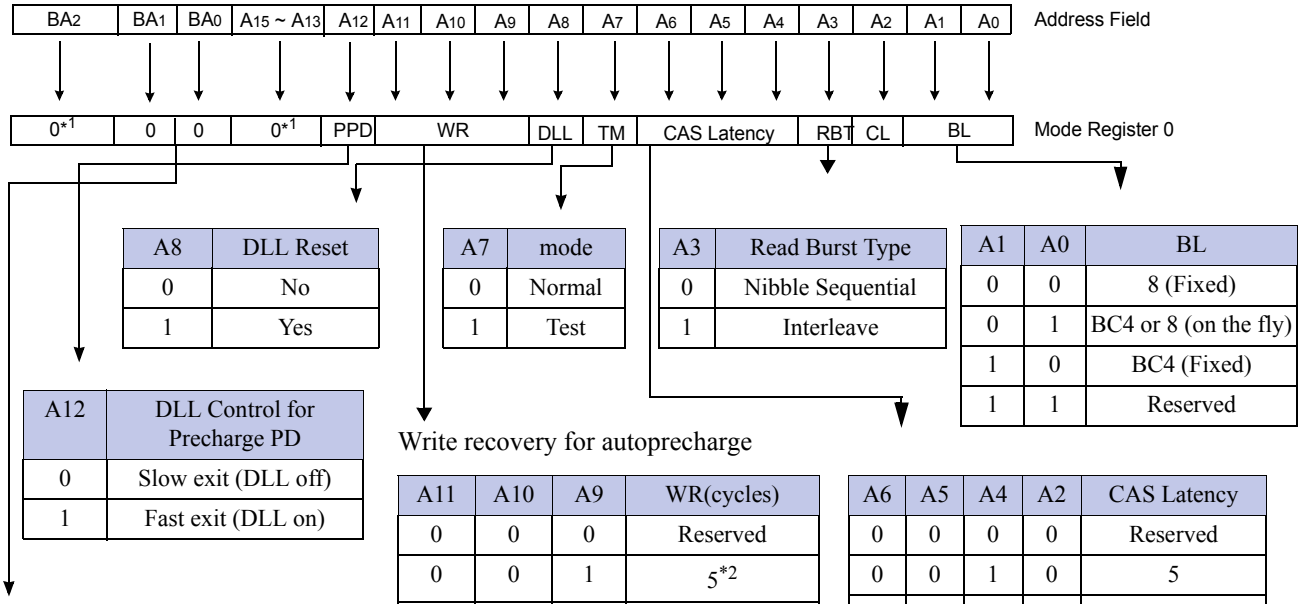
Figure 8 — tMOD Timing

3.4 Register Definition (Cont'd)
3.4.1 Programming the Mode Registers (Cont'd)

The mode register contents can be changed using the same command and timing requirements during normal operation as long as the DRAM is in idle state, i.e., all banks are in the precharged state with tRP satisfied, all data bursts are completed and CKE is high prior to writing into the mode register. If the RTT_NOM Feature is enabled in the Mode Register prior and/or after an MRS Command, the ODT Signal must continuously be registered LOW ensuring RTT is in an off State prior to the MRS command. The ODT Signal may be registered high after tMOD has expired. If the RTT_NOM Feature is disabled in the Mode Register prior and after an MRS command, the ODT Signal can be registered either LOW or HIGH before, during and after the MRS command. The mode registers are divided into various fields depending on the functionality and/or modes.

3.4.2 Mode Register MR0

The mode register MR0 stores the data for controlling various operating modes of DDR3 SDRAM. It controls burst length, read burst type, CAS latency, test mode, DLL reset, WR and DLL control for precharge Power-Down, which include various vendor specific options to make DDR3 SDRAM useful for various applications. The mode register is written by asserting low on CS#, RAS#, CAS#, WE#, BA0, BA1, and BA2, while controlling the states of address pins according to Figure 9.



A8	DLL Reset
0	No
1	Yes

A7	mode
0	Normal
1	Test

A3	Read Burst Type
0	Nibble Sequential
1	Interleave

A1	A0	BL
0	0	8 (Fixed)
0	1	BC4 or 8 (on the fly)
1	0	BC4 (Fixed)
1	1	Reserved

A12	DLL Control for Precharge PD
0	Slow exit (DLL off)
1	Fast exit (DLL on)

Write recovery for autoprecharge

A11	A10	A9	WR(cycles)
0	0	0	Reserved
0	0	1	5*2
0	1	0	6*2
0	1	1	7*2
1	0	0	8*2
1	0	1	10*2
1	1	0	12*2
1	1	1	Reserved

A6	A5	A4	A2	CAS Latency
0	0	0	0	Reserved
0	0	1	0	5
0	1	0	0	6
0	1	1	0	7
1	0	0	0	8
1	0	1	0	9
1	1	0	0	10
1	1	1	0	11 (Optional for DDR3-1600)

BA1	BA0	MR Select
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

*1: BA2 and A13~A15 are RFU and must be programmed to 0 during MRS.

*2: WR (write recovery for autoprecharge)min in clock cycles is calculated by dividing tWR(in ns) by tCK(in ns) and rounding up to the next integer: WRmin[cycles] = Roundup(tWR[ns] / tCK[ns]). The WR value in the mode register must be programmed to be equal or larger than WRmin. The programmed WR value is used with tRP to determine tDAL.

Figure 9 — MR0 Definition

3.4 Register Definition (Cont'd)
3.4.2 Mode Register MR0 (Cont'd)

3.4.2.1 Burst Length, Type and Order

Accesses within a given burst may be programmed to sequential or interleaved order. The burst type is selected via bit A3 as shown in Figure 9. The ordering of accesses within a burst is determined by the burst length, burst type, and the starting column address as shown in Table 3. The burst length is defined by bits A0-A1. Burst length options include fixed BC4, fixed BL8, and 'on the fly' which allows BC4 or BL8 to be selected coincident with the registration of a Read or Write command via A12/BC#.

Table 3 — Burst Type and Burst Order

Burst Length	READ/ WRITE	Starting Column ADDRESS (A2,A1,A0)	burst type = Sequential (decimal) A3 = 0	burst type = Interleaved (decimal) A3 = 1	Notes
4 Chop	READ	0 0 0	0,1,2,3,T,T,T,T	0,1,2,3,T,T,T,T	1, 2, 3
		0 0 1	1,2,3,0,T,T,T,T	1,0,3,2,T,T,T,T	1, 2, 3
		0 1 0	2,3,0,1,T,T,T,T	2,3,0,1,T,T,T,T	1, 2, 3
		0 1 1	3,0,1,2,T,T,T,T	3,2,1,0,T,T,T,T	1, 2, 3
		1 0 0	4,5,6,7,T,T,T,T	4,5,6,7,T,T,T,T	1, 2, 3
		1 0 1	5,6,7,4,T,T,T,T	5,4,7,6,T,T,T,T	1, 2, 3
		1 1 0	6,7,4,5,T,T,T,T	6,7,4,5,T,T,T,T	1, 2, 3
		1 1 1	7,4,5,6,T,T,T,T	7,6,5,4,T,T,T,T	1, 2, 3
	WRITE	0,V,V	0,1,2,3,X,X,X,X	0,1,2,3,X,X,X,X	1, 2, 4, 5
		1,V,V	4,5,6,7,X,X,X,X	4,5,6,7,X,X,X,X	1, 2, 4, 5
8	READ	0 0 0	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7	2
		0 0 1	1,2,3,0,5,6,7,4	1,0,3,2,5,4,7,6	2
		0 1 0	2,3,0,1,6,7,4,5	2,3,0,1,6,7,4,5	2
		0 1 1	3,0,1,2,7,4,5,6	3,2,1,0,7,6,5,4	2
		1 0 0	4,5,6,7,0,1,2,3	4,5,6,7,0,1,2,3	2
		1 0 1	5,6,7,4,1,2,3,0	5,4,7,6,1,0,3,2	2
		1 1 0	6,7,4,5,2,3,0,1	6,7,4,5,2,3,0,1	2
		1 1 1	7,4,5,6,3,0,1,2	7,6,5,4,3,2,1,0	2
	WRITE	V,V,V	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7	2, 4

NOTE 1 In case of burst length being fixed to 4 by MR0 setting, the internal write operation starts two clock cycles earlier than for the BL8 mode. This means that the starting point for tWR and tWTR will be pulled in by two clocks. In case of burst length being selected on-the-fly via A12/BC#, the internal write operation starts at the same point in time like a burst of 8 write operation. This means that during on-the-fly control, the starting point for tWR and tWTR will not be pulled in by two clocks.

NOTE 2 0...7 bit number is value of CA[2:0] that causes this bit to be the first read during a burst.

NOTE 3 T: Output driver for data and strobes are in high impedance.

NOTE 4 V: a valid logic level (0 or 1), but respective buffer input ignores level on input pins.

NOTE 5 X: Don't Care.

3.4.2.2 CAS Latency

The CAS Latency is defined by MR0 (bits A9-A11) as shown in Figure 9. CAS Latency is the delay, in clock cycles, between the internal Read command and the availability of the first bit of output data. DDR3 SDRAM does not support any half-clock latencies. The overall Read Latency (RL) is defined as Additive Latency (AL) + CAS Latency (CL); RL = AL + CL. For more information on the supported CL and AL settings based on the operating clock frequency, refer to "Standard Speed Bins" on page 157. For detailed Read operation, refer to "READ Operation" on page 56.

3.4 Register Definition (Cont'd)
3.4.2 Mode Register MR0 (Cont'd)

3.4.2.3 Test Mode

The normal operating mode is selected by MR0 (bit A7 = 0) and all other bits set to the desired values shown in Figure 9. Programming bit A7 to a '1' places the DDR3 SDRAM into a test mode that is only used by the DRAM Manufacturer and should NOT be used. No operations or functionality is specified if A7 = 1.

3.4.2.4 DLL Reset

The DLL Reset bit is self-clearing, meaning that it returns back to the value of '0' after the DLL reset function has been issued. Once the DLL is enabled, a subsequent DLL Reset should be applied. Any time that the DLL reset function is used, tDLLK must be met before any functions that require the DLL can be used (i.e., Read commands or ODT synchronous operations).

3.4.2.5 Write Recovery

The programmed WR value MR0 (bits A9, A10, and A11) is used for the auto precharge feature along with tRP to determine tDAL. WR (write recovery for auto-precharge) min in clock cycles is calculated by dividing tWR (in ns) by tCK (in ns) and rounding up to the next integer: WRmin[cycles] = Roundup(tWR[ns]/tCK[ns]). The WR must be programmed to be equal to or larger than tWR(min).

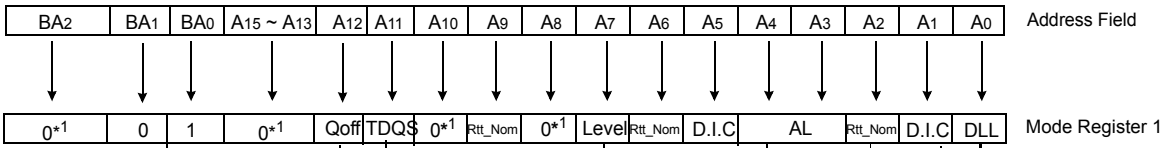
3.4.2.6 Precharge PD DLL

MR0 (bit A12) is used to select the DLL usage during precharge power-down mode. When MR0 (A12 = 0), or 'slow-exit', the DLL is frozen after entering precharge power-down (for potential power savings) and upon exit requires tXPDLL to be met prior to the next valid command. When MR0 (A12 = 1), or 'fast-exit', the DLL is maintained after entering precharge power-down and upon exiting power-down requires tXP to be met prior to the next valid command.

3 Functional Description (Cont'd)
3.4 Register Definition (Cont'd)

3.4.3 Mode Register MR1

The Mode Register MR1 stores the data for enabling or disabling the DLL, output driver strength, Rtt_Nom impedance, additive latency, Write leveling enable, TDQS enable and Qoff. The Mode Register 1 is written by asserting low on CS#, RAS#, CAS#, WE#, high on BA0 and low on BA1 and BA2, while controlling the states of address pins according to Figure 10.



A11	TDQS enable
0	Disabled
1	Enabled

A7	Write leveling enable
0	Disabled
1	Enabled

A4	A3	Additive Latency
0	0	0 (AL disabled)
0	1	CL-1
1	0	CL-2
1	1	Reserved

A9	A6	A2	Rtt_Nom*3
0	0	0	Rtt_Nom disabled
0	0	1	RZQ/4
0	1	0	RZQ/2
0	1	1	RZQ/6
1	0	0	RZQ/12*4
1	0	1	RZQ/8*4
1	1	0	Reserved
1	1	1	Reserved

Note: RZQ = 240 Ω

***3: In Write leveling Mode (MR1[bit7] = 1) with MR1[bit12]=1, all RTT_Nom settings are allowed; in Write Leveling Mode (MR1[bit7] = 1) with MR1[bit12]=0, only RTT_Nom settings of RZQ/2, RZQ/4 and RZQ/6 are allowed.**
***4: If RTT_Nom is used during Writes, only the values RZQ/2, RZQ/4 and RZQ/6 are allowed.**

A0	DLL Enable
0	Enable
1	Disable

A12	Qoff *2
0	Output buffer enabled
1	Output buffer disabled *2

*2: Outputs disabled - DQs, DQSs, DQS#s.

A5	A1	Output Driver Impedance Control
0	0	RZQ/6
0	1	RZQ/7
1	0	RZQ/TBD
1	1	RZQ/TBD

Note: RZQ = 240 Ω

BA1	BA0	MR Select
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

*** 1 : BA2 and A8, A10, and A13 ~ A15 are RFU and must be programmed to 0 during MRS.**

Figure 10 — MR1 Definition

3.4.3.1 DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having the DLL disabled. During normal operation (DLL-on) with

3.4 Register Definition (Cont'd)
3.4.3 Mode Register MR1 (Cont'd)

MR1 (A0 = 0), the DLL is automatically disabled when entering Self-Refresh operation and is automatically re-enabled upon exit of Self-Refresh operation. Any time the DLL is enabled and subsequently reset, tDLLK clock cycles must occur before a Read or synchronous ODT command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the tDQSCK, tAON or tAOF parameters. During tDLLK, CKE must continuously be registered high. DDR3 SDRAM does not require DLL for any Write operation, except when RTT_WR is enabled and the DLL is required for proper ODT operation. For more detailed information on DLL Disable operation refer to "DLL-off Mode" on page 37.

The direct ODT feature is not supported during DLL-off mode. The on-die termination resistors must be disabled by continuously registering the ODT pin low and/or by programming the RTT_Nom bits MR1{A9,A6,A2} to {0,0,0} via a mode register set command during DLL-off mode.

The dynamic ODT feature is not supported at DLL-off mode. User must use MRS command to set Rtt_WR, MR2 {A10, A9} = {0,0}, to disable Dynamic ODT externally.

3.4.3.2 Output Driver Impedance Control

The output driver impedance of the DDR3 SDRAM device is selected by MR1 (bits A1 and A5) as shown in Figure 10.

3.4.3.3 ODT Rtt Values

DDR3 SDRAM is capable of providing two different termination values (Rtt_Nom and Rtt_WR). The nominal termination value Rtt_Nom is programmed in MR1. A separate value (Rtt_WR) may be programmed in MR2 to enable a unique RTT value when ODT is enabled during writes. The Rtt_WR value can be applied during writes even when Rtt_Nom is disabled.

3.4.3.4 Additive Latency (AL)

Additive Latency (AL) operation is supported to make command and data bus efficient for sustainable bandwidths in DDR3 SDRAM. In this operation, the DDR3 SDRAM allows a read or write command (either with or without auto-precharge) to be issued immediately after the active command. The command is held for the time of the Additive Latency (AL) before it is issued inside the device. The Read Latency (RL) is controlled by the sum of the AL and CAS Latency (CL) register settings. Write Latency (WL) is controlled by the sum of the AL and CAS Write Latency (CWL) register settings. A summary of the AL register options are shown in Table 4.

Table 4 — Additive Latency (AL) Settings

A4	A3	AL
0	0	0 (AL Disabled)
0	1	CL - 1
1	0	CL - 2
1	1	Reserved

NOTE: AL has a value of CL - 1 or CL - 2 as per the CL values programmed in the MR0 register.

3.4.3.5 Write leveling

For better signal integrity, DDR3 memory module adopted fly-by topology for the commands, addresses, control signals, and clocks. The fly-by topology has the benefit of reducing the number of stubs and their length, but it also causes flight time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the Controller to maintain tDQSS, tDSS, and tDSH specification. Therefore, the DDR3 SDRAM supports a 'write leveling' feature to allow the controller to compensate for skew. See 4.8 "Write Leveling" on page 42 for more details.

3.4 Register Definition (Cont'd)
3.4.3 Mode Register MR1 (Cont'd)

3.4.3.6 Output Disable

The DDR3 SDRAM outputs may be enabled/disabled by MR1 (bit A12) as shown in Figure 10. When this feature is enabled (A12 = 1), all output pins (DQs, DQS, DQS#, etc.) are disconnected from the device, thus removing any loading of the output drivers. This feature may be useful when measuring module power, for example. For normal operation, A12 should be set to '0'.

3.4.3.7 TDQS, TDQS#

TDQS (Termination Data Strobe) is a feature of X8 DDR3 SDRAM that provides additional termination resistance outputs that may be useful in some system configurations.

TDQS is not supported in X4 or X16 configurations. When enabled via the mode register, the same termination resistance function is applied to the TDQS/TDQS# pins that is applied to the DQS/DQS# pins.

In contrast to the RDQS function of DDR2 SDRAM, TDQS provides the termination resistance function only. The data strobe function of RDQS is not provided by TDQS.

The TDQS and DM functions share the same pin. When the TDQS function is enabled via the mode register, the DM function is not supported. When the TDQS function is disabled, the DM function is provided and the TDQS# pin is not used. See Table 5 for details.

The TDQS function is available in X8 DDR3 SDRAM only and must be disabled via the mode register A11=0 in MR1 for X4 and X16 configurations.

Table 5 — TDQS, TDQS# Function Matrix

MR1 (A11)	DM / TDQS	NU / TDQS
0 (TDQS Disabled)	DM	Hi-Z
1 (TDQS Enabled)	TDQS	TDQS#

NOTE 1 If TDQS is enabled, the DM function is disabled.

NOTE 2 When not used, TDQS function can be disabled to save termination power.

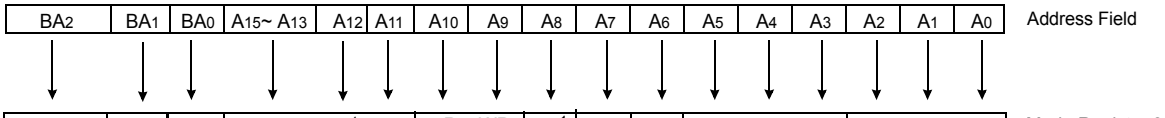
NOTE 3 TDQS function is only available for X8 DRAM and must be disabled for X4 and X16.

3 Functional Description (Cont'd)
3.4 Register Definition (Cont'd)

3.4.4 Mode Register MR2

The Mode Register MR2 stores the data for controlling refresh related features, Rtt_WR impedance, and CAS write latency. The Mode Register 2 is written by asserting low on CS#, RAS#, CAS#, WE#, high on BA1 and low on BA0 and BA2, while controlling the states of address pins according to the table below.

MR2 Programming



A7	Self-Refresh Temperature (SRT) Range
0	Normal operating temperature range
1	Extended (optional) operating temperature range

A6	Auto Self-Refresh (ASR)
0	Manual SR Reference (SRT)
1	ASR enable (Optional)

A2	A1	A0	Partial Array Self-Refresh (Optional)
0	0	0	Full Array
0	0	1	HalfArray (BA[2:0]=000,001,010, &011)
0	1	0	Quarter Array (BA[2:0]=000, & 001)
0	1	1	1/8th Array (BA[2:0] = 000)
1	0	0	3/4 Array (BA[2:0] = 010,011,100,101,110, & 111)
1	0	1	HalfArray (BA[2:0] = 100, 101, 110, &111)
1	1	0	Quarter Array (BA[2:0]=110, &111)
1	1	1	1/8th Array (BA[2:0]=111)

A10	A9	Rtt_WR *2
0	0	Dynamic ODT off (Write does not affect Rtt value)
0	1	RZQ/4
1	0	RZQ/2
1	1	Reserved

A5	A4	A3	CAS write Latency (CWL)
0	0	0	5 (tCK(avg) ≥ 2.5ns)
0	0	1	6 (2.5ns > tCK(avg) ≥ 1.875ns)
0	1	0	7 (1.875ns > tCK(avg) ≥ 1.5ns)
0	1	1	8 (1.5ns > tCK(avg) ≥ 1.25ns)
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

BA1	BA0	MR Select
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

*** 1 : BA2, A5, A8, A11 ~ A15 are RFU and must be programmed to 0 during MRS.**
*** 2 : The Rtt_WR value can be applied during writes even when Rtt_Nom is disabled. During write leveling, Dynamic ODT is not available.**

Figure 11 — MR2 Definition

3.4 Register Definition (Cont'd)
3.4.4 Mode Register MR2 (Cont'd)

3.4.4.1 Partial Array Self-Refresh (PASR)

Optional in DDR3 SDRAM: Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR3 SDRAM devices support the following options or requirements referred to in this material. If PASR (Partial Array Self-Refresh) is enabled, data located in areas of the array beyond the specified address range shown in Figure 11 will be lost if Self-Refresh is entered. Data integrity will be maintained if tREFI conditions are met and no Self-Refresh command is issued.

3.4.4.2 CAS Write Latency (CWL)

The CAS Write Latency is defined by MR2 (bits A3-A5), as shown in Figure 11. CAS Write Latency is the delay, in clock cycles, between the internal Write command and the availability of the first bit of input data. DDR3 SDRAM does not support any half-clock latencies. The overall Write Latency (WL) is defined as Additive Latency (AL) + CAS Write Latency (CWL); WL = AL + CWL. For more information on the supported CWL and AL settings based on the operating clock frequency, refer to "Standard Speed Bins" on page 157. For detailed Write operation refer to "WRITE Operation" on page 68.

3.4.4.3 Auto Self-Refresh (ASR) and Self-Refresh Temperature (SRT)

Optional in DDR3 SDRAM: Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR3 SDRAM devices support the following options or requirements referred to in this material. For more details refer to "Extended Temperature Usage" on page 46. DDR3 SDRAMs must support Self-Refresh operation at all supported temperatures. Applications requiring Self-Refresh operation in the Extended Temperature Range must use the optional ASR function or program the SRT bit appropriately.

3.4.4.4 Dynamic ODT (Rtt_WR)

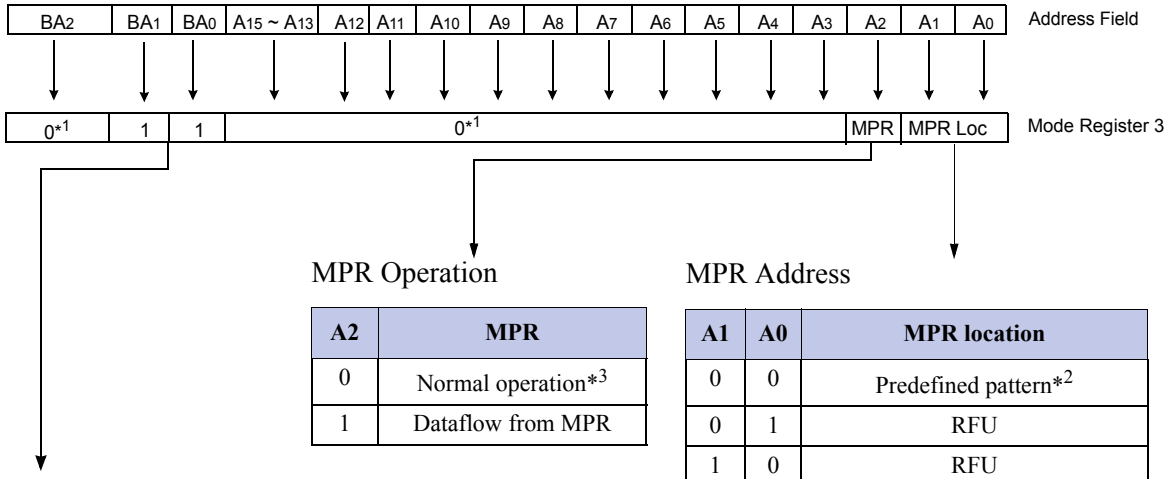
DDR3 SDRAM introduces a new feature "Dynamic ODT". In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the DDR3 SDRAM can be changed without issuing an MRS command. MR2 Register locations A9 and A10 configure the Dynamic ODT setings. In Write leveling mode, only RTT_Nom is available. For details on Dynamic ODT operation, refer to "Dynamic ODT" on page 96.

3 Functional Description (Cont'd)
3.4 Register Definition (Cont'd)

3.4.5 Mode Register MR3

The Mode Register MR3 controls Multi purpose registers. The Mode Register 3 is written by asserting low on CS#, RAS#, CAS#, WE#, high on BA1 and BA0, and low on BA2 while controlling the states of address pins according to the table below.

MR3 Programming



MPR Operation

A2	MPR
0	Normal operation*3
1	Dataflow from MPR

MPR Address

A1	A0	MPR location
0	0	Predefined pattern*2
0	1	RFU
1	0	RFU
1	1	RFU

BA1	BA0	MR Select
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

*** 1 : BA2, A3 - A15 are RFU and must be programmed to 0 during MRS.**
*** 2 : The predefined pattern will be used for read synchronization.**
*** 3 : When MPR control is set for normal operation (MR3 A[2] = 0) then MR3 A[1:0] will be ignored.**

Figure 12 — MR3 Definition

3.4.5.1 Multi-Purpose Register (MPR)

The Multi Purpose Register (MPR) function is used to Read out a predefined system timing calibration bit sequence. To enable the MPR, a MODE Register Set (MRS) command must be issued to MR3 Register with bit A2 = 1. Prior to issuing the MRS command, all banks must be in the idle state (all banks precharged and tRP met). Once the MPR is enabled, any subsequent RD or RDA commands will be redirected to the Multi Purpose Register. When the MPR is enabled, only RD or RDA commands are allowed until a subsequent MRS command is issued with the MPR disabled (MR3 bit A2 = 0). Power-Down mode, Self-Refresh, and any other non-RD/RDA command is not allowed during MPR enable mode. The RESET function is supported during MPR enable mode. For detailed MPR operation refer to "Multi Purpose Register" on page 48.

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4 DDR3 SDRAM Command Description and Operation

4.1 Command Truth Table

Notes 1, 2, 3, and 4 apply to the entire Command Truth Table

Note 5 applies to all Read/Write commands

[BA=Bank Address, RA=Row Address, CA=Column Address, BC#=Burst Chop, X=Don't Care, V=Valid]

Table 6 — Command Truth Table

Function	Abbreviation	CKE		CS#	RAS#	CAS#	WE#	BA0-BA2	A13-A15	A12-BC#	A10-AP	A0-A9, A11	Notes
		Previous Cycle	Current Cycle										
Mode Register Set	MRS	H	H	L	L	L	L	BA	OP Code				
Refresh	REF	H	H	L	L	L	H	V	V	V	V	V	
Self Refresh Entry	SRE	H	L	L	L	L	H	V	V	V	V	V	7,9,12
Self Refresh Exit	SRX	L	H	H	X	X	X	X	X	X	X	X	7,8,9, 12
				L	H	H	H	V	V	V	V	V	
Single Bank Precharge	PRE	H	H	L	L	H	L	BA	V	V	L	V	
Precharge all Banks	PREA	H	H	L	L	H	L	V	V	V	H	V	
Bank Activate	ACT	H	H	L	L	H	H	BA	Row Address (RA)				
Write (Fixed BL8 or BC4)	WR	H	H	L	H	L	L	BA	RFU	V	L	CA	
Write (BC4, on the Fly)	WRS4	H	H	L	H	L	L	BA	RFU	L	L	CA	
Write (BL8, on the Fly)	WRS8	H	H	L	H	L	L	BA	RFU	H	L	CA	
Write with Auto Precharge (Fixed BL8 or BC4)	WRA	H	H	L	H	L	L	BA	RFU	V	H	CA	
Write with Auto Precharge (BC4, on the Fly)	WRAS4	H	H	L	H	L	L	BA	RFU	L	H	CA	
Write with Auto Precharge (BL8, on the Fly)	WRAS8	H	H	L	H	L	L	BA	RFU	H	H	CA	
Read (Fixed BL8 or BC4)	RD	H	H	L	H	L	H	BA	RFU	V	L	CA	
Read (BC4, on the Fly	RDS4	H	H	L	H	L	H	BA	RFU	L	L	CA	
Read (BL8, on the Fly)	RDS8	H	H	L	H	L	H	BA	RFU	H	L	CA	
Read with Auto Precharge (Fixed BL8 or BC4)	RDA	H	H	L	H	L	H	BA	RFU	V	H	CA	
Read with Auto Precharge (BC4, on the Fly)	RDAS4	H	H	L	H	L	H	BA	RFU	L	H	CA	
Read with Auto Precharge (BL8, on the Fly)	RDAS8	H	H	L	H	L	H	BA	RFU	H	H	CA	
No Operation	NOP	H	H	L	H	H	H	V	V	V	V	V	10
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	11
Power Down Entry	PDE	H	L	L	H	H	H	V	V	V	V	V	6,12
				H	X	X	X	X	X	X	X	X	
Power Down Exit	PDX	L	H	L	H	H	H	V	V	V	V	V	6,12
				H	X	X	X	X	X	X	X	X	
ZQ Calibration Long	ZQCL	H	H	L	H	H	L	X	X	X	H	X	
ZQ Calibration Short	ZQCS	H	H	L	H	H	L	X	X	X	L	X	

4 DDR3 SDRAM Command Description and Operation (Cont'd)
4.1 Command Truth Table (Cont'd)

Table 6 — Command Truth Table (Cont'd)

Function	Abbreviation	CKE		CS#	RAS#	CAS#	WE#	BA0-BA2	A13-A15	A12-BC#	A10-AP	A0-A9, A11	Notes
		Previous Cycle	Current Cycle										

NOTE 1 All DDR3 SDRAM commands are defined by states of CS#, RAS#, CAS#, WE# and CKE at the rising edge of the clock. The MSB of BA, RA and CA are device density and configuration dependant.

NOTE 2 RESET# is Low enable command which will be used only for asynchronous reset so must be maintained HIGH during any function.

NOTE 3 Bank addresses (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register.

NOTE 4 "V" means "H or L (but a defined logic level)" and "X" means either "defined or undefined (like floating) logic level".

NOTE 5 Burst reads or writes cannot be terminated or interrupted and Fixed/on-the-Fly BL will be defined by MRS.

NOTE 6 The Power Down Mode does not perform any refresh operation.

NOTE 7 The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.

NOTE 8 Self Refresh Exit is asynchronous.

NOTE 9 VREF(Both VrefDQ and VrefCA) must be maintained during Self Refresh operation.

NOTE 10 The No Operation command should be used in cases when the DDR3 SDRAM is in an idle or wait state. The purpose of the No Operation command (NOP) is to prevent the DDR3 SDRAM from registerng any unwanted commands between operations. A No Operation command will not terminate a pervious operation that is still executing, such as a burst read or write cycle.

NOTE 11 The Deselect command performs the same function as No Operation command.

NOTE 12 Refer to the CKE Truth Table for more detail with CKE transition.

4 DDR3 SDRAM Command Description and Operation (Cont'd)

4.2 CKE Truth Table

Notes 1-7 apply to the entire CKE Truth Table.

For Power-down entry and exit parameters See 4.17 "Power-Down Modes" on page 81.

CKE low is allowed only if tMRD and tMOD are satisfied.

Table 7 — CKE Truth Table

Current State[2]	CKE		Command (N)[3] RAS#, CAS#, WE#, CS#	Action (N)[3]	Notes
	Previous Cycle[1] (N-1)	Current Cycle[1] (N)			
Power-Down	L	L	X	Maintain Power-Down	14, 15
	L	H	DESELECT or NOP	Power-Down Exit	11,14
Self-Refresh	L	L	X	Maintain Self-Refresh	15,16
	L	H	DESELECT or NOP	Self-Refresh Exit	8,12,16
Bank(s) Active	H	L	DESELECT or NOP	Active Power-Down Entry	11,13,14
Reading	H	L	DESELECT or NOP	Power-Down Entry	11,13,14,17
Writing	H	L	DESELECT or NOP	Power-Down Entry	11,13,14,17
Precharging	H	L	DESELECT or NOP	Power-Down Entry	11,13,14,17
Refreshing	H	L	DESELECT or NOP	Precharge Power-Down Entry	11
All Banks Idle	H	L	DESELECT or NOP	Precharge Power-Down Entry	11,13,14,18
	H	L	REFRESH	Self-Refresh	9,13,18
For more details with all signals See 4.1 "Command Truth Table" on page 33.					10

NOTE 1 CKE (N) is the logic state of CKE at clock edge N; CKE (N-1) was the state of CKE at the previous clock edge.

NOTE 2 Current state is defined as the state of the DDR3 SDRAM immediately prior to clock edge N.

NOTE 3 COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N), ODT is not included here.

NOTE 4 All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.

NOTE 5 The state of ODT does not affect the states described in this table. The ODT function is not available during Self-Refresh.

NOTE 6 CKE must be registered with the same value on tCKEmin consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the tCKEmin clocks of registeration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of tIS + tCKEmin + tIH.

NOTE 7 DESELECT and NOP are defined in the Command Truth Table.

NOTE 8 On Self-Refresh Exit DESELECT or NOP commands must be issued on every clock edge occurring during the tXS period. Read or ODT commands may be issued only after tXSDLL is satisfied.

NOTE 9 Self-Refresh mode can only be entered from the All Banks Idle state.

NOTE 10 Must be a legal command as defined in the Command Truth Table.

NOTE 11 Valid commands for Power-Down Entry and Exit are NOP and DESELECT only.

NOTE 12 Valid commands for Self-Refresh Exit are NOP and DESELECT only.

NOTE 13 Self-Refresh can not be entered during Read or Write operations. For a detailed list of restrictions See 4.16 "Self-Refresh Operation" on page 79 and See 4.17 "Power-Down Modes" on page 81.

4 DDR3 SDRAM Command Description and Operation (Cont'd)
4.2 CKE Truth Table (Cont'd)

Table 7 — CKE Truth Table (Cont'd)

Current State[2]	CKE		Command (N)[3] RAS#, CAS#, WE#, CS#	Action (N)[3]	Notes
	Previous Cycle[1] (N-1)	Current Cycle[1] (N)			
NOTE 14 The Power-Down does not perform any refresh operations.					
NOTE 15 "X" means "don't care" (including floating around VREF) in Self-Refresh and Power-Down. It also applies to Address pins.					
NOTE 16 VREF (Both Vref_DQ and Vref_CA) must be maintained during Self-Refresh operation.					
NOTE 17 If all banks are closed at the conclusion of the read, write or precharge command, then Precharge Power-Down is entered, otherwise Active Power-Down is entered.					
NOTE 18 'Idle state' is defined as all banks are closed (tRP, tDAL, etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied (tMRD, tMOD, tRFC, tZQinit, tZQoper, tZQCS, etc.) as well as all Self-Refresh exit and Power-Down Exit parameters are satisfied (tXS, tXP, tXPDLL, etc).					

4.3 No OPeration (NOP) Command

The No OPeration (NOP) command is used to instruct the selected DDR3 SDRAM to perform a NOP (CS# LOW and RAS#, CAS#, and WE# HIGH). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

4.4 Deselect Command

The DESELECT function (CS# HIGH) prevents new commands from being executed by the DDR3 SDRAM. The DDR3 SDRAM is effectively deselected. Operations already in progress are not affected.

4 DDR3 SDRAM Command Description and Operation (Cont'd)

4.5 DLL-off Mode

DDR3 DLL-off mode is entered by setting MR1 bit A0 to "1"; this will disable the DLL for subsequent operations until A0 bit is set back to "0". The MR1 A0 bit for DLL control can be switched either during initialization or later. Refer to "Input clock frequency change" on page 40

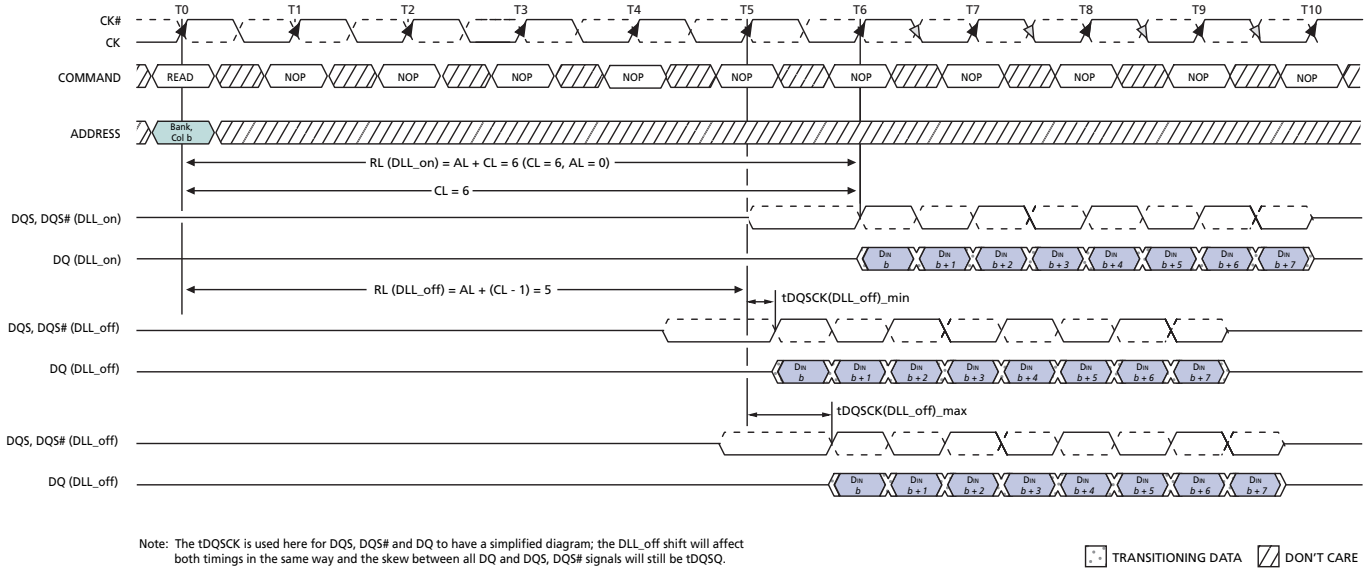
The DLL-off Mode operations listed below are an optional feature for DDR3. The maximum clock frequency for DLL-off Mode is specified by the parameter tCKDLL_OFF. There is no minimum frequency limit besides the need to satisfy the refresh interval, tREFI.

Due to latency counter and timing restrictions, only one value of CAS Latency (CL) in MR0 and CAS Write Latency (CWL) in MR2 are supported. The DLL-off mode is only required to support setting of both CL=6 and CWL=6.

DLL-off mode will affect the Read data Clock to Data Strobe relationship (tDQSCK), but not the Data Strobe to Data relationship (tDQSQ, tQH). Special attention is needed to line up Read data to controller time domain.

Comparing with DLL-on mode, where tDQSCK starts from the rising clock edge (AL+CL) cycles after the Read command, the DLL-off mode tDQSCK starts (AL+CL - 1) cycles after the read command. Another difference is that tDQSCK may not be small compared to tCK (it might even be larger than tCK) and the difference between tDQSCKmin and tDQSCKmax is significantly larger than in DLL-on mode. tDQSCK(DLL_off) values are vendor specific.

The timing relations on DLL-off mode READ operation are shown in the following Timing Diagram (CL=6, BL=8):



Note: The tDQSCK is used here for DQS, DQS# and DQ to have a simplified diagram; the DLL_off shift will affect both timings in the same way and the skew between all DQ and DQS, DQS# signals will still be tDQSQ.

Figure 13 — DLL-off mode READ Timing Operation

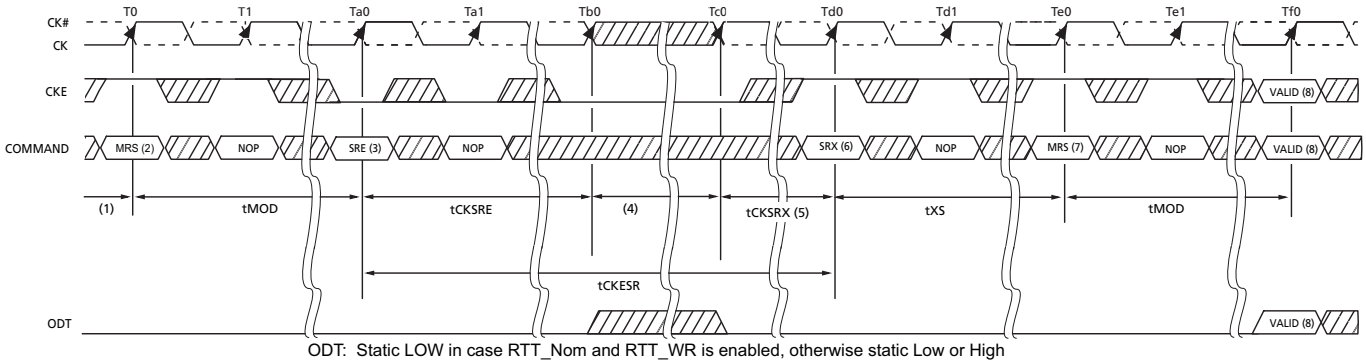
4.6 DLL on/off switching procedure

DDR3 DLL-off mode is entered by setting MR1 bit A0 to "1"; this will disable the DLL for subsequent operations until A0 bit is set back to "0".

4.6.1 DLL "on" to DLL "off" Procedure

To switch from DLL "on" to DLL "off" requires the frequency to be changed during Self-Refresh, as outlined in the following procedure:

1. Starting from Idle state (All banks pre-charged, all timings fulfilled, and DRAMs On-die Termination resistors, RTT, must be in high impedance state before MRS to MR1 to disable the DLL.)
2. Set MR1 bit A0 to "1" to disable the DLL.
3. Wait tMOD.
4. Enter Self Refresh Mode; wait until (tCKSRE) is satisfied.
5. Change frequency, in guidance with "Input clock frequency change" on page 40.
6. Wait until a stable clock is available for at least (tCKSRX) at DRAM inputs.
7. Starting with the Self Refresh Exit command, CKE must continuously be registered HIGH until all tMOD timings from any MRS command are satisfied. In addition, if any ODT features were enabled in the mode registers when Self Refresh mode was entered, the ODT signal must continuously be registered LOW until all tMOD timings from any MRS command are satisfied. If both ODT features were disabled in the mode registers when Self Refresh mode was entered, ODT signal can be registered LOW or HIGH.
8. Wait tXS, then set Mode Registers with appropriate values (especially an update of CL, CWL and WR may be necessary. A ZQCL command may also be issued after tXS).
9. Wait for tMOD, then DRAM is ready for next command.



NOTES:
1. Starting with Idle State, RTT in Hi-Z state
2. Disable DLL by setting MR1 Bit A0 to 1
3. Enter SR
4. Change Frequency
5. Clock must be stable tCKSRX
6. Exit SR
7. Update Mode registers with DLL off parameters setting
8. Any valid command

TIME BREAK DON'T CARE

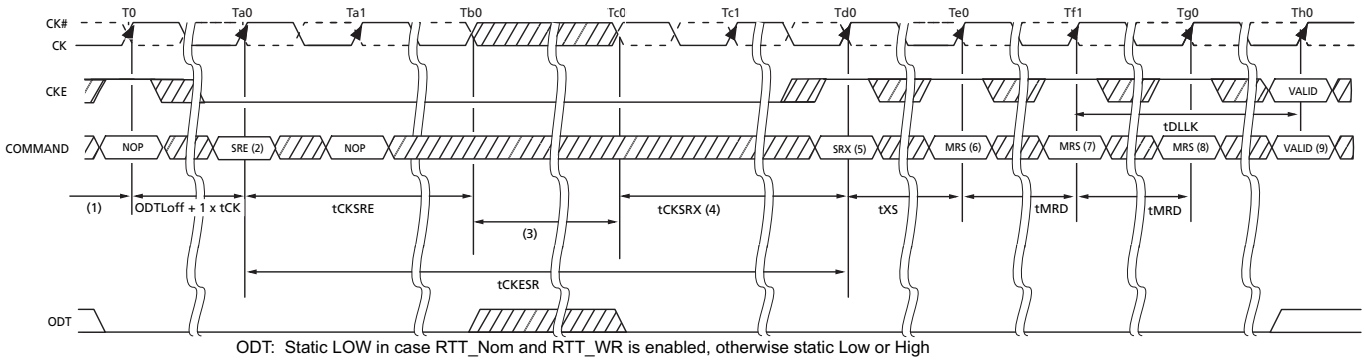
Figure 14 — DLL Switch Sequence from DLL-on to DLL-off

4 DDR3 SDRAM Command Description and Operation (Cont'd)
4.6 DLL on/off switching procedure (Cont'd)

4.6.2 DLL "off" to DLL "on" Procedure

To switch from DLL "off" to DLL "on" (with required frequency change) during Self-Refresh:

1. Starting from Idle state (All banks pre-charged, all timings fulfilled and DRAMs On-die Termination resistors (RTT) must be in high impedance state before Self-Refresh mode is entered.)
2. Enter Self Refresh Mode, wait until tCKSRE satisfied.
3. Change frequency, in guidance with "Input clock frequency change" on page 40.
4. Wait until a stable clock is available for at least (tCKSRX) at DRAM inputs.
5. Starting with the Self Refresh Exit command, CKE must continuously be registered HIGH until tDLLK timing from subsequent DLL Reset command is satisfied. In addition, if any ODT features were enabled in the mode registers when Self Refresh mode was entered, the ODT signal must continuously be registered LOW until tDLLK timings from subsequent DLL Reset command is satisfied. If both ODT features are disabled in the mode registers when Self Refresh mode was entered, ODT signal can be registered LOW or HIGH.
6. Wait tXS, then set MR1 bit A0 to "0" to enable the DLL.
7. Wait tMRD, then set MR0 bit A8 to "1" to start DLL Reset.
8. Wait tMRD, then set Mode Registers with appropriate values (especially an update of CL, CWL and WR may be necessary. After tMOD satisfied from any proceeding MRS command, a ZQCL command may also be issued during or after tDLLK.)
9. Wait for tMOD, then DRAM is ready for next command (Remember to wait tDLLK after DLL Reset before applying command requiring a locked DLL!). In addition, wait also for tZQoper in case a ZQCL command was issued.



NOTES:
1. Starting with Idle State
2. Enter SR
3. Change Frequency
4. Clock must be stable tCKSRX
5. Exit SR
6. Set DLL on by MR1 A0=0
7. Update Mode registers
8. Any valid command

TIME BREAK DON'T CARE

Figure 15 — DLL Switch Sequence from DLL Off to DLL On

4.7 Input clock frequency change

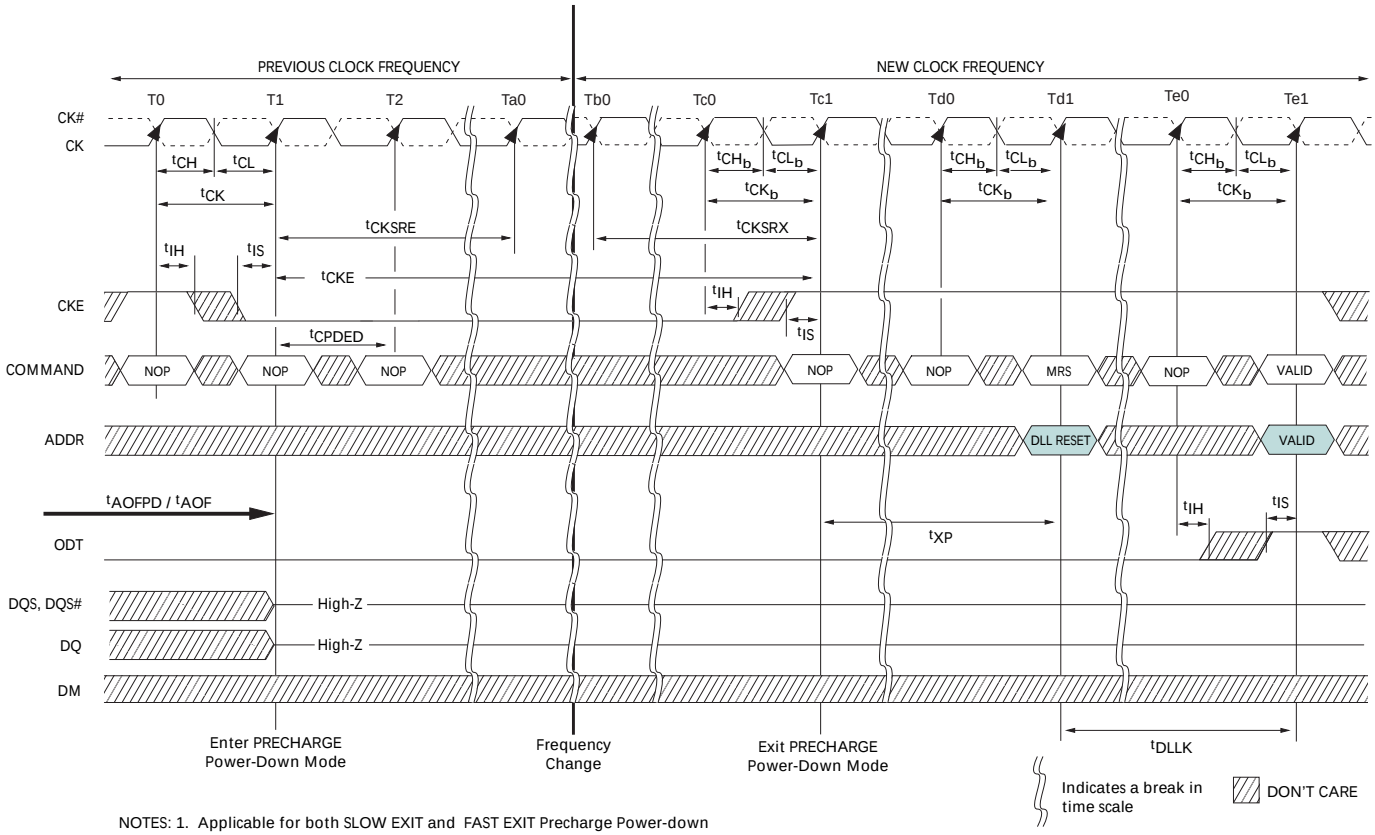
Once the DDR3 SDRAM is initialized, the DDR3 SDRAM requires the clock to be "stable" during almost all states of normal operation. This means that, once the clock frequency has been set and is to be in the "stable state", the clock period is not allowed to deviate except for what is allowed for by the clock jitter and SSC (spread spectrum clocking) specifications.

The input clock frequency can be changed from one stable clock rate to another stable clock rate under two conditions: (1) Self-Refresh mode and (2) Precharge Power-down mode. Outside of these two modes, it is illegal to change the clock frequency.

For the first condition, once the DDR3 SDRAM has been successfully placed in to Self-Refresh mode and ^{t}CKSRE has been satisfied, the state of the clock becomes a don't care. Once a don't care, changing the clock frequency is permissible, provided the new clock frequency is stable prior to ^{t}CKSRX. When entering and exiting Self-Refresh mode for the sole purpose of changing the clock frequency, the Self-Refresh entry and exit specifications must still be met as outlined in See 4.16 "Self-Refresh Operation" on page 79. The DDR3 SDRAM input clock frequency is allowed to change only within the minimum and maximum operating frequency specified for the particular speed grade. Any frequency change below the minimum operating frequency would require the use of DLL_on- mode -> DLL_off -mode transition sequence, refer to "DLL on/off switching procedure" on page 38.

The second condition is when the DDR3 SDRAM is in Precharge Power-down mode (either fast exit mode or slow exit mode). If the RTT_NOM feature was enabled in the mode register prior to entering Precharge power down mode, the ODT signal must continuously be registered LOW ensuring RTT is in an off state. If the RTT_NOM feature was disabled in the mode register prior to entering Precharge power down mode, RTT will remain in the off state. The ODT signal can be registered either LOW or HIGH in this case. A minimum of ^{t}CKSRE must occur after CKE goes LOW before the clock frequency may change. The DDR3 SDRAM input clock frequency is allowed to change only within the minimum and maximum operating frequency specified for the particular speed grade. During the input clock frequency change, ODT and CKE must be held at stable LOW levels. Once the input clock frequency is changed, stable new clocks must be provided to the DRAM ^{t}CKSRX before Precharge Power-down may be exited; after Precharge Power-down is exited and tXP has expired, the DLL must be RESET via MRS. Depending on the new clock frequency, additional MRS commands may need to be issued to appropriately set the WR, CL, and CWL with CKE continuously registered high. During DLL re-lock period, ODT must remain LOW and CKE must remain HIGH. After the DLL lock time, the DRAM is ready to operate with new clock frequency. This process is depicted in Figure 16 on page 41.

4 DDR3 SDRAM Command Description and Operation (Cont'd)
4.7 Input clock frequency change (Cont'd)



NOTES: 1. Applicable for both SLOW EXIT and FAST EXIT Precharge Power-down
2. t_{AOFPD} and t_{AOF} must be statisfied and outputs High-Z prior to T1; refer to ODT timing section for exact requirements
3. If the RTT_NOM feature was enabled in the mode register prior to entering Precharge power down mode, the ODT signal must continuously be registered LOW ensuring RTT is in an off state, as shown in Figure 13. If the RTT_NOM feature was disabled in the mode register prior to entering Precharge power down mode, RTT will remain in the off state. The ODT signal can be registered either LOW or HIGH in this case.

Figure 16 — Change Frequency during Precharge Power-down

4.8 Write Leveling

For better signal integrity, the DDR3 memory module adopted fly-by topology for the commands, addresses, control signals, and clocks. The fly-by topology has benefits from reducing number of stubs and their length, but it also causes flight time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the Controller to maintain tDQSS, tDSS, and tDSH specification. Therefore, the DDR3 SDRAM supports a 'write leveling' feature to allow the controller to compensate for skew.

The memory controller can use the 'write leveling' feature and feedback from the DDR3 SDRAM to adjust the DQS - DQS# to CK - CK# relationship. The memory controller involved in the leveling must have adjustable delay setting on DQS - DQS# to align the rising edge of DQS - DQS# with that of the clock at the DRAM pin. The DRAM asynchronously feeds back CK - CK#, sampled with the rising edge of DQS - DQS#, through the DQ bus. The controller repeatedly delays DQS - DQS# until a transition from 0 to 1 is detected. The DQS - DQS# delay established though this exercise would ensure tDQSS specification. Besides tDQSS, tDSS and tDSH specification also needs to be fulfilled. One way to achieve this is to combine the actual tDQSS in the application with an appropriate duty cycle and jitter on the DQS - DQS# signals. Depending on the actual tDQSS in the application, the actual values for tDQSL and tDQSH may have to be better than the absolute limits provided in the chapter "AC Timing Parameters" in order to satisfy tDSS and tDSH specification. A conceptual timing of this scheme is shown in Figure 17.

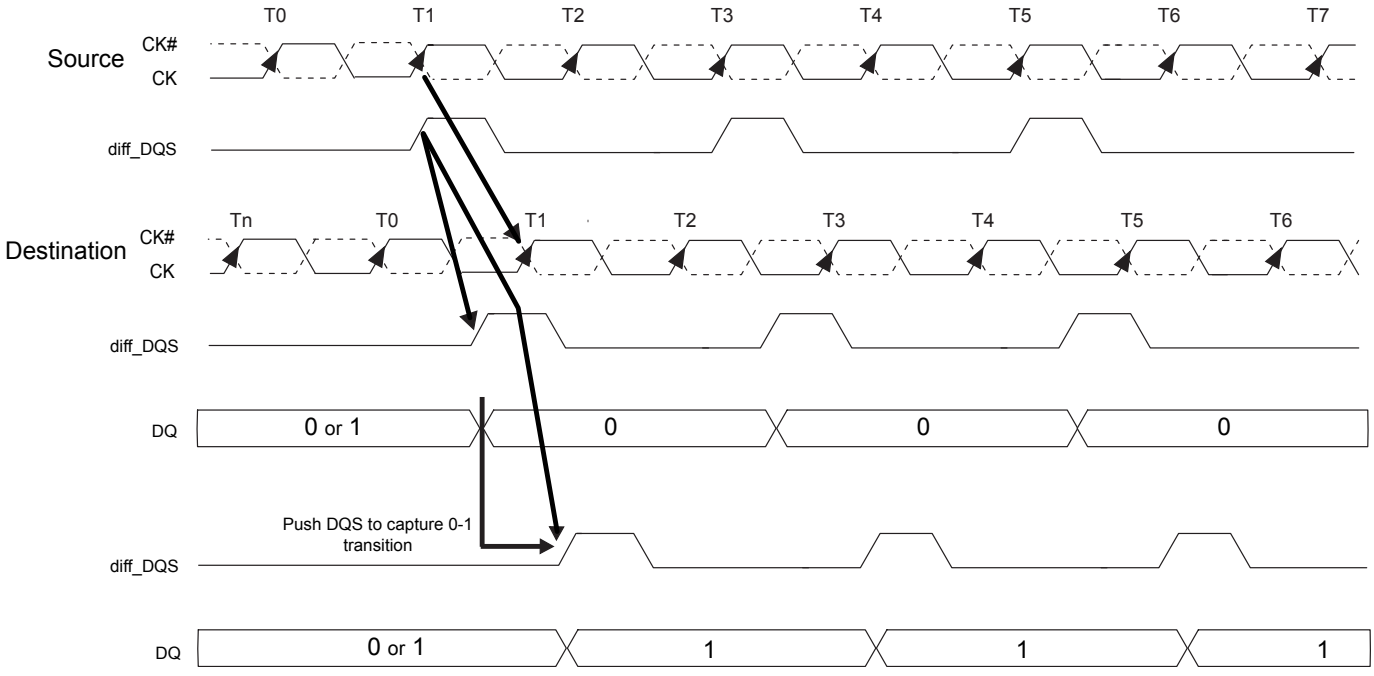


Figure 17 — Write Leveling Concept

DQS - DQS# driven by the controller during leveling mode must be terminated by the DRAM based on ranks populated. Similarly, the DQ bus driven by the DRAM must also be terminated at the controller.

One or more data bits should carry the leveling feedback to the controller across the DRAM configurations X4, X8, and X16. On a X16 device, both byte lanes should be leveled independently. Therefore, a separate feedback mechanism should be available for each byte lane. The upper data bits should provide the feedback of the upper diff_DQS(diff_UDQS) to clock relationship whereas the lower data bits would indicate the lower diff_DQS(diff_LDQS) to clock relationship.

4 DDR3 SDRAM Command Description and Operation (Cont'd)
4.8 Write Leveling (Cont'd)

4.8.1 DRAM setting for write leveling & DRAM termination function in that mode

DRAM enters into Write leveling mode if A7 in MR1 set 'High' and after finishing leveling, DRAM exits from write leveling mode if A7 in MR1 set 'Low' (Table 8). Note that in write leveling mode, only DQS/ DQS# terminations are activated and deactivated via ODT pin, unlike normal operation (Table 9).

Table 8 — MR setting involved in the leveling procedure

Function	MR1	Enable	Disable
Write leveling enable	A7	1	0
Output buffer mode (Qoff)	A12	0	1

Table 9 — DRAM termination function in the leveling mode

ODT pin @DRAM	DQS/DQS# termination	DQs termination
De-asserted	Off	Off
Asserted	On	Off

NOTE: In Write Leveling Mode with its output buffer disabled (MR1[bit7] = 1 with MR1[bit12] = 1) all RTT_Nom settings are allowed; in Write Leveling Mode with its output buffer enabled (MR1[bit7] = 1 with MR1[bit12] = 0) only RTT_Nom settings of RZQ/2, RZQ/4 and RZQ/6 are allowed.

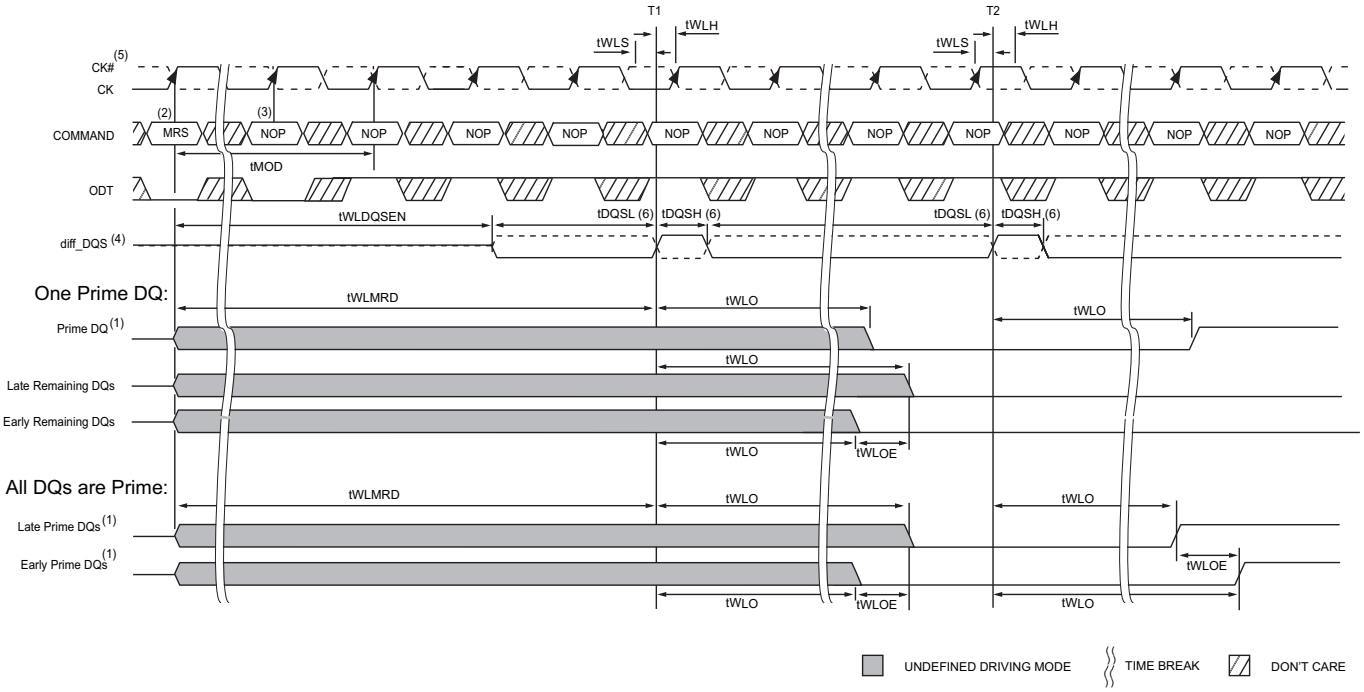
4.8.2 Procedure Description

The Memory controller initiates Leveling mode of all DRAMs by setting bit 7 of MR1 to 1. When entering write leveling mode, the DQ pins are in undefined driving mode. During write leveling mode, only NOP or DESELECT commands are allowed, as well as an MRS command to exit write leveling mode. Since the controller levels one rank at a time, the output of other ranks must be disabled by setting MR1 bit A12 to 1. The Controller may assert ODT after tMOD, at which time the DRAM is ready to accept the ODT signal.

The Controller may drive DQS low and DQS# high after a delay of tWLDQSEN, at which time the DRAM has applied on-die termination on these signals. After tDQSL and tWLMRD, the controller provides a single DQS, DQS# edge which is used by the DRAM to sample CK - CK# driven from controller. tWLMRD(max) timing is controller dependent.

DRAM samples CK - CK# status with rising edge of DQS - DQS# and provides feedback on all the DQ bits asynchronously after tWLO timing. Either one or all data bits ("prime DQ bit(s)") provide the leveling feedback. The DRAM's remaining DQ bits are driven Low statically after the first sampling procedure. There is a DQ output uncertainty of tWLOE defined to allow mismatch on DQ bits. The tWLOE period is defined from the transition of the earliest DQ bit to the corresponding transition of the latest DQ bit. There are no read strobes (DQS/DQS#) needed for these DQs. Controller samples incoming DQ and decides to increment or decrement DQS - DQS# delay setting and launches the next DQS/DQS# pulse after some time, which is controller dependent. Once a 0 to 1 transition is detected, the controller locks DQS - DQS# delay setting and write leveling is achieved for the device. Figure 18 describes the timing diagram and parameters for the overall Write Leveling procedure.

4.8 Write Leveling (Cont'd)
4.8.2 Procedure Description (Cont'd)



NOTES: 1. DRAM has the option to drive leveling feedback on a prime DQ or all DQs. If feedback is driven only on one DQ, the remaining DQs must be driven low, as shown in above Figure, and maintained at this state through out the leveling procedure.
2. MRS: Load MR1 to enter write leveling mode.
3. NOP: NOP or Deselect.
4. diff_DQS is the differential data strobe (DQS, DQS#). Timing reference points are the zero crossings. DQS is shown with solid line, DQS# is shown with dotted line.
5. CK, CK# : CK is shown with solid dark line, where as CK# is drawn with dotted line.
6. DQS, DQS# needs to fulfill minimum pulse width requirements tDQSH(min) and tDQSL(min) as defined for regular Writes; the max pulse width is system dependent.

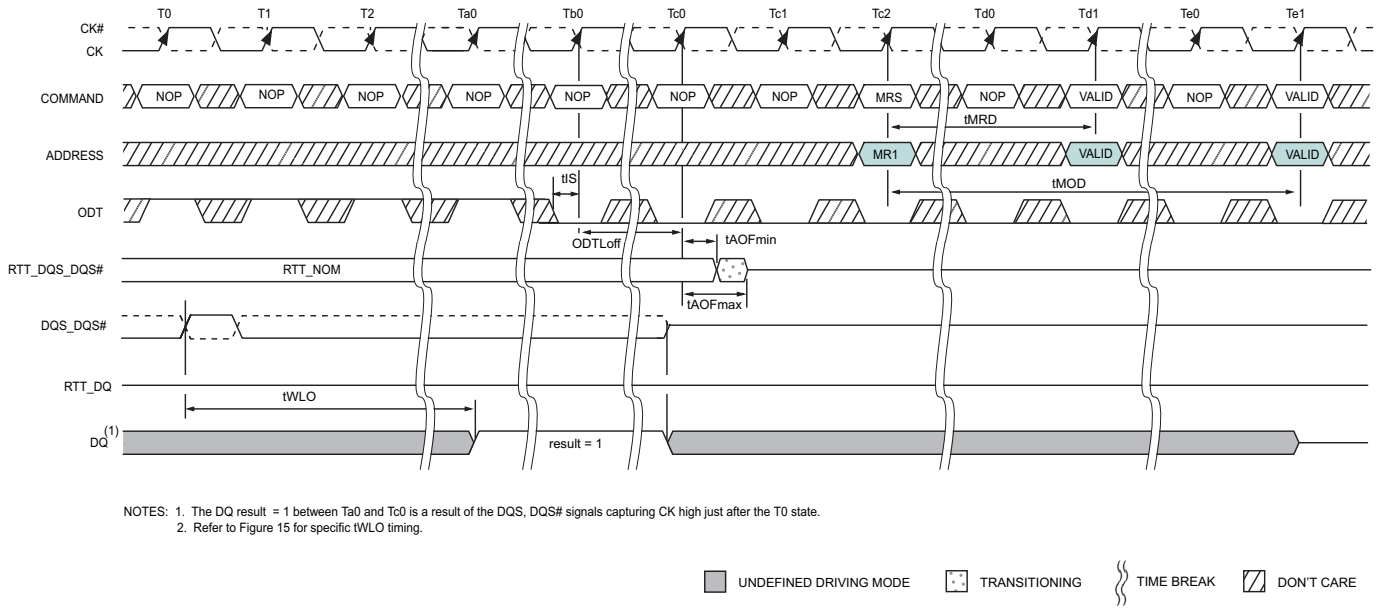
Figure 18 — Timing details of Write leveling sequence [DQS - DQS# is capturing CK - CK# low at T1 and CK - CK# high at T2

4 DDR3 SDRAM Command Description and Operation (Cont'd)
4.8 Write Leveling (Cont'd)

4.8.3 Write Leveling Mode Exit

The following sequence describes how the Write Leveling Mode should be exited:

1. After the last rising strobe edge (see ~T0), stop driving the strobe signals (see ~Tc0). Note: From now on, DQ pins are in undefined driving mode, and will remain undefined, until tMOD after the respective MR command (Te1).
2. Drive ODT pin low (tIS must be satisfied) and continue registering low. (see Tb0).
3. After the RTT is switched off, disable Write Level Mode via MRS command (see Tc2).
4. 4. After tMOD is satisfied (Te1), any valid command may be registered. (MR commands may be issued after tMRD (Td1).



NOTES: 1. The DQ result = 1 between Ta0 and Tc0 is a result of the DQS, DQS# signals capturing CK high just after the T0 state.
2. Refer to Figure 15 for specific tWLO timing.

Figure 19 — Timing details of Write leveling exit

4.9 Extended Temperature Usage

Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR3 SDRAM devices support the following options or requirements referred to in this material:

a. Auto Self-refresh supported

b. Extended Temperature Range supported

c. Double refresh required for operation in the Extended Temperature Range (applies only for devices supporting the Extended Temperature Range)

Table 10 — Mode Register Description

Field	Bits	Description
ASR	MR2 (A6)	**Auto Self-Refresh (ASR) (Optional)** when enabled, DDR3 SDRAM automatically provides Self-Refresh power management functions for all supported operating temperature values. If not enabled, the SRT bit must be programmed to indicate T_{OPER} during subsequent Self-Refresh operation 0 = Manual SR Reference (SRT) 1 = ASR enable (optional)
SRT	MR2 (A7)	**Self-Refresh Temperature (SRT) Range** If ASR = 0, the SRT bit must be programmed to indicate T_{OPER} during subsequent Self-Refresh operation If ASR = 1, SRT bit must be set to 0_b 0 = Normal operating temperature range 1 = Extended (optional) operating temperature range

4.9.0.1 Auto Self-Refresh mode - ASR Mode (optional)

DDR3 SDRAM provides an Auto Self-Refresh mode (ASR) for application ease. ASR mode is enabled by setting MR2 bit A6 = 1_b and MR2 bit A7 = 0_b. The DRAM will manage Self-Refresh entry in either the Normal or Extended (optional) Temperature Ranges. In this mode, the DRAM will also manage Self-Refresh power consumption when the DRAM operating temperature changes, lower at low temperatures and higher at high temperatures.

If the ASR option is not supported by the DRAM, MR2 bit A6 must be set to 0_b.

If the ASR mode is not enabled (MR2 bit.A6 = 0_b), the SRT bit (MR2 A7) must be manually programmed with the operating temperature range required during Self-Refresh operation.

Support of the ASR option does not automatically imply support of the Extended Temperature Range.

Please refer to the supplier data sheet and/or the DIMM SPD for Extended Temperature Range and Auto Self-Refresh option availability.

4.9.1 Self-Refresh Temperature Range - SRT

SRT applies to devices supporting Extended Temperature Range only. If ASR = 0_b, the Self-Refresh Temperature (SRT) Range bit must be programmed to guarantee proper self-refresh operation. If SRT = 0_b, then the DRAM will set an appropriate refresh rate for Self-Refresh operation in the Normal Temperature Range. If SRT = 1_b then the DRAM will set an appropriate, potentially different, refresh rate to allow Self-Refresh operation in either the Normal or Extended Temperature Ranges. The value of the SRT bit can effect self-refresh power consumption, please refer to the IDD table for details.

For parts that do not support the Extended Temperature Range, MR2 bit A7 must be set to 0_b and the DRAM should not be operated outside the Normal Temperature Range.

4 DDR3 SDRAM Command Description and Operation (Cont'd)
4.9 Extended Temperature Usage (Cont'd)

Please refer to the supplier data sheet and/or the DIMM SPD for Extended Temperature Range availability.

Table 11 — Self-Refresh mode summary

MR2 A[6]	MR2 A[7]	Self-Refresh operation	Allowed Operating Temperature Range for Self-Refresh Mode
0	0	Self-refresh rate appropriate for the Normal Temperature Range	Normal (0 - 85 ^{o}C)
0	1	Self-refresh rate appropriate for either the Normal or Extended Temperature Ranges. The DRAM must support Extended Temperature Range. The value of the SRT bit can effect self-refresh power consumption, please refer to the IDD table for details.	Normal and Extended (0 - 95 ^{o}C)
1	0	ASR enabled (for devices supporting ASR and Normal Temperature Range). Self-Refresh power consumption is temperature dependent	Normal (0 - 85 ^{o}C)
1	0	ASR enabled (for devices supporting ASR and Extended Temperature Range). Self-Refresh power consumption is temperature dependent	Normal and Extended (0 - 95 ^{o}C)
1	1	Illegal	

4.10 Multi Purpose Register

The Multi Purpose Register (MPR) function is used to Read out a predefined system timing calibration bit sequence. The basic concept of the MPR is shown in Figure 20.

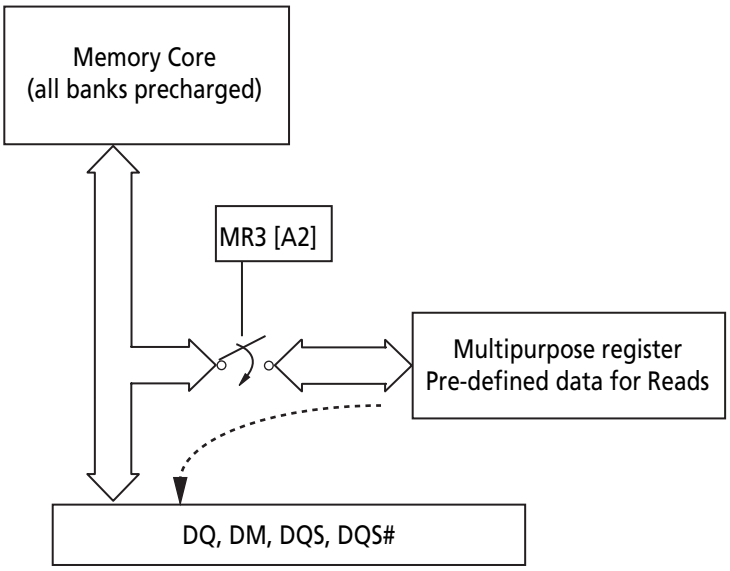


Figure 20 — MPR Block Diagram

To enable the MPR, a MODE Register Set (MRS) command must be issued to MR3 Register with bit A2 = 1, as shown in Table 12. Prior to issuing the MRS command, all banks must be in the idle state (all banks precharged and tRP met). Once the MPR is enabled, any subsequent RD or RDA commands will be redirected to the Multi Purpose Register. The resulting operation, when a RD or RDA command is issued, is defined by MR3 bits A[1:0] when the MPR is enabled as shown in Table 13. When the MPR is enabled, only RD or RDA commands are allowed until a subsequent MRS command is issued with the MPR disabled (MR3 bit A2 = 0). Note that in MPR mode RDA has the same functionality as a READ command which means the auto precharge part of RDA is ignored. Power-Down mode, Self-Refresh, and any other non-RD/RDA command is not allowed during MPR enable mode. The RESET function is supported during MPR enable mode.

Table 12 — MPR MR3 Register Definition

MR3 A[2]	MR3 A[1:0]	Function
MPR	MPR-Loc	
0b	don't care (0b or 1b)	Normal operation, no MPR transaction. All subsequent Reads will come from DRAM array. All subsequent Write will go to DRAM array.
1b	See Table 13	Enable MPR mode, subsequent RD/RDA commands defined by MR3 A[1:0].

4 DDR3 SDRAM Command Description and Operation (Cont'd)
4.10 Multi Purpose Register (Cont'd)

4.10.1 MPR Functional Description

- One bit wide logical interface via all DQ pins during READ operation.
- Register Read on x4:
  - DQ[0] drives information from MPR.
  - DQ[3:1] either drive the same information as DQ[0], or they drive 0b.
- Register Read on x8:
  - DQ[0] drives information from MPR.
  - DQ[7:1] either drive the same information as DQ[0], or they drive 0b.
- Register Read on x16:
  - DQL[0] and DQU[0] drive information from MPR.
  - DQL[7:1] and DQU[7:1] either drive the same information as DQL[0], or they drive 0b.
- Addressing during for Multi Purpose Register reads for all MPR agents:
  - BA[2:0]: don't care
  - A[1:0]: A[1:0] must be equal to '00'b. Data read burst order in nibble is fixed
  - A[2]: For BL=8, A[2] must be equal to 0b, burst order is fixed to [0,1,2,3,4,5,6,7], *) For Burst Chop 4 cases, the burst order is switched on nibble base A[2]=0b, Burst order: 0,1,2,3 *) A[2]=1b, Burst order: 4,5,6,7 *)
  - A[9:3]: don't care
  - A10/AP: don't care
  - A12/BC: Selects burst chop mode on-the-fly, if enabled within MR0.
  - A11, A13,... (if available): don't care
- Regular interface functionality during register reads:
  - Support two Burst Ordering which are switched with A2 and A[1:0]=00b.
  - Support of read burst chop (MRS and on-the-fly via A12/BC)
  - All other address bits (remaining column address bits including A10, all bank address bits) will be ignored by the DDR3 SDRAM.
  - Regular read latencies and AC timings apply.
  - DLL must be locked prior to MPR Reads.

NOTE: *) Burst order bit 0 is assigned to LSB and burst order bit 7 is assigned to MSB of the selected MPR agent.

4 DDR3 SDRAM Command Description and Operation (Cont'd)
4.10 Multi Purpose Register (Cont'd)

4.10.2 MPR Register Address Definition

Table 13 provides an overview of the available data locations, how they are addressed by MR3 A[1:0] during a MRS to MR3, and how their individual bits are mapped into the burst order bits during a Multi Purpose Register Read.

Table 13 — MPR MR3 Register Definition

MR3 A[2]	MR3 A[1:0]	Function	Burst Length	Read Address A[2:0]	Burst Order and Data Pattern
1b	00b	Read Predefined Pattern for System Calibration	BL8	000b	Burst order 0,1,2,3,4,5,6,7 Pre-defined Data Pattern [0,1,0,1,0,1,0,1]
			BC4	000b	Burst order 0,1,2,3 Pre-defined Data Pattern [0,1,0,1]
			BC4	100b	Burst order 4,5,6,7 Pre-defined Data Pattern [0,1,0,1]
1b	01b	RFU	BL8	000b	Burst order 0,1,2,3,4,5,6,7
			BC4	000b	Burst order 0,1,2,3
			BC4	100b	Burst order 4,5,6,7
1b	10b	RFU	BL8	000b	Burst order 0,1,2,3,4,5,6,7
			BC4	000b	Burst order 0,1,2,3
			BC4	100b	Burst order 4,5,6,7
1b	11b	RFU	BL8	000b	Burst order 0,1,2,3,4,5,6,7
			BC4	000b	Burst order 0,1,2,3
			BC4	100b	Burst order 4,5,6,7
NOTE: Burst order bit 0 is assigned to LSB and the burst order bit 7 is assigned to MSB of the selected MPR agent.					

4.10.3 Relevant Timing Parameters

The following AC timing parameters are important for operating the Multi Purpose Register: tRP, tMRD, tMOD, and tMPRR. For more details refer to "Electrical Characteristics & AC Timing for DDR3-800 to DDR3-1600" on page 155.

4.10.4 Protocol Example

Protocol Example (This is one example):

Read out predetermined read-calibration pattern.

Description: Multiple reads from Multi Purpose Register, in order to do system level read timing calibration based on predetermined and standardized pattern.

Protocol Steps:

- Precharge All.
- Wait until tRP is satisfied.
- MRS MR3, Opcode "A2 = 1b" and "A[1:0] = 00b"
  - Redirect all subsequent reads into the Multi Purpose Register, and load Pre-defined pattern into MPR.
- Wait until tMRD and tMOD are satisfied (Multi Purpose Register is then ready to be read). During the period MR3 A2 =1, no data write operation is allowed.
- Read:
  - A[1:0] = '00'b (Data burst order is fixed starting at nibble, always 00b here)
  - A[2] = '0'b (For BL=8, burst order is fixed as 0,1,2,3,4,5,6,7)
  - A12/BC = 1 (use regular burst length of 8)
  - All other address pins (including BA[2:0] and A10/AP): don't care

- After RL = AL + CL, DRAM bursts out the predefined Read Calibration Pattern.
- Memory controller repeats these calibration reads until read data capture at memory controller is optimized.
- After end of last MPR read burst, wait until tMPRR is satisfied.
- MRS MR3, Opcode "A2 = 0b" and "A[1:0] = valid data but value are don't care"
  - All subsequent read and write accesses will be regular reads and writes from/to the DRAM array.
- Wait until tMRD and tMOD are satisfied.
- Continue with "regular" DRAM commands, like activate a memory bank for regular read or write access,...

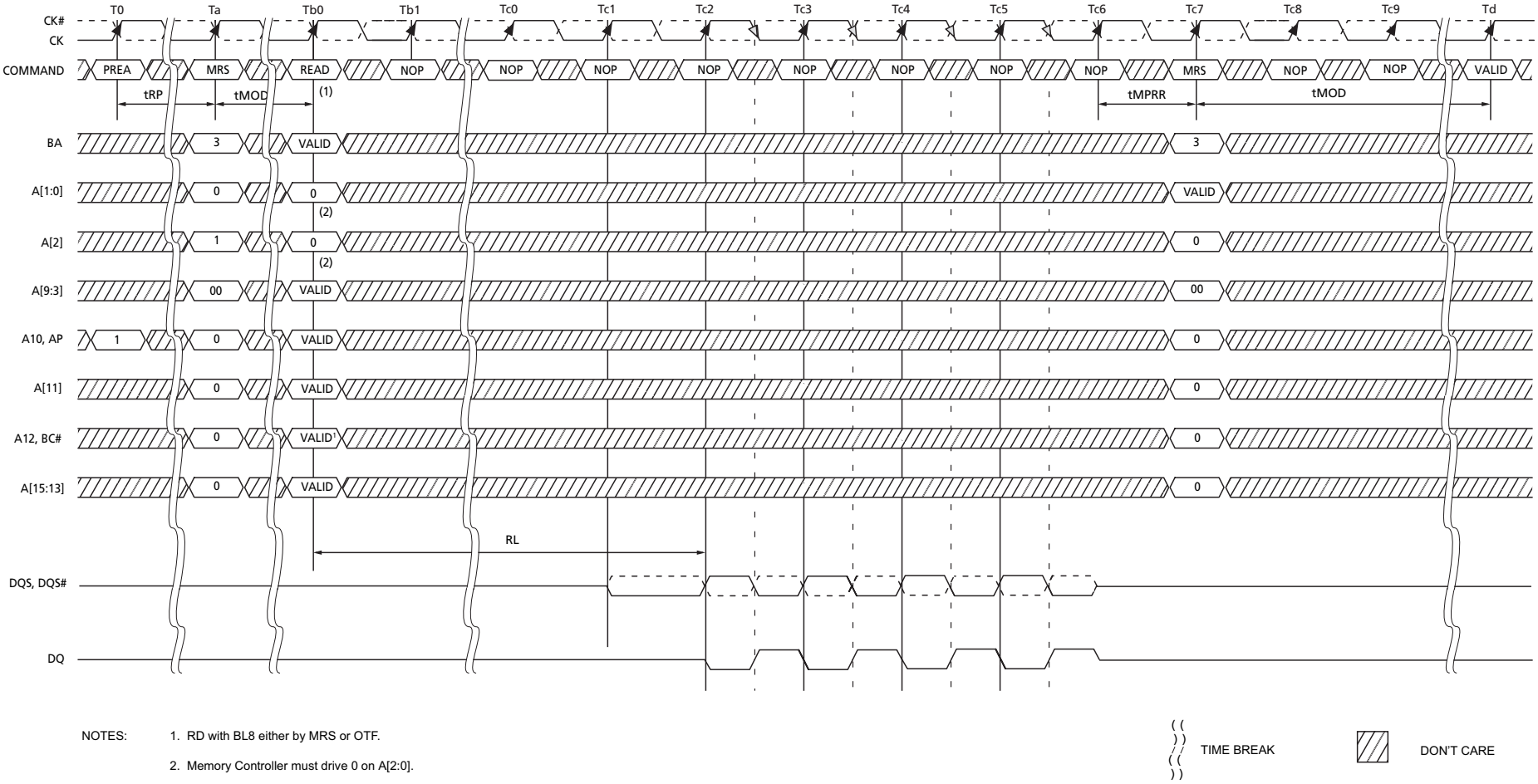


Figure 21 — MPR Readout of predefined pattern, BL8 fixed burst order, single readout

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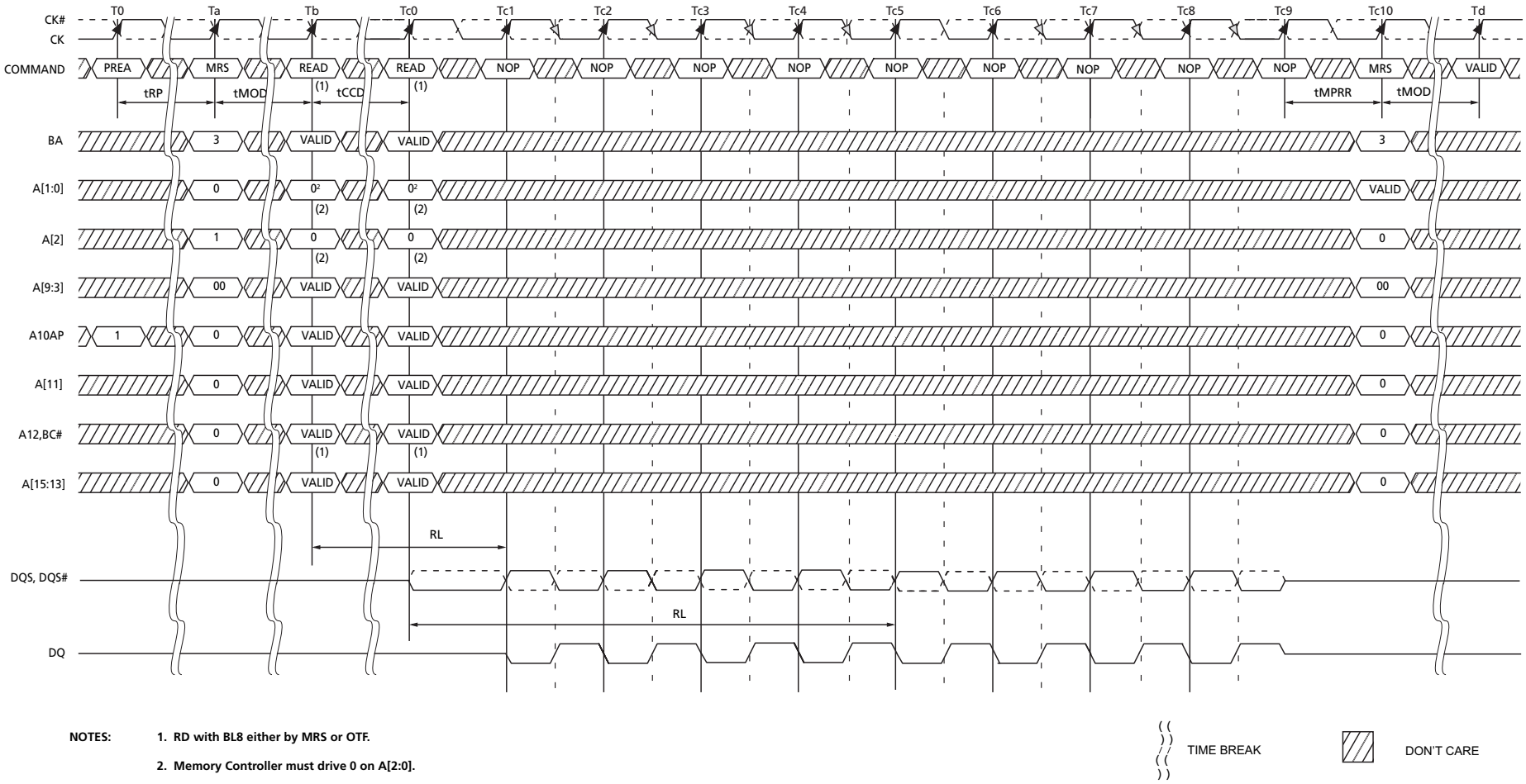
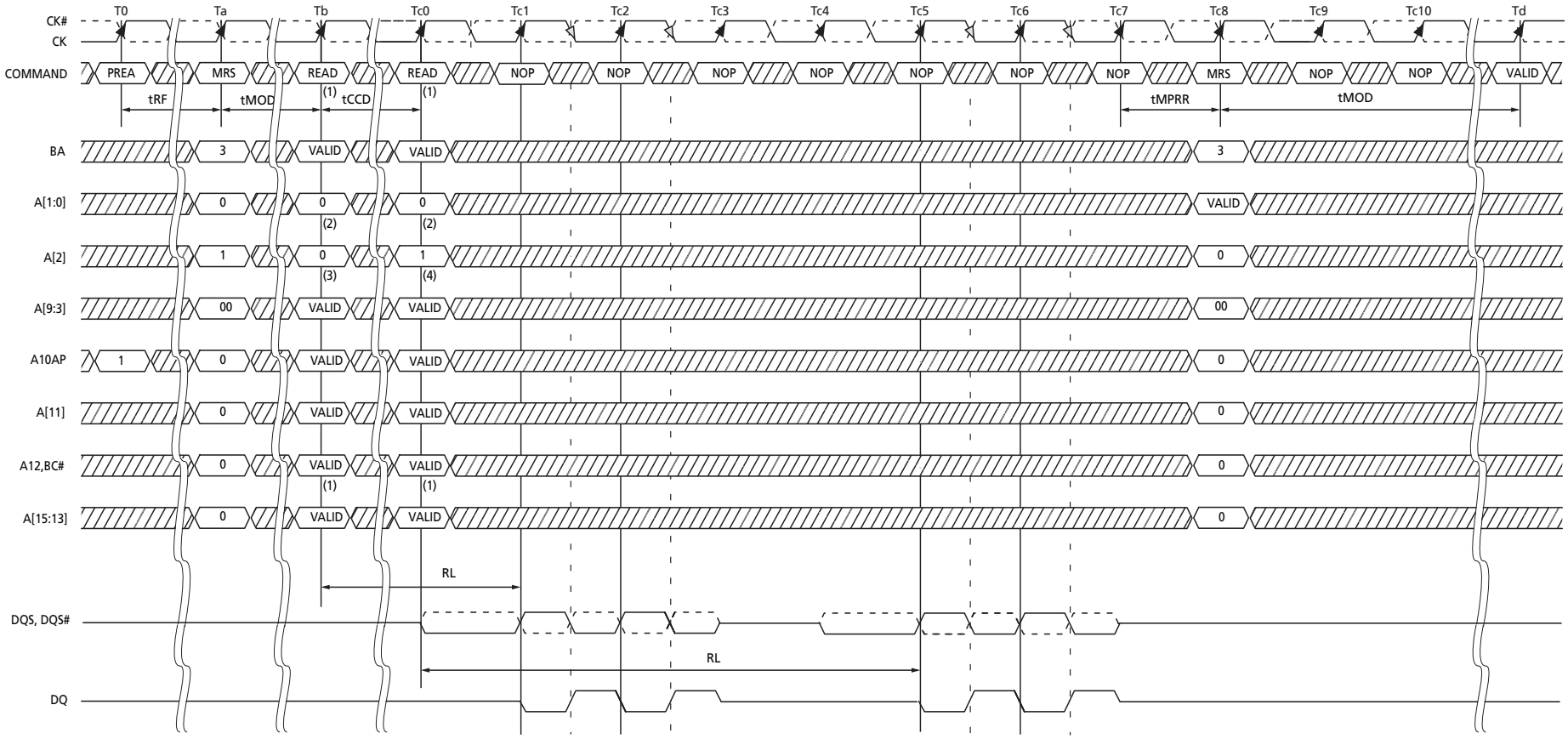


NOTES:
1. RD with BL8 either by MRS or OTF.
2. Memory Controller must drive 0 on A[2:0].

Figure 22 — MPR Readout of predefined pattern, BL8 fixed burst order, back-to-back readout



NOTES:
1. RD with BC4 either by MRS or OTF.
2. Memory Controller must drive 0 on A[1:0].
3. A[2]=0 selects lower 4 nibble bits 0....3.
4. A[2]=1 selects upper 4 nibble bits 4....7.

TIME BREAK

DON'T CARE

Figure 23 — MPR Readout predefined pattern, BC4, lower nibble then upper nibble

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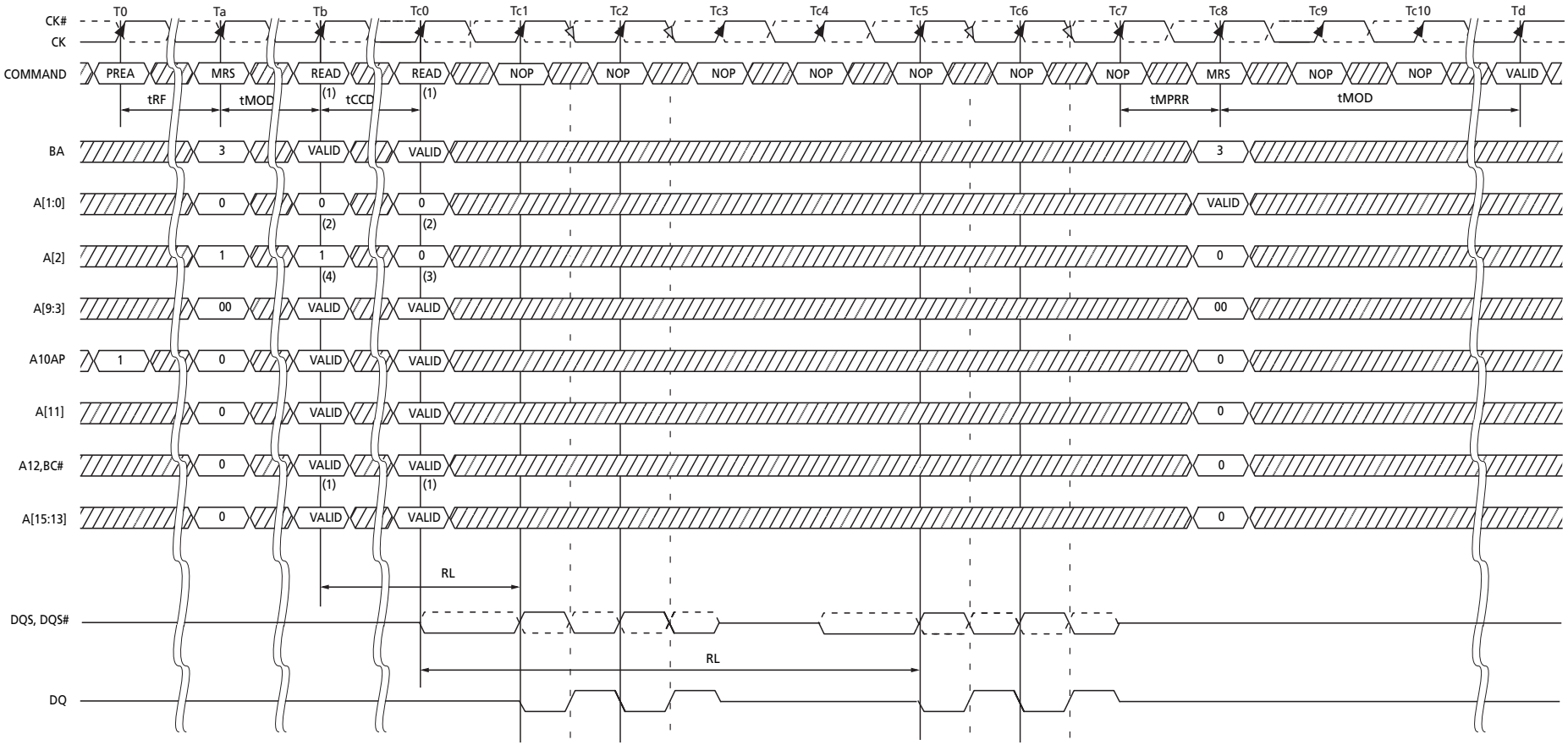


NOTES:
1. RD with BC4 either by MRS or OTF.
2. Memory Controller must drive 0 on A[1:0].
3. A[2]=0 selects lower 4 nibble bits 0....3.
4. A[2]=1 selects upper 4 nibble bits 4....7.

Figure 24 — MPR Readout of predefined pattern, BC4, upper nibble then lower nibble

4.11 ACTIVE Command

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0-BA2 inputs selects the bank, and the address provided on inputs A0-A15 selects the row. This row remains active (or open) for accesses until a precharge command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

4.12 PRECHARGE Command

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row activation a specified time (tRP) after the PRECHARGE command is issued, except in the case of concurrent auto precharge, where a READ or WRITE command to a different bank is allowed as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters. Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command is allowed if there is no open row in that bank (idle state) or if the previously open row is already in the process of precharging. However, the precharge period will be determined by the last PRECHARGE command issued to the bank.

4 DDR3 SDRAM Command Description and Operation (Cont'd)

4.13 READ Operation

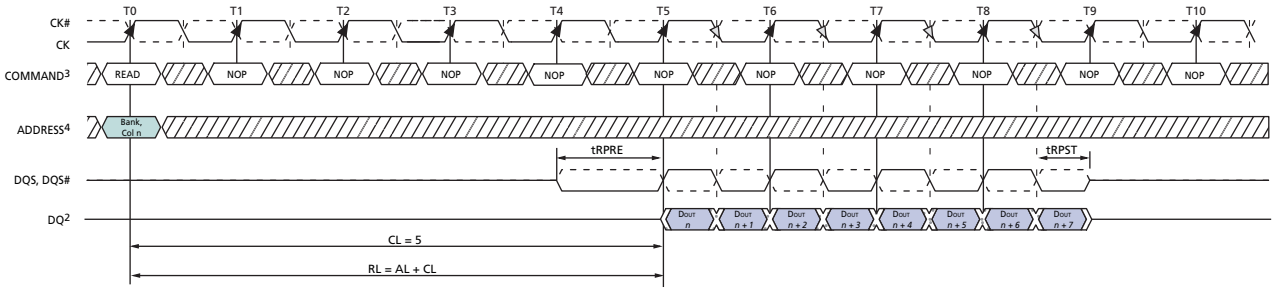
4.13.1 READ Burst Operation

During a READ or WRITE command, DDR3 will support BC4 and BL8 on the fly using address A12 during the READ or WRITE (AUTO PRECHARGE can be enabled or disabled).

A12 = 0, BC4 (BC4 = burst chop, tCCD = 4)

A12 = 1, BL8

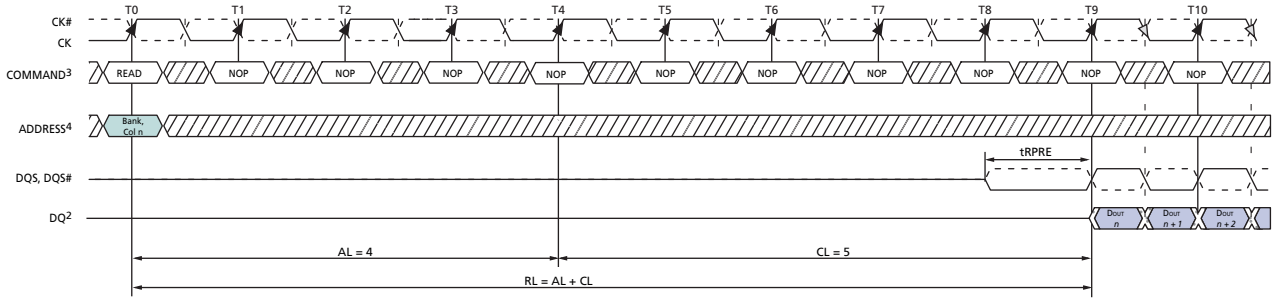
A12 is used only for burst length control, not as a column address.



NOTES: 1. BL8, RL = 5, AL = 0, CL = 5.
2. DOUT *n* = data-out from column *n*.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ command at T0.

TRANSITIONING DATA DON'T CARE

Figure 25 — READ Burst Operation RL = 5 (AL = 0, CL = 5, BL8)



NOTES: 1. BL8, RL = 9, AL = (CL - 1), CL = 5.
2. DOUT *n* = data-out from column *n*.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ command at T0.

TRANSITIONING DATA DON'T CARE

Figure 26 — READ Burst Operation RL = 9 (AL = 4, CL = 5, BL8)

4 DDR3 SDRAM Command Description and Operation (Cont'd)
4.13 READ Operation (Cont'd)

4.13.2 READ Timing Definitions

Read timing is shown in Figure 27 and is applied when the DLL is enabled and locked.

Rising data strobe edge parameters:

- tDQSCK min/max describes the allowed range for a rising data strobe edge relative to CK, CK#.
- tDQSCK is the actual position of a rising strobe edge relative to CK, CK#.
- tQSH describes the DQS, DQS# differential output high time.
- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.

Falling data strobe edge parameters:

- tQSL describes the DQS, DQS# differential output low time.
- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.

tDQSQ; both rising/falling edges of DQS, no tAC defined.

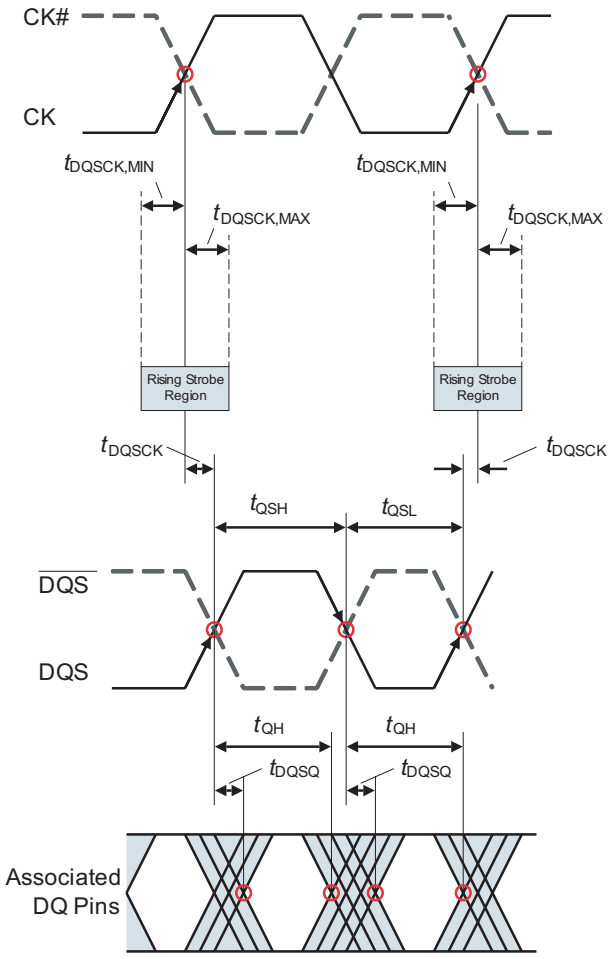


Figure 27 — READ Timing Definition

4.13 READ Operation (Cont'd)
4.13.2 READ Timing Definitions (Cont'd)

4.13.2.1 READ Timing; Clock to Data Strobe relationship

Clock to Data Strobe relationship is shown in Figure 28 and is applied when the DLL is enabled and locked.

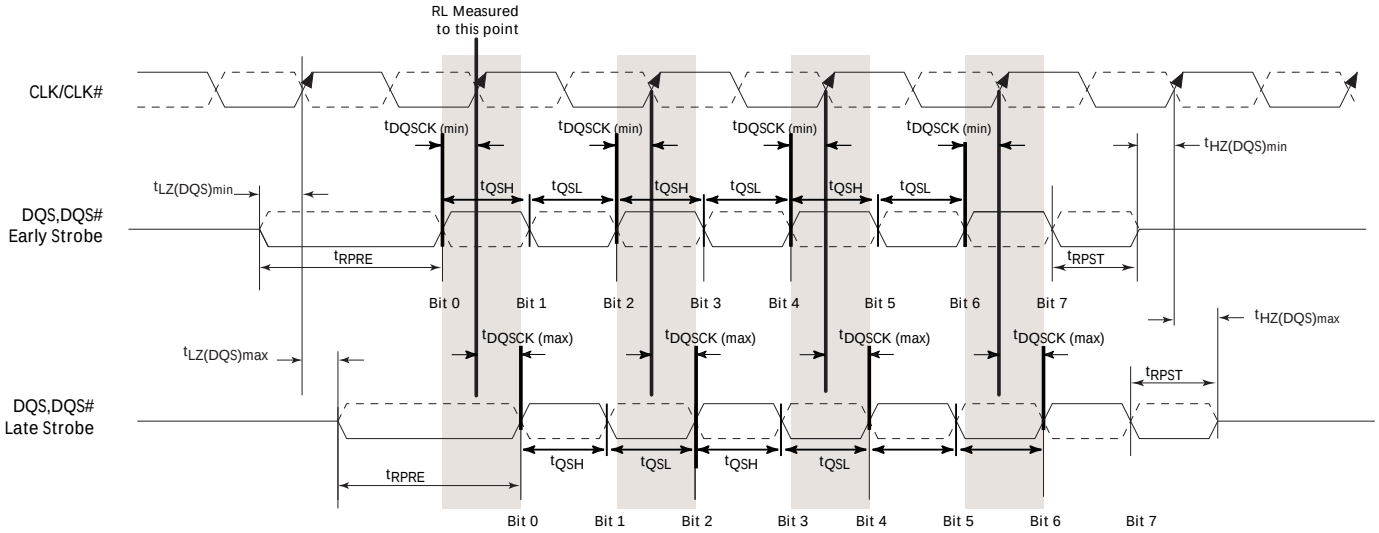
Rising data strobe edge parameters:

- tDQSCK min/max describes the allowed range for a rising data strobe edge relative to CK, CK#.
- tDQSCK is the actual position of a rising strobe edge relative to CK, CK#.
- tQSH describes the data strobe high pulse width.

Falling data strobe edge parameters:

- tQSL describes the data strobe low pulse width.

tLZ(DQS), tHZ(DQS) for preamble/postamble (see 4.13.2.3 and Figure 30)



NOTES:
1. Within a burst, rising strobe edge is not necessarily fixed to be always at tDQSCK(min) or tDQSCK(max). Instead, rising strobe edge can vary between tDQSCK(min) and tDQSCK(max).
2. The DQS, DQS# differential output high time is defined by tQSH and the DQS, DQS# differential output low time is defined by tQSL.
3. Likewise, tLZ(DQS)min and tHZ(DQS)min are not tied to tDQSCKmin (early strobe case) and tLZ(DQS)max and tHZ(DQS)max are not tied to tDQSCKmax (late strobe case).
4. The minimum pulse width of read preamble is defined by tRPRE(min).
5. The maximum read postamble is bound by tDQSCK(min) plus tQSH(min) on the left side and tHZDSQ(max) on the right side.
6. The minimum pulse width of read postamble is defined by tRPST(min).
7. The maximum read preamble is bound by tLZDQS(min) on the left side and tDQSCK(max) on the right side.

Figure 28 — Clock to Data Strobe Relationship

4.13 READ Operation (Cont'd)
4.13.2 READ Timing Definitions (Cont'd)

4.13.2.2 READ Timing; Data Strobe to Data relationship

The Data Strobe to Data relationship is shown in Figure 29 and is applied when the DLL is enabled and locked.

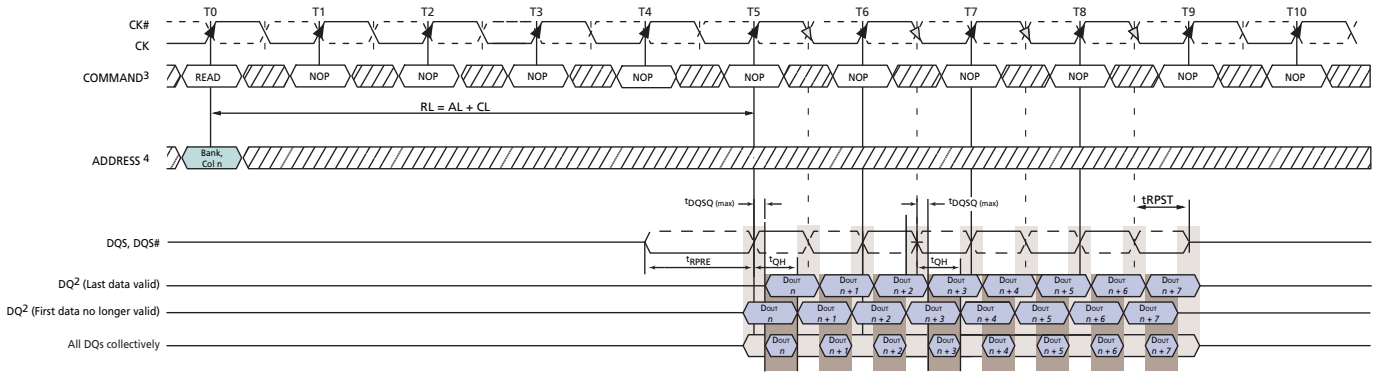
Rising data strobe edge parameters:

- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.

Falling data strobe edge parameters:

- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.

tDQSQ; both rising/falling edges of DQS, no tAC defined



NOTES: 1. BL = 8, RL = 5 (AL = 0, CL = 5)
2. DOUT *n* = data-out from column *n*.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ command at T0.
5. Output timings are referenced to VDDQ/2, and DLL on for locking.
6. tDQSQ defines the skew between DQS,DQS# to Data and does not define DQS,DQS# to Clock.
7. Early Data transitions may not always happen at the same DQ. Data transitions of a DQ can vary (either early or late) within a burst.

TRANSITIONING DATA DON'T CARE

Figure 29 — Data Strobe to Data Relationship

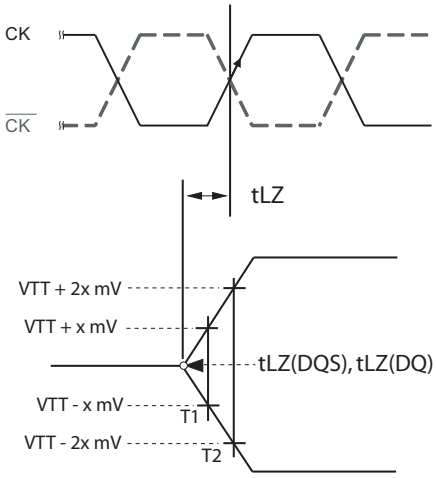
4.13.2.3 tLZ(DQS), tLZ(DQ), tHZ(DQS), tHZ(DQ) Calculation

tHZ and tLZ transitions occur in the same time window as valid data transitions. These parameters are referenced to a specific voltage level that specifies when the device output is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ). Figure 30 shows a method to calculate the point when the device is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ), by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent. The parameters tLZ(DQS), tLZ(DQ), tHZ(DQS), and tHZ(DQ) are defined as singled ended.

4.13 READ Operation (Cont'd)
4.13.2 READ Timing Definitions (Cont'd)

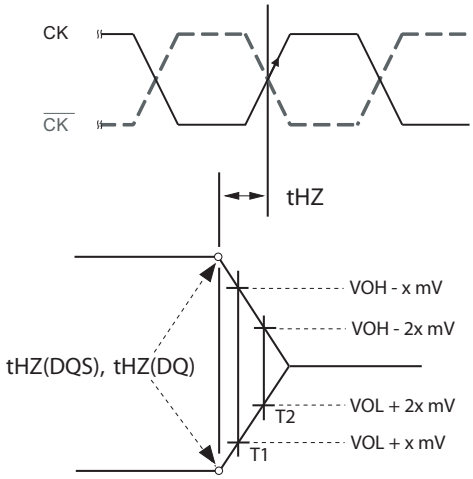
.

tLZ(DQS): CK - CK# rising crossing at RL - 1
tLZ(DQ): CK - CK# rising crossing at RL



tLZ(DQS), tLZ(DQ) begin point = 2 * T1 - T2

tHZ(DQS), tHZ(DQ) with BL8: CK - CK# rising crossing at RL + 4 nCK
tHZ(DQS), tHZ(DQ) with BC4: CK - CK# rising crossing at RL + 2 nCK



tHZ(DQS), tHZ(DQ) end point = 2 * T1 - T2

Figure 30 — tLZ and tHZ method for calculating transitions and endpoints

4.13 READ Operation (Cont'd)
4.13.2 READ Timing Definitions (Cont'd)

4.13.2.4 tRPRE Calculation

The method for calculating differential pulse widths for tRPRE is shown in Figure 31.

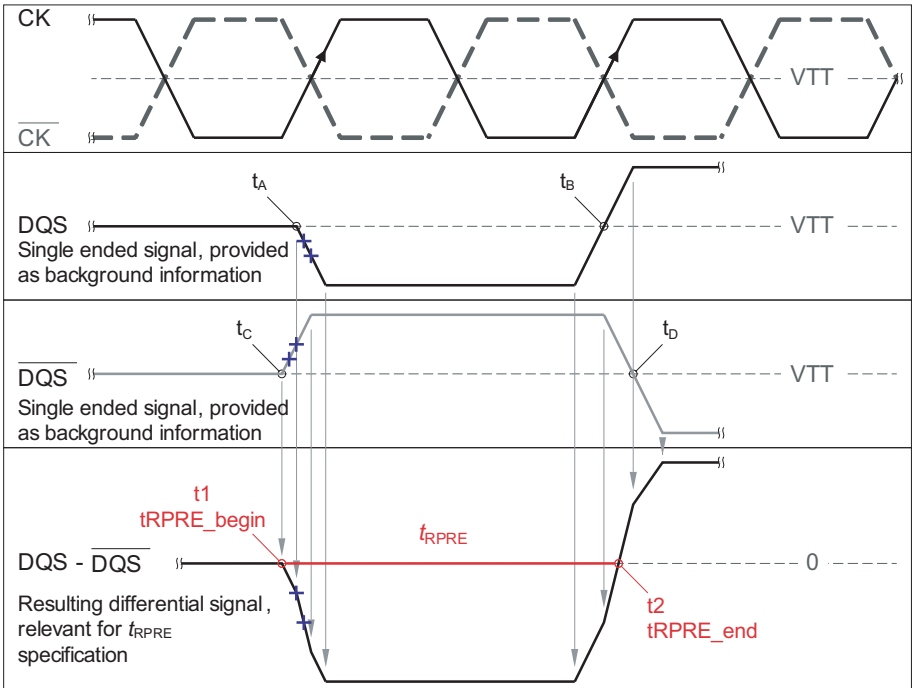


Figure 31 — Method for calculating tRPRE transitions and endpoints

4.13.2.5 tRPST Calculation

The method for calculating differential pulse widths for tRPST is shown in Figure 32.

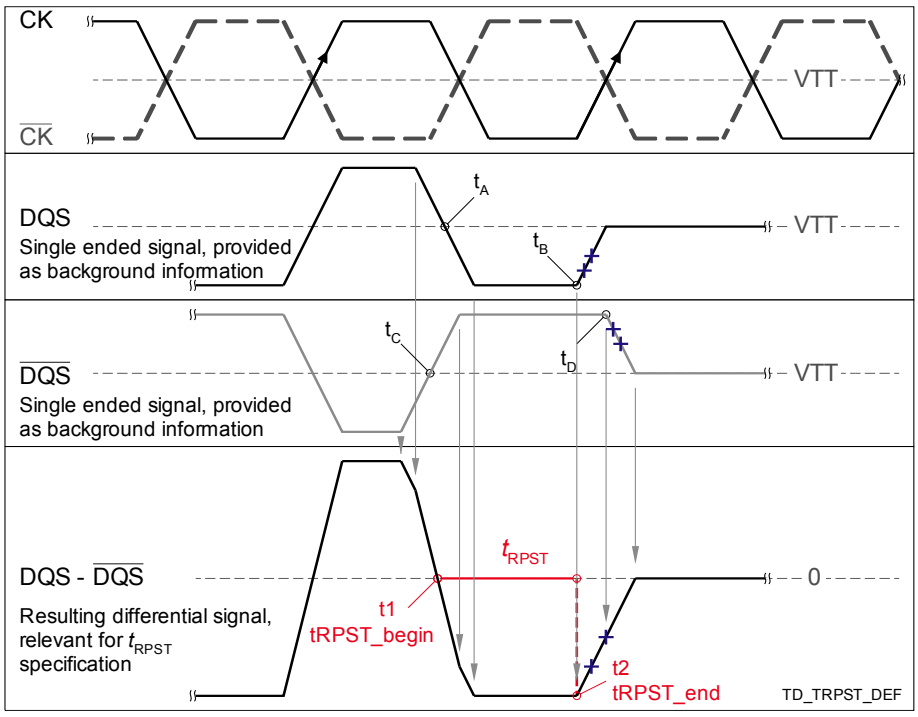
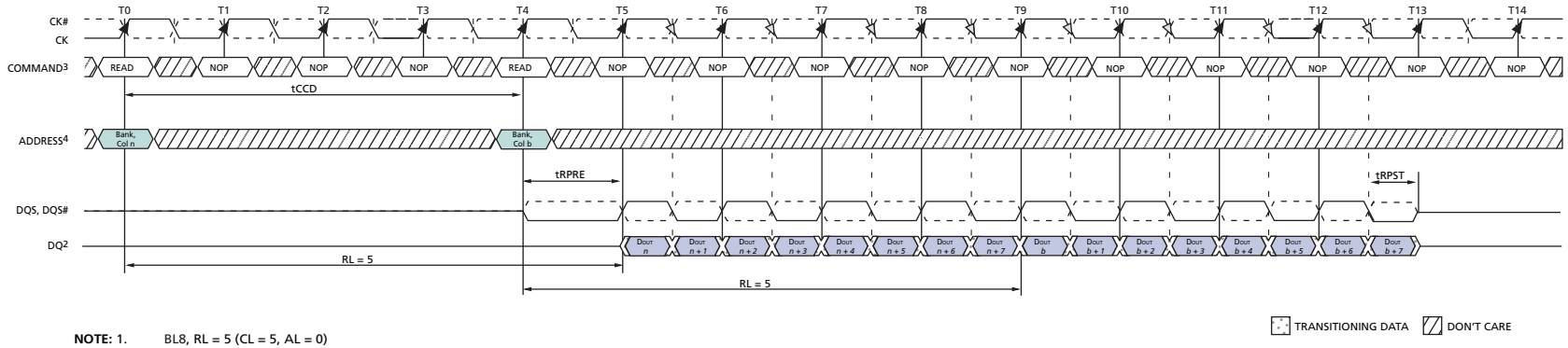
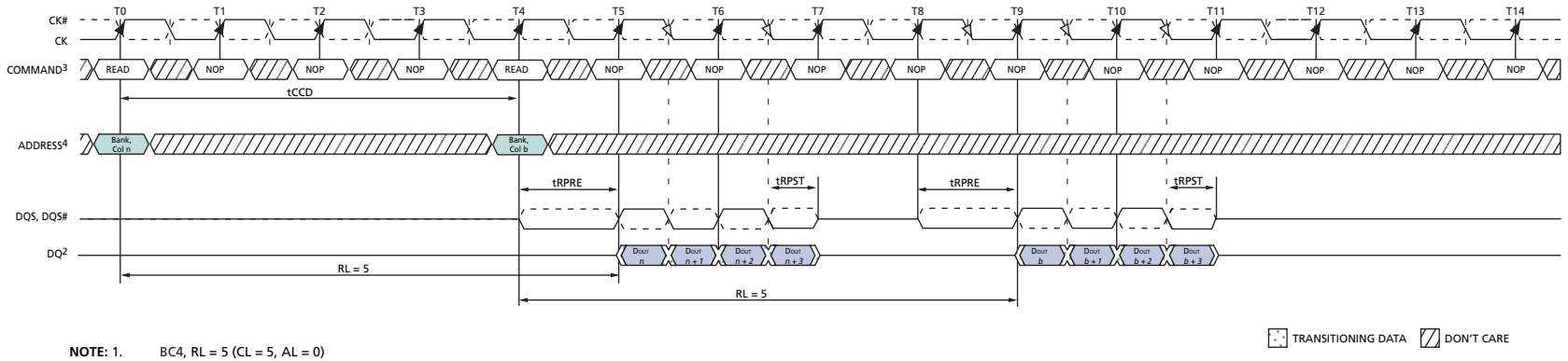


Figure 32 — Method for calculating tRPST transitions and endpoints



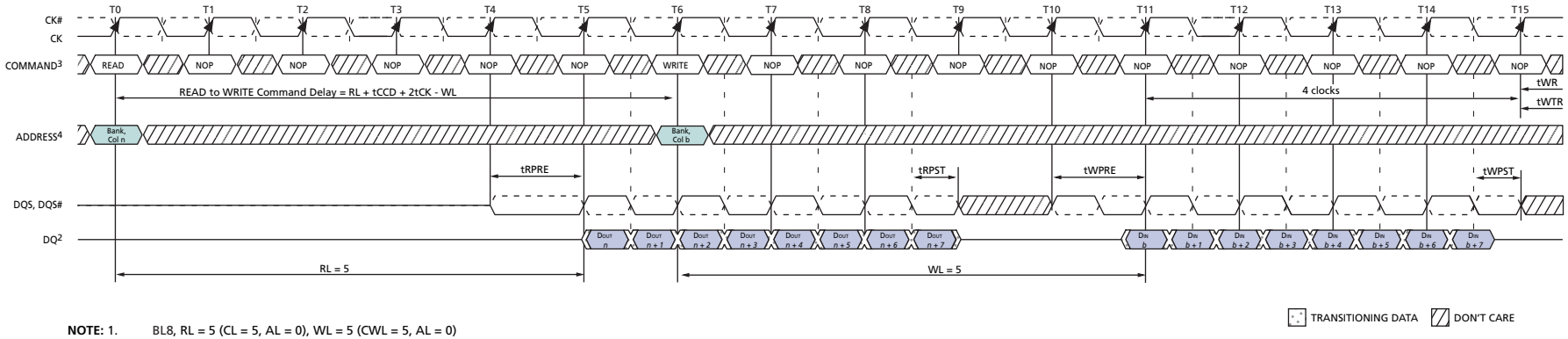
NOTE: 1. BL8, RL = 5 (CL = 5, AL = 0)
2. DOUT *n (or b)* = data-out from column *n (or column b)*.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ commands at T0 and T4.

Figure 33 — READ (BL8) to READ (BL8)



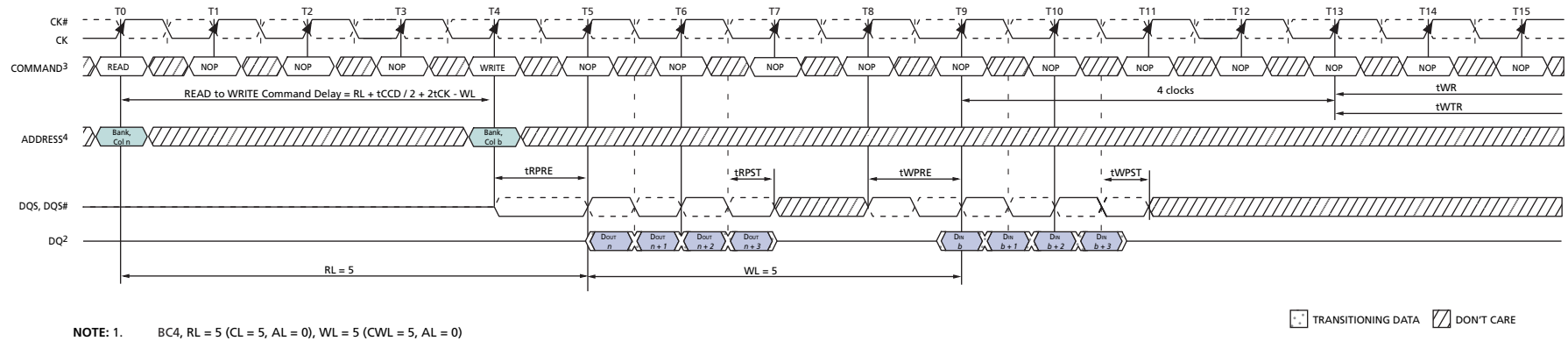
NOTE: 1. BC4, RL = 5 (CL = 5, AL = 0)
2. DOUT *n (or b)* = data-out from column *n (or column b)*.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by either MR0[A1:0 = 10] or MR0[A1:0 = 01] and A12 = 0 during READ commands at T0 and T4.

Figure 34 — READ (BC4) to READ (BC4)



NOTE: 1. BL8, RL = 5 (CL = 5, AL = 0), WL = 5 (CWL = 5, AL = 0)
2. DOUT *n* = data-out from column, DIN *b* = data-in from column *b*.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ command at T0 and WRITE command at T6.

Figure 35 — READ (BL8) to WRITE (BL8)



NOTE: 1. BC4, RL = 5 (CL = 5, AL = 0), WL = 5 (CWL = 5, AL = 0)
2. DOUT *n* = data-out from column, DIN *b* = data-in from column *b*.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:0 = 01] and A12 = 0 during READ command at T0 and WRITE command at T4.

Figure 36 — READ (BC4) to WRITE (BC4) OTF

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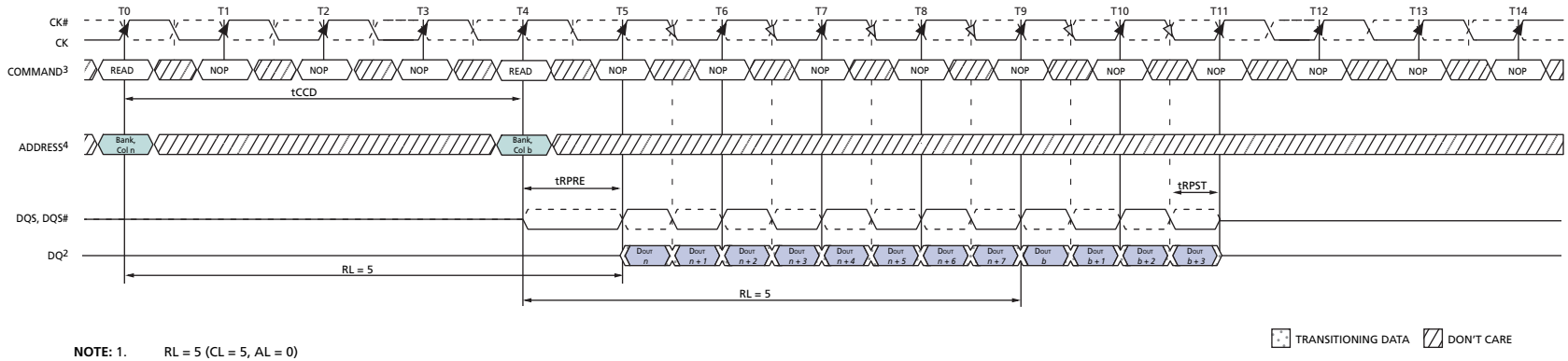
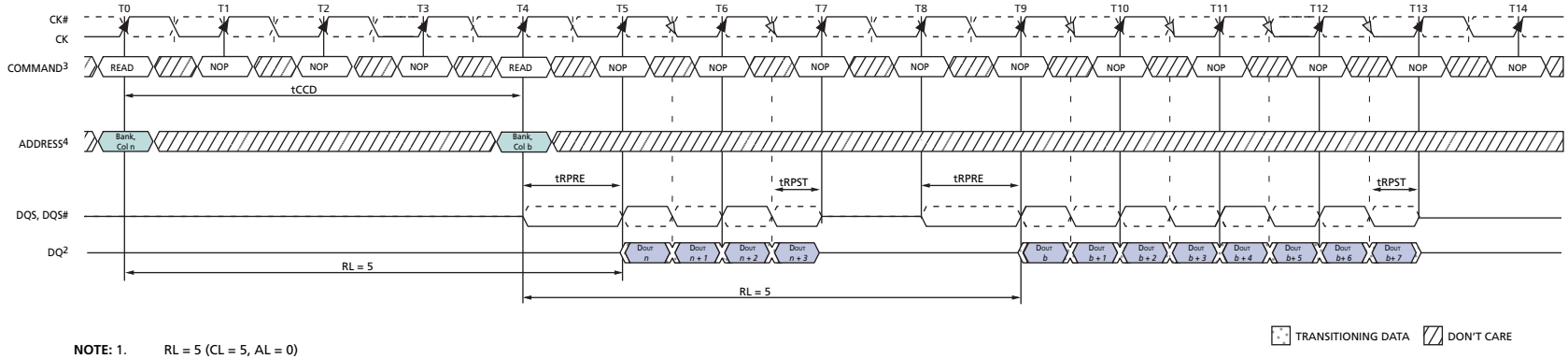


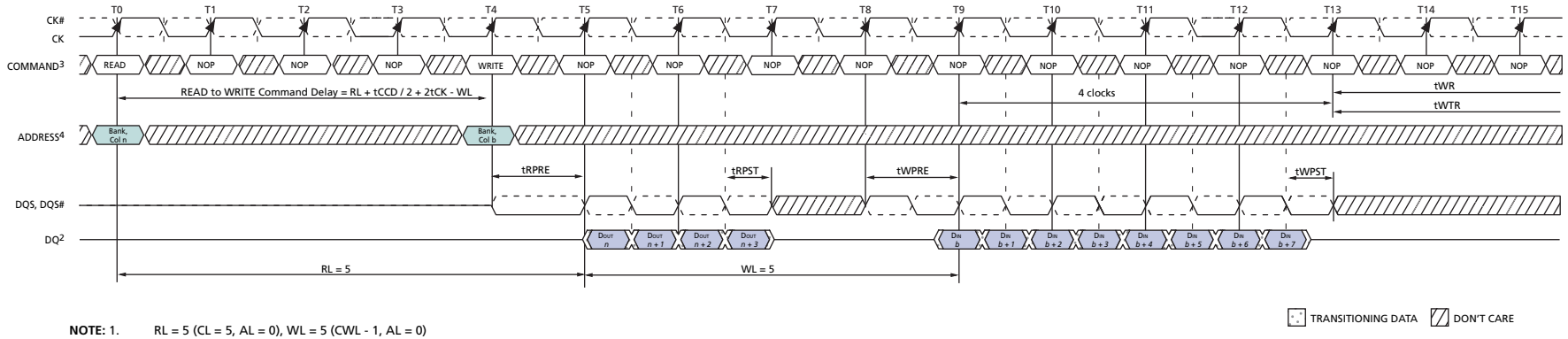
NOTE: 1. RL = 5 (CL = 5, AL = 0)
2. DOUT *n (or b)* = data-out from column *n (or column b)*.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by MR0[A1:0 = 01] and A12 = 1 during READ command at T0.
BC4 setting activated by MR0[A1:0 = 01] and A12 = 0 during READ command at T4.

Figure 37 — READ (BL8) to READ (BC4) OTF



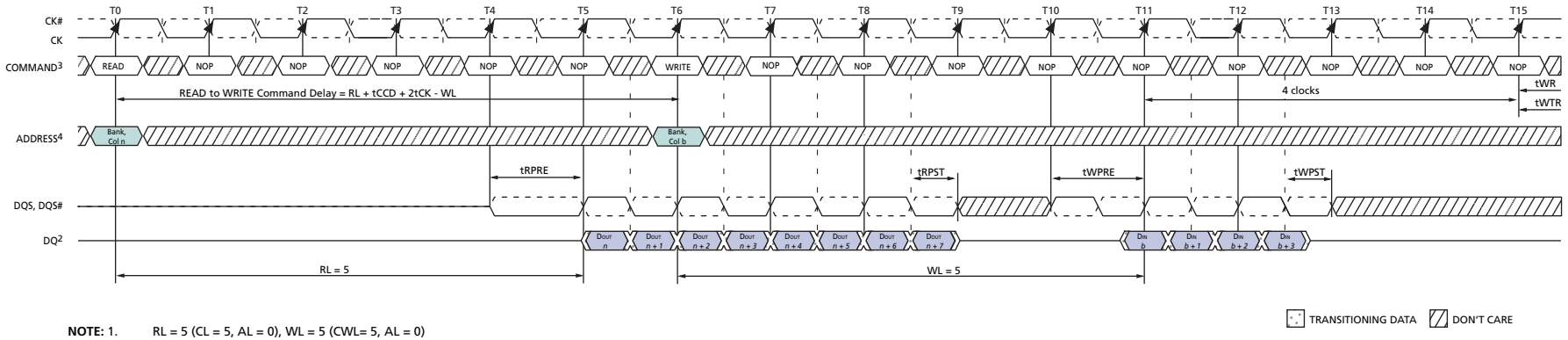
NOTE: 1. RL = 5 (CL = 5, AL = 0)
2. DOUT *n (or b)* = data-out from column *n (or column b)*.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:0 = 01] and A12 = 0 during READ command at T0.
BL8 setting activated by MR0[A1:0 = 01] and A12 = 1 during READ command at T4.

Figure 38 — READ (BC4) to READ (BL8) OTF



NOTE: 1. RL = 5 (CL = 5, AL = 0), WL = 5 (CWL - 1, AL = 0)
2. DOUT *n* = data-out from column, DIN *b* = data-in from column *b*.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:0 = 01] and A12 = 0 during READ command at T0.
BL8 setting activated by MR0[A1:0 = 01] and A12 = 1 during WRITE command at T4.

Figure 39 — READ (BC4) to WRITE (BL8) OTF



NOTE: 1. RL = 5 (CL = 5, AL = 0), WL = 5 (CWL= 5, AL = 0)
2. DOUT *n* = data-out from column, DIN *b* = data-in from column *b*.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by MR0[A1:0 = 01] and A12 = 1 during READ command at T0.
BC4 setting activated by MR0[A1:0 = 01] and A12 = 0 during WRITE command at T6.

Figure 40 — READ (BL8) to WRITE (BC4) OTF

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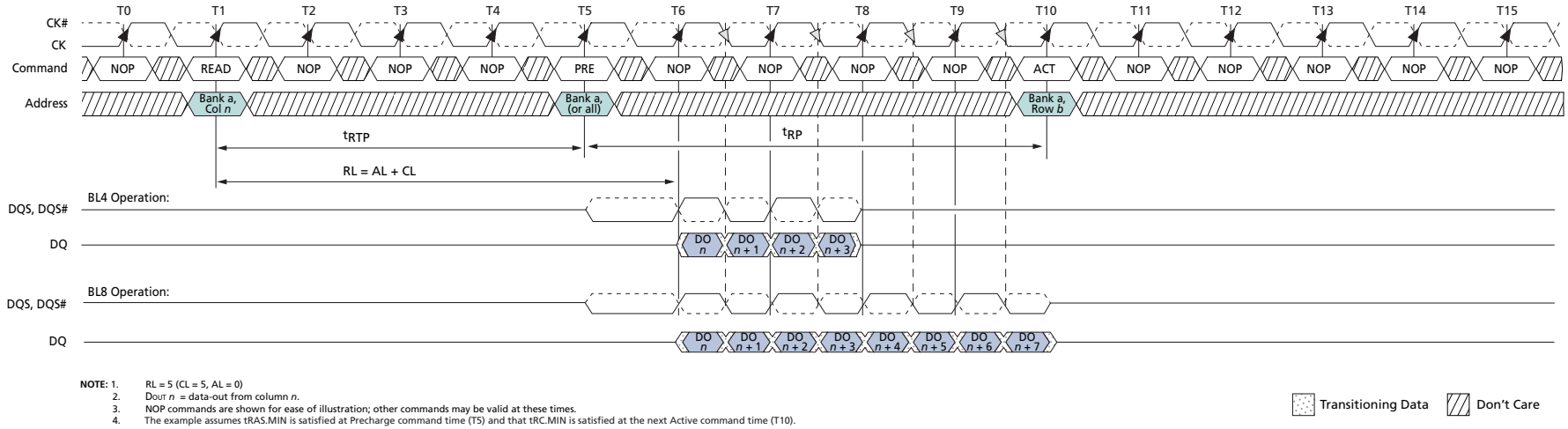
4.13.3 Burst Read Operation followed by a Precharge

The minimum external Read command to Precharge command spacing to the same bank is equal to AL + tRTP with tRTP being the Internal Read Command to Precharge Command Delay. Note that the minimum ACT to PRE timing, tRAS, must be satisfied as well. The minimum value for the Internal Read Command to Precharge Command Delay is given by tRTP.MIN = max(4 × nCK, 7.5 ns). A new bank active command may be issued to the same bank if the following two conditions are satisfied simultaneously:

1. The minimum RAS precharge time (tRP.MIN) has been satisfied from the clock at which the precharge begins.

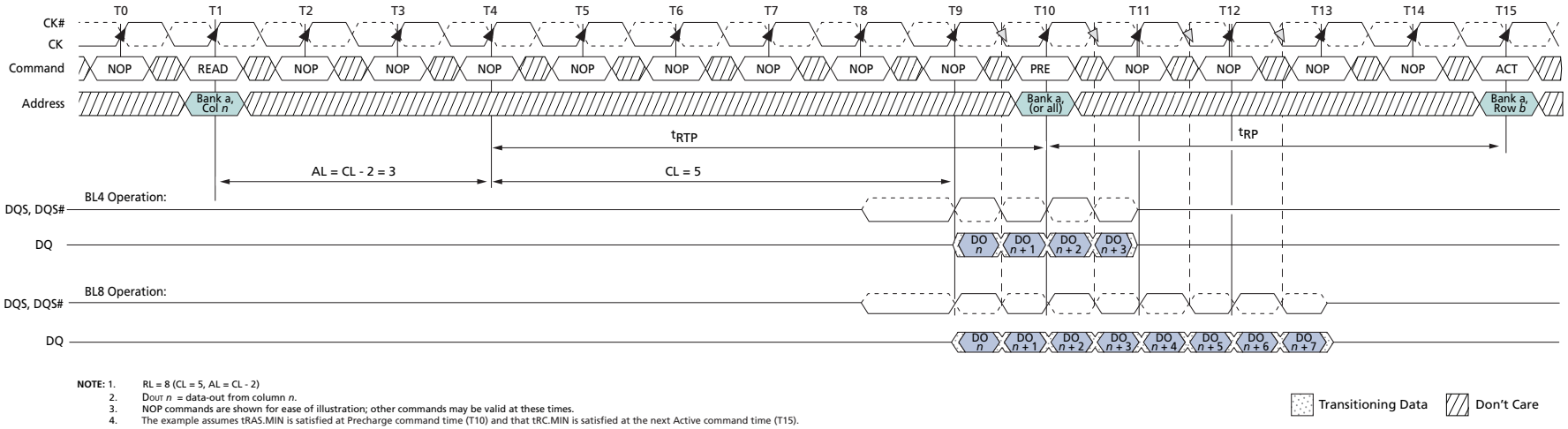
2. The minimum RAS cycle time (tRC.MIN) from the previous bank activation has been satisfied.

Examples of Read commands followed by Precharge are show in Figure 41 and Figure 42.



NOTE: 1. RL = 5 (CL = 5, AL = 0)
2. DOUT *n* = data-out from column *n*.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. The example assumes tRAS.MIN is satisfied at Precharge command time (T5) and that tRC.MIN is satisfied at the next Active command time (T10).

Figure 41 — READ to PRECHARGE, RL = 5, AL = 0, CL = 5, tRTP = 4, tRP = 5



NOTE: 1. RL = 8 (CL = 5, AL = CL - 2)
2. DOUT *n* = data-out from column *n*.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. The example assumes tRAS.MIN is satisfied at Precharge command time (T10) and that tRC.MIN is satisfied at the next Active command time (T15).

Figure 42 — READ to PRECHARGE, RL = 8, AL = CL-2, CL = 5, tRTP = 6, tRP = 5

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4.14 WRITE Operation

4.14.1 DDR3 Burst Operation

During a READ or WRITE command, DDR3 will support BC4 and BL8 on the fly using address A12 during the READ or WRITE (AUTO PRECHARGE can be enabled or disabled).

A12 = 0, BC4 (BC4 = burst chop, tCCD = 4)

A12 = 1, BL8

A12 is used only for burst length control, not as a column address.

4.14.2 WRITE Timing Violations

4.14.2.1 Motivation

Generally, if timing parameters are violated, a complete reset/initialization procedure has to be initiated to make sure that the DRAM works properly. However, it is desirable, for certain minor violations, that the DRAM is guaranteed not to "hang up," and that errors are limited to that particular operation.

For the following, it will be assumed that there are no timing violations with regards to the Write command itself (including ODT, etc.) and that it does satisfy all timing requirements not mentioned below.

4.14.2.2 Data Setup and Hold Violations

Should the data to strobe timing requirements (tDS, tDH) be violated, for any of the strobe edges associated with a write burst, then wrong data might be written to the memory location addressed with this WRITE command.

In the example (Figure 43 on page 69), the relevant strobe edges for write burst A are associated with the clock edges: T5, T5.5, T6, T6.5, T7, T7.5, T8, T8.5.

Subsequent reads from that location might result in unpredictable read data, however the DRAM will work properly otherwise.

4.14.2.3 Strobe to Strobe and Strobe to Clock Violations

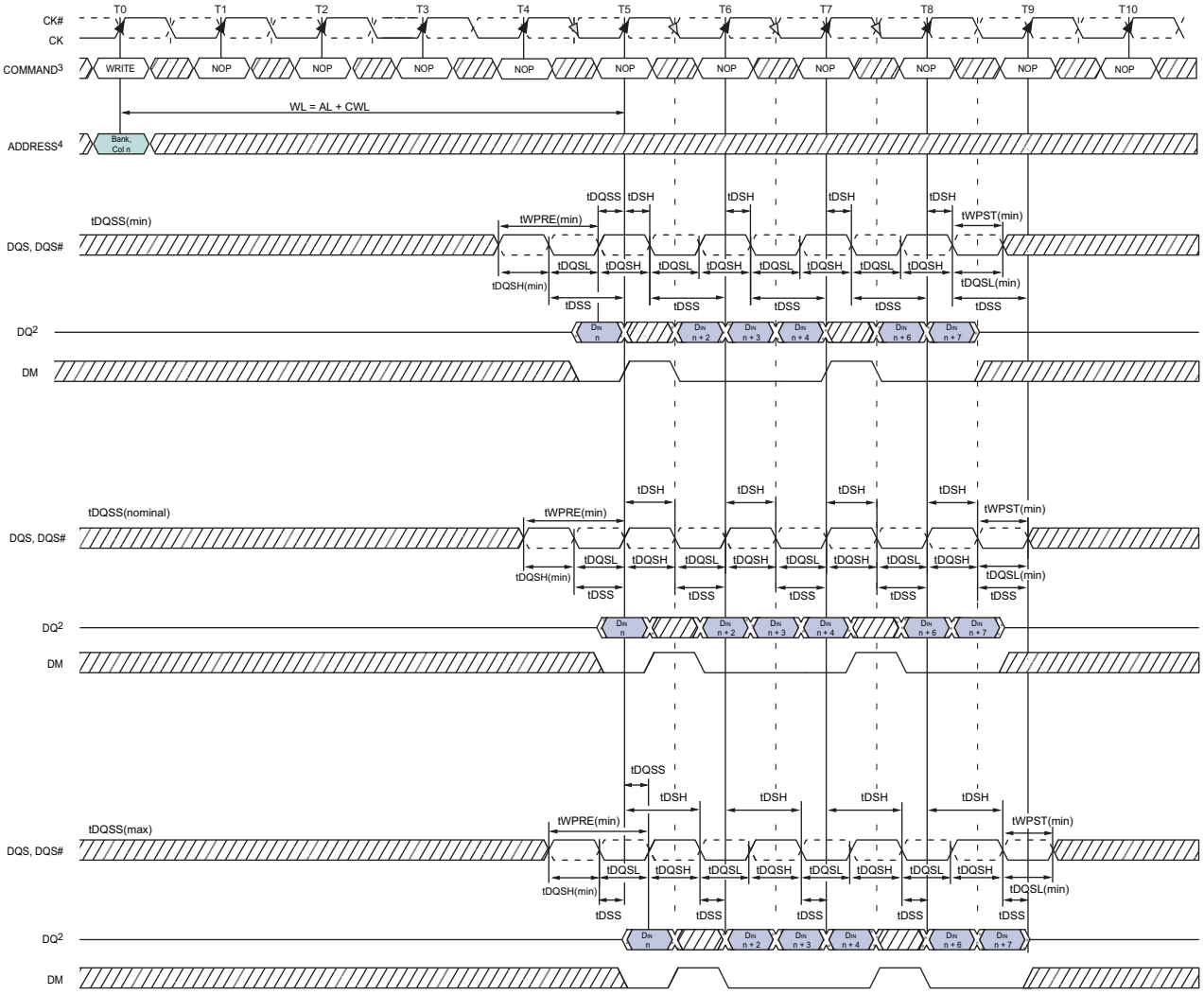
Should the strobe timing requirements (tDQSH, tDQSL, tWPRE, tWPST) or the strobe to clock timing requirements (tDSS, tDSH, tDQSS) be violated, for any of the strobe edges associated with a Write burst, then wrong data might be written to the memory location addressed with the offending WRITE command. Subsequent reads from that location might result in unpredictable read data, however the DRAM will work properly otherwise.

In the example (Figure 43 on page 69) the relevant strobe edges for Write burst *n* are associated with the clock edges: T4, T4.5, T5, T5.5, T6, T6.5, T7, T7.5, T8, T8.5 and T9. Any timing requirements starting or ending on one of these strobe edges need to be fulfilled for a valid burst. For Write burst *b* the relevant edges are T8, T8.5, T9, T9.5, T10, T10.5, T11, T11.5, T12, T12.5 and T13. Some edges are associated with both bursts.

4.14.2.4 Write Timing Parameters

This drawing is for example only to enumerate the strobe edges that "belong" to a Write burst. No actual timing violations are shown here. For a valid burst all timing parameters for each edge of a burst need to be satisfied (not only for one edge - as shown).

4.14 WRITE Operation (Cont'd)
4.14.2 WRITE Timing Violations (Cont'd)



NOTE: 1. BL8, WL = 5 (AL = 0, CWL = 5)
2. D_{IN} n = data-in from column n.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during WRITE command at T0.
5. tDQSS must be met at each rising clock edge.

TRANSITIONING DATA DON'T CARE

Figure 43 — Write Timing Definition and Parameters

4.14.3 Write Data Mask

One write data mask (DM) pin for each 8 data bits (DQ) will be supported on DDR3 SDRAMs, consistent with the implementation on DDR2 SDRAMs. It has identical timings on write operations as the data bits as shown in Figure 43, and though used in a unidirectional manner, is internally loaded identically to data bits to ensure matched system timing. DM is not used during read cycles for any bit organizations including x4, x8, and x16, however, DM of x8 bit organization can be used as TDQS during write cycles if enabled by the MR1[A11] setting. See 3.4.3.7 "TDQS, TDQS#" on page 28 for more details on TDQS vs. DM operations.

4 DDR3 SDRAM Command Description and Operation (Cont'd)
4.14 WRITE Operation (Cont'd)

4.14.4 tWPRE Calculation

The method for calculating differential pulse widths for tWPRE is shown in Figure 44.

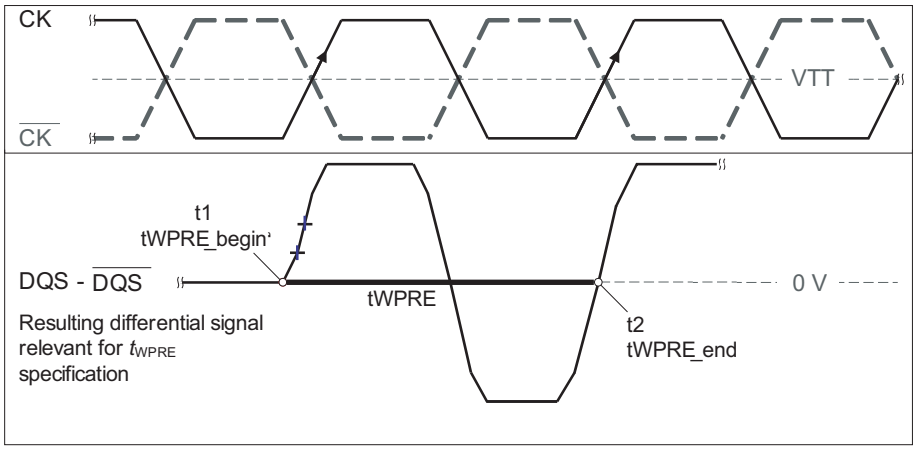


Figure 44 — Method for calculating tWPRE transitions and endpoints

4.14.5 tWPST Calculation

The method for calculating differential pulse widths for tWPST is shown in Figure 45.

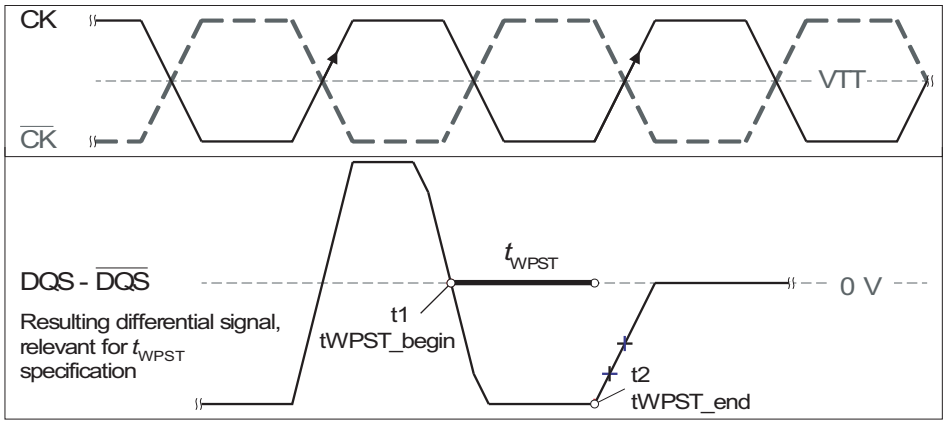
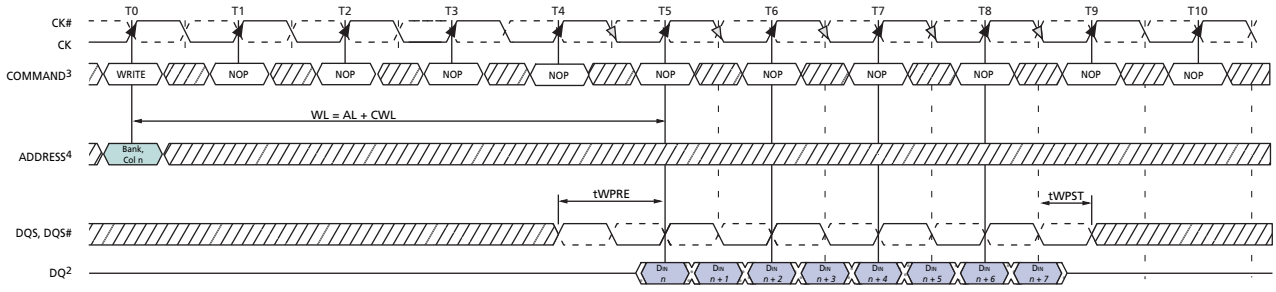


Figure 45 — Method for calculating tWPST transitions and endpoints

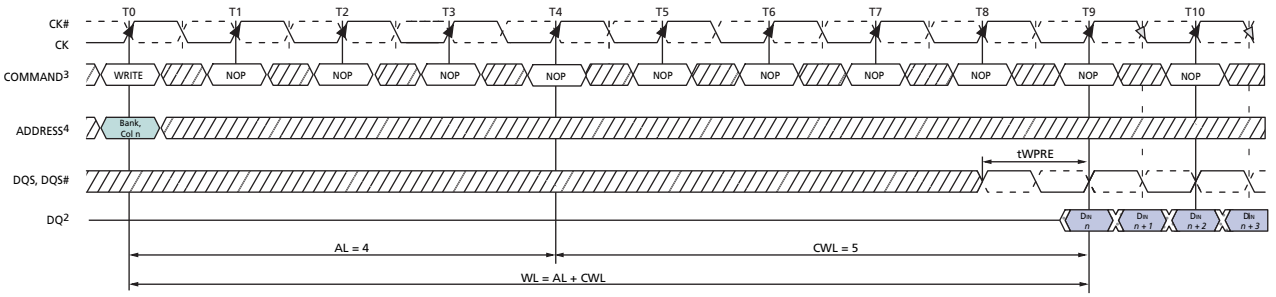
4.14 WRITE Operation (Cont'd)
4.14.5 tWPST Calculation (Cont'd)



NOTE: 1. BL8, WL = 5; AL = 0, CWL = 5.
2. DIN *n* = data-in from column *n*.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during WRITE command at T0.

TRANSITIONING DATA DON'T CARE

Figure 46 — WRITE Burst Operation WL = 5 (AL = 0, CWL = 5, BL8)

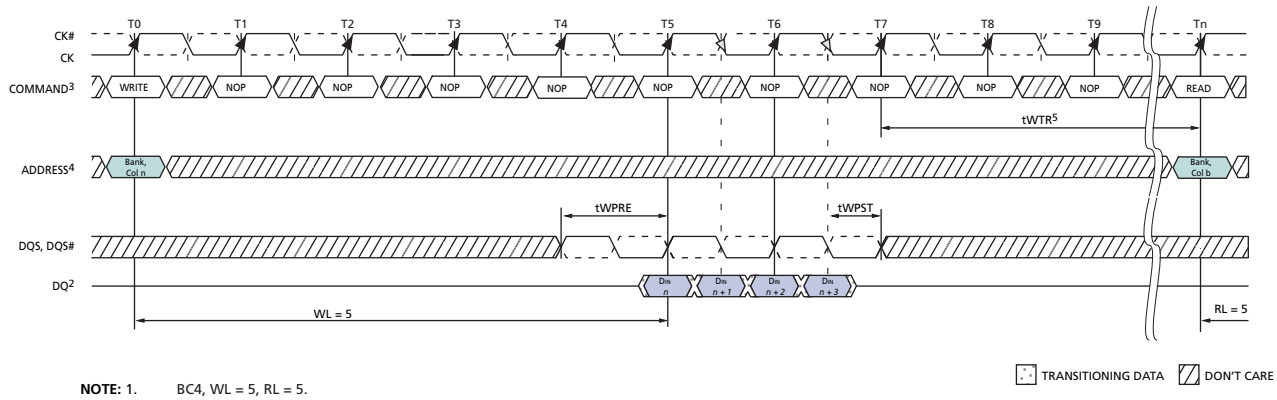


NOTE: 1. BL8, WL = 9; AL = (CL - 1), CL = 5, CWL = 5.
2. DIN *n* = data-in from column *n*.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during WRITE command at T0.

TRANSITIONING DATA DON'T CARE

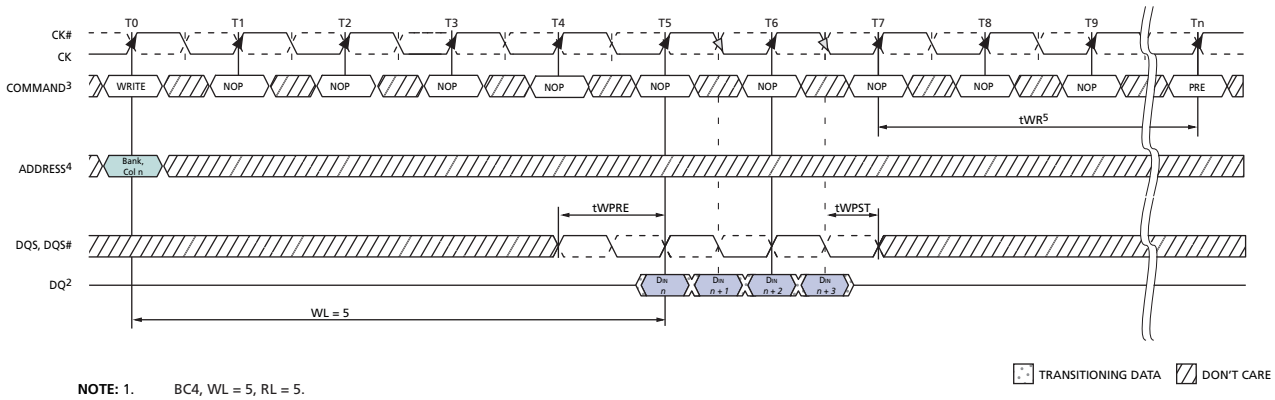
Figure 47 — WRITE Burst Operation WL = 9 (AL = CL-1, CWL = 5, BL8)

4.14 WRITE Operation (Cont'd)
4.14.5 tWPST Calculation (Cont'd)



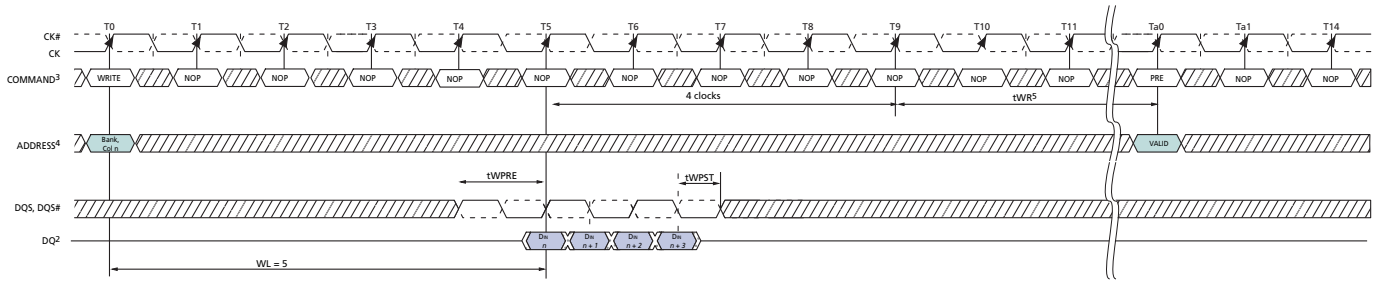
NOTE: 1. BC4, WL = 5, RL = 5.
2. DIN *n* = data-in from column *n*; DOUT *b* = data-out from column *b*.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:0 = 10] during WRITE command at T0 and READ command at Tn.
5. tWTR controls the write to read delay to the same device and starts with the first rising clock edge after the last write data shown at T7.

Figure 48 — WRITE (BC4) to READ (BC4) Operation



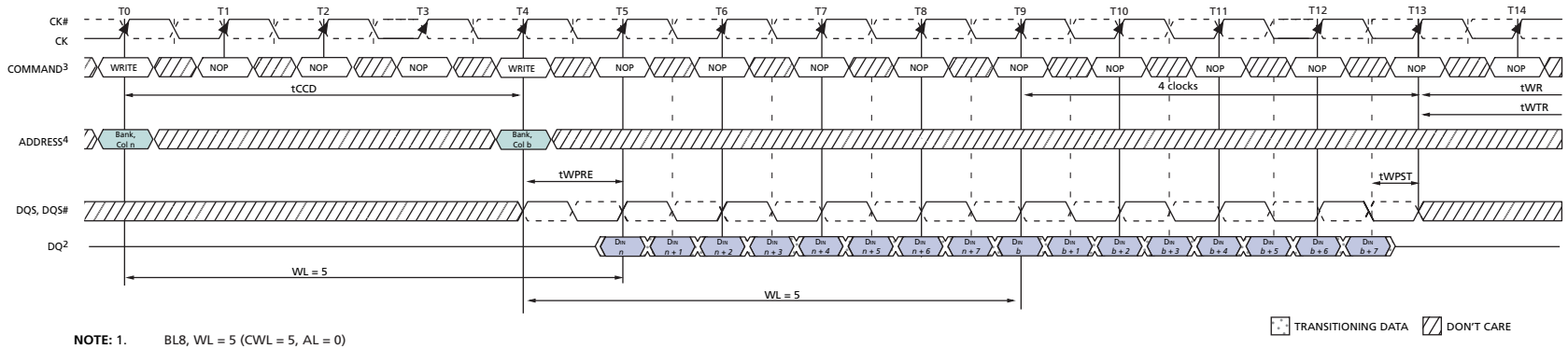
NOTE: 1. BC4, WL = 5, RL = 5.
2. DIN *n* = data-in from column *n*; DOUT *b* = data-out from column *b*.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:0 = 10] during WRITE command at T0.
5. The write recovery time (tWR) referenced from the first rising clock edge after the last write data shown at T7.
tWR specifies the last burst write cycle until the precharge command can be issued to the same bank .

Figure 49 — WRITE (BC4) to PRECHARGE Operation



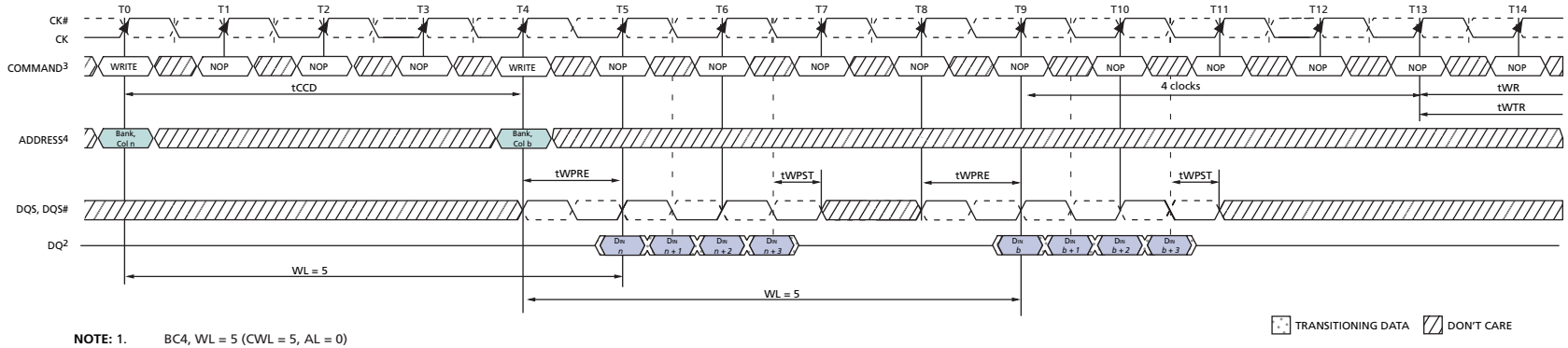
NOTE: 1. BC4 OTF, WL = 5 (CWL = 5, AL = 0)
2. DIN *n (or b)* = data-in from column *n*.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 OTF setting activated by MR0[A1:0 = 01] and A12 = 0 during WRITE command at T0.
5. The write recovery time (tWR) starts at the rising clock edge T9 (4 clocks from T5).

Figure 50 — WRITE (BC4) OTF to PRECHARGE Operation



NOTE: 1. BL8, WL = 5 (CWL = 5, AL = 0)
2. DIN *n (or b)* = data-in from column *n (or column b)*.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during WRITE command at T0 and T4.
5. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T13.

Figure 51 — WRITE (BL8) to WRITE (BL8)



NOTE: 1. BC4, WL = 5 (CWL = 5, AL = 0)
2. DIN *n (or b)* = data-in from column *n (or column b)*.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:0 = 01] and A12 = 0 during WRITE command at T0 and T4.
5. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge at T13 (4 clocks from T9).

Figure 52 — WRITE (BC4) to WRITE (BC4) OTF

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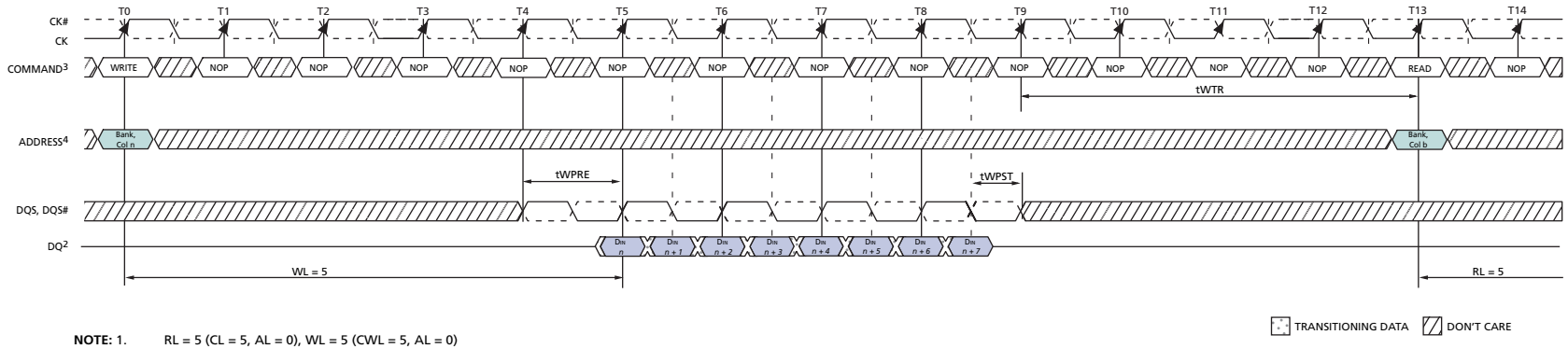
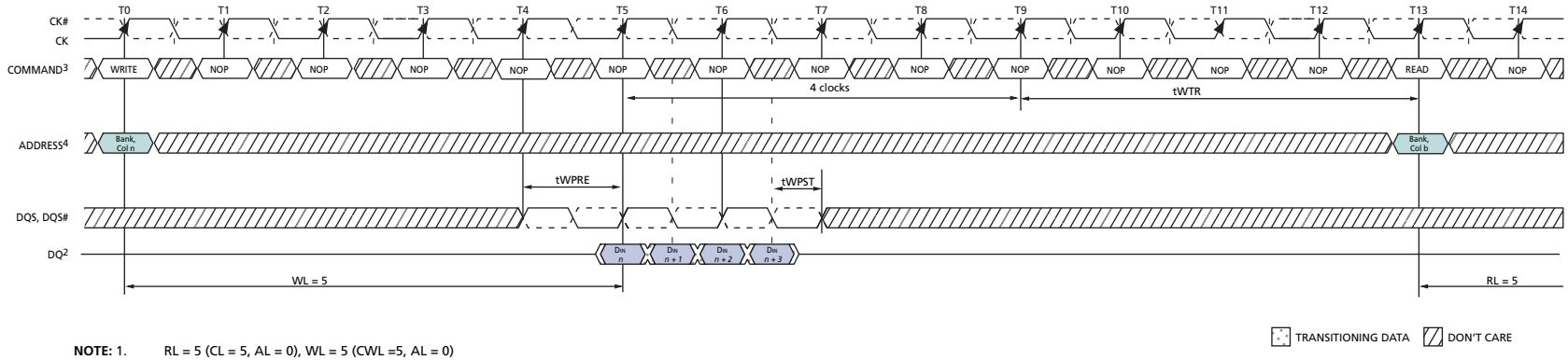


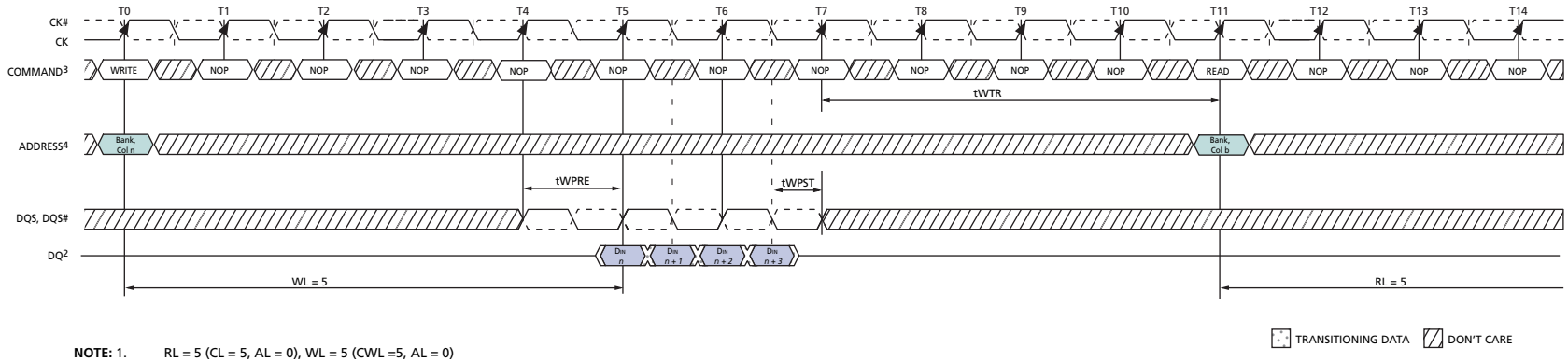
NOTE: 1. RL = 5 (CL = 5, AL = 0), WL = 5 (CWL = 5, AL = 0)
2. D_{IN} *n* = data-in from column *n*; D_{OUT} *b* = data-out from column *b*.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during WRITE command at T0.
READ command at T13 can be either BC4 or BL8 depending on MR0[A1:0] and A12 status at T13.

Figure 53 — WRITE (BL8) to READ (BC4/BL8) OTF



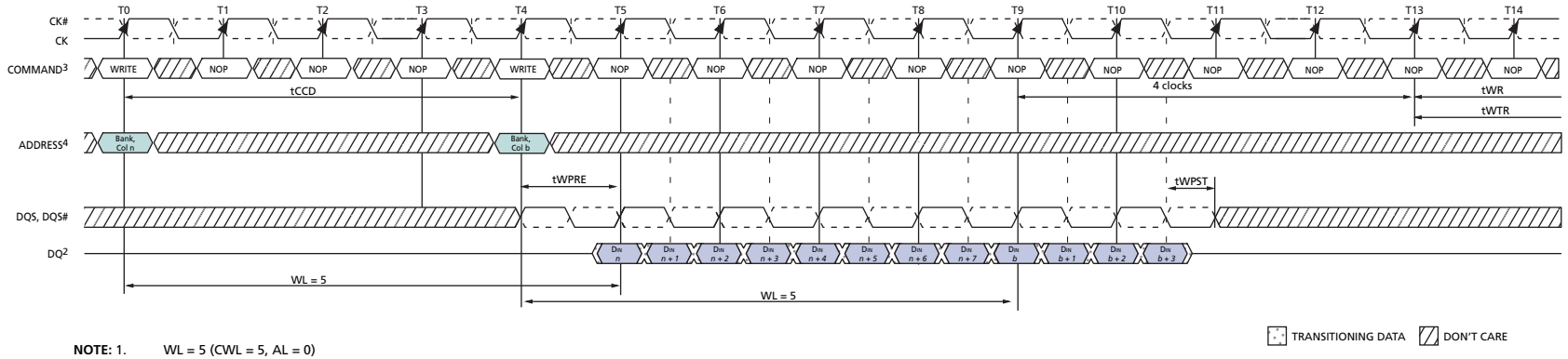
NOTE: 1. RL = 5 (CL = 5, AL = 0), WL = 5 (CWL =5, AL = 0)
2. D_{IN} *n* = data-in from column *n*; D_{OUT} *b* = data-out from column *b*.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:0 = 01] and A12 = 0 during WRITE command at T0.
READ command at T13 can be either BC4 or BL8 depending on A12 status at T13.

Figure 54 — WRITE (BC4) to READ (BC4/BL8) OTF



NOTE: 1. RL = 5 (CL = 5, AL = 0), WL = 5 (CWL =5, AL = 0)
2. DIN *n* = data-in from column *n*; DOUT *b* = data-out from column *b*.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:0 = 10].

Figure 55 — WRITE (BC4) to READ (BC4)



NOTE: 1. WL = 5 (CWL = 5, AL = 0)
2. DIN *n (or b)* = data-in from column *n (or column b)*.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by MR0[A1:0 = 01] and A12 = 1 during WRITE command at T0.
BC4 setting activated by MR0[A1:0 = 01] and A12 = 0 during WRITE command at T4.

Figure 56 — WRITE (BL8) to WRITE (BC4) OTF

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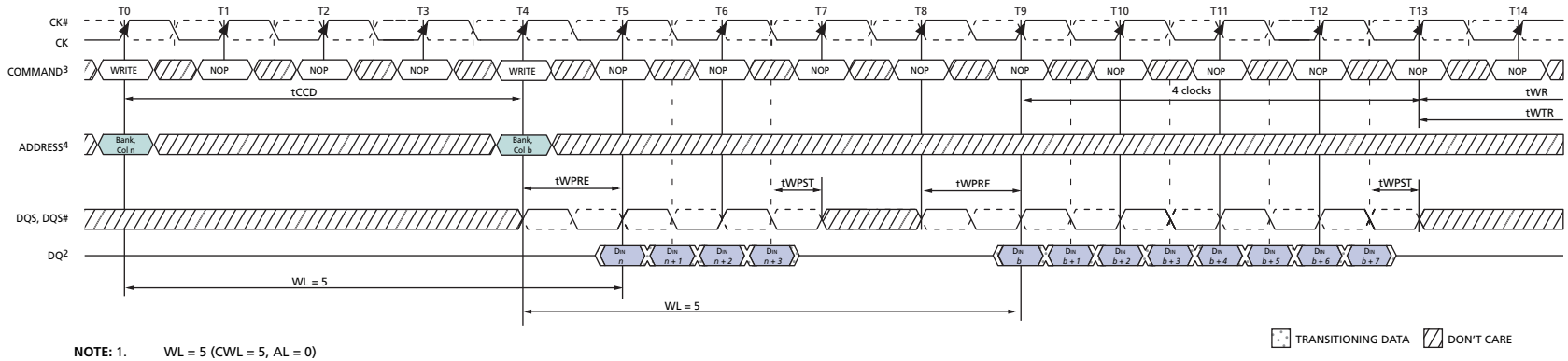


NOTE: 1. WL = 5 (CWL = 5, AL = 0)
2. D_{IN} *n (or b)* = data-in from column *n (or column b)*.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:0 = 01] and A12 = 0 during WRITE command at T0.
BL8 setting activated by MR0[A1:0 = 01] and A12 = 1 during WRITE command at T4.

Figure 57 — WRITE (BC4) to WRITE (BL8) OTF

4 DDR3 SDRAM Command Description and Operation (Cont'd)

4.15 Refresh Command

The Refresh command (REF) is used during normal operation of the DDR3 SDRAMs. This command is non persistent, so it must be issued each time a refresh is required. The DDR3 SDRAM requires Refresh cycles at an average periodic interval of tREFI. When CS#, RAS# and CAS# are held Low and WE# High at the rising edge of the clock, the chip enters a Refresh cycle. All banks of the SDRAM must be pre-charged and idle for a minimum of the precharge time tRP(min) before the Refresh Command can be applied. The refresh addressing is generated by the internal refresh controller. This makes the address bits "Don't Care" during a Refresh command. An internal address counter supplies the addresses during the refresh cycle. No control of the external address bus is required once this cycle has started. When the refresh cycle has completed, all banks of the SDRAM will be in the precharged (idle) state. A delay between the Refresh Command and the next valid command, except NOP or DES, must be greater than or equal to the minimum Refresh cycle time tRFC(min) as shown in Figure 58. Note that the tRFC timing parameter depends on memory density.

In general, a Refresh command needs to be issued to the DDR3 SDRAM regularly every tREFI interval. To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of 8 Refresh commands can be postponed during operation of the DDR3 SDRAM, meaning that at no point in time more than a total of 8 Refresh commands are allowed to be postponed. In case that 8 Refresh commands are postponed in a row, the resulting maximum interval between the surrounding Refresh commands is limited to 9 × tREFI (see Figure 59). A maximum of 8 additional Refresh commands can be issued in advance ("pulled in"), with each one reducing the number of regular Refresh commands required later by one. Note that pulling in more than 8 Refresh commands in advance does not further reduce the number of regular Refresh commands required later, so that the resulting maximum interval between two surrounding Refresh commands is limited to 9 × tREFI (see Figure 60). At any given time, a maximum of 16 REF commands can be issued within 2 x tREFI. Before entering Self-Refresh Mode, all postponed Refresh commands must be executed.

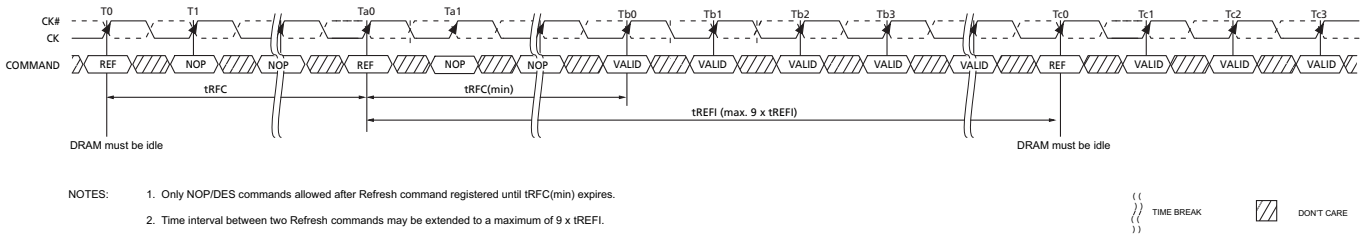


Figure 58 — Refresh Command Timing

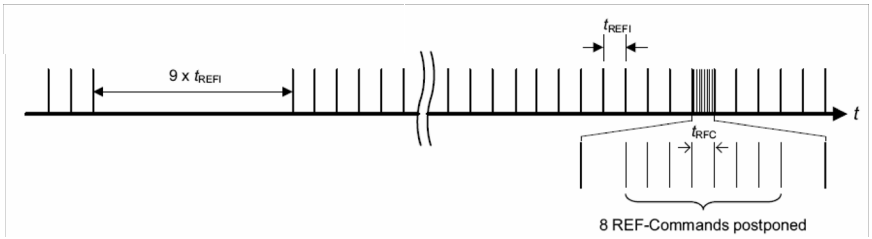


Figure 59 — Postponing Refresh Commands (Example)

4 DDR3 SDRAM Command Description and Operation (Cont'd)
4.15 Self-Refresh Operation (Cont'd)

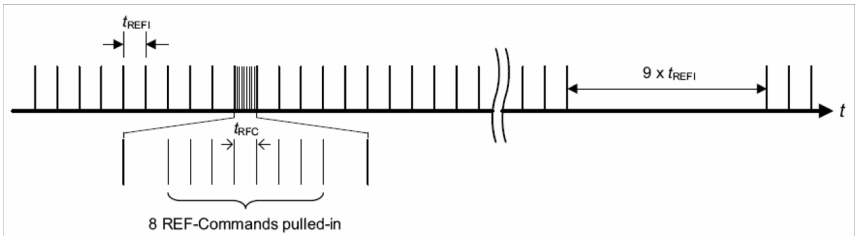


Figure 60 — Pulling-in Refresh Commands (Example)

4.16 Self-Refresh Operation

The Self-Refresh command can be used to retain data in the DDR3 SDRAM, even if the rest of the system is powered down. When in the Self-Refresh mode, the DDR3 SDRAM retains data without external clocking. The DDR3 SDRAM device has a built-in timer to accommodate Self-Refresh operation. The Self-Refresh-Entry (SRE) Command is defined by having CS#, RAS#, CAS#, and CKE held low with WE# high at the rising edge of the clock.

Before issuing the Self-Refresh-Entry command, the DDR3 SDRAM must be idle with all bank precharge state with tRP satisfied. 'Idle state' is defined as all banks are closed (tRP, tDAL, etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied (tMRD, tMOD, tRFC, tZQinit, tZQoper, tZQCS, etc.) Also, on-die termination must be turned off before issuing Self-Refresh-Entry command, by either registering ODT pin low "ODTL + 0.5tCK" prior to the Self-Refresh Entry command or using MRS to MR1 command. Once the Self-Refresh Entry command is registered, CKE must be held low to keep the device in Self-Refresh mode. During normal operation (DLL on), MR1 (A0 = 0), the DLL is automatically disabled upon entering Self-Refresh and is automatically enabled (including a DLL-Reset) upon exiting Self-Refresh.

When the DDR3 SDRAM has entered Self-Refresh mode, all of the external control signals, except CKE and RESET#, are "don't care." For proper Self-Refresh operation, all power supply and reference pins (VDD, VDDQ, VSS, VSSQ, VRefCA and VRefDQ) must be at valid levels. The DRAM initiates a minimum of one Refresh command internally within tCKE period once it enters Self-Refresh mode.

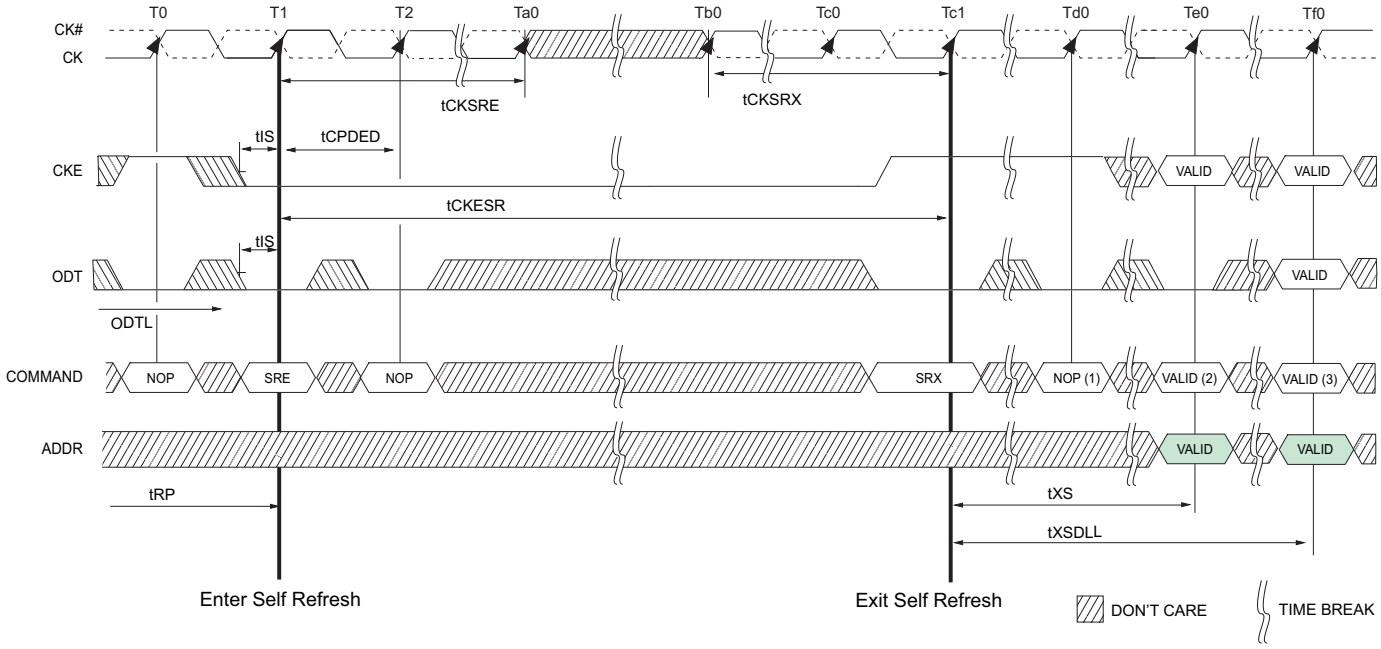
The clock is internally disabled during Self-Refresh Operation to save power. The minimum time that the DDR3 SDRAM must remain in Self-Refresh mode is tCKE. The user may change the external clock frequency or halt the external clock tCKSRE after Self-Refresh entry is registered, however, the clock must be restarted and stable tCKSRX before the device can exit Self-Refresh operation.

The procedure for exiting Self-Refresh requires a sequence of events. First, the clock must be stable prior to CKE going back HIGH. Once a Self-Refresh Exit command (SRX, combination of CKE going high and either NOP or Deselect on command bus) is registered, a delay of at least tXS must be satisfied before a valid command not requiring a locked DLL can be issued to the device to allow for any internal refresh in progress. Before a command that requires a locked DLL can be applied, a delay of at least tXSDLL and applicable ZQCAL function requirements (TBD) must be satisfied.

CKE must remain HIGH for the entire Self-Refresh exit period tXSDLL for proper operation except for Self-Refresh re-entry. Upon exit from Self-Refresh, the DDR3 SDRAM can be put back into Self-Refresh mode after waiting at least tXS period and issuing one refresh command (refresh period of tRFC). NOP or deselect commands must be registered on each positive clock edge during the Self-Refresh exit interval tXS. ODT must be turned off during tXSDLL.

4 DDR3 SDRAM Command Description and Operation (Cont'd)
4.16 Power-Down Modes (Cont'd)

The use of Self-Refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from Self-Refresh mode. Upon exit from Self-Refresh, the DDR3 SDRAM requires a minimum of one extra refresh command before it is put back into Self-Refresh Mode.



NOTES: 1. Only NOP or DES command.
2. Valid commands not requiring a locked DLL.
3. Valid commands requiring a locked DLL.

Figure 61 — Self-Refresh Entry/Exit Timing

4.17 Power-Down Modes

4.17.1 Power-Down Entry and Exit

Power-down is synchronously entered when CKE is registered low (along with NOP or Deselect command). CKE is not allowed to go low while mode register set command, MPR operations, ZQCAL operations, DLL locking or read / write operation are in progress. CKE is allowed to go low while any of other operations such as row activation, precharge or auto-precharge and refresh are in progress, but power-down IDD spec will not be applied until finishing those operations. Timing diagrams are shown in Figures 62 through Figures 74 with details for entry and exit of Power-Down.

The DLL should be in a locked state when power-down is entered for fastest power-down exit timing. If the DLL is not locked during power-down entry, the DLL must be reset after exiting power-down mode for proper read operation and synchronous ODT operation. DRAM design provides all AC and DC timing and voltage specification as well as proper DLL operation with any CKE intensive operations as long as DRAM controller complies with DRAM specifications.

During Power-Down, if all banks are closed after any in-progress commands are completed, the device will be in precharge Power-Down mode; if any bank is open after in-progress commands are completed, the device will be in active Power-Down mode.

Entering power-down deactivates the input and output buffers, excluding CK, CK#, ODT, CKE and RESET#. To protect DRAM internal delay on CKE line to block the input signals, multiple NOP or Deselect commands are needed during the CKE switch off and cycle(s) after, this timing period are defined as tCPDED. CKE_low will result in deactivation of command and address receivers after tCPDED has expired.

Table 14 — Power-Down Entry Definitions

Status of DRAM	MRS bit A12	DLL	PD Exit	Relevant Parameters
Active (A bank or more Open)	Don't Care	On	Fast	**tXP** to any valid command
Precharged (All banks Precharged)	0	Off	Slow	**tXP** to any valid command. Since it is in precharge state, commands here will be ACT, REF, MRS, PRE or PREA. **tXPDLL** to commands that need the DLL to operate, such as RD, RDA or ODT control line.
Precharged (All banks Precharged)	1	On	Fast	**tXP** to any valid command.

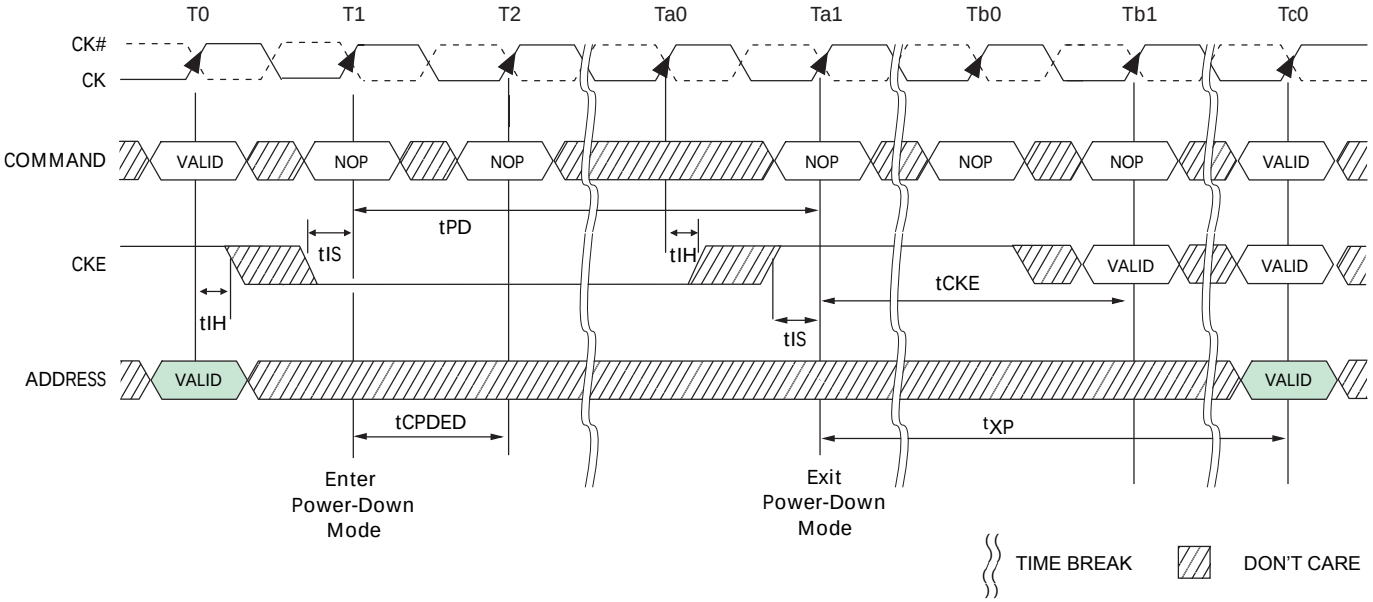
Also, the DLL is disabled upon entering precharge power-down (Slow Exit Mode), but the DLL is kept enabled during precharge power-down (Fast Exit Mode) or active power-down. In power-down mode, CKE low, RESET# high, and a stable clock signal must be maintained at the inputs of the DDR3 SDRAM, and ODT should be in a valid state, but all other input signals are "Don't Care." (If RESET# goes low during Power-Down, the DRAM will be out of PD mode and into reset state.) CKE low must be maintained until tCKE has been satisfied. Power-down duration is limited by 9 times tREFI of the device.

The power-down state is synchronously exited when CKE is registered high (along with a NOP or Deselect command). CKE high must be maintained until tCKE has been satisfied. A valid, executable command can be applied with power-down exit latency, tXP and/or tXPDLL after CKE goes high. Power-down exit latency is defined in the AC specifications table in Section 8.

Active Power Down Entry and Exit timing diagram example is shown in Figure 62. Timing Diagrams for CKE with PD Entry, PD Exit with Read and Read with Auto Precharge, Write, Write with Auto Precharge,

4.17 Power-Down Modes (Cont'd)
4.17.1 Power-Down Entry and Exit (Cont'd)

Activate, Precharge, Refresh, and MRS are shown in Figure 63 through Figure 71. Additional clarifications are shown in Figure 72 through Figure 74.



Note: VALID command at T0 is ACT, NOP, DES or PRE with still one bank remaining open after completion of the precharge command.

Figure 62 — Active Power-Down Entry and Exit Timing Diagram

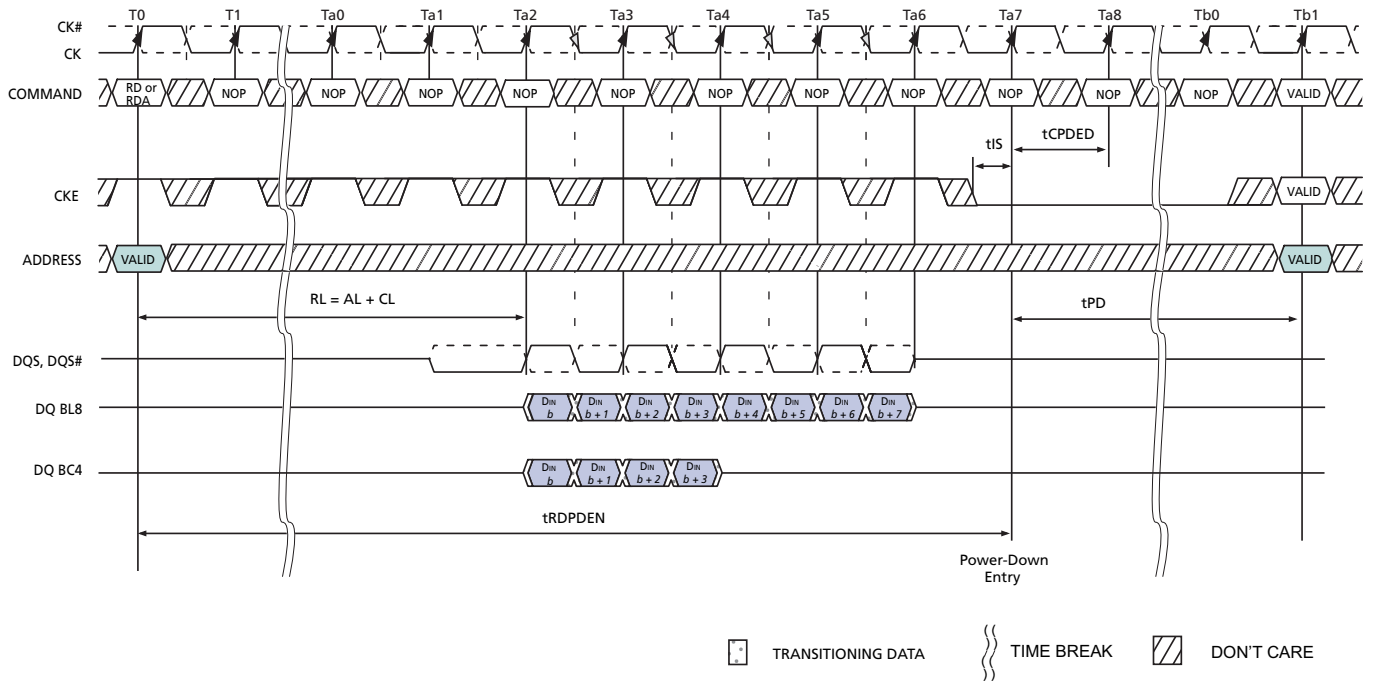


Figure 63 — Power-Down Entry after Read and Read with Auto Precharge

4.17 Power-Down Modes (Cont'd)
4.17.1 Power-Down Entry and Exit (Cont'd)

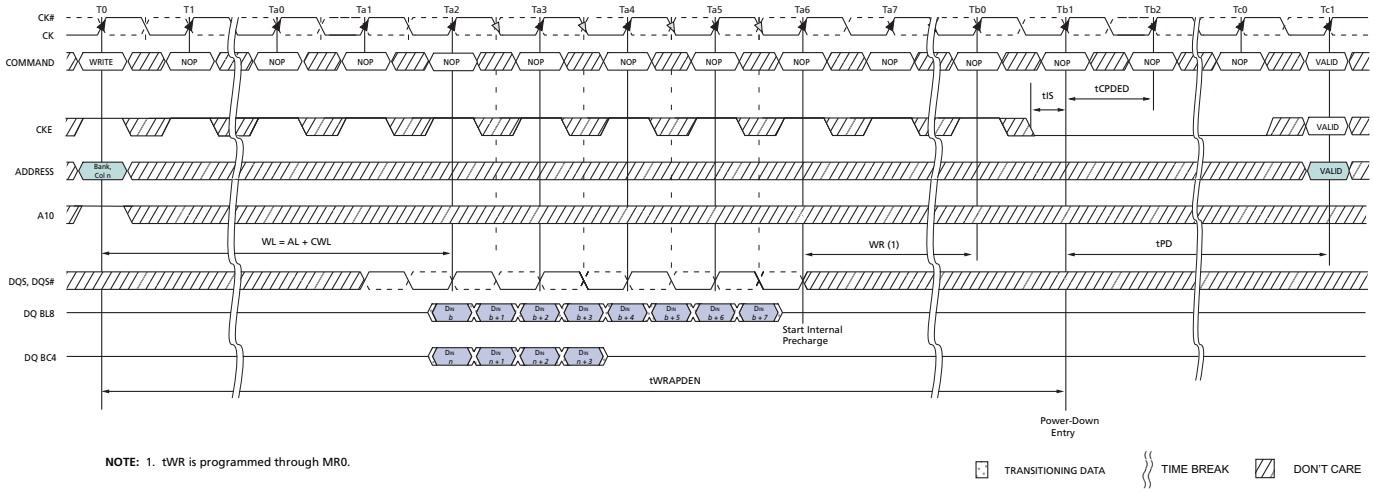


Figure 64 — Power-Down Entry after Write with Auto Precharge

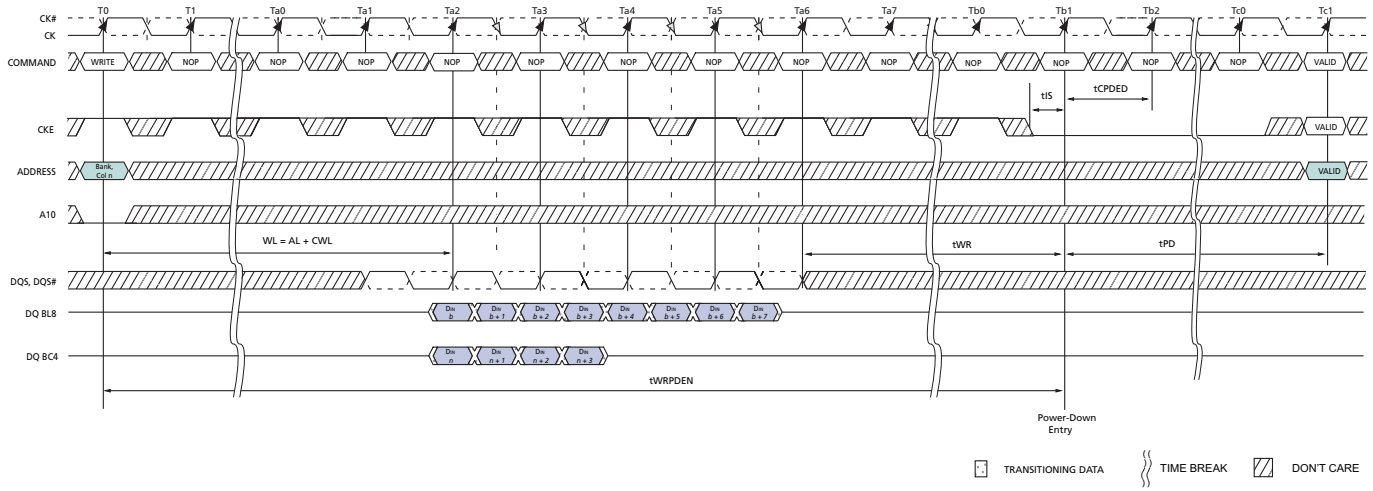


Figure 65 — Power-Down Entry after Write

4.17 Power-Down Modes (Cont'd)
4.17.1 Power-Down Entry and Exit (Cont'd)

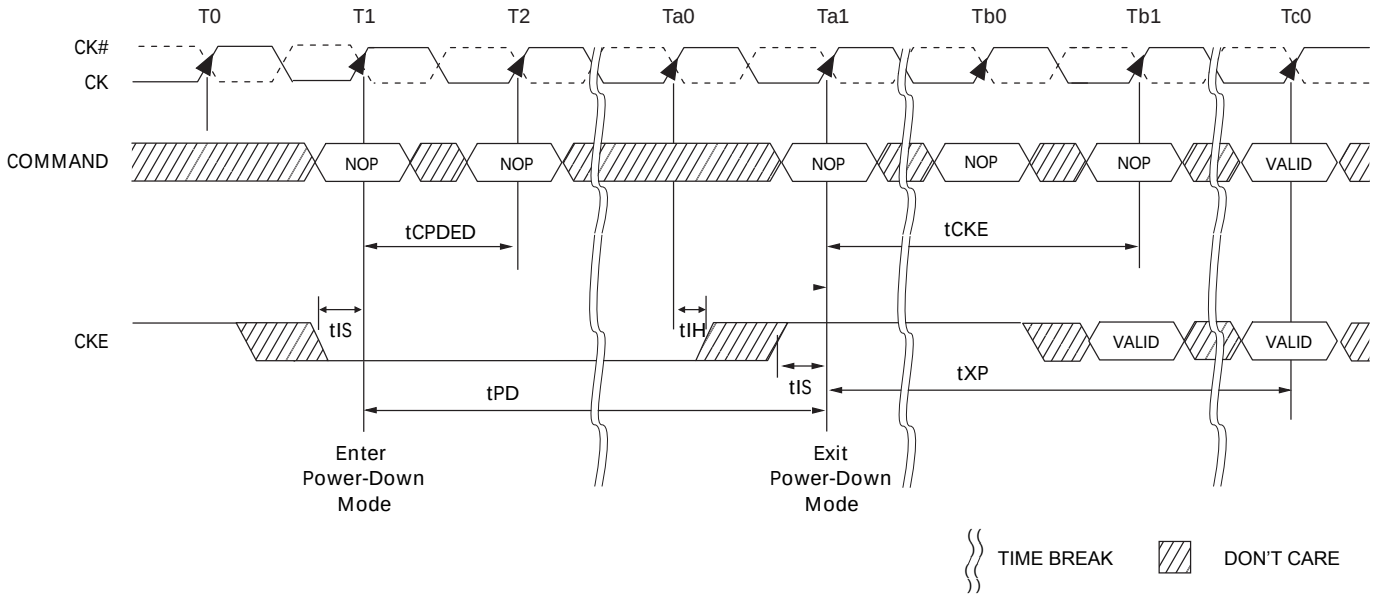


Figure 66 — Precharge Power-Down (Fast Exit Mode) Entry and Exit

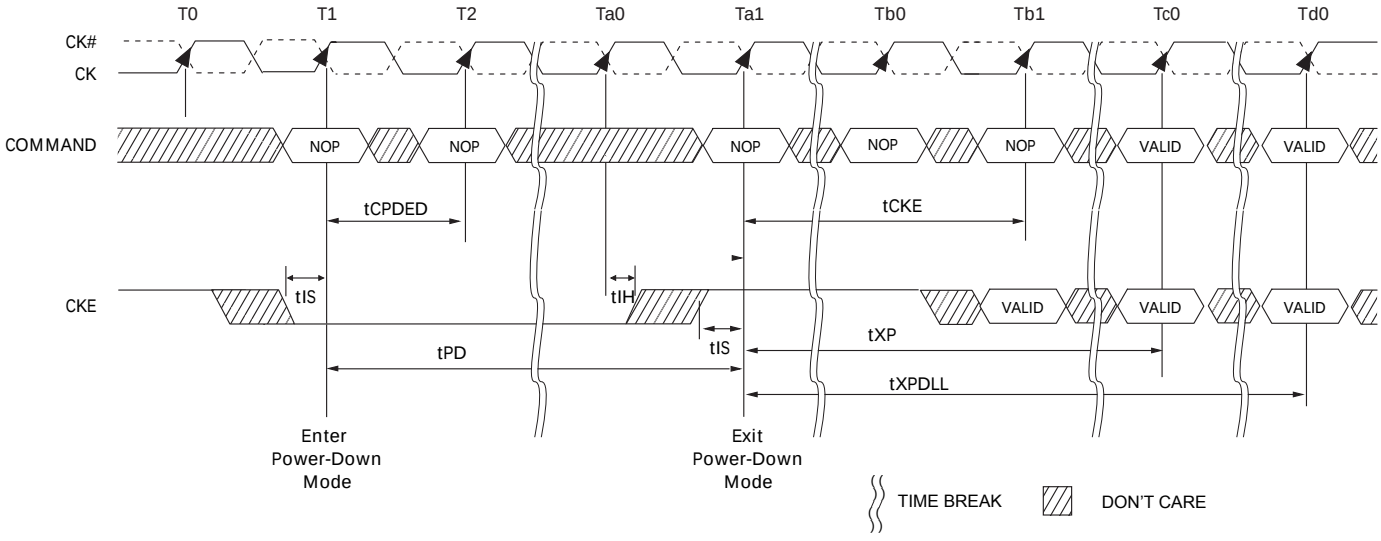


Figure 67 — Precharge Power-Down (Slow Exit Mode) Entry and Exit

4.17 Power-Down Modes (Cont'd)
4.17.1 Power-Down Entry and Exit (Cont'd)

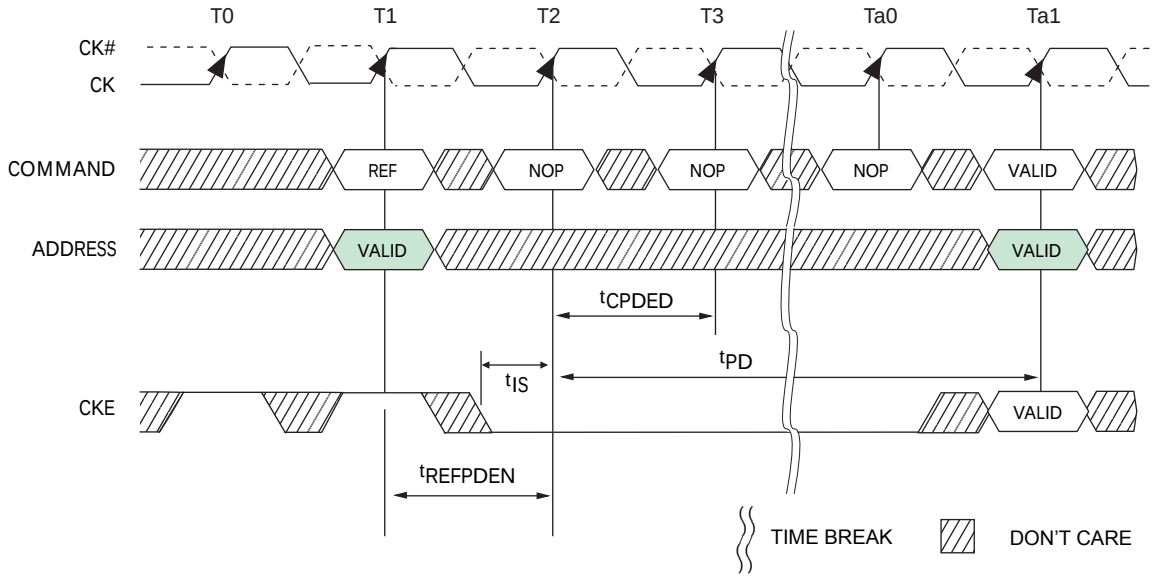


Figure 68 — Refresh Command to Power-Down Entry

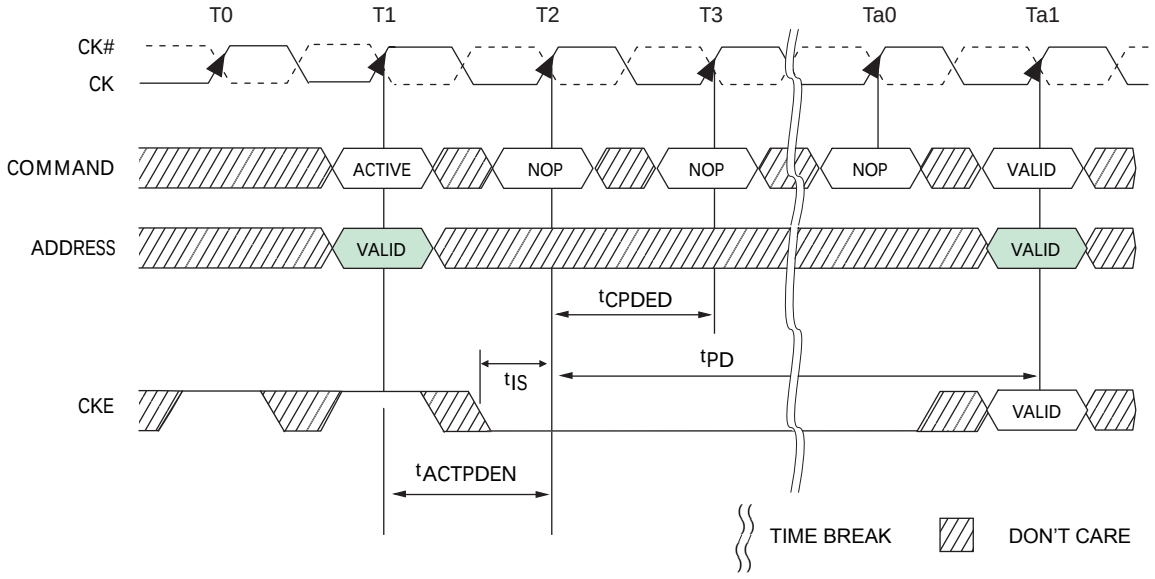


Figure 69 — Active Command to Power-Down Entry

4.17 Power-Down Modes (Cont'd)
4.17.1 Power-Down Entry and Exit (Cont'd)

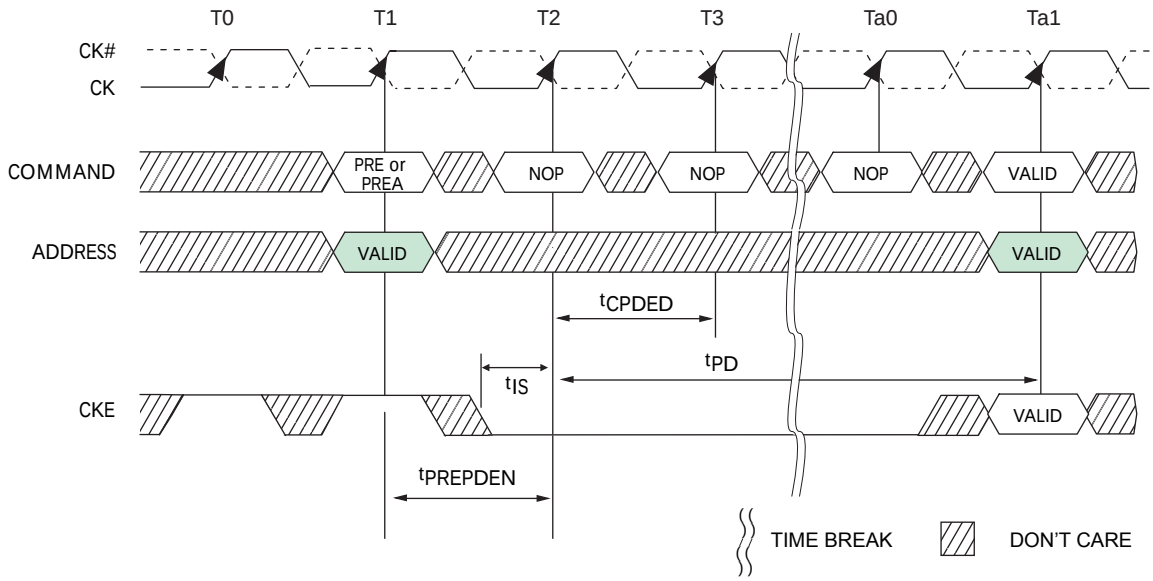


Figure 70 — Precharge / Precharge all Command to Power-Down Entry

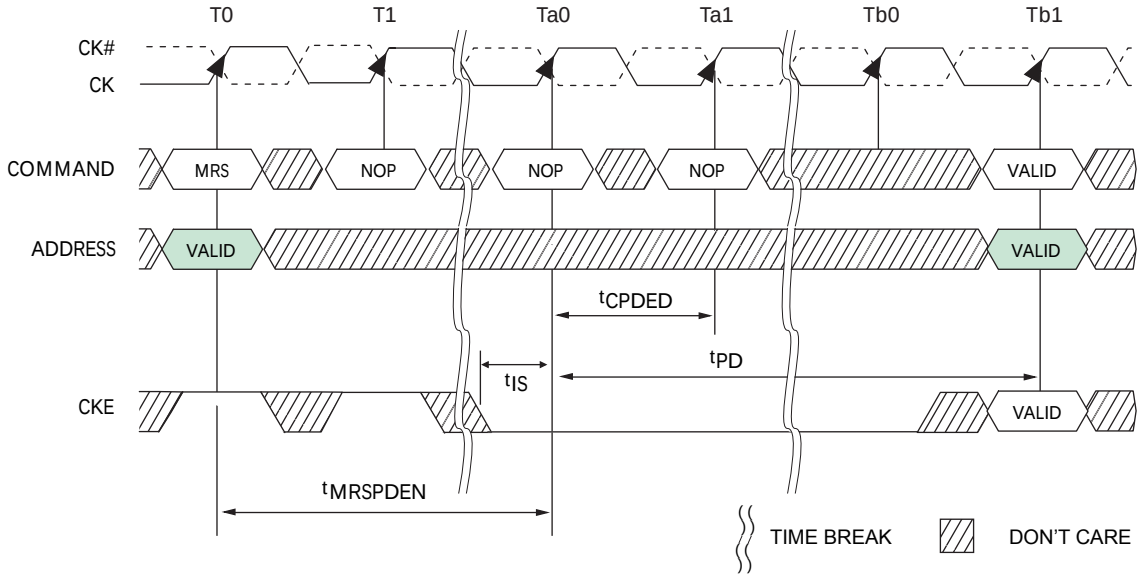


Figure 71 — MRS Command to Power-Down Entry

4.17.2 Power-Down clarifications - Case 1

When CKE is registered low for power-down entry, tPD(min) must be satisfied before CKE can be registered high for power-down exit. The minimum value of parameter tPD(min) is equal to the minimum value

4.17 Power-Down Modes (Cont'd)
4.17.2 Power-Down clarifications - Case 1 (Cont'd)

of parameter tCKE(min) as shown in Table 65, Timing Parameters by Speed Bin. A detailed example of Case 1 is shown in Figure 72.)

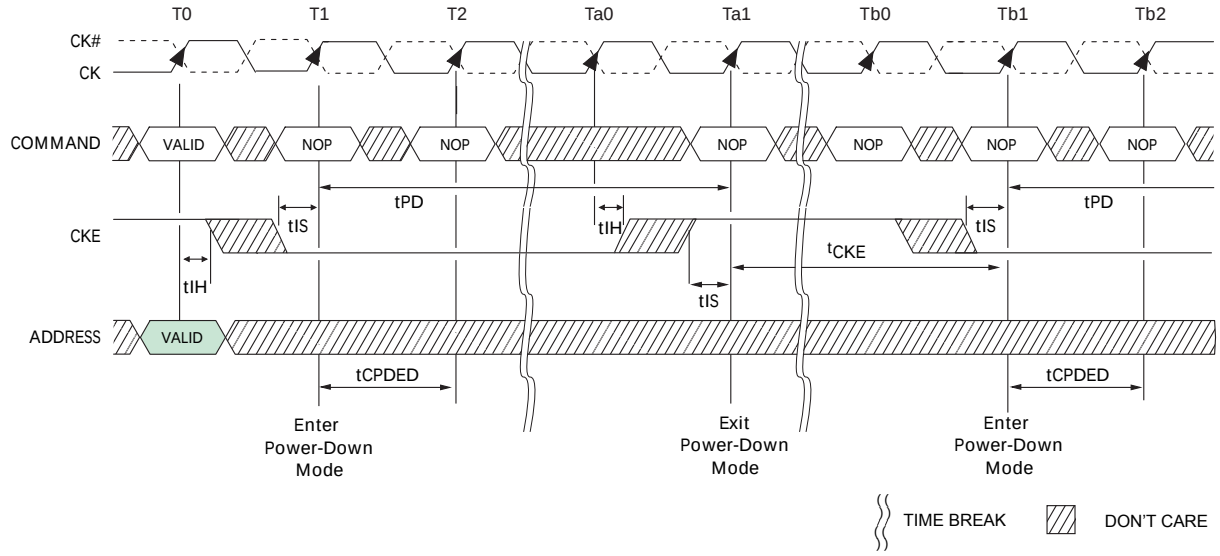


Figure 72 — Power-Down Entry/Exit Clarifications - Case 1

4.17.3 Power-Down clarifications - Case 2

For certain CKE intensive operations, for example, repeated 'PD Exit - Refresh - PD Entry' sequences, the number of clock cycles between PD Exit and PD Entry may be insufficient to keep the DLL updated. Therefore, the following conditions must be met in addition to tCKE in order to maintain proper DRAM operation when the Refresh command is issued between PD Exit and PD Entry. Power-down mode can be used in conjunction with the Refresh command if the following conditions are met: 1) tXP must be satisfied before issuing the command. 2) tXPDLL must be satisfied (referenced to the registration of PD Exit) before the next power-down can be entered. A detailed example of Case 2 is shown in Figure 73.

)

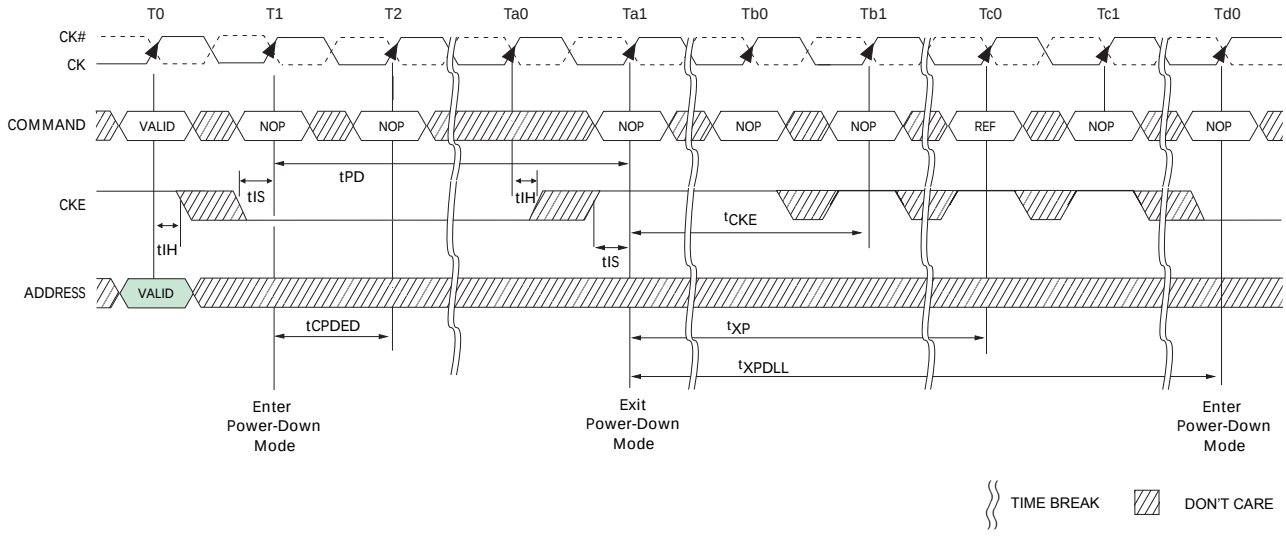


Figure 73 — Power-Down Entry/Exit Clarifications - Case 2

4 DDR3 SDRAM Command Description and Operation (Cont'd)
4.17 Power-Down Modes (Cont'd)

4.17.4 Power-Down clarifications - Case 3

If an early PD Entry is issued after a Refresh command, once PD Exit is issued, NOP or DES with CKE High must be issued until tRFC(min) from the Refresh command is satisfied. This means CKE can not be registered low twice within a tRFC(min) window. A detailed example of Case 3 is shown in Figure 74.

)

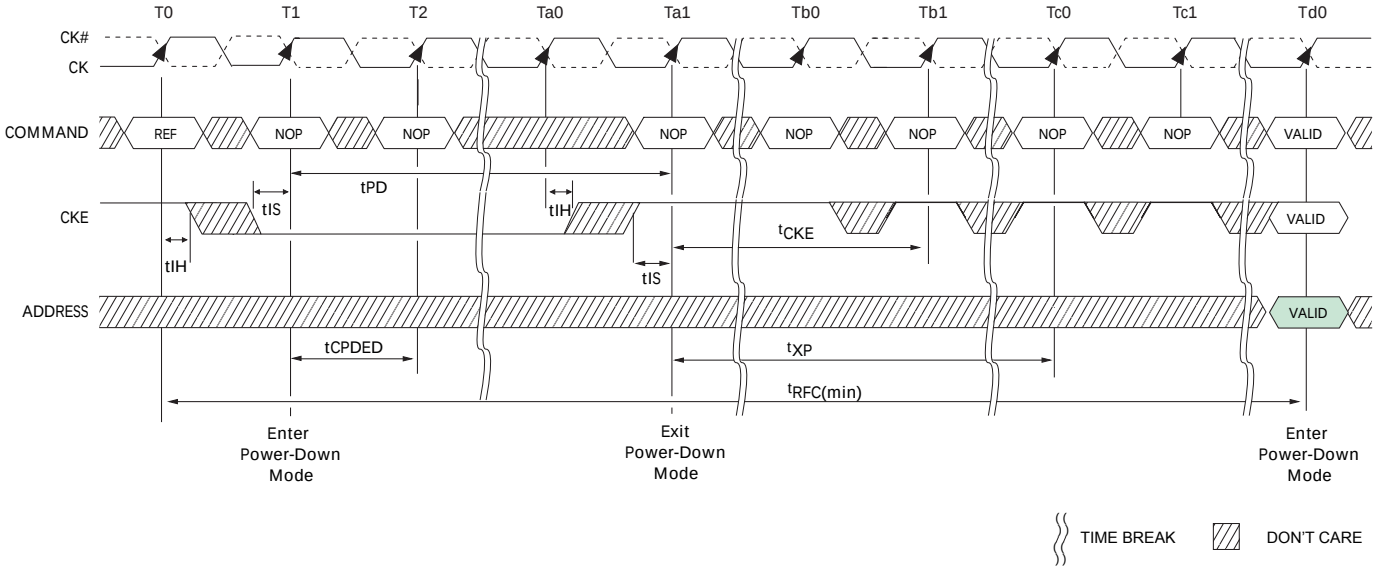


Figure 74 — Power-Down Entry/Exit Clarifications - Case 3

4.18 ZQ Calibration Commands

4.18.1 ZQ Calibration Description

ZQ Calibration command is used to calibrate DRAM Ron & ODT values. DDR3 SDRAM needs longer time to calibrate output driver and on-die termination circuits at initialization and relatively smaller time to perform periodic calibrations.

ZQCL command is used to perform the initial calibration during power-up initialization sequence. This command may be issued at any time by the controller depending on the system environment. ZQCL command triggers the calibration engine inside the DRAM and, once calibration is achieved, the calibrated values are transferred from the calibration engine to DRAM IO, which gets reflected as updated output driver and on-die termination values.

The first ZQCL command issued after reset is allowed a timing period of tZQinit to perform the full calibration and the transfer of values. All other ZQCL commands except the first ZQCL command issued after RESET are allowed a timing period of tZQoper.

ZQCS command is used to perform periodic calibrations to account for voltage and temperature variations. A shorter timing window is provided to perform the calibration and transfer of values as defined by timing parameter tZQCS. One ZQCS command can effectively correct a minimum of 0.5 % (ZQ Correction) of RON and RTT impedance error within 64 nCK for all speed bins assuming the maximum sensitivities specified in the 'Output Driver Voltage and Temperature Sensitivity' and 'ODT Voltage and Temperature Sensitivity' tables. The appropriate interval between ZQCS commands can be determined from these tables and other application-specific parameters. One method for calculating the interval between ZQCS commands, given the temperature (Tdriftrate) and voltage (Vdriftrate) drift rates that the SDRAM is subject to in the application, is illustrated. The interval could be defined by the following formula:

$$\frac{ZQCorrection}{(TSens \times Tdriftrate) + (VSens \times Vdriftrate)}$$

where TSens = max(dRTTdT, dRONdTM) and VSens = max(dRTTdV, dRONdVM) define the SDRAM temperature and voltage sensitivities.

For example, if TSens = 1.5% / ^{o}C, VSens = 0.15% / mV, Tdriftrate = 1 ^{o}C / sec and Vdriftrate = 15 mV / sec, then the interval between ZQCS commands is calculated as:

$$\frac{0.5}{(1.5 \times 1) + (0.15 \times 15)} = 0.133 \approx 128ms$$

No other activities should be performed on the DRAM channel by the controller for the duration of tZQinit, tZQoper, or tZQCS. The quiet time on the DRAM channel allows accurate calibration of output driver and on-die termination values. Once DRAM calibration is achieved, the DRAM should disable ZQ current consumption path to reduce power.

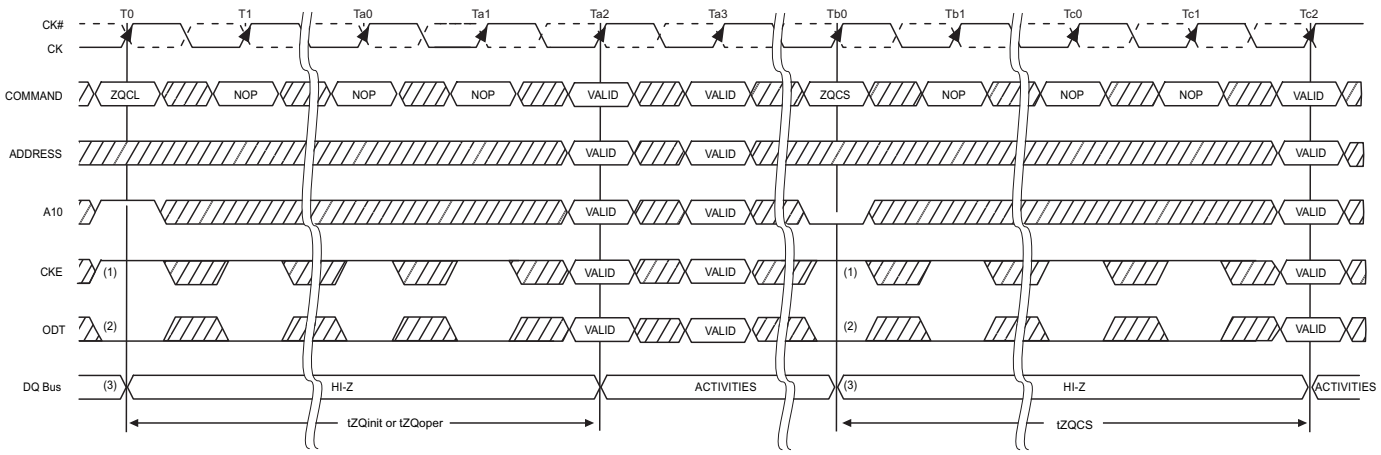
All banks must be precharged and tRP met before ZQCL or ZQCS commands are issued by the controller. See "[BA=Bank Address, RA=Row Address, CA=Column Address, BC#=Burst Chop, X=Don't Care, V=Valid]" on page 33 for a description of the ZQCL and ZQCS commands.

ZQ calibration commands can also be issued in parallel to DLL lock time when coming out of self refresh. Upon Self-Refresh exit, DDR3 SDRAM will not perform an IO calibration without an explicit ZQ calibration command. The earliest possible time for ZQ Calibration command (short or long) after self refresh exit is tXS.

4.18 DDR3 SDRAM Command Description and Operation) (Cont'd)
4.18.1 ZQ Calibration Description (Cont'd)

In systems that share the ZQ resistor between devices, the controller must not allow any overlap of tZQoper, tZQinit, or tZQCS between the devices.

4.18.2 ZQ Calibration Timing



NOTES: 1. CKE must be continuously registered high during the calibration procedure.

2. On-die termination must be disabled via the ODT signal or MRS during the calibration procedure.

3. All devices connected to the DQ bus should be high impedance during the calibration procedure.

Figure 75 — ZQ Calibration Timing

4.18.3 ZQ External Resistor Value, Tolerance, and Capacitive loading

In order to use the ZQ Calibration function, a 240 ohm +/- 1% tolerance external resistor must be connected between the ZQ pin and ground. The single resistor can be used for each SDRAM or one resistor can be shared between two SDRAMs if the ZQ calibration timings for each SDRAM do not overlap. The total capacitive loading on the ZQ pin must be limited (See Table 59 — "Input / Output Capacitance" on page 153).

5 On-Die Termination (ODT)

ODT (On-Die Termination) is a feature of the DDR3 SDRAM that allows the DRAM to turn on/off termination resistance for each DQ, DQS, DQS# and DM for x4 and x8 configuration (and TDQS, TDQS# for X8 configuration, when enabled via A11=1 in MR1) via the ODT control pin. For x16 configuration, ODT is applied to each DQU, DQL, DQSU, DQSU#, DQSL, DQSL#, DMU and DML signal via the ODT control pin. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices. More details about ODT control modes and ODT timing modes can be found further down in this document:

- The ODT control modes are described in 5.1.
- The ODT synchronous mode is described in 5.2
- The dynamic ODT feature is described in 5.3
- The ODT asynchronous mode is described in 5.4
- The transitions between ODT synchronous and asynchronous are described in 5.4.1 through 5.4.4

The ODT feature is turned off and not supported in Self-Refresh mode.

A simple functional representation of the DRAM ODT feature is shown in Figure 76.

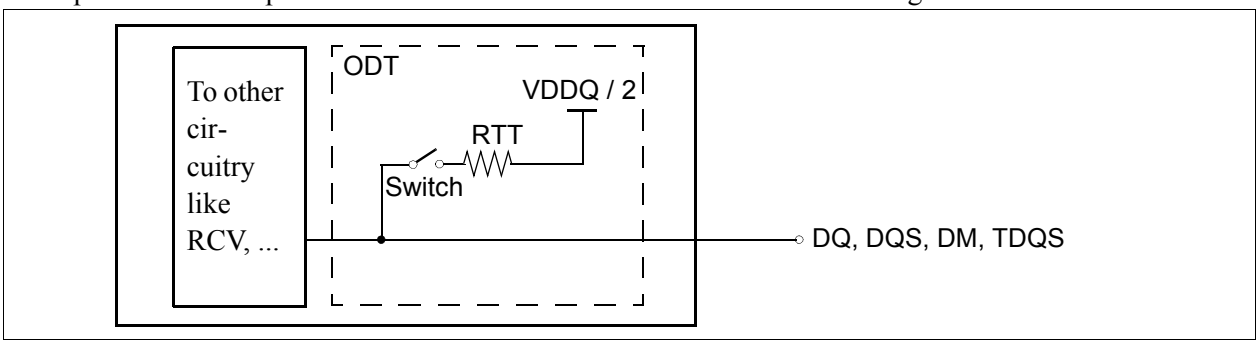


Figure 76 — Functional Representation of ODT

The switch is enabled by the internal ODT control logic, which uses the external ODT pin and other control information, see below. The value of RTT is determined by the settings of Mode Register bits (see Figure 10 on page 26 and Figure 11 on page 29). The ODT pin will be ignored if the Mode Registers MR1 and MR2 are programmed to disable ODT, and in self-refresh mode.

5.1 ODT Mode Register and ODT Truth Table

The ODT Mode is enabled if any of MR1 {A9, A6, A2} or MR2 {A10, A9} are non zero. In this case, the value of RTT is determined by the settings of those bits (see Figure on page 26).

Application: Controller sends WR command together with ODT asserted.

- One possible application: The rank that is being written to provides termination.
- DRAM turns ON termination if it sees ODT asserted (unless ODT is disabled by MR).
- DRAM does not use any write or read command decode information.
- The Termination Truth Table is shown in Table 15.

Table 15 — Termination Truth Table

ODT pin	DRAM Termination State
0	OFF
1	ON, (OFF, if disabled by MR1 {A9, A6, A2} and MR2 {A10, A9} in general)

5.2 Synchronous ODT Mode

Synchronous ODT mode is selected whenever the DLL is turned on and locked. Based on the power-down definition, these modes are:

- Any bank active with CKE high
- Refresh with CKE high
- Idle mode with CKE high
- Active power down mode (regardless of MR0 bit A12)
- Precharge power down mode if DLL is enabled during precharge power down by MR0 bit A12.

The direct ODT feature is not supported during DLL-off mode. The on-die termination resistors must be disabled by continuously registering the ODT pin low and/or by programming the RTT_Nom bits MR1{A9,A6,A2} to {0,0,0} via a mode register set command during DLL-off mode.

In synchronous ODT mode, RTT will be turned on ODTLon clock cycles after ODT is sampled high by a rising clock edge and turned off ODTLoff clock cycles after ODT is registered low by a rising clock edge. The ODT latency is tied to the write latency (WL) by: ODTLon = WL - 2; ODTLoff = WL - 2 .

5.2.1 ODT Latency and Posted ODT

In Synchronous ODT Mode, the Additive Latency (AL) programmed into the Mode Register (MR1) also applies to the ODT signal. The DRAM internal ODT signal is delayed for a number of clock cycles defined by the Additive Latency (AL) relative to the external ODT signal. ODTLon = CWL + AL - 2; ODTLoff = CWL + AL - 2. For details, refer to DDR3 SDRAM latency definitions.

Table 16 — ODT Latency

Symbol	Parameter	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	Unit
ODTLon	ODT turn on Latency	WL - 2 = CWL + AL - 2				t_{CK}
ODTLoff	ODT turn off Latency	WL - 2 = CWL + AL - 2				

5.2.2 Timing Parameters

In synchronous ODT mode, the following timing parameters apply (see also Figures 77):

ODTLon, ODTLoff, $t_{AON,min,max}$, $t_{AOF,min,max}$.

Minimum RTT turn-on time (t_{AON}min) is the point in time when the device leaves high impedance and ODT resistance begins to turn on. Maximum RTT turn on time (t_{AON}max) is the point in time when the ODT resistance is fully on. Both are measured from ODTLon.

Minimum RTT turn-off time (t_{AOF}min) is the point in time when the device starts to turn off the ODT resistance. Maximum RTT turn off time (t_{AOF}max) is the point in time when the on-die termination has reached high impedance. Both are measured from ODTLoff.

When ODT is asserted, it must remain high until ODTH4 is satisfied. If a Write command is registered by the SDRAM with ODT high, then ODT must remain high until ODTH4 (BL = 4) or ODTH8 (BL = 8) after the Write command (see Figure 78). ODTH4 and ODTH8 are measured from ODT registered high to ODT registered low or from the registration of a Write command until ODT is registered low.

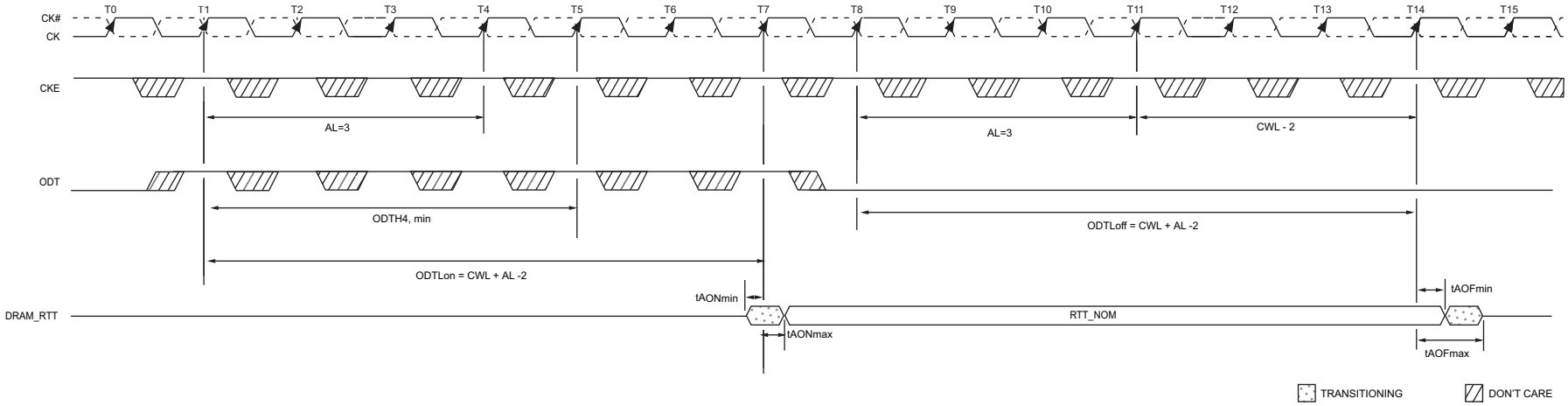


Figure 77 — Synchronous ODT Timing Example for AL = 3; CWL = 5; ODTLon = AL + CWL - 2 = 6.0; ODTLoff = AL + CWL - 2 = 6

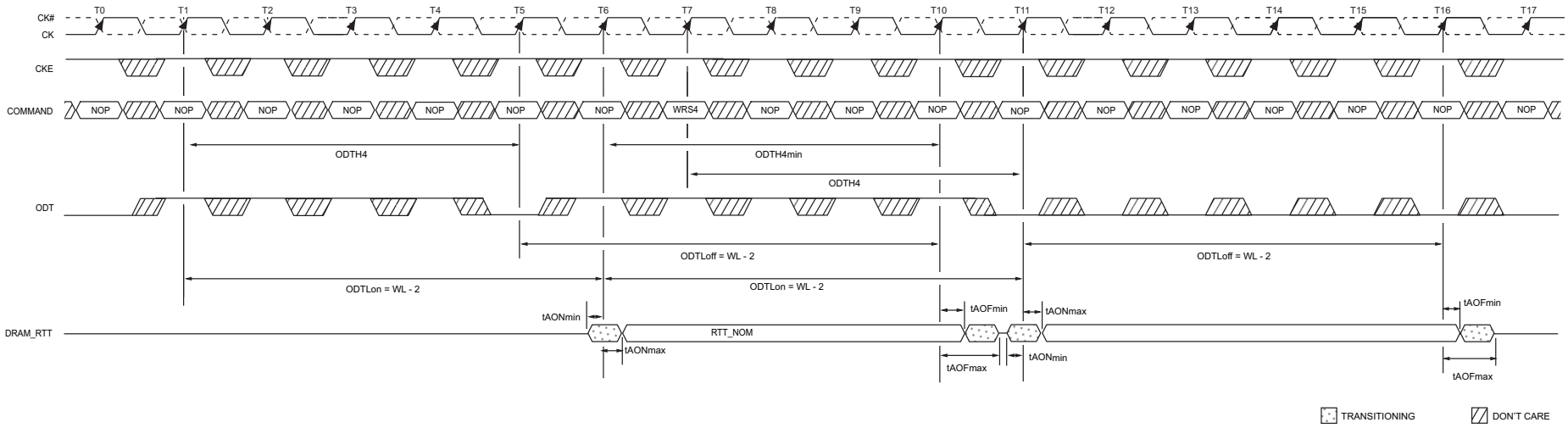


Figure 78 — Synchronous ODT example with BL = 4, WL = 7.

ODT must be held high for at least ODTH4 after assertion (T1); ODT must be kept high ODTH4 (BL = 4) or ODTH8 (BL = 8) after Write command (T7). ODTH is measured from ODT first registered high to ODT first registered low, or from registration of Write command with ODT high to ODT registered low. Note that although ODTH4 is satisfied from ODT registered high at T6 ,ODT must not go low before T11 as ODTH4 must also be satisfied from the registration of the Write command at T7.

5.2.3 ODT during Reads

As the DDR3 SDRAM can not terminate and drive at the same time, RTT must be disabled at least half a clock cycle before the read preamble by driving the ODT pin low appropriately. RTT may not be enabled until the end of the post-amble as shown in the example below. As shown in Figure 79 below, at cycle T15, DRAM turns on the termination when it stops driving, which is determined by tHZ. If DRAM stops driving early (i.e., tHZ is early), then tAONmin timing may apply. If DRAM stops driving late (i.e., tHZ is late), then DRAM complies with tAONmax timing. Note that ODT may be disabled earlier before the Read and enabled later after the Read than shown in this example in Figure 79.

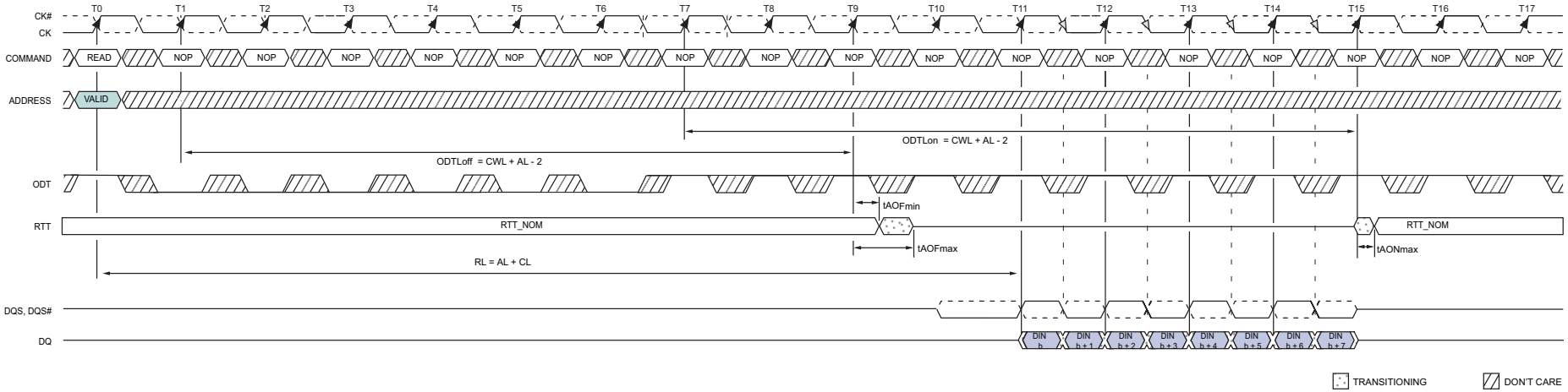


Figure 79 — ODT must be disabled externally during Reads by driving ODT low. (example: CL = 6; AL = CL - 1 = 5; RL = AL + CL = 11; CWL = 5; ODTLon = CWL + AL - 2 = 8; ODTLoff = CWL + AL - 2 = 8)

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5.3 Dynamic ODT

In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the DDR3 SDRAM can be changed without issuing an MRS command. This requirement is supported by the "Dynamic ODT" feature as described as follows:

5.3.1 Functional Description:

The Dynamic ODT Mode is enabled if bit (A9) or (A10) of MR2 is set to '1'. The function is described as follows:

- Two RTT values are available: RTT_Nom and RTT_WR.
  - The value for RTT_Nom is preselected via bits A[9,6,2] in MR1.
  - The value for RTT_WR is preselected via bits A[10,9] in MR2.
- During operation without write commands, the termination is controlled as follows:
  - Nominal termination strength RTT_Nom is selected.
  - Termination on/off timing is controlled via ODT pin and latencies ODTLon and ODTLoff.
- When a write command (WR, WRA, WRS4, WRS8, WRAS4, WRAS8) is registered, and if Dynamic ODT is enabled, the termination is controlled as follows:
  - A latency ODTLcnw after the write command, termination strength RTT_WR is selected.
  - A latency ODTLcwn8 (for BL8, fixed by MRS or selected OTF) or ODTLcwn4 (for BC4, fixed by MRS or selected OTF) after the write command, termination strength RTT_Nom is selected.
  - Termination on/off timing is controlled via ODT pin and ODTLon, ODTLoff.

Table 17 shows latencies and timing parameters which are relevant for the on-die termination control in Dynamic ODT mode.

The dynamic ODT feature is not supported at DLL-off mode. User must use MRS command to set Rtt_WR, MR2{A10, A9}={0,0}, to disable Dynamic ODT externally.

When ODT is asserted, it must remain high until ODTH4 is satisfied. If a Write command is registered by the SDRAM with ODT high, then ODT must remain high until ODTH4 (BL = 4) or ODTH8 (BL = 8) after the Write command (see Figure 78). ODTH4 and ODTH8 are measured from ODT registered high to ODT registered low or from the registration of a Write command until ODT is registered low.

Table 17 — Latencies and timing parameters relevant for Dynamic ODT

Name and Description	Abbr.	Defined from	Defined to	Definition for all DDR3 speed bins	Unit
ODT turn-on Latency	ODTLon	registering external ODT signal high	turning termination on	ODTLon = WL – 2	t_{CK}
ODT turn-off Latency	ODTLoff	registering external ODT signal low	turning termination off	ODTLoff = WL – 2	t_{CK}
ODT Latency for changing from RTT_Nom to RTT_WR	ODTLcnw	registering external write command	change RTT strength from RTT_Nom to RTT_WR	ODTLcnw = WL – 2	t_{CK}
ODT Latency for change from RTT_WR to RTT_Nom (BL = 4)	ODTLcwn4	registering external write command	change RTT strength from RTT_WR to RTT_Nom	ODTLcwn4 = 4 + ODTLoff	t_{CK}
ODT Latency for change from RTT_WR to RTT_Nom (BL = 8)	ODTLcwn8	registering external write command	change RTT strength from RTT_WR to RTT_Nom	ODTLcwn8 = 6 + ODTLoff	tCK(avg)

5.3 Dynamic ODT (Cont'd)
5.3.1 Functional Description (Cont'd)

Table 17 — Latencies and timing parameters relevant for Dynamic ODT (Cont'd)

Name and Description	Abbr.	Defined from	Defined to	Definition for all DDR3 speed bins	Unit
minimum ODT high time after ODT assertion	ODTH4	registering ODT high	ODT registered low	ODTH4 = 4	tCK(avg)
minimum ODT high time after Write (BL = 4)	ODTH4	registering Write with ODT high	ODT registered low	ODTH4 = 4	tCK(avg)
minimum ODT high time after Write (BL = 8)	ODTH8	registering Write with ODT high	ODT registered low	ODTH8 = 6	tCK(avg)
RTT change skew	t_{ADC}	ODTLcnw ODTLcwn	RTT valid	t_{ADC}(min) = 0.3 * tCK(avg) t_{ADC}(max) = 0.7 * tCK(avg)	tCK(avg)

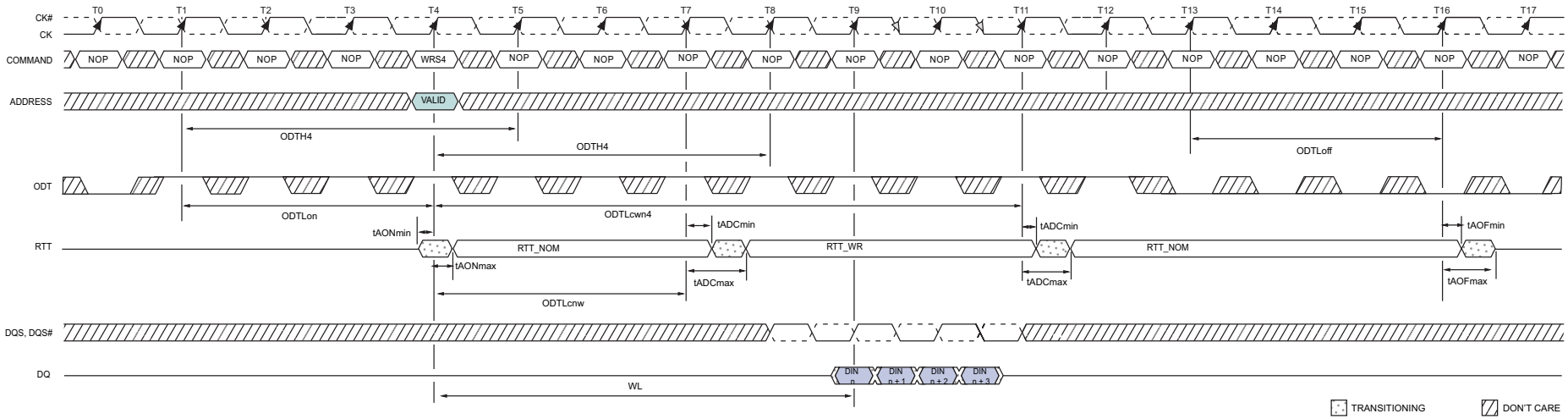
NOTE: tAOF,nom and tADC,nom are 0.5 tCK (effectively adding half a clock cycle to ODTLoff, ODTcnw and ODTLcwn)

5.3.2 ODT Timing Diagrams

The following pages provide exemplary timing diagrams as described in Table 18:

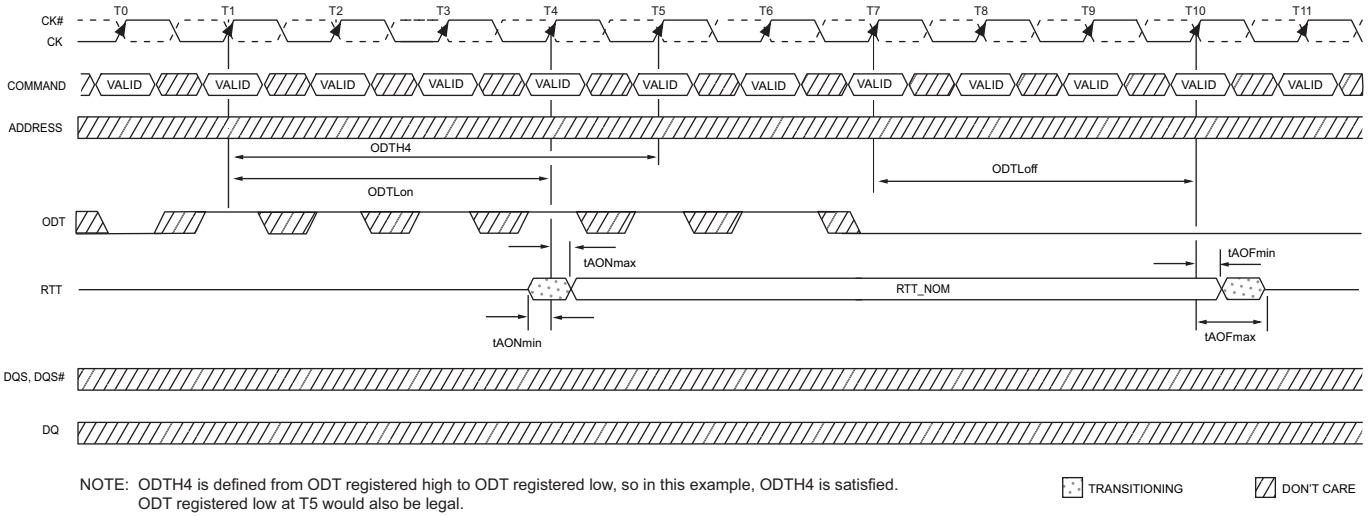
Table 18 — Timing Diagrams for "Dynamic ODT"

Figure and Page	Description
Figure 80 on page 98	Figure 80, Dynamic ODT: Behavior with ODT being asserted before and after the write.
Figure 81 on page 98	Figure 81, Dynamic ODT: Behavior without write command, AL = 0, CWL = 5.
Figure 82 on page 99	Figure 82, Dynamic ODT: Behavior with ODT pin being asserted together with write command for a duration of 6 clock cycles.
Figure 83 on page 100	Figure 83, Dynamic ODT: Behavior with ODT pin being asserted together with write command for a duration of 6 clock cycles, example for BC4 (via MRS or OTF), AL = 0, CWL = 5.
Figure 84 on page 101	Figure 84, Dynamic ODT: Behavior with ODT pin being asserted together with write command for a duration of 4 clock cycles.



NOTE: Example for BC4 (via MRS or OTF), AL = 0, CWL = 5. ODTH4 applies to first registering ODT high and to the registration of the Write command. In this example, ODTH4 would be satisfied if ODT went low at T8 (4 clocks after the Write command).

Figure 80 — Dynamic ODT: Behavior with ODT being asserted before and after the write



NOTE: ODTH4 is defined from ODT registered high to ODT registered low, so in this example, ODTH4 is satisfied. ODT registered low at T5 would also be legal.

Figure 81 — Dynamic ODT: Behavior without write command, AL = 0, CWL = 5

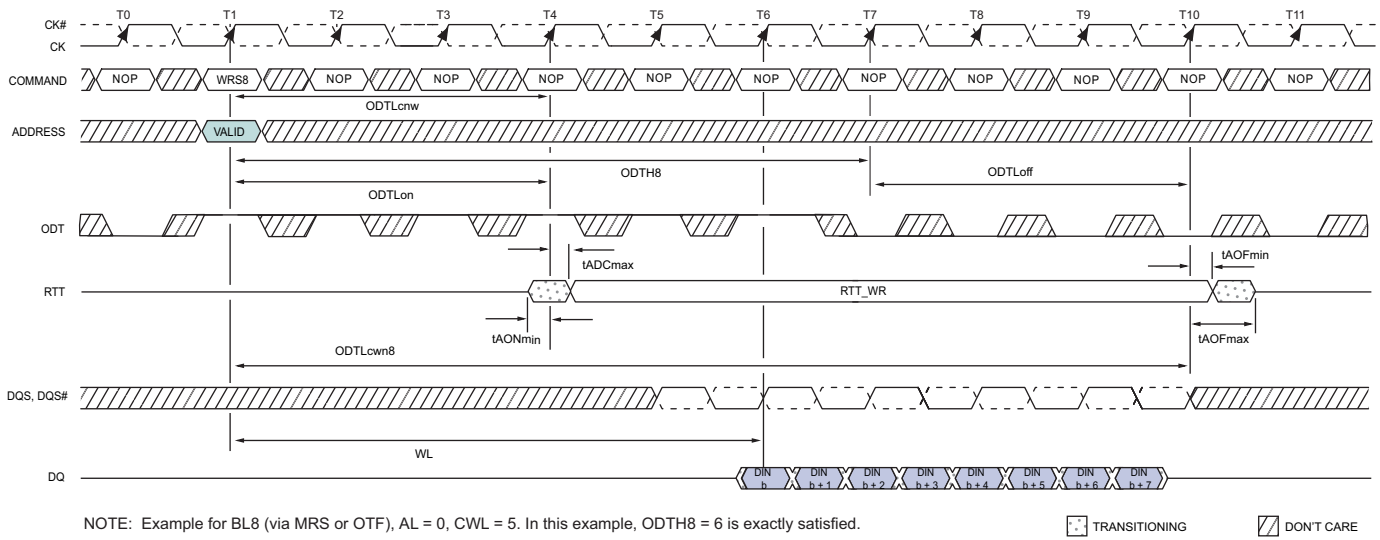


Figure 82 — Dynamic ODT: Behavior with ODT pin being asserted together with write command for a duration of 6 clock cycles

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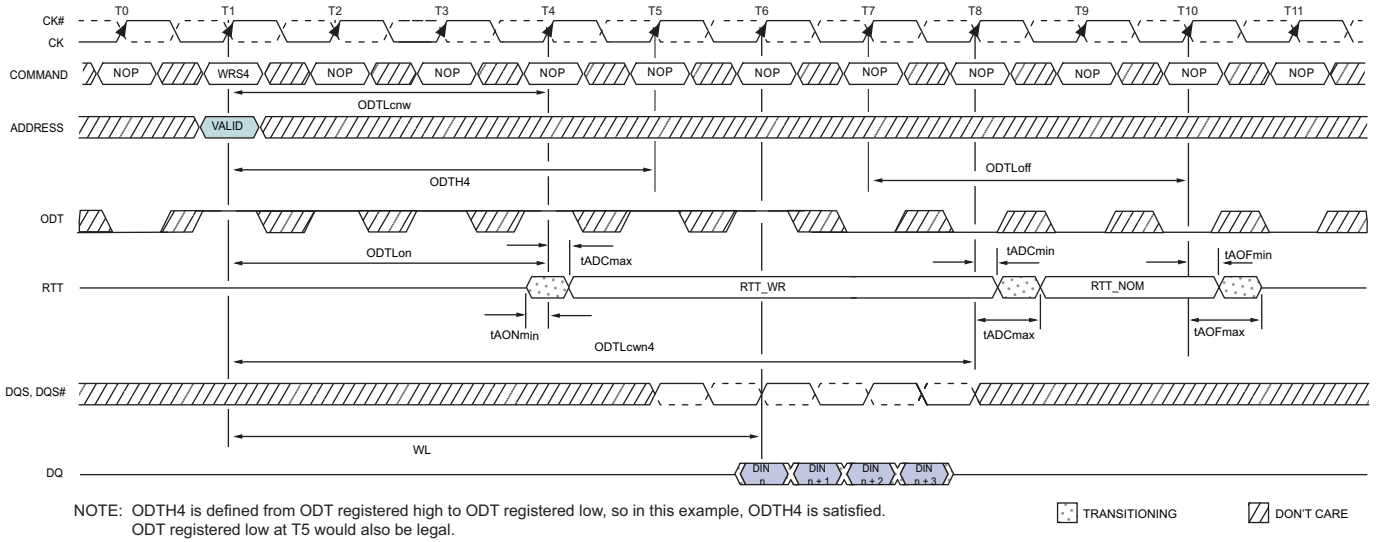

Figure 83 — Dynamic ODT: Behavior with ODT pin being asserted together with write command for a duration of 6 clock cycles, example for BC4 (via MRS or OTF), AL = 0, CWL = 5.

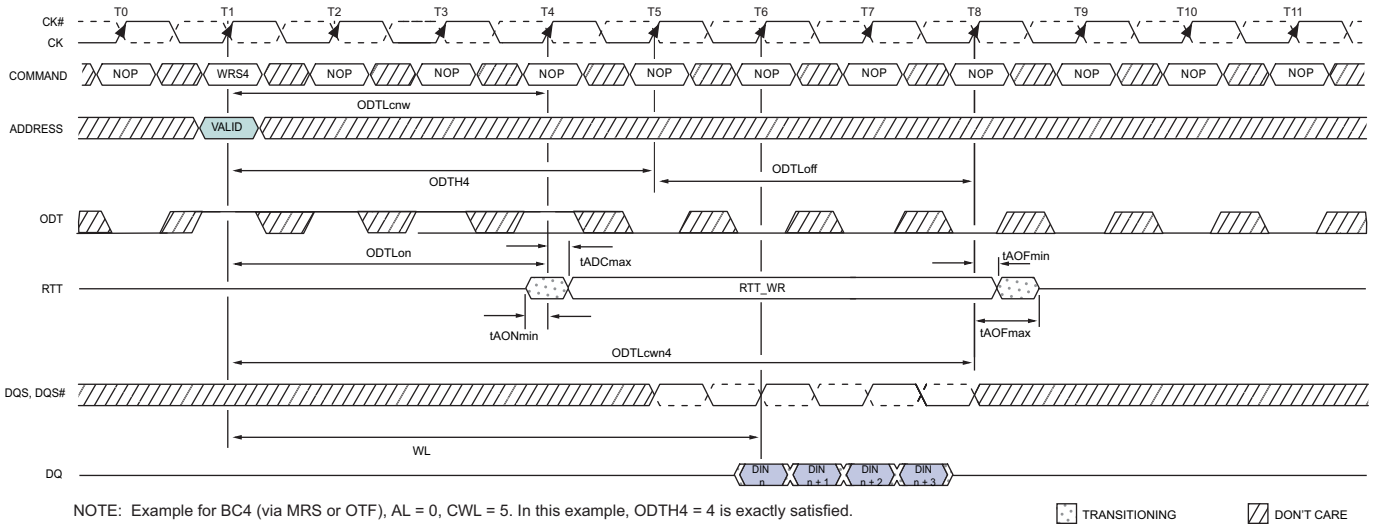

Figure 84 — Dynamic ODT: Behavior with ODT pin being asserted together with write command for a duration of 4 clock cycles

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5.4 Asynchronous ODT Mode

Asynchronous ODT mode is selected when DRAM runs in DLLon mode, but DLL is temporarily disabled (i.e. frozen) in precharge power-down (by MR0 bit A12). Based on the power down mode definitions, this is currently (comment: update editorially after everything is set and done...): Precharge power down mode if DLL is disabled during precharge power down by MR0 bit A12.

In asynchronous ODT timing mode, internal ODT command is NOT delayed by Additive Latency (AL) relative to the external ODT command.

In asynchronous ODT mode, the following timing parameters apply (see Figure 85): $t_{AONPD,min,max}$, $t_{AOFPD,min,max}$.

Minimum RTT turn-on time (t_{AONPD}min) is the point in time when the device termination circuit leaves high impedance state and ODT resistance begins to turn on. Maximum RTT turn on time (t_{AONPD}max) is the point in time when the ODT resistance is fully on.

t_{AONPD}min and t_{AONPD}max are measured from ODT being sampled high.

Minimum RTT turn-off time (t_{AOFPD}min) is the point in time when the devices termination circuit starts to turn off the ODT resistance. Maximum ODT turn off time (t_{AOFPD}max) is the point in time when the on-die termination has reached high impedance. t_{AOFPD}min and t_{AOFPD}max are measured from ODT being sampled low.

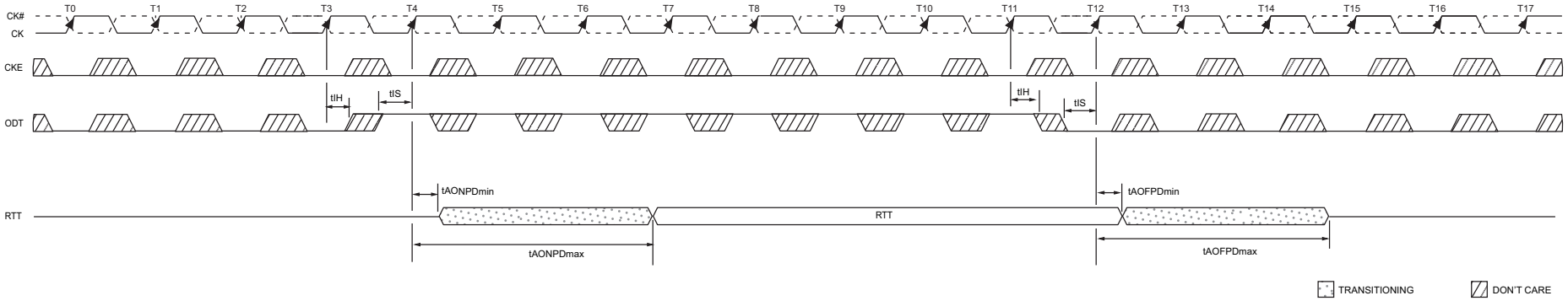

Figure 85 — Asynchronous ODT Timings on DDR3 SDRAM with fast ODT transition: AL is ignored

In Precharge Power Down, ODT receiver remains active, however no Read or Write command can be issued, as the respective ADD/CMD receivers may be disabled.

Table 19 — Asynchronous ODT Timing Parameters for all Speed Bins

Symbol	Description	min	max	Unit
t_{AONPD}	Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	2	8.5	ns
t_{AOFPD}	Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	2	8.5	ns

5 On-Die Termination (ODT) (Cont'd)
5.4 Asynchronous ODT Mode (Cont'd)

5.4.1 Synchronous to Asynchronous ODT Mode Transitions

Table 20 — ODT timing parameters for Power Down (with DLL frozen) entry and exit transition period

Description	min	max
ODT to RTT turn-on delay	min{ ODTLon * tCK + tAONmin; tAONPDmin }	max{ ODTLon * tCK + tAONmax; tAONPDmax }
	min{ (WL - 2) * tCK + tAONmin; tAONPDmin }	max{ (WL - 2) * tCK + tAONmax; tAONPDmax }
ODT to RTT turn-off delay	min{ ODTLoff * tCK +tAOFmin; tAOFPDmin }	max{ ODTLoff * tCK + tAOFmax; tAOFPDmax }
	min{ (WL - 2) * tCK +tAOFmin; tAOFPDmin }	max{ (WL - 2) * tCK + tAOFmax; tAOFPDmax }
tANPD	WL -1	

5.4.2 Synchronous to Asynchronous ODT Mode Transition during Power-Down Entry

If DLL is selected to be frozen in Precharge Power Down Mode by the setting of bit A12 in MR0 to "0", there is a transition period around power down entry, where the DDR3 SDRAM may show either synchronous or asynchronous ODT behavior.

The transition period is defined by the parameters tANPD and tCPDED(min). tANPD is equal to (WL -1) and is counted backwards in time from the clock cycle where CKE is first registered low. tCPDED(min) starts with the clock cycle where CKE is first registered low. The transition period begins with the starting point of tANPD and terminates at the end point of tCPDED(min), as shown in Figure 86. If there is a Refresh command in progress while CKE goes low, then the transition period ends at the later one of tRFC(min) after the Refresh command and the end point of tCPDED(min), as shown in Figure 87. Please note that the actual starting point at tANPD is excluded from the transition period, and the actual end points at tCPDED(min) and tRFC(min), respectively, are included in the transition period.

ODT assertion during the transition period may result in an RTT change as early as the smaller of t_{AONPD}min and (ODTLon*t_{CK} + t_{AON}min) and as late as the larger of t_{AONPD}max and (ODTLon*t_{CK} + t_{AON}max). ODT de-assertion during the transition period may result in an RTT change as early as the smaller of t_{AOFPD}min and (ODTLoff*t_{CK} + t_{AOF}min) and as late as the larger of t_{AOFPD}max and (ODTLoff*t_{CK} + t_{AOF}max). See Figure 20 and Figure 86. Note that, if AL has a large value, the range where RTT is uncertain becomes quite large. Figure 86 shows the three different cases: ODT_A, synchronous behavior before tANPD; ODT_B has a state change during the transition period; ODT_C shows a state change after the transition period.

5.4 Asynchronous ODT Mode (Cont'd)
5.4.2 Synchronous to Asynchronous ODT Mode Transition during Power-Down Entry (Cont'd)

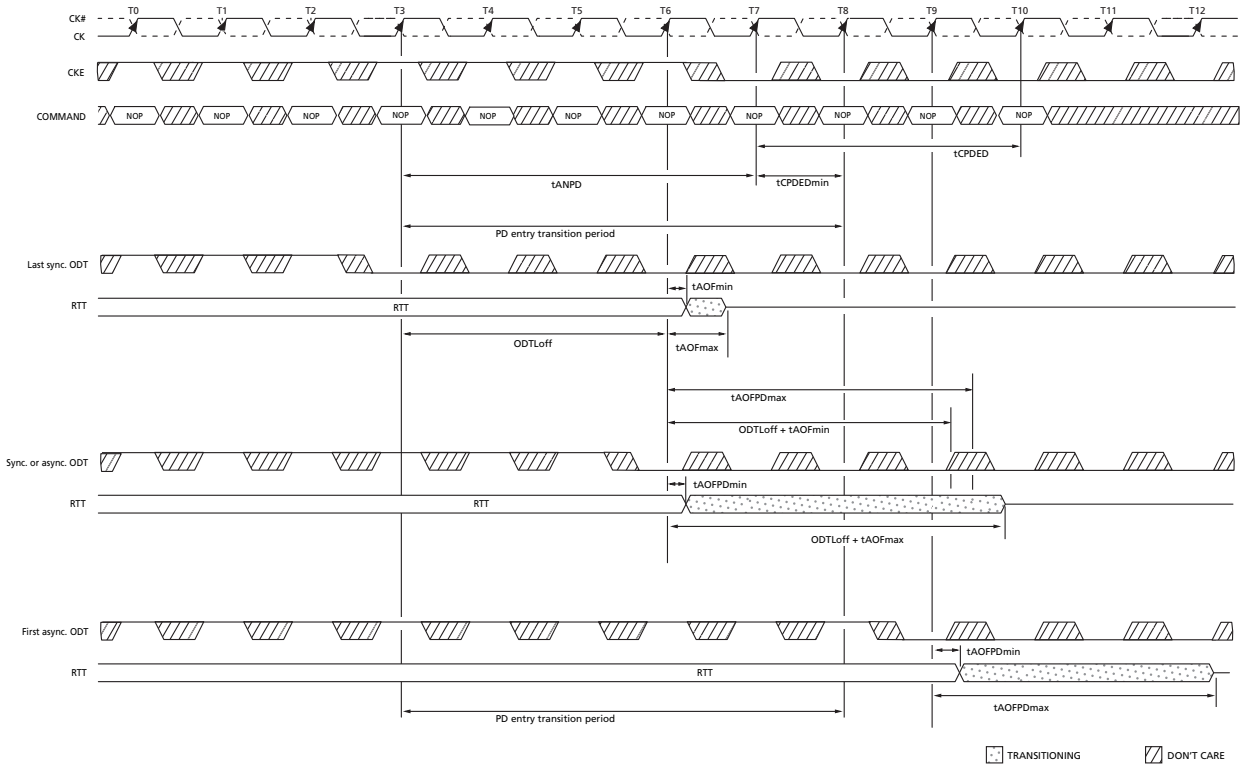

Figure 86 — Synchronous to asynchronous transition during Precharge Power Down (with DLL frozen) entry (AL = 0; CWL = 5; tANPD = WL - 1 = 4)

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5.4 Asynchronous ODT Mode (Cont'd)

5.4.2 Synchronous to Asynchronous ODT Mode Transition during Power-Down Entry (Cont'd)

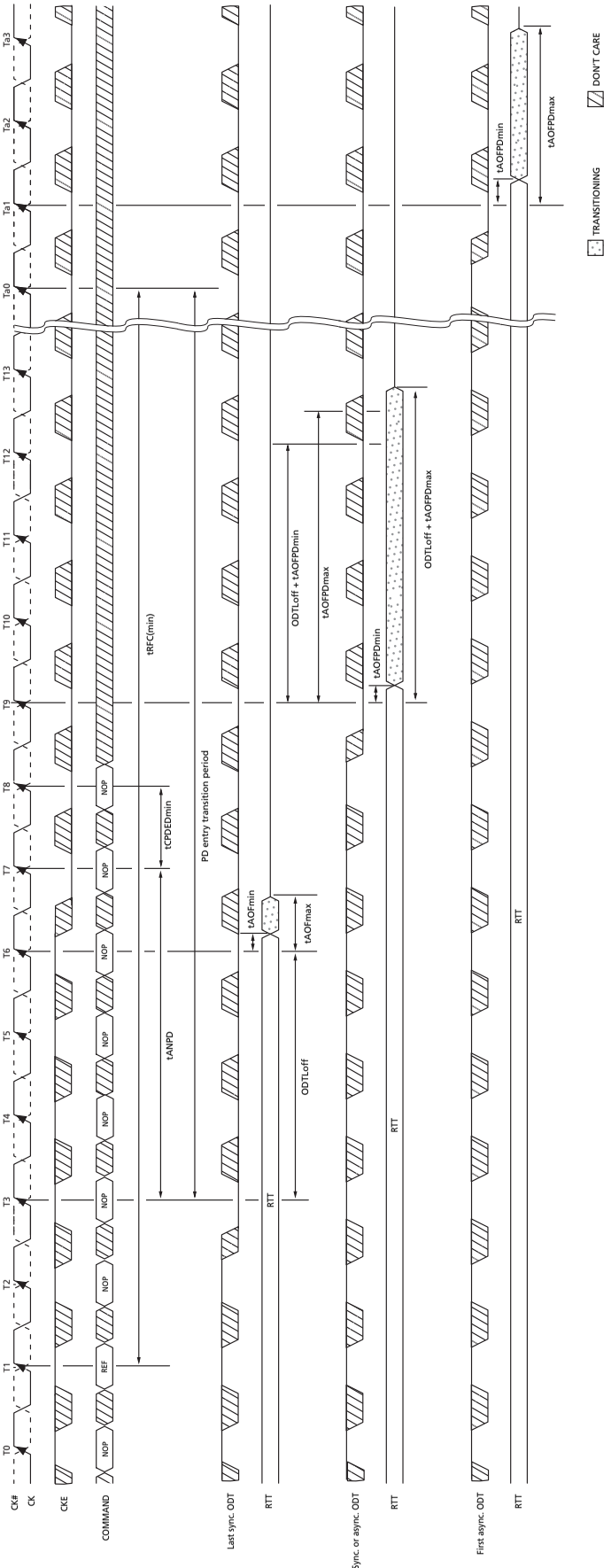

Figure 87 — Synchronous to asynchronous transition after Refresh command (AL = 0; CWL = 5; tANPD = WL - 1 = 4)

5.4.3 Asynchronous to Synchronous ODT Mode Transition during Power-Down Exit

If DLL is selected to be frozen in Precharge Power Down Mode by the setting of bit A12 in MR0 to "0", there is also a transition period around power down exit, where either synchronous or asynchronous response to a change in ODT must be expected from the DDR3 SDRAM.

This transition period starts tANPD before CKE is first registered high, and ends tXPDLL after CKE is first registered high. tANPD is equal to (WL - 1) and is counted (backwards) from the clock cycle where CKE is first registered high.

ODT assertion during the transition period may result in an RTT change as early as the smaller of t_{AONPD}min and (ODTLon*t_{CK} + t_{AON}min) and as late as the larger of t_{AONPD}max and (ODTLon*t_{CK} + t_{AON}max). ODT de-assertion during the transition period may result in an RTT change as early as the smaller of t_{AOFPD}min and (ODTLoff*t_{CK} + t_{AOF}min) and as late as the larger of t_{AOFPD}max and (ODTLoff*t_{CK} + t_{AOF}max). See Table 20.

Note that, if AL has a large value, the range where RTT is uncertain becomes quite large. Figure 88 shows the three different cases: ODT_C, asynchronous response before t_{ANPD}; ODT_B has a state change of ODT during the transition period; ODT_A shows a state change of ODT after the transition period with synchronous response.

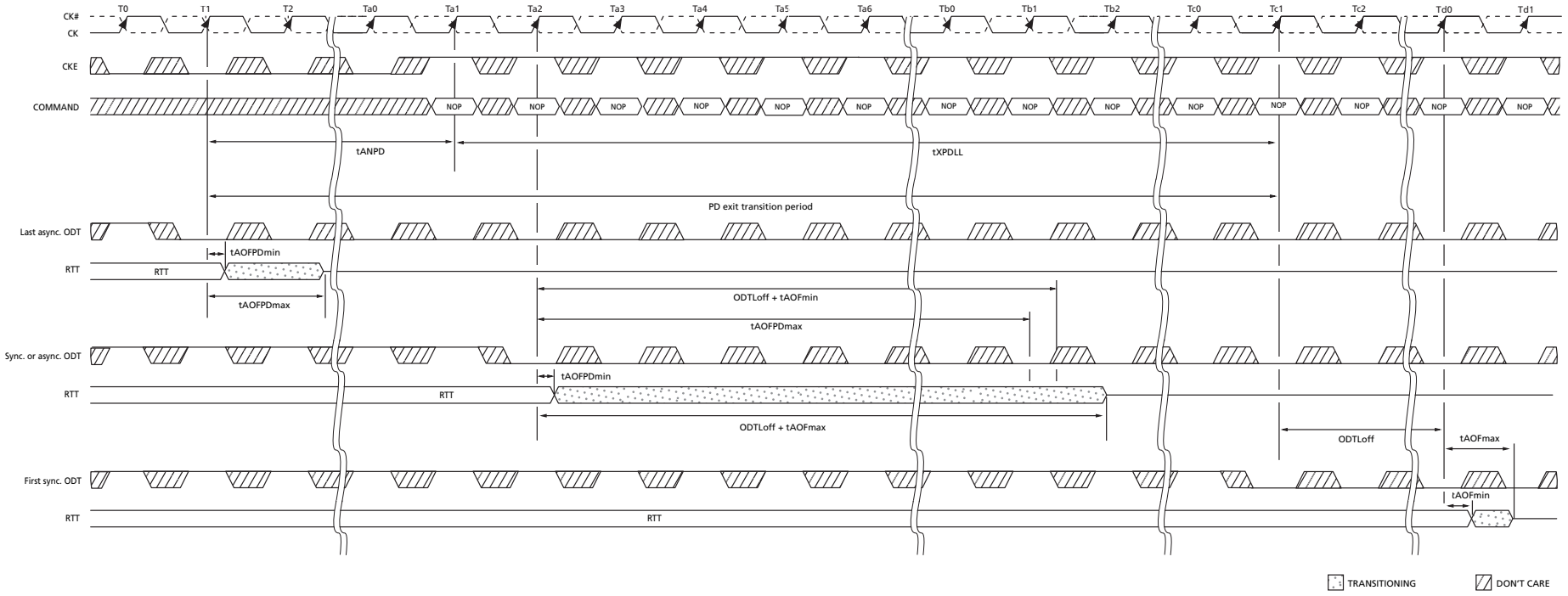

Figure 88 — Asynchronous to synchronous transition during Precharge Power Down (with DLL frozen) exit (CL = 6; AL = CL - 1; CWL = 5; tANPD = WL - 1 = 9)

5.4.4 Asynchronous to Synchronous ODT Mode during short CKE high and short CKE low periods

If the total time in Precharge Power Down state or Idle state is very short, the transition periods for PD entry and PD exit may overlap (see Figure 89). In this case, the response of the DDR3 SDRAMs RTT to a change in ODT state at the input may be synchronous OR asynchronous from the start of the PD entry transition period to the end of the PD exit transition period (even if the entry period ends later than the exit period).

If the total time in Idle state is very short, the transition periods for PD exit and PD entry may overlap. In this case the response of the DDR3 SDRAMs RTT to a change in ODT state at the input may be synchronous OR asynchronous from the start of the PD exit transition period to the end of the PD entry transition period. Note that in the bottom part of Figure 89 it is assumed that there was no Refresh command in progress when Idle state was entered.

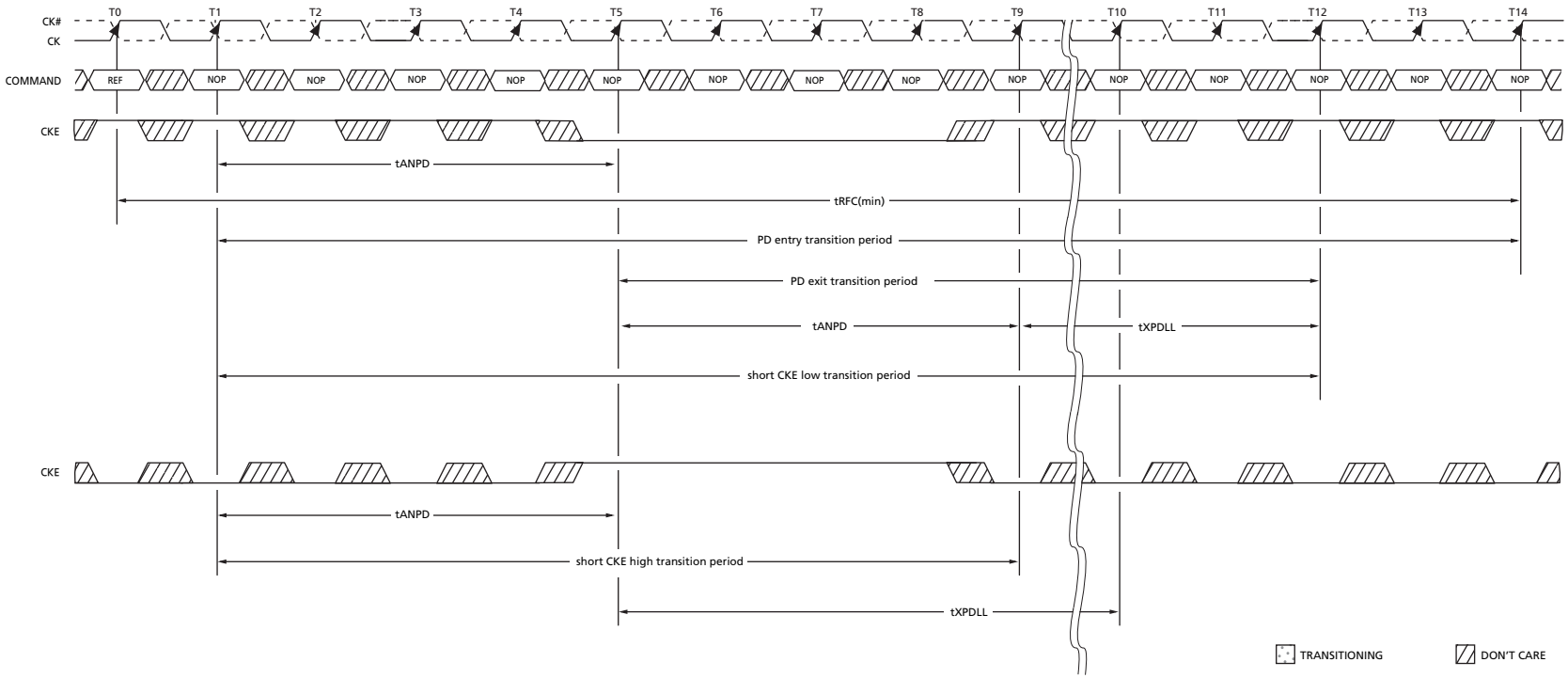

Figure 89 — Transition period for short CKE cycles, entry and exit period overlapping (AL = 0, WL = 5, tANPD = WL - 1 = 4)

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6 Absolute Maximum Ratings

6.1 Absolute Maximum DC Ratings

Table 21 — Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Notes
VDD	Voltage on VDD pin relative to Vss	-0.4 V ~ 1.975 V	V	1,3
VDDQ	Voltage on VDDQ pin relative to Vss	-0.4 V ~ 1.975 V	V	1,3
$V_{IN,}$ V_{OUT}	Voltage on any pin relative to Vss	-0.4 V ~ 1.975 V	V	1
T_{STG}	Storage Temperature	-55 to +100	°C	1,2

NOTE 1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability

NOTE 2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

NOTE 3. VDD and VDDQ must be within 300 mV of each other at all times;and VREF must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREF may be equal to or less than 300 mV

6.2 DRAM Component Operating Temperature Range

Table 22 — Temperature Range

Symbol	Parameter	Rating	Units	Notes
T_{OPER}	Normal Operating Temperature Range	0 to 85	^{o}C	1, 2
	Extended Temperature Range (Optional)	85 to 95	^{o}C	1, 3

NOTE 1. Operating Temperature T_{OPER} is the case surface temperature on the center / top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.

NOTE 2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 to 85 ^{o}C under all operating conditions

NOTE 3. Some applications require operation of the DRAM in the Extended Temperature Range between 85 ^{o}C and 95 ^{o}C case temperature. Full specifications are supported in this range, but the following additional conditions apply:

a Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 µs. It is also possible to specify a component with 1X refresh (tREFI to 7.8µs) in the Extended Temperature Range. Please refer to supplier data sheet and/or the DIMM SPD for option availability.

b If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0_b and MR2 A7 = 1_b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1_b and MR2 A7 = 0_b). Please refer to the supplier data sheet and/or the DIMM SPD for Auto Self-Refresh option availability, Extended Temperature Range support and tREFI requirements in the Extended Temperature Range.

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7 AC & DC Operating Conditions

7.1 Recommended DC Operating Conditions

Table 23 — Recommended DC Operating Conditions

Symbol	Parameter	Rating			Unit	Notes
		Min	Typ	Max		
V_{DD}	Supply Voltage	1.425	1.5	1.575	V	1, 2
V_{DDQ}	Supply Voltage for Output	1.425	1.5	1.575	V	1, 2

NOTE 1. Under all conditions VDDQ must be less than or equal to VDD.

NOTE 2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.

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8 AC and DC Input Measurement Levels

8.1 AC and DC Logic Input Levels for Single-Ended Signals

8.1.1 AC and DC Input Levels for Single-Ended Command and Address Signals

Table 24 — Single-Ended AC and DC Input Levels for Command and Address

Symbol	Parameter	DDR3-800/1066/1333/1600		Unit	Notes
		Min	Max		
VIH.CA(DC)	DC input logic high	Vref + 0.100	VDD	V	1
VIL.CA(DC)	DC input logic low	VSS	Vref - 0.100	V	1
VIH.CA(AC)	AC input logic high	Vref + 0.175	Note 2	V	1, 2
VIL.CA(AC)	AC input logic low	Note 2	Vref - 0.175	V	1, 2
VIH.CA(AC150)	AC input logic high	Vref + 0.150	Note 2	V	1, 2
VIL.CA(AC150)	AC input logic low	Note 2	Vref - 0.150	V	1, 2
$V_{RefCA(DC)}$	Reference Voltage for ADD, CMD inputs	0.49 * VDD	0.51 * VDD	V	3, 4

NOTE 1. For input only pins except RESET#. Vref = VrefCA(DC).

NOTE 2. See 9.6 “Overshoot and Undershoot Specifications” on page 125.

NOTE 3. The ac peak noise on V_{Ref} may not allow V_{Ref} to deviate from $V_{RefDQ(DC)}$ by more than +/-1% VDD (for reference: approx. +/- 15 mV).

NOTE 4. For reference: approx. VDD/2 +/- 15 mV.

8.1.2 AC and DC Input Levels for Single-Ended Data Signals

Table 25 — Single-Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	DDR3-800, DDR3-1066		DDR3-1333, DDR3-1600		Unit	Notes
		Min	Max				
VIH.DQ(DC)	DC input logic high	Vref + 0.100	VDD	Vref + 0.100	VDD	V	1
VIL.DQ(DC)	DC input logic low	VSS	Vref - 0.100	VSS	Vref - 0.100	V	1
VIH.DQ(AC)	AC input logic high	Vref + 0.175	Note 2	Vref + 0.150	Note 2	V	1, 2, 5
VIL.DQ(AC)	AC input logic low	Note 2	Vref - 0.175	Note 2	Vref - 0.150	V	1, 2, 5
$V_{RefDQ(DC)}$	Reference Voltage for DQ, DM inputs	0.49 * VDD	0.51 * VDD	0.49 * VDD	0.51 * VDD	V	3, 4

NOTE 1. For input only pins except RESET#. Vref = VrefDQ(DC).

NOTE 2. See 9.6 “Overshoot and Undershoot Specifications” on page 125.

NOTE 3. The ac peak noise on V_{Ref} may not allow V_{Ref} to deviate from $V_{RefDQ(DC)}$ by more than +/-1% VDD (for reference: approx. +/- 15 mV).

NOTE 4. For reference: approx. VDD/2 +/- 15 mV.

NOTE 5. Single-ended swing requirement for DQS, DQS# is 350 mV (peak to peak). Differential swing requirement for DQS - DQS# is 700 mV (peak to peak).

8.2 Vref Tolerances

The dc-tolerance limits and ac-noise limits for the reference voltages V_{RefCA} and V_{RefDQ} are illustrated in Figure 90. It shows a valid reference voltage $V_{Ref}(t)$ as a function of time. (V_{Ref} stands for V_{RefCA} and V_{RefDQ} likewise).

$V_{Ref}(DC)$ is the linear average of $V_{Ref}(t)$ over a very long period of time (e.g., 1 sec). This average has to meet the min/max requirements in Table 24. Furthermore $V_{Ref}(t)$ may temporarily deviate from $V_{Ref(DC)}$ by no more than +/- 1% VDD.

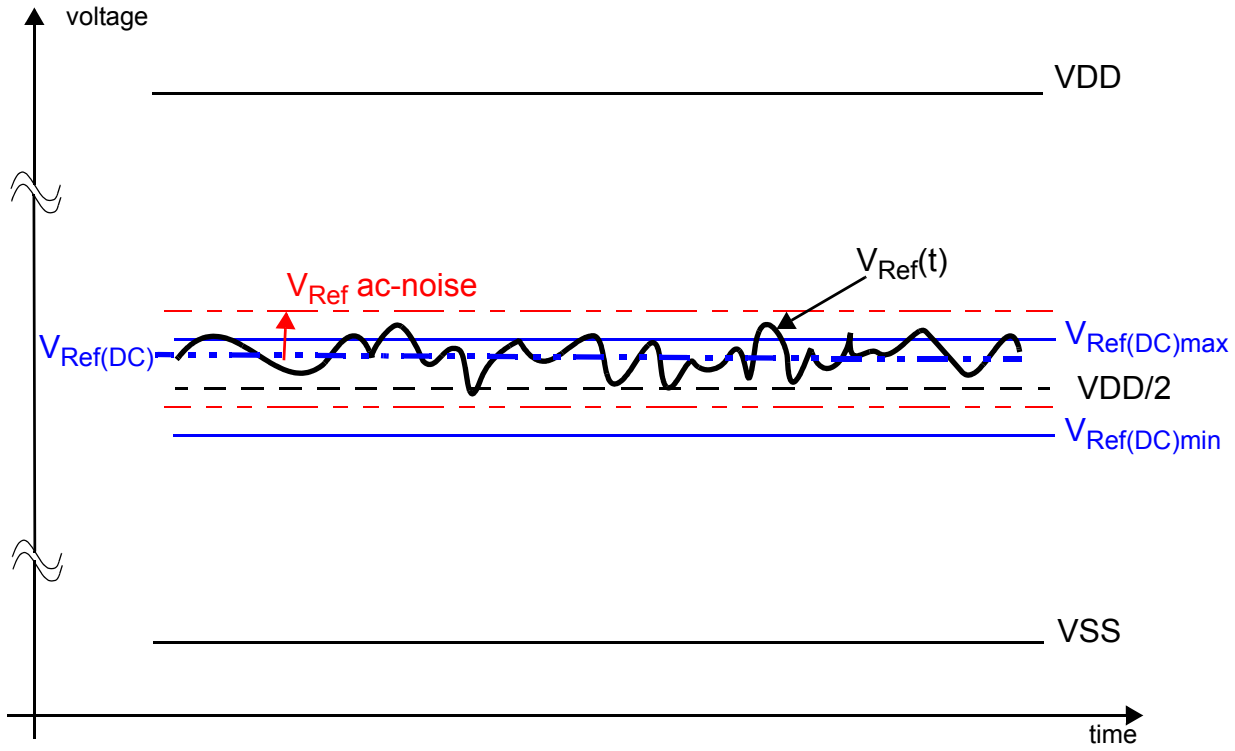

Figure 90 — Illustration of $V_{Ref(DC)}$ tolerance and V_{Ref} ac-noise limits

The voltage levels for setup and hold time measurements $V_{IH(AC)}$, $V_{IH(DC)}$, $V_{IL(AC)}$, and $V_{IL(DC)}$ are dependent on V_{Ref}.

"V_{Ref}" shall be understood as $V_{Ref(DC)}$, as defined in Figure 90.

This clarifies that dc-variations of V_{Ref} affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for $V_{Ref(DC)}$ deviations from the optimum position within the data-eye of the input signals.

This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with V_{Ref} ac-noise. Timing and voltage effects due to ac-noise on V_{Ref} up to the specified limit (+/-1% of VDD) are included in DRAM timings and their associated deratings.

8 AC and DC Input Measurement Levels (Cont'd)

8.3 AC and DC Logic Input Levels for Differential Signals

8.3.1 Differential signal definition

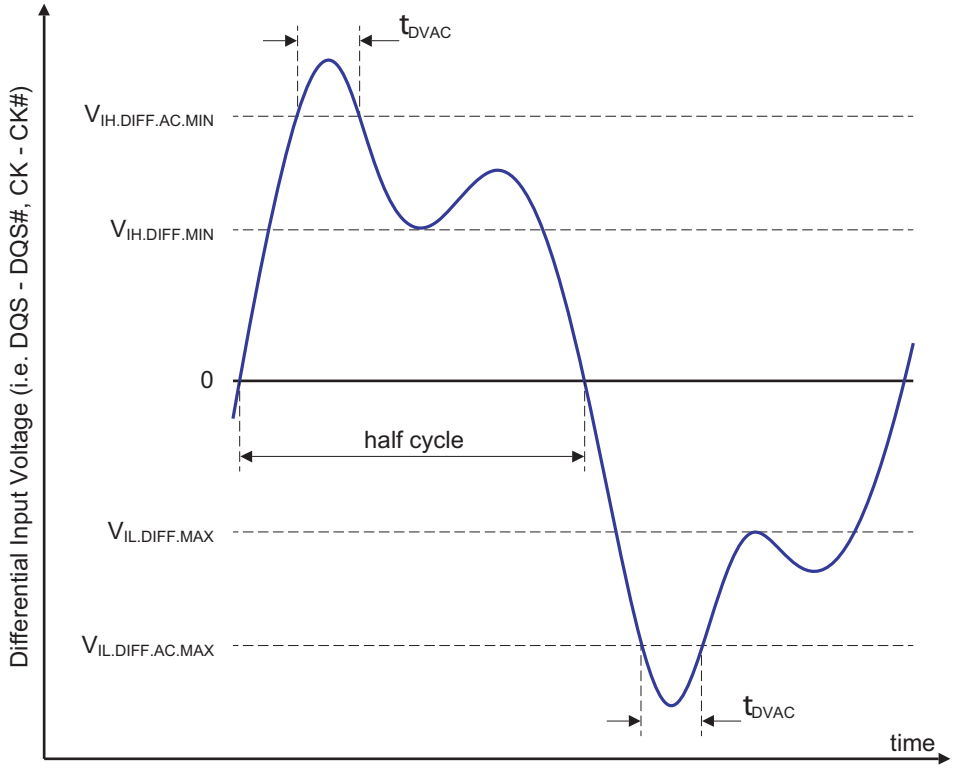

Figure 91 — Definition of differential ac-swing and "time above ac-level" t_{DVAC}

8.3.2 Differential swing requirements for clock (CK - CK#) and strobe (DQS - DQS#)

Table 26 — Differential AC and DC Input Levels

Symbol	Parameter	DDR3-800, 1066, 1333, & 1600		Unit	Notes
		Min	Max		
V_{IHdiff}	Differential input high	+ 0.200	note 3	V	1
V_{ILdiff}	Differential input logic low	Note 3	- 0.200	V	1
$V_{IHdiff(ac)}$	Differential input high ac	2 x (VIH(ac) - Vref)	Note 3	V	2
$V_{ILdiff(ac)}$	Differential input low ac	note 3	2 x (Vref - VIL(ac))	V	2

NOTE 1. Used to define a differential signal slew-rate.

NOTE 2. For CK - CK# use VIH/VIL(ac) of ADD/CMD and VREFCA; for DQS - DQS#, DQSL, DQSL#, DQSU , DQSU# use VIH/VIL(ac) of DQs and VREFDQ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.

NOTE 3. These values are not defined; however, the single-ended signals CK, CK#, DQS, DQS#, DQSL, DQSL#, DQSU, DQSU# need to be within the respective limits (VIH(dc) max, VIL(dc)min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to "Overshoot and Undershoot Specifications" on page 125

8.3 AC and DC Logic Input Levels for Differential Signals (Cont'd)
8.3.2 Differential swing requirements for clock (CK - CK#) and strobe (DQS - DQS#) (Cont'd)

Table 27 — Allowed time before ringback (tDVAC) for CK - CK# and DQS - DQS#

Slew Rate [V/ns]	tDVAC [ps] @ |VIH/Ldiff(ac)| = 350mV		tDVAC [ps] @ |VIH/Ldiff(ac)| = 300mV	
	min	max	min	max
> 4.0	75	-	175	-
4.0	57	-	170	-
3.0	50	-	167	-
2.0	38	-	163	-
1.8	34	-	162	-
1.6	29	-	161	-
1.4	22	-	159	-
1.2	13	-	155	-
1.0	0	-	150	-
< 1.0	0	-	150	-

8.3.3 Single-ended requirements for differential signals

Each individual component of a differential signal (CK, DQS, DQSL, DQSU, CK#, DQS#, DQSL#, or DQSU#) has also to comply with certain requirements for single-ended signals.

CK and CK# have to approximately reach VSEHmin / VSELmax (approximately equal to the ac-levels (VIH(ac) / VIL(ac)) for ADD/CMD signals) in every half-cycle.

DQS, DQSL, DQSU, DQS#, DQSL# have to reach VSEHmin / VSELmax (approximately the ac-levels (VIH(ac) / VIL(ac)) for DQ signals) in every half-cycle preceding and following a valid transition.

Note that the applicable ac-levels for ADD/CMD and DQ's might be different per speed-bin etc. E.g., if VIH150(ac)/VIL150(ac) is used for ADD/CMD signals, then these ac-levels apply also for the single-ended signals CK and CK#

8.3 AC and DC Logic Input Levels for Differential Signals (Cont'd)
8.3.3 Single-ended requirements for differential signals (Cont'd)

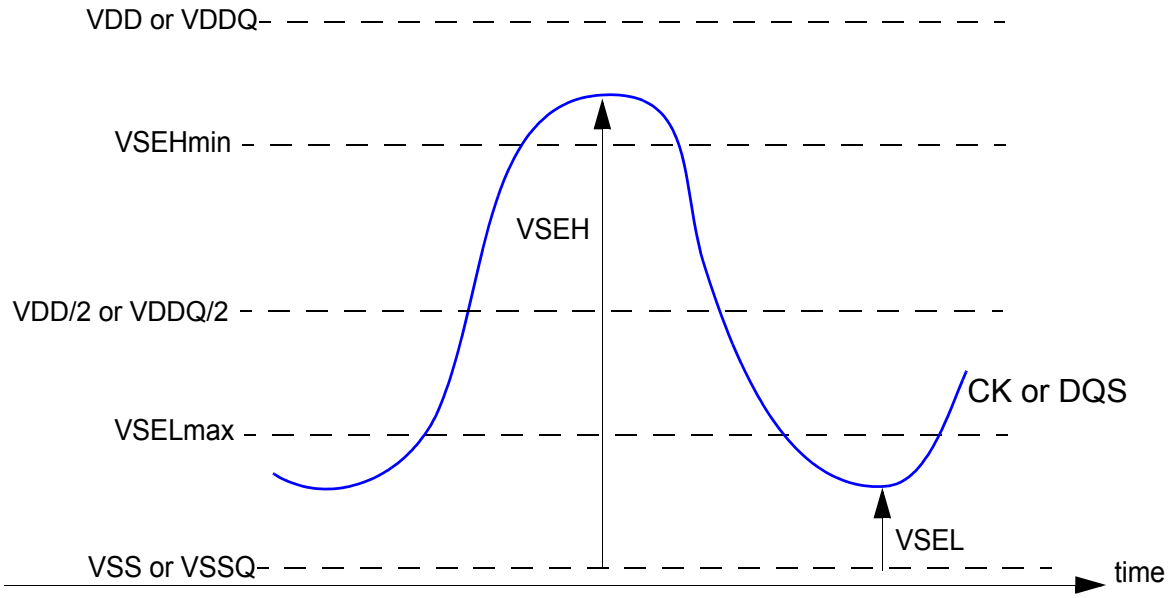

Figure 92 — Single-ended requirement for differential signals.

Note that, while ADD/CMD and DQ signal requirements are with respect to Vref, the single-ended components of differential signals have a requirement with respect to VDD / 2; this is nominally the same. The transition of single-ended signals through the ac-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach VSELmax, VSEHmin has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

Table 28 — Single-ended levels for CK, DQS, DQSL, DQSU, CK#, DQS#, DQSL# or DQSU#

Symbol	Parameter	DDR3-800, 1066, 1333, & 1600		Unit	Notes
		Min	Max		
VSEH	Single-ended high level for strobes	(VDD / 2) + 0.175	note 3	V	1, 2
	Single-ended high level for CK, CK#	(VDD / 2) + 0.175	note 3	V	1, 2
VSEL	Single-ended low level for strobes	note 3	(VDD / 2) - 0.175	V	1, 2
	Single-ended low level for CK, CK#	note 3	(VDD / 2) - 0.175	V	1, 2

NOTE 1. For CK, CK# use VIH/VIL(ac) of ADD/CMD; for strobes (DQS, DQS#, DQSL, DQSL#, DQSU, DQSU#) use VIH/VIL(ac) of DQs.

NOTE 2. VIH(ac)/VIL(ac) for DQs is based on VREFDQ; VIH(ac)/VIL(ac) for ADD/CMD is based on VREFCA; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here

NOTE 3. These values are not defined, however the single-ended signals CK, CK#, DQS, DQS#, DQSL, DQSL#, DQSU, DQSU# need to be within the respective limits (VIH(dc) max, VIL(dc)min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to "Overshoot and Undershoot Specifications" on page 125

8.4 Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK, CK# and DQS, DQS#) must meet the require-

8 AC and DC Input Measurement Levels (Cont'd)
8.4 Differential Input Cross Point Voltage (Cont'd)

ments in Table 29. The differential input cross point voltage V_{IX} is measured from the actual cross point of true and complement signals to the midlevel between of VDD and VSS.

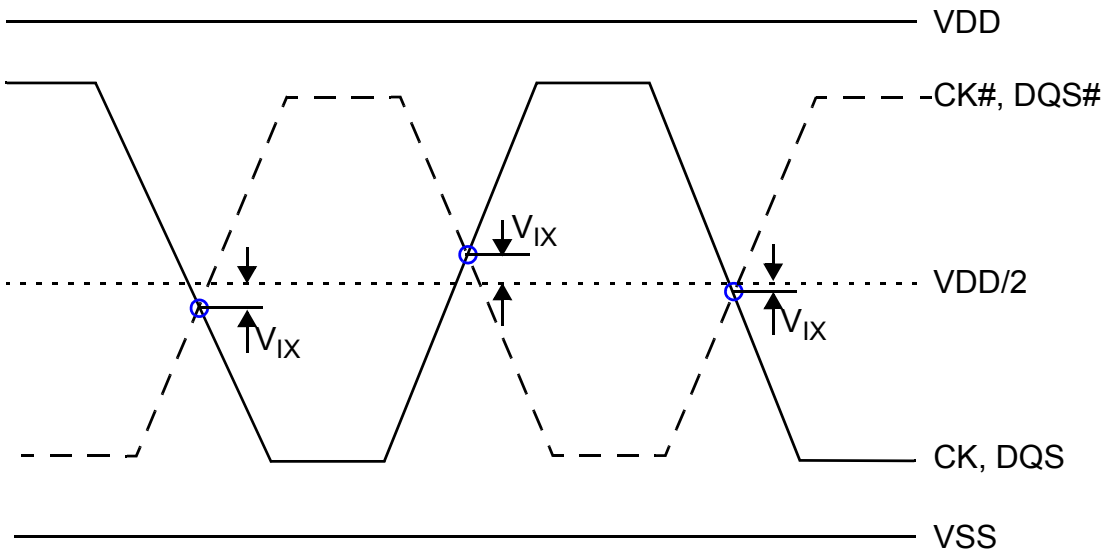

Figure 93 — Vix Definition

Table 29 — Cross point voltage for differential input signals (CK, DQS)

Symbol	Parameter	DDR3-800, DDR3-1066, DDR3-1333, DDR3-1600		Unit	Notes
		Min	Max		
V_{IX}	Differential Input Cross Point Voltage relative to VDD/2 for CK, CK#	- 150	150	mV	
		- 175	175	mV	1
V_{IX}	Differential Input Cross Point Voltage relative to VDD/2 for DQS, DQS#	- 150	150	mV	

NOTE 1. Extended range for V_{ix} is only allowed for clock and if single-ended clock input signals CK and CK# are monotonic with a single-ended swing VSEL / VSEH of at least VDD/2 +/-250 mV, and when the differential slew rate of CK - CK# is larger than 3 V/ns.
Refer to Table 28 on page 117 for VSEL and VSEH standard values.

8.5 Slew Rate Definitions for Single-Ended Input Signals

See 13.3 "Address / Command Setup, Hold and Derating" on page 173 for single-ended slew rate definitions for address and command signals.

See 13.4 "Data Setup, Hold and Slew Rate Derating" on page 180 for single-ended slew rate definitions for data signals.

8.6 Slew Rate Definitions for Differential Input Signals

Input slew rate for differential signals (CK, CK# and DQS, DQS#) are defined and measured as shown in Table 30 and Figure 94.

Table 30 — Differential Input Slew Rate Definition

Description	Measured		Defined by
	from	to	
Differential input slew rate for rising edge (CK - CK# and DQS - DQS#).	$V_{ILdiffmax}$	$V_{IHdiffmin}$	$[V_{IHdiffmin} - V_{ILdiffmax}]$ / DeltaTRdiff
Differential input slew rate for falling edge (CK - CK# and DQS - DQS#).	$V_{IHdiffmin}$	$V_{ILdiffmax}$	$[V_{IHdiffmin} - V_{ILdiffmax}]$ / DeltaTFdiff
NOTE: The differential signal (i.e., CK - CK# and DQS - DQS#) must be linear between these thresholds.			

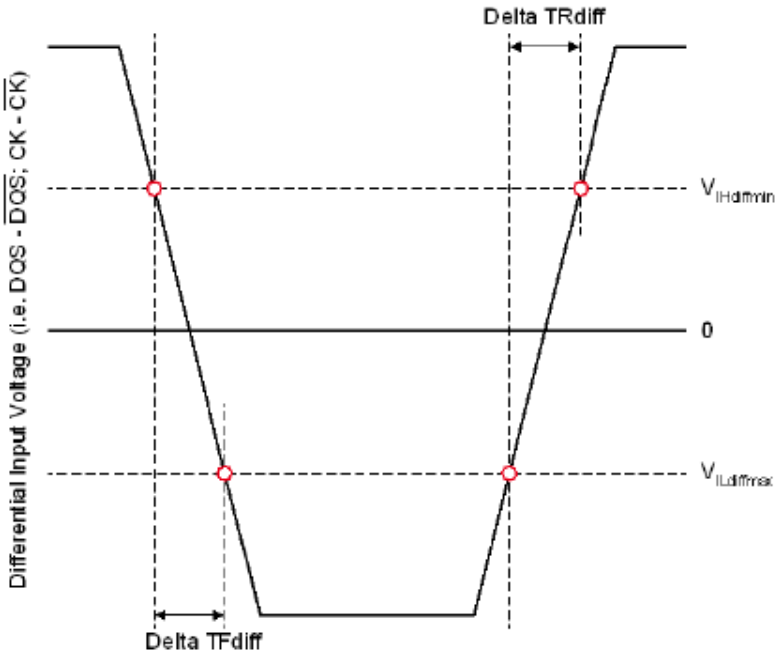

Figure 94 — Differential Input Slew Rate Definition for DQS, DQS# and CK, CK#

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9 AC and DC Output Measurement Levels

9.1 Single Ended AC and DC Output Levels

Table 31 shows the output levels used for measurements of single ended signals.

Table 31 — Single-ended AC and DC Output Levels

Symbol	Parameter	DDR3-800, 1066, 1333, and 1600	Unit	Notes
$V_{OH(DC)}$	DC output high measurement level (for IV curve linearity)	0.8 x V_{DDQ}	V	
$V_{OM(DC)}$	DC output mid measurement level (for IV curve linearity)	0.5 x V_{DDQ}	V	
$V_{OL(DC)}$	DC output low measurement level (for IV curve linearity)	0.2 x V_{DDQ}	V	
$V_{OH(AC)}$	AC output high measurement level (for output SR)	V_{TT} + 0.1 x V_{DDQ}	V	1
$V_{OL(AC)}$	AC output low measurement level (for output SR)	V_{TT} - 0.1 x V_{DDQ}	V	1
NOTE 1. The swing of ± 0.1 × V_{DDQ} is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40 Ω and an effective test load of 25 Ω to V_{TT} = V_{DDQ}/2.				

9.2 Differential AC and DC Output Levels

Table 32 shows the output levels used for measurements of differential signals.

Table 32 — Differential AC and DC Output Levels

Symbol	Parameter	DDR3-800, 1066, 1333, and 1600	Unit	Notes
$V_{OHdiff(AC)}$	AC differential output high measurement level (for output SR)	+ 0.2 x V_{DDQ}	V	1
$V_{OLdiff(AC)}$	AC differential output low measurement level (for output SR)	- 0.2 x V_{DDQ}	V	1
NOTE 1. The swing of ± 0.2 × V_{DDQ} is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40 Ω and an effective test load of 25 Ω to V_{TT} = V_{DDQ}/2 at each of the differential outputs.				

9 AC and DC Output Measurement Levels (Cont'd)

9.3 Single Ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$ for single ended signals as shown in Table 33 and Figure 95.

Table 33 — Single-ended Output Slew Rate Definition

Description	Measured		Defined by
	from	to	
Single-ended output slew rate for rising edge	$V_{OL(AC)}$	$V_{OH(AC)}$	$[V_{OH(AC)} - V_{OL(AC)}]$ / DeltaTRse
Single-ended output slew rate for falling edge	$V_{OH(AC)}$	$V_{OL(AC)}$	$[V_{OH(AC)} - V_{OL(AC)}]$ / DeltaTFse
NOTE: Output slew rate is verified by design and characterization, and may not be subject to production test.			

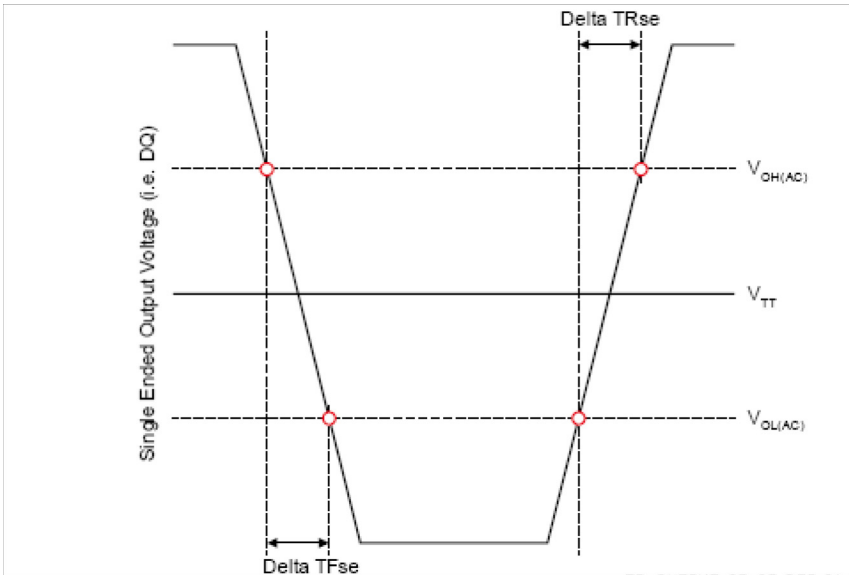

Figure 95 — Single Ended Output Slew Rate Definition

Table 34 — Output Slew Rate (single-ended)

		DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		Units
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	
Single-ended Output Slew Rate	SRQse	2.5	5	2.5	5	2.5	5	TBD	5	V/ns
Description: SR: Slew Rate Q: Query Output (like in DQ, which stands for Data-in, Query-Output) se: Single-ended Signals For Ron = RZQ/7 setting										

9 AC and DC Output Measurement Levels (Cont'd)

9.4 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLdiff(AC) and VOHdiff(AC) for differential signals as shown in Table 35 and Figure 96.

Table 35 — Differential Output Slew Rate Definition

Description	Measured		Defined by
	from	to	
Differential output slew rate for rising edge	$V_{OLdiff(AC)}$	$V_{OHdiff(AC)}$	$[V_{OHdiff(AC)} - V_{OLdiff(AC)}]$ / DeltaTRdiff
Differential output slew rate for falling edge	$V_{OHdiff(AC)}$	$V_{OLdiff(AC)}$	$[V_{OHdiff(AC)} - V_{OLdiff(AC)}]$ / DeltaTFdiff
NOTE: Output slew rate is verified by design and characterization, and may not be subject to production test.			

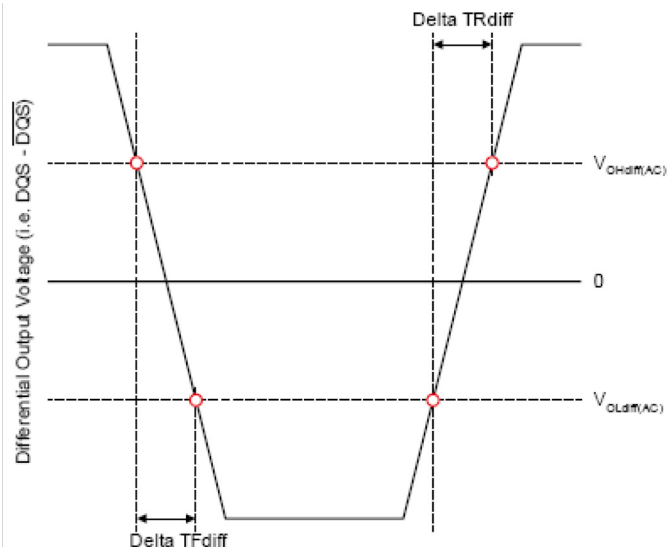

Figure 96 — Differential Output Slew Rate Definition

Table 36 — Differential Output Slew Rate

		DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		Units
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	
Differential Output Slew Rate	SRQdiff	5	10	5	10	5	10	TBD	10	V/ns
Description: SR: Slew Rate Q: Query Output (like in DQ, which stands for Data-in, Query-Output) diff: Differential Signals For Ron = RZQ/7 setting										

9.5 Reference Load for AC Timing and Output Slew Rate

Figure 97 represents the effective reference load of 25 ohms used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.

It is not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

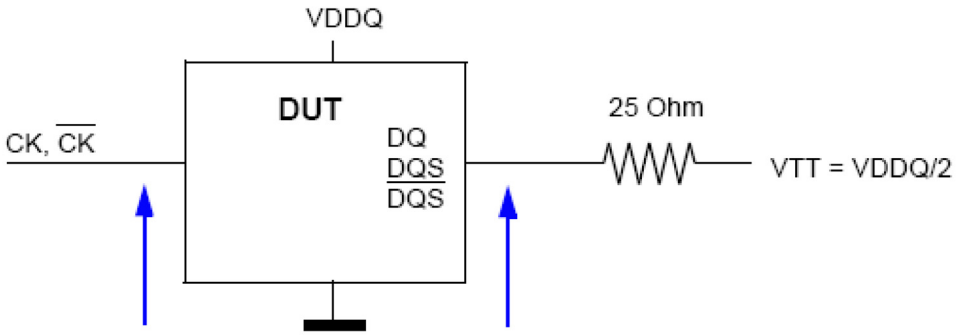

Figure 97 — Reference Load for AC Timing and Output Slew Rate

9 AC and DC Output Measurement Levels (Cont'd)

9.6 Overshoot and Undershoot Specifications

9.6.1 Address and Control Overshoot and Undershoot Specifications

Table 37 — AC Overshoot/Undershoot Specification for Address and Control Pins

	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	Units
Maximum peak amplitude allowed for overshoot area. (See Figure 98)	0.4	0.4	0.4	0.4	V
Maximum peak amplitude allowed for undershoot area. (See Figure 98)	0.4	0.4	0.4	0.4	V
Maximum overshoot area above VDD (See Figure 98)	0.67	0.5	0.4	0.33	V-ns
Maximum undershoot area below VSS (See Figure 98)	0.67	0.5	0.4	0.33	V-ns
(A0-A15, BA0-BA3, CS#, RAS#, CAS#, WE#, CKE, ODT)					

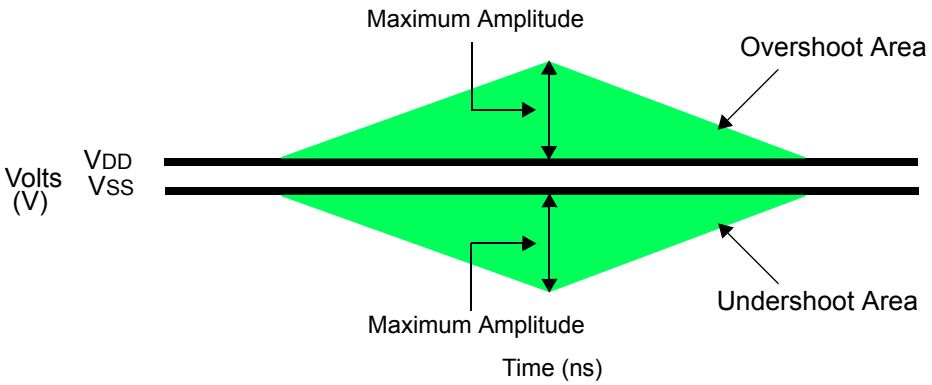

Figure 98 — Address and Control Overshoot and Undershoot Definition

9 AC and DC Output Measurement Levels (Cont'd)
9.6 Overshoot and Undershoot Specifications (Cont'd)

9.6.2 Clock, Data, Strobe and Mask Overshoot and Undershoot Specifications

Table 38 — AC Overshoot/Undershoot Specification for Clock, Data, Strobe and Mask

	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	Units
Maximum peak amplitude allowed for overshoot area. (See Figure 99)	0.4	0.4	0.4	0.4	V
Maximum peak amplitude allowed for undershoot area. (See Figure 99)	0.4	0.4	0.4	0.4	V
Maximum overshoot area above VDDQ (See Figure 99)	0.25	0.19	0.15	0.13	V-ns
Maximum undershoot area below VSSQ (See Figure 99)	0.25	0.19	0.15	0.13	V-ns
(CK, CK#, DQ, DQS, DQS#, DM)					

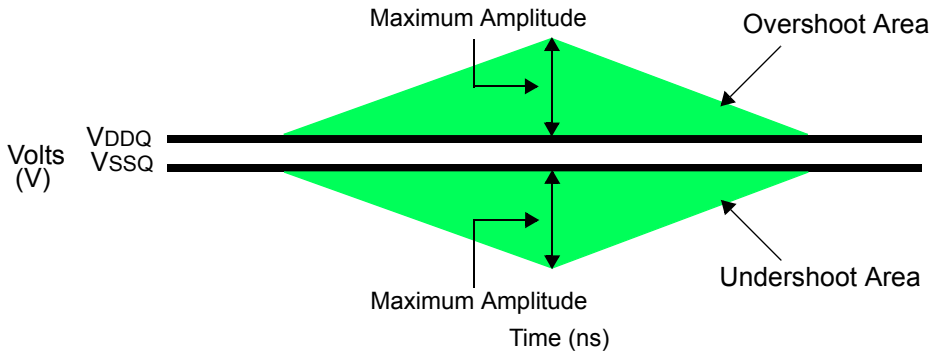

Figure 99 — Clock, Data, Strobe and Mask Overshoot and Undershoot Definition

9 AC and DC Output Measurement Levels (Cont'd)

9.7 34 ohm Output Driver DC Electrical Characteristics

A functional representation of the output buffer is shown in Figure 100. Output driver impedance *RON* is defined by the value of the external reference resistor RZQ as follows:

$RON_{34} = R_{ZQ} / 7$ (nominal 34.3 Ω ±10% with nominal $R_{ZQ} = 240$ Ω)

The individual pull-up and pull-down resistors (RON_{Pu} and RON_{Pd}) are defined as follows:

$$RON_{Pu} = \frac{V_{DDQ} - V_{Out}}{|I_{Out}|}$$ under the condition that RON_{Pd} is turned off (1)

$$RON_{Pd} = \frac{V_{Out}}{|I_{Out}|}$$ under the condition that RON_{Pu} is turned off (2)

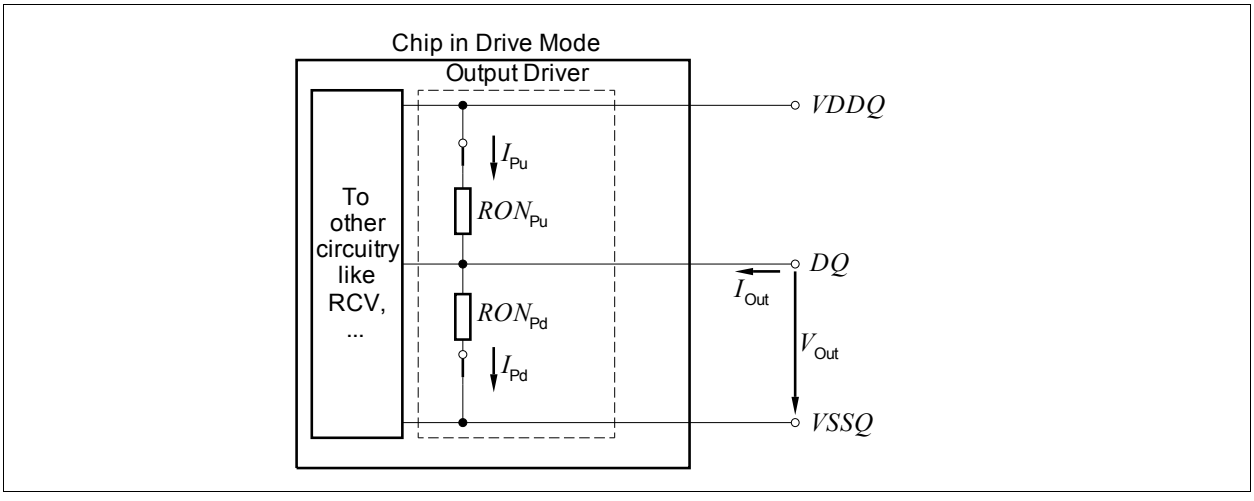

Figure 100 — Output Driver: Definition of Voltages and Currents

9 AC and DC Output Measurement Levels (Cont'd)
9.7 34 ohm Output Driver DC Electrical Characteristics (Cont'd)

Table 39 — Output Driver DC Electrical Characteristics, assuming R_{ZQ} = 240 Ω ; entire operating temperature range; after proper ZQ calibration

RON_{Nom}	Resistor	V_{Out}	min	nom	max	Unit	Notes
34 Ω	RON_{34Pd}	V_{OLdc} = 0.2 × V_{DDQ}	0.6	1.0	1.1	R_{ZQ}/7	1, 2, 3
		V_{OMdc} = 0.5 × V_{DDQ}	0.9	1.0	1.1	R_{ZQ}/7	1, 2, 3
		V_{OHdc} = 0.8 × V_{DDQ}	0.9	1.0	1.4	R_{ZQ}/7	1, 2, 3
	RON_{34Pu}	V_{OLdc} = 0.2 × V_{DDQ}	0.9	1.0	1.4	R_{ZQ}/7	1, 2, 3
		V_{OMdc} = 0.5 × V_{DDQ}	0.9	1.0	1.1	R_{ZQ}/7	1, 2, 3
		V_{OHdc} = 0.8 × V_{DDQ}	0.6	1.0	1.1	R_{ZQ}/7	1, 2, 3
40 Ω	RON_{40Pd}	V_{OLdc} = 0.2 × V_{DDQ}	0.6	1.0	1.1	R_{ZQ}/6	1, 2, 3
		V_{OMdc} = 0.5 × V_{DDQ}	0.9	1.0	1.1	R_{ZQ}/6	1, 2, 3
		V_{OHdc} = 0.8 × V_{DDQ}	0.9	1.0	1.4	R_{ZQ}/6	1, 2, 3
	RON_{40Pu}	V_{OLdc} = 0.2 × V_{DDQ}	0.9	1.0	1.4	R_{ZQ}/6	1, 2, 3
		V_{OMdc} = 0.5 × V_{DDQ}	0.9	1.0	1.1	R_{ZQ}/6	1, 2, 3
		V_{OHdc} = 0.8 × V_{DDQ}	0.6	1.0	1.1	R_{ZQ}/6	1, 2, 3
Mismatch between pull-up and pull-down, MM_{PuPd}		V_{OMdc} 0.5 × V_{DDQ}	-10		+10	%	1, 2, 4

NOTE 1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.

NOTE 2. The tolerance limits are specified under the condition that $V_{DDQ} = V_{DD}$ and that $V_{SSQ} = V_{SS}$.

NOTE 3. Pull-down and pull-up output driver impedances are recommended to be calibrated at 0.5 × V_{DDQ}. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.2 × V_{DDQ} and 0.8 × V_{DDQ}.

NOTE 4. Measurement definition for mismatch between pull-up and pull-down, MM_{PuPd}:
Measure RON_{Pu} and RON_{Pd}, both at 0.5 * V_{DDQ}:

$$MM_{PuPd} = \frac{RON_{Pu} - RON_{Pd}}{RON_{Nom}} x 100$$

9.7.1 Output Driver Temperature and Voltage sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to Table 40 and Table 41.

ΔT = T - T(@calibration); ΔV= VDDQ - VDDQ(@calibration); VDD = VDDQ

NOTE: $dR_{ON}dT$ and $dR_{ON}dV$ are not subject to production test but are verified by design and characterization.

9.7 34 ohm Output Driver DC Electrical Characteristics (Cont'd)
9.7.1 Output Driver Temperature and Voltage sensitivity (Cont'd)

Table 40 — Output Driver Sensitivity Definition

	min	max	unit
RONPU@ V_{OHdc}	0.6 - $dR_{ON}dTH*\|DT\|$ - $dR_{ON}dVH*\|DV\|$	1.1 + $dR_{ON}dTH*\|DT\|$ + $dR_{ON}dVH*\|DV\|$	RZQ/7
RON@ V_{OMdc}	0.9 - $dR_{ON}dTM*\|DT\|$ - $dR_{ON}dVM*\|DV\|$	1.1 + $dR_{ON}dTM*\|DT\|$ + $dR_{ON}dVM*\|DV\|$	RZQ/7
RONPD@ V_{OLdc}	0.6 - $dR_{ON}dTL*\|DT\|$ - $dR_{ON}dVL*\|DV\|$	1.1 + $dR_{ON}dTL*\|DT\|$ + $dR_{ON}dVL*\|DV\|$	RZQ/7

Table 41 — Output Driver Voltage and Temperature Sensitivity

Speed Bin	800/1066/1333		1600		
	min	max	min	max	unit
$dR_{ON}dTM$	0	1.5	0	1.5	%/°C
$dR_{ON}dVM$	0	0.15	0	0.13	%/mV
$dR_{ON}dTL$	0	1.5	0	1.5	%/°C
$dR_{ON}dVL$	0	0.15	0	0.13	%/mV
$dR_{ON}dTH$	0	1.5	0	1.5	%/°C
$dR_{ON}dVH$	0	0.15	0	0.13	%/mV

These parameters may not be subject to production test. They are verified by design and characterization.

9.8 On-Die Termination (ODT) Levels and I-V Characteristics

9.8.1 On-Die Termination (ODT) Levels and I-V Characteristics

On-Die Termination effective resistance RTT is defined by bits A9, A6 and A2 of the MR1 Register.

ODT is applied to the DQ, DM, DQS/DQS# and TDQS/TDQS# (x8 devices only) pins.

A functional representation of the on-die termination is shown in Figure 101. The individual pull-up and pull-down resistors (RTT_{Pu} and RTT_{Pd}) are defined as follows:

$$RTT_{Pu} = \frac{V_{DDQ} - V_{Out}}{|I_{Out}|} \text{ under the condition that } RTT_{Pd} \text{ is turned off} \quad (3)$$

$$RTT_{Pd} = \frac{V_{Out}}{|I_{Out}|} \text{ under the condition that } RTT_{Pu} \text{ is turned off} \quad (4)$$

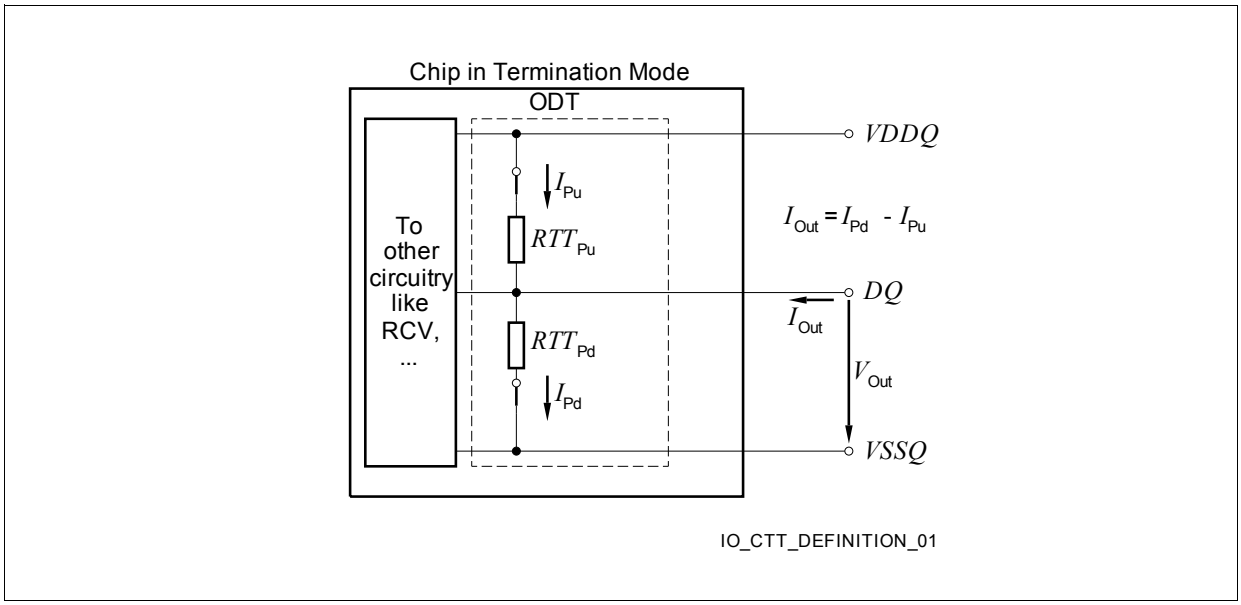

Figure 101 — On-Die Termination: Definition of Voltages and Currents

9 AC and DC Output Measurement Levels (Cont'd)
9.8 On-Die Termination (ODT) Levels and I-V Characteristics (Cont'd)

9.8.2 ODT DC Electrical Characteristics

Table 42 provides an overview of the ODT DC electrical characteristics. The values for $RTT_{60Pd120}$, $RTT_{60Pu120}$, $RTT_{120Pd240}$, $RTT_{120Pu240}$, RTT_{40Pd80}, RTT_{40Pu80}, RTT_{30Pd60}, RTT_{30Pu60} , RTT_{20Pd40}, RTT_{20Pu40} are not specification requirements, but can be used as design guide lines:

Table 42 — ODT DC Electrical Characteristics, assuming R_{ZQ} = 240 Ω +/- 1% entire operating temperature range; after proper ZQ calibration

MR1 A9, A6, A2	*RTT*	Resistor	V_{Out}	min	nom	max	Unit	Notes
0, 1, 0	120 Ω	$RTT_{120Pd240}$	V_{OLdc} $0.2 \times V_{DDQ}$	0.6	1.00	1.1	R_{ZQ}	1, 2, 3, 4,
			$0.5 \times V_{DDQ}$	0.9	1.00	1.1	R_{ZQ}	1, 2, 3, 4,
			V_{OHdc} $0.8 \times V_{DDQ}$	0.9	1.00	1.4	R_{ZQ}	1, 2, 3, 4,
		$RTT_{120Pu240}$	V_{OLdc} $0.2 \times V_{DDQ}$	0.9	1.00	1.4	R_{ZQ}	1, 2, 3, 4,
			$0.5 \times V_{DDQ}$	0.9	1.00	1.1	R_{ZQ}	1, 2, 3, 4,
			V_{OHdc} $0.8 \times V_{DDQ}$	0.6	1.00	1.1	R_{ZQ}	1, 2, 3, 4,
		RTT_{120}	$V_{IL(ac)}$ to $V_{IH(ac)}$	0.9	1.00	1.6	$R_{ZQ}/2$	1, 2, 5,
0, 0, 1	60 Ω	$RTT_{60Pd120}$	V_{OLdc} $0.2 \times V_{DDQ}$	0.6	1.00	1.1	$R_{ZQ}/2$	1, 2, 3, 4,
			$0.5 \times V_{DDQ}$	0.9	1.00	1.1	$R_{ZQ}/2$	1, 2, 3, 4,
			V_{OHdc} $0.8 \times V_{DDQ}$	0.9	1.00	1.4	$R_{ZQ}/2$	1, 2, 3, 4,
		$RTT_{60Pu120}$	V_{OLdc} $0.2 \times V_{DDQ}$	0.9	1.00	1.4	$R_{ZQ}/2$	1, 2, 3, 4,
			$0.5 \times V_{DDQ}$	0.9	1.00	1.1	$R_{ZQ}/2$	1, 2, 3, 4,
			V_{OHdc} $0.8 \times V_{DDQ}$	0.6	1.00	1.1	$R_{ZQ}/2$	1, 2, 3, 4,
		RTT_{60}	$V_{IL(ac)}$ to $V_{IH(ac)}$	0.9	1.00	1.6	$R_{ZQ}/4$	1, 2, 5,

9.8 On-Die Termination (ODT) Levels and I-V Characteristics (Cont'd)
9.8.2 ODT DC Electrical Characteristics (Cont'd)

Table 42 — ODT DC Electrical Characteristics, assuming R_{ZQ} = 240 Ω +/- 1% entire operating temperature range; after proper ZQ calibration (Cont'd)

MR1 A9, A6, A2	*RTT*	Resistor	V_{Out}	min	nom	max	Unit	Notes
0, 1, 1	40 Ω	RTT_{40Pd80}	V_{OLdc} $0.2 \times V_{DDQ}$	0.6	1.00	1.1	$R_{ZQ/3}$	1, 2, 3, 4,
			$0.5 \times V_{DDQ}$	0.9	1.00	1.1	$R_{ZQ/3}$	1, 2, 3, 4,
			V_{OHdc} $0.8 \times V_{DDQ}$	0.9	1.00	1.4	$R_{ZQ/3}$	1, 2, 3, 4,
		RTT_{40Pu80}	V_{OLdc} $0.2 \times V_{DDQ}$	0.9	1.00	1.4	$R_{ZQ/3}$	1, 2, 3, 4,
			$0.5 \times V_{DDQ}$	0.9	1.00	1.1	$R_{ZQ/3}$	1, 2, 3, 4,
			V_{OHdc} $0.8 \times V_{DDQ}$	0.6	1.00	1.1	$R_{ZQ/3}$	1, 2, 3, 4,
		RTT_{40}	$V_{IL(ac)}$ to $V_{IH(ac)}$	0.9	1.00	1.6	$R_{ZQ}/6$	1, 2, 5,
1, 0, 1	30 Ω	RTT_{30Pd60}	V_{OLdc} $0.2 \times V_{DDQ}$	0.6	1.00	1.1	$R_{ZQ/4}$	1, 2, 3, 4,
			$0.5 \times V_{DDQ}$	0.9	1.00	1.1	$R_{ZQ/4}$	1, 2, 3, 4,
			V_{OHdc} $0.8 \times V_{DDQ}$	0.9	1.00	1.4	$R_{ZQ/4}$	1, 2, 3, 4,
		RTT_{30Pu60}	V_{OLdc} $0.2 \times V_{DDQ}$	0.9	1.00	1.4	$R_{ZQ/4}$	1, 2, 3, 4,
			$0.5 \times V_{DDQ}$	0.9	1.00	1.1	$R_{ZQ/4}$	1, 2, 3, 4,
			V_{OHdc} $0.8 \times V_{DDQ}$	0.6	1.00	1.1	$R_{ZQ/4}$	1, 2, 3, 4,
		RTT_{30}	$V_{IL(ac)}$ to $V_{IH(ac)}$	0.9	1.00	1.6	$R_{ZQ}/8$	1, 2, 5,
1, 0, 0	20 Ω	RTT_{20Pd40}	V_{OLdc} $0.2 \times V_{DDQ}$	0.6	1.00	1.1	$R_{ZQ/6}$	1, 2, 3, 4,
			$0.5 \times V_{DDQ}$	0.9	1.00	1.1	$R_{ZQ/6}$	1, 2, 3, 4,
			V_{OHdc} $0.8 \times V_{DDQ}$	0.9	1.00	1.4	$R_{ZQ/6}$	1, 2, 3, 4,
		RTT_{20Pu40}	V_{OLdc} $0.2 \times V_{DDQ}$	0.9	1.00	1.4	$R_{ZQ/6}$	1, 2, 3, 4,
			$0.5 \times V_{DDQ}$	0.9	1.00	1.1	$R_{ZQ/6}$	1, 2, 3, 4,
			V_{OHdc} $0.8 \times V_{DDQ}$	0.6	1.00	1.1	$R_{ZQ/6}$	1, 2, 3, 4,
		RTT_{20}	$V_{IL(ac)}$ to $V_{IH(ac)}$	0.9	1.00	1.6	$R_{ZQ}/12$	1, 2, 5,
Deviation of V_M w.r.t. $V_{DDQ}/2$, ΔV_M				-5		+5	%	1, 2, 5, 6,

NOTE 1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.

NOTE 2. The tolerance limits are specified under the condition that $V_{DDQ} = V_{DD}$ and that $V_{SSQ} = V_{SS}$.

NOTE 3. Pull-down and pull-up ODT resistors are recommended to be calibrated at $0.5 \times V_{DDQ}$. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at $0.2 \times V_{DDQ}$ and $0.8 \times V_{DDQ}$.

NOTE 4. Not a specification requirement, but a design guide line.

9.8 On-Die Termination (ODT) Levels and I-V Characteristics (Cont'd)
9.8.2 ODT DC Electrical Characteristics (Cont'd)

NOTE 5. Measurement definition for *RTT*:
Apply $V_{IH(ac)}$ to pin under test and measure current $I(V_{IH(ac)})$, then apply $V_{IL(ac)}$ to pin under test and measure current $I(V_{IL(ac)})$ respectively.

$$RTT = \frac{V_{IH(ac)} - V_{IL(ac)}}{I(VIH(ac)) - I(VIL(ac))}$$

NOTE 6. Measurement definition for V_M and DV_M:
Measure voltage (V_M) at test pin (midpoint) with no load:

$$\Delta V_M = \left(\frac{2 \times V_M}{V_{DDQ}} - 1\right) \times 100$$

9 AC and DC Output Measurement Levels (Cont'd)
9.8 On-Die Termination (ODT) Levels and I-V Characteristics (Cont'd)

9.8.3 ODT Temperature and Voltage sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to Table 43 and Table 44.

DT = T - T(@calibration); DV= VDDQ - VDDQ(@calibration); VDD = VDDQ

Table 43 — ODT Sensitivity Definition

	min	max	unit
RTT	0.9 - $dR_{TT}dT*\|\Delta T\|$ - $dR_{TT}dV*\|\Delta V\|$	1.6 + $dR_{TT}dT*\|\Delta T\|$ + $dR_{TT}dV*\|\Delta V\|$	RZQ/2,4,6,8,12

Table 44 — ODT Voltage and Temperature Sensitivity

	min	max	unit
$dR_{TT}dT$	0	1.5	%/°C
$dR_{TT}dV$	0	0.15	%/mV

These parameters may not be subject to production test. They are verified by design and characterization

9.9 ODT Timing Definitions

9.9.1 Test Load for ODT Timings

Different than for timing measurements, the reference load for ODT timings is defined in Figure 102.

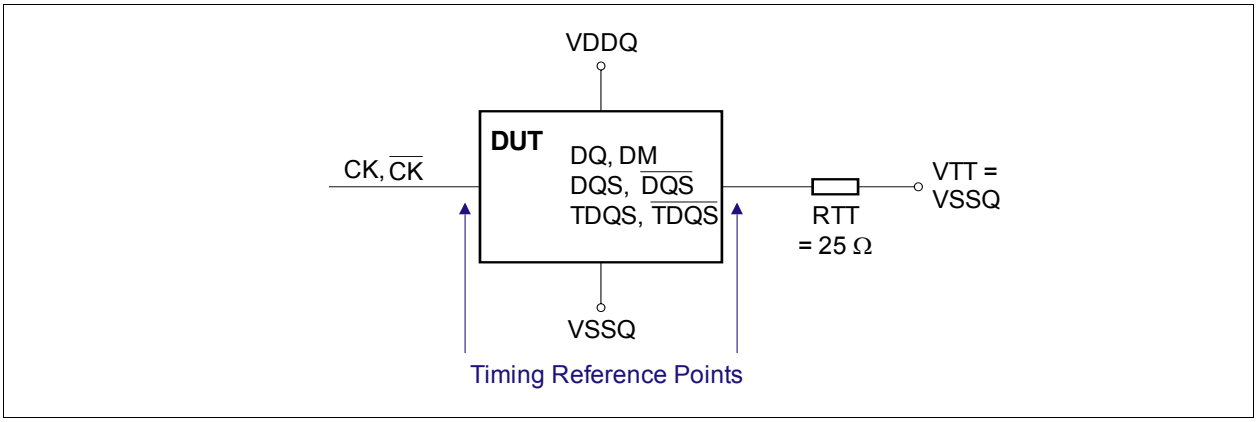

Figure 102: ODT Timing Reference Load

9 AC and DC Output Measurement Levels (Cont'd)
9.9 ODT Timing Definitions (Cont'd)

9.9.2 ODT Timing Definitions

Definitions for t_{AON}, t_{AONPD}, t_{AOF}, t_{AOFPD} and t_{ADC} are provided in Table 45 and subsequent figures. Measurement reference settings are provided in Table 46.

Table 45 — ODT Timing Definitions

Symbol	Begin Point Definition	End Point Definition	Figure
t_{AON}	Rising edge of CK - CK# defined by the end point of ODTLon	Extrapolated point at VSSQ	Figure 103
t_{AONPD}	Rising edge of CK - CK# with ODT being first registered high	Extrapolated point at VSSQ	Figure 104
t_{AOF}	Rising edge of CK - CK#defined by the end point of ODTLoff	End point: Extrapolated point at VRTT_Nom	Figure 105
t_{AOFPD}	Rising edge of CK - CK# with ODT being first registered low	End point: Extrapolated point at VRTT_Nom	Figure 106
t_{ADC}	Rising edge of CK - CK# defined by the end point of ODTLcnw, ODTLcwn4 or ODTLcwn8	End point: Extrapolated point at VRTT_Wr and VRTT_Nom respectively	Figure 107

Table 46 — Reference Settings for ODT Timing Measurements

Measured Parameter	RTT_Nom Setting	RTT_Wr Setting	V_{SW1} [V]	V_{SW2} [V]	Note
t_{AON}	$R_{ZQ}/4$	NA	0.05	0.10	
	$R_{ZQ}/12$	NA	0.10	0.20	
t_{AONPD}	$R_{ZQ}/4$	NA	0.05	0.10	
	$R_{ZQ}/12$	NA	0.10	0.20	
t_{AOF}	$R_{ZQ}/4$	NA	0.05	0.10	
	$R_{ZQ}/12$	NA	0.10	0.20	
t_{AOFPD}	$R_{ZQ}/4$	NA	0.05	0.10	
	$R_{ZQ}/12$	NA	0.10	0.20	
t_{ADC}	$R_{ZQ}/12$	$R_{ZQ}/2$	0.20	0.30	

9.9 ODT Timing Definitions (Cont'd)
9.9.2 ODT Timing Definitions (Cont'd)

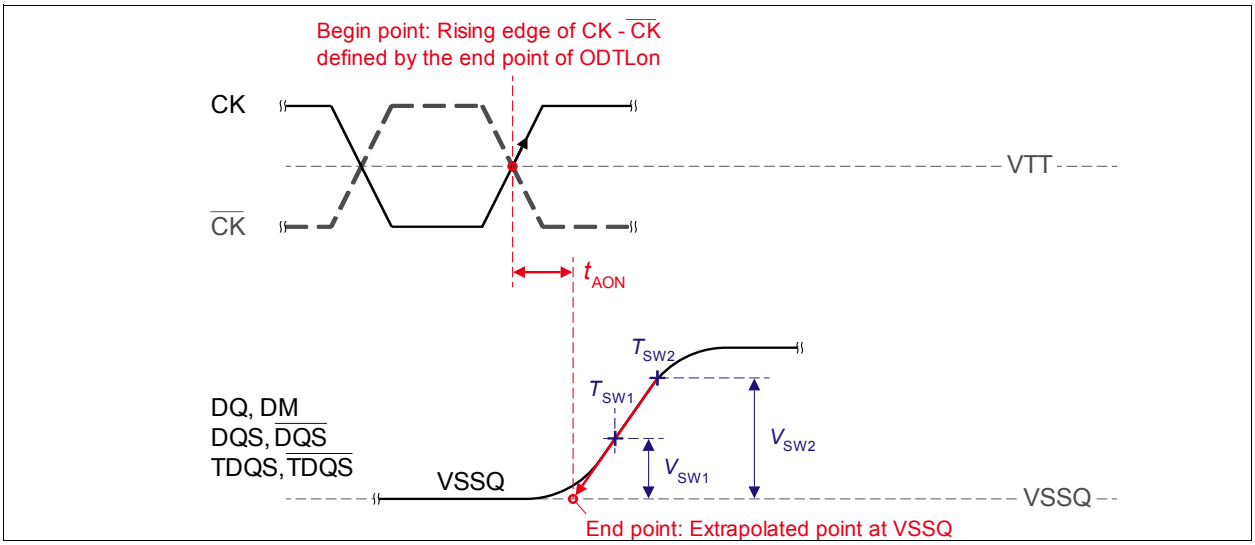

Figure 103 — Definition of t_{AON}

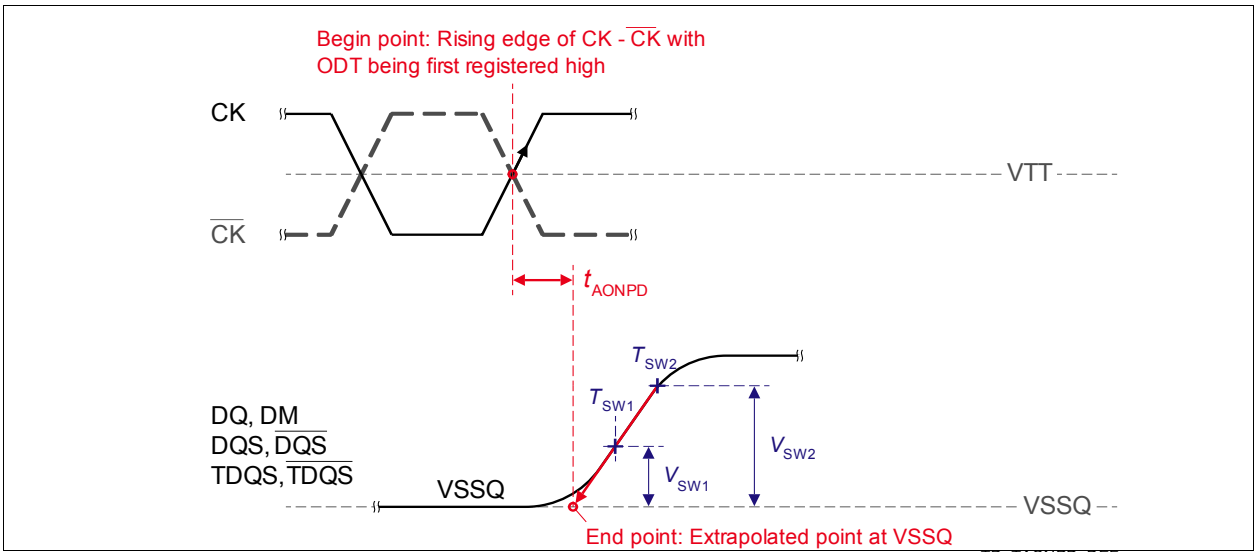

Figure 104 — Definition of t_{AONPD}

9.9 ODT Timing Definitions (Cont'd)
9.9.2 ODT Timing Definitions (Cont'd)

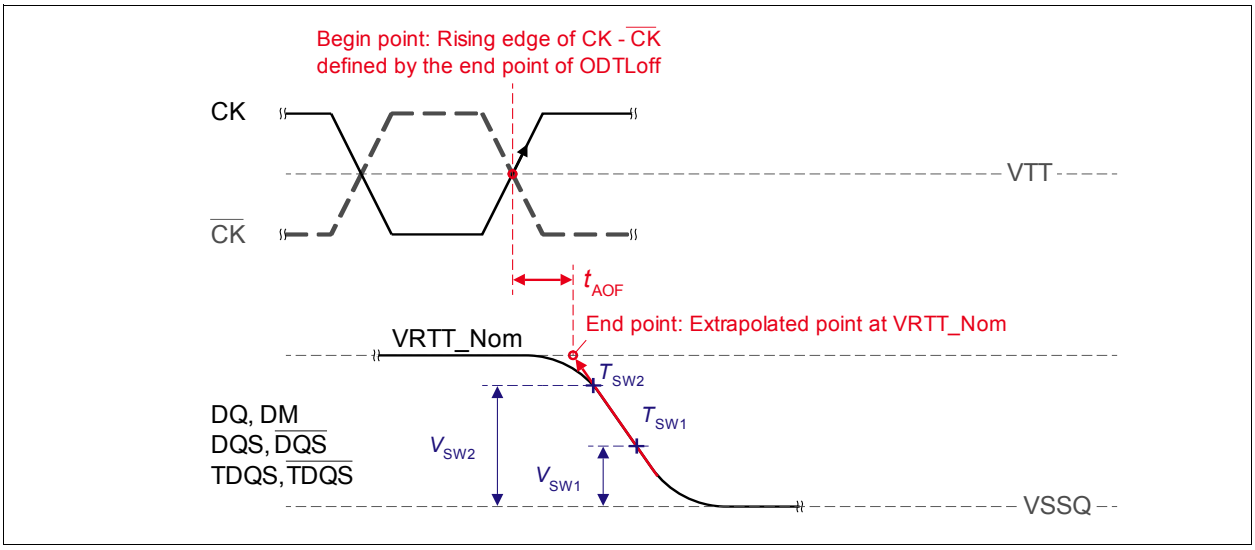

Figure 105 — Definition of t_{AOF}

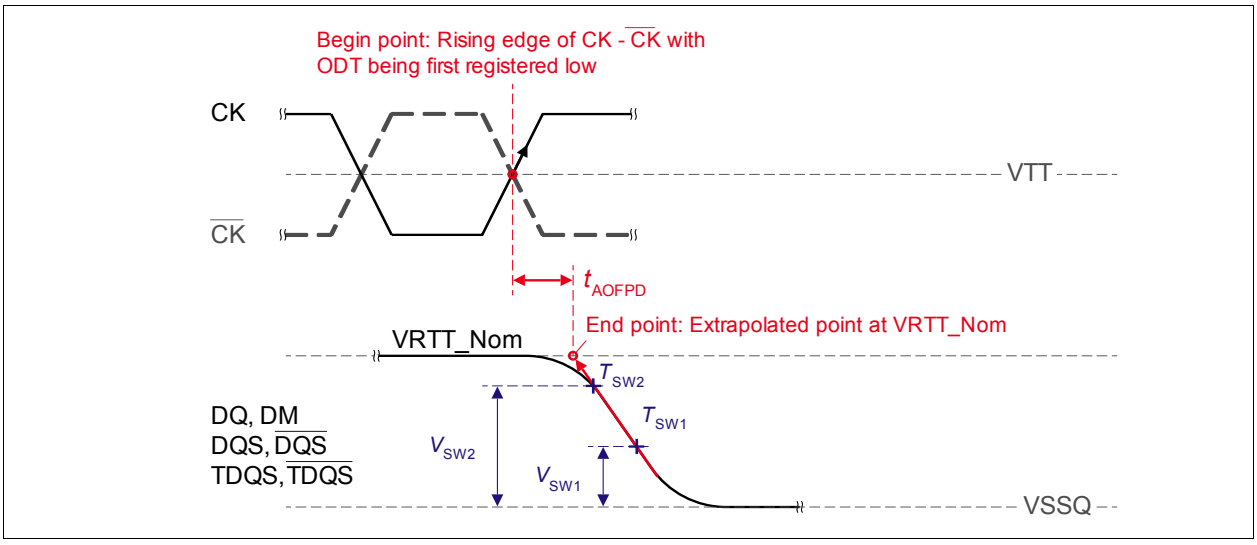

Figure 106 — Definition of t_{AOFPD}

9.9 ODT Timing Definitions (Cont'd)
9.9.2 ODT Timing Definitions (Cont'd)

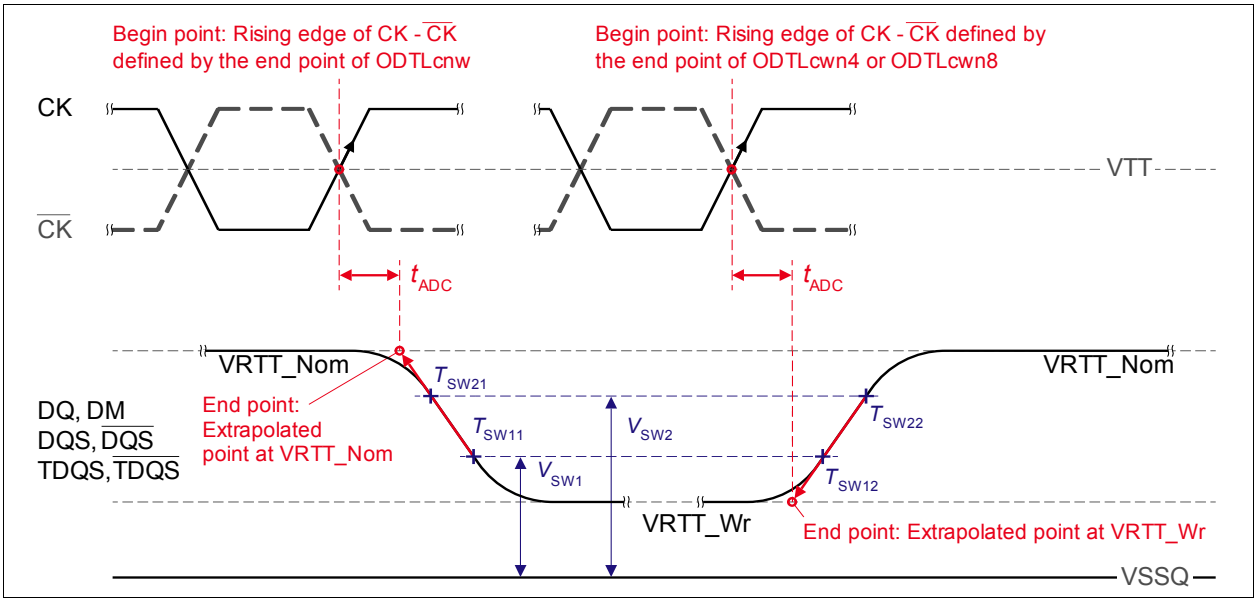

Figure 107 — Definition of t_{ADC}

10 IDD and IDDQ Specification Parameters and Test Conditions

10.1 IDD and IDDQ Measurement Conditions

In this chapter, IDD and IDDQ measurement conditions such as test load and patterns are defined. Figure 108 shows the setup and test load for IDD and IDDQ measurements.

- **IDD currents** (such as IDD0, IDD1, IDD2N, IDD2NT, IDD2P0, IDD2P1, IDD2Q, IDD3N, IDD3P, IDD4R, IDD4W, IDD5B, IDD6, IDD6ET, IDD6TC and IDD7) are measured as time-averaged currents with all VDD balls of the DDR3 SDRAM under test tied together. Any IDDQ current is not included in IDD currents.
- **IDDQ currents** (such as IDDQ2NT and IDDQ4R) are measured as time-averaged currents with all VDDQ balls of the DDR3 SDRAM under test tied together. Any IDD current is not included in IDDQ currents.
  Attention: IDDQ values cannot be directly used to calculate IO power of the DDR3 SDRAM. They can be used to support correlation of simulated IO power to actual IO power as outlined in Figure 109. In DRAM module application, IDDQ cannot be measured separately since VDD and VDDQ are using one merged-power layer in Module PCB.

For IDD and IDDQ measurements, the following definitions apply:

- "0" and "LOW" is defined as VIN <= VILAC(max).
- "1" and "HIGH" is defined as VIN >= VIHAC(min).
- "MID-LEVEL" is defined as inputs are VREF = VDD / 2.
- Timings used for IDD and IDDQ Measurement-Loop Patterns are provided in Table 47 on page 141.
- Basic IDD and IDDQ Measurement Conditions are described in Table 48 on page 141.
- Detailed IDD and IDDQ Measurement-Loop Patterns are described in Table 49 on page 144 through Table 56 on page 149.
- IDD Measurements are done after properly initializing the DDR3 SDRAM. This includes but is not limited to setting
  RON = RZQ/7 (34 Ohm in MR1);
  Qoff = 0_B (Output Buffer enabled in MR1);
  RTT_Nom = RZQ/6 (40 Ohm in MR1);
  RTT_Wr = RZQ/2 (120 Ohm in MR2);
  TDQS Feature disabled in MR1
- **Attention:** The IDD and IDDQ Measurement-Loop Patterns need to be executed at least one time before actual IDD or IDDQ measurement is started.
- Define D = {CS#, RAS#, CAS#, WE# } := {HIGH, LOW, LOW, LOW}
- Define D# = {CS#, RAS#, CAS#, WE# } := {HIGH, HIGH, HIGH, HIGH}

10 IDD Specification Parameters and Test Conditions (Cont'd)
10.1 IDD and IDDQ Measurement Conditions (Cont'd)

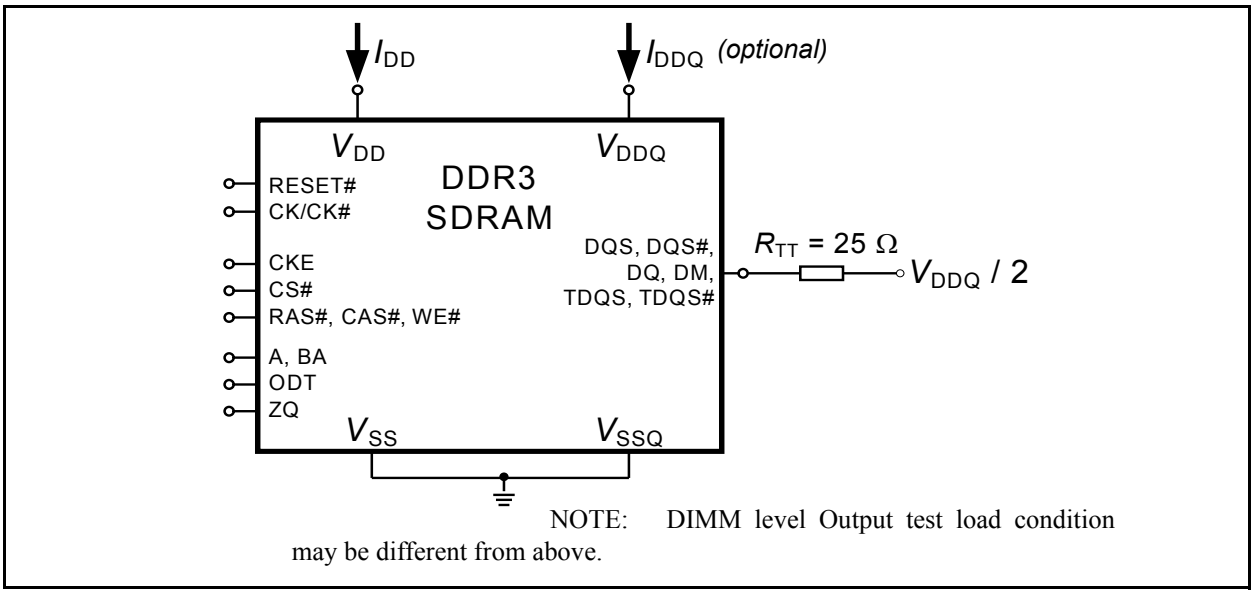

Figure 108 — Measurement Setup and Test Load for IDD and IDDQ (optional) Measurements

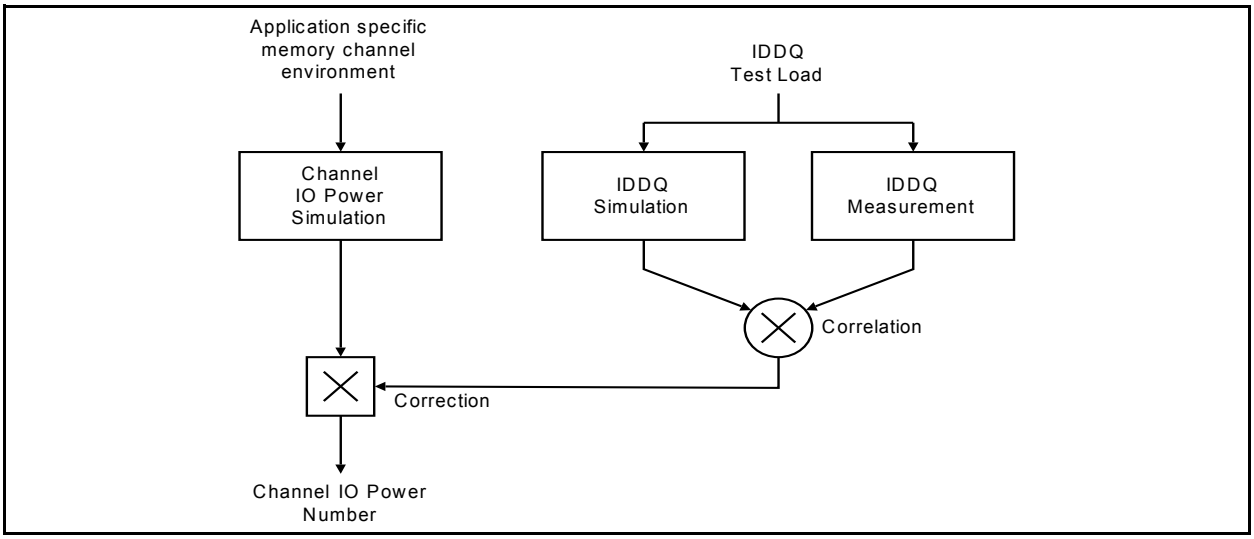

Figure 109 — Correlation from simulated Channel IO Power to actual Channel IO Power supported by IDDQ Measurement.

10 IDD and IDDQ Specification Parameters and Test Conditions (Cont'd)
10.1 IDD and IDDQ Measurement Conditions (Cont'd)

Table 47 — Timings used for IDD and IDDQ Measurement-Loop Patterns

Symbol		DDR3-800		DDR3-1066			DDR3-1333				DDR3-1600				Unit
		5-5-5	6-6-6	6-6-6	7-7-7	8-8-8	7-7-7	8-8-8	9-9-9	10-10-10	8-8-8	9-9-9	10-10-10	11-11-11	
tCK		2.5		1.875			1.5				1.25				ns
CL		5	6	6	7	8	7	8	9	10	8	9	10	11	nCK
nRCD		5	6	6	7	8	7	8	9	10	8	9	10	11	nCK
nRC		20	21	26	27	28	31	32	33	34	36	37	38	39	nCK
nRAS		15		20			24				28				nCK
nRP		5	6	6	7	8	7	8	9	10	8	9	10	11	nCK
nFAW	x4/x8	16		20			20				24				nCK
	x16	20		27			30				32				nCK
nRRD	x4/x8	4		4			4				5				nCK
	x16	4		6			5				6				nCK
nRFC 512 Mb		36		48			60				72				nCK
nRFC 1 Gb		44		59			74				88				nCK
nRFC 2 Gb		64		86			107				128				nCK
nRFC 4 Gb		120		160			200				240				nCK
nRFC 8 Gb		140		187			234				280				nCK

Table 48 — Basic IDD and IDDQ Measurement Conditions

Symbol	Description
IDD0	**Operating One Bank Active-Precharge Current** **CKE:** High; **External clock:** On; **tCK, nRC, nRAS, CL:** see Table 47 on page 141; **BL:** 8(1); **AL:** 0; **CS#**: High between ACT and PRE; **Command, Address, Bank Address Inputs:** partially toggling according to Table 49 on page 144; **Data IO:** MID-LEVEL; **DM**:stable at 0; **Bank Activity:** Cycling with one bank active at a time: 0,0,1,1,2,2,... (see Table 49 on page 144); **Output Buffer and RTT:** Enabled in Mode Registers(2); **ODT Signal:** stable at 0; **Pattern Details:** see Table 49 on page 144
IDD1	**Operating One Bank Active-Read-Precharge Current** **CKE:** High; **External clock:** On; **tCK, nRC, nRAS, nRCD, CL**: see Table 47 on page 141; **BL:** 8(1,7); **AL:** 0; **CS#**: High between ACT, RD and PRE; **Command, Address, Bank Address Inputs, Data IO:** partially toggling according to Table 50 on page 145; **DM**:stable at 0; **Bank Activity:** Cycling with one bank active at a time: 0,0,1,1,2,2,... (see Table 50 on page 145); **Output Buffer and RTT:** Enabled in Mode Registers(2); **ODT Signal:** stable at 0; **Pattern Details:** see Table 50 on page 145
IDD2N	**Precharge Standby Current** **CKE**: High; **External clock:** On; **tCK, CL**: see Table 47 on page 141; **BL:** 8(1); **AL:** 0; **CS#**: stable at 1; **Command, Address, Bank Address Inputs:** partially toggling according to Table 51 on page 146; **Data IO:** MID-LEVEL; **DM**:stable at 0; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers(2); **ODT Signal:** stable at 0; **Pattern Details:** see Table 51 on page 146
IDD2NT	**Precharge Standby ODT Current** **CKE**: High; **External clock:** On; **tCK, CL**: see Table 47 on page 141; **BL:** 8(1); **AL:** 0; **CS#**: stable at 1; **Command, Address, Bank Address Inputs:** partially toggling according to Table 52 on page 146; **Data IO:** MID-LEVEL;**DM**:stable at 0; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers(2); **ODT Signal:** toggling according to Table 52 on page 146; **Pattern Details:** see Table 52 on page 146
IDDQ2NT (optional)	**Precharge Standby ODT IDDQ Current** Same definition like for IDD2NT, however measuring IDDQ current instead of IDD current

10 IDD and IDDQ Specification Parameters and Test Conditions (Cont'd)
10.1 IDD and IDDQ Measurement Conditions (Cont'd)

Table 48 — Basic IDD and IDDQ Measurement Conditions

Symbol	Description
IDD2P0	**Precharge Power-Down Current Slow Exit** **CKE:** Low; **External clock:** On; **tCK, CL**: see Table 47 on page 141; **BL:** 8(1); **AL:** 0; **CS#**: stable at 1; **Command, Address, Bank Address Inputs:** stable at 0; **Data IO:** MID-LEVEL; **DM**:stable at 0; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers(2); **ODT Signal:** stable at 0; **Precharge Power Down Mode**: Slow Exit(3)
IDD2P1	**Precharge Power-Down Current Fast Exit** **CKE:** Low; **External clock:** On; **tCK, CL**: see Table 47 on page 141; **BL:** 8(1); **AL:** 0; **CS#**: stable at 1; **Command, Address, Bank Address Inputs:** stable at 0; **Data IO:** MID-LEVEL; **DM**:stable at 0; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers(2); **ODT Signal:** stable at 0; **Precharge Power Down Mode**: Fast Exit(3)
IDD2Q	**Precharge Quiet Standby Current** **CKE**: High; **External clock:** On; **tCK, CL**: see Table 47 on page 141; **BL:** 8(1); **AL:** 0; **CS#**: stable at 1; **Command, Address, Bank Address Inputs:** stable at 0; **Data IO:** MID-LEVEL; **DM**:stable at 0;**Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers(2); **ODT Signal:** stable at 0
IDD3N	**Active Standby Current** **CKE**: High; **External clock:** On; **tCK, CL**: see Table 47 on page 141; **BL:** 8(1); **AL:** 0; **CS#**: stable at 1; **Command, Address, Bank Address Inputs:** partially toggling according to Table 51 on page 146; **Data IO:** MID-LEVEL; **DM**:stable at 0;**Bank Activity:** all banks open; **Output Buffer and RTT:** Enabled in Mode Registers(2); **ODT Signal:** stable at 0; **Pattern Details:** see Table 51 on page 146
IDD3P	**Active Power-Down Current** **CKE:** Low; **External clock:** On; **tCK, CL**: see Table 47 on page 141; **BL:** 8(1); **AL:** 0; **CS#**: stable at 1; **Command, Address, Bank Address Inputs:** stable at 0; **Data IO:** MID-LEVEL;**DM**:stable at 0; **Bank Activity:** all banks open; **Output Buffer and RTT:** Enabled in Mode Registers(2); **ODT Signal:** stable at 0
IDD4R	**Operating Burst Read Current** **CKE:** High; **External clock:** On; **tCK, CL**: see Table 47 on page 141; **BL:** 8(1,7); **AL:** 0; **CS#**: High between RD; **Command, Address, Bank Address Inputs:** partially toggling according to Table 53 on page 147; **Data IO:** seamless read data burst with different data between one burst and the next one according to Table 53 on page 147; **DM**:stable at 0; **Bank Activity:** all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... (see Table 53 on page 147); **Output Buffer and RTT:** Enabled in Mode Registers(2); **ODT Signal:** stable at 0; **Pattern Details:** see Table 53 on page 147
IDDQ4R (optional)	**Operating Burst Read IDDQ Current** Same definition like for IDD4R, however measuring IDDQ current instead of IDD current
IDD4W	**Operating Burst Write Current** **CKE:** High; **External clock:** On; **tCK, CL**: see Table 47 on page 141; **BL:** 8(1); **AL:** 0; **CS#**: High between WR; **Command, Address, Bank Address Inputs:** partially toggling according to Table 54 on page 147; **Data IO:** seamless write data burst with different data between one burst and the next one according to Table 54 on page 147; **DM:** stable at 0; **Bank Activity:** all banks open, WR commands cycling through banks: 0,0,1,1,2,2,... (see Table 54 on page 147); **Output Buffer and RTT:** Enabled in Mode Registers(2); **ODT Signal:** stable at HIGH; **Pattern Details:** see Table 54 on page 147
IDD5B	**Burst Refresh Current** **CKE:** High; **External clock:** On; **tCK, CL, nRFC**: see Table 47 on page 141; **BL:** 8(1); **AL:** 0; **CS#**: High between REF; **Command, Address, Bank Address Inputs:** partially toggling according to Table 55 on page 148; **Data IO:** MID-LEVEL;**DM**:stable at 0; **Bank Activity:** REF command every nRFC (see Table 55 on page 148); **Output Buffer and RTT:** Enabled in Mode Registers(2); **ODT Signal:** stable at 0; **Pattern Details:** see Table 55 on page 148
IDD6	**Self Refresh Current: Normal Temperature Range** T_{CASE}**:** 0 - 85°C; **Auto Self-Refresh (ASR)**: Disabled(4); **Self-Refresh Temperature Range (SRT):** Normal(5); **CKE:** Low; **External clock:** Off; CK and CK#: LOW; **CL**: see Table 47 on page 141; **BL:** 8(1); **AL:** 0; **CS#, Command, Address, Bank Address, Data IO:** MID-LEVEL;**DM**:stable at 0; **Bank Activity:** Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers(2); **ODT Signal:** MID-LEVEL

10 IDD and IDDQ Specification Parameters and Test Conditions (Cont'd)
10.1 IDD and IDDQ Measurement Conditions (Cont'd)

Table 48 — Basic IDD and IDDQ Measurement Conditions

Symbol	Description
IDD6ET	**Self-Refresh Current: Extended Temperature Range (optional)**(6) T_{CASE}**:** 0 - 95°C; **Auto Self-Refresh (ASR)**: Disabled(4); **Self-Refresh Temperature Range (SRT):** Extended(5); **CKE:** Low; **External clock:** Off; CK and CK#: LOW; **CL**: see Table 47 on page 141; **BL:** 8(1); **AL:** 0; **CS#, Command, Address, Bank Address, Data IO:** MID-LEVEL;**DM**:stable at 0; **Bank Activity:** Extended Temperature Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers(2); **ODT Signal:** MID-LEVEL
IDD6TC	**Auto Self-Refresh Current (optional)**(6) T_{CASE}**:** 0 - 95°C; **Auto Self-Refresh (ASR)**: Enabled(4); **Self-Refresh Temperature Range (SRT):** Normal(5); **CKE:** Low; **External clock:** Off; CK and CK#: LOW; **CL**: see Table 47 on page 141; **BL:** 8(1); **AL:** 0; **CS#, Command, Address, Bank Address, Data IO:** MID-LEVEL; **DM**:stable at 0; **Bank Activity:** Auto Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers(2); **ODT Signal:** MID-LEVEL
IDD7	**Operating Bank Interleave Read Current** **CKE:** High; **External clock:** On; **tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL**: see Table 47 on page 141; **BL:** 8(1,7); **AL:** CL-1; **CS#**: High between ACT and RDA; **Command, Address, Bank Address Inputs:** partially toggling according to Table 56 on page 149; **Data IO:** read data bursts with different data between one burst and the next one according to Table 56 on page 149; **DM**:stable at 0; **Bank Activity:** two times interleaved cycling through banks (0, 1, ...7) with different addressing, see Table 56 on page 149; **Output Buffer and RTT:** Enabled in Mode Registers(2); **ODT Signal:** stable at 0; **Pattern Details:** see Table 56 on page 149

NOTE 1. Burst Length: BL8 fixed by MRS: set MR0 A[1,0]=00B

NOTE 2. Output Buffer Enable: set MR1 A[12] = 0B; set MR1 A[5,1] = 01B; RTT_Nom enable: set MR1 A[9,6,2] = 011B; RTT_Wr enable: set MR2 A[10,9] = 10B

NOTE 3. Pecharge Power Down Mode: set MR0 A12=0B for Slow Exit or MR0 A12=1B for Fast Exit

NOTE 4. Auto Self-Refresh (ASR): set MR2 A6 = 0B to disable or 1B to enable feature

NOTE 5. Self-Refresh Temperature Range (SRT): set MR2 A7=0B for normal or 1B for extended temperature range

NOTE 6. Refer to DRAM supplier data sheet and/or DIMM SPD to determine if optional features or requirements are supported by DDR3 SDRAM device

NOTE 7. Read Burst Type: Nibble Sequential, set MR0 A[3] = 0B

10 IDD and IDDQ Specification Parameters and Test Conditions (Cont'd)
10.1 IDD and IDDQ Measurement Conditions (Cont'd)

Table 49 — IDD0 Measurement-Loop Pattern[1]

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[2]
toggling	Static High	0	0	**ACT**	0	0	1	1	0	**0**	00	0	0	**0**	0	-
			1, 2	D, D	1	0	0	0	0	**0**	00	0	0	**0**	0	-
			3, 4	D#, D#	1	1	1	1	0	**0**	00	0	0	**0**	0	-
			...	repeat pattern 1...4 until nRAS - 1, truncate if necessary												
			nRAS	**PRE**	0	0	1	0	0	0	00	0	0	**0**	0	-
			...	repeat pattern 1...4 until nRC - 1, truncate if necessary												
			1*nRC + 0	**ACT**	0	0	1	1	0	**0**	00	0	0	**F**	0	-
			1*nRC + 1, 2	D, D	1	0	0	0	0	**0**	00	0	0	**F**	0	-
			1*nRC + 3, 4	D#, D#	1	1	1	1	0	**0**	00	0	0	**F**	0	-
			...	repeat pattern nRC + 1,...,4 until 1*nRC + nRAS - 1, truncate if necessary												
			1*nRC + nRAS	**PRE**	0	0	1	0	0	0	00	0	0	**F**	0	-
			...	repeat nRC + 1,...,4 until 2*nRC - 1, truncate if necessary												
		1	2*nRC	repeat Sub-Loop 0, use **BA[2:0] = 1** instead												
		2	4*nRC	repeat Sub-Loop 0, use **BA[2:0] = 2** instead												
		3	6*nRC	repeat Sub-Loop 0, use **BA[2:0] = 3** instead												
		4	8*nRC	repeat Sub-Loop 0, use **BA[2:0] = 4** instead												
		5	10*nRC	repeat Sub-Loop 0, use **BA[2:0] = 5** instead												
		6	12*nRC	repeat Sub-Loop 0, use **BA[2:0] = 6** instead												
		7	14*nRC	repeat Sub-Loop 0, use **BA[2:0] = 7** instead												

NOTE:
1.DM must be driven LOW all the time. DQS, DQS# are MID-LEVEL.
2.DQ signals are MID-LEVEL.

10 IDD Specification Parameters and Test Conditions (Cont'd)
10.1 IDD and IDDQ Measurement Conditions (Cont'd)

Table 50 — IDD1 Measurement-Loop Pattern[1]

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[2]
toggling	Static High	0	0	**ACT**	0	0	1	1	0	**0**	00	0	0	**0**	0	-
			1, 2	D, D	1	0	0	0	0	**0**	00	0	0	**0**	0	-
			3,4	D#, D#	1	1	1	1	0	**0**	00	0	0	**0**	0	-
			...	repeat pattern 1...4 until nRCD - 1, truncate if necessary												
			nRCD	**RD**	0	1	0	1	0	**0**	00	0	0	**0**	0	**00000000**
			...	repeat pattern 1...4 until nRAS - 1, truncate if necessary												
			nRAS	**PRE**	0	0	1	0	0	0	00	0	0	**0**	0	-
			...	repeat pattern 1...4 until nRC - 1, truncate if necessary												
			1*nRC + 0	**ACT**	0	0	1	1	0	**0**	00	0	0	**F**	0	-
			1*nRC + 1, 2	D, D	1	0	0	0	0	**0**	00	0	0	**F**	0	-
			1*nRC + 3, 4	D#, D#	1	1	1	1	0	**0**	00	0	0	**F**	0	-
			...	repeat pattern nRC + 1,..., 4 until nRC + nRCD - 1, truncate if necessary												
			1*nRC + nRCD	**RD**	0	1	0	1	0	**0**	00	0	0	**F**	0	**00110011**
			...	repeat pattern nRC + 1,..., 4 until nRC +nRAS - 1, truncate if necessary												
			1*nRC + nRAS	**PRE**	0	0	1	0	0	0	00	0	0	**F**	0	-
			...	repeat pattern nRC + 1,..., 4 until 2 * nRC - 1, truncate if necessary												
		1	2*nRC	repeat Sub-Loop 0, use **BA[2:0] = 1** instead												
		2	4*nRC	repeat Sub-Loop 0, use **BA[2:0] = 2** instead												
		3	6*nRC	repeat Sub-Loop 0, use **BA[2:0] = 3** instead												
		4	8*nRC	repeat Sub-Loop 0, use **BA[2:0] = 4** instead												
		5	10*nRC	repeat Sub-Loop 0, use **BA[2:0] = 5** instead												
		6	12*nRC	repeat Sub-Loop 0, use **BA[2:0] = 6** instead												
		7	14*nRC	repeat Sub-Loop 0, use **BA[2:0] = 7** instead												

NOTE:

1. DM must be driven LOW all the time. DQS, DQS# are used according to RD Commands, otherwise MID-LEVEL.
2. Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are MID-LEVEL.

10 IDD Specification Parameters and Test Conditions (Cont'd)
10.1 IDD and IDDQ Measurement Conditions (Cont'd)

Table 51 — IDD2N and IDD3N Measurement-Loop Pattern[1]

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[2]
toggling	Static High	0	0	D	1	0	0	0	0	**0**	0	0	0	**0**	0	-
			1	D	1	0	0	0	0	**0**	0	0	0	**0**	0	-
			2	D#	1	1	1	1	0	**0**	0	0	0	**F**	0	-
			3	D#	1	1	1	1	0	**0**	0	0	0	**F**	0	-
		1	4-7	repeat Sub-Loop 0, use **BA[2:0] = 1** instead												
		2	8-11	repeat Sub-Loop 0, use **BA[2:0] = 2** instead												
		3	12-15	repeat Sub-Loop 0, use **BA[2:0] = 3** instead												
		4	16-19	repeat Sub-Loop 0, use **BA[2:0] = 4** instead												
		5	20-23	repeat Sub-Loop 0, use **BA[2:0] = 5** instead												
		6	24-27	repeat Sub-Loop 0, use **BA[2:0] = 6** instead												
		7	28-31	repeat Sub-Loop 0, use **BA[2:0] = 7** instead												

NOTE:
1.DM must be driven LOW all the time. DQS, DQS# are MID-LEVEL.
2.DQ signals are MID-LEVEL.

Table 52 — IDD2NT and IDDQ2NT Measurement-Loop Pattern[1]

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[2]
toggling	Static High	0	0	D	1	0	0	0	**0**	**0**	0	0	0	**0**	0	-
			1	D	1	0	0	0	**0**	**0**	0	0	0	**0**	0	-
			2	D#	1	1	1	1	**0**	**0**	0	0	0	**F**	0	-
			3	D#	1	1	1	1	**0**	**0**	0	0	0	**F**	0	-
		1	4-7	repeat Sub-Loop 0, but **ODT = 0** and **BA[2:0] = 1**												
		2	8-11	repeat Sub-Loop 0, but **ODT = 1** and **BA[2:0] = 2**												
		3	12-15	repeat Sub-Loop 0, but **ODT = 1** and **BA[2:0] = 3**												
		4	16-19	repeat Sub-Loop 0, but **ODT = 0** and **BA[2:0] = 4**												
		5	20-23	repeat Sub-Loop 0, but **ODT = 0** and **BA[2:0] = 5**												
		6	24-27	repeat Sub-Loop 0, but **ODT = 1** and **BA[2:0] = 6**												
		7	28-31	repeat Sub-Loop 0, but **ODT = 1** and **BA[2:0] = 7**												

NOTE:
1.DM must be driven LOW all the time. DQS, DQS# are MID-LEVEL.
2.DQ signals are MID-LEVEL.

10 IDD Specification Parameters and Test Conditions (Cont'd)
10.1 IDD and IDDQ Measurement Conditions (Cont'd)

Table 53 — IDD4R and IDDQ4R Measurement-Loop Pattern[1]

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[2]
toggling	Static High	0	0	RD	0	1	0	1	0	0	00	0	0	0	0	00000000
			1	D	1	0	0	0	0	0	00	0	0	0	0	-
			2, 3	D#,D#	1	1	1	1	0	0	00	0	0	0	0	-
			4	RD	0	1	0	1	0	0	00	0	0	F	0	**00110011**
			5	D	1	0	0	0	0	0	00	0	0	F	0	-
			6, 7	D#,D#	1	1	1	1	0	0	00	0	0	F	0	-
		1	8-15	repeat Sub-Loop 0, but **BA[2:0] = 1**												
		2	16-23	repeat Sub-Loop 0, but **BA[2:0] = 2**												
		3	24-31	repeat Sub-Loop 0, but **BA[2:0] = 3**												
		4	32-39	repeat Sub-Loop 0, but **BA[2:0] = 4**												
		5	40-47	repeat Sub-Loop 0, but **BA[2:0] = 5**												
		6	48-55	repeat Sub-Loop 0, but **BA[2:0] = 6**												
		7	56-63	repeat Sub-Loop 0, but **BA[2:0] = 7**												

NOTE:
1.DM must be driven LOW all the time. DQS, DQS# are used according to RD Commands, otherwise MID-LEVEL.
2.Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are MID-LEVEL.

Table 54 — IDD4W Measurement-Loop Pattern[1]

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[2]
toggling	Static High	0	0	WR	0	1	0	0	1	0	00	0	0	0	0	00000000
			1	D	1	0	0	0	1	0	00	0	0	0	0	-
			2, 3	D#,D#	1	1	1	1	1	0	00	0	0	0	0	-
			4	WR	0	1	0	0	1	0	00	0	0	F	0	**00110011**
			5	D	1	0	0	0	1	0	00	0	0	F	0	-
			6, 7	D#,D#	1	1	1	1	1	0	00	0	0	F	0	-
		1	8-15	repeat Sub-Loop 0, but **BA[2:0] = 1**												
		2	16-23	repeat Sub-Loop 0, but **BA[2:0] = 2**												
		3	24-31	repeat Sub-Loop 0, but **BA[2:0] = 3**												
		4	32-39	repeat Sub-Loop 0, but **BA[2:0] = 4**												
		5	40-47	repeat Sub-Loop 0, but **BA[2:0] = 5**												
		6	48-55	repeat Sub-Loop 0, but **BA[2:0] = 6**												
		7	56-63	repeat Sub-Loop 0, but **BA[2:0] = 7**												

NOTE:
1.DM must be driven LOW all the time. DQS, DQS# are used according to WR Commands, otherwise MID-LEVEL.
2.Burst Sequence driven on each DQ signal by Write Command. Outside burst operation, DQ signals are MID-LEVEL.

10 IDD Specification Parameters and Test Conditions (Cont'd)
10.1 IDD and IDDQ Measurement Conditions (Cont'd)

Table 55 — IDD5B Measurement-Loop Pattern[1]

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[2]
toggling	Static High	0	0	**REF**	0	0	0	1	0	**0**	0	0	0	**0**	0	-
		1	1, 2	D, D	1	0	0	0	0	0	00	0	0	0	0	-
			3, 4	D#, D#	1	1	1	1	0	0	00	0	0	F	0	-
			5...8	repeat cycles 1...4, but **BA[2:0] = 1**												
			9...12	repeat cycles 1...4, but **BA[2:0] = 2**												
			13...16	repeat cycles 1...4, but **BA[2:0] = 3**												
			17...20	repeat cycles 1...4, but **BA[2:0] = 4**												
			21...24	repeat cycles 1...4, but **BA[2:0] = 5**												
			25...28	repeat cycles 1...4, but **BA[2:0] = 6**												
			29...32	repeat cycles 1...4, but **BA[2:0] = 7**												
		2	33 ... nRFC - 1	**repeat Sub-Loop 1, until nRFC - 1**. Truncate, if necessary.												

NOTE:
1.DM must be driven Low all the time. DQS, DQS# are MID-LEVEL.
2.DQ signals are MID-LEVEL.

10 IDD Specification Parameters and Test Conditions (Cont'd)
10.1 IDD and IDDQ Measurement Conditions (Cont'd)

Table 56 — IDD7 Measurement-Loop Pattern[1]

ATTENTION: Sub-Loops 10-19 have inverse A[6:3] Pattern and Data Pattern than Sub-Loops 0-9

CK, CK#	CKE	Sub-Loop	Cycle Number	Command	CS#	RAS#	CAS#	WE#	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[2]
toggling	Static High	0	0	ACT	0	0	1	1	0	0	00	0	0	0	0	-
			1	RDA	0	1	0	1	0	0	00	1	0	0	0	00000000
			2	D	1	0	0	0	0	0	00	0	0	0	0	-
			...	repeat above D Command until nRRD - 1												
		1	nRRD	ACT	0	0	1	1	0	1	00	0	0	F	0	-
			nRRD + 1	RDA	0	1	0	1	0	1	00	1	0	F	0	**00110011**
			nRRD + 2	D	1	0	0	0	0	1	00	0	0	F	0	-
			...	repeat above D Command until 2 * nRRD -1												
		2	2 * nRRD	repeat Sub-Loop 0, but **BA[2:0] = 2**												
		3	3 * nRRD	repeat Sub-Loop 1, but **BA[2:0] = 3**												
		4	4 * nRRD	D	1	0	0	0	0	3	00	0	0	F	0	-
				Assert and repeat above D Command until nFAW - 1, if necessary												
		5	nFAW	repeat Sub-Loop 0, but **BA[2:0] = 4**												
		6	nFAW+nRRD	repeat Sub-Loop 1, but **BA[2:0] = 5**												
		7	nFAW+2*nRRD	repeat Sub-Loop 0, but **BA[2:0] = 6**												
		8	nFAW+3*nRRD	repeat Sub-Loop 1, but **BA[2:0] = 7**												
		9	nFAW+4*nRRD	D	1	0	0	0	0	7	00	0	0	F	0	-
				Assert and repeat above D Command until 2 * nFAW - 1, if necessary												
		10	2*nFAW+0	ACT	0	0	1	1	0	0	00	0	0	F	0	-
			2*nFAW+1	RDA	0	1	0	1	0	0	00	1	0	F	0	**00110011**
			2*nFAW+2	D	1	0	0	0	0	0	00	0	0	F	0	-
				Repeat above D Command until 2 * nFAW + nRRD - 1												
		11	2*nFAW+nRRD	ACT	0	0	1	1	0	1	00	0	0	0	0	-
			2*nFAW+nRRD+1	RDA	0	1	0	1	0	1	00	1	0	0	0	00000000
			2*nFAW+nRRD+2	D	1	0	0	0	0	1	00	0	0	0	0	-
				repeat above D Command until 2 * nFAW + 2 * nRRD -1												
		12	2*nFAW+2*nRRD	repeat Sub-Loop 10, but **BA[2:0] = 2**												
		13	2*nFAW+3*nRRD	repeat Sub-Loop 11, but **BA[2:0] = 3**												
		14	2*nFAW+4 * nRRD	D	1	0	0	0	0	3	00	0	0	0	0	-
				Assert and repeat above D Command until 3 * nFAW - 1, if necessary												
		15	3*nFAW	repeat Sub-Loop 10, but **BA[2:0] = 4**												
		16	3*nFAW+nRRD	repeat Sub-Loop 11, but **BA[2:0] = 5**												
		17	3*nFAW+2*nRRD	repeat Sub-Loop 10, but **BA[2:0] = 6**												
		18	3*nFAW+3*nRRD	repeat Sub-Loop 11, but **BA[2:0] = 7**												
		19	3*nFAW+4*nRRD	D	1	0	0	0	0	7	00	0	0	0	0	-
				Assert and repeat above D Command until 4 * nFAW - 1, if necessary												

NOTE:
1.DM must be driven LOW all the time. DQS, DQS# are used according to RD Commands, otherwise MID-LEVEL
2.Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are MID-LEVEL.

10.2 IDD Specifications

IDD values are for full operating range of voltage and temperature unless otherwise noted.

Table 57 — I_{DD} Specification Example 512M DDR3

Speed Grade Bin	DDR3 - 800 5-5-5	DDR3 - 1066 7-7-7	DDR3 - 1333 8-8-8	DDR3 - 1600 9-9-9		
Symbol	**Max.**	**Max.**	**Max.**	**Max.**	**Unit**	**Notes**
I_{DD0}					mA	x4/x8
					mA	x16
I_{DD1}					mA	x4/x8
					mA	x16
I_{DD2P} (0) slow exit					mA	x4/x8/x16
I_{DD2P} (1) fast exit					mA	x4/x8/x16
I_{DD2N}					mA	x4/x8/x16
I_{DD2NT}					mA	x4/x8
					mA	x16
I_{DDQ2NT} (Optional)					mA	x4/x8
					mA	x16
I_{DD2Q}					mA	x4/x8/x16
I_{DD3P} (fast exit)					mA	x4/x8/x16
I_{DD3N}					mA	x4/x8/x16
I_{DD4R}					mA	x4
					mA	x8
					mA	x16
I_{DDQ4R} (Optional)					mA	x4
					mA	x8
					mA	x16
I_{DD4W}					mA	x4
					mA	x8
					mA	x16
I_{DD5B}					mA	x4/x8/x16
I_{DD6}					mA	Refer to Table 58 on page 151
I_{DD6ET}[1]					mA	
I_{DD6TC1}					mA	
I_{DD7}					mA	x4/x8
					mA	x16

NOTE 1. Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR3 SDRAM devices support the following options or requirements referred to in this material.

10 IDD Specification Parameters and Test Conditions (Cont'd)
10.2 IDD Specifications (Cont'd)

Table 58 — I_{DD6} Specification

Symbol	Temperature Range	Value	Unit	Notes
I_{DD6}	0 - 85 °C		mA	3,4
I_{DD6ET}	0 - 95 °C		mA	5,6
I_{DD6TC}	0 °C ~ T_a		mA	6,7,8
	T_b ~ T_y		mA	6,7,8
	T_z ~ $T_{OPERmax}$		mA	6,7,8

NOTE 1. Some I_{DD} currents are higher for x16 organization due to larger page-size architecture.

NOTE 2. Max. values for I_{DD} currents considering worst case conditions of process, temperature and voltage.

NOTE 3. Applicable for MR2 settings A6=0 and A7=0.

NOTE 4. Supplier data sheets include a max value for I_{DD6}.

NOTE 5. Applicable for MR2 settings A6=0 and A7=1. I_{DD6ET} is only specified for devices which support the Extended Temperature Range feature.

NOTE 6. Refer to the supplier data sheet for the value specification method (e.g. max, typical) for I_{DD6ET} and I_{DD6TC}

NOTE 7. Applicable for MR2 settings A6=1 and A7=0. I_{DD6TC} is only specified for devices which support the Auto Self Refresh feature.

NOTE 8. The number of discrete temperature ranges supported and the associated Ta - Tz values are supplier/design specific. Temperature ranges are specified for all supported values of T_{OPER}. Refer to supplier data sheet for more information.

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11 Input/Output Capacitance

11.1 Input/Output Capacitance

Table 59 — Input / Output Capacitance

		DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
Input/output capacitance (DQ, DM, DQS, DQS#, TDQS,TDQS#)	C_{IO}	1.5	3.0	1.5	2.7	1.5	2.5	1.5	2.3	pF	1,2,3
Input capacitance, CK and CK#	C_{CK}	0.8	1.6	0.8	1.6	0.8	1.4	0.8	1.4	pF	2,3
Input capacitance delta, CK and CK#	C_{DCK}	0	0.15	0	0.15	0	0.15	0	0.15	pF	2,3,4
Input/output capacitance delta DQS and DQS#	C_{DDQS}	0	0.2	0	0.2	0	0.15	0	0.15	pF	2,3,5
Input capacitance, (CTRL, ADD, CMD input-only pins)	C_{I}	0.75	1.5	0.75	1.5	0.75	1.3	0.75	1.3	pF	2,3,6
Input capacitance delta, (All CTRL input-only pins	C_{DI_CTRL}	-0.5	0.3	-0.5	0.3	-0.4	0.2	-0.4	0.2	pF	2,3,7,8
Input capacitance delta, (All ADD/ CMD input-only pins)	$C_{DI_ADD_CMD}$	-0.5	0.5	-0.5	0.5	-0.4	0.4	-0.4	0.4	pF	2,3,9, 10
Input/output capacitance delta, DQ, DM, DQS, DQS#, TDQS, TDQS#	C_{DIO}	-0.5	0.3	-0.5	0.3	-0.5	0.3	-0.5	0.3	pF	2,3,11
Input/output capacitance of ZQ pin	C_{ZQ}	-	3	-	3	-	3	-	3	pF	2,3,12

NOTE 1. Although the DM, TDQS and TDQS# pins have different functions, the loading matches DQ and DQS

NOTE 2. This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147("PROCEDURE FOR MEASURING INPUT CAPACITANCE USING A VECTOR NETWORK ANALYZER(VNA)") with VDD, VDDQ, VSS, VSSQ applied and all other pins floating (except the pin under test, CKE, RESET# and ODT as necessary). VDD=VDDQ=1.5V, VBIAS=VDD/2 and on-die termination off.

NOTE 3. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here

NOTE 4. Absolute value of C_{CK}-C_{CK}#

NOTE 5. Absolute value of C_{IO}(DQS)-C_{IO}(DQS#)

NOTE 6. C_I applies to ODT, CS#, CKE, A0-A15, BA0-BA2, RAS#, CAS#, WE#.

NOTE 7. C_{DI_CTRL} applies to ODT, CS# and CKE

NOTE 8. C_{DI_CTRL}=C_I(CTRL)-0.5*(C_I(CLK)+C_I(CLK#))

NOTE 9. $C_{DI_ADD_CMD}$ applies to A0-A15, BA0-BA2, RAS#, CAS# and WE#

NOTE 10. $C_{DI_ADD_CMD}$=C_I(ADD_CMD) - 0.5*(C_I(CLK)+C_I(CLK#))

NOTE 11. C_{DIO}=C_{IO}(DQ,DM) - 0.5*(C_{IO}(DQS)+C_{IO}(DQS#))

NOTE 12. Maximum external load capacitance on ZQ pin: 5 pF.

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12 Electrical Characteristics & AC Timing for DDR3-800 to DDR3-1600

12.1 Clock Specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input clocks violating the min/max values may result in malfunction of the DDR3 SDRAM device.

12.1.1 Definition for tCK(avg)

tCK(avg) is calculated as the average clock period across any consecutive 200 cycle window, where each clock period is calculated from rising edge to rising edge.

$$tCK(avg) = \left(\sum_{j=1}^{N} tCK_j \right) / N$$

$$where \qquad N = 200$$

12.1.2 Definition for tCK(abs)

tCK(abs) is defined as the absolute clock period, as measured from one rising edge to the next consecutive rising edge. tCK(abs) is not subject to production test.

12.1.3 Definition for tCH(avg) and tCL(avg)

tCH(avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

$$tCH(avg) = \left(\sum_{j=1}^{N} tCH_j \right) / (N \times tCK(avg))$$

$$where \qquad N = 200$$

tCL(avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$tCL(avg) = \left(\sum_{j=1}^{N} tCL_j \right) / (N \times tCK(avg))$$

$$where \qquad N = 200$$

12.1.4 Definition for tJIT(per) and tJIT(per,lck)

tJIT(per) is defined as the largest deviation of any signal tCK from tCK(avg).

12.1 Clock Specification (Cont'd)
12.1.4 Definition for tJIT(per) and tJIT(per,lck) (Cont'd)

tJIT(per) = Min/max of $\{tCK_i - tCK(avg)$ where i = 1 to 200$\}$.

tJIT(per) defines the single period jitter when the DLL is already locked.

tJIT(per,lck) uses the same definition for single period jitter, during the DLL locking period only.

tJIT(per) and tJIT(per,lck) are not subject to production test.

12.1.5 Definition for tJIT(cc) and tJIT(cc,lck)

tJIT(cc) is defined as the absolute difference in clock period between two consecutive clock cycles.

tJIT(cc) = Max of $|\{tCK_{i+1} - tCK_i\}|$.

tJIT(cc) defines the cycle to cycle jitter when the DLL is already locked.

tJIT(cc,lck) uses the same definition for cycle to cycle jitter, during the DLL locking period only.

tJIT(cc) and tJIT(cc,lck) are not subject to production test.

12.1.6 Definition for tERR(nper)

tERR is defined as the cumulative error across n multiple consecutive cycles from tCK(avg). tERR is not subject to production test.

12.2 Refresh parameters by device density

Table 60 — Refresh parameters by device density

Parameter	Symbol		512Mb	1Gb	2Gb	4Gb	8Gb	Units	Notes
REF command to ACT or REF command time	tRFC		90	110	160	300	350	ns	
Average periodic refresh interval	tREFI	0 °C ≤ T_{CASE} ≤ 85 °C	7.8	7.8	7.8	7.8	7.8	µs	
		85 °C < T_{CASE} ≤ 95 °C	3.9	3.9	3.9	3.9	3.9	µs	1

NOTE 1. Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR3 SDRAM devices support the following options or requirements referred to in this material.

12.3 Standard Speed Bins

DDR3 SDRAM Standard Speed Bins include tCK, tRCD, tRP, tRAS and tRC for each corresponding bin.

Table 61 — DDR3-800 Speed Bins and Operating Conditions

For specific Notes See 12.3.1 "Speed Bin Table Notes" on page 161.								
Speed Bin			**DDR3-800D**		**DDR3-800E**		**Unit**	**Notes**
CL - nRCD - nRP			**5-5-5**		**6-6-6**			
Parameter		**Symbol**	**min**	**max**	**min**	**max**		
Internal read command to first data		t_{AA}	12.5	20	15	20	ns	
ACT to internal read or write delay time		t_{RCD}	12.5	—	15	—	ns	
PRE command period		t_{RP}	12.5	—	15	—	ns	
ACT to ACT or REF command period		t_{RC}	50	—	52.5	—	ns	
ACT to PRE command period		t_{RAS}	37.5	9 * tREFI	37.5	9 * tREFI	ns	
CL = 5	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	Reserved		ns	1,2,3,4,
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	2.5	3.3	ns	1,2,3,
Supported CL Settings			5, 6		6		n_{CK}	
Supported CWL Settings			5		5		n_{CK}	

12 Electrical Characteristics & AC Timing for DDR3-800 to DDR3-1600 (Cont'd)
12.3 Standard Speed Bins (Cont'd)

Table 62 — DDR3-1066 Speed Bins and Operating Conditions

For specific Notes See 12.3.1 "Speed Bin Table Notes" on page 161.											
Speed Bin			**DDR3-1066E**		**DDR3-1066F**		**DDR3-1066G**		**Unit**	**Note**
CL - nRCD - nRP			**6-6-6**		**7-7-7**		**8-8-8**			
Parameter		**Symbol**	**min**	**max**	**min**	**max**	**min**	**max**		
Internal read command to first data		t_{AA}	11.25	20	13.125	20	15	20	ns	
ACT to internal read or write delay time		t_{RCD}	11.25	—	13.125	—	15	—	ns	
PRE command period		t_{RP}	11.25	—	13.125	—	15	—	ns	
ACT to ACT or REF command period		t_{RC}	48.75	—	50.625	—	52.5	—	ns	
ACT to PRE command period		t_{RAS}	37.5	9 * tREFI	37.5	9 * tREFI	37.5	9 * tREFI	ns	
CL = 5	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	Reserved		Reserved		ns	1,2,3,4,6,
	CWL = 6	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		ns	4,
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	2.5	3.3	2.5	3.3	ns	1,2,3,6,
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	Reserved		Reserved		ns	1,2,3,4,
CL = 7	CWL = 5	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		ns	4,
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	1.875	< 2.5	Reserved		ns	1,2,3,4,
CL = 8	CWL = 5	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		ns	4,
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	1.875	< 2.5	1.875	< 2.5	ns	1,2,3,
Supported CL Settings			5, 6, 7, 8		6, 7, 8		6, 8		n_{CK}	
Supported CWL Settings			5, 6		5, 6		5, 6		n_{CK}	

12 Electrical Characteristics & AC Timing for DDR3-800 to DDR3-1600 (Cont'd)
12.3 Standard Speed Bins (Cont'd)

Table 63 — DDR3-1333 Speed Bins and Operating Conditions

For specific Notes See 12.3.1 "Speed Bin Table Notes" on page 161.													
Speed Bin			**DDR3-1333F (optional)**		**DDR3-1333G**		**DDR3-1333H**		**DDR3-1333J (optional)**		**Unit**	**Note**
CL - nRCD - nRP			**7-7-7**		**8-8-8**		**9-9-9**		**10-10-10**			
Parameter		**Symbol**	**min**	**max**	**min**	**max**	**min**	**max**	**min**	**max**		
Internal read command to first data		t_{AA}	10.5	20	12	20	13.5	20	15	20	ns	
ACT to internal read or write delay time		t_{RCD}	10.5	—	12	—	13.5	—	15	—	ns	
PRE command period		t_{RP}	10.5	—	12	—	13.5	—	15	—	ns	
ACT to ACT or REF command period		t_{RC}	46.5	—	48	—	49.5	—	51	—	ns	
ACT to PRE command period		t_{RAS}	36	9 * tREFI	36	9 * tREFI	36	9 * tREFI	36	9 * tREFI	ns	
CL = 5	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	2.5	3.3	Reserved		Reserved		ns	1,2,3,4,7
	CWL = 6, 7	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	2.5	3.3	2.5	3.3	2.5	3.3	ns	1,2,3,7
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	Reserved		Reserved		Reserved		ns	1,2,3,4,7
	CWL = 7	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
CL = 7	CWL = 5	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	1.875	< 2.5	Reserved		Reserved		ns	1,2,3,4,7
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	Reserved		Reserved		Reserved		ns	1,2,3,4
CL = 8	CWL = 5	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	1.875	< 2.5	1.875	< 2.5	1.875	< 2.5	ns	1,2,3,7
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	1.5	<1.875	Reserved		Reserved		ns	1,2,3,4
CL = 9	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	1.5	<1.875	1.5	<1.875	Reserved		ns	1,2,3,4
CL = 10	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	1.5	<1.875	1.5	<1.875	1.5	<1.875	ns	1,2,3
			(Optional)		(Optional)		(Optional)				ns	5
Supported CL Settings			5, 6, 7, 8, 9, (10)		5, 6, 7, 8, 9, (10)		6, 8, 9, (10)		6, 8, 10		n_{CK}	
Supported CWL Settings			5, 6, 7		5, 6, 7		5, 6, 7		5, 6, 7		n_{CK}	

12 Electrical Characteristics & AC Timing for DDR3-800 to DDR3-1600 (Cont'd)
12.3 Standard Speed Bins (Cont'd)

Table 64 — DDR3-1600 Speed Bins and Operating Conditions

For specific Notes See 12.3.1 "Speed Bin Table Notes" on page 161.												
Speed Bin			**DDR3-1600G (optional)**		**DDR3-1600H**		**DDR3-1600J**		**DDR3-1600K (optional)**		**Unit**	**Note**
CL - nRCD - nRP			**8-8-8**		**9-9-9**		**10-10-10**		**11-11-11**			
Parameter		**Symbol**	**min**	**max**	**min**	**max**	**min**	**max**	**min**	**max**		
Internal read command to first data		t_{AA}	10	20	11.25	20	12.5	20	13.75	20	ns	
ACT to internal read or write delay time		t_{RCD}	10	—	11.25	—	12.5	—	13.75	—	ns	
PRE command period		t_{RP}	10	—	11.25	—	12.5	—	13.75	—	ns	
ACT to ACT or REF command period		t_{RC}	45	—	46.25	—	47.5	—	48.75	—	ns	
ACT to PRE command period		t_{RAS}	35	9 * tREFI	35	9 * tREFI	35	9 * tREFI	35	9 * tREFI	ns	
CL = 5	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	2.5	3.3	2.5	3.3	Reserved		ns	1,2,3,4,8
	CWL = 6, 7, 8	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	2.5	3.3	2.5	3.3	2.5	3.3	ns	1,2,3,8
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	1.875	< 2.5	Reserved		Reserved		ns	1,2,3,4,8
	CWL = 7, 8	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
CL = 7	CWL = 5	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	1.875	< 2.5	1.875	< 2.5	Reserved		ns	1,2,3,4,8
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	Reserved		Reserved		Reserved		ns	1,2,3,4,8
	CWL = 8	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
CL = 8	CWL = 5	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	1.875	< 2.5	1.875	< 2.5	1.875	< 2.5	ns	1,2,3,8
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	1.5	<1.875	Reserved		Reserved		ns	1,2,3,4,8
	CWL = 8	$t_{CK(AVG)}$	1.25	< 1.5	Reserved		Reserved		Reserved		ns	1,2,3,4
CL = 9	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	1.5	<1.875	1.5	<1.875	Reserved		ns	1,2,3,4,8
	CWL = 8	$t_{CK(AVG)}$	1.25	< 1.5	1.25	< 1.5	Reserved		Reserved		ns	1,2,3,4
CL = 10	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	1.5	<1.875	1.5	<1.875	1.5	<1.875	ns	1,2,3,8
	CWL = 8	$t_{CK(AVG)}$	1.25	< 1.5	1.25	< 1.5	1.25	< 1.5	Reserved		ns	1,2,3,4
CL = 11	CWL = 5, 6, 7	$t_{CK(AVG)}$	Reserved		Reserved		Reserved		Reserved		ns	4
	CWL = 8	$t_{CK(AVG)}$	1.25	< 1.5	1.25	< 1.5	1.25	< 1.5	1.25	< 1.5	ns	1,2,3
			(Optional)		(Optional)		(Optional)				ns	5
Supported CL Settings			5, 6, 7, 8, 9, 10, (11)		5, 6, 7, 8, 9, 10, (11)		5, 6, 7, 8, 9, 10, (11)		6, 8, 10, 11		n_{CK}	
Supported CWL Settings			5, 6, 7, 8		5, 6, 7, 8		5, 6, 7, 8		5, 6, 7, 8		n_{CK}	

12 Electrical Characteristics & AC Timing for DDR3-800 to DDR3-1600 (Cont'd)
12.3 Standard Speed Bins (Cont'd)

12.3.1 Speed Bin Table Notes

Absolute Specification (T_{OPER}; V_{DDQ} = V_{DD} = 1.5V +/- 0.075 V);

NOTE 1. The CL setting and CWL setting result in tCK(AVG).MIN and tCK(AVG).MAX requirements. When making a selection of tCK(AVG), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.

NOTE 2. tCK(AVG).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK(AVG) value (2.5, 1.875, 1.5, or 1.25 ns) when calculating CL [nCK] = tAA [ns] / tCK(AVG) [ns], rounding up to the next 'Supported CL'.

NOTE 3. tCK(AVG).MAX limits: Calculate tCK(AVG) = tAA.MAX / CL SELECTED and round the resulting tCK(AVG) down to the next valid speed bin (i.e. 3.3ns or 2.5ns or 1.875 ns or 1.25 ns). This result is tCK(AVG).MAX corresponding to CL SELECTED.

NOTE 4. 'Reserved' settings are not allowed. User must program a different value.

NOTE 5. 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Refer to supplier's data sheet and/or the DIMM SPD information if and how this setting is supported.

NOTE 6. Any DDR3-1066 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.

NOTE 7. Any DDR3-1333 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.

NOTE 8. Any DDR3-1600 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.

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Table 65 — Timing Parameters by Speed Bin

NOTE: The following general notes from page 170 apply to Table 65: Note a. VDD =VDDQ = 1.5V +/- 0.075V

		DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
Clock Timing											
Minimum Clock Cycle Time (DLL off mode)	tCK (DLL_OFF)	8	-	8	-	8	-	8	-	ns	6
Average Clock Period	tCK(avg)	See 12.3 “Standard Speed Bins” on page 157								ps	
Average high pulse width	tCH(avg)	0.47	0.53	0.47	0.53	0.47	0.53	0.47	0.53	tCK(avg)	
Average low pulse width	tCL(avg)	0.47	0.53	0.47	0.53	0.47	0.53	0.47	0.53	tCK(avg)	
Absolute Clock Period	tCK(abs)	tCK(avg)min + tJIT(per)min	tCK(avg) max + tJIT(per) max	tCK(avg)min + tJIT(per)min	tCK(avg) max + tJIT(per) max	tCK(avg)min + tJIT(per)min	tCK(avg) max + tJIT(per) max	tCK(avg)min + tJIT(per)min	tCK(avg) max + tJIT(per) max	ps	
Absolute clock HIGH pulse width	tCH(abs)	0.43	-	0.43	-	0.43	-	0.43	-	tCK(avg)	25
Absolute clock LOW pulse width	tCL(abs)	0.43	-	0.43	-	0.43	-	0.43	-	tCK(avg)	26
Clock Period Jitter	JIT(per)	- 100	100	- 90	90	- 80	80	-70	70	ps	
Clock Period Jitter during DLL locking period	tJIT(per, lck)	- 90	90	- 80	80	- 70	70	-60	60	ps	
Cycle to Cycle Period Jitter	tJIT(cc)	200		180		160		140		ps	
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	180		160		140		120		ps	
Duty Cycle Jitter	tJIT(duty)	-	-	-	-	-	-	-	-	ps	
Cumulative error across 2 cycles	tERR(2per)	- 147	147	- 132	132	- 118	118	- 103	103	ps	
Cumulative error across 3 cycles	tERR(3per)	- 175	175	- 157	157	- 140	140	- 122	122	ps	
Cumulative error across 4 cycles	tERR(4per)	- 194	194	- 175	175	- 155	155	- 136	136	ps	
Cumulative error across 5 cycles	tERR(5per)	- 209	209	- 188	188	- 168	168	- 147	147	ps	
Cumulative error across 6 cycles	tERR(6per)	- 222	222	- 200	200	- 177	177	- 155	155	ps	
Cumulative error across 7 cycles	tERR(7per)	- 232	232	- 209	209	- 186	186	- 163	163	ps	

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Table 65 — Timing Parameters by Speed Bin (Cont'd)

NOTE: The following general notes from page 170 apply to Table 65: Note a. VDD =VDDQ = 1.5V +/- 0.075V

		DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
Cumulative error across 8 cycles	tERR(8per)	- 241	241	- 217	217	- 193	193	- 169	169	ps	
Cumulative error across 9 cycles	tERR(9per)	- 249	249	- 224	224	- 200	200	- 175	175	ps	
Cumulative error across 10 cycles	tERR(10per)	- 257	257	- 231	231	- 205	205	- 180	180	ps	
Cumulative error across 11 cycles	tERR(11per)	- 263	263	- 237	237	- 210	210	- 184	184	ps	
Cumulative error across 12 cycles	tERR(12per)	- 269	269	- 242	242	- 215	215	- 188	188	ps	
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR(nper)	^{t}ERR(nper)min = (1 + 0.68ln(n)) * ^{t}JIT(per)min ^{t}ERR(nper)max = (1 + 0.68ln(n)) * ^{t}JIT(per)max								ps	24
Data Timing											
DQS, DQS# to DQ skew, per group, per access	tDQSQ	-	200	-	150	-	125	-	100	ps	13
DQ output hold time from DQS, DQS#	tQH	0.38	-	0.38	-	0.38	-	0.38	-	tCK(avg)	13, g
DQ low-impedance time from CK, CK#	tLZ(DQ)	- 800	400	- 600	300	- 500	250	- 450	225	ps	13, 14, f
DQ high impedance time from CK, CK#	tHZ(DQ)	-	400	-	300	-	250	-	225	ps	13, 14, f
Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels	tDS(base)	75		25		30		10		ps	d, 17
Data hold time from DQS, DQS# referenced to Vih(dc) / Vil(dc) levels	tDH(base)	150		100		65		45		ps	d, 17
DQ and DM Input pulse width for each input	tDIPW	600	-	490	-	400	-	360	-	ps	28
Data Strobe Timing											
DQS,DQS# differential READ Preamble	tRPRE	0.9	Note 19	0.9	Note 19	0.9	Note 19	0.9	Note 19	tCK(avg)	13, 19, g
DQS, DQS# differential READ Postamble	tRPST	0.3	Note 11	0.3	Note 11	0.3	Note 11	0.3	Note 11	tCK(avg)	11, 13, g
DQS, DQS# differential output high time	tQSH	0.38	-	0.38	-	0.40	-	0.40	-	tCK(avg)	13, g
DQS, DQS# differential output low time	tQSL	0.38	-	0.38	-	0.40	-	0.40	-	tCK(avg)	13, g
DQS, DQS# differential WRITE Preamble	tWPRE	0.9	-	0.9	-	0.9	-	0.9	-	tCK(avg)	
DQS, DQS# differential WRITE Postamble	tWPST	0.3	-	0.3	-	0.3	-	0.3	-	tCK(avg)	
DQS, DQS# rising edge output access time from rising CK, CK#	tDQSCK	- 400	400	- 300	300	- 255	255	- 225	225	ps	13, f

Table 65 — Timing Parameters by Speed Bin (Cont'd)

NOTE: The following general notes from page 170 apply to Table 65: Note a. VDD =VDDQ = 1.5V +/- 0.075V

		DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
DQS and DQS# low-impedance time (Referenced from RL - 1)	tLZ(DQS)	- 800	400	- 600	300	- 500	250	- 450	225	ps	13, 14, f
DQS and DQS# high-impedance time (Referenced from RL + BL/2)	tHZ(DQS)	-	400	-	300	-	250	-	225	ps	13, 14, f
DQS, DQS# differential input low pulse width	tDQSL	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK(avg)	29, 31
DQS, DQS# differential input high pulse width	tDQSH	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK(avg)	30, 31
DQS, DQS# rising edge to CK, CK# rising edge	tDQSS	- 0.25	0.25	- 0.25	0.25	- 0.25	0.25	- 0.27	0.27	tCK(avg)	c
DQS, DQS# falling edge setup time to CK, CK# rising edge	tDSS	0.2	-	0.2	-	0.2	-	0.18	-	tCK(avg)	c, 32
DQS, DQS# falling edge hold time from CK, CK# rising edge	tDSH	0.2	-	0.2	-	0.2	-	0.18	-	tCK(avg)	c, 32
Command and Address Timing											
DLL locking time	tDLLK	512	-	512	-	512	-	512	-	nCK	
Internal READ Command to PRECHARGE Command delay	tRTP	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-		e
Delay from start of internal write transaction to internal read command	tWTR	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-		e, 18
WRITE recovery time	tWR	15	-	15	-	15	-	15	-	ns	e, 18
Mode Register Set command cycle time	tMRD	4	-	4	-	4	-	4	-	nCK	
Mode Register Set command update delay	tMOD	max(12nCK, 15ns)	-	max(12nCK, 15ns)	-	max(12nCK, 15ns)	-	max(12nCK, 15ns)	-		
ACT to internal read or write delay time	tRCD	Refer to Table 61 to Table 64 on pages pages 157 to pages 160									e
PRE command period	tRP	Refer to Table 61 to Table 64 on pages pages 157 to pages 160									e
ACT to ACT or REF command period	tRC	Refer to Table 61 to Table 64 on pages pages 157 to pages 160									e
CAS# to CAS# command delay	tCCD	4	-	4	-	4	-	4	-	nCK	
Auto precharge write recovery + precharge time	tDAL(min)	WR + roundup(tRP / tCK(avg))								nCK	
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-	1	-	1	-	nCK	22

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Table 65 — Timing Parameters by Speed Bin (Cont'd)

NOTE: The following general notes from page 170 apply to Table 65: Note a. VDD =VDDQ = 1.5V +/- 0.075V

		DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
ACTIVE to PRECHARGE command period	tRAS	See 12.3 "Standard Speed Bins" on page 157									e
ACTIVE to ACTIVE command period for 1KB page size	tRRD	max(4nCK, 10ns)	-	max(4nCK, 7.5ns)	-	max(4nCK, 6ns)	-	max(4nCK, 6ns)	-		e
ACTIVE to ACTIVE command period for 2KB page size	tRRD	max(4nCK, 10ns)	-	max(4nCK, 10ns)	-	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-		e
Four activate window for 1KB page size	tFAW	40	-	37.5	-	30	-	30	-	ns	e
Four activate window for 2KB page size	tFAW	50	-	50	-	45	-	40	-	ns	e
Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels	tIS(base)	200		125		65		45		ps	b, 16
Command and Address hold time from CK, CK# referenced to Vih(dc) / Vil(dc) levels	tIH(base)	275		200		140		120		ps	b, 16
Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels	tIS(base) AC150	200 + 150	-	125 + 150	-	65 + 125		45 + 125		ps	b, 16, 27
Control and Address Input pulse width for each input	tIPW	900	-	780	-	620	-	560	-	ps	28
Calibration Timing											
Power-up and RESET calibration time	tZQinit	512	-	512	-	512	-	512	-	nCK	
Normal operation Full calibration time	tZQoper	256	-	256	-	256	-	256	-	nCK	
Normal operation Short calibration time	tZQCS	64	-	64	-	64	-	64	-	nCK	23
Reset Timing											
Exit Reset from CKE HIGH to a valid command	tXPR	max(5nCK, tRFC(min) + 10ns)	-	max(5nCK, tRFC(min) + 10ns)	-	max(5nCK, tRFC(min) + 10ns)	-	max(5nCK, tRFC(min) + 10ns)	-		
Self Refresh Timings											
Exit Self Refresh to commands not requiring a locked DLL	tXS	max(5nCK, tRFC(min) + 10ns)	-	max(5nCK, tRFC(min) + 10ns)	-	max(5nCK, tRFC(min) + 10ns)	-	max(5nCK, tRFC(min) + 10ns)	-		
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	nCK	

Table 65 — Timing Parameters by Speed Bin (Cont'd)

NOTE: The following general notes from page 170 apply to Table 65: Note a. VDD =VDDQ = 1.5V +/- 0.075V

		DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
Minimum CKE low width for Self Refresh entry to exit timing	tCKESR	tCKE(min) + 1 nCK	-	tCKE(min) + 1 nCK	-	tCKE(min) + 1 nCK	-	tCKE(min) + 1 nCK	-		
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	max(5 nCK, 10 ns)	-	max(5 nCK, 10 ns)	-	max(5 nCK, 10 ns)	-	max(5 nCK, 10 ns)	-		
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max(5 nCK, 10 ns)	-	max(5 nCK, 10 ns)	-	max(5 nCK, 10 ns)	-	max(5 nCK, 10 ns)	-		
Power Down Timings											
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max(3nCK, 7.5ns)	-	max(3nCK, 7.5ns)	-	max(3nCK, 6ns)	-	max(3nCK, 6ns)	-		
Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	tXPDLL	max(10nCK, 24ns)	-	max(10nCK, 24ns)	-	max(10nCK, 24ns)	-	max(10nCK, 24ns)	-		2
CKE minimum pulse width	tCKE	max(3nCK 7.5ns)	-	max(3nCK, 5.625ns)	-	max(3nCK, 5.625ns)	-	max(3nCK, 5ns)	-		
Command pass disable delay	tCPDED	1	-	1	-	1	-	1	-	nCK	
Power Down Entry to Exit Timing	tPD	tCKE(min)	9 * tREFI	tCKE(min)	9 * tREFI	tCKE(min)	9 * tREFI	tCKE(min)	9 * tREFI		15
Timing of ACT command to Power Down entry	tACTPDEN	1	-	1	-	1	-	1	-	nCK	20
Timing of PRE or PREA command to Power Down entry	tPRPDEN	1	-	1	-	1	-	1	-	nCK	20
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL + 4 + 1	-	RL + 4 + 1	-	RL + 4 + 1	-	RL + 4 + 1	-	nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL + 4 + (tWR / tCK(avg))	-	WL + 4 + (tWR / tCK(avg))	-	WL + 4 + (tWR / tCK(avg))	-	WL + 4 + (tWR / tCK(avg))	-	nCK	9
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL + 4 + WR + 1	-	WL + 4 + WR + 1	-	WL + 4 + WR + 1	-	WL + 4 + WR + 1	-	nCK	10

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Table 65 — Timing Parameters by Speed Bin (Cont'd)

NOTE: The following general notes from page 170 apply to Table 65: Note a. VDD =VDDQ = 1.5V +/- 0.075V

		DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
Timing of WR command to Power Down entry (BC4MRS)	tWRPDEN	WL + 2 + (tWR / tCK(avg))	-	WL + 2 + (tWR / tCK(avg))	-	WL + 2 + (tWR / tCK(avg))	-	WL + 2 + (tWR / tCK(avg))	-	nCK	9
Timing of WRA command to Power Down entry (BC4MRS)	tWRAPDEN	WL + 2 + WR + 1	-	WL + 2 + WR + 1	-	WL + 2 + WR + 1	-	WL + 2 + WR + 1	-	nCK	10
Timing of REF command to Power Down entry	tREFPDEN	1	-	1	-	1	-	1	-	nCK	20, 21
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-		
ODT Timings											
ODT high time without write command or with write command and BC4	ODTH4	4	-	4	-	4	-	4	-	nCK	
ODT high time with Write command and BL8	ODTH8	6	-	6	-	6	-	6	-	nCK	
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONPD	2	8.5	2	8.5	2	8.5	2	8.5	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFPD	2	8.5	2	8.5	2	8.5	2	8.5	ns	
RTT turn-on	tAON	-400	400	-300	300	-250	250	-225	225	ps	7, f
RTT_Nom and RTT_WR turn-off time from ODTLoff reference	tAOF	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)	8, f
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)	f
Write Leveling Timings											
First DQS/DQS# rising edge after write leveling mode is programmed	tWLMRD	40	-	40	-	40	-	40	-	nCK	3
DQS/DQS# delay after write leveling mode is programmed	tWLDQSEN	25	-	25	-	25	-	25	-	nCK	3
Write leveling setup time from rising CK, CK# crossing to rising DQS, DQS# crossing	tWLS	325	-	245	-	195	-	165	-	ps	

Table 65 — Timing Parameters by Speed Bin (Cont'd)

NOTE: The following general notes from page 170 apply to Table 65: Note a. VDD =VDDQ = 1.5V +/- 0.075V

		DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
Write leveling hold time from rising DQS, DQS# crossing to rising CK, CK# crossing	tWLH	325	-	245	-	195	-	165	-	ps	
Write leveling output delay	tWLO	0	9	0	9	0	9	0	7.5	ns	
Write leveling output error	tWLOE	0	2	0	2	0	2	0	2	ns	

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13.1 Jitter Notes

Specific Note a Unit 'tCK(avg)' represents the actual tCK(avg) of the input clock under operation. Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges.ex) tMRD = 4 [nCK] means; if one Mode Register Set command is registered at Tm, another Mode Register Set command may be registered at Tm+4, even if (Tm+4 - Tm) is 4 x tCK(avg) + tERR(4per),min.

Specific Note b These parameters are measured from a command/address signal (CKE, CS#, RAS#, CAS#, WE#, ODT, BA0, A0, A1, etc.) transition edge to its respective clock signal (CK/CK#) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as the setup and hold are relative to the clock signal crossing that latches the command/address. That is, these parameters should be met whether clock jitter is present or not.

Specific Note c These parameters are measured from a data strobe signal (DQS(L/U), DQS(L/U)#) crossing to its respective clock signal (CK, CK#) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.

Specific Note d These parameters are measured from a data signal (DM(L/U), DQ(L/U)0, DQ(L/U)1, etc.) transition edge to its respective data strobe signal (DQS(L/U), DQS(L/U)#) crossing.

Specific Note e For these parameters, the DDR3 SDRAM device supports tnPARAM [nCK] = RU{ tPARAM [ns] / tCK(avg) [ns] }, which is in clock cycles, assuming all input clock jitter specifications are satisfied. For example, the device will support tnRP = RU{tRP / tCK(avg)}, which is in clock cycles, if all input clock jitter specifications are met. This means: For DDR3-800 6-6-6, of which tRP = 15ns, the device will support tnRP = RU{tRP / tCK(avg)} = 6, as long as the input clock jitter specifications are met, i.e. Precharge command at Tm and Active command at Tm+6 is valid even if (Tm+6 - Tm) is less than 15ns due to input clock jitter.

Specific Note f When the device is operated with input clock jitter, this parameter needs to be derated by the actual tERR(mper),act of the input clock, where 2 <= m <= 12. (output deratings are relative to the SDRAM input clock.)
For example, if the measured jitter into a DDR3-800 SDRAM has tERR(mper),act,min = - 172 ps and tERR(mper),act,max = + 193 ps, then tDQSCK,min(derated) = tDQSCK,min - tERR(mper),act,max = - 400 ps - 193 ps = - 593 ps and tDQSCK,max(derated) = tDQSCK,max - tERR(mper),act,min = 400 ps + 172 ps = + 572 ps. Similarly, tLZ(DQ) for DDR3-800 derates to tLZ(DQ),min(derated) = - 800 ps - 193 ps = - 993 ps and tLZ(DQ),max(derated) = 400 ps + 172 ps = + 572 ps. (Caution on the min/max usage!)
Note that tERR(mper),act,min is the minimum measured value of tERR(nper) where 2 <= n <= 12, and tERR(mper),act,max is the maximum measured value of tERR(nper) where 2 <= n <= 12.

Specific Note g When the device is operated with input clock jitter, this parameter needs to be derated by the actual tJIT(per),act of the input clock. (output deratings are relative to the SDRAM input clock.)
For example, if the measured jitter into a DDR3-800 SDRAM has tCK(avg),act = 2500 ps, tJIT(per),act,min = - 72 ps and tJIT(per),act,max = + 93 ps, then tRPRE,min(derated) = tRPRE,min + tJIT(per),act,min = 0.9 x tCK(avg),act + tJIT(per),act,min = 0.9 x 2500 ps - 72 ps = + 2178 ps. Similarly, tQH,min(derated) = tQH,min + tJIT(per),act,min = 0.38 x tCK(avg),act + tJIT(per),act,min = 0.38 x 2500 ps - 72 ps = + 878 ps. (Caution on the min/max usage!)

13.2 Timing Parameter Notes

NOTE 1. Actual value dependant upon measurement level definitions which are TBD.

NOTE 2. Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.

NOTE 3. The max values are system dependent.

NOTE 4. WR as programmed in mode register

NOTE 5. Value must be rounded-up to next higher integer value

NOTE 6. There is no maximum cycle time limit besides the need to satisfy the refresh interval, tREFI.

NOTE 7. For definition of RTT turn-on time tAON See 5.2.2 "Timing Parameters" on page 92.

NOTE 8. For definition of RTT turn-off time tAOF See 5.2.2 "Timing Parameters" on page 92.

NOTE 9. tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR / tCK to the next integer.

NOTE 10. WR in clock cycles as programmed in MR0.

NOTE 11. The maximum read postamble is bound by tDQSCK(min) plus tQSH(min) on the left side and tHZ(DQS)max on the right side. See Figure 28 — "Clock to Data Strobe Relationship" on page 58

NOTE 12. Output timing deratings are relative to the SDRAM input clock. When the device is operated with input clock jitter, this parameter needs to be derated by t.b.d.

NOTE 13. Value is only valid for RON34

NOTE 14. Single ended signal parameter. Refer to chapter <t.b.d.> for definition and measurement method.

NOTE 15. tREFI depends on TOPER

NOTE 16. tIS(base) and tIH(base) values are for 1V/ns CMD/ADD single-ended slew rate and 2V/ns CK, CK# differential slew rate. Note for DQ and DM signals, VREF(DC) = VRefDQ(DC). For input only pins except RESET#, VRef(DC) = VRefCA(DC). See 13.3 "Address / Command Setup, Hold and Derating" on page 173

NOTE 17. tDS(base) and tDH(base) values are for 1V/ns DQ single-ended slew rate and 2V/ns DQS, DQS# differential slew rate. Note for DQ and DM signals, VREF(DC) = VRefDQ(DC). For input only pins except RESET#, VRef(DC) = VRefCA(DC). See 13.4 "Data Setup, Hold and Slew Rate Derating" on page 180.

NOTE 18. Start of internal write transaction is defined as follows:

For BL8 (fixed by MRS and on- the-fly): Rising clock edge 4 clock cycles after WL.

For BC4 (on- the- fly): Rising clock edge 4 clock cycles after WL.

For BC4 (fixed by MRS): Rising clock edge 2 clock cycles after WL.

NOTE 19. The maximum read preamble is bound by tLZ(DQS)min on the left side and tDQSCK(max) on the right side. See Figure 28 — "Clock to Data Strobe Relationship" on page 58

NOTE 20. CKE is allowed to be registered low while operations such as row activation, precharge, auto-precharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.

NOTE 21. Although CKE is allowed to be registered LOW after a REFRESH command once tREFPDEN(min) is satisfied, there are cases where additional time such as tXPDLL(min) is also required. See 4.17.3 "Power-Down clarifications - Case 2" on page 87

NOTE 22. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.

13 Electrical Characteristics and AC Timing (Cont'd)
13.2 Timing Parameter Notes (Cont'd)

NOTE 23. One ZQCS command can effectively correct a minimum of 0.5 % (ZQ Correction) of RON and RTT impedance error within 64 nCK for all speed bins assuming the maximum sensitivities specified in the 'Output Driver Voltage and Temperature Sensitivity' and 'ODT Voltage and Temperature Sensitivity' tables. The appropriate interval between ZQCS commands can be determined from these tables and other application-specific parameters.

One method for calculating the interval between ZQCS commands, given the temperature (Tdriftrate) and voltage (Vdriftrate) drift rates that the SDRAM is subject to in the application, is illustrated. The interval could be defined by the following formula:

$$\frac{ZQCorrection}{(TSens \times Tdriftrate) + (VSens \times Vdriftrate)}$$

where TSens = max(dRTTdT, dRONdTM) and VSens = max(dRTTdV, dRONdVM) define the SDRAM temperature and voltage sensitivities.

For example, if TSens = 1.5% / ^{o}C, VSens = 0.15% / mV, Tdriftrate = 1 ^{o}C / sec and Vdriftrate = 15 mV / sec, then the interval between ZQCS commands is calculated as:

$$\frac{0.5}{(1.5 \times 1) + (0.15 \times 15)} = 0.133 \approx 128ms$$

NOTE 24. n = from 13 cycles to 50 cycles. This row defines 38 parameters.

NOTE 25. tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.

NOTE 26. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.

NOTE 27. The tIS(base) AC150 specifications are adjusted from the tIS(base) specification by adding an additional 100 ps of derating to accommodate for the lower alternate threshold of 150 mV and another 25 ps to account for the earlier reference point [(175 mv - 150 mV) / 1 V/ns].

NOTE 28. Pulse width of a input signal is defined as the width between the first crossing of Vref(dc) and the consecutive crossing of Vref(dc).

NOTE 29. tDQSL describes the instantaneous differential input low pulse width on DQS - DQS#, as measured from one falling edge to the next consecutive rising edge.

NOTE 30. tDQSH describes the instantaneous differential input high pulse width on DQS - DQS#, as measured from one rising edge to the next consecutive falling edge.

NOTE 31. tDQSH,act + tDQSL,act = 1 tCK,act ; with tXYZ,act being the actual measured value of the respective timing parameter in the application.

NOTE 32. tDSH,act + tDSS,act = 1 tCK,act ; with tXYZ,act being the actual measured value of the respective timing parameter in the application.

13.3 Address / Command Setup, Hold and Derating

For all input signals the total tIS (setup time) and tIH (hold time) required is calculated by adding the data sheet tIS(base) and tIH(base) value (see Table 66) to the ΔtIS and ΔtIH derating value (see Table 67) respectively. Example: tIS (total setup time) = tIS(base) + ΔtIS

Setup (tIS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of $V_{IH(ac)}$min. Setup (tIS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of Vil(ac)max. If the actual signal is always earlier than the nominal slew rate line between shaded '$V_{REF(dc)}$ to ac region', use nominal slew rate for derating value (see Figure Figure 110). If the actual signal is later than the nominal slew rate line anywhere between shaded '$V_{REF(dc)}$ to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value (see Figure 112).

Hold (tIH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of Vil(dc)max and the first crossing of $V_{REF(dc)}$. Hold (tIH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of Vih(dc)min and the first crossing of $V_{REF(dc)}$. If the actual signal is always later than the nominal slew rate line between shaded 'dc to $V_{REF(dc)}$ region', use nominal slew rate for derating value (see Figure 111). If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to $V_{REF(dc)}$ region', the slew rate of a tangent line to the actual signal from the dc level to $V_{REF(dc)}$ level is used for derating value (see Figure 113).

For a valid transition the input signal has to remain above/below $V_{IH/IL(ac)}$ for some time t_{VAC} (see Table 69).

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached $V_{IH/IL(ac)}$ at the time of the rising clock transition, a valid input signal is still required to complete the transition and reach $V_{IH/IL(ac)}$.

For slew rates in between the values listed in Table 67, the derating values may obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization.

Table 66 — ADD/CMD Setup and Hold Base-Values for 1V/ns

Unit [ps]	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	Reference
tIS(base)	200	125	65	45	$V_{IH/L(ac)}$
tIH(base)	275	200	140	120	$V_{IH/L(dc)}$
tIS(base) AC150	200 + 150	125 + 150	65 + 125	45 + 125	$V_{IH/L(dc)}$

NOTE 1. (ac/dc referenced for 1V/ns Address/Command slew rate and 2 V/ns differential CK-CK# slew rate)

NOTE 2. The tIS(base) AC150 specifications are adjusted from the tIS(base) specification by adding an additional 125 ps for DDR3-800/1066 or 100ps for DDR3-1333/1600 of derating to accommodate for the lower alternate threshold of 150 mV and another 25 ps to account for the earlier reference point [(175 mv - 150 mV) / 1 V/ns].

13 Electrical Characteristics and AC Timing (Cont'd)
13.3 Address / Command Setup, Hold and Derating (Cont'd)

Table 67 — Derating values DDR3-800/1066/1333/1600 tIS/tIH - ac/dc based

ΔtIS, ΔtIH derating in [ps] AC/DC based AC175 Threshold -> VIH(ac)=VREF(dc)+175mV, VIL(ac)=VREF(dc)-175mV																	
		CK,CK# Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD/ ADD Slew rate V/ns	2.0	88	50	88	50	88	50	96	58	104	66	112	74	120	84	128	100
	1.5	59	34	59	34	59	34	67	42	75	50	83	58	91	68	99	84
	1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	-2	-4	-2	-4	-2	-4	6	4	14	12	22	20	30	30	38	46
	0.8	-6	-10	-6	-10	-6	-10	2	-2	10	6	18	14	26	24	34	40
	0.7	-11	-16	-11	-16	-11	-16	-3	-8	5	0	13	8	21	18	29	34
	0.6	-17	-26	-17	-26	-17	-26	-9	-18	-1	-10	7	-2	15	8	23	24
	0.5	-35	-40	-35	-40	-35	-40	-27	-32	-19	-24	-11	-16	-2	-6	5	10
	0.4	-62	-60	-62	-60	-62	-60	-54	-52	-46	-44	-38	-36	-30	-26	-22	-10

Table 68 — Derating values DDR3-800/1066/1333/1600 tIS/tIH - ac/dc based - Alternate AC150 Threshold

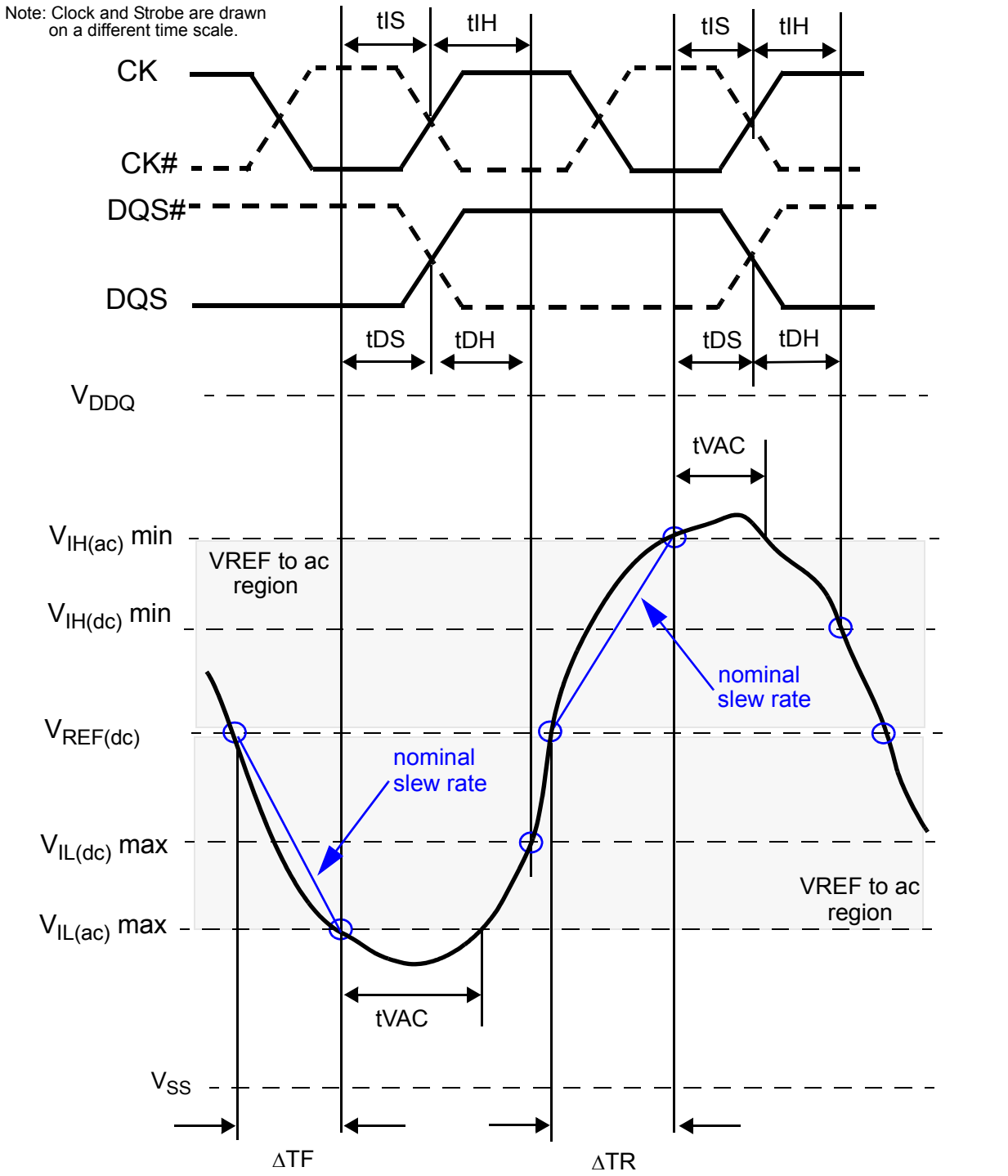
ΔtIS, ΔtIH derating in [ps] AC/DC based Alternate AC150 Threshold -> VIH(ac)=VREF(dc)+150mV, VIL(ac)=VREF(dc)-150mV																	
		CK,CK# Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD/ ADD Slew rate V/ns	2.0	75	50	75	50	75	50	83	58	91	66	99	74	107	84	115	100
	1.5	50	34	50	34	50	34	58	42	66	50	74	58	82	68	90	84
	1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	0	-4	0	-4	0	-4	8	4	16	12	24	20	32	30	40	46
	0.8	0	-10	0	-10	0	-10	8	-2	16	6	24	14	32	24	40	40
	0.7	0	-16	0	-16	0	-16	8	-8	16	0	24	8	32	18	40	34
	0.6	-1	-26	-1	-26	-1	-26	7	-18	15	-10	23	-2	31	8	39	24
	0.5	-10	-40	-10	-40	-10	-40	-2	-32	6	-24	14	-16	22	-6	30	10
	0.4	-25	-60	-25	-60	-25	-60	-17	-52	-9	-44	-1	-36	7	-26	15	-10

13 Electrical Characteristics and AC Timing (Cont'd)
13.3 Address / Command Setup, Hold and Derating (Cont'd)

Table 69 — Required time t_{VAC} above VIH(ac) {below VIL(ac)} for valid transition

Slew Rate [V/ns]	t_{VAC} @ 175mV [ps]		t_{VAC} @ 150mV [ps]	
	min	max	min	max
> 2.0	75	-	175	-
2.0	57	-	170	-
1.5	50	-	167	-
1.0	38	-	163	-
0.9	34	-	162	-
0.8	29	-	161	-
0.7	22	-	159	-
0.6	13	-	155	-
0.5	0	-	150	-
< 0.5	0	-	150	-

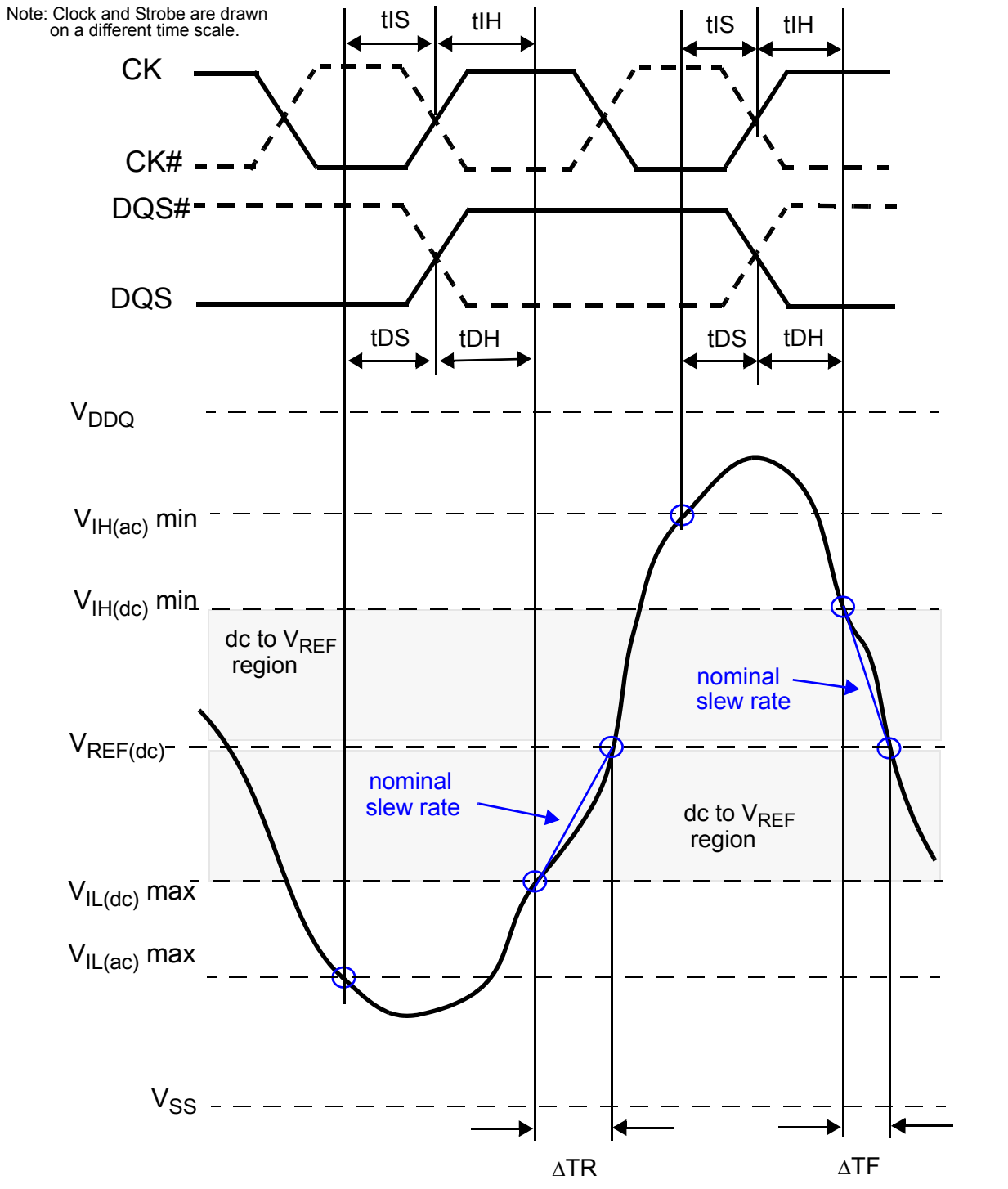
13 Electrical Characteristics and AC Timing (Cont'd)
13.3 Address / Command Setup, Hold and Derating (Cont'd)



$$\text{Setup Slew Rate}_{\text{Falling Signal}} = \frac{V_{REF(dc)} - V_{IL(ac)}max}{\Delta TF} \qquad \text{Setup Slew Rate}_{\text{Rising Signal}} = \frac{V_{IH(ac)}min - V_{REF(dc)}}{\Delta TR}$$

Figure 110 — Illustration of nominal slew rate and t_{VAC} for setup time t_{DS} (for DQ with respect to strobe) and t_{IS} (for ADD/CMD with respect to clock).

13 Electrical Characteristics and AC Timing (Cont'd)
13.3 Address / Command Setup, Hold and Derating (Cont'd)



$$\text{Hold Slew Rate Rising Signal} = \frac{V_{REF(dc)} - V_{IL(dc)}max}{\Delta TR} \qquad \text{Hold Slew Rate Falling Signal} = \frac{V_{IH(dc)}min - V_{REF(dc)}}{\Delta TF}$$

Figure 111 — Illustration of nominal slew rate for hold time t_{DH} (for DQ with respect to strobe) and t_{IH} (for ADD/CMD with respect to clock).

13 Electrical Characteristics and AC Timing (Cont'd)
13.3 Address / Command Setup, Hold and Derating (Cont'd)

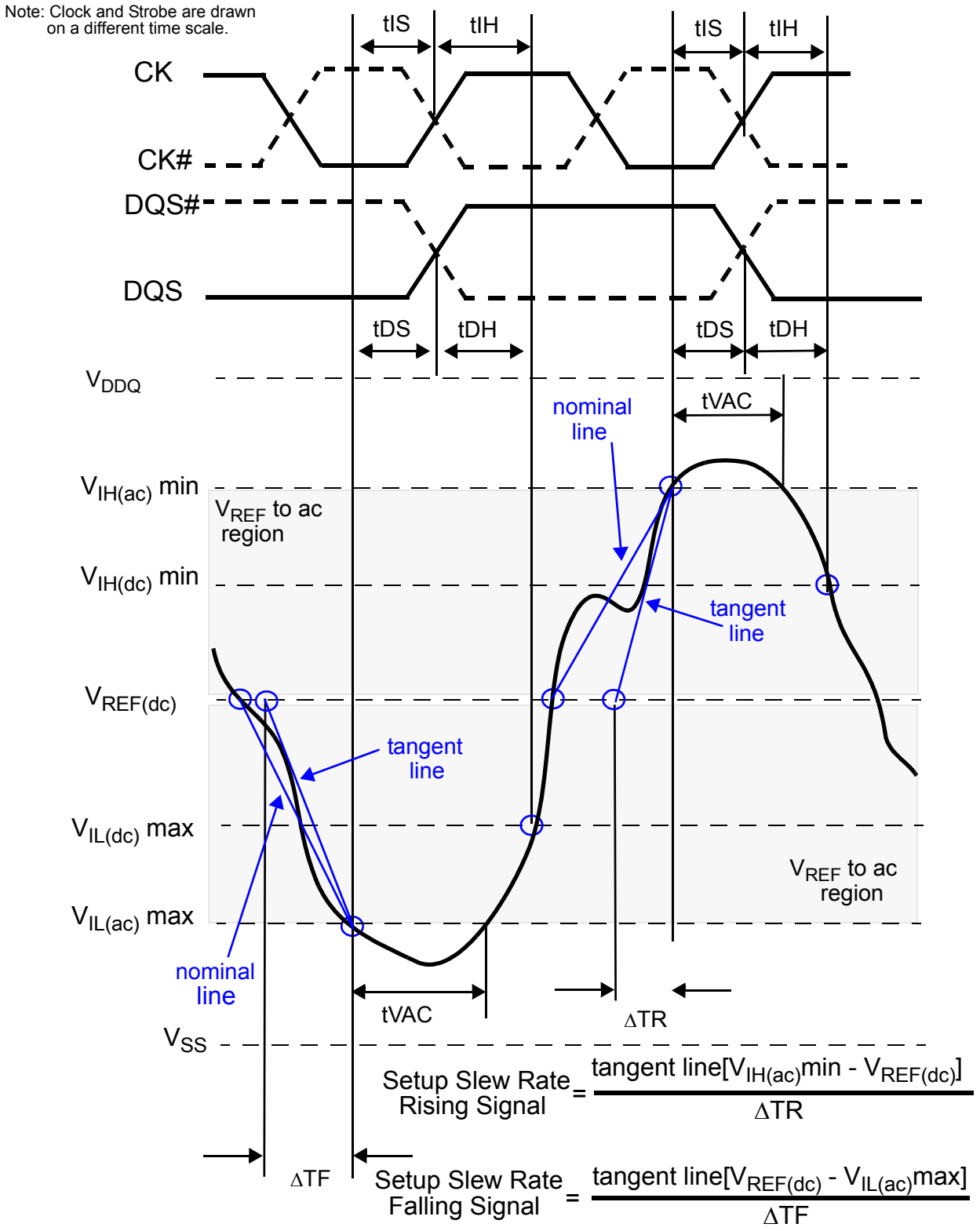


Figure 112 — Illustration of tangent line for setup time t_{DS} (for DQ with respect to strobe) and t_{IS} (for ADD/CMD with respect to clock)

13 Electrical Characteristics and AC Timing (Cont'd)
13.3 Address / Command Setup, Hold and Derating (Cont'd)

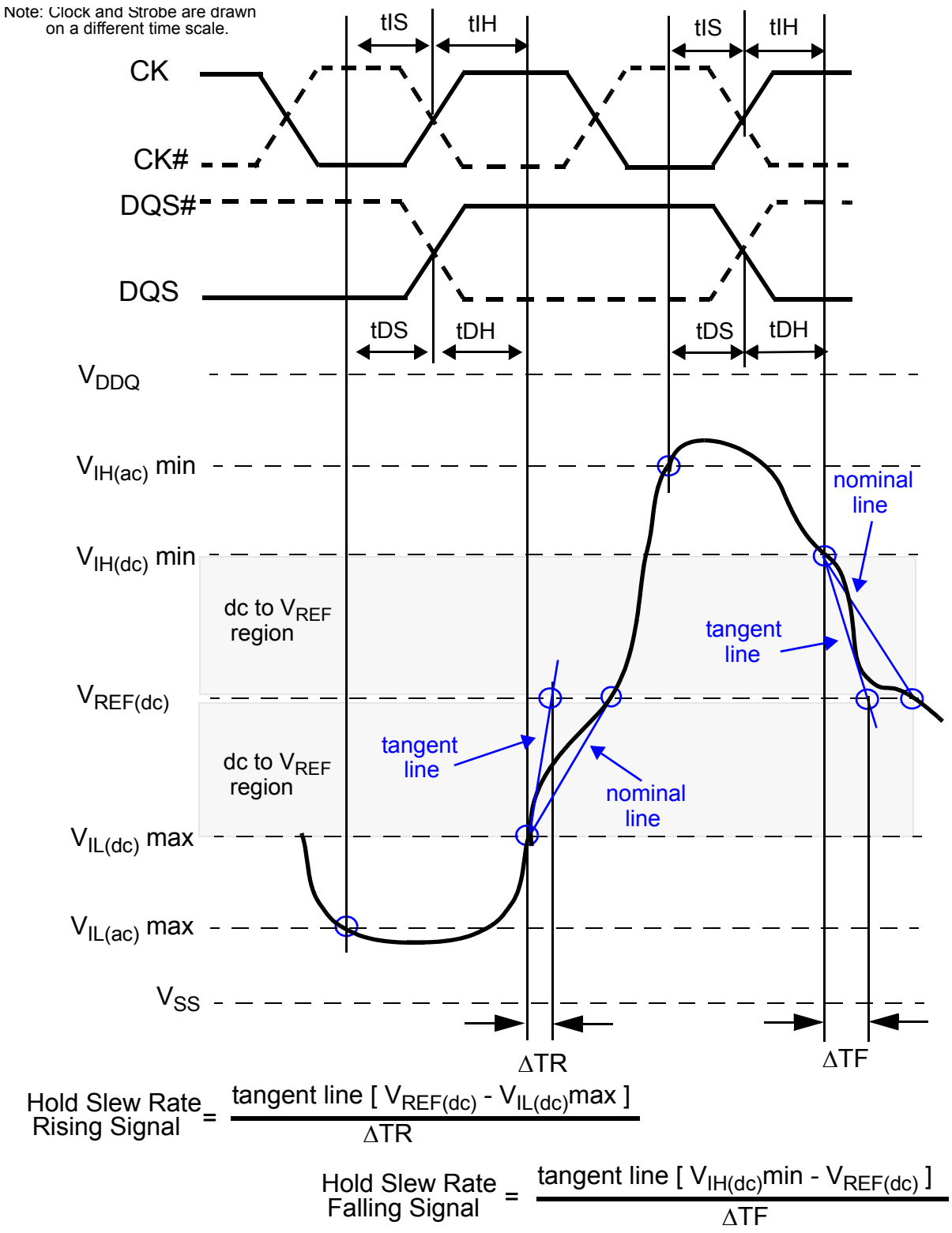


Figure 113 — Illustration of tangent line for for hold time t_{DH} (for DQ with respect to strobe) and t_{IH} (for ADD/CMD with respect to clock)

13.4 Data Setup, Hold and Slew Rate Derating

For all input signals the total tDS (setup time) and tDH (hold time) required is calculated by adding the data sheet tDS(base) and tDH(base) value (see Table 70) to the ΔtDS and ΔtDH (see Table 71) derating value respectively. Example: tDS (total setup time) = tDS(base) + ΔtDS.

Setup (tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of $V_{IH(ac)}$min. Setup (tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of $V_{IL(ac)}$max (see Figure 114). If the actual signal is always earlier than the nominal slew rate line between shaded '$V_{REF(dc)}$ to ac region', use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded '$V_{REF(dc)}$ to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value (see Figure 116).

Hold (tDH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(dc)}$max and the first crossing of $V_{REF(dc)}$. Hold (tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(dc)}$min and the first crossing of $V_{REF(dc)}$ (see Figure 115). If the actual signal is always later than the nominal slew rate line between shaded 'dc level to $V_{REF(dc)}$ region', use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to $V_{REF(dc)}$ region', the slew rate of a tangent line to the actual signal from the dc level to $V_{REF(dc)}$ level is used for derating value (see Figure 117).

For a valid transition the input signal has to remain above/below $V_{IH/IL(ac)}$ for some time t_{VAC} (see Table 73).

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached $V_{IH/IL(ac)}$ at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach $V_{IH/IL(ac)}$.

For slew rates in between the values listed in the tables the derating values may obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization.

Table 70 — Data Setup and Hold Base-Values

Units [ps]	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	Reference
tDS(base)	75	25	30	10	$V_{IH/L(ac)}$
tDH(base)	150	100	65	45	$V_{IH/L(dc)}$

NOTE: (ac/dc referenced for 1V/ns DQ-slew rate and 2 V/ns DQS slew rate)

13 Electrical Characteristics and AC Timing (Cont'd)
13.4 Data Setup, Hold and Slew Rate Derating (Cont'd)

Table 71 — Derating values DDR3-800/1066 tDS/tDH - ac/dc based

ΔtDS, ΔDH derating in [ps] AC/DC based[1]																
		DQS, DQS# Differential Slew Rate														
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew rate V/ns	2.0	88	50	88	50	88	50	-	-	-	-	-	-	-	-	-	-
	1.5	59	34	59	34	59	34	67	42	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	8	8	16	16	-	-	-	-	-	-
	0.9	-	-	-2	-4	-2	-4	6	4	14	12	22	20	-	-	-	-
	0.8	-	-	-	-	-6	-10	2	-2	10	6	18	14	26	24	-	-
	0.7	-	-	-	-	-	-	-3	-8	5	0	13	8	21	18	29	34
	0.6	-	-	-	-	-	-	-	-	-1	-10	7	-2	15	8	23	24
	0.5	-	-	-	-	-	-	-	-	-	-	-11	-16	-2	-6	5	10
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-30	-26	-22	-10

NOTE 1. Cell contents shaded in red are defined as 'not supported'.

Table 72 — Derating values for DDR3-1333/1600 tDS/tDH - ac/dc based

ΔtDS, ΔDH derating in [ps] AC/DC based[1]																
		DQS, DQS# Differential Slew Rate														
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew rate V/ns	2.0	75	50	75	50	75	50	-	-	-	-	-	-	-	-	-	-
	1.5	50	34	50	34	50	34	58	42	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	8	8	16	16	-	-	-	-	-	-
	0.9	-	-	0	-4	0	-4	8	4	16	12	24	20	-	-	-	-
	0.8	-	-	-	-	0	-10	8	-2	16	6	24	14	32	24	-	-
	0.7	-	-	-	-	-	-	8	-8	16	0	24	8	32	18	40	34
	0.6	-	-	-	-	-	-	-	-	15	-10	23	-2	31	8	39	24
	0.5	-	-	-	-	-	-	-	-	-	-	14	-16	22	-6	30	10
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	7	-26	15	-10

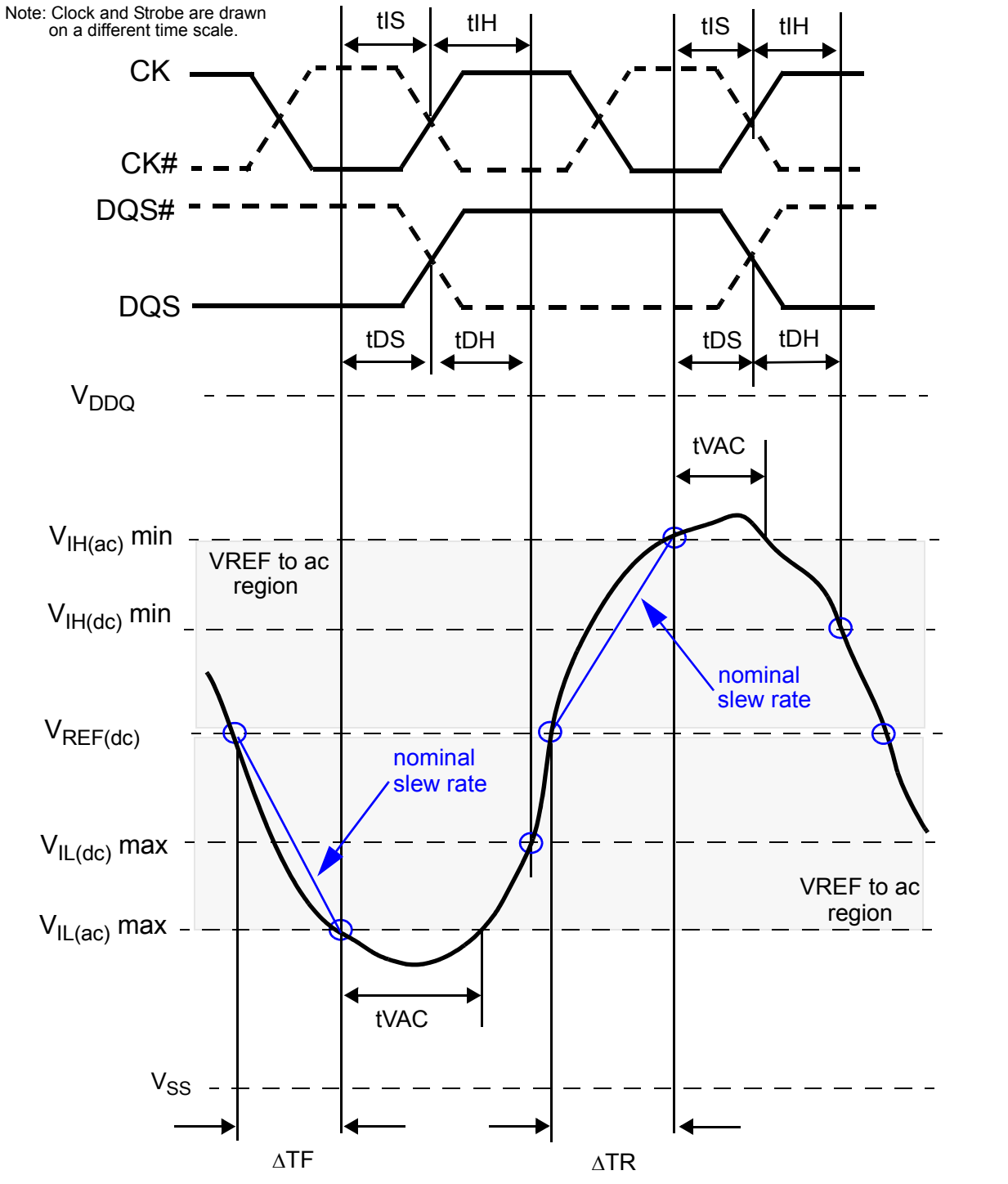
NOTE 1. Cell contents shaded in red are defined as 'not supported'.

13 Electrical Characteristics and AC Timing (Cont'd)
13.4 Data Setup, Hold and Slew Rate Derating (Cont'd)

Table 73 — Required time t_{VAC} above VIH(ac) {below VIL(ac)} for valid transition

Slew Rate [V/ns]	DDR3-800/1066		DDR3-1333/1600	
Slew Rate [V/ns]	t_{VAC} [ps]		t_{VAC} [ps]	
	min	max	min	max
> 2.0	75	-	175	-
2.0	57	-	170	-
1.5	50	-	167	-
1.0	38	-	163	-
0.9	34	-	162	-
0.8	29	-	161	-
0.7	22	-	159	-
0.6	13	-	155	-
0.5	0	-	155	-
< 0.5	0	-	150	-

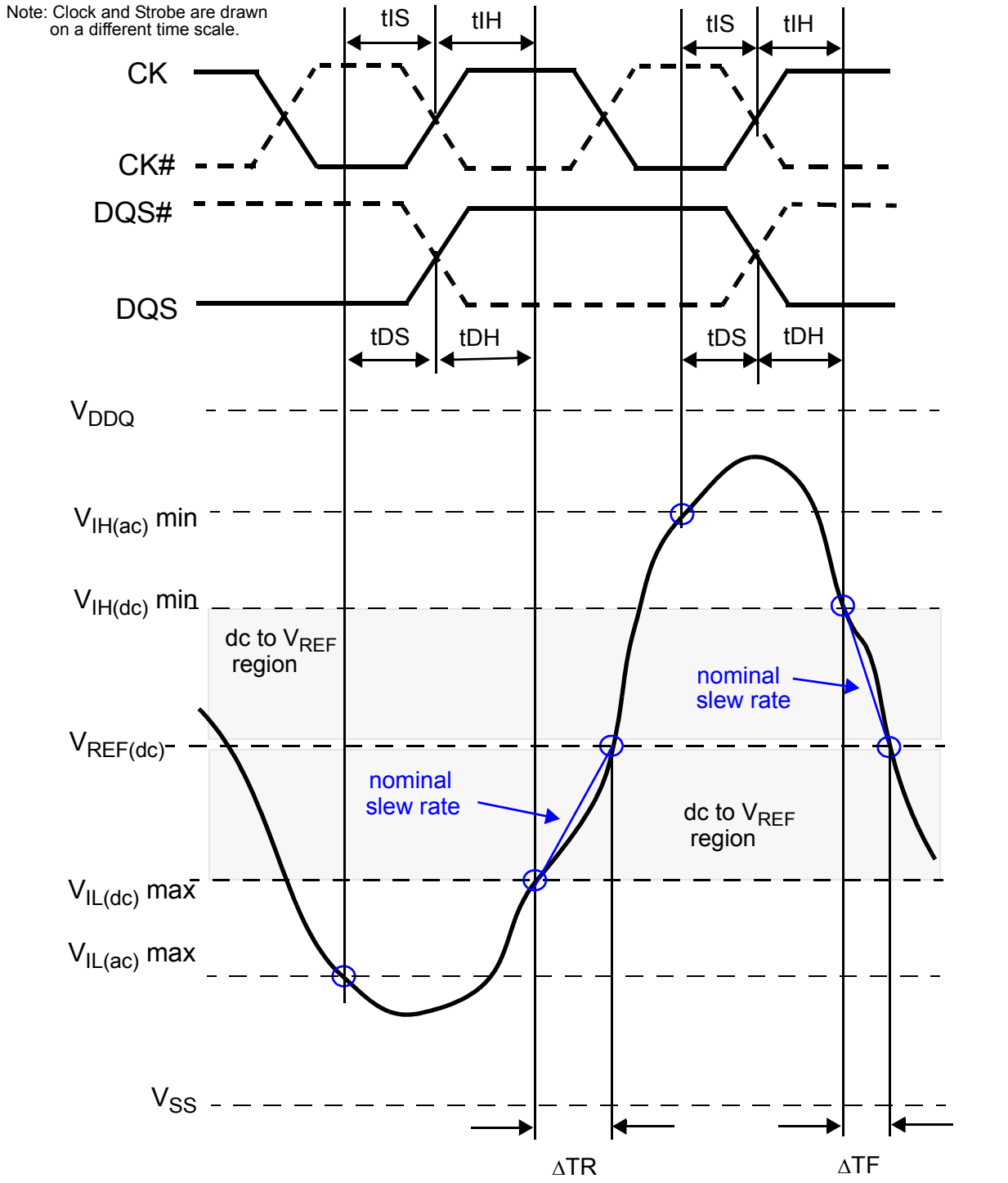
13 Electrical Characteristics and AC Timing (Cont'd)
13.4 Data Setup, Hold and Slew Rate Derating (Cont'd)



$$\text{Setup Slew Rate Falling Signal} = \frac{V_{REF(dc)} - V_{IL(ac)}\text{max}}{\Delta TF} \qquad \text{Setup Slew Rate Rising Signal} = \frac{V_{IH(ac)}\text{min} - V_{REF(dc)}}{\Delta TR}$$

Figure 114 — Illustration of nominal slew rate and t_{VAC} for setup time t_{DS} (for DQ with respect to strobe) and t_{IS} (for ADD/CMD with respect to clock).

13 Electrical Characteristics and AC Timing (Cont'd)
13.4 Data Setup, Hold and Slew Rate Derating (Cont'd)



$$\text{Hold Slew Rate Rising Signal} = \frac{V_{REF(dc)} - V_{IL(dc)}max}{\Delta TR} \qquad \text{Hold Slew Rate Falling Signal} = \frac{V_{IH(dc)}min - V_{REF(dc)}}{\Delta TF}$$

Figure 115 — Illustration of nominal slew rate for hold time t_{DH} (for DQ with respect to strobe) and t_{IH} (for ADD/CMD with respect to clock).

13 Electrical Characteristics and AC Timing (Cont'd)
13.4 Data Setup, Hold and Slew Rate Derating (Cont'd)

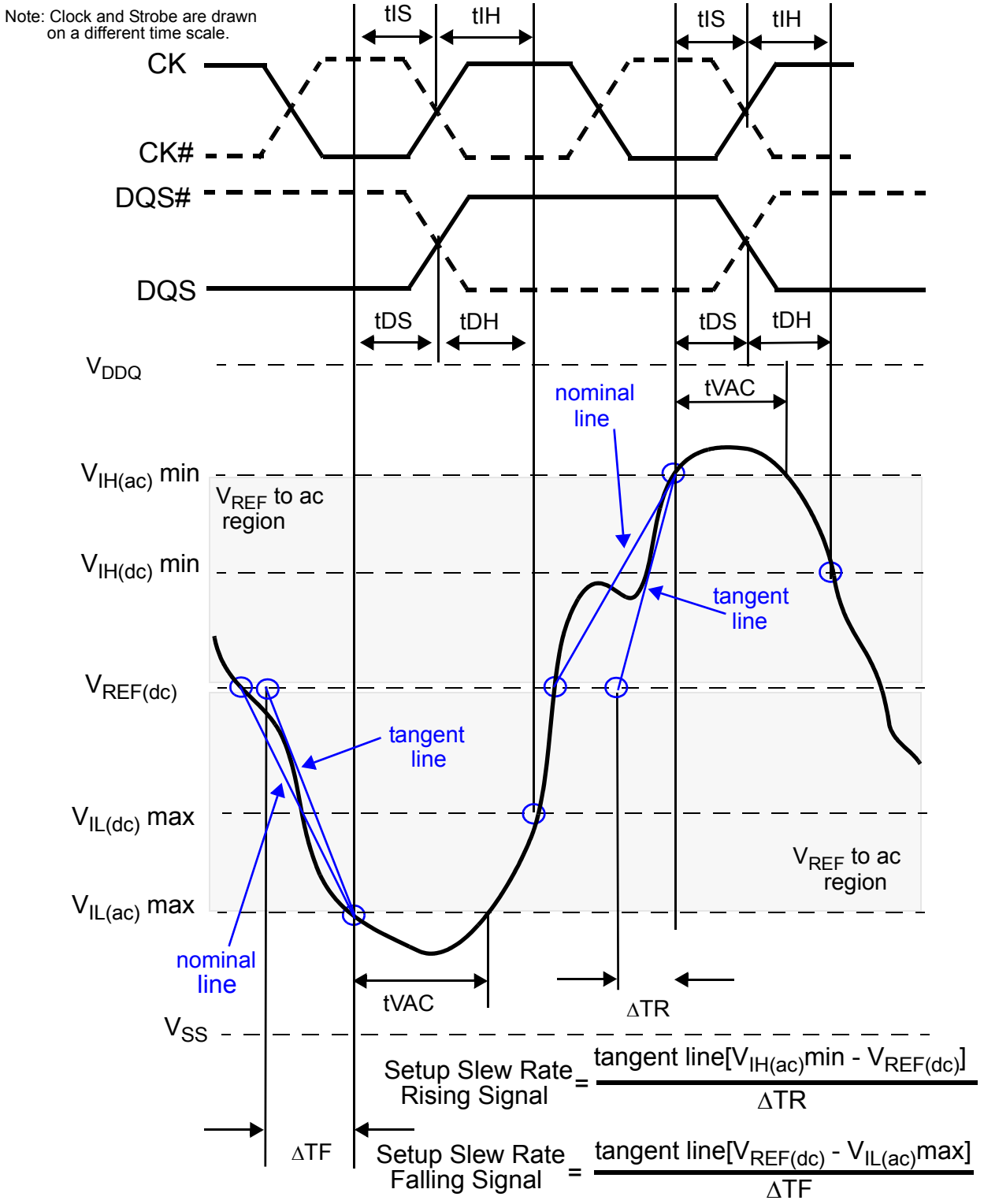


Figure 116 — Illustration of tangent line for setup time t_{DS} (for DQ with respect to strobe) and t_{IS} (for ADD/CMD with respect to clock)

13 Electrical Characteristics and AC Timing (Cont'd)
13.4 Data Setup, Hold and Slew Rate Derating (Cont'd)

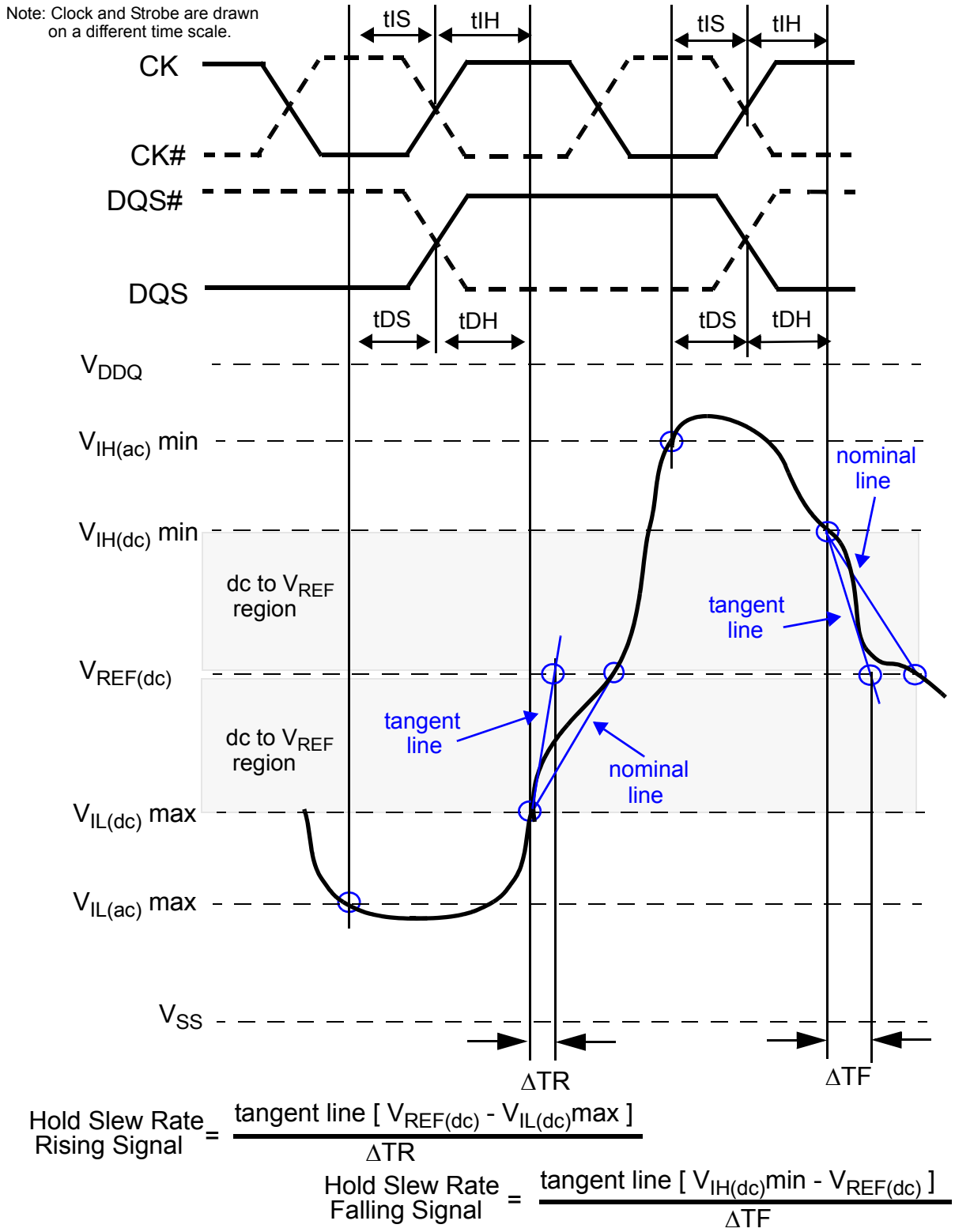


Figure 117 — Illustration of tangent line for for hold time t_{DH} (for DQ with respect to strobe) and t_{IH} (for ADD/CMD with respect to clock).

Annex A (informative) Differences between JESD79-3C, and JESD79-3B.

This table briefly describes most of the changes made to this standard, JESD79-3C, compared to its predecessor, JESD79-3B. Some editorial changes are not included.

Page	Description of Change
22	Updated Figure 7, tMRD Timing Updated Figure 8, tMOD Timing
26	Updated Figure 10, MR1 Definition
33	Updated Table 6, Command Truth Table
63	Updated Figure 35, READ (BL8) to WRITE (BL8) Updated Figure 36, READ (BC4) to WRITE (BC4) OTF
65	Updated Figure 39, READ (BL4) to WRITE (BL8) OTF Updated Figure 40, READ (BL8) to WRITE (BC4) OTF
66	Updated Section 4.13.3, Burst REad Operation followed by a Precharge Added Figure 41, READ to Precharge, RL=5, AL=0, CL=5, tRTP=4, tRP=5 Renumbered subsequent figures.
67	Added Figure 42, READ to Precharge, RL=8, AL=CL-2, CL=5, tRTP=6, tRP=5 Renumbered subsequent figures.
72	Updated Figure 48, WRITE (BC4) to READ (BC4) Operation Updated Figure 49, WRITE (BC4) to PRECHARGE Operation Added Figure 50, WRITE (BC4) OTF to PRECHARGE Operation Renumbered subsequent figures.
73	Updated Figure 51, WRITE (BL8) to WRITE (BL8) Operation Updated Figure 52, WRITE (BC4) to WRITE (BC4) OTF
74	Updated Figure 53, WRITE (BL8) to READ (BC4/BL8) OTF Updated Figure 54, WRITE (BC4) to WRITE (BC4) OTF
75	Added Figure 55, WRITE (BC4) to READ (BC4) Renumbered subsequent figures Updated Figure 56, WRITE (BL8) to WRITE (BC4) OTF
76	Updated Figure 57, WRITE (BC4) to WRITE (BL8) OTF
77	Updated Section 4.15, Refresh Command
79	Updated Section 4.16, Self Refresh Operation
102	Updated Table 19, Asynchronous ODT Timing Paramaters for all Speed Bins
113	Updated Table 24, Single-Ended AC and DC Input Levels for Command and Address
128	Updated Table 39, Output Driver DC Electrical Characteristics
129	Updated Table 41, Output Driver Voltage and Temperature Sensitivity
39	Updated Section 10, IDD and IDDQ Specification Parameters and Test Conditions
140	Removed Figures 104, IDD1 Example Removed Figures 105, IDD2N/IDD3N Example Removed Figures 106, IDD4 Example Added Figure 108, Measurement Setup and Test Load for IDD and IDDQ (option) Measurements Added Figure 109, Correlation from Simulated Channel IO Power to Actual Channel IO Power suppored by IDDQ Measurements

Annex A (informative) Differences between JESD79-3C, and JESD79-3B.

This table briefly describes most of the changes made to this standard, JESD79-3C, compared to its predecessor, JESD79-3B. Some editorial changes are not included.

Page	Description of Change
141	Updated Table 47, Timings used for IDD and IDDQ Measurement-Loop Patterns Updated Table 48, Basic IDD and IDDQ Measurement Conditions
144	Updated Table 49, IDD0 Measurement-Loop Pattern
145	Updated Table 50, IDD1 Measurement-Loop Pattern
146	Updated Table 51, IDD2N and IDD3N Measurement-Loop Pattern Updated Table 52, IDD2NT and IDDQ2NT Measurement-Loop Pattern
147	Updated Table 53, IDD4R and IDDQ4R Measurement-Loop Pattern Updated Table 54, IDD4W Measurement-Loop Pattern
148	Updated Table 55, IDD5B Measurement-Loop Pattern
149	Updated Table 56, IDD7 Measurement-Loop Pattern
150	Updated Table 57 IDD Specification Example 512M DDR3
153	Updated Table 59, Input/Output Capacitance
163-169	Updated Table 65, Timing Paramaters by Speed Bin
173	Updated Table 66, ADD/CMD Setup and Hold Base-Values for 1V/ns
174	Updated Table 68, Derating Values DDR3-800/1066/1333/1600 tIS/tIH ac/dc based - Alternate AC150 Threshold

Annex A.1 (informative) Differences between JESD79-3B, and JESD79-3A.

This table briefly describes most of the changes made to this standard, JESD79-3B, compared to its predecessor, JESD79-3A. Some editorial changes and format-updates of figures are not included.

Page	Description of Change
3-8	Updated ballout diagrams
9-11	Added ballouts for Quad-Stacked/Quadl-die DDR3 SDRAM in x4, x8, x16 ballout. Renumbered subsequent figures.
13	Updated Table 1, Input/Output Functional Description
17	Updated Figure 4, Simplified State Diagram
29	Updated Figure 11, MR2 Definition
44	Updated Figure 18, Timing Details of Write Leveling Sequence
45	Updated Figure 19, Timing Details of Write Leveling Exit
58	Updated Figure 28, Clock to Data Strobe Relationship
60	Updated Figure 30, tLZ and tHZ Method for Calculating Transitions and Endpoints
66	Updated Section 4.14.2.3; Strobe to Strobe and Strobe to Clock Violations
67	Added Section 4.14.3, Write Data Mask Updated Figure-41, Write Timing Definition and Parameters
74	Added Section 4.15, Refresh Command. Subsequent sections renumbered accordingly.
83	Updated Figure 67, MRS Command to Power Down Entry
89	Updated Figure 72, Sync ODT Timing Example.
99	Updated second paragraph in Section 5.4.2, Sync to Async ODT Mode Transition During Power-Down Entry
100	Updated Figure 81, Sync to async transition during Precharge Power Down (with DLL frozen)
101	updated Figures 82, Sync to async transition after Refresh command
111	Split Table 24 into two tables: Table 24, Single-Ended AC and DC Input Levels for Command and Address Table 25, Single-ended AC and DC Input Levels for DQ and DM
112	Added Section, 8.2, Vref Tolerances
113	Updated Figure 87, Definition of differential ac-swing and “time above ac-level”.
115	Updated Table 28, Single-ended levels for CK, DQS, DQSL, DQSU, CK#, DQS#, DQS#, DQSL# or DQSU#
116	Updated Table 29, Cross point voltage for differential input signals (CD, DQS).
117	Replaced Table 29, Single-Ended INput Slew Rate Definition Figure 83, Input NOminal Slew RAte Definition for Singe-Ended Signals Section 8.4.1, Input Slew Rate for Input Setup Time and Data Setup Time Section 8.4.2 Input Slew Rate for Input Hold Time and Data Hold Time with reference to existing definitions of single-ended signals in Sections 13.3 and 13.4.
117	Updated Table 30, Differential Input Slew Rate Definition
139	Added summary Table 51, IDD Measurement Conditions, to replace existing Tables 51-54,56-57
147	Updated Table 55, Input/Output Capacitance
153	Updated Table 59, DDR3-1333 Speed Bins and Operating Conditions.
154	Updated Table 60, DDR3-1333 Speed Bins and Operating Conditions.

Annex A.1 (informative) Differences between JESD79-3B, and JESD79-3A.

This table briefly describes most of the changes made to this standard, JESD79-3B, compared to its predecessor, JESD79-3A. Some editorial changes and format-updates of figures are not included.

Page	Description of Change
157	Updated Table 61, Timing Parameters by Speed Bin
164	Updated and reordered Specific Notes a - g
165	Updated notes 11 and 19 for read tRPRE and tRPST and added reference to Fig-28.
A-1	Added Annex A (Informative) Differences between JESD79-3B and JESD79-3A.

Annex A.2 (informative) Differences between JESD79-3A, and JESD79-3.

This table briefly describes most of the changes made to this standard, JESD79-3A, compared to its predecessor, JESD79-3. Some editorial changes and format-updates of figures are not included.

Page	Description of Change
13	Per JCB-07-070, DDR3 Specification Updated Figure 1 – Simplified State Diagram Updated Table 2 – State Diagram Command Definitions
54	Per JCB-07-070, DDR3 Specification Updated Section 4.13.2.1 – READ Timing; Clock to Data Strobe relationship
55	Per JCB-07-070, DDR3 Specification Updated Section 4.13.2.2 – READ Timing; Data Strobe to Data Strobe relationship
57	Per JCB-07-070, DDR3 Specification Added Figure 28 – Method for calculationg tRPRE transitions and endpoints
63	Per JCB-07-070, DDR3 Specification Removed Figure 40 – Write Timing Parameters Moved Figure 45, renamed as Write Timing Definition and Parameters, to page 63, as Figure 38
64	Per JCB-07-034, tWPRE, tWPST Added Section 4.14.3 – tWPRE Calculation Added Section 4.14.4 – tWPST Calculation
72-79	Per JCB-07-070, DDR3 Specification Reorganized subsections 4.16.1 and 4.16.2, moving Figures 52-61 into 4.16.1 and making one subsection each (4.16.2, 3, and 4) for the power-down entry/exit clarification cases (1-3).
75	Per JCB-07-070, DDR3 Specification Removed Figure 57 – Active Power-Down Entry and Exit Timing Diagram
79	Per JCB-07-070, DDR3 Specification Removed Table 15 – Timing Values tXXXPDEN Parameters
84	Per JCB-07-036, ODT Read Timing Updated Figure 68 – OCT must be disabled...during Reads...
86	Per JCB-07-036, ODT Read Timing Updated Section 5.2.3 – ODT During READs
96, 97	Per JCB-07-067, ZQ Input Capacitance Updated Section 5.5.1 – ZQ Calibration Description Replaced Section 5.5.3. Is now: ZQ External Resistor Value, Tolerance, and Capacitance Loading
97	Per JCB-07-070, DDR3 Specification Removed Table 22 – ZQ Calibration Command Truth Table
101	Per JCB-07-065, Vih(dc)max, Vil(dc)min Updated Table 24 – Single Ended AC and DC Input Levels
103-106	Per JCB-07-068, Differention Signal Input Specification Added Section 8.2 – AC and CD Logic Input Levels for Differential Signals
128	Per JCB-07-070, DDR3 Specification Updated Table 50 – For IDD testing the followign parameters are utilized

Annex A.2 (informative) Differences between JESD79-3A, and JESD79-3.

This table briefly describes most of the changes made to this standard, JESD79-3A, compared to its predecessor, JESD79-3. Some editorial changes and format-updates of figures are not included.

Page	Description of Change
141	Per JCB-07-038, Capacitance Updated Table 61 – Input/Output Capacitance
141	Per JCB-07-067, ZQ Input Capacitance Updated Table 61 – Input/Output Capacitance
142, 143	Per JCB-07-070, DDR3 Specification Removed unnumbered tables from subsection 12.1. Moved subsection 12.2 material into 12.1. Renumbered subsequent subsections.
149	Per JCB-07-041, tJIT (duty) note modification Updated Table 67 – Timing Parameters by Speed Bin
149, 150	Per JCB-07-032, Cumulative Jitter Updated Table 67 – Timing Parameters by Speed Bin
150	Per JCB-07-034, tWPRE, tWPST Updated Table 67 – Timing Parameters by Speed Bin
150	Per JCB-07-040, Jitter Values for DDR3-1600 Updated Table 67 – Timing Parameters by Speed Bin
150	Per JCB-07-029, Jitter Output Derating Updated Table 67 – Timing Parameters by Speed Bin
150	Per JCB-07-031, tDQSCK tQH Updated Table 67 – Timing Parameters by Speed Bin
150	Per JCB-07-066, tQSH, tQSL values Updated Table 67 – Timing Parameters by Speed Bin
152	Per JCB-07-042, tIS, tIH, DDR3-1333 Updated Table 67 – Timing Parameters by Speed Bin
154	Per JCB-07-035, tWLS, tWLH Updated Table 67 – Timing Parameters by Speed Bin
156-158	Per JCB-07-033, tCH (abs) and tCL (abs) Removed Specific Note F from Table 67 – Timing Parameters by Speed Bin. This action included remvoing the Table – Min and Max SPEC values. Removed Note 22 from Table 67 – Timing Parameters by Speed Bin Added Notes 25 and 26 to Table 67 – Timing Parameters by Speed Bin
157	Per JCB-07-039, tZQCS Added Note 23
157, 158	Per JCB-07-039, tZQCS Updated Note 23 of Table 67 – Timing Parameters by Speed Bin
158	Per JCB-07-042, tIS, tIH, DDR3-1333 Added Note 27
159	Per JCB-07-027 Updated Table 68 – ADD/CMD Setup and Hold Base-Values for 1V/ns

Annex A.2 (informative) Differences between JESD79-3A, and JESD79-3.

This table briefly describes most of the changes made to this standard, JESD79-3A, compared to its predecessor, JESD79-3. Some editorial changes and format-updates of figures are not included.

Page	Description of Change
160	Per JCB-07-027 Updated Table 69 – Derating values DDR3-800/1066/1333/1600 tIS/tIH - ac/dc based Added Table 70 – Derating values DDR3-1333/1600 tIS/tIH - ac/dc based - Alternate AC150 Threshold
161	Per JCB-07-027 Updated Table 71 – Required time T_{VAC} above VIH(ac) [below VIL(ac)] for valid transition
166	Per JCB-07-037, tDS, tDH 1333 Updated Table 72 – Data Setup and Hold Base-Values
A-1	Added Annex A (Informative) Differences between JESD79-3A and JESD79-3.

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Exhibit B

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[Document type-|- Committees-|-Keywords-|-Revision Status]

Document Type

NUMBER	JEDEC Engineering Bulletins (JEB)	PRICE
JEB 5-A	METHODS OF MEASUREMENT FOR SEMICONDUCTOR LOGIC GATING MICROCIRCUITS: The purpose of this bulletin is to recommend for use in the rating of semiconductor logic gating microcircuits which use the binary states to represent and process logic information. Both static and dynamic measurements are covered. January 1970; Reaffirmed February 1984 /JEDEC Committee	$63.00
JEB 6	STANDARD MEASURMENTS OF THE ELECTRICAL CHARACTERISTICS OF SEMICONDUCTOR INTEGRATED CIRCUITS December 1966; Rescinded October 1984 / Committee!33JCJEDC	
JEB 15	TERMINOLOGY AND METHODS OF MEASUREMENT FOR BISTABLE SEMICONDUCTOR MICROCIRCUITS: This bulletin explains the terminology and methods of measurement for bistable semiconductor microcircuits. It is also intended to be used with the EIA Registration Data Format for semiconductor integrated bistable logic circuits. November 1969 /JC-40 Committee	$109.00
JEB 16	USER GUIDE FOR MICROCIRCUIT FAILURE ANALYSIS: This guide defines generalized procedures for the failure analysis of monolithic integrated microelectronic circuits. Although the generalized procedural steps may apply to all microelectronic circuits, additional analysis steps unique to thin/thick film hybrid devices are not covered. July 1970; Rescinded November 2004 September 2003 /JC-14 Committee	$41.00
JEB 17	USER GUIDELINES FOR QUALITY AND RELIABILITY ASSURANCE OF LSI COMPONENTS November 1970; Rescinded April 1987 April 1987	
JEB 19	RECOMMENDED CHARACTERIZATION OF MOS SHIFT REGISTERS: This recommendation applies to MOS Shift Registers. Definitions are given for P-channel registers but are applicable to all CMOS and N-channel with changes in power supply notation. November 1972 /JC-40 Committee	$40.00
JEB 20	ACCEPTED PRACTICES FOR MAKING MICROELECTRONIC DEVICE THERMAL CHARACTERISTICS TESTS January 1975; Rescinded November 1988 /JC-11 Committee	
NUMBER	**Tentative Standards (TENTSTD)**	**PRICE**
TENTSTD 11	HANDLING AND INSTALLATION OF POWER SEMICONDUCTORS IN DISC TYPE PACKAGES: Included in JESD282 and EIA397. July 1973; Rescinded June 1992 June 1992 /JC-22.2 Subcommittee	
TENTSTD 12	STANDARD FOR SELENIUM SURGE SUPPRESSORS: The suppresser furnished under this standard shall be a product that has been tested and meets the definitions and minimum requirements specified herein. November 1973 /JC-22.5 Subcommittee	$49.00
NUMBER	**JEDEC Specifications (JES)**	**PRICE**
JES 2	TRANSISTOR, GALLIUM ARSENIDE POWER FET, GENERIC SPECIFICATION: Establishes guideline requirements and quality assurance provisions for gallium arsenide power field-effect transistors (FETs, also know as MESFETs) designed for use in high-reliability space	

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	application such as spacecraft communications transmitters. Identifies the electrical parameters, wafer acceptance tests, screening tests, qualification tests, and lot acceptance tests pertinent to power GaAs FETs. Applicable to packaged and chip-carrier parts; portions may not be applicable to unpackaged and unmounted chips. July 1992 /JC-14.7 Subcommittee	$71.00

NUMBER	JEDEC Standards (JESD)	PRICE
JESD 1	**LEADLESS CHIP CARRIER PINOUTS STANDARDIZED FOR LINEARS:** This standard shows how to convert existing DIP pinouts for op-amps, comparators, and D/A converters, to chip carrier packages. April 1982 / Committee!33JC41	$41.00
JESD 15	**THERMAL MODELING OVERVIEW** This document and the associated series of documents are intended to promote the continued development of modeling methods, while providing a coherent framework for their use by defining a common vocabulary to discuss modeling, creating requirements for what information should be included in a thermal modeling report, and specifying modeling procedures, where appropriate, and validation methods. This document provides an overview of the methodology necessary for performing meaningful thermal simulations for packages containing semiconductor devices. The actual methodology components are contained in separate detailed documents. October 2008 March 2006 /JC-15.1 Subcommittee	$47.00
JESD 15-1	**COMPACT THERMAL MODEL OVERVIEW** This document should be used in conjunction with the master document, JESD15, and JESD15-2, and subsidiary documents as they become available. This document is intended to function as an overview to support the effective use of Compact Thermal Model (CTM) methodologies as specified in the companion methods documents. At present, there are two such documents; JESD15-3, and JESD15-4. October 2008 October 2006 /JC-15.1 Subcommittee	$51.00
JESD 15-4	**DELPHI COMPACT THERMAL MODEL GUIDELINE** This guideline specifies the definition and lists acceptable approaches for constructing a compact thermal model (CTM) based on the DELPHI methodology. The purpose of this document is twofold. First, it aims to provide clear guidance to those seeking to create DELPHI compact models of packages. Second, it aims to provide users with an understanding of the methodology by which they are created and validated, and the issues associated with their use. October 2008 March 2006 /JC-15 Committee	$62.00
JESD 2	**DIGITAL BIPOLAR LOGIC PINOUTS FOR CHIP CARRIERS:** This standard provides a chip carrier format for digital devices by defining pin functions and locations for 20, 38, 44, 52, and 68-terminal devices. December 1982 /JC-40.1 Subcommittee	$41.00
JESD 3-C	**STANDARD DATA TRANSFER FORMAT BETWEEN DATA PREPARATION SYSTEM AND PROGRAMMABLE LOGIC DEVICE PROGRAMMER:** This standard was developed to prevent the proliferation of data transfer formats that occurred with microprocessor development systems. The focus of the standard is on field programmable devices and their support tools. It is not intended for other types of semicustom logic devices or other types of fabrication or testing equipment. June 1994 / Committee!33JC421	$61.00
JESD 4	**DEFINITION OF EXTERNAL CLEARANCE AND CREEPAGE DISTANCES OF DISCRETE SEMICONDUCTOR PACKAGES FOR THYRISTORS AND RECTIFIER DIODES:** This standard defines reference distances between terminals of the device and the external package at specific voltages. November 1983; Reaffirmed January 1991, April 1999, April 2002 April 2002 /JC-22.2 Subcommittee	$38.00
JESD 5	**MEASUREMENT OF TEMPERATURE COEFFICIENT OF VOLTAGE REGULATOR DIODES:** This standard is designed to define voltage-temperature characteristic measurement techniques and a method of calculation. Although many methods could be defined, this method provides a desired uniformity and lends itself to production testing. Formerly JEDEC Suggested Standard No. 5A	

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February 1982; Reaffirmed April 1999, April 2002 April 2002 /JC-22.4 Subcommittee $38.00

JESD 6

MEASUREMENT OF SMALL VALUES OF TRANSISTOR CAPACITANCE: This standard gives a test method for measuring transistor capacitance using a three-terminal bridge which employs a guard-circuit that eliminates the effect of extraneous capacitance.

February 1967; Reaffirmed September 1981, April 1999, October 2002 /JC-25 Committee $47.00

JESD 7-A

STANDARD FOR DESCRIPTION OF 54/74HCXXXX AND 54/74HCTXXXX HIGH SPEED CMOS DEVICES: This standard provides uniformity, multiplicity of sources, eliminate confusion, and ease of device specification and design by users for HC, and HCT CMOS devices. This standard specifies electrical parameters. It also includes appendices listing part numbers.

August 1986 / Committee!33JC402 $109.00

JESD 8- 1

ADDENDUM No. 1 to JESD8: INTERFACE STANDARD FOR LOW VOLTAGE TTL-COMPATIBLE (LVTTL) VLSI DIGITAL CIRCUITS

June 1994; Incorporated into JESD8-A, June 1994. JESD8-A was replaced by JESD8-B, September 1999. /JC-16 Committee

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JESD 8- 1-A

INTERFACE STANDARD FOR NOMINAL 0.3 V/3.3 V SUPPLY DIGITAL INTEGRATED CIRCUITS

June 1994; Incorporated into JESD8-A, June 1994. JESD8-A was replaced by JESD8-B, September 1999. /JC-16 Committee

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JESD 8- 2

ADDENDUM No. 2 to JESD8 - STANDARD FOR OPERATING VOLTAGES AND INTERFACE LEVELS FOR LOW VOLTAGE EMITTER-COUPLED LOGIC (ECL) INTEGRATED CIRCUITS: This Addendum No. 2 to JEDEC Standard No. 8 provides standard operating voltage and interface levels that can be used by designers and application engineers as they develop and introduce new products. Covers the ECL logic family designated 300K ECL. The 300K ECL family is Voltage and Temperature Compensated, with I/O interface levels compatible with the existing 100K ECL and 101K ECl families.

March 1993 /JC-16 Committee $40.00

JESD 8- 3A

ADDENDUM No. 3A to JESD8 - GUNNING TRANSCEIVER LOGIC (GTL) LOW-LEVEL, HIGH-SPEED INTERFACE STANDARD FOR DIGITAL INTEGRATED CIRCUITS: This Addendum No. 3 to JEDEC Standard No. 8 defines the dc input and output specifications for a low-level, high-speed interface for integrated devices.

May 2007 December 2006 /JC-16 Committee $40.00

JESD 8- 4

ADDENDUM No. 4 to JESD8 - CENTER-TAP-TERMINATED (CTT) INTERFACE LOW-LEVEL, HIGH-SPEED INTERFACE STANDARD FOR DIGITAL INTEGRATED CIRCUITS: This Addendum No. 4 to JEDEC Standard No. 8 defines the dc input and output specifications for a low-level, high-speed interface for integrated devices that can be a super-set of LVCMOS and LVTTL.

November 1993 /JC-16 Committee $38.00

JESD 8- 5A.01

ADDENDUM No. 5 to JESD8 - 2.5 V 0.2 V (NORMAL RANGE), AND 1.8 V TO 2.7 V (WIDE RANGE) POWER SUPPLY VOLTAGE AND INTERFACE STANDARD FOR NONTERMINATED DIGITAL INTEGRATED CIRCUIT: This standard defines power supply voltage ranges, dc interface parameters for a high speed, low voltage family of non-terminated digital circuits driving/driven by parts of the same family. The specifications in this standard represent a minimum set of 'base line' set of interface specifications for CMOS-compatible circuits.

September 2007 September 2004 /JC-16 Committee $43.00

JESD 8- 6

ADDENDUM No. 6 to JESD8 - HIGH SPEED TRANSCEIVER LOGIC (HSTL)- A 1.5 V OUTPUT BUFFER SUPPLY VOLTAGE BASED INTERFACE STANDARD FOR DIGITAL INTEGRATED CIRCUITS: This standard is a 1.5 volt high performance CMOS-based interface document suitable for high I/O count CMOS and BiCMOS devices operating at frequencies in excess of 200 Mhz.

August 1995 /JC-16 Committee $48.00

JESD 8- 7A

ADDENDUM No. 7 to JESD8 - 1.8 V + -0.15 V (NORMAL RANGE), AND 1.2 V - 1.95 V (WIDE RANGE) POWER SUPPLY VOLTAGE AND INTERFACE STANDARD FOR NONTERMINATED DIGITAL INTEGRATED CIRCUIT: This standard continues the voltage specification migration

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to the next level beyond the 2.5 V specification already established. Since this migration is driven by both process changes and performance/power, more entries can be expected in supporting required voltage levels. The rapidity of this evolution is expecting to increase because of the same feature sizes expected.

June 2006 June 2004 /JC-16 Committee $43.00

JESD 8- 8

ADDENDUM No. 8 to JESD8 - STUB SERIES TERMINATED LOGIC FOR 3.3 VOLTS (SSTL_3) A 3.3 V VOLTAGE BASED INTERFACE STANDARD FOR DIGITAL INTEGRATED CIRCUITS: This standard is a result of a major effort by the JC-16 Committee to develop a high performance CMOS-based interface suitable for high speed main memory applications in excess of 125 MHz.

August 1996 /JC-16 Committee $47.00

JESD 8- 9B

ADDENDUM No. 9B to JESD8 - STUB SERIES TERMINATED LOGIC FOR 2.5 VOLTS (SSTL_2): Includes Errata and Corrected Page 7 as of October 18, 2002. This standard defines the input, output specifications and ac test conditions for devices that are designed to operate in the SSTL_2 logic switching range, nominally 0 V to 2.5 V. The standard may be applied to ICs operating with separate VDD and VDDQ supply voltages. This standard has been developed particularly with the objective of providing a relatively simple upgrade path from MOS push-pull interface designs. The standard is particularly intended to improve operation in situations where busses must be isolated from relatively large stubs.

May 2002 /JC-16 Committee $55.00

JESD 8-11A.01

ADDENDUM No. 11A.01 to JESD8 - 1.5 V +/- 0.1 V (NORMAL RANGE) AND 0.9 - 1.6 V (WIDE RANGE) POWER SUPPLY VOLTAGE AND INTERFACE STANDARD FOR NONTERMINATED DIGITAL INTEGRATED CIRCUITS: This new standard provides specifications that will be used by several companies in new 1.5 V products designed in 0.12-0.15 um CMOS technologies, and in components that interface with them. The specifications allow limited interoperability with products using the existing JEDEC HSTL specification (JESD8-6). This version is a minor editorial revision as noted in Annex A.

September 2007 June 2004 /JC-16 Committee $41.00

JESD 8-12A.01

1.2 V +/- 0.1 V (NORMAL RANGE) AND 0.8 - 1.3 V (WIDE RANGE) POWER SUPPLY VOLTAGE AND INTERFACE STANDARD FOR NONTERMINATED DIGITAL INTEGRATED CIRCUITS: This standard defines power supply voltage ranges, dc interface and switching parameters for a high speed, low voltage family of nonterminated digital circuits driving/driven by parts of the same family, or mixed families which comply with the input receiver specifications. The specifications in this standard represent a minimum set of interface specifications for CMOS compatible circuits.

September 2007 June 2004 /JC-16 Committee $41.00

JESD 8-13

SCALABLE LOW-VOLTAGE SIGNALING FOR 400 MV (SLVS-400): This standard defines the input, output, and termination specifications for differential signaling in the SLVS-400 environment, nominally between 0 and 400 mV. Power supplies other than the nominal 800 mV power for the SLVS interface are not specified.

October 2001 /JC-16 Committee $41.00

JESD 8-14A.01

1.0 V +/- 0.1 V (NORMAL RANGE) AND 0.7 V - 1.1 V (WIDE RANGE) POWER SUPPLY VOLTAGE AND INTERFACE STANDARD FOR NONTERMINATED DIGITAL INTEGRATED CIRCUITS: This new standard provides specifications that will be used by several companies in new 1.0 V products designed in 0.10-0.12 um CMOS technologies, and in components that interface with them. This standard defines power supply voltage ranges, dc interface and switching parameters for a high speed, low voltage family of nonterminated digital circuits driving/driven by parts of the same family, or mixed families which comply with the input receiver specifications. The specifications in this standard represent a minimum set of interface specifications for CMOS compatible circuits. This version is a minor editorial revision as noted in Annex A.

September 2007 June 2004 /JC-16 Committee $41.00

JESD 8-15A

STUB SERIES TERMINATED LOGIC FOR 1.8 V (SSTL_18): This standard defines the input, output specifications and ac test conditions for devices that are designed to operate in the SSTL_18 logic switching range, nominally 0 V to 1.8 V. The standard may be applied to ICs

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operating with separate VDD and VDDQ supply voltages. The VDD value is not specified in this standard; however VDD and VDDQ will have the same voltage level in many cases.

September 2003 /JC-16 Committee $49.00

JESD 8-17

DRIVER SPECIFICATIONS FOR 1.8 V POWER SUPPLY POINT-TO-POINT DRIVERS This material is intended to be reflected in supplier specifications for point to point DDR devices ranging from 400 Mb/s to 800 Mb/s operation. It is a method to specify driver impedance with something other than a number that does not nec-essarily define how it operates in a real net This standard addresses this issue using net lengths and specifies how much uncertainty can exist in the data for each speed supported.

November 2004 May 2002 /JC-16 Committee $40.00

JESD 8-18A

FBDIMM SPECIFICATION: HIGH SPEED DIFFERENTIAL PTP LINK AT 1.5 V This specification defines the high-speed differential point-to-point signaling link for FBDIMM, operating at the buffer supply voltage of 1.5V that is provided at the FBDIMM DIMM connector. This specification also applies to FBDIMM host chips which may operate with a different supply voltage. The link consists of a transmitter and a receiver and the interconnect in between them. The transmitter sends serialized bits into a lane and the receiver accepts the electrical signals of the serialized bits and transforms them into a serialized bit-stream. The first generation FBDIMM link is being specified to operate from 3.2 to 4.8 Gb/s. The specifications are defined for three distinct bit-rates of operation: 3.2 Gb/s, 4.0 Gb/s and 4.8 Gb/s.

March 2008 March 2007 /JC-16 Committee $98.00

JESD 8C.01

INTERFACE STANDARD FOR NOMINAL 3.0 V/3.3 V SUPPLY DIGITAL INTEGRATED CIRCUITS: This standard (a replacement of JEDEC Standards No. 8, 8-1, 8-1-A, and 8-A) defines dc interface parameters for a family of digital circuits operating from a power supply of nominal 3.0 V/3.3. V and driving/driven by parts of the same family. The specifications in this standard represent a minimum set of 'base line' set of interface specifications for LVTTL-compatible and LVCMOS-compatible circuits.

September 2007 June 2004 /JC-16 Committee $45.00

JESD 9-A

METAL PACKAGE SPECIFICATION FOR MICROELECTRONIC PACKAGES AND COVERS: This standard establishes the general requirements and quality assurance provisions that can be specified and met in procuring microelectronics packages and covers, manufactured from matched seal with and without high thermal conductivity base materials, intended for use in fabricating hybrid microelectronics circuits. This document details those minimum requirements necessary for metal packages' use exclusively.

April 1987; Under Revision /JC-13.5 Subcommittee $71.00

JESD 10

LOW FREQUENCY POWER TRANSISTORS: This standard consists of a listing of letter symbols, terms, and definitions that are used in power transistors. It also includes information on JEDEC registration procedures, verification tests, and thermal characteristics.

January 1976; Reaffirmed September 1981, October 2002 April 1999 /JC-25 Committee $147.00

JESD 11

CHIP CARRIER PINOUTS STANDARDIZED FOR CMOS 4000, HC AND HCT SERIES OF LOGIC CIRCUITS: This standard indicates the procedures used to convert existing DIP and flat packages for digital parts (SSI & MSI) to chip carrier packages.

December 1984 / Committee!33JC402 $41.00

JESD 12

SEMICUSTOM INTEGRATED CIRCUITS (FORMERLY PUBLISHED AS STANDARD FOR GATE ARRAY BENCHMARK SET): The purpose of these benchmarks is to provide a common set of high level functions which serve as vehicles for comparing the performance of gate arrays implemented in any technology using any internal structure. These benchmarks effectively provide an unbiased measure of gate array vendors' ability to implement a desired complex function on a particular gate array at a known level of performance.

June 1985 / Committee!33JC44 $43.00

JESD 12-1B

ADDENDUM No. 1 to JESD12 - TERMS AND DEFINITIONS FOR GATE ARRAYS AND CELL-BASED INTEGRATED CIRCUITS: The purpose of this standard is to promote the uniform use of abbreviations, terms, and definitions throughout the semiconductor industry. It is a useful guide for users, manufactures, educators, technical writers, and others interested in the characterization, nomenclature, and classification of semicustom integrated circuits.

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August 1993 / Committee!33JC44 $48.00

JESD 12-2

ADDENDUM No. 2 to JESD12 - STANDARD FOR CELL-BASED INTEGRATED CIRCUIT BENCHMARK SET: The purpose of these benchmarks is to provide a common set of high level functions that serve as vehicles for comparing the performance of cell-based ICs implemented in any technology using any internal structure. JESD12-2 extends the gate array benchmark set (JESD12) to cell-based ICs.

February 1986 / Committee!33JC44 $61.00

JESD 12-3

ADDENDUM No. 3 to JESD12 - CMOS GATE ARRAY MACROCELL STANDARD: This standard defines a minimum set of macro cell standards for CMOS gate arrays. A total of 41 macro cell types are addressed, all of which are commonly used by gate array designers to implement Application Specific Integrated Circuits.

June 1986 / Committee!33JC44 $47.00

JESD 12-4

ADDENDUM No. 4 to JESD12 - METHOD OF SPECIFICATION OF PERFORMANCE PARAMETERS FOR CMOS SEMICUSTOM INTEGRATED CIRCUITS: This standard defines how to specify various performance parameters of semicustom ICs, including cell and interconnect propagation delays, input/output levels and capacitance, and power dissipation.

April 1987 / Committee!33JC44 $48.00

JESD 12-5

ADDENDUM No. 5 to JESD12 - DESIGN FOR TESTABILITY GUIDELINES: This standard is intended to provide circuit designers with the information needed to develop complex integrated circuits that can be reliably and economically tested without compromising flexibility.

August 1988 / Committee!33JC44 $109.00

JESD 12-6

ADDENDUM No. 6 to JESD12 - INTERFACE STANDARD FOR SEMICUSTOM INTEGRATED CIRCUITS: This standard defines logic interface levels for CMOS, TTL, ECL, and BiCC inputs and outputs. This standard is intended to provide an industry-wide set of specifications, for Application Specific Integrated Circuit (ASIC) signal inputs and outputs, both necessary and sufficient to define a circuits electrical interfacing with the external environment. JESD12-6 is intended to provide the ASIC manufacturer and user with a common set of signal interface levels. The standard defines interface levels for 5 volt operation.

March 1991 / Committee!33JC44 $43.00

JESD 13-B

STANDARD SPECIFICATION FOR DESCRIPTION OF B SERIES CMOS DEVICES: This standard provides for uniformity, multiplicity of sources, elimination of confusion, and ease of device specifications and system design by users. It gives electrical levels and timing diagrams for B Series CMOS devices.

May 1980 / Committee!33JC402 $63.00

JESD 14

SEMICONDUCTOR POWER CONTROL MODULES: Semiconductor Power Control Modules (SPCM) are modules consisting of thyristors or transistors, or both, as the primary controlling elements. Methods of manufacture of semiconductor power control modules include the assembling of individual components and the use of semiconductor hybrids or monolithic processing technologies, or both.

November 1986; Reaffirmed June 1992, April 1999, April 2002 April 2002 /JC-22.2 Subcommittee $47.00

JESD 15-3

TWO-RESISTOR COMPACT THERMAL MODEL GUIDELINE This document specifies the definition and construction of a two-resistor compact thermal model (CTM) from the JEDEC junction-to-case and junction-to-board thermal metrics. The guidance provided in this document only applies to thermal metrics defined in JEDEC standards JESD51-8 and JESD51-12. The scope of this document is limited to single-die packages that can be effectively represented by a single junction temperature.

July 2008 March 2006 /JC-15 Committee $57.00

JESD 16-A

ASSESSMENT OF AVERAGE OUTGOING QUALITY LEVELS IN PARTS PER MILLION (PPM): This standard was revised to clarify assumptions necessary to estimate AOQ, revise the minimum sample size algorithm, address small sample size concerns, and provide methods for combining groups for AOQ estimation. Derivation of any new methods for combing groups for AOQ estimation. Derivation of any new methods introduced into this document

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have been provided in annexes. A statistical method is based on confidence interval statistics. A procedure was established for reporting AOQ when the minimum sample size criterion is not met.

April 1995 /JC-13 Committee $61.00

JESD 17 **LATCH-UP IN CMOS INTEGRATED CIRCUITS - SUPERSEDED BY JESD78, February 1999**

August 1988; Rescinded February 1999 February 1999 / Committee!33JC402

JESD 18-A **STANDARD FOR DESCRIPTION OF FAST CMOS TTL COMPATIBLE LOGIC:** The purpose of this standard is to provide for uniformity, multiplicity of sources, elimination of confusion, and ease of device specification and design by users. The standard covers specifications for description of '54/74FCTXXXX' series fast CMOS TTL compatible devices.

January 1993 / Committee!33JC402 $63.00

JESD 19 **GENERAL STANDARD FOR STATISTICAL PROCESS CONTROL (SPC) - SUPERSEDED by EIA-557-A**

July 1988; Rescinded July 1995 /JC-13 Committee

JESD 20 **STANDARD FOR DESCRIPTION OF 54/74ACXXXXX AND 54/74ACTXXXXX ADVANCED HIGH-SPEED CMOS DEVICES:** This standard describes electrical parameters for this class of CMOS devices.

September 1990 / Committee!33JC402 $147.00

JESD 21-C **CONFIGURATIONS FOR SOLID STATE MEMORIES:** This revision of JESD21 is substantially different from previous issues because it reflects advancement in semiconductor technology and computer design needs. A new class of memory devices, the multiport DRAM (MPDRAM) C also know as 'Video Ram' because of the most common application for the devices C is represented. A new family of SRAMs which addresses the increasing need for high speed is introduced. Additional families of devices in the SOJ and Zip packages are included. The material in this revision is organized primarily by function (ROM, EPROM, SRAM, DRAM, etc.) rather than by technology and word length. Pinouts for SIMM and DIMM are included along with presence detect schemes. A current set of terms has also been included. JESD21-C is a compilation of all memory device standards that have been developed by the JC-42 Committee and approved by the JEDEC BoD from September 1989 to present. This latest issue has changed to a loose-leaf format and comes in a three-ring binder so that new drawings can be added without requiring a new publication. Time of publication of the material is identified by release number, i.e., if marked Release 8, this item was approved and released in 1998, if marked Release 13, this item was approved and released in 2003.

May 2003; Under Revision Sections in this document may be under revision at any time. /JC-42 Committee $150.00

JESD 21-C AUS **ANNUAL UPDATING SERVICE:** The JEDEC Office has generated a mailing list for those who wish to subscribe to updates of this publication. A payment is required for subscription to this updating service.

January 2004 /JC-42 Committee $50.00

JESD 22-A100C **CYCLED TEMPERATURE HUMIDITY BIAS LIFE TEST:** The Cycled Temperature-humidity-bias Life Test is performed for the purpose of evaluating the reliability of nonhermetic packaged solid state devices in humid environments. It employs conditions of temperature cycling, humidity, and bias that accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors that pass through it. The Cycled Temperature-Humidity-Bias Life Test is typically performed on cavity packages (e.g., MQUADs, lidded ceramic pin grid arrays, etc.) as an alternative to JESD22-A101 or JESD22-A110.

October 2007 January 2007 /JC-14.1 Subcommittee $49.00

JESD 22-A101-B **STEADY-STATE TEMPERATURE HUMIDITY BIAS LIFE TEST:** This standard establishes a defined method and conditions for performing a temperature humidity life test with bias applied. The test is used to evaluate the reliability of non-hermetic packaged solid state devices in humid environments. It employs high temperature and humidity conditions to

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accelerate the penetration of moisture through external protective material or along interfaces between the external protective coating and conductors or other features which pass through it. This revision enhances the ability to perform this test on a device which cannot be biased to achieve very low power dissipation.

April 1997 /JC-14.1 Subcommittee $40.00

JESD 22-A102-C **ACCELERATED MOISTURE RESISTANCE - UNBIASED AUTOCLAVE:** This test allows the user to evaluate the moisture resistance of nonhermetic packaged solid state devices. The Unbiased Autoclave Test is performed to evaluate the moisture resistance integrity of non-hermetic packaged solid state devices using moisture condensing or moisture saturated steam environments. It is a highly accelerated test which employs conditions of pressure, humidity and temperature under condensing conditions to accelerate moisture penetration through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors passing through it. This test is used to identify failure mechanisms internal to the package and is destructive.

December 2000; Reaffirmed June 2008 /JC-14.1 Subcommittee $38.00

JESD 22-A103C **HIGH TEMPERATURE STORAGE LIFE:** The test is applicable for evaluation, screening, monitoring, and/or qualification of all solid state devices. High Temperature storage test is typically used to determine the effect of time and temperature, understorage conditions, for thermally activated failure mechanisms of solid state electronic devices, includingnonvolatile memory devices (data retention failure mechanisms). During the test elevated temperatures(accelerated test conditions) are used without electrical stress applied. This test may be destructive,depending on Time, Temperature and Packaging (if any).

November 2004 June 2004 /JC-14.1 Subcommittee $40.00

JESD 22-A104C **TEMPERATURE CYCLING:** This standard provides a method for determining solid state devices capability to withstand extreme temperature cycling. Changes in this revision include requirements that the worst-case load temperature must reach the specific extremes rather than just requiring that the chamber ambient temperature reach the extremes. This ensures that the test specimens will reach the specified temperature extremes regardless of chamber loading. Definitions are provided for Load, Monitoring Sensor, Worst-Case Load Temperature, and Working Zone. The transfer time has been tightened from 5 minutes to 1 minute. Five new test conditions have been added as well as a caution on test conditions which exceed the glass transition temperature of plastic package solid devices.

May 2005 January 2005 /JC-14.1 Subcommittee $45.00

JESD 22-A105C **POWER AND TEMPERATURE CYCLING:** The power and temperature cycling test is performed to determine the ability of a device to withstand alternate exposures at high and low temperature extremes and simultaneously the operating biases are periodically applied and removed. It is intended to simulate worst case conditions encountered in application environments. The power and temperature cycling test is considered destructive and is only intended for device qualification. This test method applies to semiconductor devices that are subjected to temperature excursions and required to power on and off during all temperatures.

January 2004 June 2003 /JC-14.1 Subcommittee $40.00

JESD 22-A106B **THERMAL SHOCK:** This test is conducted to determine the resistance of a part to sudden exposure to extreme changes in temperature and to the effect of alternate exposures to these extremes.

June 2004 January 2003 /JC-14.1 Subcommittee $40.00

JESD 22-A107B **SALT ATMOSPHERE:** This salt Atmosphere test is conducted to determine the resistance of solid state devices to corrosion. It is an accelerated test that simulates the effects of severe seacoast atmosphere on all exposed surfaces. The salt atmosphere test is considered destructive. It is intended for lot acceptance, process monitor, and qualification testing.

January 2004 January 2003 /JC-14.1 Subcommittee $38.00

JESD 22-A108C **TEMPERATURE, BIAS, AND OPERATING LIFE:** A revised method for determining the effects of bias conditions and temperature, over time, on solid state devices is now available. Revision B of A108 includes low temperature operating life (LTOL) and high temperature

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gate bias (HTGB) stress conditions, revised cool down requirements for high temperature stress, and a procedure to follow if parts are not tested within the allowed time window.

June 2005 March 2004 /JC-14.1 Subcommittee $43.00

JESD 22-A109-A **HERMETICITY:** This revised test method establishes a standard procedure for determining the effectiveness of the seal of hermetically sealed solid state devices. The objective of this revision was to modify the test parameters to reflect current practice and to eliminate the specification of fluorocarbons, banned from use due to environmental concerns.

July 2001 /JC-14.1 Subcommittee $43.00

JESD 22-A110-B **HIGHLY ACCELERATED TEMPERATURE AND HUMIDITY STRESS TEST (HAST)** The purpose of this new test method is to evaluate the reliability of nonhermetic packaged solid state devices in humid environments. It employs severe conditions of temperature, humidity, and bias that accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors which pass through it.

February 1999; Reaffirmed June 2008 /JC-14.1 Subcommittee $40.00

JESD 22-A111 **EVALUATION PROCEDURE FOR DETERMINING CAPABILITY TO BOTTOM SIDE BOARD ATTACH BY FULL BODY SOLDER IMMERSION OF SMALL SURFACE MOUNT SOLID STATE DEVICES:** The purpose of this test method is to identify the potential wave solder classification level of small plastic Surface Mount Devices (SMDs) that are sensitive to moisture-induced stress so that they can be properly packaged, stored, and handled to avoid subsequent mechanical damage during the assembly wave solder attachment and/or repair operations. This test method also provides a reliability preconditioning sequence for small SMDs that are wave soldered using full body immersion. This test method, may be used by users to determine what classification level should be used for initial board level reliability qualification.

May 2004 June 2000 /JC-14.1 Subcommittee $47.00

JESD 22-A112-A **MOISTURE-INDUCED STRESS SENSITIVITY FOR PLASTIC SURFACE MOUNT DEVICES - SUPERSEDED BY J-STD-020A, April 1999.** J-STD-020 is now on revision D.

November 1995; Rescinded May 2000 May 2000 /JC-14.1 Subcommittee

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JESD 22-A113F **PRECONDITIONING OF PLASTIC SURFACE MOUNT DEVICES PRIOR TO RELIABILITY TESTING:** This Test Method establishes an industry standard preconditioning flow for nonhermetic solid state SMDs (surface mount devices) that is representative of a typical industry multiple solder reflow operation. These SMDs should be subjected to the appropriate preconditioning sequence of this document by the semiconductor manufacturer prior to being submitted to specific in-house reliability testing (qualification and reliability monitoring) to evaluate long term reliability (which might be impacted by solder reflow).

October 2008 January 2008 /JC-14.1 Subcommittee $51.00

JESD 22-A114E **ELECTROSTATIC DISCHARGE (ESD) SENSITIVITY TESTING HUMAN BODY MODEL (HBM):** This test method establishes a standard procedure for testing and classifying microcircuits according to their susceptibility to damage or degradation by exposure to a defined electrostatic Human Body Model (HBM) discharge (ESD). The objective is to provide reliable, repeatable HBM ESD test results so that accurate classifications can be performed.

January 2007 October 2005 /JC-14.1 Subcommittee $49.00

JESD 22-A115-A **ELECTROSTATIC DISCHARGE (ESD) SENSITIVITY TESTING MACHINE MODEL (MM):** This method establishes a standard procedure for testing and classifying microcircuits according to their susceptibility to damage or degradation by exposure to a defined Machine Model (MM) electrostatic discharge (ESD). The objective is to provide reliable, repeatable MM ESD test results so that accurate classifications can be performed.

October 1997 This is a valid test method, however it is not currently being used in the industry, the preferred industry test methods are JESD22A114 or JESD22C101. /JC-14.1 Subcommittee $45.00

JESD 22-A117A **ELECTRICALLY ERASABLE PROGRAMMABLE ROM (EEPROM) PROGRAM/ERASE ENDURANCE AND DATA RETENTION TEST:** This method establishes a standard procedure for determining the data cycling endurance and data retention capability of non-volatile memory cells. It is intended as a qualification and monitor test procedure. This test is also applicable to FLASH

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EEPROM integrated circuits and Erasable Programmable Logic Devices (EPLD) with embedded EEPROM or FLASH memory.

March 2006 June 2005 /JC-14.3 Subcommittee $45.00

JESD 22-A118

ACCELERATED MOISTURE RESISTANCE - UNBIASED HAST: The Unbiased HAST is performed for the purpose of evaluating the reliability of non-hermetic packaged solid-state devices in humid environments. It is a highly accelerated test which employs temperature and humidity under non-condensing conditions to accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors which pass through it. Bias is not applied in this test to ensure the failure mechanisms potentially overshadowed by bias can be uncovered (e.g. galvanic corrosion). This test is used to identify failure mechanisms internal to the package and is destructive.

December 2000; Reaffirmed June 2008 /JC-14.1 Subcommittee $41.00

JESD 22-A119

LOW TEMPERATURE STORAGE LIFE The test is applicable for evaluation, screening, monitoring, and/or qualification of all solid state devices. Low Temperature storage test is typically used to determine the effect of time and temperature, under storage conditions, for thermally activated failure mechanisms of solid state electronic devices, including nonvolatile memory devices (data retention failure mechanisms). During the test reduced temperatures (test conditions) are used without electrical stress applied. This test may be destructive, depending on Time, Temperature and Packaging (if any).

November 2004 June 2004 /JC-14.1 Subcommittee $40.00

JESD 22-A120A

TEST METHOD FOR THE MEASUREMENT OF MOISTURE DIFFUSIVITY AND WATER SOLUBILITY IN ORGANIC MATERIALS USED IN INTEGRATED CIRCUITS: This specification details the procedures for the measurement of characteristic bulk material properties of moisture diffusivity and water solubility in organic materials used in the packaging of IC components. These two material properties are important parameters for the effective reliability performance of plastic packaged ICs after exposure to moisture and subjected to high temperature solder reflow.

January 2008 June 2006 /JC-14.1 Subcommittee $50.00

JESD 22-A121A

MEASURING WHISKER GROWTH ON TIN AND TIN ALLOY SURFACE FINISHES The predominant terminal finishes on electronic components have been Sn-Pb alloys. As the industry moves toward Pb-free components and assembly processes, the predominant terminal finish materials will be pure Sn and alloys of Sn, including Sn-Bi and Sn-Ag. Pure Sn and Sn-based alloy electrodeposits and solder-dipped finishes may grow tin whiskers, which could electrically short across component terminals or break off the component and degrade the performance of electrical or mechanical parts.

July 2008 September 2008 /JC-14.1 Subcommittee $68.00

JESD 22-B100B

PHYSICAL DIMENSION: The standard provides a method for determining whether the external physical dimensions of the device are in accordance with the applicable procurement document. This revision includes a change in details to be specified by the procurement document.

June 2003; Reaffirmed June 2006 September 2002 /JC-14.1 Subcommittee $38.00

JESD 22-B101A

EXTERNAL VISUAL: The purpose of this inspection is to verify that the materials, design, construction, markings, and workmanship of the device are in accordance with the applicable procurement document. External visual is a nondestructive test and applicable for all package types. The test is useful for qualification, process monitor, or lot acceptance.

October 2004 January 2004 /JC-14.1 Subcommittee $43.00

JESD 22-B102E

SOLDERABILITY: This test method provides optional conditions for preconditioning and soldering for the purpose of assessing the solderability of device package terminations. It provides procedures for dip & look solderability testing of through hole, axial and surface mount devices and a surface mount process simulation test for surface mount packages. The purpose of this test method is to provide a means of determining the solderability of device package terminations that are intended to be joined to another surface using lead (Pb) containing or Pb-free solder for the attachment.

October 2007 January 2007 /JC-14.1 Subcommittee $62.00

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JESD 22-B103B **VIBRATION, VARIABLE FREQUENCY:** The Vibration, Variable Frequency Test Method is intended to determine the ability of component(s) to withstand moderate to severe vibration as a result of motion produced by transportation or filed operation of electrical equipment. This is a destructive test that is intended for component qualification.

June 2002; Reaffirmed June 2006 /JC-14.1 Subcommittee $43.00

JESD 22-B104C **MECHANICAL SHOCK:** This test is intended to determine the suitability of component parts for use in electronic equipment that may be subjected to moderately severe shocks as a result of suddenly applied forces or abrupt changes in motion produced by rough handling, transportation, or field operation. Shock of this type may disturb operating characteristics, particularly if the shock pulses are repetitive. This is a destructive test intended for device qualification. It is normally applicable to cavity-type packages.

November 2004 - Typo found on pg.1 in title, a new version dated December 2004 has been posted. if you downloaded between 11/10/04 & 12/10/04, please download againJanuary 2004 /JC-14.1 Subcommittee $41.00

JESD 22-B105C **LEAD INTEGRITY:** This test method provides various tests for determining the integrity lead/package interface and the lead itself when the lead(s) are bent due to faulty board assembly followed by rework of the part for reassembly. For hermetic packages it is rececommend that this test be followed by hermeticity tests in accordance with Test Method A109 to determine if there are any adverse effects from the stresses applied to the seals as well as to the leads. These tests, including each of its test conditions, is considered destructive and is only recommended for qualification testing. This test is applicable to all through-hole devices and surface-mount devices requiring lead forming by the user.

May 2003; Reaffirmed June 2006 /JC-14.1 Subcommittee $48.00

JESD 22-B106D **RESISTANCE TO SOLDER SHOCK FOR THROUGH-HOLE MOUNTED DEVICES:** This method established a standard procedure for determining whether through-hole solid state devices can withstand the effects of the temperature to which they will be subject during soldering of their leads. This revision updates the references to currently military standards.

April 2008 November 2007 /JC-14.1 Subcommittee $49.00

JESD 22-B107C **MARKING PERMANENCY:** This test method provides two tests for determining the marking permanency of ink marked integrated circuits. A new non-destructive tape test method is introduced to quickly determine marking integrity. The test method also specifies a resistance to solvents method based upon MIL Std 883 Method 2015.

September 2004 October 2002 /JC-14.1 Subcommittee $43.00

JESD 22-B108A **COPLANARITY TEST FOR SURFACE-MOUNT SEMICONDUCTOR DEVICES:** The purpose of this test is to measure the deviation of the terminals (leads or solder balls) from coplanarity for surface-mount semiconductor devices.

January 2003 /JC-14.1 Subcommittee $41.00

JESD 22-B109 **FLIP CHIP TENSILE PULL:** The Flip Chip Tensile Pull Test Method is performed to determine the fracture mode and strength of the solder bump interconnection between the flip chip die and the substrate. It should be used to assess the consistency of the chip join process. This test method is a destructive test.

June 2002 /JC-14.1 Subcommittee $41.00

JESD 22-B110A **SUBASSEMBLY MECHANICAL SHOCK:** The new test method JESD22-B110 provides guidance for in-situ testing of mechanical shock resistance of components as mounted in a subassembly. Using terms, procedures, and test levels in common with JESD22-B104B, this test method provides a range of test level options to improve test applicability and compatibility with fragility test procedures. Test procedures are detailed, including test card and fixture needs, test tolerances, test documentation, component preparation, and definition of terms.

November 2004 January 2004 /JC-14.1 Subcommittee $45.00

JESD 22-B111 **BOARD LEVEL DROP TEST METHOD OF COMPONENTS FOR HANDHELD ELECTRONIC PRODUCTS:** This Board Level Drop Test Method is intended to evaluate and compare drop performance of surface mount electronic components for handheld electronic product applications in an accelerated test environment, where excessive flexure of a circuit board causes product failure. The purpose is to standardize the test board and test methodology to provide a

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reproducible assessment of the drop test performance of surface mounted components while duplicating the failure modes normally observed during product level test.

July 2003 /JC-14.1 Subcommittee $48.00

JESD 22-B112

HIGH TEMPERATURE PACKAGE WARPAGE MEASUREMENT METHODOLOGY The purpose of this test method is to measure the deviation from uniform flatness of an integrated circuit package body for the range of environmental conditions experienced during the surface-mount soldering operation.

May 2005 October 2004 /JC-14.1 Subcommittee $49.00

JESD 22-B113

BOARD LEVEL CYCLIC BEND TEST METHOD FOR INTERCONNECT RELIABILITY CHARACTERIZATION OF COMPONENTS FOR HANDHELD ELECTRONIC PRODUCTS The Board Level Cyclic Bend Test Method is intended to evaluate and compare the performance of surface mount electronic components in an accelerated test environment for handheld electronic products applications. The purpose is to standardize the test methodology to provide a reproducible performance assessment of surface mounted components while duplicating the failure modes normally observed during product level test. This is not a component qualification test and is not meant to replace any product level test that may be needed to qualify a specific product and assembly.

March 2006 October 2005 /JC-14.1 Subcommittee $49.00

JESD 22-B115

SOLDER BALL PULL This document describes a test method only; acceptance criteria and qualification requirements are not defined. This test method applies to solder ball pull force testing prior to end-use attachment. Solder balls are pulled individually using mechanical jaws; force and failure mode data are collected and analyzed. Other specialized solder ball pull methods using a heated thermode, gang pulling of multiple solder joints, etc., are outside the scope of this document. Both low and high speed testing are covered by this document.

May 2007 September 2006 /JC-14.1 Subcommittee $49.00

JESD 22-B116

WIRE BOND SHEAR TEST: This test method establishes a standard procedure for determining the strength of an integrated circuit wire bond by shearing the wire from the surface it is bonded to and measuring the force required. This method serves as an alternative to pulling the wire vertically until the wire separates from one of it's two bonded surfaces. It also provides guidelines for determining an appropriate minimum shear force for gold balls on aluminum alloy bonding surfaces.

July 1998 /JC-14.1 Subcommittee $45.00

JESD 22-B117A

SOLDER BALL SHEAR: The purpose of this test is conducted to assess the ability of solder balls to withstand mechanical shear forces that may be applied during device manufacturing, handling, test, shipment and end-use conditions. Solder ball shear is a destructive test.

October 2006 January 2006 /JC-14.1 Subcommittee $45.00

JESD 22-C100-A HIGH TEMPERATURE CONTINUITY - RESCINDED, November 1999

April 1990; Rescinded November 1999 /JC-14.1 Subcommittee

JESD 22-C101D

FIELD-INDUCED CHARGED-DEVICE MODEL TEST METHOD FOR ELECTROSTATIC DISCHARGE WITHSTAND THRESHOLDS OF MICROELECTRONIC COMPONENTS: This new test method describes a uniform method for establishing charged-device model electrostatic discharge withstand thresholds. The charged-device-model simulates charging/discharging events that occur in production equipment and processes. Potential for CDM ESD events occurs whenever there is metal-to-metal contact in manufacturing. One of many examples is a device sliding down a shipping tube hitting a metal surface. Discharges to devices on unterminated circuit assemblies are also well-modeled by the CDM test. DM ESD events not only reduce assembly yields but can also produce device damage that goes undetected by factory test and later is the cause of a latent failure.

October 2008 January 2008 /JC-14.1 Subcommittee $54.00

JESD 22B114

MARK LEGIBILITY This standard describes a nondestructive test to assess solid state device mark legibility. The specification applies only to solid state devices that contain markings, regardless of the marking method. It does not define what devices must be marked or the method in which the device is marked, i.e., ink, laser, etc. The standard is

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limited in scope to the legibility requirements of solid state devices, and does not replace related reference documents listed in this standard.

March 2008 September 2007 /JC-14.3 Subcommittee $50.00

JESD 23

TEST METHODS AND CHARACTER DESIGNATION FOR LIQUID CRYSTAL DEVICES: This standard specifies a collection of procedures for testing and character designation of liquid crystal devices.

May 1982 $57.00

JESD 24

POWER MOSFETS: This standard contains a listing of terms and definitions and letter symbols; a description of established procedures that are followed in the assignment of semiconductor-industry-type designations to power transistors; electrical verification test; thermal characteristics; and a user's guide.

July 1985 /JC-25 Committee $71.00

JESD 24- 1

ADDENDUM No. 1 to JESD24 - METHOD FOR MEASUREMENT OF POWER DEVICE TURN-OFF SWITCHING LOSS: Describes the method of a typical oscilloscope waveform and the basic test circuit employed in the measurement of turn off loss for bipolar, IGBT and MOSFET power semiconductors. This method can be used as a standard for evaluating power semiconductor turn-off switching loss capability and defines standard terminology that should be referenced within the electronic industry.

October 1989; Reaffirmed April 1999, October 2002 /JC-25 Committee $41.00

JESD 24- 2

ADDENDUM No. 2 to JESD24 - GATE CHARGE TEST METHOD: This addendum establishes a method for measuring power device gate charge. A gate charge test is performed by driving the device gate with a constant current and measuring the resulting gate voltage response. Constant gate current scales the gate voltage, a function of time, to a function of coulombs. The slope of the generated response reflects the active device capacitance as it varies during the switching transition . Gate charge measurements are useful for characterizing the large signal switching performance of power MOS and IGBT devices. Developed over a four year span by the JEDEC JC-25 Committee, the method defines a repeatable means of measuring the widely published Qgd charge values.

January 1991; Reaffirmed October 2002 April 1999 /JC-25 Committee $41.00

JESD 24- 3

ADDENDUM No. 3 to JESD24 - THERMAL IMPEDANCE MEASUREMENTS FOR VERTICAL POWER MOSFETS (DELTA SOURCE-DRAIN VOLTAGE METHOD): The purpose of this test method is to measure the thermal impedance of the MOSFET under the specified conditions of applied voltage, current and pulse duration. The temperature sensitivity if the forward voltage drop of the source-drain is used as the junction temperature indicator. This method is particularly suitable to enhancement mode, power MOSFETs having relatively long thermal response times. This test method may be used to measure the thermal response of junction to a heating pulse, to ensure proper die mountdown to its case, or the dc thermal resistance, by the proper choice of the pulse duration and magnitude if the heating pulse.

November 1990; Reaffirmed April 1999 /JC-25 Committee $47.00

JESD 24- 4

ADDENDUM No. 4 to JESD24 - THERMAL IMPEDANCE MEASUREMENTS FOR BIPOLAR TRANSISTORS (DELTA BASE-EMITTER VOLTAGE METHOD): The purpose of this test method is to measure the thermal impedance of the Bipolar Transistor under the specified conditions of applied voltage, current and pulse duration. The temperature sensitivity of the base-emitter voltage is used as the junction temperature indicator. This test method is used to measure the thermal response of the junction to a heating pulse. Specifically, the test may be used to measure dc thermal resistance, and to ensure proper die mountdown to its case. This is accomplished through the appropriate choice of pulse duration and heating power magnitude.

November 1990; Reaffirmed October 2002 April 1999 /JC-25 Committee $47.00

JESD 24- 5

ADDENDUM No. 5 to JESD24 - SINGLE PULSE UNCLAMPED INDUCTIVE SWITCHING (UIS) AVALANCHE TEST METHOD: This method describes a means for testing the ability of a power switching device to withstand avalanche breakdown.

August 1990; Reaffirmed october 2002 April 1999 /JC-25 Committee $38.00

JESD 24- 6

ADDENDUM No. 6 to JESD24 - THERMAL IMPEDANCE MEASUREMENTS FOR INSULATED GATE BIPOLAR TRANSISTORS: This standard describes in detail the method for thermal

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measurements of Insulated Gate Bipolar Transistors (IGBTs) and is suitable for use both in manufacturing and application of the devices. The method covers both thermal transient and thermal equilibrium measurements for manufacturing process control and device characterization purposes. Properly implemented, JESD24-6 provides a basis for obtaining realistic thermal parametric values that will benefit supplier's internal effectiveness and will be useful to the design and manufacturer of reliable IGBT circuits.

October 1991; Reaffirmed October 2002 April 1999 /JC-25 Committee $47.00

JESD 24- 7

ADDENDUM No. 7 to JESD24 - COMMUTATING DIODE SAFE OPERATING AREA TEST PROCEDURE FOR MEASURING dv/dt DURING REVERSE RECOVERY OF POWER TRANSISTORS: Defines methods for verifying the diode recovery stress capability of power transistors.

August 1982; Reaffirmed October 2002 April 1999 /JC-25 Committee $40.00

JESD 24- 8

ADDENDUM No. 8 to JESD24 - METHOD FOR REPETITIVE INDUCTIVE LOAD AVALANCHE SWITCHING: Determines the repetitive inductive avalanche switching capability of power switching transistors.

August 1992; Reaffirmed October 2002 April 1999 /JC-25 Committee $40.00

JESD 24- 9

ADDENDUM No. 9 to JESD24 - SHORT CIRCUIT WITHSTAND TIME TEST METHOD: Test method to determine how long a device can survive a short circuit condition with a given drive level.

August 1992; Reaffirmed October 2002 April 1999 /JC-25 Committee $40.00

JESD 24-10

ADDENDUM No. 10 to JESD24 - TEST METHOD FOR MEASUREMENT OF REVERSE RECOVERY TIME trr FOR POWER MOSFET DRAIN-SOURCE DIODES: Test method to measure the reverse recovery characteristics of the drain source diode of a power MOSFET.

August 1994; Reaffirmed October 2002 April 1999 /JC-25 Committee $41.00

JESD 24-11

ADDENDUM No. 11 to JESD24 - POWER MOSFET EQUIVALENT SERIES GATE RESISTANCE TEST METHOD: Test method to measure the equivalent resistance of the gate to source of a power MOSFET.

August 1996; Reaffirmed March 2001, October 2002 March 2001 /JC-25 Committee $38.00

JESD 24-12

THERMAL IMPEDANCE MEASUREMENT FOR INSULATED GATE BIPOLAR TRANSISTORS - (Delta VCE(on) Method) The purpose of this test method is to measure the thermal impedance of the IGBT (Insulated Gate Bipolar Transistor) under the specified conditions of applied voltage, current and pulse duration. The temperature sensitivity of the collector-emitter on voltage, VCE(on), is used as the junction temperature indicator. This is an alternative method to JEDEC Standard No. 24-6.

June 2004 September 2002 /JC-25 Committee $45.00

JESD 25

MEASUREMENT OF SMALL-SIGNAL TRANSISTOR SCATTERING PARAMETERS: This standard provides a test method and definition for small-signal conditions at microwave frequencies.

November 1972; Reaffirmed September 1981, April 2000, October 2002 /JC-25 Committee $57.00

JESD 26-A

GENERAL SPECIFICATION FOR PLASTIC ENCAPSULATED MICROCIRCUITS FOR USE IN RUGGED APPLICATIONS - RESCINDED, July 2001

April 1990; Rescinded July 2001 /JC-13.2 Subcommittee

JESD 27

CERAMIC PACKAGE SPECIFICATION FOR MICROELECTRONIC PACKAGES: The intent of this standard is to be a guide in the manufacture and procurement of ceramic packages, especially for the hybrid industry. Manufacturers or ceramic packages and procuring activities for these packages will now be able to use this document as the means for agreement in the imposition of minimum requirements in qualification, screening, and quality conformance.

August 1993; Under Revision , will be merged with JESD9-A /JC-13.5 Subcommittee $67.00

JESD 28-1

N-CHANNEL MOSFET HOT CARRIER DATA ANALYSIS: This addendum provides data analysis examples useful in analyzing MOSFET n-channel hot-carrier-induced degradation data. This addendum to JESD28 (Hot carrier n-channel testing standard) suggests hot-carrier data analysis techniques.

September 2001 /JC-14.2 Subcommittee $43.00

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JESD 28-A

A PROCEDURE FOR MEASURING N-CHANNEL MOSFET HOT-CARRIER-INDUCED DEGRADATION UNDER DC STRESS: This document describes an accelerated test for measuring the hot-carrier-induced degradation of a single n-channel MOSFET using dc bias. The purpose of this document is to specify a minimum set of measurements so that valid comparisons can be made between different technologies, IC processes, and process variations in a simple, consistent and controlled way. The measurements specified should be viewed as a starting point in the characterization and benchmarking of the transistor manufacturing process.

December 2001 /JC-14.2 Subcommittee $47.00

JESD 29-A

FAILURE-MECHANISM-DRIVEN RELIABILITY MONITORING - SUPERSEDED BY EIA/ANSI-659, July 1996.

July 1996; Superseded July 1996 /JC-14.3 Subcommittee

JESD 30E

DESCRIPTIVE DESIGNATION SYSTEM FOR SEMICONDUCTOR-DEVICE PACKAGES: This standard describes a systematic method for generating universal descriptive designators for semiconductor-device packages. The descriptive designator is intended to provide a useful communication tool but has no implied control for assuring package interchangeability.

August 2008 January 2008 /JC-11 Committee $69.00

JESD 31C

GENERAL REQUIREMENTS FOR DISTRIBUTORS OF COMMERCIAL AND MILITARY SEMICONDUCTOR DEVICES: This publication identifies the general requirements for Distributors that supply Commercial and Military products. This document identifies the general requirements for Distributors that supply Commercial and Military products. Now updated to provide clarification, these requirements apply to all discrete semiconductors, integrated circuits and hybrids, whether packaged or in wafer/die form, manufactured by all component Manufacturers. This revision was incorporated to better define the requirements for the handling of moisture-sensitive devices in distribution. The addition of IPC/JEDEC J-STD-020 and IPC/JEDEC J-STD-033 ensure consistent requirements throughout the distribution channel.

September 2003 January 2003 /JC-14.4 Subcommittee $52.00

JESD 32

STANDARD FOR CHAIN DESCRIPTION FILE: This document provides a standard for describing an ISP device chain, opening up the possibility for third-party companies to provide value-added ISP software. The purpose of the Chain Description File is to describe the configuration of a programming chain made up of devices that can be connected in some serial fashion. No assumptions are made about how data is used by the device, nor about the nature or configuration of the control signals that affect programming. It will support devices configured using electrically-erasable(EE), Flash, SRAM, or any other reconfigurable cell. For devices programmed via an IEEE programmable devices in the same chain.

June 1996 / Committee!33JC421 $47.00

JESD 33-B

STANDARD METHOD FOR MEASURING AND USING THE TEMPERATURE COEFFICIENT OF RESISTANCE TO DETERMINE THE TEMPERATURE OF A METALLIZATION LINE: This newly revised test method provides a procedure for measuring the temperature coefficient of resistance, TCR(T), of thin-film metallizations used in microelectronic circuits and devices. Procedures are also provided to use the TCR(T) to determine the temperature of a metallization line under Joule-heating conditions and to determine the ambient temperature where the metallization line is used as a temperature sensor. Originally, the method was intended only for aluminum-based metallizations and for other metallizations that satisfy the linear dependence and stability stipulations of the method. The method has been revised to make it explicitly applicable to copper-based metallizations, as well, and at temperatures beyond where the resistivity of copper is no longer linearly dependent on temperature (beyond approximately 200 °C). Using the TCR(T) measured for copper in the linear-dependent region, a factor is used to correct the calculated temperature at these higher temperatures.

February 2004 April 2003 /JC-14.2 Subcommittee $61.00

JESD 34

FAILURE-MECHANISM-DRIVEN RELIABILITY QUALIFICATION OF SILICON DEVICES: This document applies to the reliability qualification of new or changed silicon devices, and their materials or manufacturing processes. Does not address qualification of product quality or functionality. Provides an alternative to traditional stress-driven qualification.

March 1993; Rescinded November 2004 June 2004 /JC-14.2 Subcommittee $43.00

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JESD 35-1

ADDENDUM No. 1 to JESD35 - GENERAL GUIDELINES FOR DESIGNING TEST STRUCTURES FOR THE WAFER-LEVEL TESTING OF THIN DIELECTRICS: This addendum expands the usefulness of the Standard 35 (JESD35) by detailing the various sources of measurement error that could effect the test results obtained by the ramped tests described in JESD35. Each source of error is described and its implications on test structure design is noted. This addendum can be used as a guide when designing test structures for the qualification and characterization of thin oxide reliability, specifically, by implementing accelerated voltage or current ramp tests.

September 1995 /JC-14.2 Subcommittee $52.00

JESD 35-2

ADDENDUM No. 2 to JESD35 - TEST CRITERIA FOR THE WAFER-LEVEL TESTING OF THIN DIELECTRICS: This addendum includes test criteria to supplement JESD35. JESD35 describes procedures developed for estimating the overall integrity of thin oxides in the MOS Integrated Circuit manufacturing industry. Two test procedures are included in JESD35: a Voltage-Ramp (V-Ramp) and a Current-Ramp (J-Ramp). As JESD35 became implemented into production facilities on a variety of test structures and oxide attributes, a need arose to clarify end point determination and point out some of the obstacles that could be overcome by careful characterization of the equipment and test structures.

February 1996 /JC-14.2 Subcommittee $43.00

JESD 35-A

PROCEDURE FOR WAFER-LEVEL-TESTING OF THIN DIELECTRICS: The revised JESD35 is intended for use in the MOS Integrated Circuit manufacturing industry. It describes procedures developed for estimating the overall integrity and reliability of thin gate oxides. Three basic test procedures are described, the Voltage-Ramp (V-Ramp), the Current-Ramp (J-Ramp) and the new Constant Current (Bounded J-Ramp) test. Each test is designed for simplicity, speed and ease of use. The standard has been updated to include breakdown criteria that are more robust in detecting breakdown in thinner gate oxides that may not experience hard thermal breakdown.

April 2001 /JC-14.2 Subcommittee $67.00

JESD 36

STANDARD DESCRIPTION OF LOW-VOLTAGE TTL-COMPATIBLE, 5 V TOLERANT CMOS LOGIC DEVICES: This standard outlines the standard dc specifications, test conditions, and test loading for logic products that are designed to tolerate input and output voltages which exceed the device's power supply. More specifically this standardizes 5 V - tolerant logic prducts that run from 'low voltage' (2.7 V to 3.6 V) power supplies. Products that meet this standard can be used to effectively interface between LVCMOS/LVTTL and 5 V TTL buses, bridging the gap between low-voltage and 5 V TTL busses.

June 1996 /JC-40 Committee $45.00

JESD 37

STANDARD LOGNORMAL ANALYSIS OF UNCENSORED DATA, AND OF SINGLY RIGHT -CENSORED DATA UTILIZING THE PERSSON AND ROOTZEN METHOD: This standard details techniques for estimating the values of a two parameter lognormal distribution from complete lifetime data (all samples in an experiment have failed) or singly right-censored lifetime data (the experiment have failed) or singly right-censored lifetime data gathered from rapid stress test; however, not all types of failure data can be analyzed with these techniques.

October 1992 /JC-14.2 Subcommittee $59.00

JESD 38

STANDARD FOR FAILURE ANALYSIS REPORT FORMAT: This standard is to promote unification of content and format of semiconductor device failure-analysis reports so that reports from diverse laboratories may be easily read, compared, and understood by customers. Additional objectives are to ensure that reports can be easily ready by users, satisfactorily reproduced on copying machines, adequately transmitted by telefax, and conveniently stored in standard filing cabinets.

December 1995 /JC-14.6 Subcommittee $43.00

JESD 39-A

QUALITY SYSTEM ASSESSMENT - SUPERSEDED BY ANSI/EIA-670, June 1997.

June 1997; Superseded /JC-14.4 Subcommittee

JESD 40

PROCUREMENT QUALITY OF SOLID STATE COMPONENTS BY GOVERNMENT CONTRACTORS - SUPERSEDED BY EIA-623, July 1994

July 1994; Superseded /JC-13 Committee

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JESD 41 **REVERSE RECOVERY CHARACTERISTICS OF SILICON DIODES: Rescinded June 2002.**

May 1995; Rescinded June 2002 /JC-22.1 Subcommittee

JESD 42 **REQUIREMENTS FOR HANDLING ELECTROSTATIC-DISCHARGE-SENSITIVE (ESDS) DEVICES - SUPERSEDED BY EIA-625, November 1994.**

March 1994; Superseded /JC-13 Committee

JESD 43 **COMPONENT PROBLEM ANALYSIS AND CORRECTIVE ACTION REQUIREMENTS - SUPERSEDED BY EIA-671, November 1996.**

November 1996; Superseded /JC-14.4 Subcommittee

JESD 45 **MEASUREMENT METHOD FOR THERMAL RESISTANCE OF BRIDGE RECTIFIER ASSEMBLIES: RESCINDED, June 2002. Replaced by JESD282-B.**

December 1994; Rescinded June 2002 June 2002 /JC-22.2 Subcommittee

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JESD 46C **CUSTOMER NOTIFICATION OF PRODUCT/PROCESS CHANGES BY SEMICONDUCTOR SUPPLIERS:** This standard establishes procedures to notify customers of semiconductor product and process changes. Requirements include: documentation; procedures for classification, notification and customer response; content; and records.Documentation of a suppliers change notification system should set clear and understandable expectations for both the originators of the change and their end customers.

October 2006 January 2006 /JC-14.4 Subcommittee $41.00

JESD 47F **STRESS-TEST-DRIVEN QUALIFICATION OF INTEGRATED CIRCUITS:** This standard describes a baseline set of acceptance tests for use in qualifying electronic components as new products, a product family, or as products in a process which is being changed.

December 2007 June 2007 /JC-14.3 Subcommittee $62.00

JESD 48B **PRODUCT DISCONTINUANCE:** This standard establishes the requirements for timely customer notification of planned productdiscontinuance, which will assist customers in managing end-of-life supply, or to transition on-goingrequirements to alternate products.

May 2005 January 2005 /JC-14.4 Subcommittee $40.00

JESD 49A **PROCUREMENT STANDARD FOR KNOWN GOOD DIE (KGD):** This standard was created to facilitate the procurement and use of high reliability semiconductor microcircuits or discrete devices provided in bare die form, commonly known as Known Good Die (KGD).

September 2005 January 2005 /JC-13 Committee $48.00

JESD 50B.01 **SPECIAL REQUIREMENTS FOR MAVERICK PRODUCT ELIMINATION AND OUTLIER MANAGEMENT** This standard applies to the identification and control of Maverick Product that can occur during fabrication, assembly, packaging, or test of any electronic component. It can be implemented for an entire product line or to segregate product that has a higher probability of adversely impacting quality or reliability.

November 2008 January 2008 /JC-14.3 Subcommittee $54.00

JESD 51 **METHODOLOGY FOR THE THERMAL MEASUREMENT OF COMPONENT PACKAGES (SINGLE SEMICONDUCTOR DEVICE)** This standard and its subsequent addendum's, provides a standard for thermal measurement that, if followed fully, will provide correct and meaningful data that will allow for determination of junction temperature for specific conditions. The data can be used for package design evaluation, device characterization and reliability predictions.

December 1995 /JC-15.1 Subcommittee $40.00

JESD 51- 1 **INTEGRATED CIRCUIT THERMAL MEASUREMENT METHOD - ELECTRICAL TEST METHOD (SINGLE SEMICONDUCTOR DEVICE):** The purpose of this test method is to define a standard Electrical Test Method (ETM) that can be used to determine the thermal characteristics of single integrated circuit devices housed in some form of electrical package. This method will provide a basis for comparison of different devices housed in the same electronic package or similar devices housed in different electronic packages.

December 1995 /JC-15.1 Subcommittee $61.00

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JESD 51- 2A

INTEGRATED CIRCUITS THERMAL TEST METHOD ENVIRONMENTAL CONDITIONS - NATURAL CONVECTION (STILL AIR): This document outlines the environmental conditions necessary to ensure accuracy and repeatability for a standard junction-to-ambient thermal resistance measurement in natural convection.

January 2007 March 2007 /JC-15.1 Subcommittee $57.00

JESD 51- 3

LOW EFFECTIVE THERMAL CONDUCTIVITY TEST BOARD FOR LEADED SURFACE MOUNT PACKAGES: This standard describes design requirements for a single layer, leaded surface mount integrated circuit package thermal test board. The standard describes board material and geometry requirements, minimum trace lenghts, trace thickness, and routing considerations. Application includes still air and moving air thermal tests.

August 1996 /JC-15.1 Subcommittee $41.00

JESD 51- 4

THERMAL TEST CHIP GUIDELINE (WIRE BOND TYPE CHIP): This guideline describes design requirements for wire bond type semiconductor chips to be used for thermal resistance listing of IC packages. This document provides specific guidelines for chip design but allows flexibility in the materials and layout requirements.

February 1997 /JC-15.1 Subcommittee $45.00

JESD 51- 5

EXTENSION OF THERMAL TEST BOARD STANDARDS FOR PACKAGES WITH DIRECT THERMAL ATTACHMENT MECHANISMS: This extension of the thermal standards provides a standard fixture for direct attach type packages such as deep-downset of thermally tabbed packages. This specification provides additional design detail for use in developing thermal test boards with application to these package types. This document is in addition to and not replacement for the design specifications in other standards.

February 1999 /JC-15.1 Subcommittee $38.00

JESD 51- 6

INTEGRATED CIRCUIT THERMAL TEST METHOD ENVIRONMENTAL CONDITIONS - FORCED CONVECTION (MOVING AIR): This standard specifies the environmental conditions for determining thermal performance of an integrated circuit device in a forced convection environment when mounted on a standard thermal test board.

March 1999 /JC-15.1 Subcommittee $38.00

JESD 51- 7

HIGH EFFECTIVE THERMAL CONDUCTIVITY TEST BOARD FOR LEADED SURFACE MOUNT PACKAGES: This fixturing further defines the environment for thermal test of packaged microelectronic devices. Its function is to provide an alternate mounting surface for the analysis of heat flow in electronic components. The objective of the standard is to provide a high effective thermal conductivity mounting surface that can be compared equally against standard tests done in different laboratories with typical variations of less than or equal to 10%.

February 1999 /JC-15.1 Subcommittee $41.00

JESD 51- 8

INTEGRATED CIRCUIT THERMAL TEST METHOD ENVIRONMENTAL CONDITIONS - JUNCTION-TO-BOARD: This specification should be used in conjunction with the overview document JESD51, Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Device) [1] and the electrical test procedures described in JESD51-1, 'Integrated Circuit Thermal Measurement Method (Single Semiconductor Device' [2. The environmental conditions described in this document are specifically designed for testing of integrated circuit devices that are mounted on standard test boards with two internal copper planes [3]. This standard is not applicable to packages that have asymmetric heat flow paths to the printed board caused by such thermal enhancements as fused leads (leads connected to the die pad) or power style packages with the exposed heat slug on one side of the package.

October 1999 /JC-15.1 Subcommittee $45.00

JESD 51- 9

TEST BOARDS FOR AREA ARRAY SURFACE MOUNT PACKAGE THERMAL MEASUREMENTS: This standard covers the design of printed circuit boards (PCBs) used in the thermal characterization of ball grid array (BGA) and land grid array (LGA) packages. It is intended to be used in conjunction with the JESD51 series of standards that cover the test methods and test environments. JESD51-9 was developed to give a figure-of-merit of thermal performance that allows for accurate comparisons of packages from different suppliers. It can be used to give a first order approximation of system performance and, in conjunction

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with the other JESD51 PCB standards, allows for comparisons of the various package families.

July 2000 /JC-15.1 Subcommittee $48.00

JESD 51-10 **TEST BOARDS FOR THROUGH-HOLE PERIMETER LEADED PACKAGE THERMAL MEASUREMENTS:** This standard covers the design of printed circuit boards (PCBs) used in the thermal characterization of Dual-Inline Packages (DIP) and Single-Inline Packages (SIP). It is intended to be used in conjunction with the JESD51 series of standards that cover the test methods and test environments. JESD51-10 was developed to give a figure-of-merit of thermal performance that allows for accurate comparisons of packages from different suppliers. It can be used to give a first order approximation of system performance and, in conjunction with the other JESD51 PCB standards, allows for comparisons of the various package families.

July 2000 /JC-15.1 Subcommittee $45.00

JESD 51-11 **TEST BOARDS FOR THROUGH-HOLE AREA ARRAY LEADED PACKAGE THERMAL MEASUREMENT:** This standard covers the design of printed circuit boards (PCBs) used in the thermal characterization of Pin Grid Array (PGA) packages. It is intended to be used in conjunction with the JESD51 series of standards that cover the test methods and test environments. JESD51-11 was developed to give a figure-of-merit of thermal performance that allows for accurate comparisons of packages from different suppliers. It can be used to give a first order approximation of system performance and, in conjunction with the other JESD51 PCB standards, allows for comparisons of the various package families.

June 2001 /JC-15.1 Subcommittee $47.00

JESD 51-31 **THERMAL TEST ENVIRONMENT MODIFICATIONS FOR MULTICHIP PACKAGES** This document specifies the appropriate modifications needed for Multi-Chip Packages to the thermal test environmental conditions specified in the JESD51 series of specifications. The data obtained from methods of this document are the raw data used to document the thermal performance of the package. The use of this data will be documented in JESD51-XX, Guideline to Support Effective Use of MCP Thermal Measurements which is being prepared.

July 2008 November 2007 /JC-15 Committee $54.00

JESD 52 **STANDARD FOR DESCRIPTION OF LOW VOLTAGE TTL-COMPATIBLE CMOS LOGIC DEVICES:** This standard describes dc interface specifications and test environment for these devices that operate with 2.7 V to 3.6 V power supplies. The goal is to provide a consistent set of dc specifications for reference by logic suppliers and users alike.

November 1995 /JC-40 Committee $45.00

JESD 53 **MANAGEMENT OF COMPONENT OBSOLESCENCE BY GOVERNMENT CONTRACTORS: RESCINDED, October 2002**

January 1996; Rescinded October 2002 October 2002 /JC-13.2 Subcommittee

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JESD 54 **STANDARD FOR DESCRIPTION OF 54/74ABTXXX AND 74BCXXX TTL-COMPATIBLE BiCMOS LOGIC DEVICES:** The purpose is to provide a standard of BiCMOS Logic series specifications to provide for uniformity, multiplicity of sources, elimination of confusion, and ease of device specification and design by users.

February 1996 /JC-40 Committee $61.00

JESD 55 **STANDARD FOR DESCRIPTION OF LOW-VOLTAGE TTL-COMPATIBLE BiCMOS LOGIC DEVICES:** The purpose is to provide a standard of BiCMOS Logic series specifications for uniformity, multiplicity of sources, elimination of confusion, and ease of device specification and design by users.

May 1996 /JC-40 Committee $49.00

JESD 57 **TEST PROCEDURE FOR THE MANAGEMENT OF SINGLE-EVENT EFFECTS IN SEMICONDUCTOR DEVICES FROM HEAVY ION IRRADIATION:** This test method defines requirements and procedures for ground simulation and single event effects (SEE) and implementation of the method in testing integrated circuits. This standard is valid when using a cyclotron or Van de Graaff accelerator. Microcircuits under test must be delidded. The ions used at the facilities have an atomic number Z > 2. It does not apply to SEE testing that uses protons, neutrons, or other lighter particles. This standard is designed to eliminate any

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misunderstanding between users of the method and test facilities, to minimize delays, and to promote standardization of testing and test data.

December 1996; Under Revision September 2003 /JC-13.4 Subcommittee $67.00

JESD 59

BOND WIRE MODELING STANDARD: This standard describes the modeling of a bond wire from an integrated circuit (IC) die to a package lead in a ball or wedge type wire bond configuration.

June 1997 /JC-15.2 Subcommittee $45.00

JESD 60A

A PROCEDURE FOR MEASURING P-CHANNEL MOSFET HOT-CARRIER-INDUCED DEGRADATION AT MAXIMUM GATE CURRENT UNDER DC STRESS: This method establishes a standard procedure for accelerated testing of the hot-carrier-induced change of a p-channel MOSFET. The objective is to provide a minimum set of measurements so that accurate comparisons can be made between different technologies. The measurements specified should be viewed as a starting pint in the characterization and benchmarking of the trasistor manufacturing process.

September 2004 August 2002 /JC-14.2 Subcommittee $52.00

JESD 61A.01

ISOTHERMAL ELECTROMIGRATION TEST PROCEDURE: This standard describes an algorithm for the execution of the isothermal test, using computer-controlled instrumentation. The primary use of this test is for the monitoring of microelectronic metallization lines at wafer level (1) in process development, to evaluate process options, (2) in manufacturing, to monitor metallization reliability and (3) to monitor/evaluate process equipment. While it is developed as a fast WLR test, it can also be an effective tool for complementing the reliability data obtained through the standard package level electromigration test.

October 2007 June 2006 /JC-14.2 Subcommittee $67.00

JESD 62-A

OUTLIER IDENTIFICATION AND MANAGEMENT SYSTEM FOR ELECTRONIC COMPONENTS: This revision incorporates recommended tests and an example of a statistics-based method for identifying and removing outliers, i.e., parts that meet supplier specifications and end-user requirements but lie outside typical distribution limits. Outlier product can occur during fabrication, assembly, packaging, or test of any electronic components.

May 2002 /JC-14.3 Subcommittee $45.00

JESD 63

STANDARD METHOD FOR CALCULATING THE ELECTROMIGRATION MODEL PARAMETERS FOR CURRENT DENSITY AND TEMPERATURE: This method provides procedures to calculate sample estimates and their confidence intervals for the electromigration model parameters of current density and temperature. The model parameter for current density is the exponent (n) to which the current density is raised in Black's equation. The parameter for temperature is the activation energy for the electromigration failure process.

February 1998 /JC-14.2 Subcommittee $61.00

JESD 64-A

STANDARD FOR DESCRIPTION OF 2.5 V CMOS LOGIC DEVICES WITH 3.6 V CMOS TOLERANT INPUTS AND OUTPUTS: The purpose is to provide a standard for 2.5 V nominal supply voltage logic devices for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use. This specification provides for compatibility between devices operating between either the Standard Range of 1.8 V to 2.7 V or the optional Extended Range of 1.65 V to 2.7 V supply voltages, as well as over-voltage tolerance with devices operating at 3.6 V.

October 2000 /JC-40 Committee $40.00

JESD 65B

DEFINITION OF SKEW SPECIFICATIONS FOR STANDARD LOGIC DEVICES: This standard defines skew specifications and skew testing for standard logic devices. The purpose is to provide a standard for specifications to achieve uniformity, multiplicity of sources, elimination of confusion, and ease of device specification and design by users.

September 2003 /JC-40 Committee $48.00

JESD 66

TRANSIENT VOLTAGE SUPPRESSOR STANDARD FOR THYRISTOR SURGE PROTECTIVE DEVICE: This standard is applicable to Thyristor Surge Protective Devices. It describes terms and definitions and explains methods for verifying device ratings and measuring device characteristics. The intended users of this standard are those interested in Thyristor Surge Protective Device characterization and rating verification. These devices are used primarily by the telecommunications industry to protect circuits from harmful overvoltages. The

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Thyristor Surge Protective Device (TSPD) is a semiconductor device that is finding widespread application in the telecommunication industry. The intent of this stand is to provide information on test methods that will reduce the possibility of disagreement and misunderstanding between TSPD vendors and users, and facilitate the determination of device interchangeability.

November 1999 /JC-22.5 Subcommittee $91.00

JESD 67

I/O DRIVERS AND RECEIVERS WITH CONFIGURABLE COMMUNICATION VOLTAGE, IMPEDANCE, AND RECEIVER THRESHOLD: This standard attempts to aid in the design of electronic systems comprised of components that operate at several different supply voltages. This document covers respectively configurable I/O voltage, receiver type and switchpoint, and driver impedance.

February 1999 /JC-16 Committee $45.00

JESD 68.01

COMMON FLASH INTERFACE (CFI): The Common Flash Interface (CFI) specification outlines a device and host system software interrogation handshake that allows specific software algorithms to be used for entire families of devices. This allows device-independent, JEDEC ID-independent, and forward- and backward-compatible software support for the specific flash families. It allows flash vendors to standardize their existing interfaces for long-term compatibility. The changes for this minor revision are indicated in Annex A on page 11.

September 2003 December 2002 /JC-42.4 Subcommittee $48.00

JESD 69B

INFORMATION REQUIREMENTS FOR THE QUALIFICATION OF SILICON DEVICES: This standard establishes the information required by semiconductor users from IC manufacturers and distributors in order to judge whether a semiconductor component is fit for use in their particular application. It establishes a set of data elements that describes the component and defines what each element means. It does not define the quality and reliability requirements that the component must satisfy. This standard can be used in conjunction with other reliability qualification standards, such as JESD34 'Failure Mechanism-Driven Reliability Qualification of Silicon Devices' and JESD47 'Stress Test Driven Qualification of Integrated Circuits'.

October 2007 June 2007 /JC-14.3 Subcommittee $50.00

JESD 70

2.5 V BiCMOS LOGIC DEVICE FAMILY SPECIFICATION WITH 5 V TOLERANT INPUTS AND OUTPUTS: The purpose is to provide a standard for 2.5 V nominal supply voltage logic devices, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use, thus providing compatibility between devices operating between 2.3 V and 2.7 V supply voltages, as well as overvoltage tolerance with devices operating at 3.3 V, or 5 V.

June 1999 /JC-40 Committee $41.00

JESD 71

STANDARD TEST AND PROGRAMMING LANGUAGE (STAPL): STAPL is a vendor- and platform-independent language for programming and testing devices via the IEEE standard 1149.1 interface, commonly known as JTAG. STAPL enables programming of designs into programmable logic devices (PLDs) offered by a variety of PLD vendors. STAPL is also suitable for testing 1149.1-compliant devices.

August 1999 / Committee!33JC421 $67.00

JESD 72

TEST METHODS AND ACCEPTANCE PROCEDURES FOR THE EVALUATION OF POLYMERIC MATERIALS: This Test Method covers the minimum requirements that should be in effect for the evaluation and acceptance of polymeric materials for use in industrial, military, space, and other special-condition products which may require capabilities beyond standard commercial microelectronics applications. It is not the intent of this Publication to specify a material, but to evaluate the material to assure that the quality and reliability of the microelectronic devices are not compromised. This document replaces JEP105, JEP107 and JEP112.

June 2001; Reaffirmed January 2007 January 2001 /JC-13.5 Subcommittee $52.00

JESD 73

DESCRIPTION OF 5 V BUS SWITCH WITH TTL-COMPATIBLE CONTROL INPUTS: This standard covers specifications for a family of 5 V NMOS FET bus switch devices with 5 V TTL compatible control inputs. Not included in this document are device-specific parameters and performance levels that the vendor must also apply for full device description.

June 1999 /JC-40 Committee $40.00

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JESD 73-1

STANDARD FOR DESCRIPTION OF 3.3 V NFET BUS SWITCH DEVICES: This standard covers specifications for a family of 3.3 V NMOS FET bus switch devices. Not included in this document are device specific parameters and performance levels that the vendor must also supply for full device description. The purpose of this document is to provide a set of uniform data sheet parameters for the description of bus switch devices. This standard includes required parameters, test conditions, test levels, and measurement methods for data sheet descriptions of bus switch devices.

August 2001 /JC-40 Committee $40.00

JESD 73-2

STANDARD FOR DESCRIPTION OF 3.3 V NFET BUS SWITCH DEVICES WITH INTEGRATED CHARGE PUMPS: This standard covers specifications for a family of 3.3 V NMOS FET bus switch devices with integrated charge pumps. Not included in this document are device specific parameters and performance levels that the vendor must also supply for full device description. The purpose of this standard is to provide a set of uniform data sheet parameters for the description of bus switch devices. This standard includes required parameters, test conditions, test levels, and measurement methods for data sheet descriptions of bus switch devices.

August 2001 /JC-40 Committee $40.00

JESD 73-3

STANDARD FOR DESCRIPTION OF 3867 - 2.5 V, SINGLE 10-BIT, 2-PORT, DDR FET SWITCH: This standard provides a set of uniform data sheet parameters for the description of a single 10-bit, 2.5 V FET transmission-gate bus switch device for DDR memory module and motherboard applications. This bus switch device has a low ON resistance allowing inputs to be connected directly to outputs, with near zero propagation delay.

November 2001 / Committee!33JC402 $40.00

JESD 73-4

STANDARD FOR DESCRIPTION OF 3877 - 2.5 V, DUAL 5-BIT, 2-PORT, DDR FET SWITCH: This standard provides a set of uniform data sheet parameters for the description of a dual 5-bit, 2.5 V FET transmission-gate bus switch device for DDR memory module and motherboard applications. This bus switch device has a low ON resistance allowing inputs to be connected directly to outputs, with near zero propagation delay.

November 2001 / Committee!33JC402 $40.00

JESD 74A

EARLY LIFE FAILURE RATE CALCULATION PROCEDURE FOR SEMICONDUCTOR COMPONENTS: This standard defines methods for calculating the early life failure rate of a product, using accelerated testing, whose failure rate is constant or decreasing over time. For technologies where there is adequate field failure data, alternative methods may be used to establish the early life failure rate. The purpose of this standard is to define a procedure for performing measurement and calculation of early life failure rates. Projections can be used to compare reliability performance with objectives, provide line feedback, support service cost estimates, and set product test and screen strategies to ensure that the ELFR meets customers' requirements.

February 2007 September 2006 /JC-14.3 Subcommittee $61.00

JESD 75

BALL GRID ARRAY PINOUTS STANDARDIZED FOR 32-BIT LOGIC FUNCTIONS: The purpose of this standard is to provide a pinout standard for dual-die 32-bit logic devices offered in a 96- and 144-ball grid array package for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease use. This standard defines device output for 32-bit wide buffer, driver and transceiver functions. This pinout specifically applies to the conversion of DIP-packaged 16-bit logic devices to LFBGA-packaged dual-die 32-bit logic devices.

November 1999 /JC-40 Committee $38.00

JESD 75-1

BALL GRID ARRAY PINOUTS STANDARDIZED FOR 16, 18, AND 20-BIT LOGIC FUNCTIONS USING A 54 BALL PACKAGE: This standard establishes a 54 Ball Grid Array pinout for 16, 18 and 20-bit standard logic devices that are currently being produced in 48 and 56 Pin SSOP and TSSOP packages. The 54 Ball Grid Array Package is organized as a 6 x 9 array with balls on a .8mm x .8mm grid pitch.

October 2001 /JC-40 Committee $38.00

JESD 75-2

BALL GRID ARRAY PINOUTS STANDARDIZED FOR 16-BIT LOGIC FUNCTIONS: This standard provides a pinout standard for 16-bit wide logic devices offered in a 56-ball areagrid array

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package to provide for uniformity, multiplicity of sources, elimination of confusion,ease of device specification, and ease of use.

July 2001 /JC-40 Committee $38.00

JESD 75-3

BALL GRID ARRAY PINOUTS STANDARDIZED FOR 8-BIT LOGIC FUNCTIONS: This standard provides a pinout standard for 8-bit logic devices offered in a 20-ball area gridarray package to provide for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

July 2001 /JC-40 Committee $37.00

JESD 75-4

BALL GRID ARRAY PINOUT FOR 1-, 2-, AND 3-BIT LOGIC FUNCTIONS: This standard defines device pinout for 1-, 2- and 3-bit wide logic functions. This pinout specifically applies to the conversion of Dual-Inline-Packaged (DIP) 1-, 2- and 3-bit logic devices to DSBGA-packaged 1-, 2- and 3-bit logic devices.

March 2004 June 2003 /JC-40 Committee $41.00

JESD 75-5

SON/QFN PACKAGE PINOUTS STANDARDIZED FOR 1-, 2-, AND 3-BIT LOGIC FUNCTIONS
This standard defines device pinout for 1-, 2- and 3-bit wide logic functions. This pinout specifically applies to the conversion of Dual-Inline-Packaged (DIP) 1-, 2- and 3-bit logic devices to SON/QFN packaged 1-, 2- and 3-bit logic devices. The purpose of this document is to provide a pinout standard for 1-, 2- and 3-bit logic devices offered in 5-, 6- or 8-land SON/QFN packages for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

July 2004 December 2003 /JC-40.1 Subcommittee $41.00

JESD 75-6

PSO-N/PQFN PINOUTS STANDARDIZED FOR 14-, 16-, 20-, AND 24-LEAD LOGIC FUNCTIONS: This standard defines device pinouts for 14-, 16-, 20-, and 24-lead logic functions. This pinout standard specifically applies to the conversion of DIP-packaged logic devices to PSO-N/PQFN packages logic devices. The purpose of this standard is to provide a pinout standard for 14-, 16-, 20-, and 24-lead logic devices offered in 14-, 16-, 20-, and 24-lead PSO-N/PQFN packages for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

March 2006 September 2005 /JC-40.1 Subcommittee $41.00

JESD 76

DESCRIPTION OF 1.8 V CMOS LOGIC DEVICES: This standard continues the voltage specification migration to the next level beyond the 2.5 V specification already established in JESD80. In this standard, the input and output conditions are described for CMOS Logic products in a 1.8 V (Normal Range) application.

April 2000 /JC-40.1 Subcommittee $38.00

JESD 76-1

STANDARD DESCRIPTION OF 1.2 V CMOS LOGIC DEVICES (WIDE RANGE OPERATION): This standard defines dc interface, switching parameters and test loading for digital logic devices based on 1.2 V (nominal) power supply levels. The purpose is to provide a standard specification for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

June 2001 /JC-40 Committee $38.00

JESD 76-2

STANDARD DESCRIPTION OF 1.2 V CMOS LOGIC DEVICES (NORMAL RANGE OPERATION):
This standard defines dc interface, switching parameters and test loading for digital logic devices based on 1.2 V (normal range) power supply levels. The purpose is to provide a standard specification for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

June 2001 /JC-40 Committee $38.00

JESD 76-3

STANDARD DESCRIPTION OF 1.5 V CMOS LOGIC DEVICES: This standard continues the voltage specification migration to the next level beyond the 1.8 V specification already established. The purpose is to provide a standard for 1.5 V nominal supply voltage CMOS logic devices, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

August 2001 /JC-40.1 Subcommittee $38.00

JESD 77B.01

TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR DISCRETE SEMICONDUCTOR AND OPTOELECTRONIC DEVICES: A revised and significantly expanded reference for technical

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writers and educators, manufacturers, buyers and users of discrete semiconductor and optoelectronic devices, is now available. Revision B of JEDEC Standard No. 77 includes extensive information on: letter symbol conventions; diodes and rectifiers (including signal, rectifier, microwave, tunnel and backward, voltage-regulator, voltage-reference, current regulator, and varactor diodes); transistors (including FETs, JFETs, and IGBTs); photosensitive devices, photoemitters, and optocouplers; thyristors and PUTs; and transient voltage suppressors. Terms and symbols, with their definitions, are arranged alphabetically by product type. Where applicable, graphical symbols are also included.

July 2006 /JC-10 Committee $162.00

JESD 78A

IC LATCH-UP TEST: This standard has been adopted by the Defense Logistics Agency (DLA) as project 5962-1880. This standard establishes a defined method for latch-up testing of ICs. It defines Classes and Levels for a device's latch-up capability so that both the user and supplier understand a device's latch-up capabilities. It is applicable to NMOS, CMOS, Bipolar, and all variations and combinations of these technologies. Latch-up is an extremely important factor in determining product reliability. This document contains the corrected figure 4 to include T6 on page 12, this change was made in January 1998.

February 2006 January 2005 /JC-14.1 Subcommittee $55.00

JESD 79-2E

DDR2 SDRAM SPECIFICATION This comprehensive standard defines all required aspects of 256Mb through 4Gb DDR2 SDRAMs with x4/x8/x16 data interfaces, including pinout, addressing, functional description, features, ac and dc parametrics, truth tables, and packages. Standard JESD79-2 uses a SSTL_18 interface, which is described in another JEDEC standard called JESD8-15. The purpose of this Standard is to define the minimum set of requirements for compliant devices 256Mb through 4Gb, x4/x8/x16 DDR2 SDRAMs. System designs based on the required aspects of this specification will be supported by all DDR2 SDRAM vendors providing compliant devices. Changes between versions is indicated in Annex A.

April 2008 June 2007 /JC-42.3 Subcommittee $177.00

JESD 79-3C

DDR3 SDRAM STANDARD This document defines the DDR3 SDRAM specification, including features, functionalities, AC and DC characteristics, packages, and ball/signal assignments. The purpose of this Specification is to define the minimum set of requirements for JEDEC compliant 512 Mb through 8 Gb for x4, x8, and x16 DDR3 SDRAM devices. This specification was created based on the DDR2 specification (JESD79-2) and some aspects of the DDR specification (JESD79). Each aspect of the changes for DDR3 SDRAM operation were considered and approved by committee ballots). The accumulation of these ballots were then incorporated to prepare this JESD79-3 specification, replacing whole sections and incorporating the changes into Functional Description and Operation.

November 2008 March 2008 /JC-42.3 Subcommittee $229.00

JESD 79F

DOUBLE DATA RATE (DDR) SDRAM SPECIFICATION: This comprehensive standard defines all required aspects of 64Mb through 1Gb DDR SDRAMs with X4/X8/X16 data interfaces, including features, functionality, ac and dc parametrics, packages and pin assignments. This scope will subsequently be expanded to formally apply to x32 devices, and higher density devices as well. The purpose of this Standard is to define the minimum set of requirements for JEDEC compliant 64Mb through 1Gb, X4/X8/X16 DDR SDRAMs. System designs based on the required aspects of this specification will be supported by all DDR SDRAM vendors providing JEDEC compliant devices.

February 2008 /JC-42.3 Subcommittee $109.00

JESD 8-16A

BUS INTERCONNECT LOGIC (BIC) FOR 1.2 V This standard defines the electrical parameters for high-speed interfaces for use in the 1.2V electrical environment. Included in the standard are a single ended signaling interface suitable for parallel busses, and a differential signaling interface suitable for clock applications or parallel differential buses. JEDEC ?BIC? Standard JESD8-16A continues the tradition of the JESD8-xx standards, defining electrical interfaces for the industry as new technologies and bus requirements develop. Previously, JEDEC defined standard JESD8-6, the ?HSTL? standard, for use in 1.5V electrical environments. BIC is similar to HSTL, except the power supply voltage has dropped from 1.5V to 1.2V, and interface requirements are tightened to allow much higher speeds.

November 2004 June 2004 /JC-16 Committee $52.00

JESD 80

STANDARD FOR DESCRIPTION OF 2.5 V CMOS LOGIC DEVICES: The purpose of this

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standard is to provide a standard for 2.5 V nominal supply-voltage CMOS logic devices, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use. This standard defines dc interface parameters and test loading for CMOS digital logic family based on 2.5 V (nominal) power supply levels at 2.5 V input tolerance.

November 1999 /JC-40 Committee $38.00

JESD 82 **DEFINITION OF CDCV857 PLL CLOCK DRIVER FOR REGISTERED DDR DIMM APPLICATIONS:** This specification is a reference for Registered DDR DIMM designers. JESD82 defines the physical, electrical, interface and timing requirements of a 1:10 PLL clock driver for DDR Registered DIMMs from DDR200 to DDR266 as refined in revision C of JEDEC Standard 21-C (JESD21-C). JESD82 was also written to meet the future performance requirements of Registered DIMMs for DDR300 and DDR333.

July 2000 /JC-40 Committee $47.00

JESD 82-10A **DEFINITION OF THE SSTU32866 1.8 V CONFIGURABLE REGISTERED BUFFER WITH PARITY FOR DDR2 RDIMM APPLICATIONS** This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of the SSTU32866 registered buffer with parity test for DDR2 RDIMM applications. The purpose is to provide a standard for the SSTU32866 (see Note) logic device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

May 2007 September 2006 /JC-40.4 Subcommittee $63.00

JESD 82-11 **DEFINITION OF 'CU878 PLL CLOCK DRIVER FOR REGISTERED DDR2 DIMM APPLICATIONS** This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of a ?CU878 PLL clock device for registered DDR2 DIMM applications. The purpose is to provide a standard for a ?CU878 PLL clock device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

September 2004 February 2004 /JC-40.3 Subcommittee $48.00

JESD 82-12A **DEFINITION OF THE SSTU32S869 & SSTU32D869 REGISTERED BUFFER WITH PARITY FOR DDR2 RDIMM APPLICATIONS** This standard defines standard specifications of DC interface parameters, switching parameters, and test loading for definition of the SSTU32S869 and SSTU32D869 registered buffer with parity for driving heavy load on high-density DDR2 RDIMM applications. A typical application would be a 36 SDRAM planar DIMM. The purpose is to provide a standard for the SSTU32S869 and SSTU32D869 logic devices, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

April 2007 September 2006 /JC-40 Committee $57.00

JESD 82-13A **DEFINITION OF THE SSTVN16859 2.5-2.6 V 13-BIT TO 26-BIT SSTL_2 REGISTERED BUFFER FOR PC1600, PC2100, PC2700 AND PC3200 DDR DIMM APPLICATIONS** This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of the SSTVN16859 13-bit to 26-bit SSTL_2 registered buffer for PC1600, PC2100, PC2700 and PC3200 DDR DIMM applications. The SSTVN16859 is a speed upgrade of the SSTV16859 (JESD82-4) for use in PC3200 DDR DIMMs. It is fully backward compatible with SSTV16859 for all speed grades.

May 2005 September 2004 /JC-40 Committee $48.00

JESD 82-14A **DEFINITION OF THE SSTUB32868 1.8 V CONFIGURABLE REGISTERED BUFFER WITH PARITY FOR DDR2 RDIMM APPLICATIONS** This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of the SSTUB32868 registered buffer with parity test for DDR2 RDIMM applications. SSTU32S2868 denotes a single-die implementation and SSTU32D868 denotes a dual-die implementation.

October 2006 June 2005 /JC-40 Committee $57.00

JESD 82-15 **STANDARD FOR DEFINITION OF CUA878 PLL CLOCK DRIVER FOR REGISTERED DDR2 DIMM APPLICATIONS** This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of a CUA878 PLL clock device for registered DDR2 DIMM applications. The purpose is to provide a standard for a CUA878 PLL clock device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

November 2005 September 2004 /JC-40 Committee $49.00

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JESD 82-16A

DEFINITION OF THE SSTUA32866 1.8 V CONFIGURABLE REGISTERED BUFFER WITH PARITY TEST FOR DDR2 RDIMM APPLICATIONS This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of the SSTUA32866 registered buffer with parity test for DDR2 RDIMM applications. The purpose is to provide a standard for the SSTUA32866 (see Note) logic device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

May 2007 June 2006 /JC-40 Committee $63.00

JESD 82-17

DEFINITION OF THE SSTUA32S868 AND SSTUA32D868 REGISTERED BUFFER WITH PARITY FOR 2R X 4 DDR2 RDIMM APPLICATIONS This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of the SSTUA32S868 and SSTUA32D868 registered buffer with parity test for DDR2 RDIMM applications.

November 2005 June 2004 /JC-40.3 Subcommittee $57.00

JESD 82-18A

STANDARD FOR DEFINITION OF THE CUA877 AND CU2A877 PLL CLOCK DRIVERSFOR REGISTERED DDR2 DIMM APPLICATIONS This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of the CUA877 and CU2A877 PLL clock devices for registered DDR2 DIMM applications.The purpose is to provide a standard for the CUA877 and CU2A877 PLL clock devices, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

January 2007 June 2006 /JC-40 Committee $49.00

JESD 82-19A

DEFINITION OF THE SSTUA32S865 AND SSTUA32D865 28-BIT 1:2 REGISTERED BUFFER WITH PARITY FOR DDR2 RDIMM APPLICATIONS This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of the SSTUA32S865 and SSTUA32D865 registered buffer with parity for 2 rank by 4 or similar high-density DDR2 RDIMM applications.

May 2007 June 2006 /JC-40 Committee $55.00

JESD 82-1A

DEFINITION OF CVF857 PLL CLOCK DRIVER FOR REGISTERED PC1600, PC2100, PC2700, AND PC3200 DIMM APPLICATIONS: This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of a CV857 PLL clock device for registered PC1600, PC2100, PC2700 and PC3200 DIMM applications. The purpose is to provide a standard for a CV857 PLL clock device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

May 2004 /JC-40 Committee $52.00

JESD 82-2

STANDARD FOR DESCRIPTION OF A 3.3 V, 18-BIT, LVTTL I/O REGISTER FOR PC133 REGISTERED DIMM APPLICATIONS: This standard defines the register support devices needed for standard height and low profile registered PC133 SDRAM DIMM modules. The objective of the standard is to clearly define the functionality, pinout and electrical characteristics required for this type of SDRAM module.

July 2001 /JC-40 Committee $45.00

JESD 82-20

FBDIMM: ADVANCED MEMORY BUFFER (AMB) This document is a core specification for a Fully Buffered DIMM (FBD) memory system. This document, along with the other core specifications, must be treated as a whole. Information critical to a Advanced Memory Buffer design appears in the other specifications, with specific cross-references provided.

March 2007 March 2006 /JC-40 Committee $177.00

JESD 82-21

STANDARD FOR DEFINITION OF CUA845 PLL CLOCK DRIVER FOR REGISTERED DDR2 DIMM APPLICATIONS This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of a CUA845 PLL clock device for registered DDR2 DIMM applications.The purpose is to provide a standard for a CUA845 PLL clock device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

January 2007 March 2006 /JC-40 Committee $48.00

JESD 82-22

INSTRUMENTATION CHIP DATA SHEET FOR FBDIMM DIAGNOSTIC SENSELINES This device is a one-chip spectrum analyzer that operates in the frequency range from 1 to 2 GHz. It

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requires no external components except some filtering of the voltage supply (one inductor, one bypass capacitor). The frequency of the VCO is adjusted by an internal DAC. No PLL loop is used to lock the VCO to a reference frequency. A counter is used to determine the VCO frequency. The device has a serial I2C data interface. The device is available in a 28 pin TQFN package and is specified over the extended industrial (-40 C to +85 C) temperature range.

November 2006 March 2006 /JC-40.4 Subcommittee $47.00

JESD 82-23

DEFINITION OF the SSTUA32S869 AND SSTUA32D869 REGISTERED BUFFER WITH PARITY FOR DDR2 RDIMM APPLICATIONS This standard defines standard specifications of DC interface parameters, switching parameters, and test loading for definition of the SSTUA32S869 and SSTUA32D869 registered buffer with parity for driving heavy load on high-density DDR2 RDIMM applications. A typical application would be a 36 SDRAM planar DIMM. The SSTUA32S869 and SSTUA32D869 are identical in functionality to the SSTU32S869 and SSTU32D869 devices respectively but specify tighter timing characteristics and a higher application frequency of up to 410MHz.

May 2007 June 2006 /JC-40 Committee $59.00

JESD 82-24

DEFINITION OF the SSTUB32865 28-bit 1:2 REGISTERED BUFFER WITH PARITY FOR DDR2 RDIMM APPLICATIONS This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of the SSTUB32865 registered buffer with parity for 2 rank by 4 or similar high-density DDR2 RDIMM applications. The SSTUB32865 is identical in functionality to the SSTU32865 but specifies tighter timing characteristics and a higher application frequency of up to 410MHz.

May 2007 September 2006 /JC-40 Committee $55.00

JESD 82-25

DEFINITION OF the SSTUB32866 1.8 V CONFIGURABLE REGISTERED BUFFER WITH PARITY FOR DDR2 RDIMM APPLICATIONS This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of the SSTUB32866 registered buffer with parity test for DDR2 RDIMM applications.

May 2007 September 2006 /JC-40 Committee $63.00

JESD 82-26

DEFINITION OF THE SSTUB32868 REGISTERED BUFFER WITH PARITY FOR 2R x 4 DDR2 RDIMM APPLICATIONS This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of the SSTUB32868 registered buffer with parity test for DDR2 RDIMM applications.

May 2007 September 2006 /JC-40 Committee $57.00

JESD 82-27

DEFINITION OF THE SSTUB32869 REGISTERED BUFFER WITH PARITY FOR DDR2 RDIMM APPLICATIONS: This standard defines standard specifications of DC interface parameters, switching parameters, and test loading for definition of the SSTUB32869 registered buffer with parity for driving heavy load on high-density DDR2 RDIMM applications. A typical application would be a 36 SDRAM planar DIMM.

May 2007 September 2006 /JC-40 Committee $59.00

JESD 82-28A

FULLY BUFFERED DIMM DESIGN FOR TEST, DESIGN FOR VALIDATION (DFx) This FBDIMM DFx document covers Design for Test, Design for Manufacturing and Design for Validation (DFx) requirements and implementation guidelines for Fully Buffered DIMM technology.

July 2008 March 2006 /JC-40.5 Subcommittee $151.00

JESD 82-3B

DEFINITION OF THE SSTV16857 2.5 V, 14-BIT SSTL_2 REGISTERED BUFFER FOR DDR DIMM APPLICATIONS: This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of the SSTV16857 14-bit SSTL_2 registered buffer for DDR DIMM applications.The purpose is to provide a standard for the SSTV16857 logic device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

November 2004 December 2003 JC-40.3 $48.00

JESD 82-4B

STANDARD FOR DEFINITION OF THE SSTV16859 2.5 V, 13-BIT TO 26-BIT SSTL_2 REGISTERED BUFFER FOR STACKED DDR DIMM APPLICATIONS: This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of the SSTV16859 13-bit to 26-bit SSTL_2 registered buffer for stacked DDR DIMM applications. The purpose is to provide a standard for the SSTV16859 logic device,

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	for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use. May 2003 /JC-40 Committee	$47.00
JESD 82-5	**STANDARD FOR DESCRIPTION OF A 3.3 V, ZERO DELAY CLOCK DISTRIBUTION DEVICE COMPLIANT WITH THE JESD21-C PC133 REGISTERED DIMM SPECIFICATION** This standard defines the PLL support devices required for standard height and low profile registered PC133 SDRAM DIMM modules. The objective of the standard is to clearly define the functionality, pinout and electrical characteristics of the PLL used on JEDEC standard modules.JESD82-5 is the latest specification to be added to the JESD82 family of specifications for memory module support devices. Additional specifications are currently under development for DDR2 support devices. July 2002 /JC-40 Committee	$43.00
JESD 82-6A	**DEFINITION OF THE SSTV32852 2.5 V 24-BIT TO 48-BIT SSTL_2 REGISTERED BUFFER FOR 1U STACKED DDR DIMM APPLICATIONS:** This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of the SSTV32852 24-bit to 48-bit SSTL_2 registered buffer for stacked DDR DIMM applications. The purpose is to provide a standard for the SSTV32852 logic device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use. November 2004 December 2003 /JC-40 Committee	$47.00
JESD 82-7A	**DEFINITION OF THE SSTU32864 1.8-V CONFIGURABLE REGISTERED BUFFER FOR DDR2 RDIMM APPLICATIONS:** This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of the SSTU32864 configurable registered buffer for DDR2 RDIMM applications. The purpose is to provide a standard for the SSTU32864 logic device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use. October 2004 /JC-40.4 Subcommittee	$47.00
JESD 82-9B	**DEFINITION OF SSTU32865 REGISTERED BUFFER WITH PARITY FOR 2R x 4 DDR2 RDIMM APPLICATIONS** This standard provides the functional definition, ball-out configuration and package outline, signal definitions and input/output characteristics for a 28-bit 1:2 registered driver with parity suitable for use on DDR2 RDIMMs. The SSTU32865 integrates the functional equivalent of two SSTU32864 devices (as defined in JESD82-7) into a single device, thereby easing layout and board design constraints especially on high density RDIMMs such as dual rank, by four configurations. Moreover, the optional use of a parity function is provided for, permitting detection and reporting of parity errors across its 22 data inputs. JESD82-9 specifies a 160-pin Thin-profile, fine-pitch ball-grid array (TFBGA) package. May 2007 September 2006 /JC-40.4 Subcommittee	$52.00
JESD 84-A41	**EMBEDDED MULTIMEDIACARD (eMMC) PRODUCT STANDARD, STANDARD CAPACITY** This document provides a definition of the Embedded MultiMediaCard product, its environment, and handling. It also provides design guidelines and defines a tool box of macro functions and algorithms intended to reduce design-in costs. July 2007 If you downloaded this file prior to 8/23/07 please download again. May 2007 /JC-64 Committee	$55.00
JESD 84-A42	**EMBEDDED MULTIMEDIACARD (eMMC) PRODUCT STANDARD, HIGH CAPACITY** This document provides a definition of the Embedded MultiMediaCard product, its environment, and handling. It also provides design guidelines and defines a tool box of macro functions and algorithms intended to reduce design-in costs. July 2007 If you downloaded this file prior to 8/23/07 please download again. June 2007 /JC-64 Committee	$57.00
JESD 84-B41	**MULTIMEDIACARD (MMC) ELECTRICAL STANDARD, STANDARD CAPACITY (MMCA, 4.1)** This document provides a comprehensive definition of the MultiMediaCard, its environment, and handling. It also provides design guidelines and defines a tool box of macro functions and algorithms intended to reduce design-in costs. June 2007 June 2007 /JC-64.1 Subcommittee	$162.00

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JESD 84-B42

MULTIMEDIACARD (MMC) ELECTRICAL STANDARD, HIGH CAPACITY (MMCA, 4.2) The purpose of the specification is the definition of the eMMC, its environment and handling. It provides guidelines for systems designers. The specification also defines a tool box (a set of macro functions and algorithms) that contributes to reducing design-in costs.

July 2007 March 2007 /JC-64.1 Subcommittee $162.00

JESD 85

METHODS FOR CALCULATING FAILURE RATES IN UNITS OF FITS: This standard establishes methods for calculating failure rates in units of FITs by using data in varying degrees of detail such that results can be obtained from almost any data set. The objective is to provide a reference to the way failure rates are calculated.

July 2001 /JC-14.3 Subcommittee $55.00

JESD 86

ELECTRICAL PARAMETERS ASSESSMENT: This standard is intended to describe various methods for obtaining electrical variate data on devices currently produced on the manufacturing and testing process to be qualified. The intent is to assess the device?s capability to function within the specification parameters over time and the application environment (operating range of temperature, voltage, humidity, input/output levels, noise, power supply stability etc.).

August 2001 /JC-14.3 Subcommittee $38.00

JESD 87

STANDARD TEST STRUCTURE FOR RELIABILITY ASSESSMENT OF AlCu METALLIZATIONS WITH BARRIER MATERIALS This document describes design of test structures needed to assess the reliability of aluminum-copper, refractory metal barrier interconnect systems. This includes any metal interconnect system where a refractory metal barrier or other barrier material prevents the flow of aluminum and/or copper metal ions from moving between interconnect layers. This document is not intended to show design of test structures to assess aluminum or aluminum-copper alloy systems, without barriers to Al and Cu ion movement, nor for Cu only metal systems. Some total interconnect systems might not include barrier materials on all metal layers. The structures in this standard are designed for cases where a barrier material separates two Al or Al alloy metal layers. The purpose of this document is to describe the design of test structures needed to assess electromigration (EM) and stress-induced-void (SIV) reliability of AlCu barrier metal systems.

July 2001 /JC-14.2 Subcommittee $43.00

JESD 88C

DICTIONARY OF TERMS FOR SOLID STATE TECHNOLOGY, Fourth Edition: This reference for technical writers and educators, manufacturers, and buyers and users of discrete solid state devices is now available. It should aid the technical committees of JEDEC in the avoidance of multiple definitions and reduce the proliferation of redundant definitions. The long-term goal is to include definitions from all JEDEC publications and standards. Even in this fourth edition, that goal has been largely met. Each of the approximately two thousand entries is referenced to its source publication, and an annex listing the names of the source publications and their releases dates is included. All entries were reviewed for punctuation, grammar, and clarity, as well as accuracy, and reworded if such was considered warranted. The purpose of this dictionary is to promote the uniform use of terms, definitions, abbreviations, and symbols throughout the solid state industry.

July 2007 /JC-10 Committee $150.00

JESD 89-1A

TEST METHOD FOR REAL-TIME SOFT ERROR RATE: This test is used to determine the Soft Error Rate (SER) of solid state volatile memory arrays and bistable logic elements (e.g. flip-flops) for errors which require no more than re-reading or re-writing to correct and as used in terrestrial environments. It simulates the operating condition of the device and is used for qualification, characterization, or reliability monitoring. This test is intended for execution in ambient conditions without the artificial introduction of radiation sources.

October 2007 February 2007 /JC-14.1 Subcommittee $52.00

JESD 89-2A

TEST METHOD FOR ALPHA SOURCE ACCELERATED SOFT ERROR RATE: This test method is offered as standardized procedure to determine the alpha particle Soft Error Rate (SER) sensitivity of solid state volatile memory arrays and bistable logic elements (e.g. flipflops) by measuring the error rate while the device is irradiated by a characterized, solid alpha source.

October 2007 February 2007 /JC-14.1 Subcommittee $55.00

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JESD 89-3A

TEST METHOD FOR BEAM ACCELERATED SOFT ERROR RATE This test is used to determine the terrestrial cosmic ray Soft Error Rate (SER) sensitivity of solid state volatile memory arrays and bistable logic elements (e.g. flip-flops) by measuring the error rate while the device is irradiated in a neutron or proton beam of known flux. The results of this accelerated test can be used to estimate the terrestrial cosmic ray induced SER for a given terrestrial cosmic ray radiation environment. This test cannot be used to project alpha-particleinduced SER.

November 2007 January 2007 /JC-14.1 Subcommittee $66.00

JESD 89A

MEASUREMENT AND REPORTING OF ALPHA PARTICLE AND TERRESTRIAL COSMIC RAY INDUCED SOFT ERRORS IN SEMICONDUCTOR DEVICES: This specification defines the standard requirements and procedures for terrestrial soft-error-rate (SER)testing of integrated circuits and reporting of results. Both real-time (unaccelerated) and acceleratedtesting procedures are described. At terrestrial, Earth-based altitudes, the predominant sources of radiation include both cosmic-ray radiation and alpha-particle radiation from radioisotopic impurities in the package and chip materials. An overall assessment of a device?s SER is complete, only when an unaccelerated test is done, or accelerated SER data for the alpha-particle component and the cosmic-radiation component has been obtained.

October 2006 January 2006 /JC-13.4 Subcommittee $109.00

JESD 90

A PROCEDURE FOR MEASURING P-CHANNEL MOSFET NEGATIVE BIAS TEMPERATURE INSTABILITIES This document describes an accelerated stress and test methodology for measuring device parameter changes of a single p-channel MOSFET after Negative Bias Temperature Instability (NBTI) stress at dc bias conditions. This document gives a procedure to investigate NBTI stress in a symmetric voltage condition with the channel inverted (VGS < 0) and no channel conduction (VDS = 0).There can be NBTI degradation during channel conduction (VGS < 0, VDS < 0), however, this document does not cover this phenomena.

November 2004 August 2002 /JC-14.2 Subcommittee $48.00

JESD 91-A

METHOD FOR DEVELOPING ACCELERATION MODELS FOR ELECTRONIC COMPONENT FAILURE MECHANISMS: The method described in this document applies to all reliability mechanisms associated with electronic components.The purpose of this standard is to provide a reference for developing acceleration models for defect-related and wear-out mechanisms in electronic components.

August 2003 /JC-14.3 Subcommittee $49.00

JESD 92

PROCEDURE FOR CHARACTERIZING TIME-DEPENDENT DIELECTRIC BREAKDOWN OF ULTRA-THIN GATE DIELECTRICS: This document defines a constant voltage stress test procedure for characterizing time-dependent dielectric breakdown or ?wear-out? of thin gate dielectrics used in integrated circuit technologies. The test is designed to obtain voltage and temperature acceleration parameters required to estimate oxide life at use conditions. The test procedure includes sophisticated techniques to detect breakdown in ultra-thin films that typically exhibit large tunneling currents and soft or noisy breakdown characteristics. This document includes an annex that discusses test structure design, methods to determine the oxide electric field in ultra-thin films, statistical models, extrapolation models, and example failure-rate calculations.

August 2003 July 2002 /JC-14.2 Subcommittee $57.00

JESD 94A

APPLICATION SPECIFIC QUALIFICATION USING KNOWLEDGE BASED TEST METHODOLOGY: The method described in this document applies to all application specific reliability testing for solid state components with known failure mechanisms where the test duration and conditions vary based on application variables. This document does not cover reliability tests that are characterization based or essentially go / no-go type tests, for example, ESD, latch-up, or electrical over stress. Also, it does not attempt to cover every failure mechanism or test environment, but does provide a methodology that can be extended to other failure mechanisms and test environments.

July 2008 January 2008 /JC-14.3 Subcommittee $62.00

JESD 95-1

DESIGN REQUIRMENTS FOR OUTLINES OF SOLID STATE AND RELATED PRODUCTS: DISCONTINUED AS A SEPARATE ITEM CONTAINED IN JEP95, BOOK 1, SECTION 4.

September 2000; Incorporated /JC-11 Committee

JESD 96A

RADIO FRONT END - BASEBAND (RF-BB) INTERFACE The normative information in this

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standard is intended to provide a technical design team to construct the interface on a FED and a BED such that they will operate correctly with each other (at the interface level), when designed to this specification. Additional informative information is provided in the appendices to help illustrate the normative material. This document addresses the following interface topics: 1) RF-BB Electrical layer: time and amplitude specifications for lines, drivers, receivers, clocks; 2)RF-BB Link layer: bits, clock-data synchronization, power modes; 3) RF-BB Transport layer: data types, data framing, data bandwidth, connection to core IC; 4) RF-BB Interface Registers. This document defines a high-speed serial link that enables the bi-directional transfer of data and control information between the FED and BED. The document does not mandate the use of specific signaling, standard framing or standard messaging needed to make this an interoperable interface standard for RF devices or BB devices.

February 2006 February 2005 /JC-61 Committee $71.00

JESD 97

MARKING, SYMBOLS, AND LABELS FOR IDENTIFICATION OF LEAD (Pb) FREE ASSEMBLIES, COMPONENTS, AND DEVICES - SUPERSEDED BY J-STD-609, August 2007

May 2004; Superseded by J-STD-609, August 2007 June 2003 /JC-14.1 Subcommittee $45.00

JESD 99-1

ADDENDUM No. 1 to JESD99 - TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR ANALOG-TO-DIGITAL AND DIGITAL-TO-ANALOG CONVERTERS: This addendum has now been incorporated into JESD99.

July 1989; Incorporated into JESD99-A, May 2000 /JC-10 Committee

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JESD 99B

TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR MICROELECTRONIC DEVICES: This standard will be useful to users, manufacturers, educators, technical writers, and others interested in the characterization, nomenclature, and classification of microelectronics devices. There are general guidelines for both letter symbols and abbreviations applicable to all integrated circuits, and detailed sections for digital ICs, linear (analog) ICs, interface ICs (including D/A and A/D converters), voltage regulators, charge-transfer devices. The standard lists and defines more than 400 of the most common physical and electrical terms applicable to these devices and shows the industry-standard symbol and abbreviations that have been established for such terms.

May 2007 /JC-10 Committee $127.00

JESD 100B.01

TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR MICROCOMPUTERS, MICROPROCESSORS, AND MEMORY INTEGRATED CIRCUITS: A revised reference for technical writers and educators, manufacturers, buyers and users of microprocessors, microcomputers, mircocontrollers, memory ICs, and other complex devices. The terms and their definitions in this standard have been updated and are in general agreement with the latest publications of the IEEE and the IEC. The companion standard for other integrated circuits is JESD99A. Also included is a system for generating symbols for time intervals found in complex sequential circuits, including memories. JESD100B.01 is the first minor revision of JESD100-B, December 1999. Annex A briefly shows entries that have changed.

December 2002 /JC-10 Committee $71.00

JESD 201A

ENVIRONMENTAL ACCEPTANCE REQUIREMENTS FOR TIN WHISKER SUSCEPTIBILITY OF TIN AND TIN ALLOY SURFACE FINISHED: The methodology described in this document is applicable for environmental acceptance testing of tin based surface finishes and mitigation practices for tin whiskers. This methodology may not be sufficient for applications with special requirements, (i.e., military, aerospace, etc.). Additional requirements may be specified in the appropriate requirements (procurement) documentation.

August 2008 September 2007 /JC-14.3 Subcommittee $71.00

JESD 202

METHOD FOR CHARACTERIZING THE ELECTROMIGRATION FAILURE TIME DISTRIBUTION OF INTERCONNECTS UNDER CONSTANT-CURRENT AND TEMPERATURE STRESS: This is an accelerated stress test method for determining sample estimates and their confidence limits of the median-time-to-failure, sigma, and early percentile of a log-Normal distribution, which are used to characterize the electromigration failure-time distribution of equivalent metal lines subjected to a constant current-density and temperature stress. Failure is defined as some pre-selected fractional increase in the resistance of the line under test. Analysis procedures are provided to analyze complete and singly, right-censored failure-time data. Sample calculations for complete and right-censored data are provided in Annex A. The analyses are not intended for the case when the failure distribution cannot be characterized by a single log-Normal distribution.

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March 2006 June 2004 /JC-14.2 Subcommittee $61.00

JESD 203

STANDARD TEST LOADS FOR DUAL-SUPPLY LEVEL TRANSLATION DEVICES This standard defines ac test loads for dual-supply level translation devices. Uniform test loads enable easy comparison of electrical parameters of dual-supply level translation devices across functions, logic families and IC suppliers. This standard is only intended to apply to devices released subsequent to the publication of this document.

November 2005 June 2004 /JC-40.1 Subcommittee $40.00

JESD 204A

SERIAL INTERFACE FOR DATA CONVERTERS This specification describes a serialized interface between data converters and logic devices. It contains normative information to enable designers to implement devices that communicate with other devices covered by this specification. Informative sections are included to clarify and exemplify the specification.

April 2008 August 2007 /JC-16 Committee $130.00

JESD 205

FBDIMM STANDARD: DDR2 SDRAM FULLY BUFFERED DIMM (FBDIMM) DESIGN SPECIFICATION: This specification defines the electrical and mechanical requirements for 240-pin, PC2-4200/PC2-5300/PC2-6400, 72 bit-wide, Fully Buffered Double Data Rate Synchronous DRAM Dual In-Line Memory Modules (DDR2 SDRAM FB-DIMMs).These SDRAM FB-DIMMs are intended for use as main memory when installed in systems such as servers and workstations. PC2-4200/PC2-5300/PC2-6400 refers to the DIMM naming convention in which PC2-4200/PC2-5300/PC2-6400 indicates a 240-pin DDR2 DIMM running at 266/333/400 MHz DRAM clock speed and offering 4266/5333/6400 MB/s bandwidth.

March 2007 March 2006 /JC-45.4 Subcommittee $147.00

JESD 206

FBDIMM Architecture and Protocol

January 2007 March 2006 /JC-40 Committee $147.00

JESD 208

SPECIALITY DDR2-1066 SDRAM This document defines the Specialty DDR2-1066 SDRAM specification, including features, functionalities, AC and DC characteristics, packages, and ball/signal assignments. The purpose of this Specification is to define the minimum set of requirements for JEDEC compliant 256 Mb through 4 Gb for x4, x8, and x16 Specialty DDR2-1066 SDRAM devices.

November 2007 March 2007 /JC-42.3 Subcommittee $130.00

JESD 209

LOW POWER DOUBLE DATA RATE (LPDDR) SDRAM STANDARD This document was numbered as JESD79-4 May 2006 to August 2007. The document number has been corrected to JESD209 09/17/2007. The purpose of this Specification is to define the minimum set of requirements for JEDEC compliant 128 Mb through 1 Gb for x16 and x32 Low Power Double Data Rate SDRAM devices. System designs based on the required aspects of this specification will be supported by all LPDDR SDRAM vendors providing compliant devices.

August 2007 June 2005 /JC-42.3 Subcommittee $83.00

JESD 210

AVALANCHE BREAKDOWN DIODE (ABD) TRANSIENT VOLTAGE SUPPRESSORS This standard is applicable to avalanche breakdown diodes when used as a surge protector or transient voltage suppressor (TVS). It describes terms and definitions and explains methods for verifying device ratings and measuring device characteristics. This standard may be applied to other surge-protection components with similar characteristics as the ABD.

December 2007 April 2003 /JC-22.5 Subcommittee $72.00

JESD 22-A122

POWER CYCLING This Test Method establishes a uniform method for performing component package power cycling stress test. This specification covers power induced temperature cycling of a packaged component, simulating the non-uniform temperature distribution resulting from a device powering on and off in the application.

August 2007 January 2007 /JC-14.1 Subcommittee $47.00

JESD 282B.01

SILICON RECTIFIER DIODES: This standard provided definitions, electrical characteristics circuit technology, letter symbols and registration format for diodes and stacks. It also covers rating and characteristics, manufacturing and performance as well as test practices to demonstrate the performance of semiconductor rectifier diodes and rectifier stacks used

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for the conversion and/or control of electric power. This version contains minor revisions to JESD282-B, April 2000.

November 2002 /JC-22.2 Subcommittee $177.00

JESD 284-A

TEST METHODS FOR THE COLLECTOR-BASE TIME CONSTANT AND FOR THE RESISTIVE PART OF THE COMMON-EMITTER INPUT IMPEDANCE: The test methods described in this Standard are generally applicable to alloy-like devices for which the usual simplified equivalent circuits can be employed.

November 1963; Reaffirmed November 1963, June 1972, April 1981, April 1999, October 2002 /JC-25 Committee $38.00

JESD 286-B

STANDARD FOR MEASURING FORWARD SWITCHING CHARACTERISTICS OF SEMICONDUCTOR DIODES: This method updates the standard procedure for characterizing the switching of signal or switching diodes when a step function of forward current is applied. The objective is to provide a standard so that accurate comparisons can be made.

February 2000 /JC-22.4 Subcommittee $40.00

JESD 307

VOLTAGE REGULATOR DIODE NOISE VOLTAGE MEASUREMENT: This standard is intended to cover the measurement of noise voltage in voltage regulator diodes in the reverse breakdown region. It describes noise voltage measurements at specified conditions, but may be used as a guide for making such measurements at other than specified conditions. (Formerly EIA-307)

May 1965; Reaffirmed January 1992, April 1999, April 2002 April 2002 /JC-22.4 Subcommittee $38.00

JESD 313-B

THERMAL RESISTANCE MEASUREMENTS OF CONDUCTION COOLED POWER TRANSISTORS: This standard provides a test method for measuring thermal resistance for conduction cooled power transistors.

October 1975; Reaffirmed April 1981, April 2001 /JC-25 Committee $45.00

JESD 320-A

CONDITIONS FOR MEASUREMENT OF DIODE STATIC PARAMETERS: This standard provides guidance for achieving equilibrium when measuring temperature sensitive static parameters of signal diodes. (Formerly EIA-302-A)

December 1992; Reaffirmed April 1999, April 2002 (Original publication July 1965) /JC-22.4 Subcommittee $37.00

JESD 381-A

METHOD OF DIODE Q MEASUREMENT: This standard was updated and revised for the purpose of clarifying the method used to measure Q of a Voltage-Variable-Capacitance Diode in the low VHF range using an RF admittance bridge. Originally published November 1981. Approved as ANSI/EIA-381-A-1992, July 1992. Became JESD381-A after ANSI expiration July 2002.

November 1981; Reaffirmed April 1999, April 2002 April 1999 /JC-22.4 Subcommittee $48.00

JESD 419-A

STANDARD LIST OF VALUES TO BE USED IN SEMICONDUCTOR DEVICE SPECIFICATIONS AND REGISTRATION FORMAT: This document contains standard lists of values which are recommended for use in semiconductor device specification and JEDEC Registration Formats. Good reasons should exist in those cases where values are used that are not included in these lists.

October 1980; Reaffirmed March 2001 /JC-25 Committee $37.00

JESD 482-A

LIST OF PREFERRED VALUES FOR USE ON VARIOUS TYPES OF SMALL SIGNAL AND REGULATOR DIODES: This standard specifies preferred values to be used on signal and regulator diodes. It will facilitate the standardization for nominal values used on small signal regulator diodes previously established in JEDEC Suggested Standard No. 2. (Formerly EIA-482-A)

August 1984; Reaffirmed April 1999, April 2002 April 2002 /JC-22.4 Subcommittee $38.00

JESD 51-12

GUIDELINES FOR REPORTING AND USING ELECTRONIC PACKAGE THERMAL INFORMATION: This document provides guidelines for both reporting and using electronic package thermal information generated using JEDEC JESD51 standards. By addressing these two areas, this document can be used as the common basis for discussion between electronic package thermal information suppliers and users.

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May 2005 October 2004 /JC-15.1 Subcommittee $49.00

JESD 531

THERMAL RESISTANCE TEST METHOD FOR SIGNAL AND REGULATOR DIODES (FORWARD VOLTAGE, SWITCHING METHOD): This standard describes a test method for measuring the thermal resistance of signal and regulator diodes. The need for modification of this test method arose out of the limited description that existed earlier for both signal and regulator diode applications in testing for thermal resistance. Previously published as ID-13. ANSI/EIA-531-1986 (July) expired June 1996. Became JESD531 after reaffirmation April 2002.

July 1986; Reaffirmed April 1999, April 2002 April 1999 /JC-22.4 Subcommittee $47.00

JESD 625-A

REQUIREMENTS FOR HANDLING ELECTROSTATIC-DISCHARGE-SENSITIVE (ESDS) DEVICES: This standard establishes the minimum requirements for Electrostatic Discharge (ESD) control methods and materials used to protect electronic devices that are susceptible to damage or degradation from electrostatic discharge (ESD). The passage of a static charge through an electrostatic-discharge-sensitive (ESDS) device can result in catastrophic failure or performance degradation of the part. Device sensitivity to ESD is determined by test methods such as EIA/JESD22-A114. ESDS devices with human body model sensitivities of less than +200 volts may need additional protective measures beyond those specified in this standard.

December 1999 /JC-14.1 Subcommittee $55.00

JESD 659B

FAILURE-MECHANISM-DRIVEN RELIABILITY MONITORING: This method establishes requirements for application of Statistical Reliability Monitoring 'SRM' technology to monitor and improve the reliability of electronic components and subassemblies. The standard also describes the condition under with a monitor may be replaced or eliminated.

February 2007 September 2006 /JC-14.3 Subcommittee $45.00

JESD 671-A

COMPONENT QUALITY PROBLEM ANALYSIS AND CORRECTIVE ACTION REQUIREMENTS (INCLUDING ADMINISTRATIVE QUALITY PROBLEMS): This revision now encompasses administrative quality problems, in addition to the electrical and visual/mechanical quality problems that were addressed in the original release. A standard set of problem categories for each of these three types of component problems is presented for tracking and reporting purposes. A common set of customer and supplier expectations and requirements are set forth to help facilitate the successful problem analysis and corrective action of any type of component quality problem.

December 1999 /JC-14.4 Subcommittee $43.00

JESD 8-19

POD18 - 1.8 V Pseudo Open Drain I/O This standard defines the dc and ac single-ended (data) and differential (clock) operating conditions, I/O impedances, and the termination and calibration scheme for 1.8 V Pseudo Open Drain I/Os. The 1.8 V Pseudo Open Drain interface, also known as POD18, is primarily used to communicate with GDDR3 SGRAM devices.

December 2006 December 2003 /JC-16 Committee $43.00

JESD 8-20

POD15 - 1.5 V Pseudo Open Drain I/O This standard defines the dc and ac single-ended (data) and differential (clock) operating conditions, I/O impedances, and the termination and calibration scheme for 1.5 V Pseudo Open Drain I/Os. The 1.5 V Pseudo Open Drain interface, also known as POD15, is primarily used to communicate with GDDR4 SGRAM devices.

December 2006 March 2006 /JC-16 Committee $43.00

JESD 82-8.01

STANDARD FOR DEFINITION OF ?CU877 PLL CLOCK DRIVER FOR REGISTERED DDR2 DIMM APPLICATIONS This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of a ?CU877 PLL clock device for registered DDR2 DIMM applications. The purpose is to provide a standard for a ?CU877 PLL clock device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use. This document includes minor editorial changes as noted in Annex A, page 16.

February 2004 /JC-40 Committee $49.00

JESD 84-A43

EMBEDDED MULTIMEDIACARD (EMMC) EMMC/CARD PRODUCT STANDARD, HIGH CAPACITY, INCLUDING RELIABLE WRITE, BOOT, AND SLEEP MODES (MMCA, 4.3) This document is a

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complete specification for embedded memory devices and removable memory cards using the MMC interface version 4.3. New features developed through the Electrical Joint Task Group include: Sleep mode, Boot mode and Reliable Write.

December 2007 July 2007 /JC-64 Committee

JESD 84-C01

MULTIMEDIACARD (MMC) MECHANICAL STANDARD This document is a mechanical product specification for a removable non-volatile flash memory device using the MMC interface version 4.2. The electrical specification for the MMC interface version 4.2 is document JESD84-B42.

December 2007 August 2007 /JC-64 Committee

JESD 84-C43

EMBEDDED MULTIMEDIACARD (eMMC)MECHANICAL STANDARD This document is a mechanical product specification for a high capacity embedded memory device using the MMC interface version 4.2 and a BGA package.

December 2007 August 2007 /JC-64.2 Subcommittee

JESD 93

HYBRIDS/MCM This specification establishes the general requirements for hybrid microcircuits, RF/microwave hybrid microcircuits and MCMs (hereafter referred to as devices). Detailed performance requirements for a specific device are specified in the applicable device acquisition document. In the event of a conflict between this document and the device acquisition document, the device acquisition document will take precedence.

September 2005 May 2002 /JC-13.5 Subcommittee $49.00

JESD 96A-1

Addendum 1 to JESD96A - INTEROPERABILITY AND COMPLIANCE TECHNICAL REQUIREMENTS FOR JEDEC STANDARD JESD96A - RECOMMENDED PRACTICE FOR USE WITH IEEE 802.11N The normative information in this publication is intended to provide a technical design team to construct the interface on a FED and a BED such that they will operate correctly with each other (at the interface level), when designed to JESD96A.

January 2007 March 2006 /JC-61 Committee $45.00

JESD JIG-101

Material Composition Declaration Guide for Electronic Products The purpose of this guide establishes the materials and substances to be disclosed by suppliers when those materials and substances are present in products and subparts that are incorporated into EEE. It benefits suppliers and their commercial customers by providing consistency and efficiency to the material declaration process. It promotes the development of consistent data exchange formats and tools that will facilitate and improve data transfer along the entire global supply chain.

June 2005 January 2003 /JC-14 Committee

NUMBER **Joint IPC/JEDEC Standards (J-STD-)** **PRICE**

J-STD- 002B

SOLDERABILITY TESTS FOR COMPONENT LEADS, TERMINATIONS, LUGS, TERMINALS AND WIRES: At the request of IPC, J-STD-002B has been temporarily removed from the free download area until such time when it is revised to include lead-free. In its place, JEDEC's Test Method B102-D, Solderability, which includes lead-free, is available for free downloading.

February 2003 Removed 01/21/04 /JC-14.1 Subcommittee

J-STD- 020D.01

JOINT IPC/JEDEC STANDARD FOR MOISTURE/REFLOW SENSITIVITY CLASSIFICATION FOR NONHERMETIC SOLID STATE SURFACE-MOUNT DEVICES: This document identifies the classification level of nonhermetic solid-state surface mount devices (SMDs) that are sensitive to moisture-induced stress. It is used to determine what classification level should be used for initial reliability qualification. Once identified, the SMDs can be properly packaged, stored and handled to avoid subsequent thermal and mechanical damage during the assembly solder reflow attachment and/or repair operation. This revision now covers components to be processed at higher temperatures for lead-free assembly. A hard cop version is available for $20 each for IPC/JEDEC members and $40 for nonmembers.

March 2008 September 2006 /JC-14.1 Subcommittee

J-STD- 033B.1

JOINT IPC/JEDEC STANDARD FOR HANDLING, PACKING, SHIPPING AND USE OF MOISTURE/REFLOW SENSITIVE SURFACE-MOUNT DEVICES: NOTE - The Moisture Sensitive Caution Label (figure 3-4) has been editorially revised since originally posted 11/04/05, if you downloaded this file prior to 12/14/05 please download this revised version. This

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document provides SMD manufacturers and users with standardized methods for handling, packing, shipping and use of moisture/reflow sensitive SMDs. Now updated to support components that may need to be processed at higher temperatures, such as lead-free processes, these methods help avoid damage from moisture absorption and exposure to solder reflow temperatures that can result in yield and reliability degradation. IPC/JEDEC J-STD-033B helps achieve safe and damage-free reflow with the dry packing process and provides a minimum shelf life of 12 months from the seal date when using sealed dry bags.

January 2007 (Available in German, www.ihs.com) October 2004 /JC-14.1 Subcommittee

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J-STD- 035

JOINT IPC/JEDEC STANDARD FOR ACOUSTIC MICROSCOPY FOR NONHERMETRIC ENCAPSULATED ELECTRONIC COMPONENTS: This test method defines the procedures for performing acoustic microscopy on non-hermetic encapsulated electronic components. This method provides users with an acoustic microscopy process reflow for detecting defects non-destructively in plastic packages while achieving reproducibility.

May 1999; Under Revision /JC-14.1 Subcommittee $35.00

J-STD- 609

MARKING AND LABELING OF COMPONENTS, PCBs AND PCBAs TO IDENTIFY LEAD (Pb), Pb-FREE AND OTHER ATTRIBUTES This standard applies to boards/assemblies, to identify the type of Pb-free or Pb-containing solder used. This standard documents a method for identifying board surface finishes and Printed Circuit Board (PCB) resin systems. This standard applies to PCB base materials and for marking the type of conformal coating utilized on Printed Circuit Board Assemblies (PCBAs). Material and their containers previously marked or labeled according to JESD 97 or IPC-1066 need not be remarked unless agreed upon by the supplier and customer.

May 2007 January 2007 /JC-14.4 Subcommittee

NUMBER	Joint Publication (JP)	PRICE

JP 001.01

FOUNDRY PROCESS QUALIFICATION GUIDELINES (Wafer Fabrication Manufacturing Sites) This document provides a guideline for the minimum set of measurements to qualify a new semiconductor wafer process. It is written with particular reference to a generic silicon based CMOS logic technology. While it may be applicable to other technologies (e.g. analog CMOS, bipolar, BICMOS, GaAs, etc.), some sections apply specifically to CMOS. No effort was made in the present document to cover all the qualification requirements for specific other technologies, e.g. Cu/Low K interconnects or ultra thin gate oxide. This publication, is co-sponsored by JEDEC JC-14.2 and the FSA (Fabless Semiconductor Association). It originated at the FSA as a technology specific document, and has evolved into a generic set of qualification requirements.

May 2004 /JC-14.2 Subcommittee $67.00

JP 002

CURRENT TIN WHISKERS THEORY AND MITIGATION PRACTICES GUIDELINE This document will provide insight into the theory behind tin whisker formation as it is known today and, based on this knowledge, potential mitigation practices that may delay the onset of, or prevent tin whisker formation. The potential effectiveness of various mitigation practices will also be briefly discussed. References behind each of the theories and mitigation practices are provided.

March 2006 June 2005 /JC-14.1 Subcommittee $55.00

NUMBER	Joint Standard (JS)	PRICE

JS 9702

MONOTONIC BEND CHARACTERIZATION OF BOARD-LEVEL INTERCONNECTS (IPC/JEDEC-9702) This publication specifies a common method of establishing the fracture resistance of board-level device interconnects to flexural loading during non-cyclic board assembly and test operations. Monotonic bend test qualification pass/fail requirements are typically specific to each device application and are outside the scope of this document.

June 2004 September 2003 /JC-14.1 Subcommittee

JS 9704

Printed Wiring Board (PWB) Strain Gage Test Guideline This document describes specific guidelines for strain gage testing for Printed Wiring Board (PWB)assemblies. The suggested procedures enables board manufacturers to conduct required strain gage testing independently, and provides a quantitative method for measuring board flexure, and assessing risk levels. The topics covered include: Test setup and equipment; requirements; Strain measurement; Report format

June 2005 January 2005 /JC-14.1 Subcommittee

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NUMBER	JEDEC Publications (JEP)	PRICE
JEP 64	SOLID STATE PRODUCTS REGISTRATION LIST(ORDER FROM TYPE ADMINISTRATION OFFICE): This publication includes addenda from 1976 to August 1986. The purpose of this list is to determine release numbers (file numbers) for JEDEC Type Designations. (See page 6 for more information.) September 1986; Reaffirmed November 2002 / Committee!33JCJEDC	$162.00
JEP 65	TEST PROCEDURES FOR VERIFICATION OF MAXIMUM RATINGS OF POWER TRANSISTORS: This publication describes tests which are intended to represent the verification of maximum ratings for data sheets; they are not tests for performance or quality level. This material is to be used in conjunction with formats developed for device registration and defining data. December 1967; Reaffirmed September 1981, April 1999 /JC-25 Committee	$52.00
JEP 69-B	PREFERRED LEAD CONFIGURATION FOR FIELD-EFFECT TRANSISTORS: This publication indicates preferred pinouts for FETs in various package designs. November 1973; Reaffirmed September 1981, April 1999 /JC-25 Committee	$38.00
JEP 70-B	QUALITY AND RELIABILITY STANDARDS AND PUBLICATIONS: Contains a listing and description of commonly used quality and reliability related standards and publications that are applicable to the semiconductor industry. It is intended to be a reference aid in finding available standards and obtaining a copy from the source of the standard. It is not intended to recommend or imply the applicability of any standard for a specific purpose. This revision has been updated to include recent releases as well as revisions, in addition, URLs have been added to the October 1999 /JC-14.4 Subcommittee	$57.00
JEP 74	STANDARD LIST OF VALUES TO BE USED IN POWER TRANSISTOR DEVICE REGISTRATION AND MINIMUM DIFFERENCES FOR DISCRETENESS OF REGISTRATIONS - SUPERSEDED BY EIA-419-A, February 1996. July 1969; Rescinded February 1996 /JC-25 Committee	$38.00
JEP 75	LETTER SYMBOLS USED WITH INFRARED DEVICES - INCORPORATED INTO JESD77-A. August 1984; Rescinded August 1984 /JC-10 Committee	
JEP 78	RELATIVE SPECTRAL RESPONSE CURVES FOR SEMICONDUCTOR INFRARED DETECTORS: The intent of this publication is to facilitate the specification of infrared detector diodes, particularly in conjunction with the preparation of data for JEDEC type registration. October 1969 /JEDEC Committee	$52.00
JEP 79	LIFE TEST METHODS FOR PHOTOCONDUCTIVE CELLS: This publication is for photoconductive cells sensitive primarily in the visible and near infrared region. September 1969	$52.00
JEP 84A	RECOMMENDED PRACTICE FOR MEASUREMENT OF TRANSISTOR LEAD TEMPERATURE: This publication covers recommended methods for measurement of transistor lead temperatures under various load conditions. The techniques described are sufficiently accurate for most applications. June 2004 September 2002 /JC-25 Committee	$41.00
JEP 86-A	RECOMMENDED PRACTICE FOR DUAL DIMENSIONING May 1976; Rescinded November 1999 /JC-11 Committee	
JEP 87	FORWARD TURN-ON TIME MEASUREMENT ON SEMI-DIODES - INCORPORATED INTO EIA-282-A. June 1992; Rescinded June 1985 /JC-22.2 Subcommittee	
JEP 88	THERMAL RESISTANCE AND THERMAL IMPEDANCE TEST METHODS FOR STUD AND BASE-MOUNTED RECTIFIER DIODES AND THYRISTORS January 1974; Rescinded June 1992 /JC-22.1 Subcommittee	

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JEP 90	**THERMAL RESISTANCE FOR TEST METHODS FOR SIGNAL DIODES - SUPERSEDED BY EIA-531, July 1986. See JESD531, April 2002.** September 1983; Rescinded September 1986 /JC-22.4 Subcommittee	
JEP 93	**MICROELECTRONIC DEVICE TYPE ASSIGNMENTS** August 1975; Rescinded June 1992 June 1992 / Committee!33JCJEDC	
JEP 95	**JEDEC REGISTERED AND STANDARD OUTLINES FOR SOLID STATE AND RELATED PRODUCTS:** This publication is a compilation of some 1800 pages of outline drawings for microelectronic packages including transistors, diodes, DIPS, chip carriers and package interface BGA outlines in both inch and metric versions. January 2000 /JC-11 Committee	$425.00
JEP 95 AUS	**ANNUAL UPDATING SERVICE:** Subscription to this updating service is available from the JEDEC Office. New outlines are shipped to subscribers for insertion into the appropriate sections of Publication No. 95. JEP95 and Updating Service can be ordered through JEDEC at (703)907-7540 or ptanner@jedec.org. January 2000 /JC-11 Committee	$125.00
JEP 96	**GUIDELINES FOR NONDESTRUCTIVE PULL TESTING OF WIRE BONDS ON HYBRID DEVICES** March 1977; Rescinded April 2000 /JC-13.5 Subcommittee	
JEP 99	**GLOSSARY OF MICROELECTRONIC TERMS, DEFINITIONS, AND SYMBOLS: ELEVATED TO JESD99, June 1985.** July 1977; Rescinded June 1985 /JC-10 Committee	
JEP 100	**TERMS, DEFINTIONS, AND LETTER SYMBOLS FOR MICROCOMPUTERS AND MEMORY INTEGRATED CIRCUITS: ELEVATED TO JESD100, August 1993.** September 1979; Rescinded October 1983 /JC-10 Committee	
JEP 101-C	**JEDEC REQUIREMENTS FOR CLASS B MICROCIRCUITS: RESCINDED, May 2006** November 1995; Rescinded May 2006 /JC-13.2 Subcommittee	$38.00
JEP 102	**STANDARD FOR 64K x 1 DYNAMIC RAM - SUPERSEDED BY JESD21-C.** September 1978; Rescinded April 1985 April 1985 /JC-42 Committee	
JEP 103A	**SUGGESTED PRODUCT-DOCUMENTATION, CLASSIFICATIONS, AND DISCLAIMERS** In order to improve understanding between manufacturers and users, a consistent set of product-documentation classifications associated with the stages of product development. July 1996; Reaffirmed November 1999, May 2003 /JC-10 Committee	$38.00
JEP 104C.01	**REFERENCE GUIDE TO LETTER SYMBOLS FOR SEMICONDUCTOR DEVICES:** This publication provides a quick reference to the letter symbols and corresponding terms that are defined in JESD77-B, Terms, Definitions, and Letter Symbols for Discrete Semiconductor and Optoelectronic Devices; JESD99-A, Terms, Definitions, and Letter Symbols for Microelectronic Devices, and JESD100-B, Terms, Definitions, and Letter Symbols for Microcomputers, Microprocessors, and Memory Integrated Circuits. It is intended to simplify interpretation of data sheets and specifications and to promote the uniform use of these symbols. The symbols relate to ratings and characteristics found in data sheets and other specifications. Some abbreviations used in lieu of symbols are also included. The newly added Annex B is provided as an aid to determining what symbol should be used and is organized by term, whereas the main body of the publication is organized by symbol or abbreviation as in previous versions. This version contains minor revisions. May 2003 /JC-10 Committee	$91.00
JEP 105	**JEDEC GUIDELINE FOR THE CHARACTERIZATION OF HYBRID POLYMERIC MATERIALS - SUPERSEDED BY JESD72, June 2001** April 1983; Rescinded June 2001 /JC-13.5 Subcommittee	
JEP 106Y	**STANDARD MANUFACTURERS IDENTIFICATION CODE:** The manufacturers identification code is defined by one or more 8 bit fields, each consisting of 7 data bits plus 1 odd parity bit. The	

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manufacturers identification code is assigned, maintained and updated by the JEDEC Office. The intent of this identification code is that it may be used whenever a digital field is required, e.g., hardware, software, documentation, etc. To make a request for an ID Code please go to http://www.jedec.org/Home/MIDCODE_request.cfm

June 2008 NOTE: JEP106U was in error starting with bank two an additional continuation code was added. This has been corrected, JEP106U should be discarded. /JC-42.3 Subcommittee $62.00

JEP 107

TEST METHOD FOR QUALIFICATION AND ACCEPTANCE OF PARTICLE GETTERS FOR USE IN HYBRID MICROELECTRONIC APPLICATIONS - SUPERSEDED BY JESD72, June 2001

April 1985; Rescinded June 2001 /JC-13.5 Subcommittee

JEP 108-B

DISTRIBUTOR REQUIREMENTS FOR HANDLING ELECTROSTATIC -DISCHARGE SENSITIVE (ESDS) DEVICES: SUPERSEDED BY JESD42, March 1994.

April 1991; Superseded /JC-14.1 Subcommittee

JEP 109-C

GENERAL REQUIREMENTS FOR DISTRIBUTORS OF MILITARY SEMICONDUCTOR DEVICES: Superseded by JESD31-A, June 2001.

March 1995; Rescinded November 2001 /JC-13 Committee

JEP 110

GUIDELINES FOR THE MEASUREMENT OF THERMAL RESISTANCE OF GaAs FETS: This publication is intended for power GaAs FET applications requiring high reliability. An accurate measurement of thermal resistance is extremely important to provide the user with knowledge of the FETs operating temperature so that more accurate life estimates can be made. FET failure mechanisms and failure rates have, in general, an exponential dependence on temperature (which is why temperature-accelerated testing is successful). Because of the exponential relationship of failure rate with temperature, the thermal resistance should be referenced to the hottest part of the FET.

July 1988 /JC-14.7 Subcommittee $43.00

JEP 111

TEST PROCEDURES FOR CUSTOM MONOLITHIC MICROCIRCUITS - SUPERSEDED BY MIL-PRF-38535C.

July 1986; Rescinded June 1996 June 1996 /JC-13.2 Subcommittee

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JEP 112

TEST METHOD FOR QUALIFICATION AND ACCEPTANCE OF CIRCUIT SUPPORT FILMS FOR USE IN MICROELECTRONIC APPLICATIONS - SUPERSEDED BY JESD72, June 2001

June 1987; Rescinded June 2001 /JC-13 Committee $52.00

JEP 113-B

SYMBOL AND LABELS FOR MOISTURE-SENSITIVE DEVICES: Certain PSMC (Plastic Surface-mount Components) are subject to permanent damage due to moisture-induced failures encountered during high-temperature surface-mount processing unless appropriate precautions are observed. The purpose of this publication is to provide a distinctive symbol and labels to be used to identify those devices that require special packing and handling precautions.

May 1999 /JC-14.1 Subcommittee $45.00

JEP 114.01

GUIDELINES FOR PARTICLE IMPACT NOISE DETECTION (PIND) TESTING, OPERATOR TRAINING, AND CERTIFICATION: This publication was developed to help the user of this test methodology avoid common interference Æs to successful application. The guide contains sections on typical specification requirements, sources of particles, PIND test systems, calibration, maintenance, test interference's, operator training, particle recovery and failure analysis. Application of the information contained in the guide will improve the quality and affectivity for any PIND testing operation.

October 2007 August 2007 /JC-13.5 Subcommittee $72.00

JEP 115

POWER MOSFET ELECTRICAL DOSE RATE TEST METHOD: The purpose of this Test Method is to establish electrical criteria for comparing and specifying power MOSFET performance under high dose rate radiation.

August 1989; Reaffirmed April 1999 /JC-25 Committee $41.00

JEP 116

CMOS SEMICUSTOM DESIGN GUIDELINES: The design of ASIC circuits is becoming a significant part of system or product design, yet many problems continue to exist in

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current design practice. The guidelines in this document provide an explanation of common ASIC design problems and concerns and where possible offer solutions.

November 1991 / Committee!33JC44 $109.00

JEP 117

GUIDELINES FOR USER NOTIFICATION OF PRODUCT/PROCESS CHANGES BY SEMICONDUCTOR SUPPLIERS - SUPERSEDED BY JESD46, August 1997.

April 1994; Rescinded July 1994 /JC-14.4 Subcommittee

JEP 118

GUIDELINES FOR GaAs MMIC AND FET LIFE TESTING: These guidelines apply to monolithic microwave GaAs integrated circuits (MMICs) and their individual component building blocks, such as GaAs field effect transistors (FETs), resistors, and capacitors. The purpose of this document is to define a standard approach for evaluating the expected live of GaAs MMICs so that results from different life tests can be compared and so that wording of this document that the MMIC contains at least one FET, but the use of this document has no such limitation.

January 1993 /JC-14.7 Subcommittee $48.00

JEP 119A

A PROCEDURE FOR EXECUTING SWEAT: This document describes an algorithm for performing the Standard Wafer Level Electromigration Accelerated Test (SWEAT) method with computer controlled instrumentation. The algorithm requires a separate iterative technique (not provided) to calculate the force current for a given target time to failure. This document does not specify what test structure to use with this procedure. However, users of this algorithm report its effectiveness on both straight-lines and via-terminated test structures. Some test-structures design features are provided in JESD87 and in ASTM 1259M - 96.

August 2003 /JC-14.2 Subcommittee $57.00

JEP 120-A

INDEX OF TERMS DEFINED IN JEDEC PUBLICATIONS: This publication provides an index to terms that are defined in certain JEDEC publications. It is intended to promote the uniform use of these terms and their definitions while reducing the proliferation of new definitions for old terms.

May 2000 /JC-10 Committee $109.00

JEP 121A

REQUIREMENTS FOR MICROELECTRONIC SCREENING AND TEST OPTIMIZATION: The purpose of this document provides the basis for the optimization of 100% screening/stress operations and sample inspection test activities. This document is designed to assist the manufacturer in optimizing the test flow while maintaining and/or improving assurance of providing high quality and reliable product in an efficient manner. This will allow for optimization of testing that is not adding value, hence, reducing cycle time and costs.

October 2006 May 2006 /JC-13.2 Subcommittee $59.00

JEP 122D

FAILURE MECHANISMS AND MODELS FOR SEMICONDUCTOR DEVICES: This publication provides a list of failure mechanisms and their associated activation energies or acceleration factors that may be used in making system failure rate estimations when the only available data is based on tests performed at accelerated stress test conditions. The method to be used is the Sum of the Failure Rates method.

October 2008 January 2008 /JC-14.1 Subcommittee $130.00

JEP 123

GUIDELINE FOR MEASUREMENT OF ELECTRONIC PACKAGE INDUCTANCE AND CAPACITANCE MODEL PARAMETERS: The need for this guideline arose from widespread lack of consistency in characterizing electrical parameters of electronic packages, which existed in the industry until the early 1990s. Then, the JEDEC Committee JC-15 provided the forum where various methods were discussed and commonality in approach emerged. The result is that today we have relatively consistent results in measuring and reporting electrical package parameters, as well as specialized tools (e.g., the IPA-510, the interconnect parameter analyzer) which were developed to support the methodology.

October 1995 /JC-15.2 Subcommittee $49.00

JEP 124

GUIDELINES FOR THE PACKING, HANDLING, AND REPACKING OF MOISTURE-SENSITIVE COMPONENTS - SUPERSEDED BY J-STD-033, May 1999.

December 1995; Rescinded November 1999 November 1999 /JC-14.4 Subcommittee

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JEP 126

GUIDELINE FOR DEVELOPING AND DOCUMENTING PACKAGE ELECTRICAL MODELS DERIVED

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FROM COMPUTATIONAL ANALYSIS: This publication provides a guideline to suppliers of IC components with a template for documenting the numerical simulation assumptions. In addition this guideline also suggests a model environment to reference when comparing various packages or component suppliers. This publication should improve the communication between the package model suppliers. This publication should improve the communication between the package model supplier and the end user.

May 1996 /JC-15.2 Subcommittee $38.00

JEP 128

GUIDE FOR STANDARD PROBE PAD SIZES AND LAYOUTS FOR WAFER LEVEL ELECTRICAL TESTING: This guide was developed to expedite inter-laboratory experiments used to evaluate or develop standard test methods that involve test-structure measurements or tests. It also facilitates, generally, any electrical tests that require wafer-probe card to make electrical contact to test structures. Widespread use of this guide will afford the efficient and cost-effective use of water-probe test stations because of the need for fewer probe cards and probe-card changes to accommodate the various test structures that may need to be tested.

November 1996 /JC-14.2 Subcommittee $40.00

JEP 129

THERMAL TEST CHIP GUIDELINE (WIRE BOND TYPE CHIP)- SUPERSEDED BY JESD51-4, September 1997.

February 1997; Elevated September 1997 /JC-15.1 Subcommittee

JEP 130A

GUIDELINES FOR PACKING AND LABELING OF INTEGRATED CIRCUITS IN UNIT CONTAINER PACKING: This document establishes guidelines for integrated circuit unit container and the next level (intermediate) container packing and labeling. The guidelines include tube/rail standardization, intermediate packing, date codes, tube labeling, intermediate container and shipping labels, and standardize tube quantities. Future revisions of this document will also include tray and reel guidelines. The objective of this publication is to promote the standardization of practices between manufacturers and distributors resulting in improved efficiency, profitability, and product quality.

February 2006 January 2005 /JC-14.4 Subcommittee $43.00

JEP 131A

PROCESS FAILURE MODE AND EFFECTS ANALYSIS (FMEA): This publication was created in response to the need for a straight forward FMEA procedure. The objective is to provide a guideline for the application of FMEA techniques to improve quality, reliability and/or consistency of electronic components and subassemblies by continually evaluating processes/products against potential failure modes.

May 2005 October 2004 /JC-15.1 Subcommittee $55.00

JEP 132

PROCESS CHARACTERIZATION GUIDELINE: This guideline provides a methodology to characterize a new or existing process and is applicable to any manufacturing or service process. It describes when to use specific tools such as failure mode effects analysis (FEMA), design or experiments (DOE), measurement system evaluation (MSE), capability analysis (CpK), statistical process control (SPC), and problem solving tools. It also provides a brief description of each tool. In December 2004 the document was renumbered to conform with JM7, JEDEC Style Manual.

July 1998; Reaffirmed September 2003, January 2007 /JC-13 Committee $59.00

JEP 133B

GUIDE FOR THE PRODUCTION AND ACQUISITION OF RADIATION-HARDNESS ASSURED MULTICHIP MODULES AND HYBRID MICROCIRCUITS: A revised and expanded publication for suppliers and users of radiation hardness assured (RHA) multichip modules (MCMs) and hybrid microcircuits, is now available. Revision A of JEP133 includes modifications to the introduction, clarification of a definition and clarification of several technical issues within the document. In addition, the Bibliography section was updated to include added references. The document provides guidance as to how to achieve, maintain and ensure required levels of radiation-hardness given the fact that the constituent dice can have different levels of hardness assurance. It also describes how to deal with the various radiation hardness situations that an MCM/Hybrid developer, procuring activity or user will encounter. The guide is intended to supplement three relevant performance specifications: MIL-PRF-38534, MIL-PRF-38535 and MIL-PRF-19500.

March 2005 September 2003 /JC-13.5 Subcommittee $59.00

JEP 134

GUIDELINES FOR PREPARING CUSTOMER-SUPPLIED BACKGROUND INFORMATION RELATING TO A SEMICONDUCTOR-DEVICE FAILURE ANALYSIS: The purpose of this Guideline is to provide

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a vehicle for acquiring and transmitting the necessary information in a concise, organized, and consistent format. Included in the Guideline is a sample form that facilitates transferring the maximum amount of background data to the failure analyst in a readily interpretable format. Immediate availability of this key information assists that analyst in completing a timely and accurate failure analysis.

September 1998 /JC-14.6 Subcommittee $45.00

JEP 136

SIGNATURE ANALYSIS: Signature Analysis is a method to reduce the number of comprehensive physical failure analyses by the application of statistical inference techniques. The purpose of this document is to promote a common definition of Signature Analysis by inference, using the same statistical techniques, and to recognize that it is formal means of doing failure analysis.

July 1999 /JC-14.6 Subcommittee $47.00

JEP 137B

COMMON FLASH INTERFACE (CFI) IDENTIFICATION CODES: This publication is a companion document to the Common Flash Interface (CFI) standard, JESD68, which outlines the device and host system software interrogation handshake. JEP137 documents ID Code assignments for: 1)) the Algorithm-specific Command Set and Control Interfaces and 2) the Device Interfaces. It is published as needed when additions are made to either of these lists of codes. To make a request for an ID Code please contact the JEDEC Office at (703)907-7558.

May 2004 /JC-42.4 Subcommittee $41.00

JEP 138

USER GUIDELINES FOR IR THERMAL IMAGING DETERMINATION OF DIE TEMPERATURE: The purpose of these user guidelines is to provide background and an example for the use of an infrared (IR) microscope to determine die temperature of electronic devices for calculations such as thermal resistance.

September 1999 /JC-25 Committee $41.00

JEP 139

GUIDELINE FOR CONSTANT TEMPERATURE AGING TO CHARACTERIZE ALUMINUM INTERCONNECT METALLIZATIONS FOR STRESS-INDUCED VOIDING: This document describes a constant temperature (isothermal) aging method for testing aluminum (Al) metallization test structures on microelectronics wafers for susceptibility to stress-induced voiding. This method is valid for metallization/dielectric systems in which the dielectric is deposited onto the metallization at a temperature considerably above the intended use temperature, and above or equal to the deposition temperature of the metal. Although this is a wafer test, it is not a fast (less than 5 minutes per probe) test. It is intended to be used for lifetime prediction and failure analysis, not for production Go-NoGo lot checking.

December 2000 /JC-14.2 Subcommittee $47.00

JEP 140

BEADED THERMOCOUPLE TEMPERATURE MEASUREMENT OF SEMICONDUCTOR PACKAGES: The beaded thermocouple temperature measurement guideline provides a procedure to accurately and consistently measure the temperature of semiconductor packages during exposure to thermal excursions. The guideline applications can include, but not limited to, temperature profile measurement in reliability test chambers and solder reflow operations that are associated with component assembly to printed wiring boards.

June 2002; Reaffirmed June 2006 /JC-14.1 Subcommittee $43.00

JEP 142

GUIDELINE FOR OBTAINING AND ACCEPTING MATERIAL FOR USE IN HYBRID / MCM PRODUCTS: This document provides guidance regarding design considerations, material assessment techniques, and recommendations for material acceptance prior to use in Hybrid / MCM Products. As part of the risk assessment process, both technical requirements and cost should be carefully considered with regard to testing / evaluating the elements of a hybrid microcircuit or Multi-chip Module (MCM) prior to material release for assembly. The intent of this document is to highlight various options that are available to the Hybrid / MCM manufacturer and provide associated guidance, not to impose a specific set of tests.

May 2002 /JC-13.5 Subcommittee $55.00

JEP 143B.01

SOLID STATE RELIABILITY ASSESSMENT QUALIFICATION METHODOLOGIES: The purpose of this publication is to provide an overview of some of the most commonly used systems and test methods historically performed by manufacturers to assess and qualify the reliability of solid state products. The appropriate references to existing and proposed JEDEC (or EIA) standards and publications are cited. This document is also intended to provide an

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educational background and overview of some of the technical and economic factors associated with assessing and qualifying microcircuit reliability.

June 2008 September 2007 /JC-14.3 Subcommittee $70.00

JEP 144

GUIDELINE FOR RESIDUAL GAS ANALYSIS (RGA) FOR MICROELECTRONIC PACKAGES The intent of this document is to give guidance on the Residual Gas Analysis (RGA) process and surrounding issues. The guideline describes how to select a suitable test lab and includes RGA history, measurement methodology, and issues that arise with the test. Interpreting the lab results along with common failure mechanisms are discussed at length along with process controls and alternative test techniques for measuring the moisture content within packages.

July 2002 /JC-13 Committee $57.00

JEP 145

GUIDELINE FOR ASSESSING THE CURRENT-CARRYING CAPABILITY OF THE LEADS IN A POWER PACKAGE SYSTEM: This publication is intended as a guideline to establish procedures, consideration and common practices that will allow a manufacturer, an application entity, a system designer and other interested parties to define current capability limitations in the leads of components and power systems with semiconductor components. This is a guideline, not a standardized method, it was developed over several years to clarify questions that had been posed to committee members in their respective engineering functions.

February 2003 /JC-25 Committee $41.00

JEP 146

GUIDELINES FOR SUPPLIER PERFORMANCE RATING: The intent of this document is to establish guidelines and provide examples by which customers can measure their suppliers based on mutually agreed upon objective criteria. These results can then be used to improve communications between customers and suppliers.

June 2003 September 2002 /JC-14.4 Subcommittee $47.00

JEP 147

PROCEDURE FOR MEASURING INPUT CAPACITANCE USING A VECTOR NETWORK ANALYZER (VNA): This procedure describes a recommended way to measure pin capacitance of devices with SSTL (Stub Series Terminated Logic) interface pins by use of a Vector Network Analyzer. One purpose of this standard procedure is to reduce the lengthy and often inaccurate footnote - usually found around the specification of pin parasitics - to a simple reference to this document. In special cases modifying statements may adjust this procedure to the special needs of certain component.

October 2003 December 2002 / Committee!33JC162 $41.00

JEP 148

RELIABILITY QUALIFICATION OF SEMICONDUCTOR DEVICES BASED ON PHYSICS OF FAILURE RISK AND OPPORTUNITY ASSESSMENT A concept is outlined, which proactively integrates qualification into the development process and provides a systematic procedure as support tool to development and gives early focus on required activities. It converts requirements for a product into measures of development and qualification in combination with a risk and opportunity assessment step and accompanies the development process as guiding and recording tool for advanced quality planning and confirmation. The collected data enlarge the knowledge database for DFR / BIR (design for reliability / building-in reliability) to be used for future projects. The procedure challenges and promotes teamwork of all involved disciplines. Based on the Physics-of-Failure (PoF) concept the reliability qualification methodology is re-arranged with regard to the relationships between design, technology, manufacturing and the different product life phases at use conditions. It makes use of the Physics-of-Failure concept by considering the potential individual failure mechanisms and relates most of the reliability aspects to the technology rather than to the individual product design. Evaluation of complex products using common reliability models and definition of sample sizes with respect to systematic inherent product properties and fractions of defects are discussed.

April 2004 January 2003 /JC-14.3 Subcommittee $63.00

JEP 149

APPLICATION THERMAL DERATING METHODOLOGIES: This publication applies to the application of integrated circuits and their associated packages in end use designs. It summarizes the methodology of thermal derating and the suitability of such methodologies.

November 2004 June 2004 /JC-14.3 Subcommittee $47.00

JEP 150

STRESS-TEST-DRIVEN QUALIFICATION OF AND FAILURE MECHANISMS ASSOCIATED WITH

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	ASSEMBLED SOLID STATE SURFACE-MOUNT COMPONENTS This publication contains a set of frequently recommended and accepted JEDEC reliability stress tests. These tests are used for qualifying new and modified technology/ process/ product families, as well as individual solid state surface-mount products, in particular leadless chip carriers, ball grid array (BGA) packages, direct chip attach die and packages with exposed pads that are attached to the PWB for thermal considerations. Assembly level testing may not be a prerequisite for device qualification; however, if the effect of assembly conditions on the component is not known, there could be reliability concerns for that component that are not evident in component level testing. As such, it is recommended that assembly level testing be performed to determine if there are any adverse effects on that component due to its assembly to a PWB. May 2005 October 2004 /JC-14.3 Subcommittee	$48.00
JEP 152	**DDR2 DIMM CLOCK SKEW MEASUREMENT PROCEDURE USING A CLOCK REFERENCE BOARD** This document is the work product of the JC-45.1 DDR2 DIMM Clock Skew Measurement task group.The purpose of this document is to define procedures to measure clock parameters on registered DIMMs using the DDR2 Clock Reference Board. It is NOT the intent of this document to set specification values or validation requirements. May 2007 February 2004 /JC-45.1 Subcommittee	$55.00
JEP 153	**CHARACTERIZATION AND MONITORING OF THERMAL STRESS TEST OVEN TEMPURATURES** This document provides an industry standard method for characterization and monitoring thermal stress test oven temperatures. The procedures described in this document should be used to insure thermal stress test conditions are being achieved and maintained during various test procedures. January 2008 June 2007 /JC-14.1 Subcommittee	$55.00
JEP 154	**GUIDELINE FOR CHARACTERIZING SOLDER BUMP ELECTROMIGRATION UNDER CONSTANT CURRENT AND TEMPERATURE STRESS** This document describes a method to test the electromigration (EM) susceptibility of solder bumps, including other types of bumps, such as solder capped copper pillars, used in flip-chip packages. The method is valid for Sn/Pb eutectic, high Pb, and Pb-free solder bumps. The document discusses the advantages and concerns associated with EM testing, as well as options for data analysis. January 2008 September 2007 /JC-14.1 Subcommittee	$70.00
JEP 155	**RECOMMENDED ESD TARGET LEVELS FOR HBM/MM QUALIFICATION** This document was written with the intent to provide information for quality organizations in both semiconductor companies and their customers to assess and make decisions on safe ESD level requirements. It will be shown through this document why realistic modifying of the ESD target levels for component level ESD is not only essential but is also urgent. The document is organized in different sections to give as many technical details as possible to support the purpose given in the abstract. August 2008 September 2007 /JC-14 Committee	$84.00
JEP 179	**DDR2 SPD Interpretation of Temperature Range and (Self-) Refresh Operation** The purpose of this document is to explain the meaning of SPD setting (JESD21 SPD section) for DDR2 SDRAM (JESD79-2) in normal and extended temperature operationy67. June 2006 March 2005 /JC-42.3 Subcommittee	$40.00
NUMBER	**EIA Standards (EIA)**	**PRICE**
EIA 236-C	**COLOR CODING OF DISCRETE SEMICONDUCTOR DEVICES:** This standard details the methods to be followed if color coding is used to identify JEDEC-assigned type numbers or for cathode identification of discrete semiconductor devices. ANSI/EIA-236-C-1986. March 1986; Reaffirmed November 1999 /JC-10 Committee	$38.00
EIA 282-A	**STANDARD FOR SILICON RECTIFIER DIODES: SEE JESD282-B** ANSI/EIA-282-A-1989 February 1990; Elevated Became JESD282-B after revision April 2000 /JC-22.2 Subcommittee	
EIA 283	**TEST METHOD FOR TRANSISTOR NOISE FIGURE MEASUREMENTS AT MEDIUM FREQUENCIES - SUPERSEDED BY EIA-311-A.**	

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November 1963; Rescinded November 1981 November 1981 /JC-25 Committee

EIA 284-A **TEST METHODS FOR THE COLLECTOR-BASE TIME CONSTANT AND FOR THE RESISTIVE PART OF THE COMMON-EMITTER INPUT IMPEDANCE: SEE JESD284A.** EIA-284-A became JESD284A after reaffirmation in October 2002.

November 1963; Reaffirmed /JC-25 Committee

EIA 286-A **STANDARD FOR MEASURING FORWARD SWITCHING CHARACTERISTICS OF SEMICONDUCTOR DIODES: SEE JESD286-B.** ANSI/EIA-286-A-1991.

February 1991; Elevated Became JESD286-B after revision February 2000 /JC-22.4 Subcommittee

EIA 302 **RANGES AND CONDITIONS FOR SPECIFYING BETA FOR LOW POWER, AUDIO FREQUENCY TRANSISTORS FOR ENTERTAINMENT SERVICE:** This standard establishes the preferred rating ranges and conditions for specifying beta for low power, audio frequency transistors intended for entertainment service.

January 1965; Reaffirmed April 1981, April 1999 /JC-25 Committee $37.00

EIA 306 **MEASUREMENT OF SMALL SIGNAL HF, VHF, AND UHF POWER GAIN OF TRANSISTORS:** This standard provides a method of measurement for small-signal HF, VHF, and UHF power gain of low power transistors.

May 1965; Reaffirmed April 1981, April 1999 /JC-25 Committee $38.00

EIA 308-A **PREPARATION OF OUTLINE DRAWINGS OF SOLID-STATE PRODUCTS FOR JEDEC TYPE REGISTRATION:** This standard is intended to serve as a guide to manufacturers of solid state products for the preparation of outline drawings of solid state product packages for JEDEC type registration.

August 1981 /JC-11 Committee $38.00

EIA 311-A **MEASUREMENT OF TRANSISTOR NOISE FIGURE AT MF, HF, AND VHF:** This standard describes a test method for measurement of transistor noise figure and effective input noise temperature at MF, HF, and VHF. This standard also adds the necessary information to make 'effective input noise temperature measurements'. This method is a revision of EIA-311 and incorporates material previously found in EIA-283.

November 1981; Reaffirmed April 1999 /JC-25 Committee $48.00

EIA 318-B **MEASUREMENT OF REVERSE RECOVERY TIME FOR SEMICONDUCTOR SIGNAL DIODES:** This standard describes the measurement of signal diodes (I_F <=500mA dc) reverse recovery times of less than 300 ns duration. It may, however, also be used for the measurement of longer recovery times. This standard is also intended to establish a method which to characterize the test fixture used for this measurement.

July 1996; Reaffirmed April 1999 /JC-22.4 Subcommittee $47.00

EIA 321-C **NUMBERING OF LIKE-NAMED TERMINAL FUNCTIONS IN SEMICONDUCTOR DEVICES AND DESIGNATION OF UNITS IN MULTIPLE-UNIT SEMICONDUCTOR DEVICES:** This standard gives the system for numbering like-named electrodes or terminal functions in semiconductor devices and for assigning numerical designations to units of multiple-unit semiconductor devices. It applies to both integrated circuits and discrete devices. ANSI/EIA-321-C-1987

February 1987; Reaffirmed November 1995 November 1995 /JC-10 Committee $41.00

EIA 323 **AIR-CONVECTION-COOLED, LIFE TEST ENVIRONMENT FOR LEAD-MOUNTED SEMICONDUCTOR DEVICES:** This standard is applicable to life testing of lead-mounted semiconductor devices intended for applications in a natural air-cooled environment where most of the power dissipation is obtained by convection and radiation losses from the body to the device.

March 1966; Reaffirmed February 1972, November 2002 November 2002 /JC-22.1 Subcommittee $40.00

EIA 340 **STANDARD FOR THE MEASUREMENT OF CRE:** This standard offers an easily measured parameter which is one of the significant characteristics in determining the stability of a transistor intended for small-signal operation. The measurement technique allows rapid testing. Its correlation to AC stability will help to establish the interchangeability of a device.

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November 1967; Reaffirmed April 1981, April 1999 /JC-25 Committee $43.00

EIA 353 **THE MEASUREMENT OF TRANSISTOR NOISE FIGURE AT FREQUENCIES UP TO 20 kHz BY SINUSOIDAL SIGNAL-GENERATOR METHOD:** This noise measurement method applies to transistors whose noise has a Gaussian power distribution, to transistors whose noise has a flat (white) power distribution, and to transistors whose noise has a l/f (power inversely proportional to frequency) power distribution.

April 1968; Reaffirmed April 1981, April 1999 /JC-25 Committee $40.00

EIA 354 **THE MEASUREMENT OF TRANSISTOR EQUIVALENT NOISE VOLTAGE AND EQUIVALENT NOISE CURRENT AT FREQUENCIES OF UP TO 20 kHz:** This standard provides a method for determining values, for device registration purposes, for transistor equivalent noise voltage and equivalent noise current at frequencies up to 20 kHz. This method is applicable to transistors whose noise has a Gaussian, flat (white) or I/f power distribution.

April 1968; Reaffirmed April 1981, April 1999 /JC-25 Committee $40.00

EIA 365 **PERFORMANCE TEST PROCEDURE FOR SOLAR CELLS AND CALIBRATION PROCEDURE FOR SOLAR CELL STANDARDS FOR SPACE VEHICLE SERVICE:** The purpose of this standard is to classify the output of solar cells for space vehicle service in accordance with requirements of EIA Format JS4-RDF4.

November 1969; Reaffirmed February 1984 / Committee!33JC231 $47.00

EIA 371 **THE MEASUREMENT OF SMALL-SIGNAL VHF-UHF TRANSISTOR SHORT-CIRCUIT FORWARD CURRENT TRANSFER RATIO:** This standard describes the method to be used for the measurement of small-signal VHF-UHF transistor short-circuit forward current transfer ratio, in preparing data sheets for JEDEC registration of low power transistors.

February 1970; Reaffirmed April 1981, April 1999 /JC-25 Committee $41.00

EIA 372 **THE MEASUREMENT OF SMALL-SIGNAL VHF-UHF TRANSISTOR ADMITTANCE PARAMETERS:** This standard describes the method to be used for the measurement of small-signal VHF-UHF transistor admittance parameters, in preparing data sheets for JEDEC registration of low power transistors.

May 1970; Reaffirmed April 1981, April 1999 /JC-25 Committee $43.00

EIA 397 **RECOMMENDED STANDARD FOR THYRISTORS:** One section of this standard presents a thorough explanation of thyristor principals, defining thedifferent classes of these devices, their Physical structure and detailing the numerous test methods and ratings required in their application to electronic and power circuitry. Another section presents a universally accepted listing of letter symbols. Considerable effort is devoted to the use of JEDEC Type Registration System as related to thyristors. This will permit the device manufacturer to employ a uniform procedure in the development of maximum rating and presentation of performance data.

June 1972 /JC-22.1 Subcommittee $177.00

EIA 397-1 **ADDENDUM No. 1 TO EIA-397:** A compilation of 12 new or revised thyristor test methods which have been adopted since the original standard was issued in 1972.

July 1980 /JC-22.1 Subcommittee $83.00

EIA 398 **MEASUREMENT OF SMALL VALUES OF TRANSISTOR CAPACITANCE:** This standard contains a three-terminal procedure for capacitance measurement with due precautions for shielding of extraneous effects due to terminal leads and metal enclosures.

July 1972; Reaffirmed April 1981, April 1999 /JC-25 Committee $43.00

EIA 428-A **TYPE DESIGNATION SYSTEM FOR MICROELECTRONIC DEVICES**

October 1988; Rescinded September 1993 September 1993 /JC-10 Committee

EIA 435 **STANDARD FOR THE MEASUREMENT OF SMALL-SIGNAL TRANSISTOR SCATTERING PARAMETERS:** This standard specifies the standard for the measurement of small-signal transistor scattering parameters.

June 1976; Reaffirmed April 1999 /JC-25 Committee $49.00

EIA 471 **SYMBOL AND LABEL FOR ELECTROSTATIC SENSITIVE DEVICES:** This standard will be useful

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to anyone engaged in handling semiconductor devices and integrated circuits that are subject to permanent damage due to electrostatic potentials. The standard establishes a symbol and label that will gain the attention of those persons who might inflict electrostatic damage to the device. The label which is placed on the lowest practical level of packaging contains the words 'ATTENTION - OBSERVE PRECAUTIONS FOR HANDLING ELECTROSTATIC SENSITIVE DEVICES'. The symbol contained in this label, which may be used on the device itself, shows a hand in a triangle with a bar through it.

February 1980; Reaffirmed October 1988, September 1996, November 1996 /JC-10 Committee $38.00

EIA 554A **Method Selection for Assessment of Nonconforming Levels in Parts Per Million (PPM)** This standard is intended to provide guidance for the selection of a method for estimating and reporting th proportion nonconforming. The PPM philosophy applies to the average quality level of a product, not to acceptance plans.

July 1996; Reaffirmed September 5, 2002 January 2006 /JC-13.2 Subcommittee $IHS

EIA 557B **STATISTICAL PROCESS CONTROL SYSTEMS:** SPC embraces a management philosophy of continuous process improvement that has a primary focus on prevention of defects. After a process has been characterized using statistical techniques (i.e., design experiments (DOE), capability studies, etc.), SPC is a tool that can be applied to control and optimize the process and reduce variability. An acceptable approach toward an SPC system involves the use of 'end-of-process' data to control the process through the application of SPC techniques. However, the intent of this standard is to emphasize the use of in-process data in order to better control and forecast system quality. This proactive use of SPC in conjunction with other techniques and the appropriate responsiveness to out-of-control situations serves to make SPC techniques critical in continuous process improvement and achieving excellence.

February 2006 /JC-13.5 Subcommittee $IHS

EIA 599-A **NATIONAL ELECTRONIC PROCESS CERTIFICATION STANDARD; GOVERNMENT CONTRACTORS:** Due to notification from the JC-14.4 subcommittee that the material contained in EIA599 has been replaced by the ISO 9000 series, the JEDEC Board of Directors, at its August 2003 meeting, approved to remove this standard from the JEDEC Free Download Area.

June 1998; Rescinded August 25, 2003 August 2003 /JC-14.4 Subcommittee

EIA 623 **PROCUREMENT QUALITY OF SOLID STATE COMPONENTS BY GOVERNMENT CONTRACTORS: RESCINDED, May 2006**

July 1994; Rescinded May 2006 January 2004 /JC-13 Committee $40.00

EIA 625 **REQUIREMENTS FOR HANDLING ELECTROSTATIC-DISCHARGE-SENSITIVE (ESDS) DEVICES (SUPERSEDES JEP108-B): SEE JESD625-A.**

November 1994; Elevated Became JESD625A after Revision December 1999 /JC-13 Committee

EIA 659 **FAILURE-MECHANISM-DRIVEN RELIABILITY MONITORING (SUPERSEDES JESD29-A): SEE JESD659-A.**

July 1996; Elevated Became JESD659A after Revision September 1999 /JC-14.3 Subcommittee

EIA 670 **QUALITY SYSTEM ASSESSMENT (SUPERSEDES JESD39-A):** This standard is used by the electronic industry for preparation of audit checklists for assessing compliance of quality systems to the requirements of ANSI/ASQC Q9001 (ISO9001), ANSI/ASQC Q9002 (ISO9002), ANSI/ASQC Q9003 (ISO9003), and ANSI/EIA599, National Electronic Process Certification Standard. It also provides a tool for quality system evaluation in accordance with the guidelines of ANSI/ASQC Q9004 (ISO9004) and the Malcolm Baldrige National Quality Award Criteria.

June 1997 /JC-14.4 Subcommittee $63.00

EIA 671 **COMPONENT PROBLEM ANALYSIS AND CORRECTIVE ACTION REQUIREMENTS: SEE JESD671-A.**

November 1996; Elevated Became JESD671A after revision December 1999 /JC-14.4 Subcommittee

JESD 370B **DESIGNATION SYSTEM FOR SEMICONDUCTOR DEVICES:** This standard includes several new

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items and has been completely rewritten from the original EIA-370. The first is a new letter symbol C so that a JEDEC type designation may now be 2C1234, to indicate that a chip is being designated that if it were properly mounted on the package registered for the 2N1234, it would display characteristics similar to those of the 2N1234. The second major addition is the method for assigning the first numeric symbol for type designations of optoelectronic devices. ANSI/EIA-370-B-1992.

February 1982; Reaffirmed November 1995, November 1999, May 2003 /JC-10 Committee $43.00

JESD 390-A **STANDARD TEST PROCEDURE FOR NOISE MARGIN MEASUREMENTS FOR SEMICONDUCTOR LOGIC GATING MICROCIRCUITS, Reaffirmed September 2003.**

February 1981; Rescinded October 2008 May 2008 /JC-13 Committee

NUMBER **Joint Industry Guide (JIG)** **PRICE**

JIG -101-A **Material Composition Declaration for Electronic Products** This document has been worked on for more than three years by member companies of EICTA (Europe), JGPSSI (Japan), EIA (USA) and JEDEC (USA). The purpose of this guide establishes the materials and substances to be disclosed by suppliers when those materials and substances are present in products and subparts that are incorporated into EEE. It benefits suppliers and their commercial customers by providing consistency and efficiency to the material declaration process. It promotes the development of consistent data exchange formats and tools that will facilitate and improve data transfer along the entire global supply chain.

September 2007 January 2002 /JC-14 Committee

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Committees

JC-10 Terms/Defin/Symbols

JESD 99B TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR MICROELECTRONIC DEVICES:

JESD 99-1 ADDENDUM No. 1 to JESD99 - TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR ANALOG-TO-DIGITAL AND DIGITAL-TO-ANALOG CONVERTERS:

JEP 104C.01 REFERENCE GUIDE TO LETTER SYMBOLS FOR SEMICONDUCTOR DEVICES:

JESD 77B.01 TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR DISCRETE SEMICONDUCTOR AND OPTOELECTRONIC DEVICES:

JESD 88C DICTIONARY OF TERMS FOR SOLID STATE TECHNOLOGY, Fourth Edition:

JESD 100B.01 TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR MICROCOMPUTERS, MICROPROCESSORS, AND MEMORY INTEGRATED CIRCUITS:

JEP 99 GLOSSARY OF MICROELECTRONIC TERMS, DEFINITIONS, AND SYMBOLS: ELEVATED TO JESD99, June 1985.

JEP 120-A INDEX OF TERMS DEFINED IN JEDEC PUBLICATIONS:

JEP 75 LETTER SYMBOLS USED WITH INFRARED DEVICES - INCORPORATED INTO JESD77-A.

JEP 100 TERMS, DEFINTIONS, AND LETTER SYMBOLS FOR MICROCOMPUTERS AND MEMORY INTEGRATED CIRCUITS: ELEVATED TO JESD100, August 1993.

JEP 103A SUGGESTED PRODUCT-DOCUMENTATION, CLASSIFICATIONS, AND DISCLAIMERS

EIA 428-A TYPE DESIGNATION SYSTEM FOR MICROELECTRONIC DEVICES

EIA 471 SYMBOL AND LABEL FOR ELECTROSTATIC SENSITIVE DEVICES:

EIA 236-C COLOR CODING OF DISCRETE SEMICONDUCTOR DEVICES:

EIA 321-C NUMBERING OF LIKE-NAMED TERMINAL FUNCTIONS IN SEMICONDUCTOR DEVICES AND DESIGNATION OF UNITS IN MULTIPLE-UNIT SEMICONDUCTOR DEVICES:

JESD 370B DESIGNATION SYSTEM FOR SEMICONDUCTOR DEVICES:

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JEB 20	ACCEPTED PRACTICES FOR MAKING MICROELECTRONIC DEVICE THERMAL CHARACTERISTICS TESTS
JEP 86-A	RECOMMENDED PRACTICE FOR DUAL DIMENSIONING
JEP 95 AUS	ANNUAL UPDATING SERVICE:
JEP 95	JEDEC REGISTERED AND STANDARD OUTLINES FOR SOLID STATE AND RELATED PRODUCTS:
JESD 95-1	DESIGN REQUIRMENTS FOR OUTLINES OF SOLID STATE AND RELATED PRODUCTS: DISCONTINUED AS A SEPARATE ITEM CONTAINED IN JEP95, BOOK 1, SECTION 4.
JESD 30E	DESCRIPTIVE DESIGNATION SYSTEM FOR SEMICONDUCTOR-DEVICE PACKAGES:

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JESD 16-A	ASSESSMENT OF AVERAGE OUTGOING QUALITY LEVELS IN PARTS PER MILLION (PPM):
JESD 19	GENERAL STANDARD FOR STATISTICAL PROCESS CONTROL (SPC) - SUPERSEDED by EIA-557-A
JESD 40	PROCUREMENT QUALITY OF SOLID STATE COMPONENTS BY GOVERNMENT CONTRACTORS - SUPERSEDED BY EIA-623, July 1994
JESD 42	REQUIREMENTS FOR HANDLING ELECTROSTATIC-DISCHARGE-SENSITIVE (ESDS) DEVICES - SUPERSEDED BY EIA-625, November 1994.
JESD 49A	PROCUREMENT STANDARD FOR KNOWN GOOD DIE (KGD):
JEP 132	PROCESS CHARACTERIZATION GUIDELINE:
JEP 109-C	GENERAL REQUIREMENTS FOR DISTRIBUTORS OF MILITARY SEMICONDUCTOR DEVICES:
JEP 112	TEST METHOD FOR QUALIFICATION AND ACCEPTANCE OF CIRCUIT SUPPORT FILMS FOR USE IN MICROELECTRONIC APPLICATIONS - SUPERSEDED BY JESD72, June 2001
EIA 623	PROCUREMENT QUALITY OF SOLID STATE COMPONENTS BY GOVERNMENT CONTRACTORS: RESCINDED, May 2006
EIA 625	REQUIREMENTS FOR HANDLING ELECTROSTATIC-DISCHARGE-SENSITIVE (ESDS) DEVICES (SUPERSEDES JEP108-B): SEE JESD625-A.
JESD 390-A	STANDARD TEST PROCEDURE FOR NOISE MARGIN MEASUREMENTS FOR SEMICONDUCTOR LOGIC GATING MICROCIRCUITS, Reaffirmed September 2003.
JEP 144	GUIDELINE FOR RESIDUAL GAS ANALYSIS (RGA) FOR MICROELECTRONIC PACKAGES

JC-13.2 Microelec. Devices

EIA 554A	Method Selection for Assessment of Nonconforming Levels in Parts Per Million (PPM)
JEP 101-C	JEDEC REQUIREMENTS FOR CLASS B MICROCIRCUITS: RESCINDED, May 2006
JEP 111	TEST PROCEDURES FOR CUSTOM MONOLITHIC MICROCIRCUITS - SUPERSEDED BY MIL-PRF-38535C.
JEP 121A	REQUIREMENTS FOR MICROELECTRONIC SCREENING AND TEST OPTIMIZATION:
JESD 53	MANAGEMENT OF COMPONENT OBSOLESCENCE BY GOVERNMENT CONTRACTORS: RESCINDED, October 2002
JESD 26-A	GENERAL SPECIFICATION FOR PLASTIC ENCAPSULATED MICROCIRCUITS FOR USE IN RUGGED APPLICATIONS - RESCINDED, July 2001

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JESD 57 TEST PROCEDURE FOR THE MANAGEMENT OF SINGLE-EVENT EFFECTS IN SEMICONDUCTOR DEVICES FROM HEAVY ION IRRADIATION:

JESD 89A MEASUREMENT AND REPORTING OF ALPHA PARTICLE AND TERRESTRIAL COSMIC RAY INDUCED SOFT ERRORS IN SEMICONDUCTOR DEVICES:

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JESD 93 HYBRIDS/MCM

JESD 27 CERAMIC PACKAGE SPECIFICATION FOR MICROELECTRONIC PACKAGES:

JESD 9-A METAL PACKAGE SPECIFICATION FOR MICROELECTRONIC PACKAGES AND COVERS:

JEP 142 GUIDELINE FOR OBTAINING AND ACCEPTING MATERIAL FOR USE IN HYBRID / MCM PRODUCTS:

JESD 72 TEST METHODS AND ACCEPTANCE PROCEDURES FOR THE EVALUATION OF POLYMERIC MATERIALS:

JEP 114.01 GUIDELINES FOR PARTICLE IMPACT NOISE DETECTION (PIND) TESTING, OPERATOR TRAINING, AND CERTIFICATION:

JEP 133B GUIDE FOR THE PRODUCTION AND ACQUISITION OF RADIATION-HARDNESS ASSURED MULTICHIP MODULES AND HYBRID MICROCIRCUITS:

JEP 96 GUIDELINES FOR NONDESTRUCTIVE PULL TESTING OF WIRE BONDS ON HYBRID DEVICES

JEP 105 JEDEC GUIDELINE FOR THE CHARACTERIZATION OF HYBRID POLYMERIC MATERIALS - SUPERSEDED BY JESD72, June 2001

JEP 107 TEST METHOD FOR QUALIFICATION AND ACCEPTANCE OF PARTICLE GETTERS FOR USE IN HYBRID MICROELECTRONIC APPLICATIONS - SUPERSEDED BY JESD72, June 2001

EIA 557B STATISTICAL PROCESS CONTROL SYSTEMS:

JC-14 Quality/Reliability

JEB 16 USER GUIDE FOR MICROCIRCUIT FAILURE ANALYSIS:

JEP 155 RECOMMENDED ESD TARGET LEVELS FOR HBM/MM QUALIFICATION

JIG -101-A Material Composition Declaration for Electronic Products

JESD JIG-101 Material Composition Declaration Guide for Electronic Products

JC-14.1 Rel.Test Meth.Pkg.Dev.

JESD 22-B112 HIGH TEMPERATURE PACKAGE WARPAGE MEASUREMENT METHODOLOGY

JESD 22-A121A MEASURING WHISKER GROWTH ON TIN AND TIN ALLOY SURFACE FINISHES

JS 9702 MONOTONIC BEND CHARACTERIZATION OF BOARD-LEVEL INTERCONNECTS (IPC/JEDEC-9702)

JESD 89-2A TEST METHOD FOR ALPHA SOURCE ACCELERATED SOFT ERROR RATE:

JESD 22-A119 LOW TEMPERATURE STORAGE LIFE

JS 9704 Printed Wiring Board (PWB) Strain Gage Test Guideline

J-STD- 002B SOLDERABILITY TESTS FOR COMPONENT LEADS, TERMINATIONS, LUGS, TERMINALS AND WIRES:

JESD 22-B113 BOARD LEVEL CYCLIC BEND TEST METHOD FOR INTERCONNECT RELIABILITY CHARACTERIZATION OF COMPONENTS FOR HANDHELD ELECTRONIC PRODUCTS

JESD 22-B111 BOARD LEVEL DROP TEST METHOD OF COMPONENTS FOR HANDHELD ELECTRONIC PRODUCTS:

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JESD 22-A105C POWER AND TEMPERATURE CYCLING:

JESD 97 MARKING, SYMBOLS, AND LABELS FOR IDENTIFICATION OF LEAD (Pb) FREE ASSEMBLIES, COMPONENTS, AND DEVICES - SUPERSEDED BY J-STD-609, August 2007

JESD 22-A111 EVALUATION PROCEDURE FOR DETERMINING CAPABILITY TO BOTTOM SIDE BOARD ATTACH BY FULL BODY SOLDER IMMERSION OF SMALL SURFACE MOUNT SOLID STATE DEVICES:

JESD 89-1A TEST METHOD FOR REAL-TIME SOFT ERROR RATE:

JESD 89-3A TEST METHOD FOR BEAM ACCELERATED SOFT ERROR RATE

JEP 113-B SYMBOL AND LABELS FOR MOISTURE-SENSITIVE DEVICES:

JEP 122D FAILURE MECHANISMS AND MODELS FOR SEMICONDUCTOR DEVICES:

JESD 22-A100C CYCLED TEMPERATURE HUMIDITY BIAS LIFE TEST:

JESD 22-A101-B STEADY-STATE TEMPERATURE HUMIDITY BIAS LIFE TEST:

JESD 22-A102-C ACCELERATED MOISTURE RESISTANCE - UNBIASED AUTOCLAVE:

JESD 22-A103C HIGH TEMPERATURE STORAGE LIFE:

JESD 22-A104C TEMPERATURE CYCLING:

JESD 22-A106B THERMAL SHOCK:

JESD 22-A107B SALT ATMOSPHERE:

JESD 22-A109-A HERMETICITY:

JESD 22-A110-B HIGHLY ACCELERATED TEMPERATURE AND HUMIDITY STRESS TEST (HAST)

JESD 22-A112-A MOISTURE-INDUCED STRESS SENSITIVITY FOR PLASTIC SURFACE MOUNT DEVICES - SUPERSEDED BY J-STD-020A, April 1999.

JESD 22-A113F PRECONDITIONING OF PLASTIC SURFACE MOUNT DEVICES PRIOR TO RELIABILITY TESTING:

JESD 22-A114E ELECTROSTATIC DISCHARGE (ESD) SENSITIVITY TESTING HUMAN BODY MODEL (HBM):

JESD 22-A115-A ELECTROSTATIC DISCHARGE (ESD) SENSITIVITY TESTING MACHINE MODEL (MM):

JESD 22-B100B PHYSICAL DIMENSION:

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JESD 22-B104C MECHANICAL SHOCK:

JESD 22-B105C LEAD INTEGRITY:

JESD 22-B106D RESISTANCE TO SOLDER SHOCK FOR THROUGH-HOLE MOUNTED DEVICES:

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JESD 22-C100-A	HIGH TEMPERATURE CONTINUITY - RESCINDED, November 1999
JESD 22-C101D	FIELD-INDUCED CHARGED-DEVICE MODEL TEST METHOD FOR ELECTROSTATIC DISCHARGE WITHSTAND THRESHOLDS OF MICROELECTRONIC COMPONENTS:
J-STD-020D.01	JOINT IPC/JEDEC STANDARD FOR MOISTURE/REFLOW SENSITIVITY CLASSIFICATION FOR NONHERMETIC SOLID STATE SURFACE-MOUNT DEVICES:
J-STD- 033B.1	JOINT IPC/JEDEC STANDARD FOR HANDLING, PACKING, SHIPPING AND USE OF MOISTURE/REFLOW SENSITIVE SURFACE-MOUNT DEVICES:
JEP 108-B	DISTRIBUTOR REQUIREMENTS FOR HANDLING ELECTROSTATIC -DISCHARGE SENSITIVE (ESDS) DEVICES: SUPERSEDED BY JESD42, March 1994.
JP 002	CURRENT TIN WHISKERS THEORY AND MITIGATION PRACTICES GUIDELINE
JESD 22-B115	SOLDER BALL PULL
JESD 22-A122	POWER CYCLING
JEP 153	CHARACTERIZATION AND MONITORING OF THERMAL STRESS TEST OVEN TEMPURATURES
JEP 154	GUIDELINE FOR CHARACTERIZING SOLDER BUMP ELECTROMIGRATION UNDER CONSTANT CURRENT AND TEMPERATURE STRESS
JESD 22-A118	ACCELERATED MOISTURE RESISTANCE - UNBIASED HAST:
JESD 22-A108C	TEMPERATURE, BIAS, AND OPERATING LIFE:
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JESD 22-B109	FLIP CHIP TENSILE PULL:
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	RESISTANCE TO DETERMINE THE TEMPERATURE OF A METALLIZATION LINE:
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JESD 201A	ENVIRONMENTAL ACCEPTANCE REQUIREMENTS FOR TIN WHISKER SUSCEPTIBILITY OF TIN AND TIN ALLOY SURFACE FINISHED:
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JEP 148	RELIABILITY QUALIFICATION OF SEMICONDUCTOR DEVICES BASED ON PHYSICS OF FAILURE RISK AND OPPORTUNITY ASSESSMENT
JESD 50B.01	SPECIAL REQUIREMENTS FOR MAVERICK PRODUCT ELIMINATION AND OUTLIER MANAGEMENT
JESD 659B	FAILURE-MECHANISM-DRIVEN RELIABILITY MONITORING:
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JESD 29-A	FAILURE-MECHANISM-DRIVEN RELIABILITY MONITORING - SUPERSEDED BY EIA/ANSI-659, July 1996.
JESD 86	ELECTRICAL PARAMETERS ASSESSMENT:
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JEP 143B.01	SOLID STATE RELIABILITY ASSESSMENT QUALIFICATION METHODOLOGIES:
JESD 69B	INFORMATION REQUIREMENTS FOR THE QUALIFICATION OF SILICON DEVICES:

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JESD 74A EARLY LIFE FAILURE RATE CALCULATION PROCEDURE FOR SEMICONDUCTOR COMPONENTS:

JESD 22-A117A ELECTRICALLY ERASABLE PROGRAMMABLE ROM (EEPROM) PROGRAM/ERASE ENDURANCE AND DATA RETENTION TEST:

EIA 659 FAILURE-MECHANISM-DRIVEN RELIABILITY MONITORING (SUPERSEDES JESD29-A): SEE JESD659-A.

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EIA 670 QUALITY SYSTEM ASSESSMENT (SUPERSEDES JESD39-A):

EIA 671 COMPONENT PROBLEM ANALYSIS AND CORRECTIVE ACTION REQUIREMENTS: SEE JESD671-A.

EIA 599-A NATIONAL ELECTRONIC PROCESS CERTIFICATION STANDARD; GOVERNMENT CONTRACTORS:

JEP 130A GUIDELINES FOR PACKING AND LABELING OF INTEGRATED CIRCUITS IN UNIT CONTAINER PACKING:

JEP 70-B QUALITY AND RELIABILITY STANDARDS AND PUBLICATIONS:

JEP 117 GUIDELINES FOR USER NOTIFICATION OF PRODUCT/PROCESS CHANGES BY SEMICONDUCTOR SUPPLIERS - SUPERSEDED BY JESD46, August 1997.

JEP 124 GUIDELINES FOR THE PACKING, HANDLING, AND REPACKING OF MOISTURE-SENSITIVE COMPONENTS - SUPERSEDED BY J-STD-033, May 1999.

JESD 671-A COMPONENT QUALITY PROBLEM ANALYSIS AND CORRECTIVE ACTION REQUIREMENTS (INCLUDING ADMINISTRATIVE QUALITY PROBLEMS):

JESD 31C GENERAL REQUIREMENTS FOR DISTRIBUTORS OF COMMERCIAL AND MILITARY SEMICONDUCTOR DEVICES:

JESD 48B PRODUCT DISCONTINUANCE:

JESD 46C CUSTOMER NOTIFICATION OF PRODUCT/PROCESS CHANGES BY SEMICONDUCTOR SUPPLIERS:

JESD 39-A QUALITY SYSTEM ASSESSMENT - SUPERSEDED BY ANSI/EIA-670, June 1997.

JESD 43 COMPONENT PROBLEM ANALYSIS AND CORRECTIVE ACTION REQUIREMENTS - SUPERSEDED BY EIA-671, November 1996.

JEP 146 GUIDELINES FOR SUPPLIER PERFORMANCE RATING:

J-STD- 609 MARKING AND LABELING OF COMPONENTS, PCBs AND PCBAs TO IDENTIFY LEAD (Pb), Pb-FREE AND OTHER ATTRIBUTES

JC-14.6 Failure Analysis

JESD 38 STANDARD FOR FAILURE ANALYSIS REPORT FORMAT:

JEP 134 GUIDELINES FOR PREPARING CUSTOMER-SUPPLIED BACKGROUND INFORMATION RELATING TO A SEMICONDUCTOR-DEVICE FAILURE ANALYSIS:

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JEP 118 GUIDELINES FOR GaAs MMIC AND FET LIFE TESTING:

JEP 110 GUIDELINES FOR THE MEASUREMENT OF THERMAL RESISTANCE OF GaAs FETS:

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JESD 15-4	DELPHI COMPACT THERMAL MODEL GUIDELINE

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JESD 15-1	COMPACT THERMAL MODEL OVERVIEW
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JESD 15	THERMAL MODELING OVERVIEW
JEP 131A	PROCESS FAILURE MODE AND EFFECTS ANALYSIS (FMEA):
JEP 129	THERMAL TEST CHIP GUIDELINE (WIRE BOND TYPE CHIP)- SUPERSEDED BY JESD51-4, September 1997.
JESD 51	METHODOLOGY FOR THE THERMAL MEASUREMENT OF COMPONENT PACKAGES (SINGLE SEMICONDUCTOR DEVICE)
JESD 51- 1	INTEGRATED CIRCUIT THERMAL MEASUREMENT METHOD - ELECTRICAL TEST METHOD (SINGLE SEMICONDUCTOR DEVICE):
JESD 51- 2A	INTEGRATED CIRCUITS THERMAL TEST METHOD ENVIRONMENTAL CONDITIONS - NATURAL CONVECTION (STILL AIR):
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JESD 51- 4	THERMAL TEST CHIP GUIDELINE (WIRE BOND TYPE CHIP):
JESD 51- 5	EXTENSION OF THERMAL TEST BOARD STANDARDS FOR PACKAGES WITH DIRECT THERMAL ATTACHMENT MECHANISMS:
JESD 51- 6	INTEGRATED CIRCUIT THERMAL TEST METHOD ENVIRONMENTAL CONDITIONS - FORCED CONVECTION (MOVING AIR):
JESD 51- 7	HIGH EFFECTIVE THERMAL CONDUCTIVITY TEST BOARD FOR LEADED SURFACE MOUNT PACKAGES:
JESD 51- 8	INTEGRATED CIRCUIT THERMAL TEST METHOD ENVIRONMENTAL CONDITIONS - JUNCTION-TO-BOARD:
JESD 51- 9	TEST BOARDS FOR AREA ARRAY SURFACE MOUNT PACKAGE THERMAL MEASUREMENTS:
JESD 51-10	TEST BOARDS FOR THROUGH-HOLE PERIMETER LEADED PACKAGE THERMAL MEASUREMENTS:
JESD 51-11	TEST BOARDS FOR THROUGH-HOLE AREA ARRAY LEADED PACKAGE THERMAL MEASUREMENT:

JC-15.2 Elec. Char. Tech.

JESD 59	BOND WIRE MODELING STANDARD:
JEP 126	GUIDELINE FOR DEVELOPING AND DOCUMENTING PACKAGE ELECTRICAL MODELS DERIVED FROM COMPUTATIONAL ANALYSIS:
JEP 123	GUIDELINE FOR MEASUREMENT OF ELECTRONIC PACKAGE INDUCTANCE AND CAPACITANCE MODEL PARAMETERS:

JC-16 Elec. Intrfcs/Pwr Supply

JESD 8- 1	ADDENDUM No. 1 to JESD8: INTERFACE STANDARD FOR LOW VOLTAGE TTL-COMPATIBLE (LVTTL) VLSI DIGITAL CIRCUITS
JESD 8- 2	ADDENDUM No. 2 to JESD8 - STANDARD FOR OPERATING VOLTAGES AND INTERFACE LEVELS FOR LOW VOLTAGE EMITTER-COUPLED LOGIC (ECL) INTEGRATED CIRCUITS:
JESD 8- 3A	ADDENDUM No. 3A to JESD8 - GUNNING TRANSCEIVER LOGIC (GTL) LOW-LEVEL, HIGH-SPEED INTERFACE STANDARD FOR DIGITAL INTEGRATED CIRCUITS:

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JESD 8- 4 ADDENDUM No. 4 to JESD8 - CENTER-TAP-TERMINATED (CTT) INTERFACE LOW-LEVEL, HIGH-SPEED INTERFACE STANDARD FOR DIGITAL INTEGRATED CIRCUITS:

JESD 8- 5A.01 ADDENDUM No. 5 to JESD8 - 2.5 V 0.2 V (NORMAL RANGE), AND 1.8 V TO 2.7 V (WIDE RANGE) POWER SUPPLY VOLTAGE AND INTERFACE STANDARD FOR NONTERMINATED DIGITAL INTEGRATED CIRCUIT:

JESD 8- 6 ADDENDUM No. 6 to JESD8 - HIGH SPEED TRANSCEIVER LOGIC (HSTL)- A 1.5 V OUTPUT BUFFER SUPPLY VOLTAGE BASED INTERFACE STANDARD FOR DIGITAL INTEGRATED CIRCUITS:

JESD 8- 7A ADDENDUM No. 7 to JESD8 - 1.8 V + -0.15 V (NORMAL RANGE), AND 1.2 V - 1.95 V (WIDE RANGE) POWER SUPPLY VOLTAGE AND INTERFACE STANDARD FOR NONTERMINATED DIGITAL INTEGRATED CIRCUIT:

JESD 8- 8 ADDENDUM No. 8 to JESD8 - STUB SERIES TERMINATED LOGIC FOR 3.3 VOLTS (SSTL_3) A 3.3 V VOLTAGE BASED INTERFACE STANDARD FOR DIGITAL INTEGRATED CIRCUITS:

JESD 8- 9B ADDENDUM No. 9B to JESD8 - STUB SERIES TERMINATED LOGIC FOR 2.5 VOLTS (SSTL_2): Includes Errata and Corrected Page 7 as of October 18, 2002.

JESD 8-12A.01 1.2 V +/- 0.1 V (NORMAL RANGE) AND 0.8 - 1.3 V (WIDE RANGE) POWER SUPPLY VOLTAGE AND INTERFACE STANDARD FOR NONTERMINATED DIGITAL INTEGRATED CIRCUITS:

JESD 8-14A.01 1.0 V +/- 0.1 V (NORMAL RANGE) AND 0.7 V - 1.1 V (WIDE RANGE) POWER SUPPLY VOLTAGE AND INTERFACE STANDARD FOR NONTERMINATED DIGITAL INTEGRATED CIRCUITS:

JESD 8-13 SCALABLE LOW-VOLTAGE SIGNALING FOR 400 MV (SLVS-400):

JESD 8-11A.01 ADDENDUM No. 11A.01 to JESD8 - 1.5 V +/- 0.1 V (NORMAL RANGE) AND 0.9 - 1.6 V (WIDE RANGE) POWER SUPPLY VOLTAGE AND INTERFACE STANDARD FOR NONTERMINATED DIGITAL INTEGRATED CIRCUITS:

JESD 67 I/O DRIVERS AND RECEIVERS WITH CONFIGURABLE COMMUNICATION VOLTAGE, IMPEDANCE, AND RECEIVER THRESHOLD:

JESD 8- 1-A INTERFACE STANDARD FOR NOMINAL 0.3 V/3.3 V SUPPLY DIGITAL INTEGRATED CIRCUITS

JESD 8C.01 INTERFACE STANDARD FOR NOMINAL 3.0 V/3.3 V SUPPLY DIGITAL INTEGRATED CIRCUITS:

JESD 8-18A FBDIMM SPECIFICATION: HIGH SPEED DIFFERENTIAL PTP LINK AT 1.5 V

JESD 204A SERIAL INTERFACE FOR DATA CONVERTERS

JESD 8-17 DRIVER SPECIFICATIONS FOR 1.8 V POWER SUPPLY POINT-TO-POINT DRIVERS

JESD 8-15A STUB SERIES TERMINATED LOGIC FOR 1.8 V (SSTL_18):

JESD 8-16A BUS INTERCONNECT LOGIC (BIC) FOR 1.2 V

JESD 8-19 POD18 - 1.8 V Pseudo Open Drain I/O

JESD 8-20 POD15 - 1.5 V Pseudo Open Drain I/O

JC-22.1 Thyristors

EIA 397 RECOMMENDED STANDARD FOR THYRISTORS:

JESD 41 REVERSE RECOVERY CHARACTERISTICS OF SILICON DIODES: Rescinded June 2002.

JEP 88 THERMAL RESISTANCE AND THERMAL IMPEDANCE TEST METHODS FOR STUD AND BASE-MOUNTED RECTIFIER DIODES AND THYRISTORS

EIA 323 AIR-CONVECTION-COOLED, LIFE TEST ENVIRONMENT FOR LEAD-MOUNTED SEMICONDUCTOR DEVICES:

EIA 397-1 ADDENDUM No. 1 TO EIA-397:

JC-22.2 Rectifier Diodes

EIA 282-A STANDARD FOR SILICON RECTIFIER DIODES: SEE JESD282-B

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JESD 45	MEASUREMENT METHOD FOR THERMAL RESISTANCE OF BRIDGE RECTIFIER ASSEMBLIES: RESCINDED, June 2002. Replaced by JESD282-B.
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Lugs	**J-STD- 002B**
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Master	**JEP 95 Index**
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Moisture-Induced	**JESD 22-A112-A**
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NAND	**MO 259-A**
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PSO-N	**MO 241-B**
PSO-N/PQFN	**JESD 75-6**
PSOF	**TO 270C**
PSOF-2	**DO 220-B**
PSRAM	**PSRAM 3_08** **MCP 3_12_01** **MCP 3_12_03**
PTH	**JESD 22-B106D**
PTP Link	**JESD 8-18A**
Pull	**JESD 22-B115**
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Quad Flat Pack	**CO 011-B** **CO 012-C**
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Quick Reference Guide	JEB 15
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Real-Time	**JESD 89-1A**
Receiver Type	**JESD 67**
Receiving Inspection	**EIA 623**
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Reflow	**J-STD- 020D.01** **J-STD- 033B.1**
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Reliability Monitoring - Electrostatic-Discharge Sensitive Devices	**JESD 625-A**
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Retangular	**MO 261A**
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Reverse Recovery Time - Measurement of	**JESD 24-10**
Reverse Recovery Time - Signal Diodes	**EIA 318-B**
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RFIC	**JESD 207**
RFID	**MO 283B**
RL-PLGA	**MO 277A**
	MO 278A
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Round Lead	**DO 204B-D**
RT-PLGA	**MO 279A**
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Salt Atmosphere	**JESD 22-A107B**
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Scope	JM 18L
Screening	JEP 121A JESD 22-A103C
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Screw Mount	MO 253-B
SDR	MODULE 4_5_11 MCP 3_12_01
SDRAM	JESD 79-3C JESD 208 SPD 4_01_02_11 MODULE 4_20_10 MODULE 4_20_12 SDRAM 3_11_02 SDRAM 3_11_03 SDRAM 3_11_04 SDRAM 3_11_05TOC SPD 4_01_02_04 SPD 4_01_02_09 MODULE 4_4_8 MODULE 4_5_2 MODULE 4_5_6 MODULE 4_05_10 MODULE 4_5_11 MODULE 4_5_13 MODULE 4_5_07 JESD 79F MODULE 4_20_06 JESD 82-6A MO 237G SO 001B MODULE 4_05_14 MODULE 4_20_08 MODULE 4_20_18 JESD 79-2E MODULE 4_20_09 SPD 4_01_02_10 JESD 8-17 JESD 209 MO 281A SO 006B SDRAM 3_11_05_01 MO 290A SDRAM 3_11_05_05 MODULE 4_20_16 SDRAM 3_11_05_04 SDRAM 3_11_05_02 SDRAM 3_11_05_03 MODULE 4_20_19 MODULE 4_20_13 MO 269E MODULE 4_20_11
SDRAM. SPD	SPD 4_01_02_05
Seatin Plane	JESD 22-B108A
Semiconductor	JEP 104C.01
Semiconductor Device Failure	JEP 134
Semiconductor Devices - Designation System	JESD 370B
Semiconductor Power Control Modules - SPCM	JESD 14
Semiconductor Suppliers - User Notification	JESD 46C
Semicustom Design - ASIC	JEP 116
Semicustom Integrated Circuits	JESD 12-1B JESD 12-6

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Senselines	**JESD 82-22**
Sensitivity Testing	**JESD 22-A114E** **JESD 22-A115-A**
Sequence Order	**MCP 3_12_03**
SER	**JESD 89-1A** **JESD 89-2A** **JESD 89-3A**
Serial	**SPD 4_01_02_11** **SPD 4_01_02** **SPD 4_01_02_10**
Serial Data	**DRAM 3_09_05**
Serial Interface	**JESD 204A**
Serial Presence	**SPD 4_01_02_09** **SPD 4_01_03**
SGRAM	**MODULE 4_5_09** **SDRAM 3_11_05_08** **SDRAM 3_11_05_06** **SDRAM 3_11_05_07** **JESD 8-19** **JESD 8-20**
SGRAM/SDRAM	**MODULE 4_5_8**
Shear	**JESD 22-B117A**
Shelf life	**J-STD- 033B.1**
Shipping	**J-STD- 033B.1** **CO 010-E** **CO 011-B** **CO 012-C** **CO 015-B** **CO 016-B** **CO 030-A** **CO 031-A** **CO 032-A** **CO 033-A** **CO 034-D** **CS 002-A** **CS 003-B** **CS 004-B** **CS 005-B** **CS 008-A** **Design 4.10D** **CO 034-C** **CO 029-H**
Short Circuit Withstand Time	**JESD 24- 9**
Shrink	**GS 003C** **MO 137D**
Signal Diodes	**EIA 318-B** **EIA 435** **JESD 531**
Signal Names	**JESD 100B.01**
Signature Analysis	**JEP 136**
Silicon Diodes - Reverse Recovery Characteristics	**JESD 41**
Silicon Pad	**MCP 3_12_03**
SIMM	**MODULE 4_4_1** **MODULE 4_4_2** **MODULE 4_4_7**
Single	**MO 231-A**
Single Interconnect Array	**MO 270B**
Single Semiconductor Device	**JESD 51** **JESD 51- 1**
Single-Event Effects - SEE	**JESD 57**

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Singly Right - Censored Data	JESD 37
Sinusoidal Signal-Generator Method	EIA 353
SIV	JEP 139 JESD 87
Sixteen Byte	MODULE 4_6
Skew	JEP 152
Skew Specification	JESD 65B
SKT	SO 013A
SLVS	JESD 8-13
Small	MO 286-A MO 287-A MO 288-A MO 271A DO 215-D MO 059-B Design 4.15B MS 024H MO 229-D DO 219-B MO 137D MO 236-B MO 224E DO 220-B MO 259-A MO 274A
Small Outline	DO 221A DO 222A SO 008A CO 032-A MS 012F MS 013E MO 230-A MO 187-E MODULE 4_20_18 MO 249-A MO 252-C MO 255-B TO 278B TO 277A MO 272A
Small Scale	Design 4.20D
Small Signal - Preferred Values	JESD 482-A
Small Signal Transistors	JESD 25
Small Signal VHF-UHF	EIA 371 EIA 372
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SMD	J-STD- 033B.1
SMT	SO 014A
SMT DIMM	GS 006-A
Sn whisker theory	JP 002
SO	MO 224E
SO-004	MO 260C
SO-CDIMM	JESD 82-21
SO-DIMM	SO 008A MODULE 4_4_4 MODULE 4_5_5 MODULE 4_5_6 MODULE 4_5_09 MODULE 4_20_03 MODULE 4_5_8

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	MODULE 4_20_18
	MODULE 4_20_16
Socket	**SO 014A**
	SO 008A
	SO 009A
	SO 011A
	SO 001B
	GS 007-A
	GS 004A
	SO 002B
	SO 012A
	SO 003B
	SO 013A
	SO 005A
	SO 007B
Socket Outline	**SO 006B**
SODIMM	**MODULE 4_20_18**
	MO 224E
	MO 274A
	MODULE 4_20_16
	MO 268C
	MODULE 4_20_11
soft error	**JESD 89-2A**
Soft Error Rate	**JESD 89A**
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SOIC	**MO 286-A**
	MO 271A
	MS 012F
	MS 013E
	MS 024H
	MO 137D
	MO 272A
SOJ	**CO 032-A**
	Design 4.13
Solar Cells	**EIA 365**
Solder	**JESD 22-B115**
	JESD 22-B117A
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Solder Wave	**JESD 22-B106D**
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Solderability Testing - Dip and Look	**JESD 22-B102E**
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	MS 012F
	MS 013E
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	MO 259-A
SOT	**TO 261-C**
Space Vehicle Service	**EIA 365**
SPC System	**EIA 557B**
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	SPD 4_01_02
	SPD 4_01_02_01

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sport	JESD 50B.01
Square	MO 294A
	MO 273A
	MO 270B
	MO 156-C
	MO 192-F
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	MO 228-A
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	Design 4.20D
	MO 275-A
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	SRAM 3_7
	SRAM 3_7_1
	SRAM 3_7_4
	SRAM 3_07_05
	MODULE 4_4_1
	MCP 3_12_01
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	SRAM 3_07_08
	SRAM 3_07_07
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SSOP	MO 153-F
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SSTL - SSTL_2	JESD 8- 9B
SSTL_18	JESD 8-15A
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	JESD 82-12A
SSTL_2	JESD 82-2
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SSTL_3	JESD 8- 8
SSTU	JESD 82-26
	JESD 82-23
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	JESD 82-16A
SSTU32864	JESD 82-7A
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SSTU32866	**JESD 82-10A**
SSTU32D868	**JESD 82-14A**
SSTU32D869	**JESD 82-12A**
SSTU32S868	**JESD 82-14A**
SSTU32S869	**JESD 82-12A**
SSTUA	**JESD 82-23**
SSTUA32865	**JESD 82-19A**
SSTUA32866	**JESD 82-16A**
SSTUA32D865	**JESD 82-19A**
SSTUA32D868	**JESD 82-17**
SSTUA32S865	**JESD 82-19A**
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SSTUB	**JESD 82-26** **JESD 82-25** **JESD 82-24**
SSTUB32869	**JESD 82-27**
SSTV	**JESD 82-2**
SSTV16857	**JESD 82-3B**
SSTV16859	**JESD 82-4B**
SSTV32852	**JESD 82-6A**
SSTVN16859	**JESD 82-13A**
Stackable	**MO 266B**
Stacked	**JESD 82-6A** **MO 238-A** **MO 242c** **MCP 3_12_02** **PR N07-SM1** **MO 264A**
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Stacking Module	**Design 4.21A**
Staggered	**MO 247D** **Design 4.19D** **MO 257-B** **MO 292A** **MO 267B**
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Strain gage test	**JS 9704**
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Stress Sensitivity	**JESD 22-A112-A**
Stress Test	**JESD 22-A110-B**
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Super	**MO 288-A**
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EIA 283 TEST METHOD FOR TRANSISTOR NOISE FIGURE MEASUREMENTS AT MEDIUM FREQUENCIES - SUPERSEDED BY EIA-311-A.
November 1963; Rescinded November 1981

EIA 318-1 ADDENDUM No. 1 to EIA-318 - CHARACTERIZATION OF A REVERSE TEST FIXTURE: SUPERSEDED BY EIA-318-B, July 1996.
February 1981; Rescinded

JESD 390-A STANDARD TEST PROCEDURE FOR NOISE MARGIN MEASUREMENTS FOR SEMICONDUCTOR LOGIC GATING MICROCIRCUITS, Reaffirmed September 2003.
February 1981; Rescinded May 2008

EIA 428-A TYPE DESIGNATION SYSTEM FOR MICROELECTRONIC DEVICES
October 1988; Rescinded September 1993

EIA 599-A NATIONAL ELECTRONIC PROCESS CERTIFICATION STANDARD; GOVERNMENT CONTRACTORS:
June 1998; Rescinded August 2003

EIA 623 PROCUREMENT QUALITY OF SOLID STATE COMPONENTS BY GOVERNMENT CONTRACTORS: RESCINDED, May 2006
July 1994; Rescinded January 2004

JEB 16 USER GUIDE FOR MICROCIRCUIT FAILURE ANALYSIS:
July 1970; Rescinded September 2003

JEB 17 USER GUIDELINES FOR QUALITY AND RELIABILITY ASSURANCE OF LSI COMPONENTS
November 1970; Rescinded April 1987

JEB 20 ACCEPTED PRACTICES FOR MAKING MICROELECTRONIC DEVICE THERMAL CHARACTERISTICS TESTS
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JEB 6 STANDARD MEASURMENTS OF THE ELECTRICAL CHARACTERISTICS OF SEMICONDUCTOR INTEGRATED CIRCUITS
December 1966; Rescinded

JEP 100 TERMS, DEFINTIONS, AND LETTER SYMBOLS FOR MICROCOMPUTERS AND MEMORY INTEGRATED CIRCUITS: ELEVATED TO JESD100, August 1993.
September 1979; Rescinded October 1983

JEP 101-C JEDEC REQUIREMENTS FOR CLASS B MICROCIRCUITS: RESCINDED, May 2006
November 1995; Rescinded

JEP 102 STANDARD FOR 64K x 1 DYNAMIC RAM - SUPERSEDED BY JESD21-C.

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JEP 105 JEDEC GUIDELINE FOR THE CHARACTERIZATION OF HYBRID POLYMERIC MATERIALS - SUPERSEDED BY JESD72, June 2001
April 1983; Rescinded June 2001

JEP 107 TEST METHOD FOR QUALIFICATION AND ACCEPTANCE OF PARTICLE GETTERS FOR USE IN HYBRID MICROELECTRONIC APPLICATIONS - SUPERSEDED BY JESD72, June 2001
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April 1991; Superseded

JEP 109-C GENERAL REQUIREMENTS FOR DISTRIBUTORS OF MILITARY SEMICONDUCTOR DEVICES:
March 1995; Rescinded November 2001

JEP 111 TEST PROCEDURES FOR CUSTOM MONOLITHIC MICROCIRCUITS - SUPERSEDED BY MIL-PRF-38535C.
July 1986; Rescinded June 1996

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JEP 117 GUIDELINES FOR USER NOTIFICATION OF PRODUCT/PROCESS CHANGES BY SEMICONDUCTOR SUPPLIERS - SUPERSEDED BY JESD46, August 1997.
April 1994; Rescinded July 1994

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August 1984; Rescinded August 1984

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June 1992; Rescinded June 1985

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September 1983; Rescinded September 1986

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August 1975; Rescinded June 1992

JEP 96 GUIDELINES FOR NONDESTRUCTIVE PULL TESTING OF WIRE BONDS ON HYBRID DEVICES
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JEP 99 GLOSSARY OF MICROELECTRONIC TERMS, DEFINITIONS, AND SYMBOLS: ELEVATED TO JESD99, June 1985.
July 1977; Rescinded June 1985

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April 1990; Rescinded July 2001

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July 1996; Superseded July 1996

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JESD 41 REVERSE RECOVERY CHARACTERISTICS OF SILICON DIODES: Rescinded June 2002.
May 1995; Rescinded June 2002

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March 1994; Superseded

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November 1996; Superseded

JESD 45 MEASUREMENT METHOD FOR THERMAL RESISTANCE OF BRIDGE RECTIFIER ASSEMBLIES: RESCINDED, June 2002. Replaced by JESD282-B.
December 1994; Rescinded June 2002

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July 1973; Rescinded June 1992

MO 177-A Registration - Rescission of 200 Pin Small Outline Dual-In-Line Memory Module (DIMM) Family, 0.65 mm Pitch. Item 11.14-044.
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