

CREATING 3D CIRCUITS USING TRANSFERRED FILMS

The Ability to Fabricate 3D Circuits with Virtually
Unrestricted Placement of Interconnects

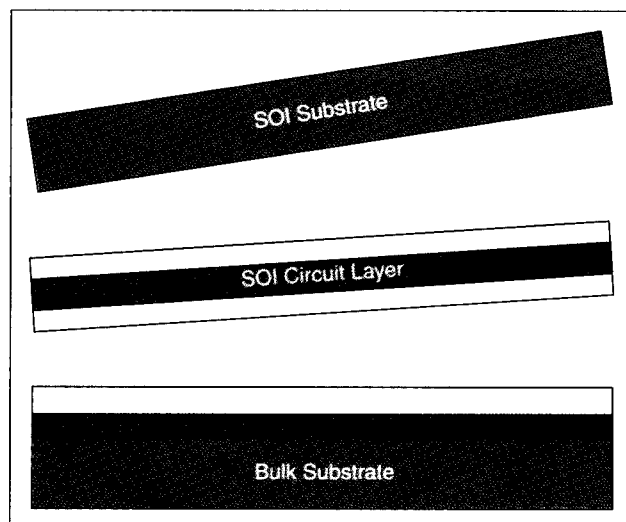
Philip M. Sailer, Piyush Singhal, Jeffrey Hopwood, David R. Kaeli, Paul M. Zavracky, Keith Warner, and D.P. Vu

Over the past two decades, the lure of three-dimensional circuits has attracted the attention of the research community. A number of groups began producing 3D devices, and in Japan development of 3D microelectronics became a national goal [1]. The advantages of 3D include reduced die size, increased functionality, and increased speed.

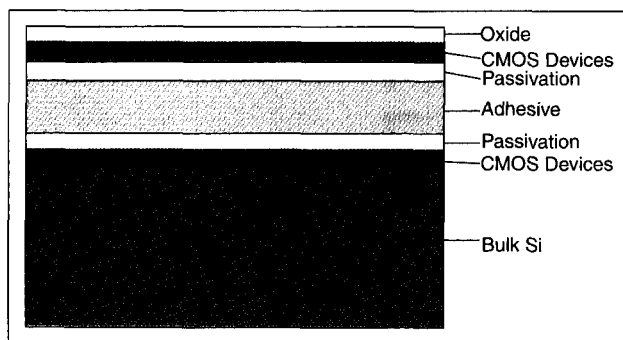
Several different approaches to developing these circuits have been taken. Some investigators have tried thinning and stacking silicon die [2]. In this approach, interconnections between levels are accomplished at the perimeter of the stack. Akiyama et al. used laser recrystallization to create layers of single crystalline silicon above completely fabricated circuits [3]. Each subsequent layer would be processed to create an additional circuit function. In this type of circuit, interconnection between layers is not limited to the perimeter of the die. In the 1980s, Fan et al. began to commercially develop thin-film transfer processes. These techniques were applied to the development of devices with mixed technologies (GaAs and Si) and were proposed as the basis for creating a 3D circuit [4, 5]. Initial results on stack inverters were promising [6].

During the past several years we have been developing technology for the creation of 3D microelectronics. Our 3D circuits are fabricated using standard bulk CMOS processing and are then transferred from one wafer to another. The transfer process allows alignment of the layers. The resulting structure consists of lower substrate and associated circuitry, with one or more thin-film circuit layers stacked on top, separated by bonding lay-

ers. We have developed an interconnection technology that allows layers to be electrically connected to one another. These interconnections are small and can be placed anywhere on the die [7]. This unrestricted placement of interconnections gives our technology a unique advantage over other existing 3D interconnect techniques [8, 9]. We report our approach in this article.



1. Transfer process taking the device layer from the SOI wafer and bonding it to the top of a processed bulk silicon wafer.



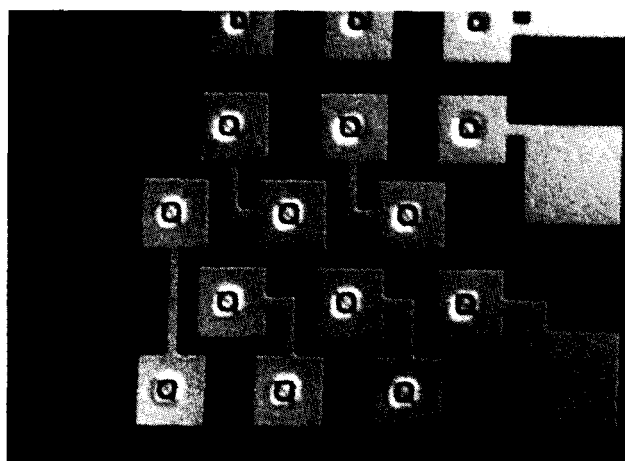
2. A simplified cross-sectional view of a 3D circuit created using Kopin's circuit transfer technology.

3D Processing

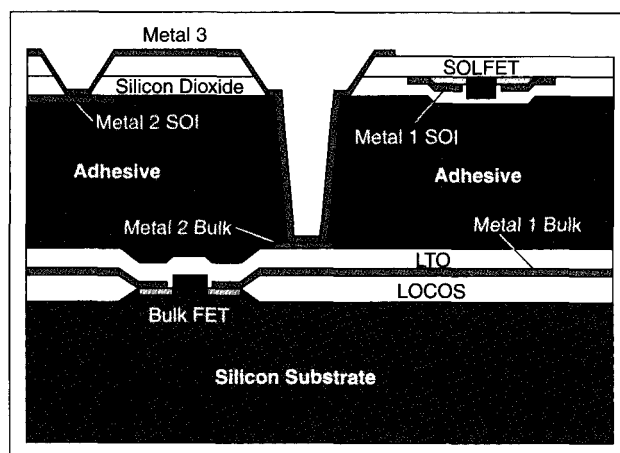
Our current work utilizes a two-level process. In this case, a bulk silicon wafer is processed with half of the circuit. A second silicon-on-insulator (SOI) wafer is processed using standard CMOS fabrication techniques, creating the second half of the circuit. An SOI wafer consists of a bulk silicon substrate with a thin layer of single crystalline silicon on top, separated from the substrate by a silicon dioxide layer (buried oxide). The SOI wafer is used because the buried oxide layer acts as an etch-stop during a subsequent back-etch step. The SOI circuit is transferred face down onto the top of the bulk wafer as shown in Fig. 1. An adhesive is used to bond the transferred circuit to the bulk silicon wafer. The result is the two-layer 3D circuit shown in Fig. 2. Electrical connections need to be made between the two active device layers after the transfer.

Interconnect Processing

The objective of the 3D interconnection process is to make electrical connections between bulk devices on the lower layer of the 3D structure and SOI devices on the upper layer. Our interconnection scheme is illustrated in Fig. 3. An extra metal layer (metal-3), positioned on the very top of the 3D circuit, is introduced. Bulk metal-2 (the top-most metal layer on the bulk CMOS circuit) and SOI metal-2 (the top-most metal layer on the



4. An optical micrograph of an interconnection test structure for measuring contact resistance. The large pads to the extreme right are 100 μm square.



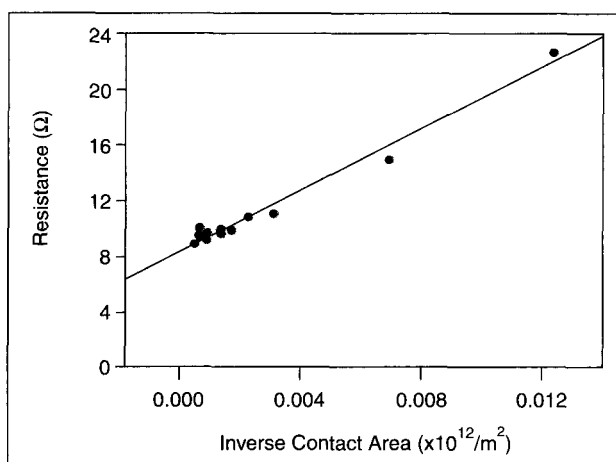
3. Schematic cross-section of an ideal deposited metal interconnection.

SOI CMOS circuit) are connected to the metal-3 through separate vias. Via etching is accomplished using an inductively coupled plasma (ICP) to anisotropically etch both oxide and adhesive layers. Via filling is performed using a conventional magnetron sputtering source with a high bias. Fig. 4 shows the results of a via test structure with chained interconnections made between metal-3 and bulk metal-2.

In Fig. 3, it can be seen that the vertical dimension of the 3D interconnection via is much larger than the via in conventional semiconductor processes. In our 3D interconnection there are approximately 5 μm of bonding adhesive and 2 μm of silicon dioxide in between the bulk silicon devices and SOI devices. In a conventional semiconductor process, the depth of via holes is in the range of 1 μm . Conventional via filling processes, such as the use of tungsten plugs, require high temperatures and may not be suitable for a 3D interconnection.

Our transfer technique has the following advantages over other 3D methods:

- ◆ The procedure is simple (the process uses conventional VLSI processes)
- ◆ Transfer is done at wafer scale, leading to potentially high production rates



5. Contact resistance data for deposited aluminum-lined vias.

- ♦ The process is conducted at low temperatures, therefore devices will not be damaged during the transfer process
- ♦ The capability of fabricating circuits with more than two layers is possible using multiple transfer steps

We use similar processes for fabricating our devices in bulk-Si and SOI technologies. Both processes employ standard CMOS processing techniques and are compatible with commercial silicon foundries. The SOI and the buried oxide thicknesses are 1 μm each. As a consequence of the thick single crystalline silicon layer, the fabricated SOI MOSFETs are not fully depleted. Therefore, body contacts on the n-channel devices are required to collect the holes that are generated by impact ionization near the drain.

Results

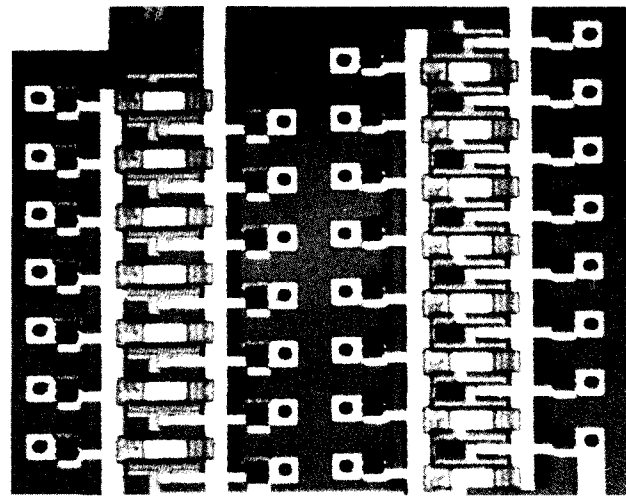
Initial tests have been completed on interconnection structures using the test mask designed for obtaining contact-resistance measurements. Contact-resistance measurements were made on contact chains, similar to those shown in Fig. 4. The chain consists of 12 interconnections between metal-2 bulk and metal-2 SOI. Structures of this type were fabricated with contact vias sizes ranging from 36 μm down to 6 μm . Figure 5 shows a plot of the contact resistance plotted versus the inverse contact area. The slope of the line is proportional to the contact resistivity ($76 \Omega/\mu\text{m}^2$), and the intercept represents the resistance of the leads and interconnection metal.

In Fig. 6 an optical micrograph of a portion of our 3D ring oscillator is shown. The pairs of large and small vias (dark areas) constitute a single interconnection between the bulk and SOI metal-2 layers. The ring oscillator threads up and down between the two circuit levels connecting together SOI and Bulk inverters.

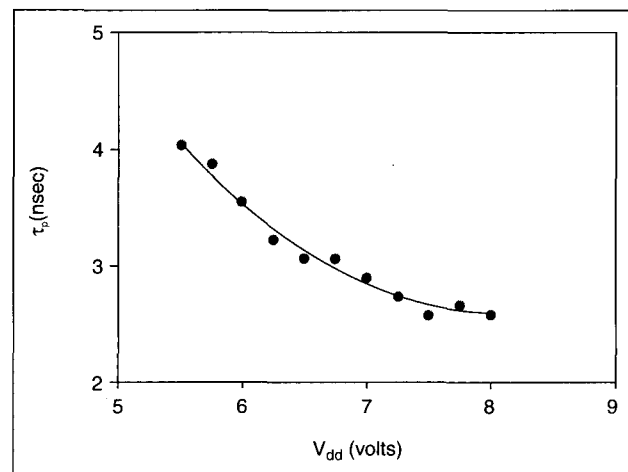
Functional 31-stage ring oscillators were fabricated in bulk, SOI, and 3D technology using a 3 μm process at Northeastern University. The bulk and SOI devices were operated at 5.5 volts and showed stage delays of about 2.98 ns for the bulk devices and 3.43 ns for the SOI devices. These results are close to simulated values. The 3D ring oscillator was constructed with one interconnection per stage. Our intent was to demonstrate the feasibility of a 3D circuit and not to demonstrate a speed improvement. Measurements of the 3D ring oscillator resulted in stage delays of about 4.0 ns. Figure 7 shows a plot of the ring-oscillator frequency versus supply voltage. The significance of this development is that it demonstrates that a large number of interconnections (31) can be incorporated into a circuit successfully. Figure 8 presents a cross-sectional view of our two-layer 3D circuit.

Conclusions

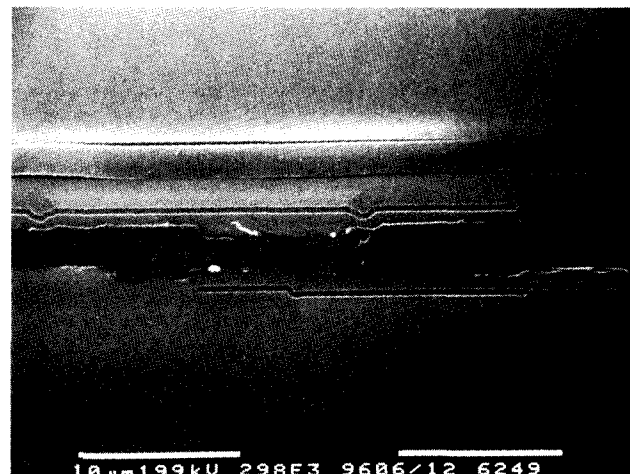
We have presented results, including functional devices, fabricated using our 3D technology based on transferred circuits. Our results indicate that it is feasible to fabricate 3D circuits with virtually unrestricted placement of interconnections between circuit layers. This 3D technology is also being used to drive a number of other projects at Northeastern, including the design of: 1) a 32-bit pipelined microprocessor [10], 2) a vision-sensing array, and 3) a 3D FPGA design [11, 12].



6. Completed 3D ring oscillator currently under test.



7. 3D ring oscillator performance.



8. Cross-section of a two-layer 3D circuit.

One issue not addressed in this article is the need for VLSI tools in order to fully exploit this technology. To date, our 3D design has been implemented using hand placement [13]. To enjoy the benefits of unrestricted via placement, and multilayered de-

vice technology, new VLSI algorithms are needed for 3D partitioning, placement, and routing. 3D partitioning tools, based on Ratio-Cut and Kernighan-Lin partitioning algorithms, have been proposed [14]. Laying out portions of our 3D microprocessor using a new 3D bounding-box placement algorithm has resulted in area savings of over 54% (compared to a 2D layout produced using the Cadence toolset). Work on 3D routing is also underway.

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References

1. S. Tantsuno, "Japan's Push into Creative Semiconductor Research: 3-Dimensional IC's," *Solid State Technology*, 30:29-30, March 1987.
2. Y. Hayashi, S. Wada, K. Kajiyana, K. Oyama, R. Koh, S. Takahasi, and T. Kunio, "Fabrication of Three-Dimensional IC Using Cumulatively Bonded IC (CUBIC) Technology," *Symposium on VLSI*, 1990.
3. S. Akiyama, S. Ogawa, M. Yoneda, Y. Yshii, and Y. Terui, "Multilayer CMOS Device Fabrication on Laser Recrystallized Silicon Islands," *Technical Digest, IEDM*, 1983, pp. 352-355.
4. P.M. Zavracky, M.M. Zavracky, J.C.C. Fan, and J.P. Salerno, "Optoelectronic Interconnection for II-V Devices on Silicon," U.S. Patent No. 4,890,895, issued January 2, 1990.
5. B.D. Dingle, M.B. Spitzer, R.W. McClelland, J.C.C. Fan, and P.M. Zavracky, "Monolithic Integration of a Light-Emitting Diode Array and a Silicon Circuit Using Transfer Process," *Applied Physics Letters*, 62(22), May 1993.
6. Private communication with D.P. Vu.
7. Dong-Mei Li, *Interconnect Process for 3-Dimensional IC*, Department of Electrical and Computer Engineering, MS Thesis, Northeastern University, Boston, MA, May 1995.
8. M.B. Kleiner, S. Kuhn, and W. Weber, "Performance Improvement of the Memory Hierarchy of RISC-Systems by Application of 3-D Technology," *Proc. of IEEE Electronics Components and Technology Conference (ECTC)*, 1995, pp. 645-655.
9. S.A. Kuhn, M.B. Kleiner, and W. Weber, "Performance Modeling of the Interconnect Structure of a 2-Dimensionally Integrated RISC-Processor/Cache System," *Proc. of IEEE Electronics Components and Technology Conference (ECTC)*, 1995, pp. 592-599.
10. Philip M. Sailer, *YIFAN - A 3-D Microprocessor*, MS Thesis, Department of Electrical and Computer Engineering, Northeastern University, Boston, MA, August 1997.
11. W.M. Meleis, M. Leeser, P.M. Zavracky, and M.M. Vai, "Architectural Design of a Three Dimensional FPGA," *Workshop on Field-Programmable Logic and Applications (FPL)*, September 1997.
12. M. Leeser, W.M. Meleis, M.M. Vai, and P.M. Zavracky, "Rothko: A Three Dimensional FPGA Architecture, It's Fabrication, and Design Tools," *Conference on Advanced Research in VLSI (ARVLSI)*, September 1997.
13. J.K. Ousterhout et al., "Magic Tutorials," Computer Science Division (EECS), University of California, Berkeley, CA.
14. Stephen Strickland, *Partitioning and Placement Algorithms for Custom 3D VLSI*, MS. Thesis, Department of Electrical and Computer Engineering, Northeastern University, Boston, MA, August 1997. CD ■
2. Semiconductor Industry Assoc., *The National Technology Roadmap for Semiconductor*, 1994.
3. B.J. Sheu and J. Choi, *Neural Information Processing and VLSI*, Kluwer Academic Publishers: Boston, MA, 1995.
4. B. Gieseke, et al., "A 600MHz superscalar RISC microprocessor with out-of-order execution," *Proc. of IEEE International Solid-State Circuits Conference*, pp. 176, Feb. 1997.
5. M. Hiltzik, "Quantum leaps," *Los Angeles Times*, May 12, 1997.
6. L. Adleman, "Molecular computation of solutions to combinatorial problems," *Science*, vol. 266, pp. 1021-1024, Nov. 11, 1994.
7. R. Pool, "Forget silicon, try DNA," *New Scientist*, vol. 151, pp. 26-31, July 13, 1996.
8. R. Pool, "A boom in plans for DNA computing," *Science*, vol. 268, pp. 498-499, April, 1995.
9. R.J. Lipton, "DNA solution of hard computational problems," *Science*, vol. 268, pp. 542-545, April 28, 1995.
10. K. Leutwyler, "Calculating with DNA," *Scientific American*, vol. 273, pp. 20-23, Sep. 1995.
11. Y. Friedman, "DNA computers," <http://www.clearlight.com/~morph>.
12. D. Tank, J. Hopfield, "Simple 'neural' optimization networks: an A/D converter, signal decision circuit, and a linear programming circuit," *IEEE Trans. on Circuits and Systems*, vol. 33, no. 5, pp. 533-541, May 1986.
13. R. Kannan, "Markov chains and polynomial time algorithm," *IEEE Proc. of the 35th Annual Symposium on Foundations of Computer Science*, pp. 656-671, 1994.
14. G. Kaluga, "Gene Genie," <http://www.cs.princeton.edu/~dabo/bio-come/bolecular.html>.
15. H. Muir, "DNA reveals its talent for computing," *New Scientist*, vol. 144, pp. 17, Nov. 26, 1994.
16. E. Winfree, "On computational power of DNA annealing and ligation," <http://dope.caltech.edu/winfree/DNA.html>.
17. V. Roychowdhury, et al., "Nanoelectronic architecture for Boolean logic," *Proc. of the IEEE*, vol. 85, no. 4, pp. 574-588, April 1997.
18. K.F. Gosser, et al., "Aspect of systems and circuits for nanoelectronics," *Proc. of the IEEE*, vol. 85, no. 4, pp. 558-573, April 1997.
19. C. Lent, P. Tougaw, "A device architecture for computing with quantum dots," *Proc. of the IEEE*, vol. 85, no. 4, pp. 541-557, April 1997.
20. C. Lent, P. Tougaw, "Bistable saturation due to single electron charging in rings of tunnel junctions," *J. Appl. Phys.*, vol. 75, pp. 4077-4080, April 1994.
21. D. Bartelink et al., "Process of the future," *Solid State Technology*, vol. 38, no. 2, pp. 43-54, 1995.
22. L.S. Kuzmin, et al., "Single-electron charging effects in one-dimensional arrays of ultrasmall tunnel junctions," *Phys. Rev. Letter*, vol. 62, pp. 2539-2542, 1989.
23. K.K. Likharev, "Correlated discrete transfer of single electron in ultrasmall tunnel junction," *IBM J. Res. Develop.*, vol. 32, no. 1, pp. 144-158, 1988.
24. C. Mead and L. Conway, *Physics of Computational Systems*, Addison-Wesley: Dedham, MA, 1980. CD ■