US006807098B2

(12) **United States Patent**
Jeong et al.

(10) **Patent No.: US 6,807,098 B2**
(45) **Date of Patent: Oct. 19, 2004**

(54) **NONVOLATILE SEMICONDUCTOR MEMORY WITH A PROGRAMMING OPERATION AND THE METHOD THEREOF**

(75) Inventors: **Jae-Yong Jeong**, Kyunggi-do (KR); **Sung-Soo Lee**, Kyunggi-do (KR)

(73) Assignee: **Samsung Electronics Co., Ltd.**, Suwon (KR)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/659,634**

(22) Filed: **Sep. 9, 2003**

(65) **Prior Publication Data**

US 2004/0047214 A1 Mar. 11, 2004

Related U.S. Application Data

(63) Continuation of application No. 10/021,639, filed on Dec. 12, 2001, now Pat. No. 6,650,566.

(30) **Foreign Application Priority Data**

Dec. 12, 2000 (KR) 2000-75641
Dec. 12, 2000 (KR) 2000-75642

(51) **Int. Cl.**[7] **G11C 16/04**
(52) **U.S. Cl.** **365/185.12**; 365/235
(58) **Field of Search** 365/235, 238.5, 365/185.12, 185.17

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,768,188 A 6/1998 Park et al.
5,768,215 A * 6/1998 Kwon et al. 365/238.5
5,862,074 A 1/1999 Park
5,966,266 A 10/1999 Park et al.
5,982,663 A 11/1999 Park
6,282,121 B1 8/2001 Cho et al.
6,285,587 B1 9/2001 Kwon
6,288,936 B1 * 9/2001 Kawamura 365/185.03
6,353,555 B1 3/2002 Jeong

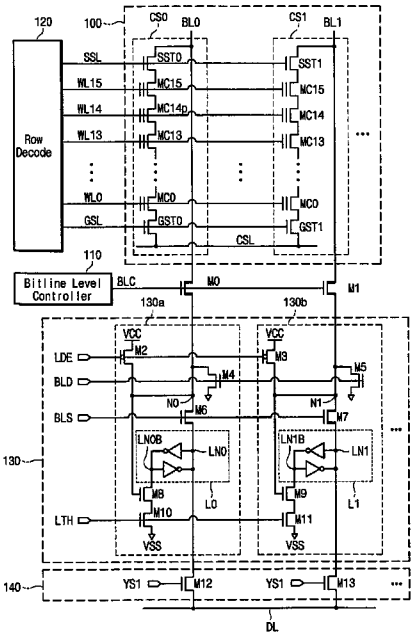
* cited by examiner

Primary Examiner—Thong Le
(74) *Attorney, Agent, or Firm*—Marger Johnson & McCollom, P.C.

(57) **ABSTRACT**

The invention provides a method of programming in a nonvolatile semiconductor memory device, having a plurality of memory cell strings connected to a plurality of bitlines and constructed of a plurality of memory cell transistors whose gates are coupled to a plurality of wordlines, and a plurality of registers corresponding to the bitlines. The method involves applying a first voltage to a first one of the bitlines and applying a second voltage to a second one of the bitline, the first bitline being adjacent to the second bitline, the first and second voltages being supplied from the registers; electrically isolating the first and second bitlines from their corresponding registers; charging the first bitline up to a third voltage higher than the first voltage and lower than the second voltage; and applying a fourth voltage to a wordline after cutting off current paths into the first and second bitlines.

15 Claims, 7 Drawing Sheets



Petitioner Micron Ex-1013, 0001

Fig. 1

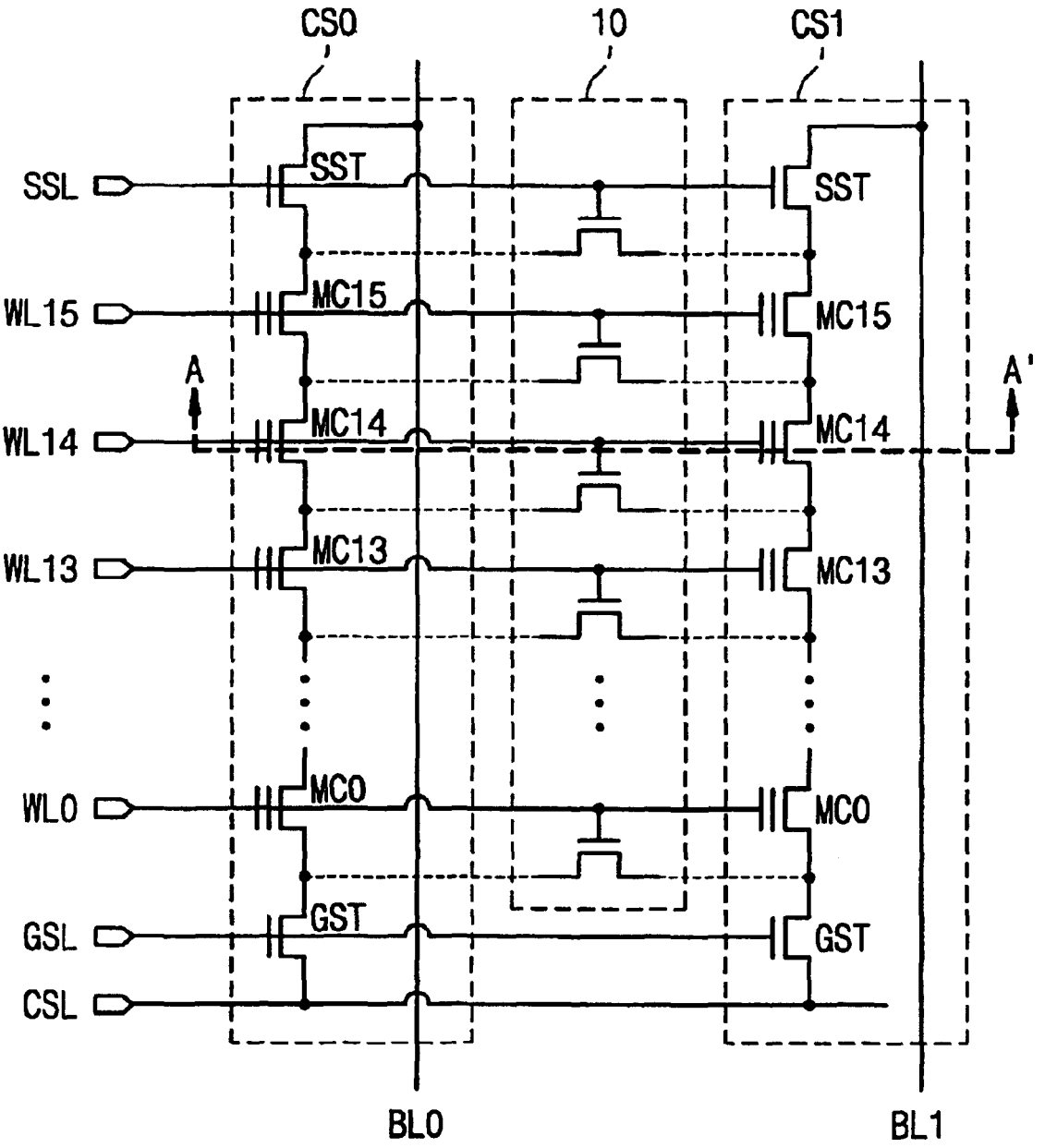

CS0
10
CS1
SSL
SST
SST
WL15
MC15
MC15
A
A'
WL14
MC14
MC14
WL13
MC13
MC13
WL0
MC0
MC0
GSL
GST
GST
CSL
BL0
BL1

Fig. 2

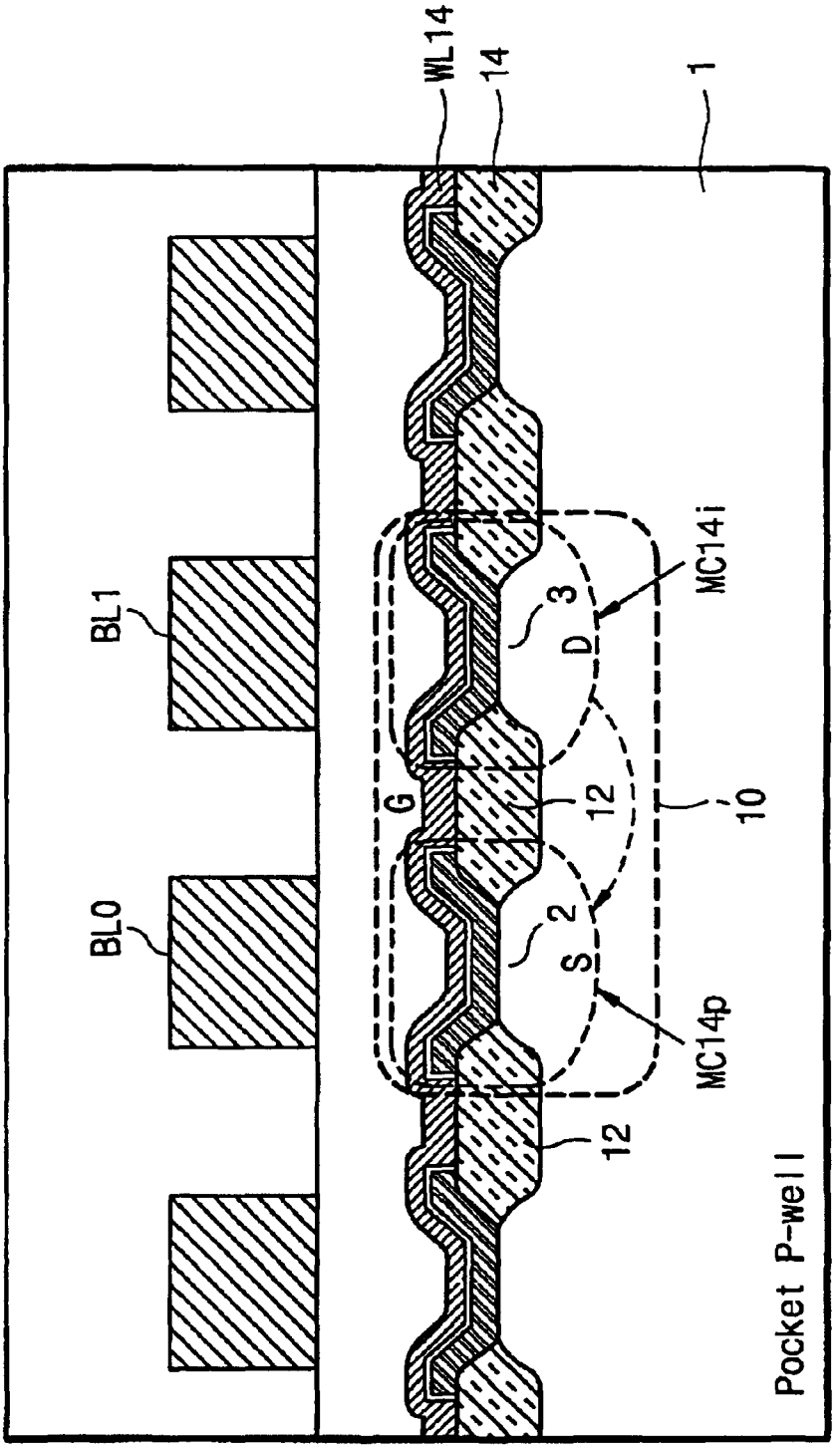


Fig. 3

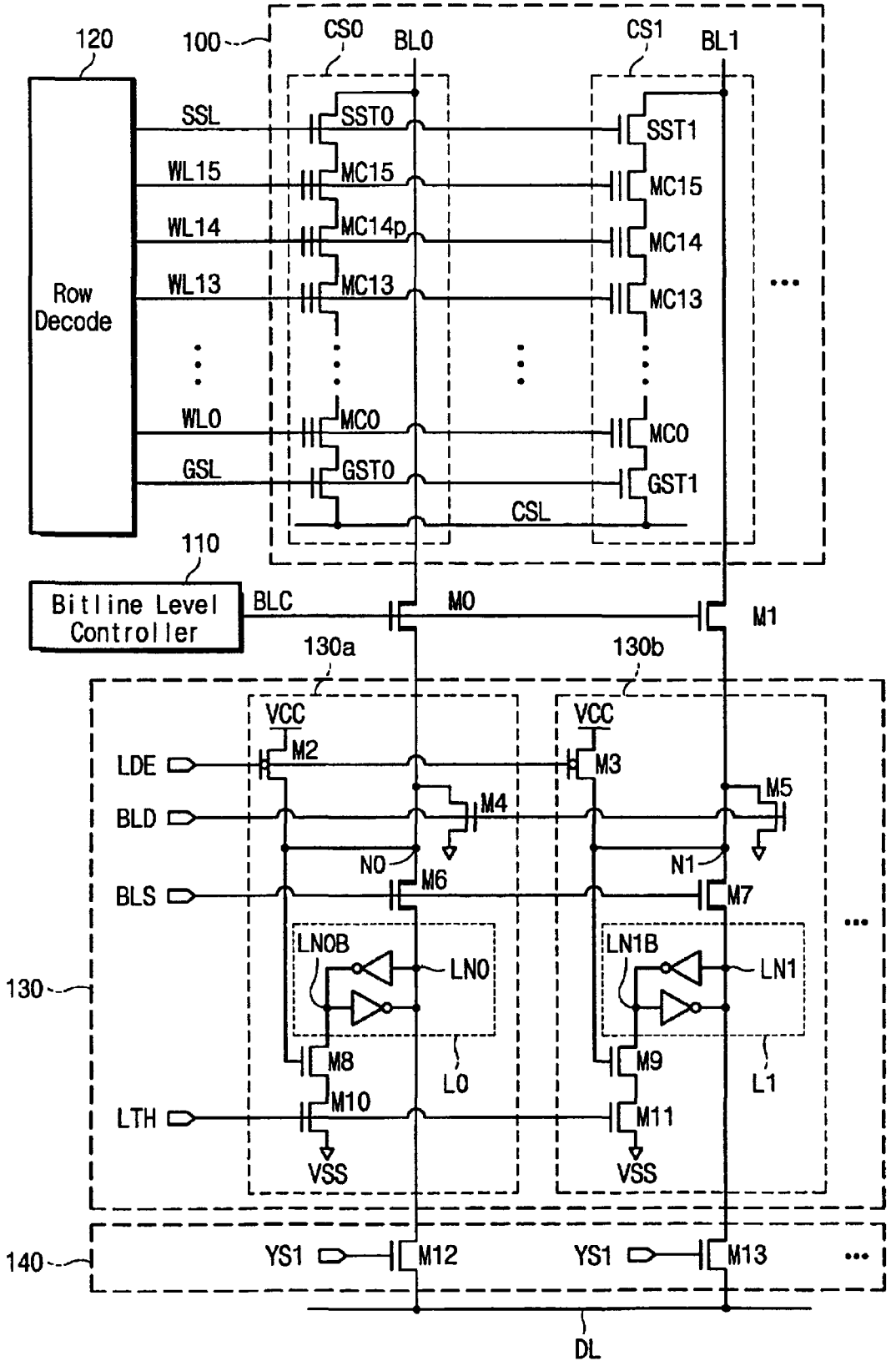

120
100
CS0
BL0
CS1
BL1
SSL
SST0
SST1
WL15
MC15
MC15
WL14
MC14p
MC14
WL13
MC13
MC13
Row Decode
WL0
MC0
MC0
GSL
GST0
GST1
CSL
110
Bitline Level Controller
BLC
M0
M1
130a
130b
VCC
VCC
M2
M3
LDE
BLD
M4
M5
N0
N1
M6
M7
BLS
LN0B
LN0
LN1B
LN1
130
M8
M9
L0
L1
M10
M11
LTH
VSS
VSS
140
YS1
M12
YS1
M13
DL

Fig. 4

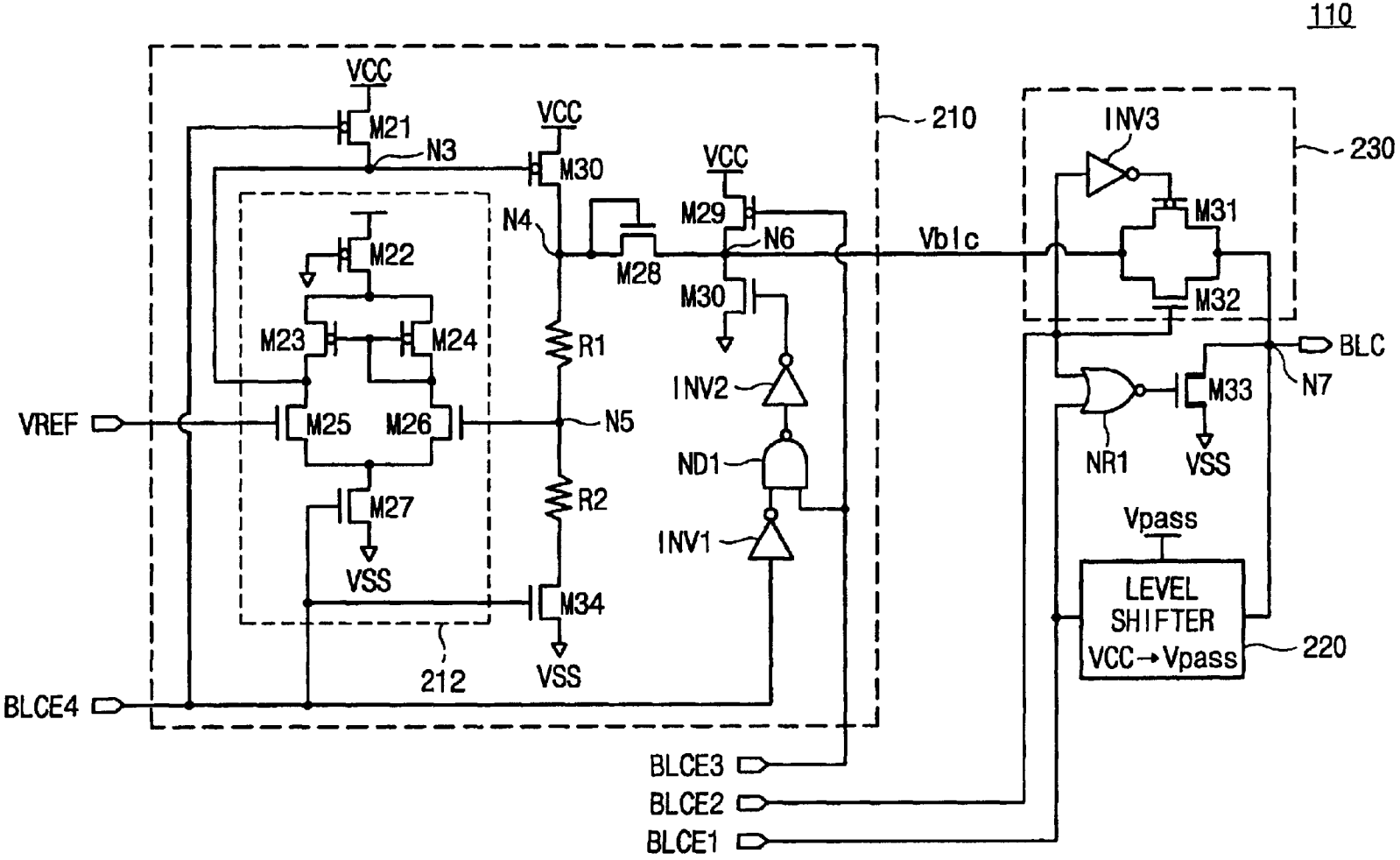

110
210
230
VCC
M21
N3
M30
N4
M28
M29
N6
Vblc
INV3
M31
M32
M22
M23
M24
R1
M30
INV2
BLC
N7
M33
VREF
M25
M26
N5
ND1
NR1
VSS
R2
M27
INV1
Vpass
LEVEL
SHIFTER
VCC→Vpass
220
VSS
M34
212
BLCE4
BLCE3
BLCE2
BLCE1

Fig. 5

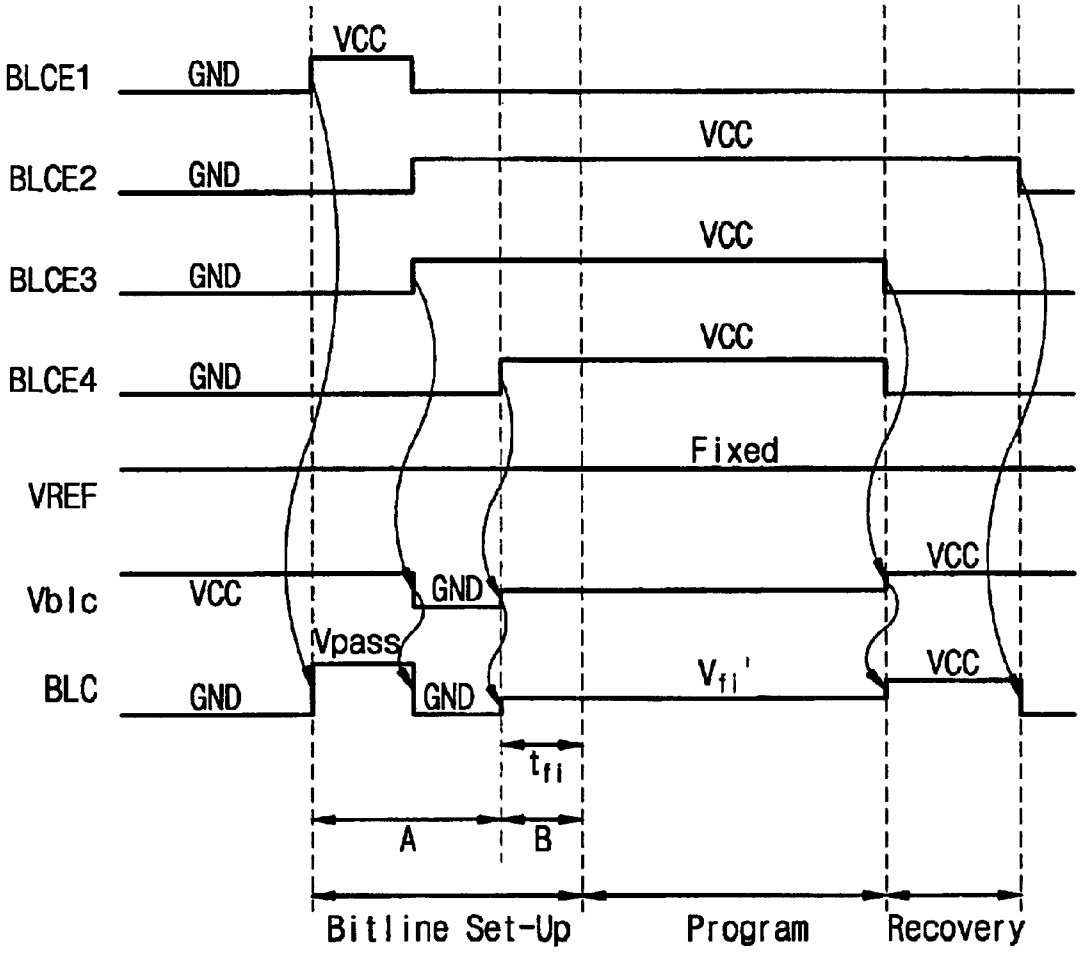

BLCE1
BLCE2
BLCE3
BLCE4
VREF
Vblc
BLC
GND
VCC
Vpass
Fixed
V_{fi}'
t_{fi}
A
B
Bitline Set-Up
Program
Recovery

Fig. 6

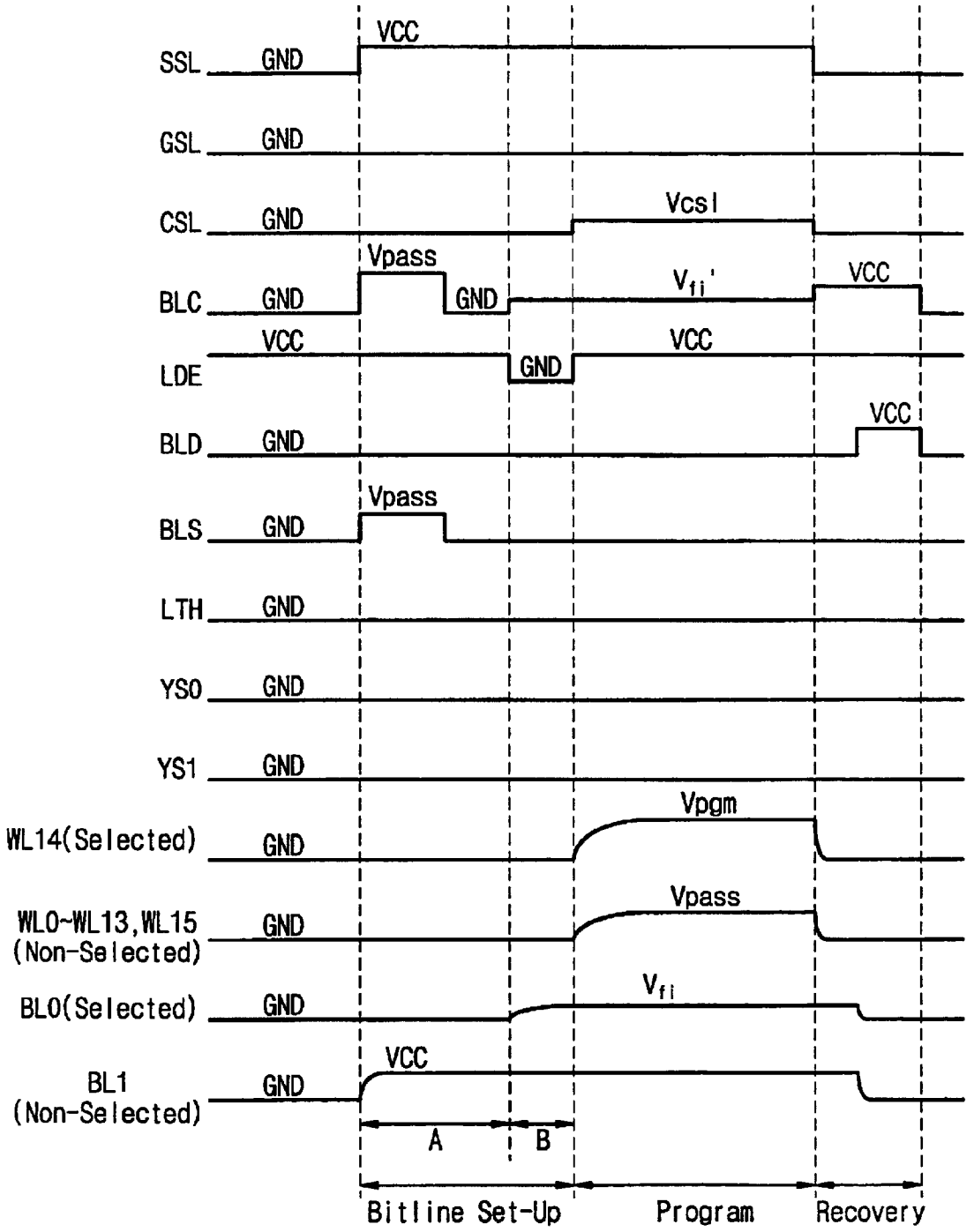
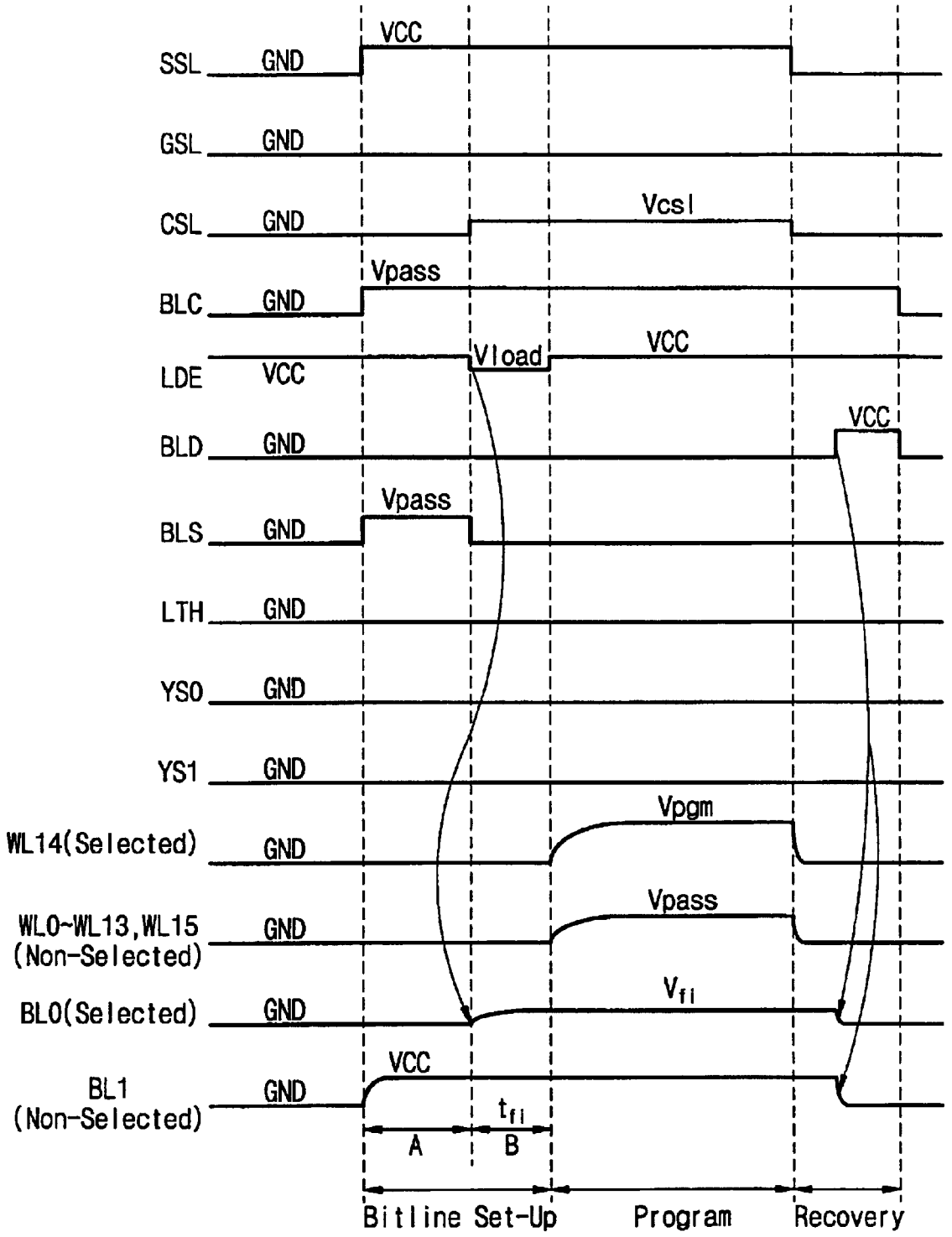

SSL
GSL
CSL
BLC
LDE
BLD
BLS
LTH
YS0
YS1
WL14(Selected)
WL0~WL13,WL15
(Non-Selected)
BL0(Selected)
BL1
(Non-Selected)
GND
VCC
Vcsl
Vpass
V_{fi}'
V_{fi}
Vpgm
A
B
Bitline Set-Up
Program
Recovery

Fig. 7


SSL
GSL
CSL
BLC
LDE
BLD
BLS
LTH
YS0
YS1
WL14(Selected)
WL0~WL13,WL15
(Non-Selected)
BL0(Selected)
BL1
(Non-Selected)
GND
VCC
Vcsl
Vpass
Vload
Vpgm
V_{fl}
t_{fl}
A
B
Bitline Set-Up
Program
Recovery

NONVOLATILE SEMICONDUCTOR MEMORY WITH A PROGRAMMING OPERATION AND THE METHOD THEREOF

This application is a continuation of U.S. Pat. No. application Ser. No. 10/021,639 Dec. 12, 2001, now U.S. Pat. No. 6,650,566 now pending, which is herein incorporated by reference in its entirety.

FIELD OF THE INVENTION

The present invention relates to nonvolatile semiconductor memory devices, and more specifically to a NAND-type flash memory device in which the threshold voltages of parasitic transistors interposed between memory cell transistors belonging to the same rows are controllable for a programming operation.

BACKGROUND OF THE INVENTION

NAND-type flash memory devices are in great demand for their high storage capacity and high integration density, without a need for refreshing, and their straightforward electrical functions of erasing and programming. The facilities of data retention of the NAND flash memory device, even during a power-off, are very useful for portable electronic systems such as mobile computers, digital still cameras, or PDAs.

The NAND flash memory device has memory cells electrically erased and programmed, i.e., EEPROM cells, each being formed of a source and a drain spaced apart from each other in a bulk region (or a semiconductor substrate), a floating gate positioned over a channel region between the source and drain, and a control gate over the floating gate. Insulation films are interposed between the control and floating gates, and between the floating gate and the channel region.

FIG. **1** shows an arrangement of a memory cell array including the EEPROM cells. Memory cell transistors MC**15**~MC**0** connected in series form a cell string CS**0** (or CS**1**). The memory cell transistor MC**15** is connected to bitline BL**0** (or BL**1**) through string selection transistor SST, and the memory cell transistor MC**0** is connected to common source line CSL through ground selection transistor GST. Control gates of the memory cell transistors M**15** arranged in a row are coupled to wordline WL**15**. In the same manner, control gates of other cell transistors in a row are coupled to their corresponding wordlines.

Threshold voltages of the cell transistors are set at about −3V by erasing, and then a programming operation is carried out for a selected memory cell transistor to raise its threshold voltage. This is done by applying a high voltage of 20V to a corresponding wordline coupled to the selected cell transistor. Threshold voltages of the other non-selected cell transistors do not change from their current values. However, typically a programming disturbance occurs whereby memory cell transistors coupled to a wordline coupled to a selected memory cell transistor are undesirably programmed by the high-leveled program voltage even though the cell transistors are not selected in a programming operation.

A program inhibit technique for preventing the non-selected memory cell transistors from being undesirably programmed has been proposed in U.S. Pat. No. 5,677,873 entitled "Method of programming flash EEPROM integrated circuit memory devices to prevent inadvertent programming of nondesignated NAND memory cells therein", or U.S. Pat. No. 5,991,202 entitled "Method for reducing program disturb during self-boosting in a NAND flash memory". In a method of program inhibition called self-boosting, a current path towards a ground is cut off by applying 0V to a gate of the ground selection transistor GST. 0V is applied to a bitline (e.g., BL**0**) assigned to a selected memory cell transistor while a non-designated bitline (e.g., BL**1**) sees a program inhibit voltage of 3.3V or 5V of a power supply voltage VCC.

At the same time, the power supply voltage VCC is applied to a gate of the string selection transistor SST so that a source of the string selection transistor is charged up to VCC-Vth (Vth is a threshold voltage of the string selection transistor). The string selection transistor is substantially shut off. Next, a high program voltage Vpgm and a pass voltage Vpass are applied to a selected wordline and non-selected wordlines, respectively, so that channel voltages of the non-selected memory cell transistors are boosted up to levels that prevent programming. The boosted channel voltages prohibit generation of F-N tunneling between the floating gate and channel region, preventing any change of the non-selected memory cell transistors from their primary erased states.

Nevertheless, there is still a problem of programming disturbance, because the non-selected memory cell transistors adjacent to a selected memory cell transistor tend to be programmed due to leakage current flowing through parasitic MOS (meal-oxide-semiconductor) transistors **10** as shown in FIG. **1**. The parasitic transistors **10** are connected between active regions (sources or drains) of cell transistors coupled to the same wordlines.

Referring to FIG. **2** which shows a sectional diagram taken along the line A-A' of FIG. **1**, channel region **2** of program cell transistor MC**14***p* (to be programmed) and channel region **3** of program-inhibit cell transistor MC**14***i* act as a source and a drain, respectively, of the parasitic transistor. And the wordline W**14** acts as a gate of the parasitic transistor. A substrate region under field oxide **14** between the channel regions **2** and **3** is assigned to a channel region of the parasitic transistor. As a result, if the program voltage Vpgm is higher than a threshold voltage of the parasitic transistor, the parasitic transistor will be turned on, inducing a generation of leakage current flowing into the channel region **2** of the program cell transistor MC**14***p* from the channel region **3** of the program-inhibit cell transistor MC**14***i* through the conductive parasitic transistor. Thus, the self-boosted voltage at the channel region **2** of the program-inhibit cell transistor MC**14***i* becomes lower, resulting in an undesirable programming disturbance.

There is a way to overcome the aforementioned problem by increasing the threshold voltage of the parasitic MOS transistor, using an ion implantation into the substrate region acting as the channel region of the parasitic transistor. However, it is preferred to restrict such an ion implantation into the substrate region because of a decrease in breakdown voltage in the drain region, or because of a scaling-down of a topological size of the memory cell array. Increasing the threshold voltage of the parasitic transistor by biasing the substrate **1** with a negative voltage is also not desirable because a longer time for charging the substrate **1** increases overall program time.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a nonvolatile semiconductor memory device capable of preventing program disturbance due to parasitic MOS transistors, and a method thereof.

Petitioner Micron Ex-1013, 0009

It is another object of the invention to provide a nonvolatile semiconductor memory device capable of increasing a threshold voltage of a parasitic MOS transistor interposed between adjacent memory cell transistors, without increasing the wordline voltage during a program operation.

In order to achieve the present objects, a nonvolatile semiconductor memory of the invention includes: a memory cell array formed of a plurality of memory cell strings each connected to a plurality of bitlines; a plurality of page buffers each connected to the bitlines; a plurality of transistors connected between the bitlines and the page buffers; and a bitline voltage controller applying a bitline control voltage to gates of the transistors. The bitline control voltage is charged to a first voltage during a first bitline setup period and charged to a second voltage during a second bitline setup voltage, the second voltage being lower than the first voltage.

Another aspect of the invention is a method of programming in a nonvolatile semiconductor memory device, which has a plurality of memory cell strings connected to a plurality of bitlines and constructed of a plurality of memory cell transistors whose gates are coupled to a plurality of wordlines, and a plurality of registers corresponding to the bitlines, including the steps of: applying a first voltage to a first one of the bitlines and applying a second voltage to a second one of the bitlines, the first bitline being adjacent to the second bitline, the first and second voltages being supplied from the registers; electrically isolating the first and second bitlines from their corresponding registers; charging the first bitline up to a third voltage higher than the first voltage and lower than the second voltage; and applying a fourth voltage to a wordline after cutting off the current paths into the first and second bitlines.

The first, the second, the third, and the fourth voltages are a ground voltage, a power supply voltage, an inhibit voltage, and a program voltage, respectively.

As the inhibit voltage is applied to the first (i.e., selected) bitline so as to shut off the parasitic transistor interposed between memory cells coupled to the same wordline, the threshold voltage of the parasitic transistor is increased up to a level higher than the program voltage, preventing program disturbance by way of the parasitic transistor.

The present invention will be better understood from the following detailed description of the exemplary embodiment thereof taken in conjunction with the accompanying drawings, and its scope will be pointed out in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete appreciation of the present invention, and many of the attendant advantages thereof, will become readily apparent as the same becomes better understood by reference to the following detailed description when considered in conjunction with the accompanying drawings in which like reference symbols indicate the same or similar components, wherein:

FIG. **1** is a circuit diagram of a general memory cell array in a NAND-type flash memory device;

FIG. **2** is a sectional physical diagram of the cell array taken along with the line A-A' of FIG. **1**;

FIG. **3** is a circuit diagram of a memory cell array and a peripheral circuit thereof to perform a programming operation, according to an embodiment of the invention;

FIG. **4** is a circuit diagram of the bitline level controller shown in FIG. **3**;

FIG. **5** is a timing diagram illustrating an operation of the bitline level controller of FIG. **4**;

FIG. **6** is a timing diagram illustrating the programming operation performed by the circuit of FIG. **3**, according a first embodiment of the invention; and

FIG. **7** is a timing diagram illustrating a programming operation performed by the circuit of FIG. **3**, according to a second embodiment of the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

It should be understood that the description of this preferred embodiment is merely illustrative and that it should not be taken in a limiting sense. In the following detailed description, several specific details are set forth in order to provide a thorough understanding of the present invention. It will be obvious, however, to one skilled in the art that the present invention may be practiced without these specific details.

Referring first to FIG. **3** showing a circuit construction for performing a program operation according to the first embodiment of the invention, including memory cell array **100**, bitline level controller **110**, row decoder **120**, page buffer (register) circuit **130**, and column gate circuit **140**. The memory cell array **100** is formed of plural cell strings CS**0**, CS**1**, etc. Cell string CS**0**, for example, is formed of string selection transistor SST**0**, EEPROM cell transistors MC**0**~MC**15**, and ground selection transistor GST**0**. The string selection transistor SST**0** is connected to bitline BL**0**, and the ground selection transistor GST**0** is connected to common source line CSL. The cell transistors MC**15**~MC**0** are connected between the string and ground selection transistors, SST**0** and GST**0**, in serial. String selection line SSL, wordlines WL**0**~WL**15**, and ground selection line GSL extend from the row decoder **120**, and are coupled to gates of the string selection transistors SST**0**, SST**1**, etc., control gates of the cell transistors MC**0**~MC**15**, and the gates of the ground selection transistors GST**0**, GST**1**, etc., respectively. The bitline BL**0** is connected to node N**0** of page buffer (register) **130***a* of the page buffer circuit **130** through high-voltage adaptable NMOS transistor M**0**, and the bitline BL**1** is connected to node N**1** of page buffer (register) **130***b* of the page buffer circuit **130** through high-voltage adaptable NMOS transistor M**1**. Gates of the transistors M**0** and M**1** are coupled to a bitline level control signal BLC generated from the bitline level controller **110**.

The page buffers (e.g., **130***a* and **103***b*) arranged in the page buffer circuit **130** each correspond to the bitlines (e.g., BL**0** and BL**1**). In the page buffer **130***a*, between VCC and the node N**0** is connected PMOS transistor M**2** whose gate is coupled to load enable signal LDE. Between N**0** and a ground voltage (or a substrate voltage VSS) is connected NMOS transistor M**4** whose gate is coupled to bitline discharge signal BLD. The node N**0** is connected to latch node LN**0** of latch circuit L**0** through high-voltage adaptable NMOS transistor M**6** whose gate is coupled to bitline selection signal BLS. Between counter nodes LN**0**, LN**0**B of the latch circuit L**0** and VSS are connected NMOS transistors M**8** and M**10**. Gates of the NMOS transistors M**8** and M**10** are coupled to the node N**0** and latch enable signal LTH, respectively. The latch node LN**0** is connected to data line DL through NMOS transistor M**12**, whose gate is coupled to column selection signal YS**0** generated from a column decoder (not shown).

In the page buffer **130***b*, between VCC and the node N**1**, is connected a PMOS transistor M**3** whose gate is coupled

Petitioner Micron Ex-1013, 0010

to load enable signal LDE. Between N1 and the ground voltage VSS is connected NMOS transistor M5 whose gate is coupled to bitline discharge signal BLD. The node N1 is connected to latch node LN1 of latch circuit L1 through high-voltage adaptable NMOS transistor M7 whose gate is coupled to bitline selection signal BLS. Between counter nodes LN1, LN1B of the latch circuit L1 and VSS are connected NMOS transistors M9 and M11. Gates of the NMOS transistors M9 and M11 are coupled to the node N1 and latch enable signal LTH, respectively. The latch node LN1 is connected to data line DL through a NMOS transistor M13 whose gate is coupled to column selection signal YS1 generated from a column decoder (not shown).

The bitline level controller **110** in FIG. **4** includes bitline control voltage generator **210**, level shifter **220**, and CMOS transmission gate **230**.

In the bitline control voltage generator **210**, reference voltage VREF is applied to the gate of NMOS transistor M25 of differential amplifier **211**. Node N5 between resistors R1 and R2 is coupled to the gate of NMOS transistor M26 of the differential amplifier **212**. The differential amplifier **212** is constructed of PMOS transistors M22~M24 and of NMOS transistors M25~M27. The PMOS and NMOS transistors, M22 and M27, connect the amplifier **212** to VCC and Vss, respectively. The gate of the PMOS transistor M22 is coupled to VSS while the gate of the NMOS transistor M27 is coupled to bitline control enable signal BLCE4. BLCE4 is also applied to the gate of PMOS transistor M21 connected between VCC and node N3, gate of NMOS transistor M34 connected between the resistor R2 and VSS, and to the input of NAND gate ND1 through inverter INV1. The node N3 is connected to the output of the differential amplifier **212** and to the gate of PMOS transistor M30 which is connected between VCC and node N4 connected to the resistor R1. Node N4 is connected to the node N6 through NMOS transistor M28 whose gate and drain are coupled in common. Between VCC and the node N6 is a PMOS transistor M29 whose gate is coupled to bitline control enable signal BLCE3. BLCE3 is also applied to the input of the NAND gate ND1 together with the output of the inverter INV1. The output of NAND gate ND1 is applied through inverter INV2 to the gate of NMOS transistor M30 connected between the node N6 and VSS.

The output node N6 of the bitline control voltage generator **210**, labeled bitline control voltage Vblc, is connected to output terminal N7 generating bitline control signal BLC via a transmission gate **230**. An N-channel electrode of the transmission gate **230** is coupled to bitline control enable signal BLCE2, while a P-channel electrode of the transmission gate is coupled to BLCE2 through an inverter INV3. BLCE2 is also applied to an input of NOR gate NR1 together with another bitline control enable signal BLCE1. The output of the NOR gate NR1 is applied to a gate of high-voltage adaptable NMOS transistor M33 connected between the output terminal N7 and VSS. A level shifter **220** converts VCC into program pass voltage Vpass in response to BLCE1.

FIG. **5** shows voltage waveforms of the signals and voltages in the bitline level controller **110**, along a sequence of a program operation. A voltage level of the bitline control signal BLC is set to Vpass in response to BLCEI going high, and then returns to the ground level in response to rising BLCE3, during period A (the first bitline set-up) within a bitline set-up time. During period B (subsequent to A) of the bitline set-up time. BLC goes up to only voltage Vfi' from the ground level before programming, which second bitline set-up voltage Vfi' may be seen from the BLC trace in FIG. **5** to be lower than first bitline set-up voltage Vpass.

The voltage level Vfi' is a sum of a threshold voltage of a bitline level control transistor (i.e., M0 or M1) and a minimum source-to-bulk voltage that is required for turning the parasitic MOS transistor on. Thus, a level Vfi is provided by the bitline level controller **110** in order to inhibit programming. The inhibit voltage Vfi, higher than the ground voltage, is supplied to a bitline assigned to the program cell. The inhibit voltage Vfi should be established with consideration for a characteristic threshold voltage of a MOS transistor, the threshold voltage of the MOS transistor (i.e., the parasitic MOS transistor) being summarized in the following equation.

$$Vt=Vto+\gamma(\sqrt{2\phi f+Vsb}-\sqrt{2\phi f}) \quad (1)$$

wherein Vto is a threshold voltage when Vsb is 0V, wherein g is a process parameter and øf is a physical parameter, as is known.

Because Vt is affected from source-to-bulk voltage Vsb, the inhibit voltage Vfi should be established to shut off a leakage current between adjacent memory cell transistors, i.e., to make the threshold voltage of the parasitic MOS transistor (or a field voltage) be higher than a program wordline voltage, without increasing the wordline voltage during programming. Of course, Vfi is adjusted by the resistance values of the resistors R1 and R2 (See FIG. **4**). To bias a bitline of the program cell on Vfi, the voltage level of the bitline level control signal BLC, i.e., Vfi', should be set to Vfi+Vth1 (Vth1: a threshold voltage of the NMOS transistor M0 or M1).

Assume that BL0 is a bitline to be programmed and BL1 is a bitline to be program-inhibited. When all of the bitline control enable signals BLCE1~BLCE4 are held at low levels (e.g., ground levels), the NMOS transistor M33 is turned on and thereby the bitline level control signal BLC is established at the ground level (or VSS). Next, when BLCE1 goes to high level (or VCC) while BLCE2~BLCE4 retain low levels, M33 is turned off and thereby BLC is converted to the pass voltage Vpass by the level shifter **220**. The transmission gate **230** is turned off, and Vblc is set to VCC by PMOS transistor M29 turned on by BLCE3. The voltage level of the bitline level control signal BLC, i.e. Vpass, is applied to the gate of the NMOS transistor M0 or M1, so that a data bit "0" to be programmed is supplied to BL0 or BL1 to be programmed through the NMOS transistor M0 or M1. When BLCE1 falls to a low level and BLCE2 and BLCE3 rise up to high levels, the transmission gate **230** and the NMOS transistor M30 are turned on. The output of the level shifter **220** is at ground level. Thus, BLC goes to ground level from Vpass through the discharging path of the transmission gate **230** and the NMOS transistor M30.

After the first bitline set-up period A, the second bitline set-up period B starts with a high transition of BLCE4 while BLCE1 remains low and BLCE2 and BLCE3 maintain high. As the NMOS transistors M27 and M34 are turned on, the differential amplifier **212** is conductive to compare the reference voltage VREF with a voltage at the node N5 divided by the resistors R1 and R2. If a voltage at the node N4 is lower than Vfi'+Vth28 (Vth28 being a threshold voltage of the NMOS transistor M28), i.e., the voltage at N5 is lower than VREF, the voltage at N4 is increased by current supplied through the PMOS transistor M21. When the voltage at N4 reaches Vfi'+Vth28, Vblc becomes Vfi' and thereby BLC is maintained at Vfi' for the programming time. The Vfi' is applied to the gate of the NMOS transistor M1 or M0, so that a data bit "1" for the program inhibition is supplied to BL1 or BL0 to be program-inhibited through the NMOS transistor M1 or M0.

Petitioner Micron Ex-1013, 0011

After the programming time, a recovery operation is performed for which BLCE1, BLCE2, BLEC3 and BLCE4 respectively are low, high, low, and low, and Vbls and BLC are set on VCC.

Now, referring to FIG. 6, a programming operation according to the first embodiment of the invention will be described in detail. It is assumed that MC14*p* is a memory cell transistor to be programmed, which means that BL0 is selected while BL1 is non-selected. Thus, the page buffer 130*a* assigned to BL0 holds data bit "0" while the page buffer 130*b* assigned to BL1 stores data bit "1". Also, WL14 coupled to the gate of MC14*p* is a selected wordline. The timing operation of the bitline level controller 110, shown in FIG. 5, is illustrated in FIG. 6.

At the beginning of the bitline set-up period, SSL goes to high level (hereinafter, referred to as VCC), BLS and BLC go to Vpass, and GSL, CSL, BLD, and LTH are low levels (hereinafter, referred to as GND). The NMOS transistors M0 and M1 are turned on by BLC of Vpass, and the string selection transistors SST0 and SST1 are turned on by SSL of VCC. The NMOS transistor M6 is turned on by BLS of Vpass. As a result, during the first bitline set-up period A, BL0 and BL1 are established GND and VCC, respectively. Before starting the second bitline set-up period B after the bitlines BL0 and BL1 are sufficiently set up each to GND and Vpass, BLC and BLS fall to GND from Vpass, thereby electrically isolating the bitlines BL0 and BL1 from their corresponding page buffers (registers) 130*a* and 130*b*.

Starting the second bitline set-up period B, BLC is charged to Vfi' (=Vfi+Vth1) as aforementioned in FIG. 5. And LDE goes to GND from VCC. Thereby, the current paths through the PMOS transistors M2/M3 and the NMOS transistors M0/M1 are connected to BL0/BL1. Since BLC is at Vfi', the selected bitline BL0 is charged to Vfi while the non-selected bitline BL1 remains at VCC that has been set in the first set-up period A. As the string selection transistors SST0 and SST1 are substantially in a shut-off state (there is no current flow), the cell strings CS0 and CS1 corresponding to BL0 and BL1 are in a floating state.

Consequently, in the programming period, the program voltage Vpgm is applied to the selected wordline WL14, and Vpass is applied to the non-selected wordlines WL0~WL13 and WL15. Since the cell string CS1 corresponding to the non-selected bitline BL1 is in the floating state, a channel voltage of the program-inhibit memory cell transistor MC14*i* rises to a level sufficient to prevent a F-N tunneling by way of a self-boosting mechanism induced from Vpgm. The boosted channel voltage of MC14*i* prohibits migration of electrons from its channel region to the floating gate because there is no discharge path due to the VCC-charged BL1. Meanwhile, a channel voltage of the program cell transistor MV14*p* is discharged to Vfi from a boosted level through BL0 even though it raises the boosted level in response to Vpgm that performs the self-boosting. Therefore, the channel voltage of the selected memory cell transistor MC14*p* is finally established at Vfi.

After programming, BL0 and BL1 are discharged to GND, and the page buffers (registers) 130*a* and 130*b* are reset.

At this point, the threshold voltage of the parasitic MOS transistor 10, as shown in equation (1), is established at a level higher than Vpgm, the actual levels being proportional to the source-to-bulk voltage Vsb, which is identical to the channel voltage of the program cell transistor (i.e., MC14), Vfi. Thus, the parasitic MOS transistor is turned on while Vpgm is applied to WL14, causing the leakage current flowing between MC14*p* and MC14*i* (See FIG. 2) through the parasitic transistor to be cut off. As a result, the program disturbance due to the parasitic transistor is eliminated.

FIG. 7 shows another case of programming according to the second embodiment of the invention. Like FIG. 6, FIG. 7 assumes that MC14*p* is a memory cell transistor to be programmed, which means that BL0 is selected while BL1 is non-selected. Thus, the page buffer (register) 130*a* assigned to BL0 holds data bit "0" while the page buffer (register) 130*b* assigned to BL1 stores data bit "1". Also, WL14 coupled to the gates of MC14*p* and MC14*i* is a selected wordline. The timing operation of the bitline level controller 110, shown in FIG. 5, is also illustrated in FIG. 6.

At the beginning of the bitline set-up period, SSL goes to VCC, BLS and BLC go to Vpass. At the same time, GSL, CSL, BLD, and LTH maintain GND. The NMOS transistor M0 and M1 are turned on by BLC of Vpass, and the string selection transistors SST0 and SST1 are turned on by SSL of VCC. The NMOS transistor M6 is turned on by BLS of Vpass. As a result, during the first bitline set-up period A, BL0 and BL1 are charged respectively to GND and VCC.

In the second bitline set-up period B, Vcsl is applied to the common source line CSL in order to prevent punch-through in the ground selection transistors GST0 and GST1. And BLS falls to GND from VCC to electrically isolate the bitlines BL0 and BL1 from their corresponding page buffers 130*a* and 130*b*. At the same time, LDE goes to Vload from VCC in order to supply load current Iload to BL0 and BL1 for a predetermined time tfi.

The time for charging the selected bitline BLn up to the inhibit voltage Vfi is associated with load current Iload in the following equation (2):

$$tfi=(CBL\times Vfi)/Iload \tag{2}$$

wherein CBL is capacitance of the bitline.

BLC is charged to Vfi' (=Vfi+Vth1) as aforementioned with respect to FIG. 5. And LDE goes to GND from VCC. Thereby, the current paths through the PMOS transistors M2/M3 and the NMOS transistors M0/M1 are connected to BL0/BL1. Since BLC is at Vfi', the selected bitline BL0 is charged to Vfi while the non-selected bitline BL1 maintains VCC that has been set in the first set-up period A. At this time, as the string selection transistors SST0 and SST1 are substantially in a shut-off state (there is no current flow), the cell strings CS0 and CS1 corresponding to BL0 and BL1 are in a floating state, i.e. current into the first and second bitlines is substantially inhibited.

Consequently, during the programming period, the program voltage Vpgm is applied to the selected wordline WL14, and Vpass is applied to the non-selected wordlines WL0~WL13, and WL15. As aforementioned, since the cell string CS1 corresponding to the non-selected bitline BL1 is in the floating state, a channel voltage of the program-inhibit memory cell transistor MC14*i* rises to a level sufficient to prevent a F-N tunneling by way of a self-boosting mechanism induced from Vpgm. The boosted channel voltage of MC14*i* to prohibits migration of electrons from its channel region to the floating gate because there is no discharge path due to the VCC-charged BL1. Meanwhile, a channel voltage of the program cell transistor MV14*p* is discharged to Vfi from a boosted level through BL0 even though it raises the boosted level in response to Vpgm that performs the self-boosting. Therefore, the channel voltage of the selected memory cell transistor MC14*p* is finally established at Vfi.

After programming, BL0 and BL1 are discharged to GND, and the page buffers 130*a* and 130*b* are reset.

At this point, the threshold voltage of the parasitic MOS transistor 10, as shown in the equation (1), is established at

Petitioner Micron Ex-1013, 0012

a level higher than Vpgm, being proportional to the source-to-bulk voltage Vsb that is identical the channel voltage of the program cell transistor (i.e., MC**14**), Vfi. Thus, the parasitic MOS transistor is turned on while Vpgm is applied to WL**14**, causing the leakage current flowing between MC**14***p* and MC**14***i* (See FIG. **2**) through the parasitic transistor to be cut off. As a result, the program disturbance due to the parasitic transistor is eliminated.

As aforementioned, as the inhibit voltage is applied to the selected bitline in order to turn off the parasitic transistor interposed between memory cells coupled to the same wordline, the threshold voltage of the parasitic transistor is increased up to a level higher than the program voltage and thereby memory devices employing the present invention are able to be free from the program disturbance caused by the parasitic transistor.

Although the preferred embodiments of the present invention have been disclosed for illustrative purposes, those skilled in the art will appreciate that various modifications, additions and substitutions are possible, without departing from the scope and spirit of the invention as described in the accompanying claims.

What is claimed is:

1. A nonvolatile semiconductor memory comprising:

a memory cell array formed of a plurality of memory cell strings each connected to a plurality of bitlines;

a plurality of page buffers each connected to a corresponding one of the bitlines;

a plurality of transistors connected between the bitlines and the page buffers, each of the plurality of transistors operative when turned off to electrically isolate each of the plurality of page buffers from the corresponding one of the plurality of bitlines; and

a bitline voltage controller applying a bitline control voltage to gates of the transistors selectively to turn the transistors off thus to effect electrical isolation between each of the plurality of page buffers and the corresponding one of the plurality of bitlines,

wherein the bitline control voltage is charged to a first voltage during a part of a first bitline setup period, a second voltage during the remaining of the first bit line period, and a third voltage during a second bitline setup period.

2. The nonvolatile semiconductor memory of claim **1**, wherein the third voltage is lower than the first voltage and higher than the second voltage.

3. The nonvolatile semiconductor memory of claim **2**, wherein the first and second voltages are a pass voltage and a ground voltage.

4. The nonvolatile semiconductor memory of claim **2**, wherein the third voltage corresponds to the sum of a field inhibition voltage and a threshold voltage of an NMOS transistor, the field inhibition voltage being a minimum source bulk voltage needed to turn off a parasitic MOS transistor.

5. The nonvolatile semiconductor memory of claim **1**, wherein the third voltage is maintained during a program period following the second bitline setup period.

6. The nonvolatile semiconductor memory of claim **5**, wherein the bitline control voltage is charged to a fourth voltage during a recovery period following the program period.

7. The nonvolatile semiconductor memory of claim **6**, wherein the fourth voltage is a power supply voltage.

8. The nonvolatile semiconductor memory of claim **6**, wherein the bitline voltage controller comprises:

a first voltage generator configured to supply the first voltage (VPASS) to a voltage line for transferring the bitline control voltage in response to a first bitline control signal (BLCE**1**);

a second voltage generator configured to generate the second voltage (GND) at an internal node in response to a second and a third bitline control signal (BLCE**2**, BLCE**3**);

a third voltage generator configured to generate the third voltage (Vfi') at the internal node in response to the fourth bitline control signal (BLCE**4**); and

a switch circuit configured to connect the internal node to the voltage line in response to the second bitline control signal (BLCE**2**).

9. The nonvolatile semiconductor memory of claim **8**, wherein the bitline voltage controller further comprises a discharge circuit configured to discharge a voltage of the voltage line in response to the first and second bitline control signals (BLCE**1**, BLCE**2**).

10. The nonvolatile semiconductor memory of claim **8**, wherein the bitline voltage controller further comprises a fourth voltage generator configured to generate the fourth voltage in response to the third control signal.

11. The nonvolatile semiconductor memory of claim **8**, wherein the first control signal is activated during the part of the first bitline setup period.

12. The nonvolatile semiconductor memory of claim **8**, wherein the second control signal is activated during the remaining of the first bitline setup period, the second bit line setup period, the program period and the recovery period.

13. The nonvolatile semiconductor memory of claim **8**, wherein the third control signal is activated during the remaining of the first bitline setup period, the second bitline setup period and the program period.

14. The nonvolatile semiconductor memory of claim **8**, wherein the fourth control signal is activated during the second bitline setup period and the program period.

15. The nonvolatile semiconductor memory of claim **8**, wherein the first voltage generator includes a level shifter and the fourth voltage generator includes a comparator and a voltage divider, respectively.

* * * * *

Petitioner Micron Ex-1013, 0013