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Real-Time Microvision System with Three-Dimensional Integration Structure

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Abstract

A number of two-dimensional LSIs (2D-LSIs) with the thickness of around 30 μm which play amplifying and converting image signal and some arithmetic operations are integrated vertically in order to achieve a real-time microvision system. This microvision system transfers the two-dimensional (2D) image data arrays as it is using high density vertical interconnections. So, the image information signals are processed in parallel in each LSI and the processings are performed in pipeline over all the system. In this study we design the test chip which plays edge detection by Laplacian operator. In CAD simulation, the processing time of the edge detection takes about 10 μsec using 2 μm CMOS design rule. In fabrication, grinding and chemical-mechanical polishing techniques are used to thin the wafer to 30 μm . The thinned wafer with buried interconnections is bonded vertically to a thick wafer through micro-bumps after careful alignment by the newly developed wafer aligner with the alignment tolerance of 1 μm . The microvision system with 3D integration structure can be fabricated by repeating such sequence.

1 Introduction

In intelligent robots which work in dynamic environment, it is desirable that the comprehension of dynamic task or environment and the generation of the appropriate action are carried out in real-time. For efficient visual servoing, it is known that the processing sampling rate of 100 μs - 1ms is required in general. In addition, tracking of ultra-high speed motion or analysis of ultra-high speed reaction, very fast real-time vision is needed.

However, in conventional vision system, digital image processing and analysis have been performed using conventional general-purpose computers in which programs and data are stored in the same memory unit and all operations are serially executed. As a result, operations of two-dimensional (2D) image data arrays require a large

amount of computing time which make difficult to process and analyze image data in real time.

A number of vision systems which tried to process and analyze image information in real-time have been developed [1]. Some of them have partial parallel processing in software or hardware, but the sampling rate of the processing basically depends on the video rate of 33 ms because of the systems using conventional input devices. Trying to overcome these problems, the scale-up model of the massively parallel processing vision or one chip vision have been developed [1]-[3]. However, the requirements of downsizing of system and high speed operation of image data in real-time analysis of dynamic scene are not fully satisfied.

In this research, we design the microvision system which has three-dimensional(3D) integration structure and process the 2D image data arrays as the flow of 2D data arrays itself in parallel[4]. The basic concept of the real-time microvision system is represented in Figure 1. Each LSI layer has a basic function, such as, amplifying and converting image information signal and some arithmetic operation, etc. A number of LSI layers are fabricated vertically by the newly developed 3D-LSI technology. So, the data is transferred vertically using high density vertical interconnections. As a result, the microvision system can be expected for dramatic improvement of the processing speed. The microvision system is also expected for vision system of mini or micro-robots because of its compactness.

We design the test chip which plays edge detection by Laplacian operator. The circuit of photodetector, amplifiers and AD converters are designed in VLSI CAD system. Also the processor elements which provide simple arithmetic operation are designed by the method of wired logic control in VLSI CAD system. The circuits of the test chip are presented in the next section.

We have developed the new 3D-LSI technology based on wafer bonding technique using micro-bumps to fabricate the microvision system[5]. The Si substrate of the 2D-LSI which has the basic circuits is ground and

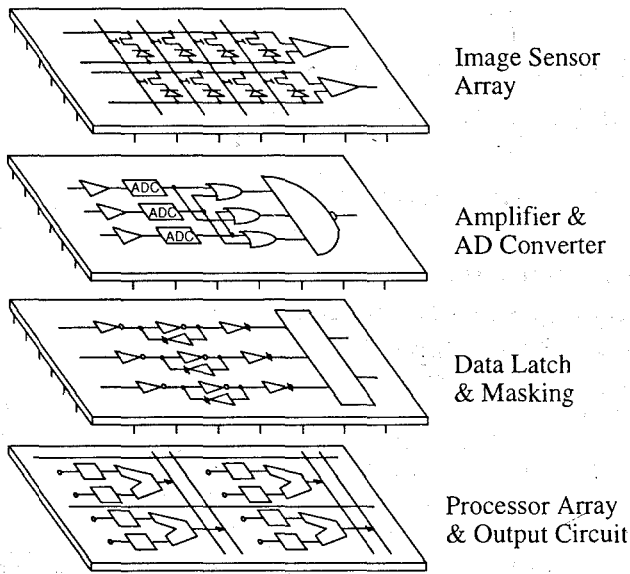


Figure 1: Basic concept of real-time microvision system with 3D integration structure

polished to make thin wafer. And the thinned wafer is aligned and bonded vertically onto a thick wafer by the 3D wafer aligner with the alignment tolerance of $1\ \mu\text{m}$. 3D-LSI can be fabricated by repeating such sequence. The fabrication sequence of 3D-LSI is introduced in a later section.

2 System Configuration and Design

2.1 System Configuration

The configuration of the unit system is represented in Figure 2. The sixty-four (8×8) photodetectors are considered a unit system. A number of unit systems are implemented depending on the scale of input image. Considering the device area of each LSI layer, we determine the corresponding ratio for devices between the respective layers as shown in Table 1. The system consists of a number of 2D LSIs vertically stacked using 3D LSI technology introduced in section 4. Each LSI is connected vertically using high density vertical interconnections. So, 2D image signals are transferred vertically at the same time and processed parallel in each LSI. The microvision system has some processing parts. At first, the optical image signals are detected and converted to the electric signals. The electric signals are amplified, restored and modulated and so on. The manipulated electric signals are digitized, and some operations for the image informations are performed in the processor. Finally, the processed informations are transferred to high level processors or some visual devices using 2D or 1D interconnections. The processings methods mentioned

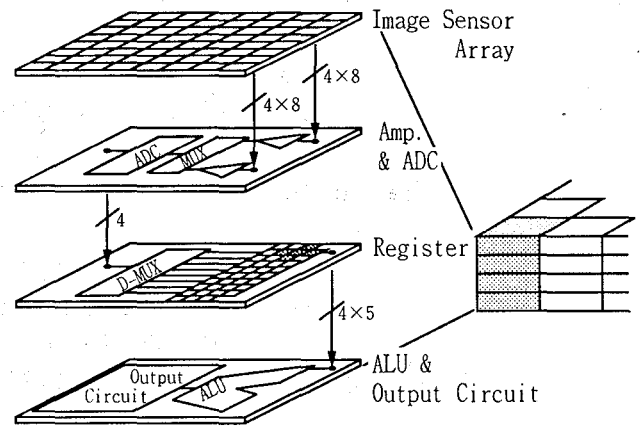


Figure 2: Description of unit system of real-time microvision system

Table 1: Configuration of unit system

Layer	No. of device
1st layer	8×8 photodetectors
2nd layer	2 amplifiers and 1 ADC
3rd layer	1 register
4th layer	1 ALU and output circuit

above are performed parallel in each LSI and in pipeline over all the LSI layers.

2.2 Design of Test Chip

We have designed the test chip using $2\ \mu\text{m}$ CMOS design rule which plays edge detection by Laplacian operator.

2.2.1 Photodetectors

The 4×8 photodiodes are precharged and then charged by the acceptance of light. The charging rate is proportioned to the intensity of the light. The charged state of the photodiodes are stored in the capacitors. And then the stored electric charge in the capacitors are transferred sequentially to the amplifier.

2.2.2 Amplifier and AD Converter

The current mirror sense amplifier is adopted. The zero gain frequency is $3.35 \times 10^8\text{ Hz}$. The gain margin of the amplifier is about 2.6 dB at the frequency of $4.06 \times 10^8\text{ Hz}$. It can be said that the amplifier is operated in stable. In the AD converter, the parallel conversion method is adopted. The four bit ADC with the conversion frequency of 25 MHz is implemented in the test chip.

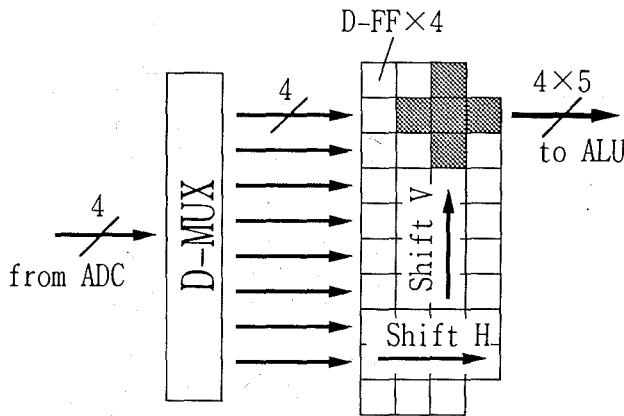


Figure 3: Register unit

2.2.3 Register

The block diagram of the register unit is represented in Figure 3. The registers have array of four bit D-flip flop in which the digitized value of input pixels with neighboring pixels of the verges are stored. The registers have two shift operation: the one shifts all the registers from the left to the right in turn (Shift H) and the other shifts right three columns of the registers from the bottom to the top in turn (Shift V). Combining the two shift operations, we shift the registers which are the candidate of the operation to the center of the gray regions with the neighboring registers in turn. The gray regions of the registers are transferred to the arithmetic logic unit (ALU) by the multiplexer.

2.2.4 ALU

The ALU consists of carry lookahead adder, register, counter and multiplexer. The operation time of the carry lookahead adder is 13 nsec. The ALU plays the edge

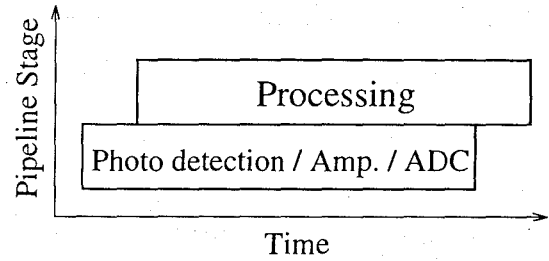


Figure 5: Pipeline process

detection using the Laplacian operator. The Laplacian operator based on the 2nd derivative detects the peak of the density change. For the pixels of 4-neighborhood, the Laplacian operator takes the following operation:

$$g(i, j) = f(i, j - 1) + f(i - 1, j) + f(i + 1, j) + f(i, j + 1) - 4f(i, j),$$

where $g(i, j)$ is the operation result of the pixel $f(i, j)$. In the processor, the wired-logic control method is adopted for high speed operation.

2.2.5 Parallel and Pipeline Processing

The configuration of the unit system is shown in the previous section. In application, a number of the unit systems are implemented in the vision system depending on the scale of input image. The interconnections of the multi-processor system which have four processor elements are shown in Figure 4. The sixty four (4×16) line and eight (4×2) line buses are used for the interconnections of the multi-processor system to transfer the data each other. Using the interconnections, the neighboring pixels' data of the verges of each processor element are transferred for the 4-neighborhood Laplacian operation. In the unit system, two pipeline stages are performed as shown in Figure 5. The first stage is the photo detection, the amplifying and the AD conversion. The second stage is the manipulation of the register and the operation in the ALU.

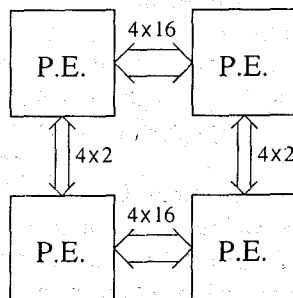


Figure 4: Block diagram of multi-processor system

3 Simulation

The timing of operation in the unit system is represented in Figure 6. Considering the the photodetector array as a matrix, the $(n - 2)th$ row data is operated in the ALU when the $(n)th$ row data is processed in the amplifier and the ADC. The timing of operation shows the processing of the two pipeline stages. The simulation result of the edge detection for multi-processor system which has four unit systems is represented in Figure 7. We can see that the operation of the edge detection is

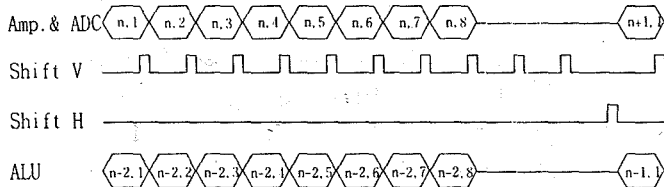


Figure 6: Timing of operation

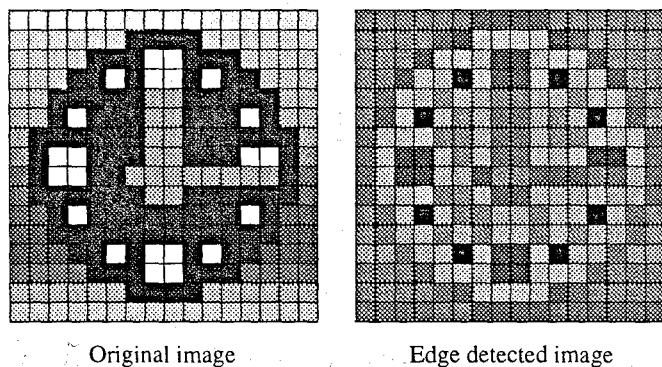


Figure 7: Example of edge detection

carried out successfully. The processing time of the edge detection takes about $10 \mu\text{sec}$.

4 Fabrication

In the past, the laser recrystallization technique is a leading candidate for 3D LSIs[6]. Also the 3D-LSI image processor which recognizes some letters had been developed using the method[7]. However, the 3D-LSI technology had not been employed in production because it was very complicated and expensive technology. In this paper, we propose more realistic 3D-LSI technology based on wafer bonding technique using micro-bumps[5]. The

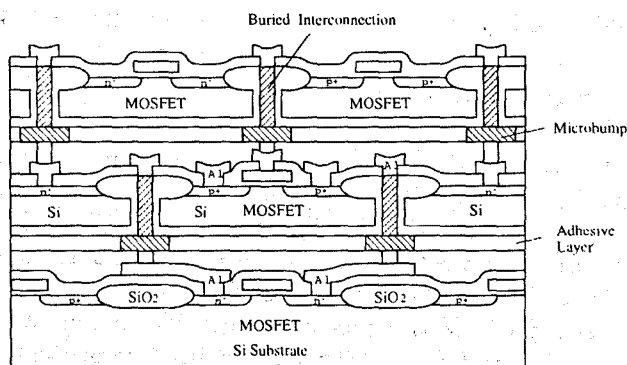


Figure 8: Cross-sectional view of 3D-LSI

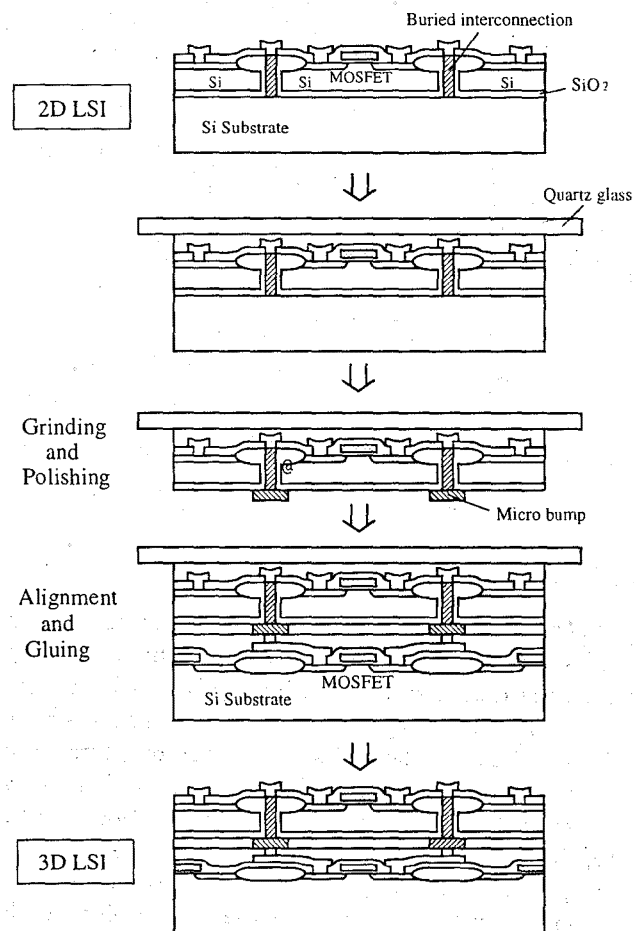


Figure 9: Fabrication sequence of 3D-LSI

cross-sectional view of the 3D-LSI is shown in Figure 8. The process sequence to fabricate the 3D-LSI is shown in Figure 9. At first, a 2D-LSI wafer with buried interconnections are prepared to fabricate 3D-LSI. The buried interconnections are used for vertical transfer of the data between the two 2D-LSIs. The buried interconnections are formed by depositing n^+ poly-Si into trenches which are formed through the field oxide. The 2D-LSI wafer with buried interconnections is glued to a quartz glass and then thinned to around $30 \mu\text{m}$ by grinding and chemical-mechanical polishing. For a wafer alignment, we have developed a new wafer aligner as shown in Figure 10. Wafer stage is precisely controlled with accuracy of 50 nm in x, y, z directions by piezo actuators in the aligner. Six inch wafers can be aligned with the alignment tolerance of $1 \mu\text{m}$. The thinned wafer is bonded to a thick wafer using In/Au micro-bumps with the minimum size of $5 \mu\text{m} \times 5 \mu\text{m}$ and UV hardening adhesive layer with thickness of $1 \mu\text{m}$ by forcing the z direction pressure after careful wafer alignment. We can monitor the wafer alignment through the ten layers using the infrared light equipped in the bottom of the aligner. The

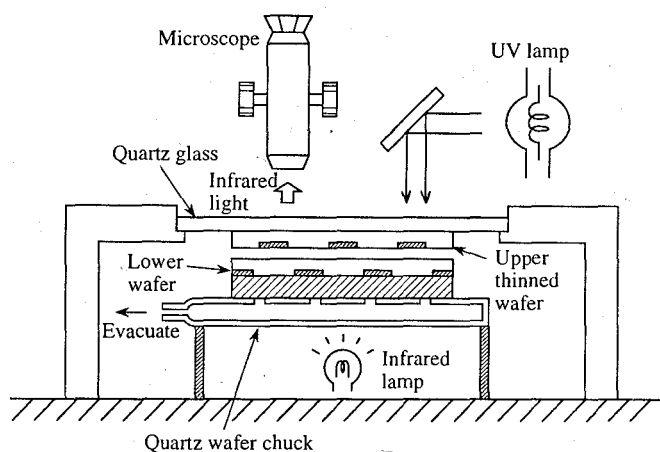


Figure 10: Schematic diagram of 3D wafer aligner

gap between two wafers are measured in-situ and precisely controlled during alignment. By repeating above sequence, the 3D-LSI can be fabricated. Good electrical contact was obtained between two micro-bumps after bonding by optimizing the micro-bump and bonding conditions. In the stacking of a number of LSI wafers, the problem of heat exhaust will occur and may limit the number of wafers to be stacked. To overcome the problem, we consider the low power consumed circuit in the design of each LSI.

5 Conclusion

The development of the real-time microvision system with 3D integration structure is introduced. By stacking a number of 2D-LSIs vertically, we can process and transfer 2D image informations as it is through the high density vertical interconnections. In the microvision system, the image informations are processed parallel in each layer and the processings are performed in pipeline over all the layers. In CAD simulation of the edge detection by Laplacian filter, the good operation was obtained and the processing time takes about 10 μsec using 2 μm CMOS design rule. The microvision system is also expected for vision system of mini or micro-robots because of its compactness. The 3D-LSI technology based on wafer bonding technique using micro-bumps has been developed to fabricate the microvision system.

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