

Silicon-on-insulator

SOI technology and ecosystem

Emerging SOI applications

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SOI basics, history and manufacturing capacity

SOI substrate 101

- Cross section through a blank SOI wafer

Silicon Film (< 10nm to > 1000nm) →

Buried Oxide (~ 10 nm to > 100 nm) →

- Substrate provides
 - mechanical strength
 - typical total wafer thickness:
 - ~ 1 mm = 1,000,000 nm

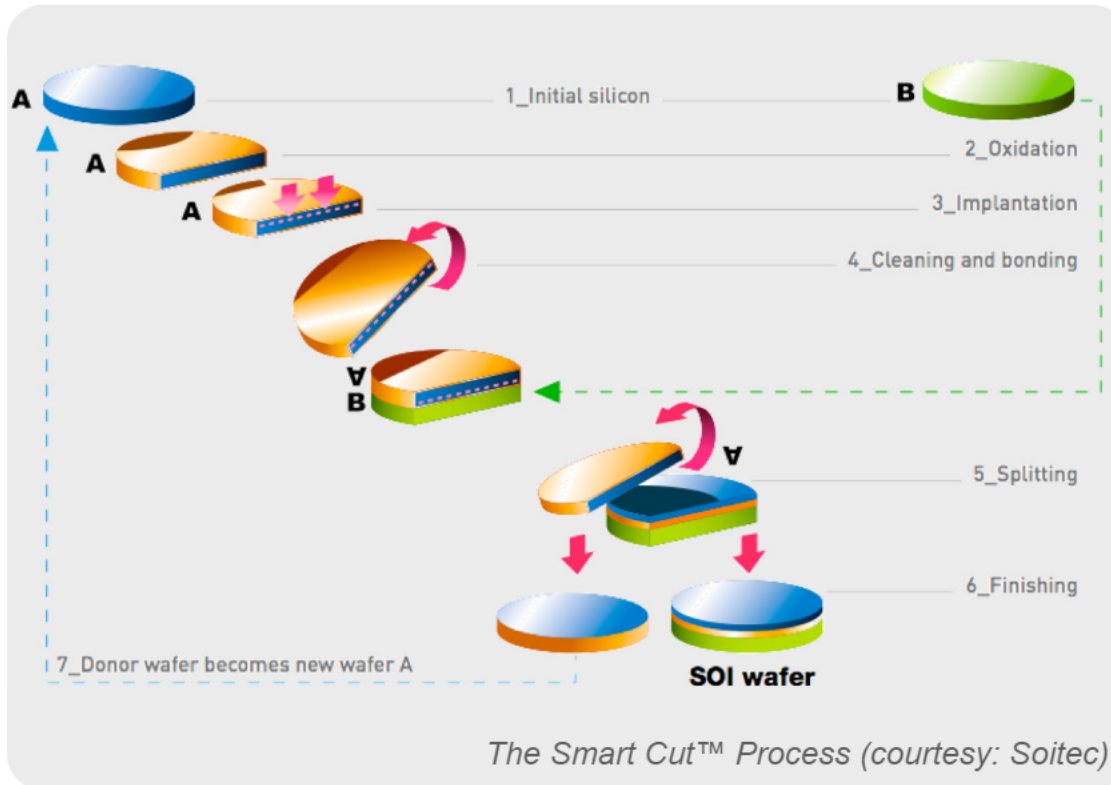
Silicon

BOX

Substrate

*Drawing is
NOT to scale!*

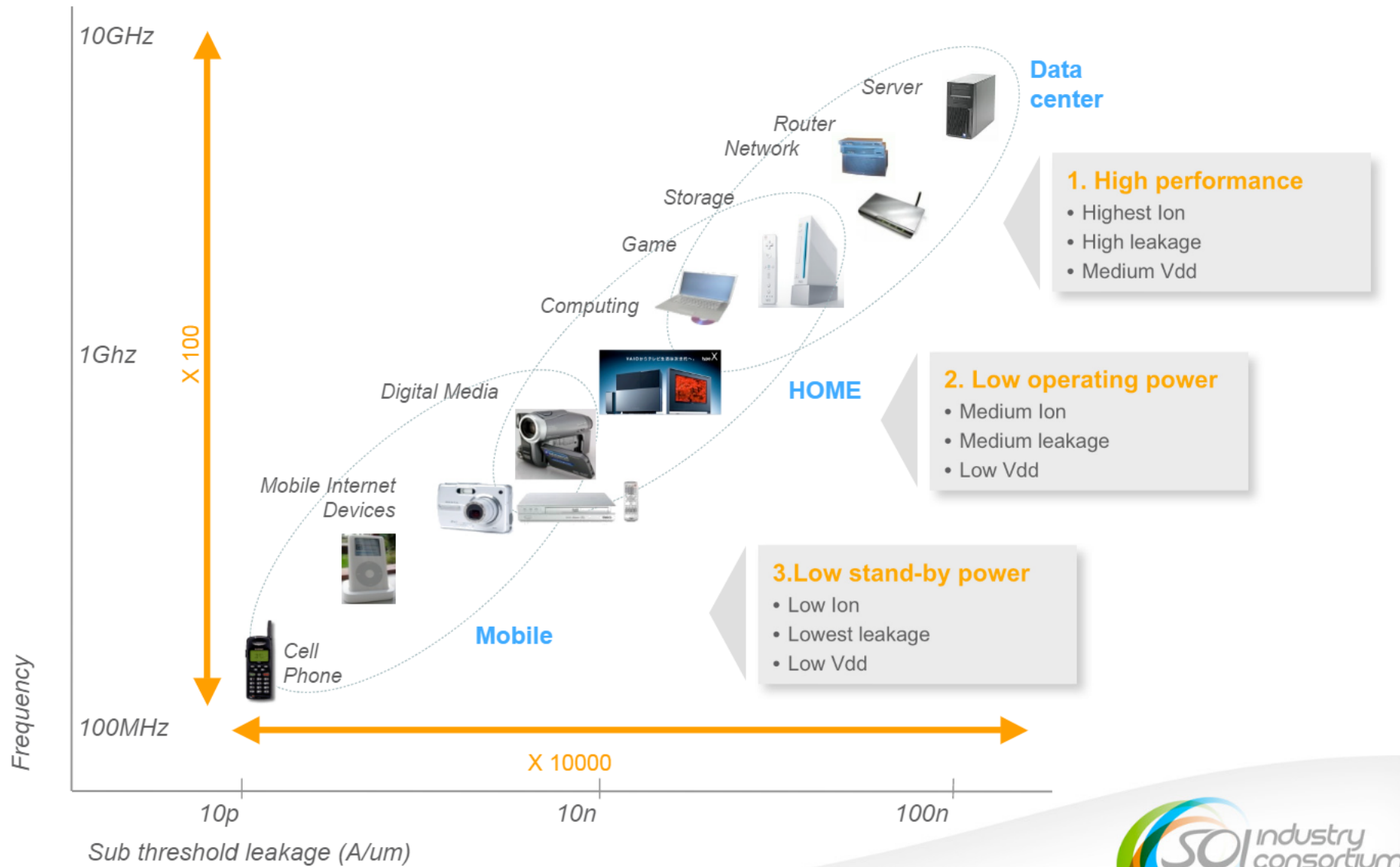
Cross section through
a blank SOI wafer



The inherent advantages of SOI are essential today

- Compared to bulk-CMOS, SOI technology offers
 - Lower power, 30- 40% lower power (or higher performance)
 - Less process complexity and variability
 - More reliable: 10x soft error rate reduction and no latch up
 - FD- SOI/ FinFET: stable SRAMs
 - Simplifies Digital, Analog and RF integration in SoCs
- Increasing variability and complexity in Bulk-CMOS are making it exceedingly difficult to meet the design windows for < 45nm
 - Power
 - Short channel effects
 - Variability and complexity
 - V_{th} mismatch

CMOS applications and operating ranges



Significantly increased SOI foundry capacity

Creating A Global Leader in the Foundry Business

The Foundry Company will be a 'new global enterprise' combining talent and resources from around the world to serve a growing global demand for leading-edge foundry services.

Technology Leadership

- Deep partnership with IBM
- Aggressive 32/22/15 nm roadmap
- Bulk and SOI

Manufacturing Excellence

- World class expertise, yields, and cycle times
- APM technology
- Best in class fabs built on LEAN principles

Leading-edge Volumes

- Industry's most advanced products in independent foundry
- Time to market
- Scale

Capital Funding

- Initial funding of \$1.4B
- Minimum committed future equity funding of \$3.6B and up to \$6.0B in total capital

Capacity Roadmap

- Industry leading capacity roadmap
- Fab 36, commitment to build out Fab 38, Upstate New York, and more...

Global World-class Team

- Experienced executive team
- Highly educated workforce



IBM's SOI offering is also enlarged

■ A fully enabled 45nm SOI foundry offering

– Value Proposition

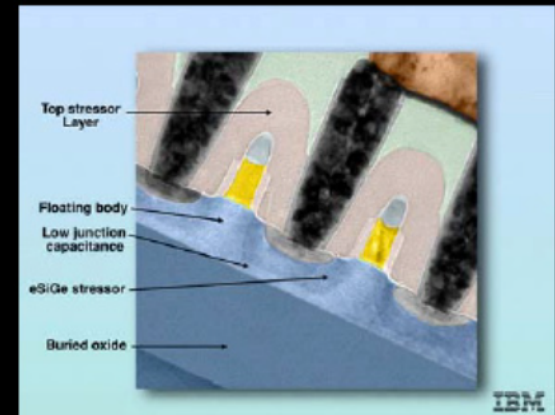
- 6th generation of SOI technology
- Brings industry leading power/performance to our foundry clients
- Broad transistor menu from high performance to ultra low power
- Natural follow up to our 45nm SOI ASIC offering

– Enablement

- ARM libraries [SC, Memories, I/Os]
- EDA views from Synopsys, Cadence, & Magma
- ASIC IP portable to foundry environment
- Dense embedded memory

– Availability

- Production PDK available now
- MOSIS MPW program



The product issues from current
Silicon technology are more than a challenge;
they are an inflection point

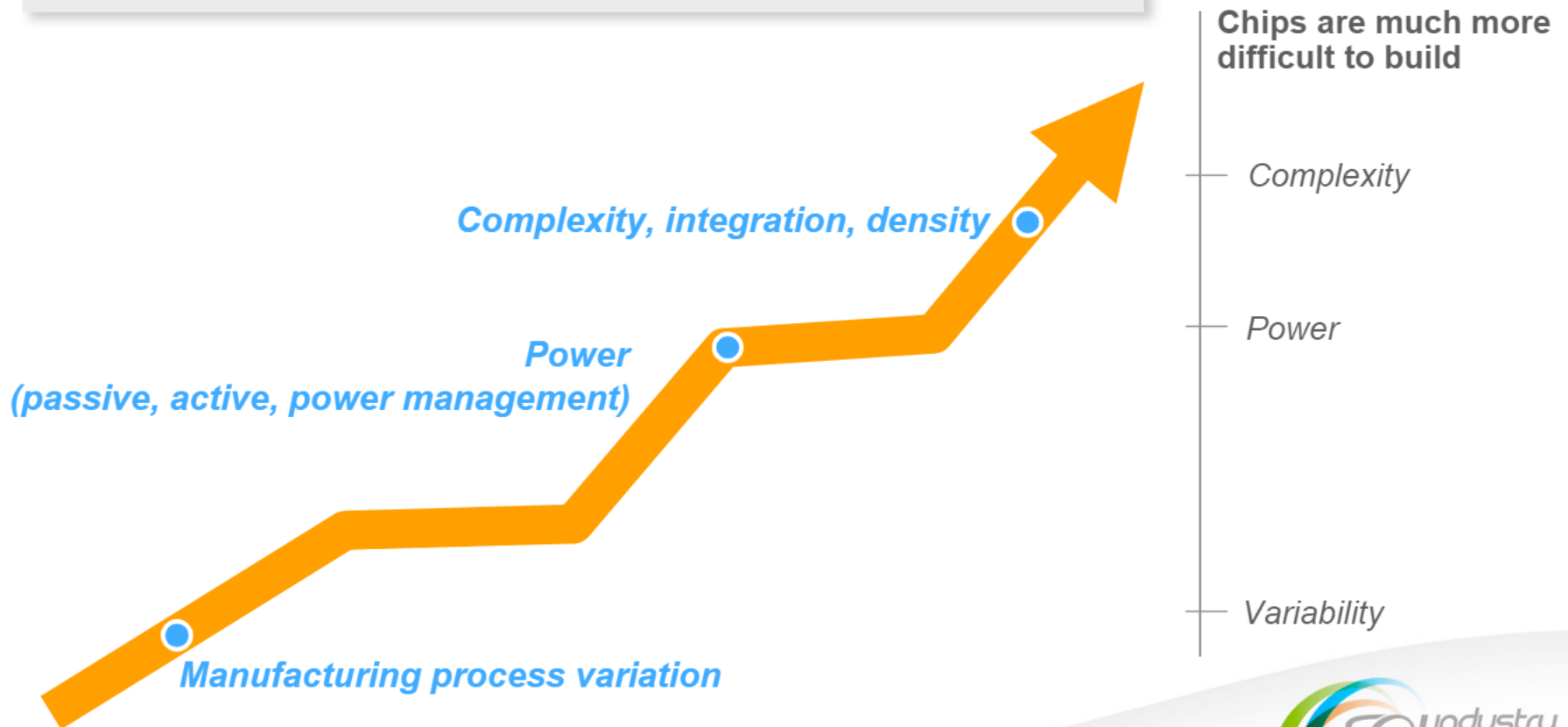
Increasing challenges with today's options

- The “traditional” challenges have become critical

- Power
- Variability Control AND Complexity



*Interdependent
like never before*

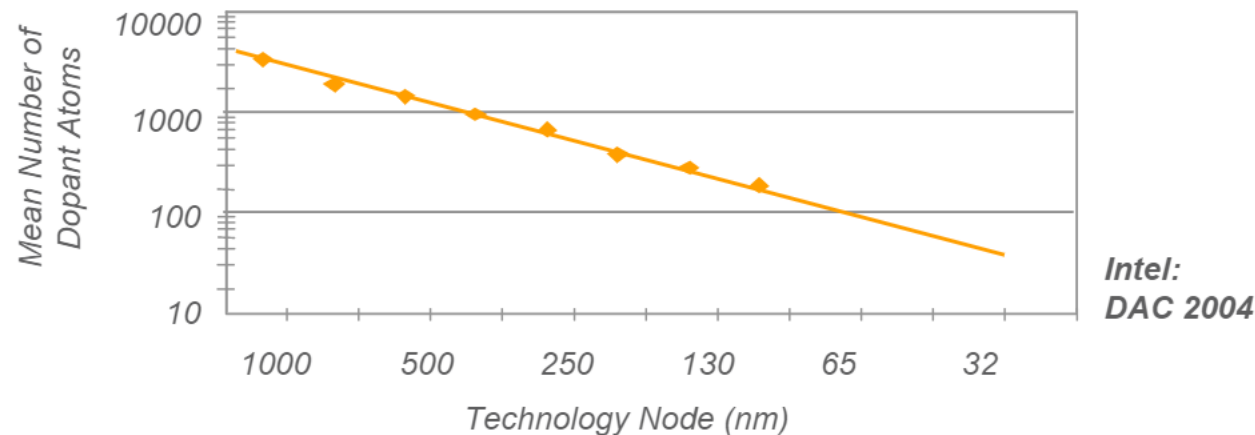


Increasing challenges with today's options

Sources of variability

- Channel length
- Channel width
- Oxide thickness T_{ox}
- Random dopant fluctuation (RDF)
- Line edge roughness

→ RDF is 60% of total variation at 45nm



Chips are much more difficult to build

Performance

Complexity

Power

Variability

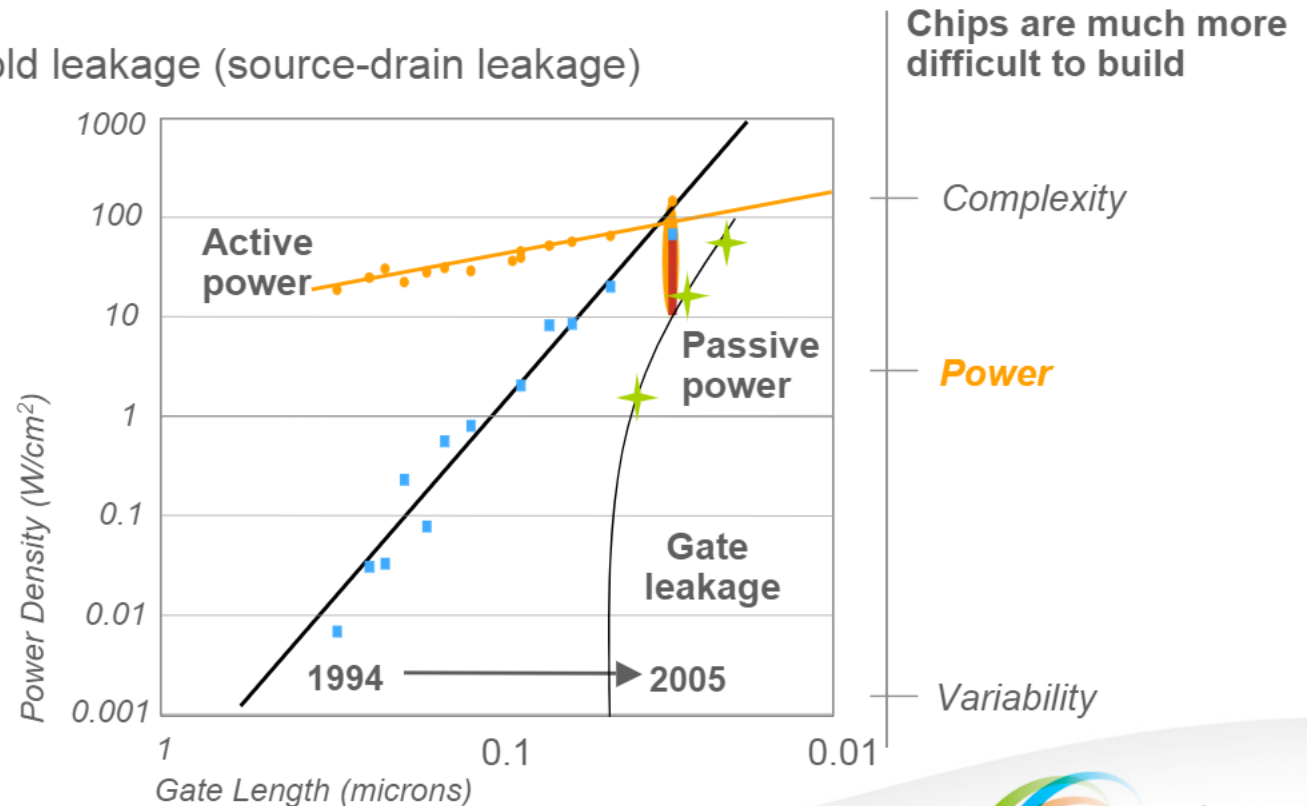
→ All variation can be translated into V_{th} variation

- Higher leakage
- Increased power

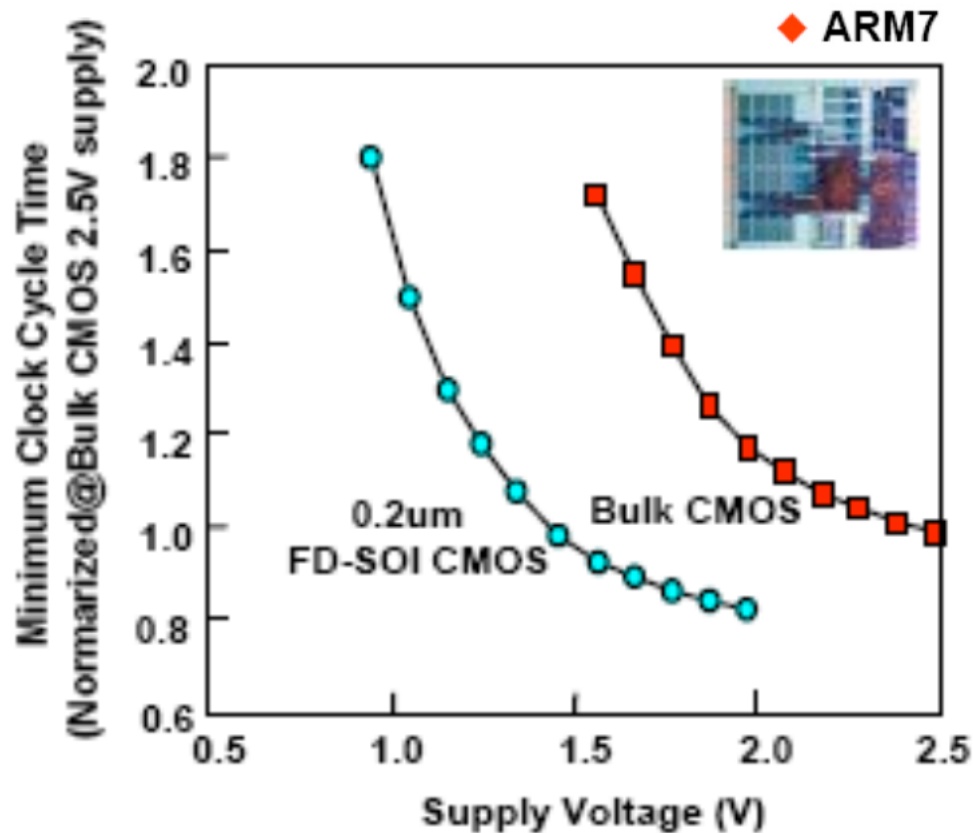
Increasing challenges with today's options

- Power problems peaking

- Active power
- Passive power
 - Sub-threshold leakage (source-drain leakage)
- Gate leakage



SOI provides a viable low-power solution



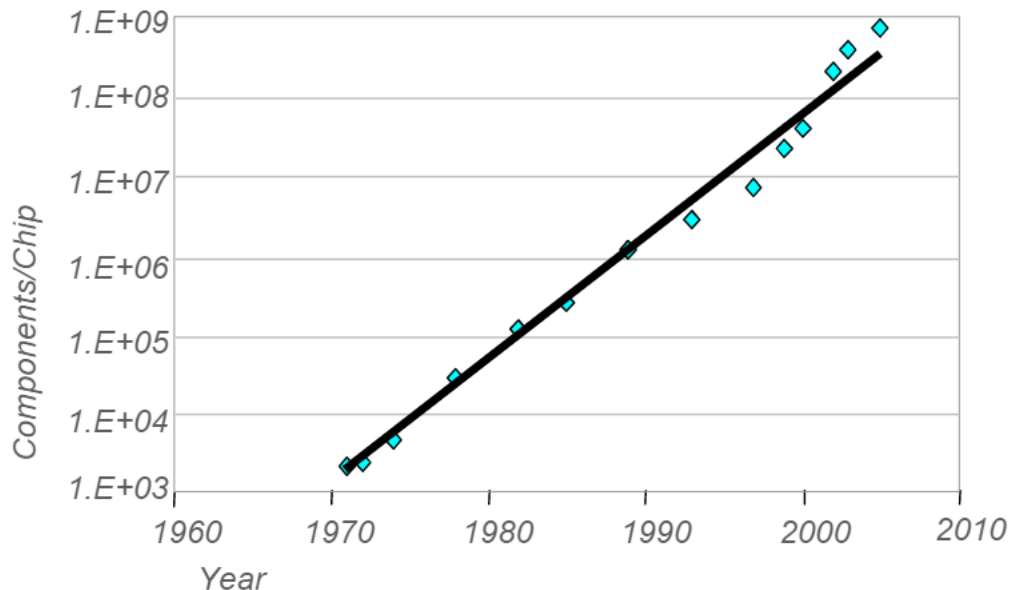
Fully depleted SOI
FD-SOI
Implementation

ARM7

▶ 1/3 power consumption
of bulk device with
same performance

Increasing challenges with today's options

- Complexity increasing exponentially
 - 5-10 billion transistors per microprocessor in the next 12-18 months
 - Controllability of variations and of the static leakage **will likely prevail** over speed and density



Chips are much more difficult to build

Complexity

Power

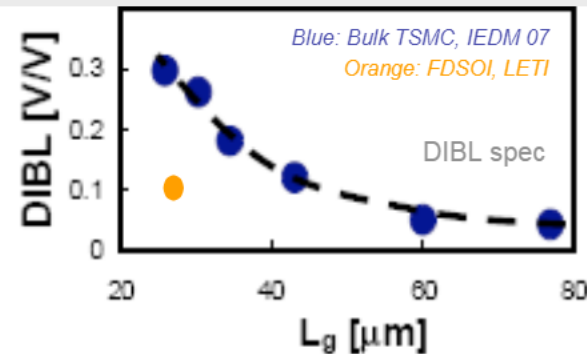
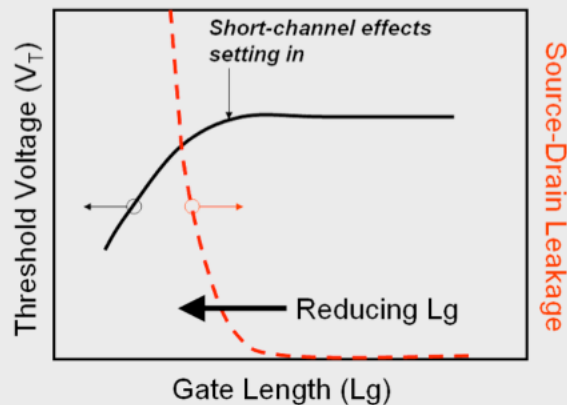
Variability

The key limitation of bulk CMOS: uncontrolled leakage

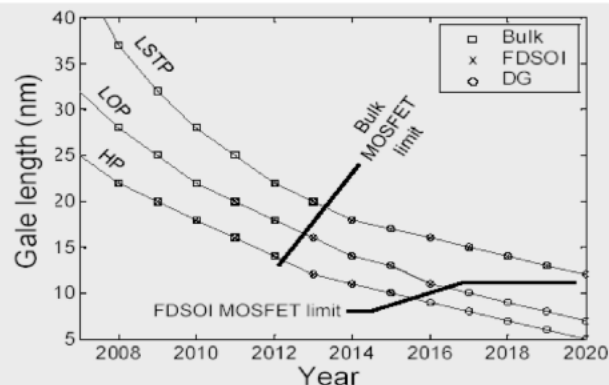
- Amplified short channel effects → main challenge for bulk as scaling continues
- Current solutions are insufficient:

Relax leakage spec → increased static power

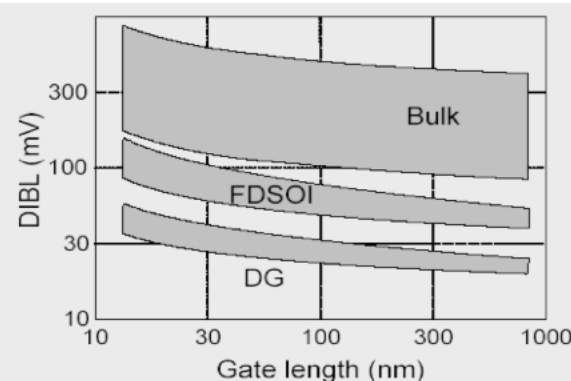
Slowdown L scaling → decreased performance & density → higher cost



(source: Leti – O. Faynot)



(source: ITRS 2005)

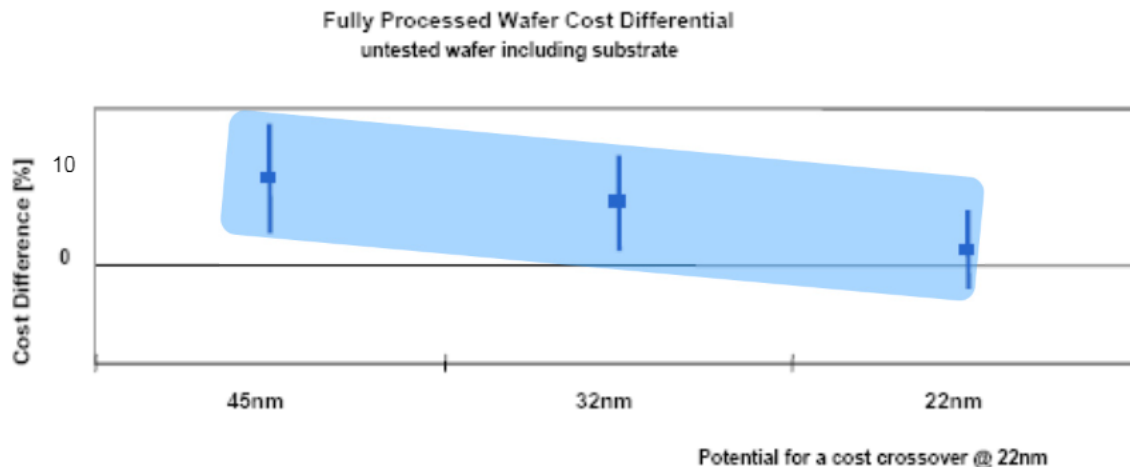


(source: JP Colinge calculated using MASTAR model)

Economics discussion

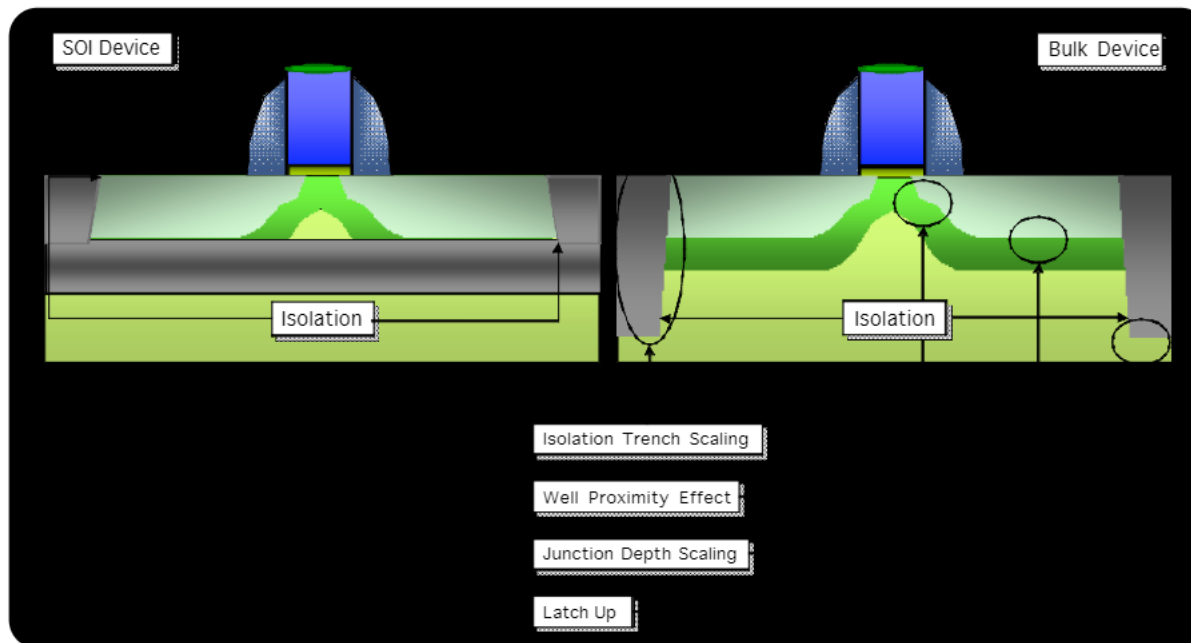
Factors driving economics

- The cost differential between bulk and SOI narrows with each generation. The factors driving are:
 1. Raw wafer differences are being reduced, caused by:
 - Higher volumes
 - Continuous process improvements
 2. Bulk scaling issues drive process complexity (see next slide)
 3. The cost crossover will begin at 32nm, most devices will crossover at 22nm



Bulk problem areas for scaling

- Process complexity issues with bulk scaling drive up cost
 - Isolation scaling and well proximity effect
 - Isolation aspect ratio getting larger in bulk
 - Trench etching and filling driving innovation/complexity
 - Shallow junction technology required by scaling
 - More complex problem in bulk
 - SOI has a natural junction “stop” that mitigates many of the issues



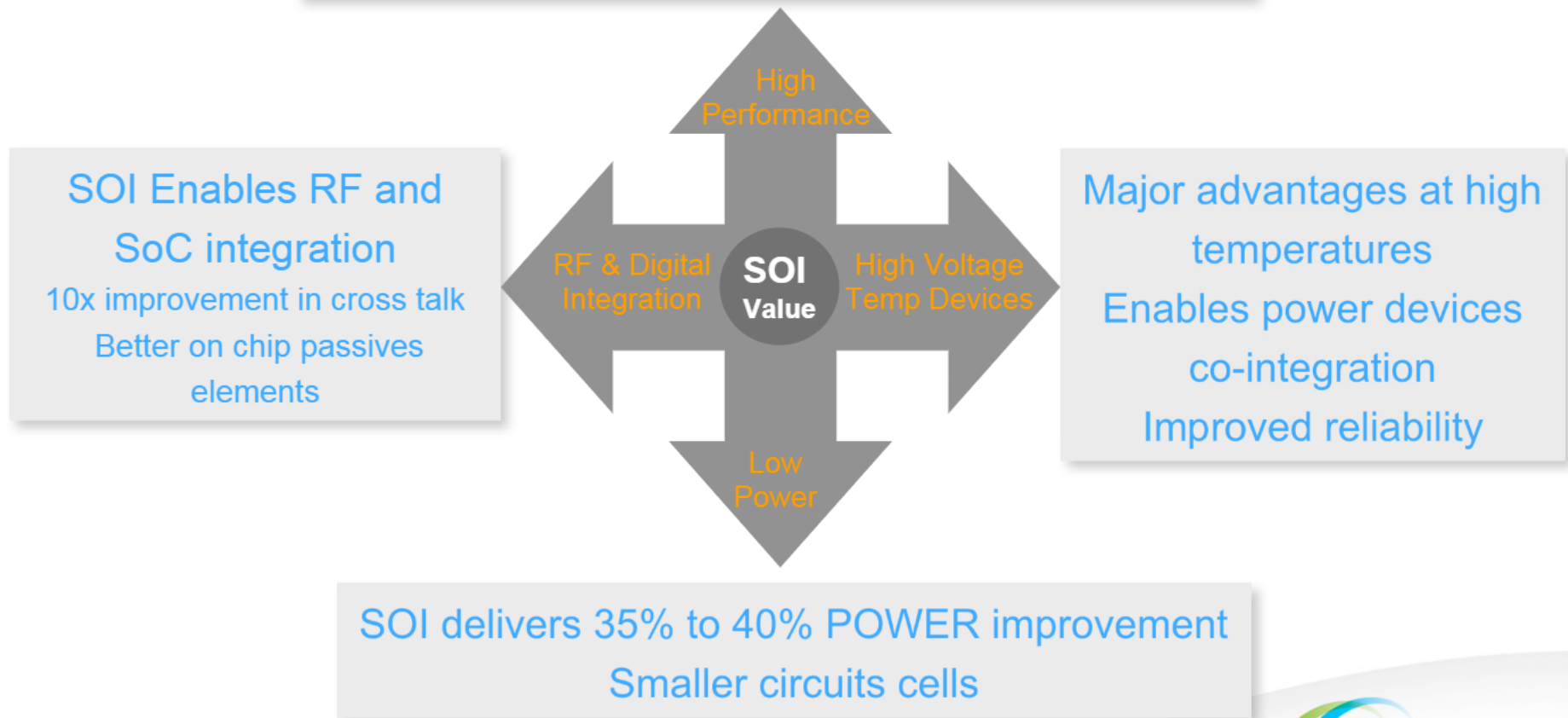
SOI applications

SOI is part of your daily life!



SOI Enables the best performance per Watt

SOI delivers > 20% performance improvement
High reliability (10 x SER)

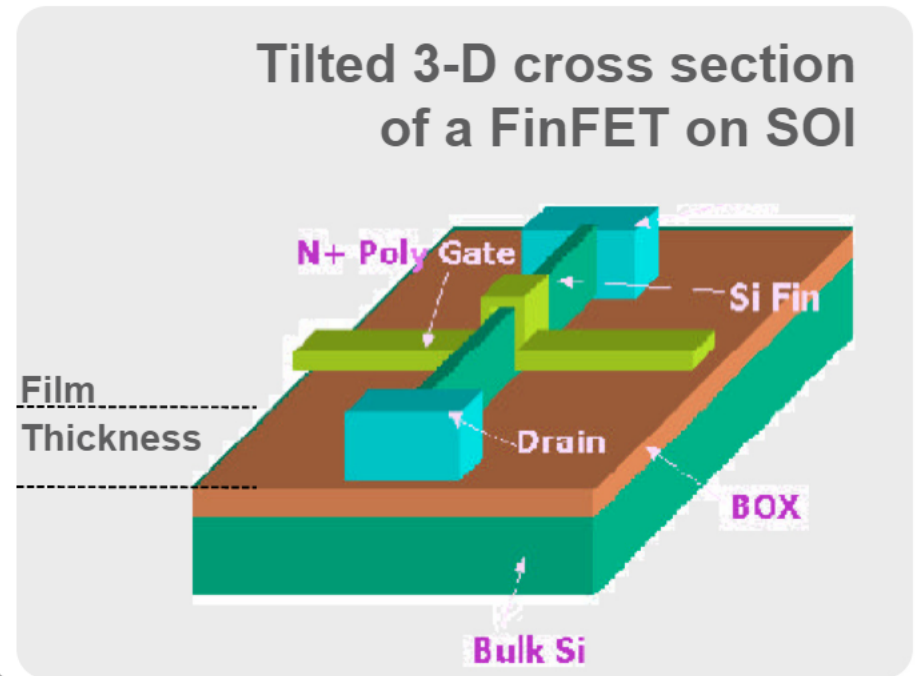


Emerging SOI application:

FinFETs manufacturing low variability & low cost

Challenge: In bulk-CMOS it's difficult to achieve an exact fin-height and minimize this additional variability.

Solution: The top silicon film thickness in SOI wafers varies only slightly (few %) and minimizes this additional source of variability → less design margin required = higher performance, less area, better yield.



http://www.rit.edu/kgcoe/ue/ameccontent/3_Rahman.pdf



Emerging SOI application:

Optical active cable

Challenge: In data centers connections between racks must be extremely fast to support system speed.

Solution: SOI technology minimizes coupling and power dissipation. It allows to integrate multiple high-speed channels reliably in a small form factor. Also, SOI simplifies manufacturing of wave-guides to interface CMOS circuits with optical fibre.



Blazar LUX5010

*Multirate 4x10G
Optical Active Cable
powered by drivers/receivers
in 0.13um SOI*

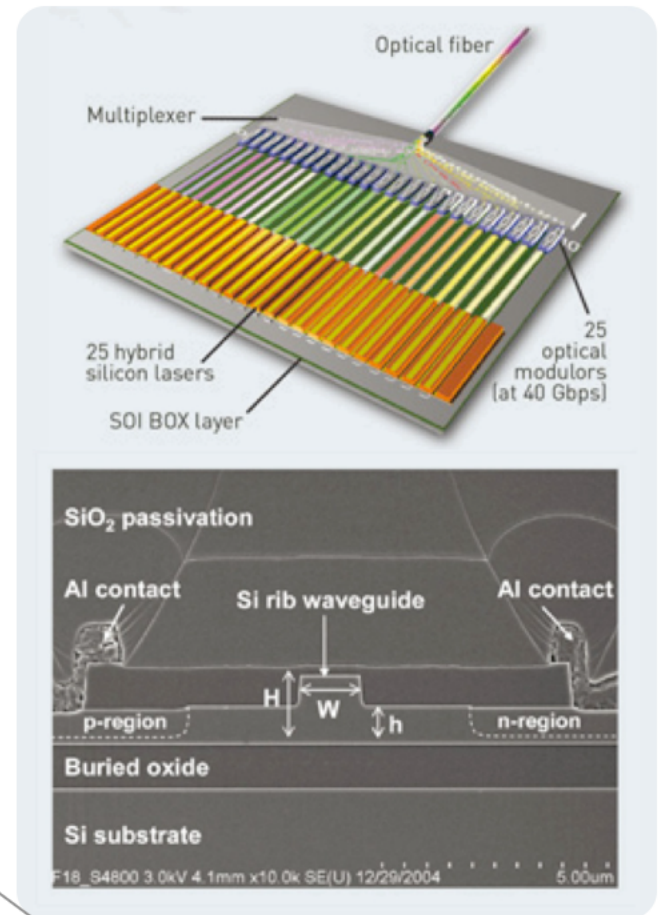


Emerging SOI application:

Optical waveguides

Challenge: To minimize signal loss and cost for optical interconnects both noise isolation and precision manufacturing are essential for highly integrated solutions.

Solution: SOI Technology enables – for example – to combine on one die 25 silicon lasers (with different frequencies) with 25 40 Gbps silicon modulators and multiplex them into one output fiber.

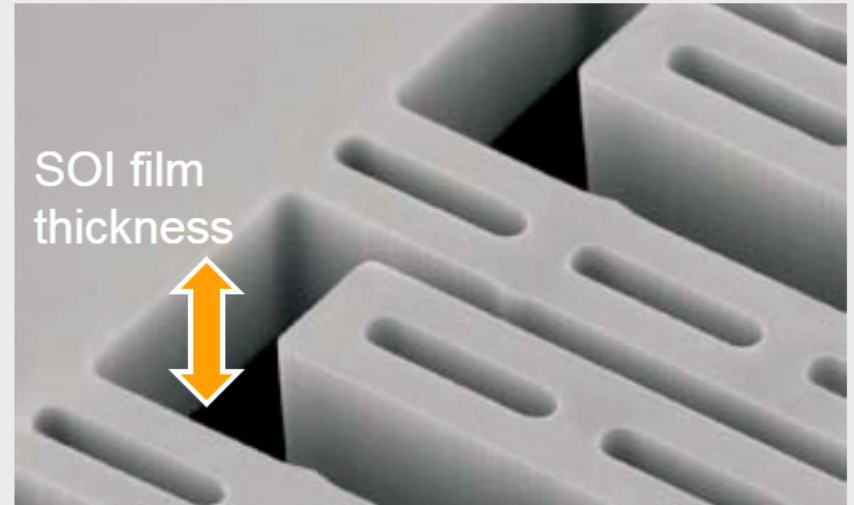


Emerging SOI application:

High-precision MEMS

Challenge: It's very difficult to achieve tight tolerances in the Z-axis (= etching depth) with bulk-CMOS wafers.

Solution: Etching MEMS out of SOI wafers guarantees very tight tolerances in the Z-axis, because the SOI film thickness can be very tightly controlled by the SOI wafer manufacturer.



MEMS revenues:

8 B\$ in 2008
16 B\$ in 2012

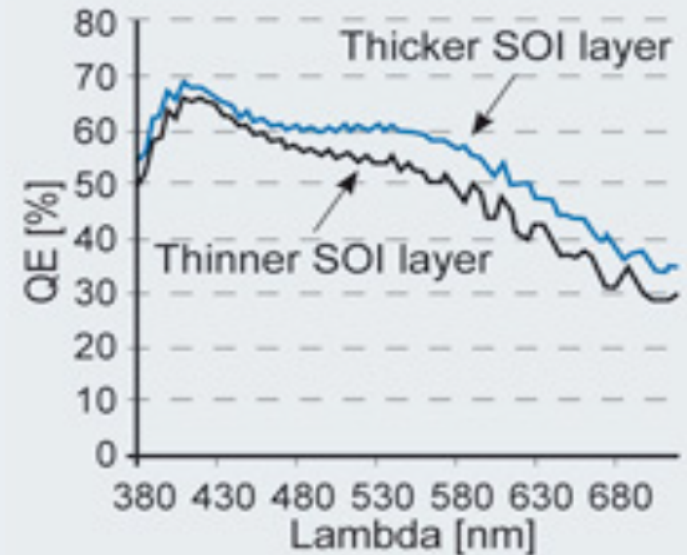


Emerging SOI application:

CMOS Image Sensor

Challenge: Less expensive cameras and mobile phones demand small and low-cost image sensors, without trading off sensitivity or quantum efficiency.

Solution: The oxide layer in the SOI wafers acts as an etch-stop and allows accurate and low-cost manufacturing of very efficient and highly sensitive image sensors, using back-side illumination.



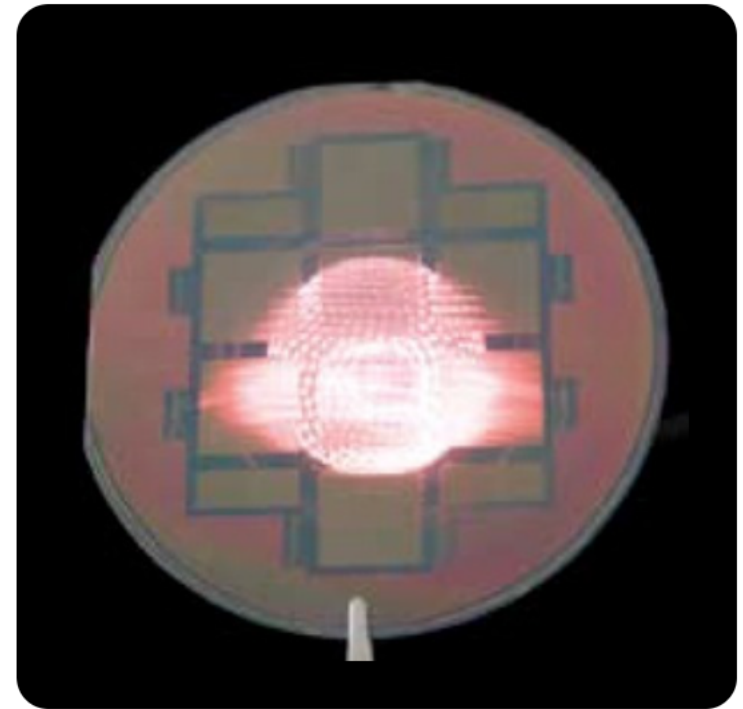
3-Megapixel image sensor

Emerging SOI application:

CMOS image sensor

Challenge: Less expensive cameras and mobile phones demand small and low-cost image sensors, without trading off sensitivity or quantum efficiency.

Solution: The oxide layer in the SOI wafers acts as an etch-stop and allows accurate and low-cost manufacturing. Very uniform thinning of 300mm wafers, down to 5 μm or less, is possible and allows low-cost and high-quality CIS manufacturing.



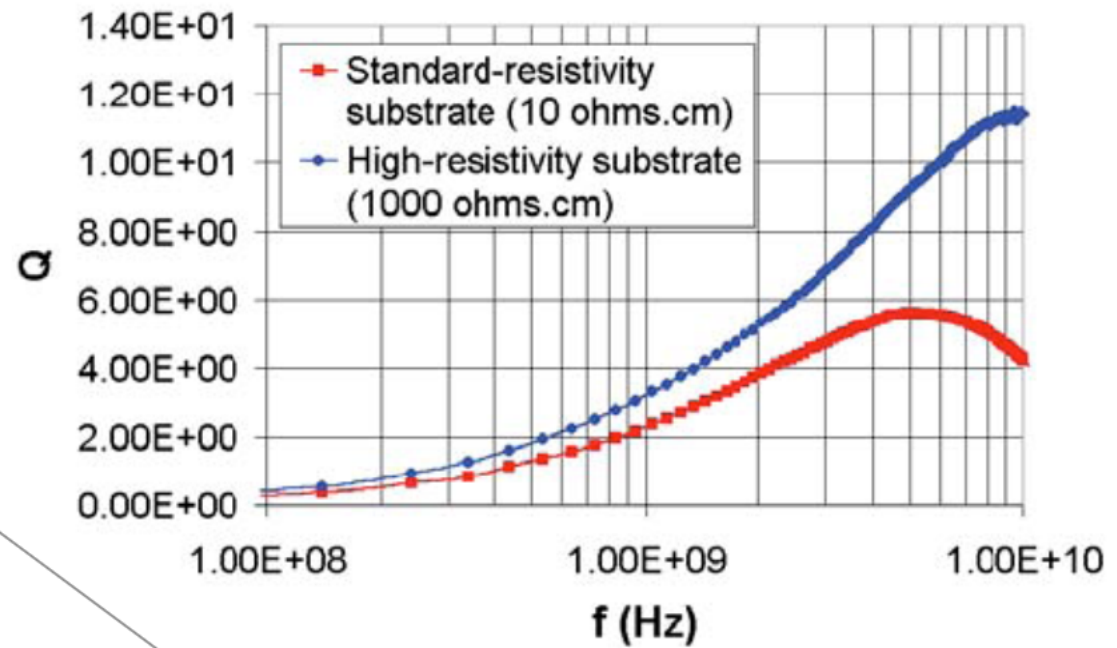
**Light passing through
a thinned silicon wafer**

Emerging SOI application:

Multi-GHz RF circuits

Challenge: In bulk-CMOS substrate currents reduce Q of inductors, especially in GHz range.

Solution: In SOI wafers the top silicon film can be of low resistivity, while the silicon substrate can be very high resistivity material → significantly improving the quality of passive components.



1.5 nH Spiral Inductor

*Why all the buzz about SOI in
RF Design Magazine, Oct 2003*

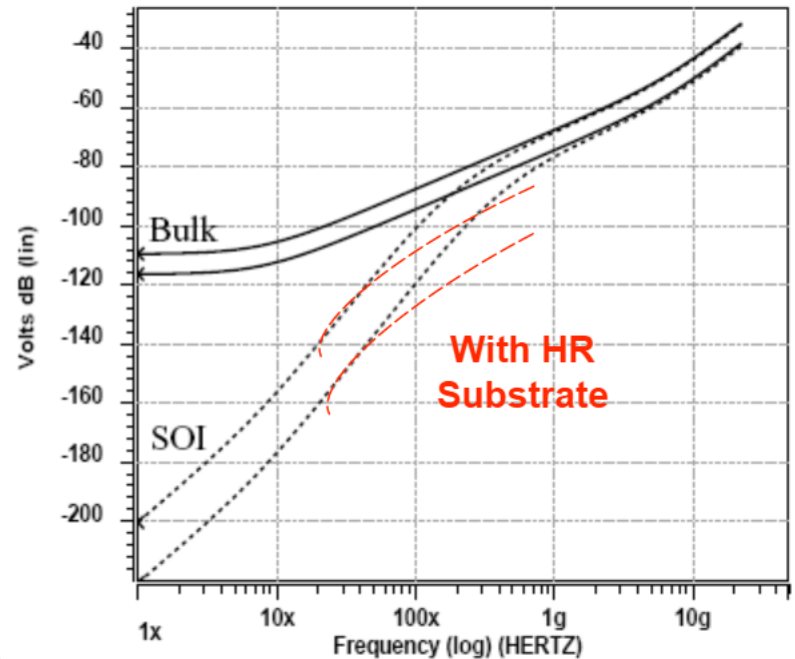
Emerging SOI application:

Analog & M/S circuits

Challenge: Analog circuits are sensitive to coupling from adjacent analog circuit elements and digital circuitry.

Solution: The BOX in SOI wafers reduces cross-currents & coupling through substrate significantly. Use of high resistivity substrate extends this SOI benefit by another 1 – 2 frequency magnitudes.

➔ Area savings and higher quality analog circuits.



Magnitude responses from the digital to the analog region for two different test structures.

http://www.es.isy.liu.se/publications/papers_and_reports/2005/RVK05_erikb.pdf

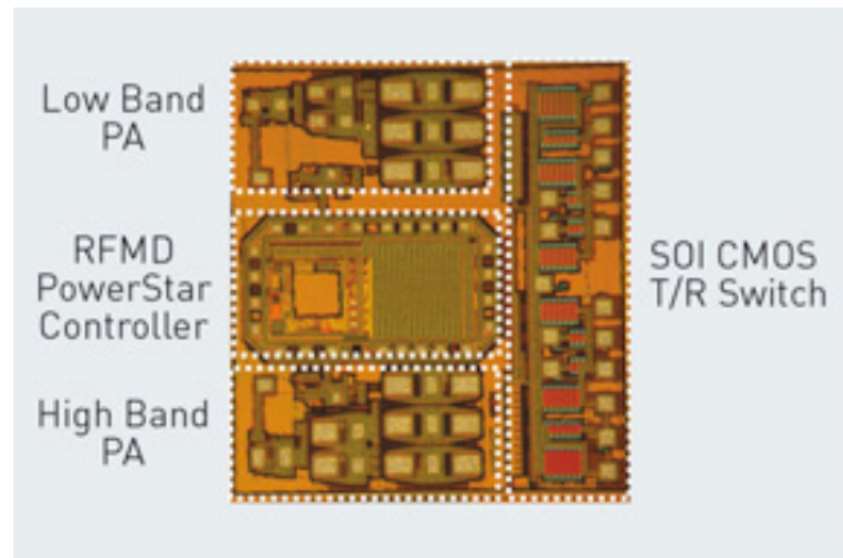


Emerging SOI application:

Highly integrated radio

Challenge: In bulk-CMOS it's difficult /costly to separate sensitive circuit elements sufficiently, due to significant substrate- and cross-coupling.

Solution: The BOX in SOI wafers isolates the active circuitry from the HR-substrate and minimizes these coupling effects. Also, the lateral oxide isolation between circuit elements separates transistors better than junction isolation and consumes less area.



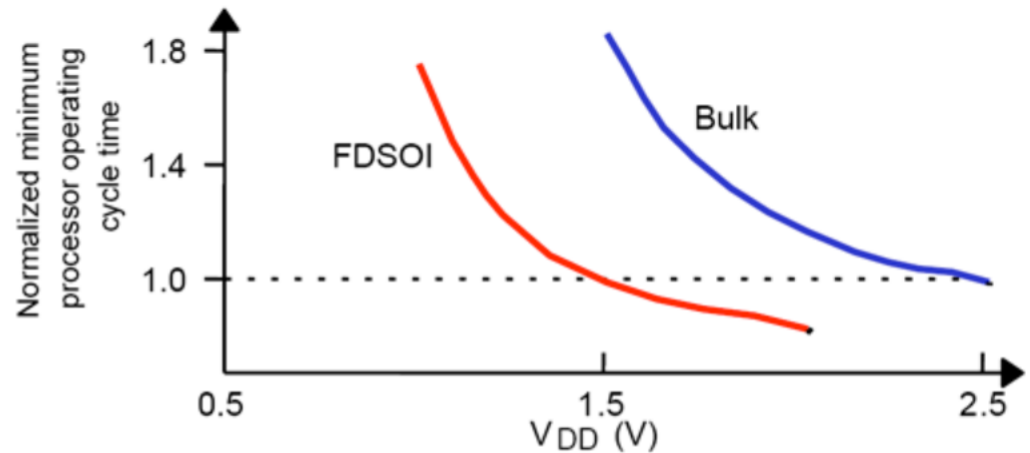
Uses thick-film SOI and high-resistivity substrate to reduce area and power

Emerging SOI application:

Ultra-low power and ultra-low voltage designs

Challenge: Bulk-CMOS circuits operate well above $\sim 0.9\text{V}$, but not significantly below this level.

Solution: In fully depleted SOI substrates the silicon film thickness determines the threshold voltage. FD SOI allows significantly lower supply voltages and/or significantly higher Clk-speeds at a given supply voltage.

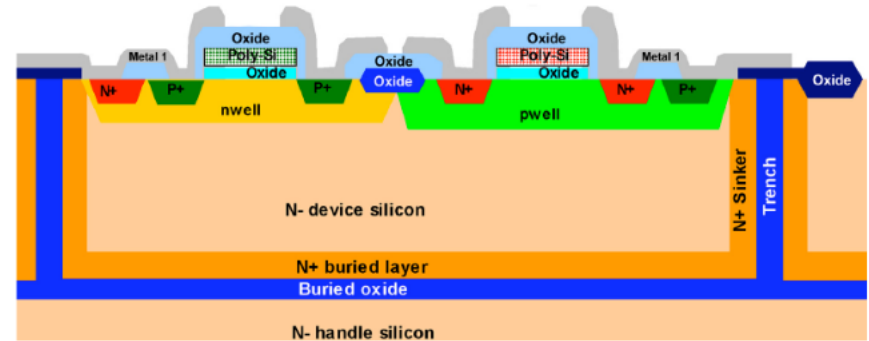


Cycle time in bulk and FD SOI processors vs. supply voltage.

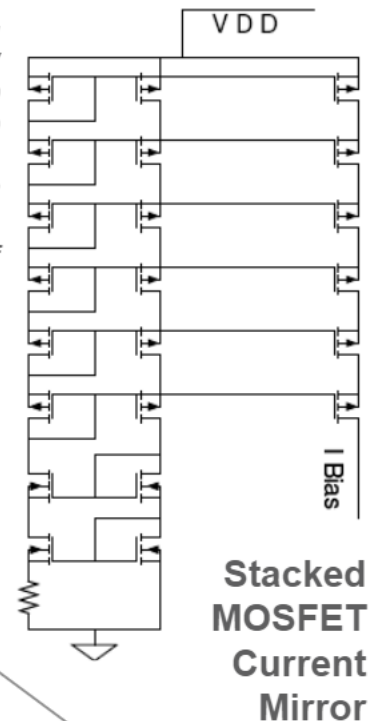
JP Colinge On-line SOI course at Stanford Univ. ~2004

STANFORD
UNIVERSITY

SOI / XDM10 process
> 350V D-S breakdown



http://www2.cambr.uidaho.edu/symposiums/12TH_NASA_VLSI_Proceedings/05%20-%20Analog%20and%20Mixed%20Signal/5.4%20-%20Penmetsa%20-%20High%20Voltage%20Operational%20Amplifiers%20in%20SOI%20.pdf



Emerging SOI application:

High-voltage switching

Challenge: Car batteries will increase to 48V, hybrid batteries output 200 – 300V and > 100A currents.

Solution: Thick SOI films (~1000 nm) allow high current switching. High breakdown-voltage transistors are separated by oxide, enabling even stacking and practically eliminating leakage currents.

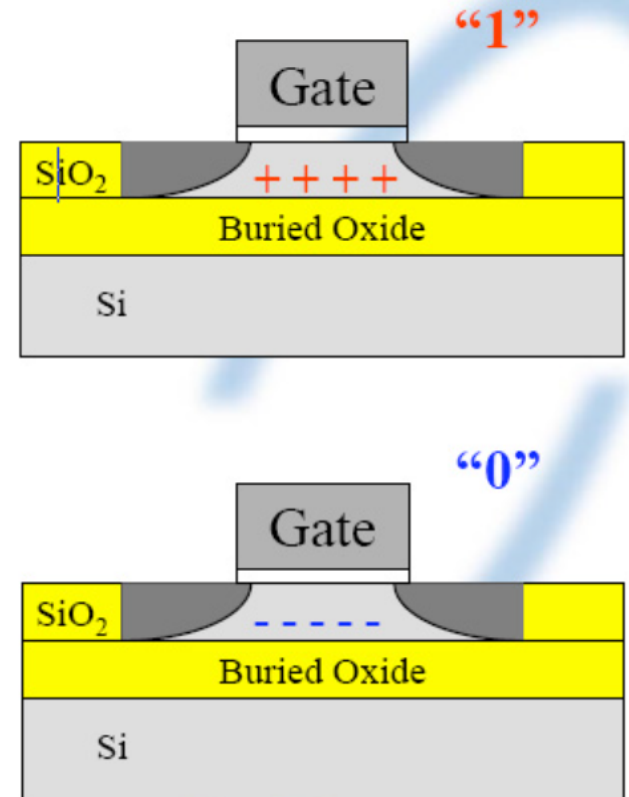


Emerging SOI application:

Zero-Capacitor RAM

Challenge: SOC's memory content is constantly increasing. High-density, low-cost and low-power memories are essential for many systems.

Solution: Z-RAMs ("Z" stands for Zero Transistor) utilize the free floating body effect of SOI transistors to store the state of the memory bit. No extra silicon area for a capacitor and no extra processing steps required.



Emerging SOI application:

Zero-Capacitor RAM

Challenge: SOC's memory content is constantly increasing. High-density, low-cost and low-power memories are essential for many systems.

Solution: A major semiconductor vendor applied the floating body effect to manufacture a 128 Mbits RAM and confirmed: High-density and easy to scale, because there is no extra capacitor and no extra process steps. Smaller area and lack of capacitor's load → higher speed.

Fig.2 128Mb FBRAM chip

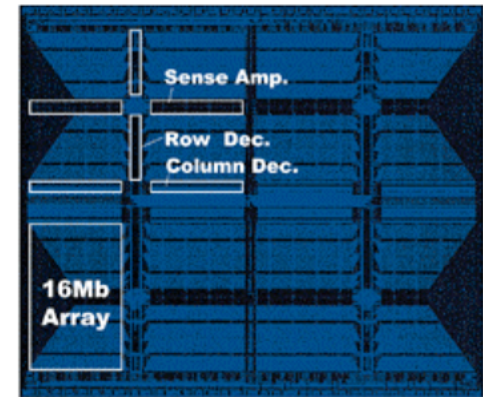
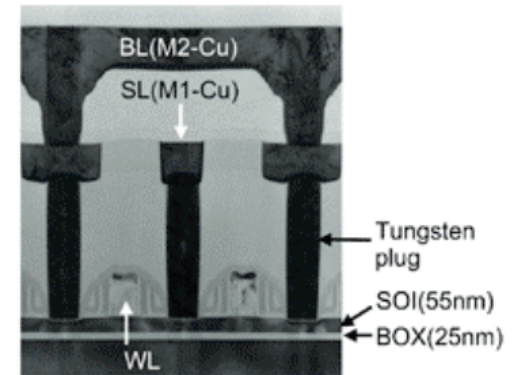


Fig.1 TEM cross-section along Bit-line



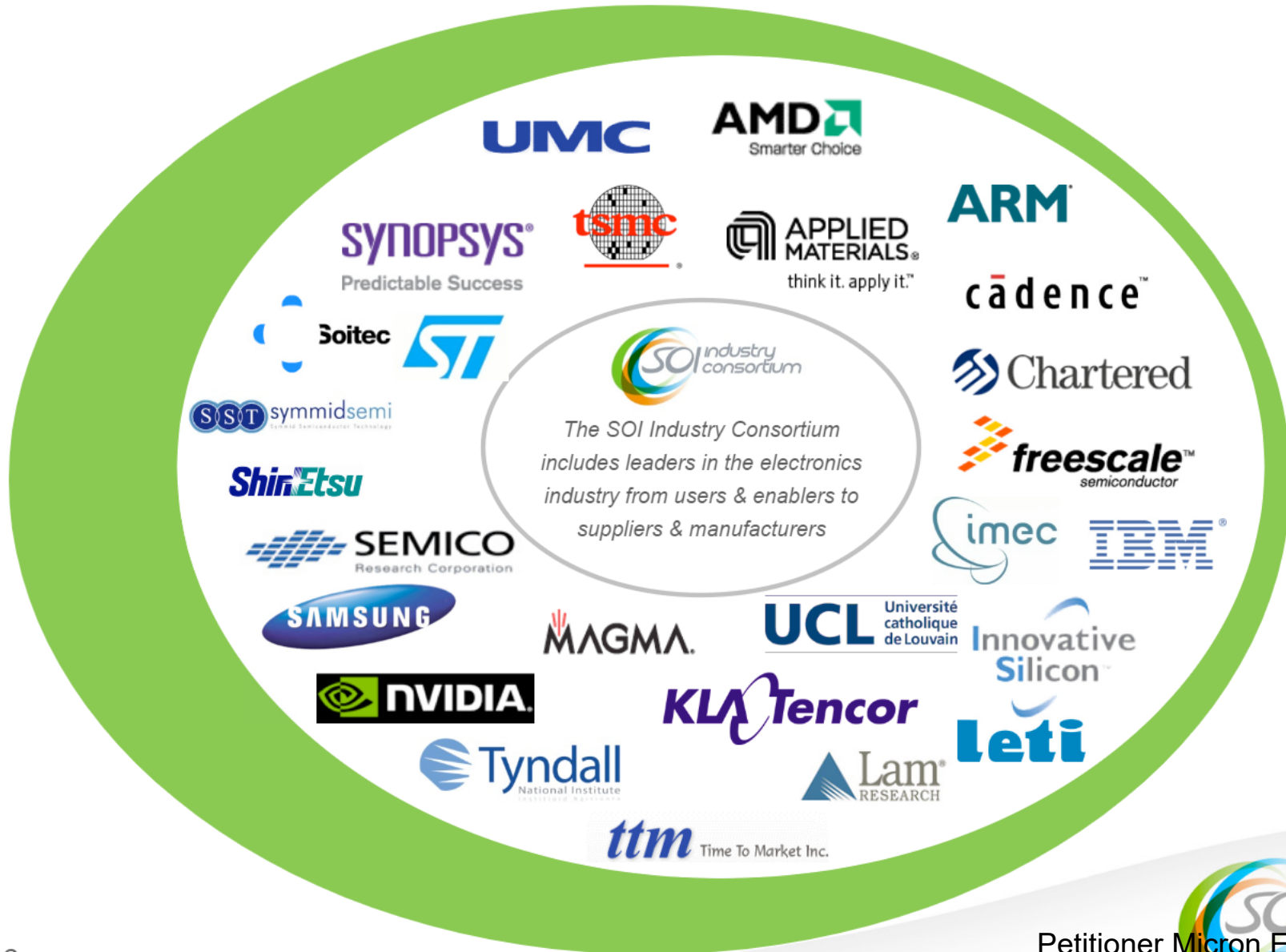
SOI industry Consortium

SOI Industry Consortium

The SOI Industry Consortium is a group of leading companies, academia and R&D institutes from the electronics industry with the mission of accelerating silicon-on insulator (SOI) innovation into broad markets by promoting the benefits of SOI technology and reducing the barriers to adoption.

More at: www.soiconsortium.org

26 members so far, focused on reducing power



Teams (volunteers from member companies)

Help closing the IP gap for SOI. Collaborate with IP partners to show functionality of most common IP on SOI

Help building an ecosystem (through group of project) around foundries

Technology Enablement team

Accelerate ecosystem collaboration to demonstrate SOI value and to enable adoption

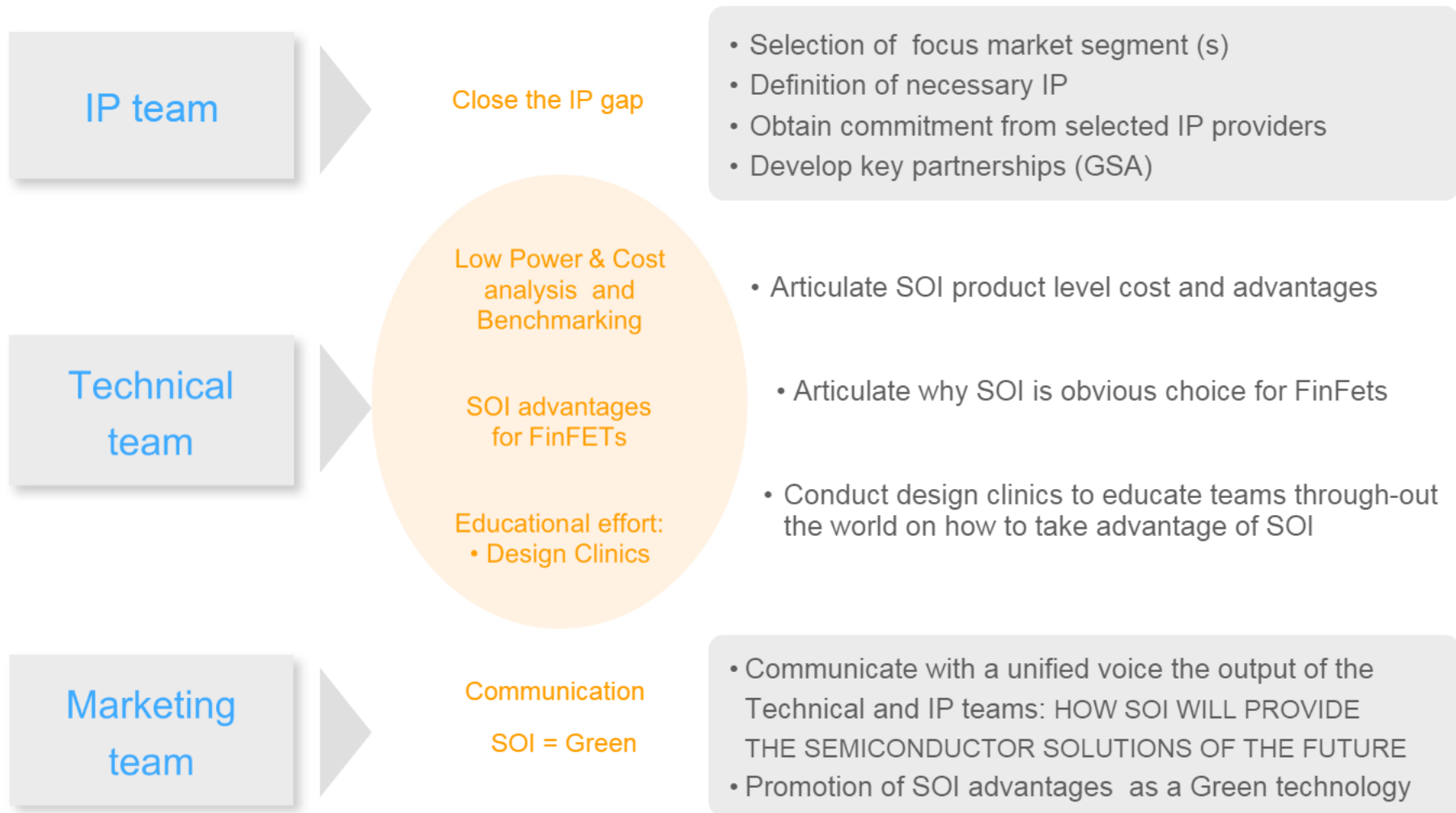
IP team

Consortium Goals

Marketing team

Communicate SOI benefits, technology innovation and momentum of SOI adoption through a unified voice

SOI Consortium major current activities



Discussion...

- **Are you considering SOI in the future?**
 - If yes, join the other leaders to enable the greatest choice of solutions and chance of success
- **Maximize your participation...what you put in is what you get**
 - Join as a full member to participate in all 3 committees
 - Consider running for the board as a full member
 - Vote for the board each year
- **Annual fees**
 - Full member: fee based
 - Technical member: fee based
 - Academic members – No fee (must be approved)
- **Review and sign agreement to support by-laws and rules**
 - Go to <http://www.soiconsortium.org/members/how-to-join.php>

*Please contact us at www.soiconsortium.org
or call Horacio Mendez +1 512 992 1809*

Thank you