The Memory Guy Blog

Jim Handy, Objective Analysis, on Semiconductor Memories

3D NAND: Benefits of Charge Traps over Floating Gates

A prior post in this series (3D NAND: Making a Vertical String) discussed the difficulties of successfully manufacturing a charge trap flash bit. Still, Spansion, and now other flash makers, have determined to take this route. Why is that?

In Spansion's case, a charge trap was a means of doubling the bit capacity of its products. It was an inexpensive alternative to standard MLC flash. To date this strategy has worked very well.

As mentioned in that earlier post, 3D NAND uses a charge trap because it's extremely difficult to create features, like a floating gate, sideways – lithography works from the top down. A charge trap, when used to replace a floating gate, doesn't need to be patterned, since the charge on one bit's charge trap will not leak through the insulating charge trap layer into an adjacent bit cell.

There are other benefits to using a charge trap though. Charge traps require a lower programming voltage than do floating gates. This, in turn, reduces the stress on the tunnel oxide. Since stress causes wear in flash memories, the lower programming voltage gives charge trap flash greater endurance than conventional floating gate.

A charge trap can improve bit reliability another way: Since the charge trap is an insulator the charge in the trap can't flow from one side of the trap to the other, the way it would in a floating gate. At the Flash Memory Summit Samsung likened this to using cheese instead of

water for the charge trap, thus this post's graphic. Although stress-induced leakage can drain the charge off a floating gate, the same phenomenon would only drain the charge off of a portion of a charge trap without disturbing the charge on the remainder of the trap. This makes it far less likely that a single point defect in the tunnel oxide layer would cause a bit to fail as it would in a conventional floating gate flash.

Reduced oxide stress, and lower sensitivity to single-point defects combine to significantly improve overall reliability. Samsung, in its V-NAND roll-out last August claimed that a charge trap provides twice to ten times the reliability of a sub-20nm planar floating gate NAND flash memory

Also, charge traps consume less energy during program and erase, so a 3D NAND that is based upon a charge trap is likely to be more energy-efficient than its floating gate counterpart. This translates to longer battery life. Samsung says its V-NAND provides a 40% improvement in power consumption over planar flash.

Charge traps are also faster to program than conventional floating gate flash. Samsung claimed that its 3D NAND charge trap supports twice the write performance of a sub-20nm planar floating gate NAND flash memory, although a subsequent release said that the sequential and random write speeds of a V-NAND-based SSD increase only 20%.

All-in-all Charge trapping is a good technology and it's something of a surprise that it hasn't found more widespread use n planar flash designs.

This post is a part of a series called ***What is 3D NAND? Why do we need it? How do they make it?*** that was published in weekly segments during the fourth quarter of 2013 on The Memory Guy blog. The different sections are listed below, with a hot link to each section.

- Why Do We Need 3D NAND?
- What Is a 3D NAND?
- Making a Vertical NAND String
- An Alternative Kind of Vertical 3D NAND String
- How Do You Access the Control Gates?
- Benefits of Charge Traps over Floating Gates
- How Do You Erase and Program 3D NAND?

- 3D NAND's Impact on the Equipment Market
- Who Will Make It and When?

Click on any of the above links to learn more about 3D NAND technology.

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