Three-Dimensional Shared Memory Fabricated Using Wafer Stacking Technology

K.W. Lee, T. Nakamura, T. Ono, Y. Yamada, T. Mizukusa, H. Hashimoto,
K.T. Park, H. Kurino and M. Koyanagi

Dept. of Machine Intelligence and Systems Engineering, Tohoku University
01 Aza-Aramaki, Aoba-ku, Sendai 980-8579, Japan
Phone:+81-22-217-6906; Fax:+81-22-217-6907; E-mail:sdlab@sd.mech.tohoku.ac.jp

Abstract

We proposed a new three-dimensional (3D) shared memory for a high performance parallel processor system. In order to realize such new 3D shared memory, we have developed a new 3D integration technology based on the wafer stacking method. We fabricated the 3D shared memory test chip with three memory layers using our 3D integration technology. It was demonstrated that the basic memory operation and the broadcast operation of 3D shared memory are successfully performed.

Introduction

The parallel processing by using a multi-processor system is the most promising way to achieve high-overall speed and efficient throughput in computation. It is well known that a shared memory is very useful to build the high-performance parallel processor system with simple configuration and architecture. However, the conventional system with a shared memory has the drawback that only limited number of processors can be connected to a shared memory due to the bus-bottleneck problem. This is because the processors are connected to the shared memory through a common bus in the conventional system as shown in Fig. 1 (a). Therefore, the date stored in the memory cannot be simultaneously shared among several processors due to bus-bottleneck. Such bus-bottleneck problem can be solved by using a multiport memory with many read/write ports which act as a real shared memory. However, it is not easy to realize a high-speed multiport memory with many read/write ports using the conventional technology. Then, we have proposed a new three-dimensional (3D) multiport memory with many read/write ports which acts as a real shared memory [1]. We can realize a high-performance parallel processor system by using such new multiport memory as shown in Fig. 1 (b). In order to achieve such 3D multiport memory that we call "3D shared memory", we have developed a new 3D integration technology based on wafer stacking method [2-5] and fabricated the 3D shared memory test chip which consists of three memory layers.

Configuration of 3D shared memory

A configuration of 3D shared memory with six read/write ports is shown in Fig. 2. This 3D shared memory consists of three memory layers each of which has two ports. Therefore, this memory has six memory mats. Each memory mat consists of a block of sense amplifiers and a memory cell array. Sense amplifiers can be also used as a built-in cache memory. We designed two kinds of 3D shared memories with DRAM cells and SRAM cells in memory cell array. The six memory mats are connected through broadcast buses in both horizontal and vertical directions. We can form many short buses with very high data transfer speed and data bandwidth for the broadcast in vertical direction by using 3D integration technology. Each processor is connected to the respective memory mat and hence six processors are connected to this shared memory. The data written to a certain memory mat by the corresponding processor are simultaneously transferred (broadcast) to other memory mats through high-speed horizontal and vertical buses. Therefore, the memory cells with an identical memory address in all memory mats have an identical data after broadcasting the data. This identical data can be read-out simultaneously and independently by several processors which are connected to the corresponding memory mats of 3D shared memory. Therefore, this 3D shared memory can act as a real shared memory without bus-bottleneck and conflict. Figure 3 shows the cross-sectional view of 3D shared memory.

Fabrication and evaluation of 3D shared memory

In order to evaluate the fundamental characteristics of 3D shared memory, we fabricated the 3D LSI test chip which includes a shared memory with three layer structure using our 3D integration technology. The fabrication sequence of 3D chip is illustrated in Fig.4. The device wafer with the buried interconnections are bonded to the other device wafer in face-to-face through the micro-bumps. In this case, the bottom wafer is used as a supporting wafer for 3D integration as well as a device wafer. After the temporary bonding using the micro-bumps, the liquid epoxy adhesive is injected into the gap between two wafers in a vacuum

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chamber to enhance the bondability of two wafers. The upper wafer is thinned from the backside using the mechanical grinding and CMP. Then, the micro-bumps are formed on the bottom of the buried interconnections at the backside. After that, another device wafer is glued to the thinned wafer stacked on the supporting wafer after a careful wafer alignment and thinned again from the backside. By repeating this sequence, the 3D stacked wafer can be obtained. To achieve such 3D chip, five key technologies such as formation of buried interconnection, micro-bumps, wafer thinning, wafer alignment and wafer bonding have been developed. It is required to form the deep Si trench in order to form the buried interconnection which acts as a vertical interconnection. The 2 μ m Si trench with depth of around 60 μ m was formed using Inductively Coupled Plasma (ICP) etching. Then, the Si trench was oxidized and filled with n+ poly-Si (0.4m Ω -cm) by LPCVD. The wafer is thinned to around 30 μ m using grinding and CMP techniques after bonded to another device wafer which acts as a mechanical supporting material. In-Au micro-bumps are formed on the back surface using the lift-off technique. Then, the thinned wafer are aligned to the bottom device wafer with the alignment tolerance $\pm$1 μ m using a newly developed 3D wafer aligner. This wafer aligner can also provide uniform force raising the temperature to guarantee a firm contact between the upper and lower micro-bumps. In-Au micro-bumps and epoxy adhesive layer are used to bond two wafers. The liquid epoxy adhesive is injected into the gap between two wafers in a vacuum chamber. The chip layout of 3D LSI test chip is shown in Fig. 5. The chip size is 12.6 mm$\times$8 mm. Figure 6 shows the SEM cross-section of 3D LSI test chip fabricated using 3D integration technology. It is clearly observed that three wafer layers are well aligned and uniformly bonded through the micro-bumps and insulating epoxy adhesive. The electrical characteristics of this 3D LSI test chip were evaluated. Figure 7 shows the I-V characteristics which were measured using the vertical interconnection chain pattern with 144-bumps and 144-buried interconnections. From this characteristics, we obtained the values of around 9 Ω for the resistance of buried interconnection and around 10 mΩ for the contact resistance of micro-bumps. The characteristics of NMOSFET with the gate length of 1.5 μ m fabricated on the bottom layer (3rd layer) were measured at the top layer (1st layer) through the vertical interconnections. Figure 8 shows the drain current – drain voltage (I_d-V_d) characteristics of NMOSFET before and after 3D wafer stacking. Excellent transistor characteristics are obtained in the 3D LSI test chip after wafer stacking. Leakage current was very low (below 10^{-9} A) even for V_d and V_g of 3.0V. Figure 9 shows subthreshold characteristics of NMOSFET before and after wafer stacking. The excellent subthreshold characteristics remain even after 3D wafer stacking without any degradation of device characteristics. High-frequency (1MHz) *C-V* characteristics of MOS capacitor with the size of 150 μ m$\times$150 μ m were evaluated before and after wafer stacking, as shown in Fig. 10. As is obvious in the figure, the *C-V* curve hardly changes even after 3D fabrication process. The characteristics of 3D inverter chain were evaluated. An NMOS inverter chain with 18 stages on the bottom layer (3rd layer) was measured at the top layer (1st layer) through the vertical interconnections. Figure 11 shows the input and output waveforms of NMOS inverter chain. You can clearly see the successful operation of the 3D inverter chain. Figure 12 shows a layout of 3D shared memory test chip. Each memory layer is electrically connected through the vertical interconnections which act as broadcast buses. Figure 13 shows photograph of shared memory test chip fabricated on the top layer (1st layer). Figure 14 shows the operation waveforms of 3D shared memory test chip. It is demonstrated in this figure that the data sent to the first layer sense amplifier are simultaneously transferred to the second layer and third layer sense amplifiers through the vertical interconnections. Thus, it was confirmed that the basic memory operation and the broadcast operation of 3D shared memory are successfully performed.

Conclusion

In order to realize a new three-dimensional (3D) shared memory, we have developed the 3D integration technology based on the wafer stacking method. Using this 3D integration technology, we fabricated the 3D test chip with three layers which includes 3D devices, 3D circuits and 3D shared memory test circuits. We obtained the excellent characteristics of 3D devices and 3D circuits. Furthermore, it was demonstrated that the basic memory operation and the broadcast operation of 3D shared memory are successfully performed.

Acknowledgement

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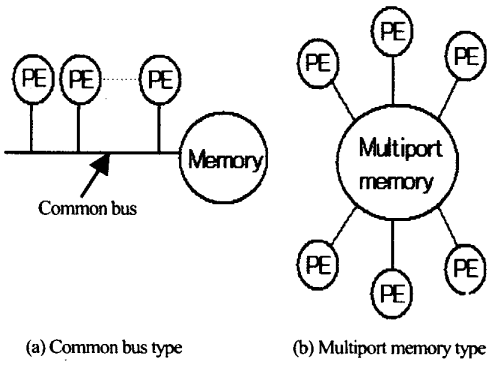
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(a) Common bus type (b) Multiport memory type

Fig. 1. Parallel processor system with shared memory.

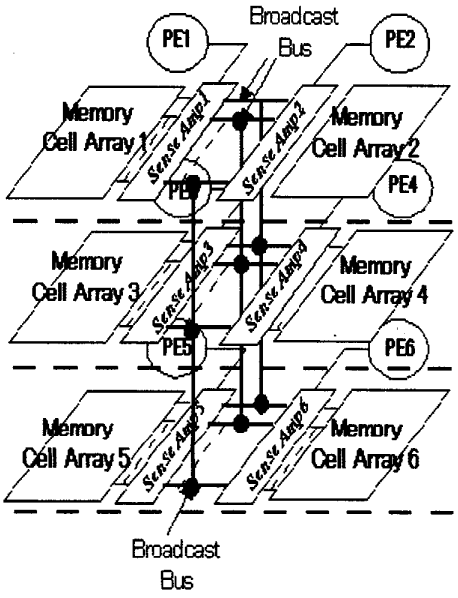


Fig.2. Configuration of 3D shared memory

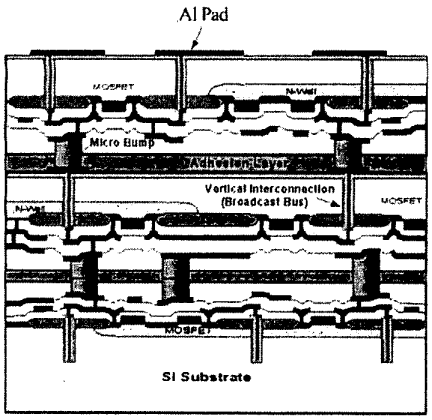


Fig. 3. Cross-sectional structure of 3D shared memory.

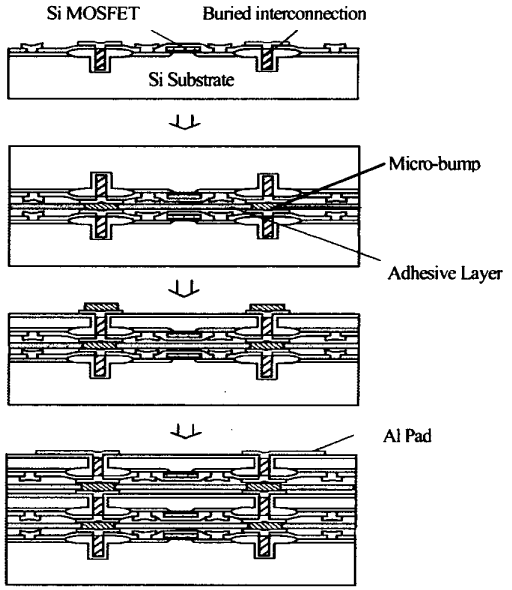


Fig. 4. Fabrication process sequence.

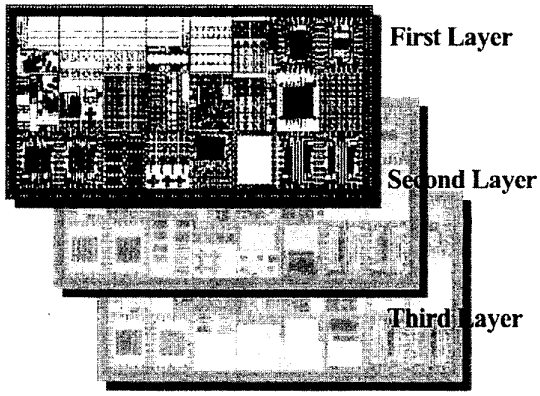


Fig.5.Chip layout of 3D LSI test chip with three layer structure

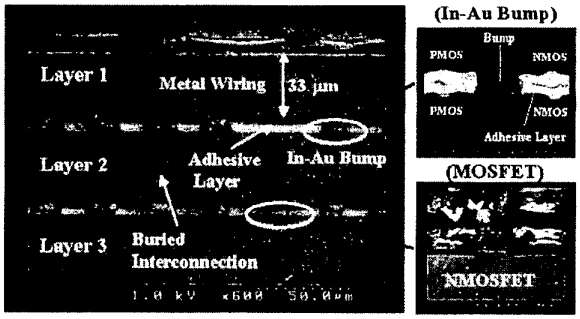


Fig. 6. SEM cross-sectional view of 3D LSI test chip.

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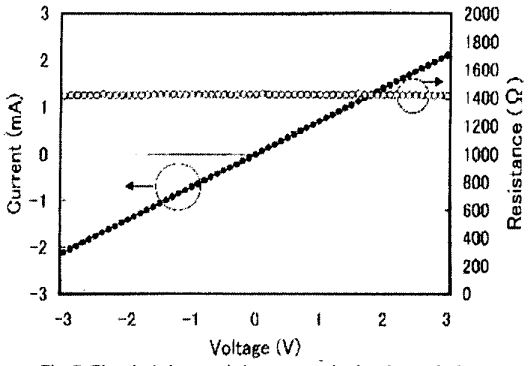


Fig. 7. Electrical characteristics measured using the vertical interconnection chain pattern on 3D LSI test chip.

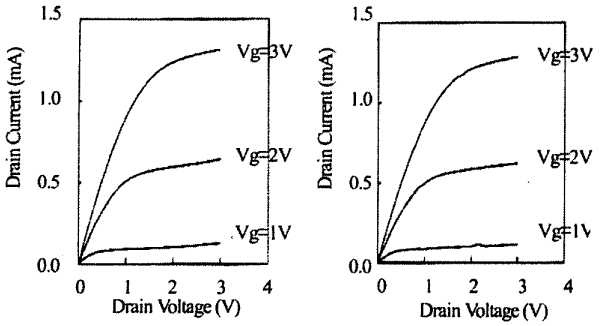


Fig. 8. I_d-V_d characteristics of NMOSFET (L_g = 1.5 μm) before and after stacking.

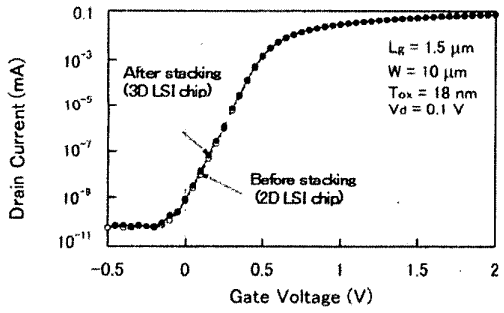


Fig. 9. Subthreshold characteristics of NMOSFET before and after stacking.

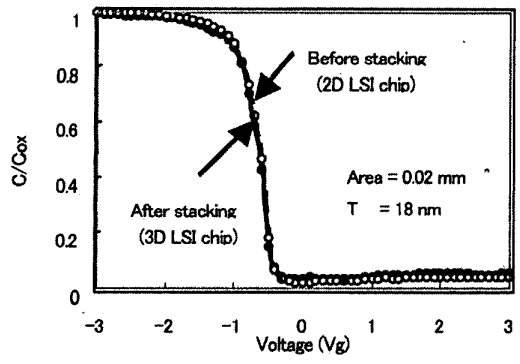


Fig. 10. High-frequency C-V curves of MOS capacitor before and after stacking.

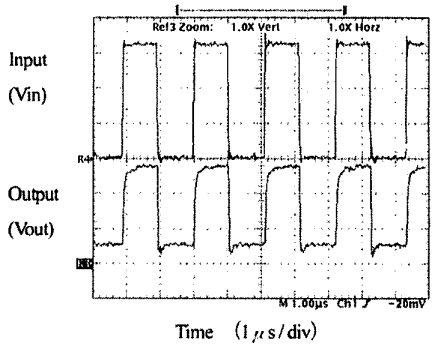


Fig. 11. Input and output waveforms of 3D NMOS inverter chain with 18 stages.

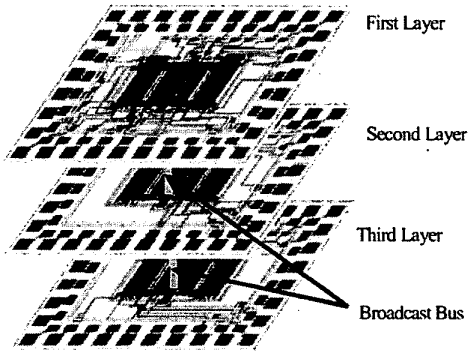


Fig. 12. Layout of 3D shared memory with three layer structure.

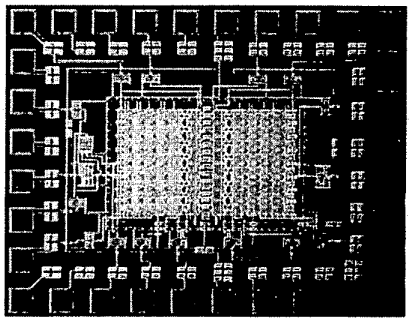


Fig. 13. Photograph of fabricated 3D shared memory (1st layer).

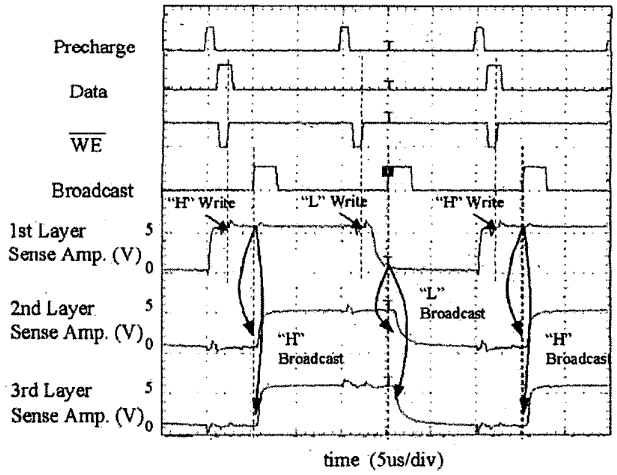


Fig. 14. Measured waveforms of the broadcast operation in 3D shared memory.

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