

REVIEW ARTICLE | APRIL 16 2003

Frontiers of silicon-on-insulator

G. K. Celler; Sorin Cristoloveanu



Journal of Applied Physics 93, 4955–4978 (2003)

<https://doi.org/10.1063/1.1558223>



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Frontiers of silicon-on-insulator

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(Received 18 September 2002; accepted 10 December 2002)

Silicon-on-insulator (SOI) wafers are precisely engineered multilayer semiconductor/dielectric structures that provide new functionality for advanced Si devices. After more than three decades of materials research and device studies, SOI wafers have entered into the mainstream of semiconductor electronics. SOI technology offers significant advantages in design, fabrication, and performance of many semiconductor circuits. It also improves prospects for extending Si devices into the nanometer region (<10 nm channel length). In this article, we discuss methods of forming SOI wafers, their physical properties, and the latest improvements in controlling the structure parameters. We also describe devices that take advantage of SOI, and consider their electrical characteristics. © 2003 American Institute of Physics. [DOI: 10.1063/1.1558223]

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I. INTRODUCTION

The conceptual breakthrough associated with the invention of integrated circuits was the realization by Noyce¹ and by Kilby² that multiple transistors could be made in the same piece of Si by isolating neighboring devices from each other with reverse biased *p-n* junctions. Monolithic integration, as we all know, has revolutionized electronics and changed the world around us. Concomitant with the rapid progress and evolution of microelectronics, it has become increasingly clear that junction isolation is not always the best approach to achieving monolithic integration. These junctions introduce extra capacitance and reduce density of transistors in the circuits. If the ambient temperature is high enough, leakage currents diminish the isolation between various circuit components. In the last 30 years, a growing body of research and some niche applications demonstrated that it is possible, and often advantageous, to build monolithic semiconductor circuits with dielectric, instead of junction, isolation. This is accomplished by utilizing silicon-on-insulator (SOI) wafers. Since approximately 1998, commercial applications of SOI have grown exponentially, and entered the mainstream of ultralarge scale integration (ULSI) electronic circuits.

SOI structures consist of a film of single crystalline Si separated by a layer of SiO₂ from the bulk substrate.^{3–5} The fact that the top Si layer must be monocrystalline, but separated by an amorphous insulating film from the single crystalline substrate, poses a major difficulty. There is no deposition method that would result in a single crystalline film grown without some kind of a template below it. There have been many attempts to utilize various localized templates and then extend epitaxial growth from these templates to other regions, but these approaches, although scientifically interesting, have not led to many practical solutions. One version of heteroepitaxial growth on a crystalline insulator, namely silicon on sapphire or SOS, became a commercial technology, but was found to be of limited utility. Several other interesting approaches have been studied, which significantly enlarged our body of knowledge about the microstructure and morphology of thin silicon films. Methods that were considered important at one time are listed in Table I, and an interested reader can obtain the details by following the references listed in it. There are also some books and conference proceedings that cover these topics.

Out of the broad range of pursuits, two technologies emerged as dominant industrial methods of SOI formation. They both rely on ion implantation but one also utilizes wafer bonding. Although ion implantation is essential to both approaches, the implanted species are different, and the goal of the implantation is also different. In the first method, known as the separation by implanted oxygen (SIMOX) process, an oxide layer is synthesized directly from oxygen ions that become buried under a superficial Si film. The second approach, known as the Smart Cut™ method, utilizes ions, most commonly hydrogen ion implantation as an atomic scalpel that cuts through the crystalline lattice and permits a clean and uniform transfer of a thin layer of Si to another substrate. In addition to the two implantation-based methods, other techniques are of interest. In one relatively recent de-

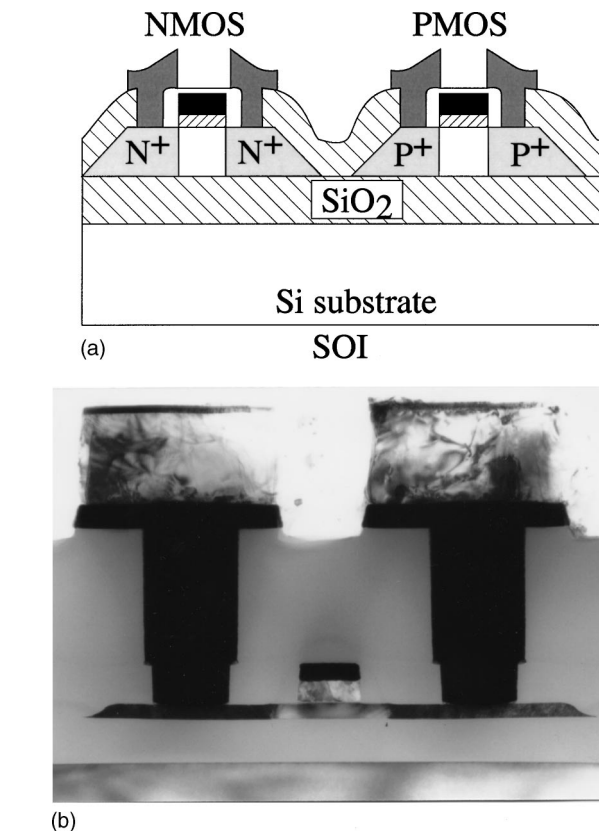


FIG. 1. (a) Schematic architecture and (b) TEM cross section of a SOI MOSFET.

velopment, an electrochemically formed porous Si layer is used instead of ion implantation to facilitate mechanical splitting of two wafers after bonding. Other SOI processes that offer unique advantages for specific device applications include epitaxial lateral overgrowth and zone melting recrystallization—these approaches may permit building multiple stacked layers of active devices, thus forming three-dimensional (3D) circuits.

In parallel with purely electronic applications, SOI wafers are becoming the material of choice for many kinds of micro-electro-mechanical systems (MEMS) and for micro-phonic chips. MEMS applications of SOI take advantage of mechanical properties of the monocrystalline films, which are superior to those of polycrystalline Si. Photonic applications rely on high refractive index contrast between Si and SiO₂, which permit photon confinement in small waveguides with sharp bends.

A. Motivation to develop SOI

A schematic configuration and a low magnification transmission electron microscopy (TEM) cross section of a MOS transistor built in SOI are shown in Figs. 1(a) and 1(b). This figure illustrates a number of points about the SOI device structures. The entire transistor body—the source, the drain, and the channel in between—is isolated from the Si substrate and from every other transistor by means of the buried oxide below, and by a combination of thermally grown and deposited oxide above and on the sides of the transistor. Metal interconnects link the source and drain to

TABLE I. Different methods of SOI formation.

Method	Description
DI—dielectric isolation ¹⁸	Oxide isolated “tubs” of monocrystalline Si supported by a polycrystalline “handle” wafer.
SOS—Si-on-sapphire ¹⁹	Si film epitaxially grown on sapphire substrates.
SOZ—Si-on-zirconia ²⁰	Si film epitaxially grown on ZrO ₂ substrates.
Recrystallization from the melt:	Rapid melting of polysilicon films deposited over a SiO ₂ layer grown on a Si wafer, followed by controlled crystallization in a strong temperature gradient:
(a) laser—seeded ²¹	(a) cw laser beam raster-scanned across the surface, with via holes that connect the polysilicon film with the single crystalline substrate.
(b) laser—unseeded ²²	(b) as above, but no seeding vias in the oxide.
(c) ZMR—zone melt recrystallization with a hot wire ²³	(c) a long and narrow molten zone is swept once across the entire wafer.
(d) LEGO—lateral epitaxial growth over oxide—stationary lamp heater ²⁴	(d) a thick Si film is melted simultaneously across the entire wafer. Gradients due to seeding vias control crystallization.
ELO—epitaxial lateral overgrowth ²⁵	Selective Si epitaxial deposition, starting from via holes in SiO ₂ and spreading laterally over the oxide.
SPE—solid phase epitaxy ²⁶	Oxidized Si wafers with via holes through the SiO ₂ are coated with amorphous Si, which is epitaxially crystallized.
FIPOS—full isolation with porous oxidized silicon ²⁷	Porous Si is formed locally under islands of crystalline Si, then it is oxidized to form isolation.
Heteroepitaxy of crystalline insulators, followed by single crystalline Si ²⁸	CaF ₂ , ZrO ₂ , spinel, and other crystalline insulators have been used.
SIMOX—separation by implantation of oxygen ²⁹	Buried oxide layer is synthesized <i>in situ</i> from implanted oxygen.
Wafer bonding and etch-back ³⁰	Two wafers are bonded with an oxide layer in between. One of the wafers is thinned by grinding and etching.
Smart-Cut™ process—layer transfer facilitated by ion implantation ³¹	One wafer is implanted, typically with H or noble gas ions. The Si layer above the implanted region is transferred to a “handle” wafer by wafer bonding and splitting along the implanted region.
ELTRAN process—layer transfer facilitated by porous silicon ³²	Epitaxial layer is grown on a porous Si region and transferred by bonding and splitting to a “handle” wafer.
SON—silicon-on-nothing ³³	Successive epitaxy of SiGe and Si films on a Si substrate is followed by removal of the sacrificial SiGe, which leaves lithography-defined small cavities. The cavity walls can be coated with SiO ₂ .

the outside, while the polysilicon gate, covered with tungsten silicide, is the third terminal with its own tungsten contact [not visible in Fig. 1(b)]. Large area *p-n* junctions, separating the source and drain from the substrate in a traditional bulk Si architecture, are replaced by dielectric isolation. The ensuing reduction of source and drain capacitance leads to faster transistor switching. Increased speed is an important advantage, but there are many other incentives for utilizing SOI substrates.

Historically, there have been three reasons for developing and using SOI. In the 1970s and 1980s, radiation hardness of SOI circuits was the main motivation for choosing these new substrates. Thin active Si films minimized the impact of ionizing radiation on device performance. The majority of charges generated, for example, by an alpha particle

impinging on a Si substrate would be stopped by the buried oxide, thus reducing the current surge in the active film.

Currently, performance enhancement motivates many integrated circuit companies to use SOI wafers. For the same supply voltage, digital logic circuits, such as microprocessors, run faster in SOI than in bulk Si. Alternatively, it is possible to reduce power consumption of SOI chips by lowering their operating voltage, while still keeping the clock rate, i.e., their performance, the same as in more power-hungry bulk circuits.

As we approach what is known as the “end of the roadmap,” SOI is needed to extend life of the traditional Si technology. Transistors with gate lengths of 25 nm or less do not perform well in bulk Si. The electric field in the transistor channel induced by the gate has to compete with the fields

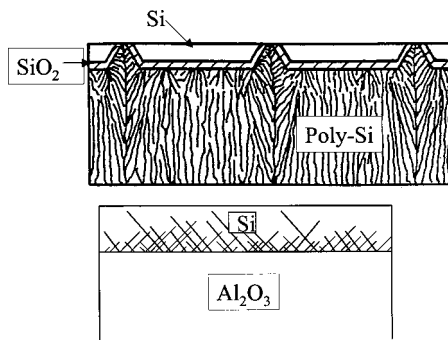


FIG. 2. Schematic representation of DI (dielectric isolation) and SOS (silicon on sapphire) structures.

from the source and drain regions. These “short channel effects” or SCE are reduced or eliminated by going to thin SOI structures. There is a close-to-unanimous agreement among experts in the field that ultrathin SOI is a key solution to the SCE.^{6,7} This is also reflected in the SOI section of the International Technology Roadmap for Semiconductors, also known as ITRS-2001.⁸

Advantages to building complementary metal-oxide semiconductor (CMOS) circuits in SOI are most frequently documented,⁹ but performance of BiCMOS, power and high voltage devices, high temperature circuits,¹⁰ and circuits exposed to ionizing radiation is also enhanced. In addition, SOI structures facilitate fabrication of MEMS and of optical waveguides.

B. Comments on bibliography

The SOI literature is very extensive, and it includes a few books and many review articles. In order not to duplicate the effort, the emphasis of this article is on the developments of the last few years. But it is also necessary to introduce the concepts, basic ideas, and major developments, and there we attempt to quote the original papers in order to acknowledge the scientists who laid the foundations for this scientific field and the technology that was built upon it. We also list a number of books, proceedings volumes, and special issues of journals that gather hundreds of papers that were important at one time, and some that possibly still are. Two conference proceedings series documented the progress in the SOI field from the earliest days.

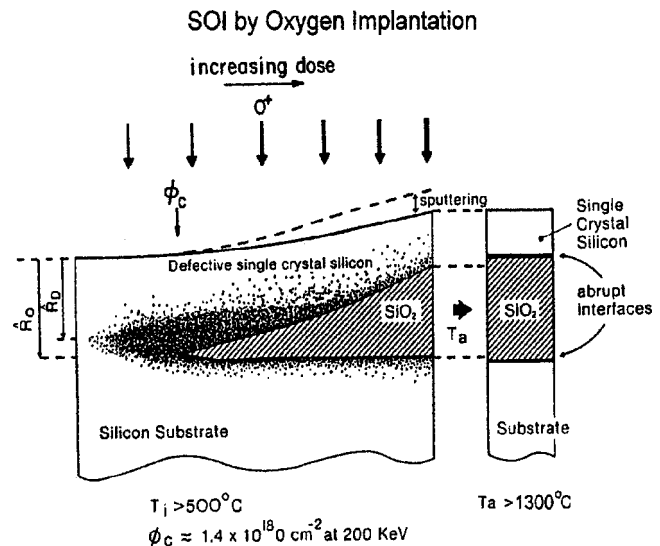


FIG. 3. Evolution of the SIMOX structure during oxygen implantation (after Hemment *et al.*, Ref. 36).

Material Research Society symposia started covering the field of laser annealing of semiconductors in 1978. SOI by controlled crystallization from the melt was a related subject and it was initially included in the same proceedings volumes, beginning in 1981.¹¹ In 1984, a separate symposia series on SOI was started that encompassed many other approaches to SOI formation beyond recrystallization from the melt.¹² Currently MRS Wafer Bonding symposia cover some aspects of material preparation for SOI applications.

The annual IEEE SOS (silicon-on-sapphire) Technology Workshop, first held in 1975, morphed in 1985 into SOS/SOI Technology Conference, and later into IEEE International SOI Conference. Although there are no full proceedings of these conferences, digests with two page extended abstracts of all presentations are available for all meetings since 1989. These short articles document the annual progress in both the material science and device physics of SOI.

The Electrochemical Society started SOI symposia series in the 1980s, on a biennial schedule.¹³ In parallel with the SOI symposium, the Wafer Bonding symposium has been held every two years for at least a decade.¹⁴

Over the years, many other conferences were at least partially dedicated to SOI, including Ion Implantation Tech-

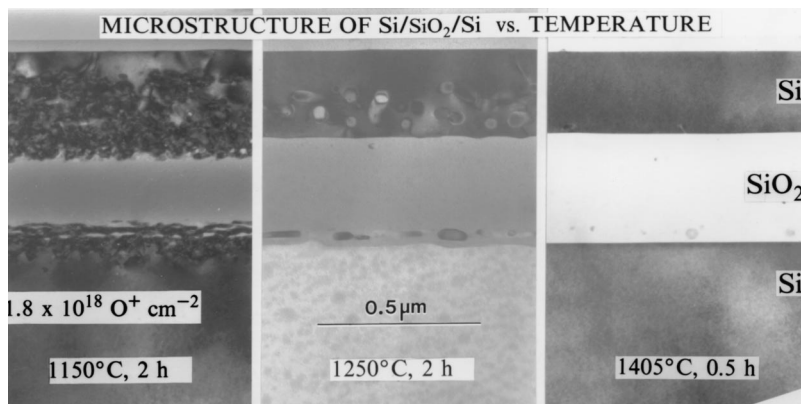


FIG. 4. The dependence of SIMOX microstructure on annealing temperature (from Marsh *et al.*, Ref. 41).

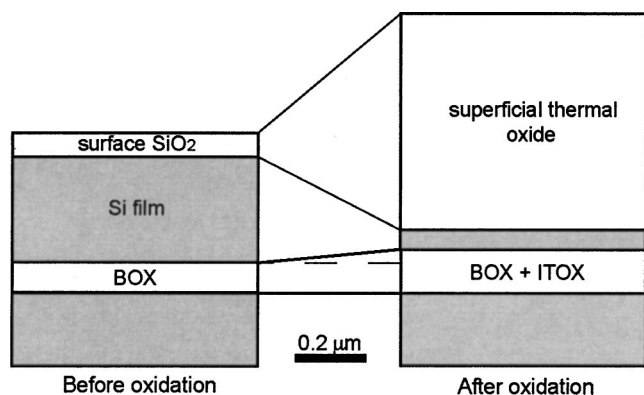


FIG. 5. Internal oxidation improves the stoichiometry of the BOX, tends to close Si pipes, and it slightly increases the overall thickness of the BOX, as shown in this drawing based on actual data of Nakashima *et al.* (Ref. 46).

nology conferences, meetings on 3D Integration, INFOS, European SOI Symposia, and most device related conferences, such as IEDM, SSDM, ESSDERC, and VLSI symposia. It is also worth mentioning some issues of journals that were dedicated to SOI technology, as they are a convenient source of referenced articles.^{15–17}

II. FABRICATION METHODS

A. Brief overview

Until 1979, when laser-annealing activities renewed interest in unconventional Si-based substrates, there were only two types of structures that we now include in the SOI category. Dielectric isolation (DI) wafers were used primarily for high voltage (up to 600 V) devices. These wafers consisted of islands of single crystalline Si that were embedded in polycrystalline substrates grown by high temperature chemical vapor deposition (CVD). Silicon-on-sapphire (SOS) wafers were obtained by heteroepitaxy of (100) Si on a (1102) face of Al_2O_3 , and these wafers were used when radiation hardness was a dominant design consideration. DI and SOS structures are shown schematically in Fig. 2.

During the 1980s, numerous novel approaches to forming SOI were explored. Many of them have not led yet to practical application, but they expanded the body of knowledge about crystal growth and defect formation and stimulated new device ideas. A few became commercial technologies with rapidly growing impact on the semiconductor industry. Different methods of SOI formation are listed in Table I.

The rest of this article is focused on two approaches to SOI that gained commercial significance, namely processes that include wafer bonding and splitting, and direct synthesis of buried oxide by oxygen implantation.

B. SIMOX process

1. Early developments and “standard dose” implants

The first pattern-independent SOI structures were produced by high dose implantation of oxygen. An early attempt to form SiO_2 by implanting oxygen into Si dates back to a 1966 publication by Watanabe and Tooi.³⁴ Implantation of about $1.5 \times 10^{18} \text{ cm}^{-2}$ oxygen at 60 keV appears to have

produced a surface layer of SiO_2 . But it was not until the late 1970s that Izumi and his associates at NTT demonstrated that a device-quality SOI structure could be formed. In 1976, experiments on buried oxide formation by ion implantation were initiated at NTT, using an Extrion 200-20a ion implanter.³⁵ In 1978, Izumi *et al.* demonstrated a 19-stage CMOS ring oscillator made in the new material, which they called SIMOX, an acronym for separation by implantation of oxygen.²⁹

The obstacles to making a high quality structure were at that time formidable. After all, these early attempts were based on the assumption that enough oxygen needed to be implanted to reach the stoichiometric concentration of oxygen (for forming SiO_2) already during implantation. For the 200 keV ion energy that was necessary to get a reasonable (at the time) thickness of about 200 nm of Si above the buried oxide (BOX in SOI community jargon), $\sim 2 \times 10^{18} \text{ ions cm}^{-2}$ were required, a dose greater than 100 times a typical implant dose utilized in device processing. High dose meant a high degree of crystalline lattice damage. In fact, at room temperature, the entire layer penetrated by the ions would have been completely amorphized. Since preservation of the single crystalline nature of the Si overlayer was essential, thermal annealing was needed concurrent with the implantation. At $T > 500^\circ\text{C}$, and typically close to 600°C , the dynamic annealing of damage during implantation preserves monocrystalline Si near the Si surface, where the ion energy is highest and thus there is less displacement damage. After implantation, very high temperature annealing is required to react oxygen ions with Si in order to form SiO_2 while annealing the damage in the Si layer above and in the Si substrate below the oxide. Evolution of the SIMOX structure during oxygen implantation is shown in Fig. 3.³⁶

Conventional furnaces with fused silica liners are limited to temperatures $< 1250^\circ\text{C}$. Wafers processed at such temperatures were used to make some devices and circuits, but the microstructure quality and device yields were poor. In these wafers, between the near-surface regions of reasonable quality single crystalline Si and the continuous buried oxide there was a broad transition region consisting of a high density of discrete oxide precipitates in a Si matrix. The oxygen concentration in this region could be as high as 20%. Annealing at very high temperatures was developed to improve the microstructure. The process of Ostwald ripening causes growth of precipitates with a radius above a critical value at the expense of smaller precipitates, which are dissolved. At temperatures above 1300°C the critical radius approaches infinity—only the planar buried oxide remains. In 1985, SIMOX structures annealed at 1300°C for several hours³⁷ or at 1405°C in a lamp furnace for 30 min^{38,39} demonstrated that atomically sharp and planar interfaces between Si and the buried oxide are feasible. The dependence of SIMOX microstructure on annealing temperature is illustrated in Fig. 4.^{40,41} Currently, all SIMOX wafers are annealed in furnaces with either polysilicon or SiC tubes at temperatures $\sim 1350^\circ\text{C}$.

Early SIMOX wafers typically had 10^{10} cm^{-2} threading dislocations intersecting the Si film. Formation of these defects depends on a complex interplay of many factors. Reduction to 10^6 cm^{-2} threading dislocations was achieved by

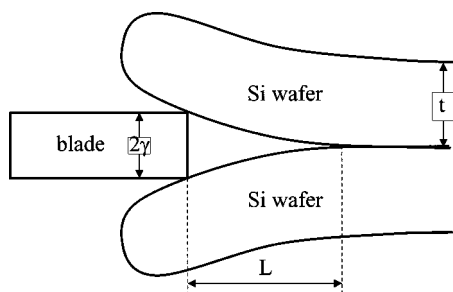


FIG. 6. The crack-opening method for measuring bond surface energy (from Maszara *et al.*, Ref. 60).

increasing implantation temperature to $\sim 600^\circ\text{C}$.⁴² A sequence of multiple partial-dose implants and anneals was shown to further reduce the defect density by an order of magnitude, but at the added cost of process complexity.⁴³

Further reductions in defect density relied on modifying the implanters. Because of the extremely high doses involved, sputtering of material from the walls of the implantation chamber and its deposition on the wafers was a significant source of contamination with metallic impurities until the systems were modified by coating the chamber interior with silicon. Elimination of particles from the wafers' surface was another essential requirement in order to prevent formation of Si "pipes" through the BOX.

2. Thinner buried oxide and internal oxidation

With SIMOX technology, the wafer cost is a strong function of the implant dose. Although initially it seemed that to obtain a continuous buried oxide a stoichiometric oxide must be formed in the as-implanted Si ($\sim 1.5 \times 10^{18} \text{ cm}^{-2}$ at 200 keV), eventually a high quality planar BOX was obtained at a much lower dose of $4 \times 10^{17} \text{ cm}^{-2}$ by modifying the implant and anneal conditions.⁴⁴ The buried oxide in this "low dose" SIMOX is about 100 nm thick, which is sufficient for the CMOS devices with the gate length $< 0.25 \mu\text{m}$. Low dose implantation has the additional benefit of reduced implantation damage and, as a direct consequence, fewer defects in the final annealed wafers. The feasibility of even thinner BOX films has been demonstrated with O^+ implantation of just $2 \times 10^{17} \text{ cm}^{-2}$ at 65 keV, followed by 4 h anneal at 1350°C , which resulted in a 56 nm thick oxide.⁴⁵

One concern with the thinner BOX is a higher probability of Si pipes that electrically short the Si film to the substrate. Internal oxidation or ITOX is a remedy for this potential problem. When an SOI wafer is oxidized at $\sim 1350^\circ\text{C}$, a small fraction of oxygen, which diffuses through the surface oxide, penetrates into the silicon and reacts with it at the Si/BOX interface.⁴⁶ This provides several benefits. Internal oxidation improves the stoichiometry of the BOX, tends to close Si pipes, and it slightly increases the overall thickness of the BOX, as shown in Fig. 5.

Another improvement of the SIMOX structure was obtained by adding a low dose (10^{15} cm^{-2}) room temperature implant after the "standard" hot implant.⁴⁷ This amorphizes the Si just above the peak of oxygen concentration R_p and helps in obtaining a continuous and flat BOX layer that has few if any Si inclusions.

3. Patterned buried oxide

There are some applications where it would be preferable to have buried oxide only in specific areas, with the rest of the wafer being conventional bulk Si. They include merging low voltage SOI circuits with high voltage bipolar transistors or combining digital logic circuits with dynamic random access memories (DRAM) on the same chip. The embedded DRAMs require deep capacitor trenches made in bulk Si. Therefore building the logic on SOI and the DRAM cells in bulk Si would optimize the performance of the entire system.

Since SIMOX SOI is formed by a blanket oxygen implantation, it would seem that just by masking some regions of the wafer, a patterned buried oxide could be obtained. Early experiments on masked oxygen implantation were performed in the mid-1980s.⁴⁸ This work involved the standard $2 \times 10^{18} \text{ cm}^{-2}$ implant dose and it demonstrated that the boundary between the SOI and bulk regions is extremely defective because of high stresses at the oxide edges. After low dose SIMOX was developed, the density of defects at the boundary was reduced considerably, but it was still high enough to potentially cause problems with device yield and reliability.

A novel solution to the patterned SIMOX problem, proposed by Cohen and Sadana, greatly reduces the number of defects in the transition region.⁴⁹ A blanket low-dose oxygen implantation is followed by a touch-up amorphizing O^+ implant at room temperature and then by patterned internal oxidation (ITOX process). This leads to a thicker buried oxide in regions exposed to oxidation (but also much thinner Si in the same areas). In the extreme case of a subthreshold O^+ implant dose of $1.5 \times 10^{17} \text{ cm}^{-2}$ the BOX is discontinuous under the oxidation mask. An alternative approach by Ogura⁵⁰ relies on oxygen precipitation in regions that were previously damaged by He^+ implantation.

It should be mentioned here that SOI wafers formed by methods other than oxygen implantation could be patterned later, during device processing, in order to combine SOI logic circuits with embedded DRAMs in the bulk.⁵¹ It is too early to predict whether patterning during SOI wafer production or at a later stage is more practical and cost effective.

C. Processes based on wafer bonding

1. Bonding mechanism

Fabrication of SOI structures by means of wafer bonding was first proposed by Frye *et al.*⁵² at Bell Labs and independently by J. Laski at IBM.⁵³ The first method required an electric field to press the wafers together in order to initiate the bonding process—or so it seemed at the time. Laski showed that bonding only required applying some slight mechanical force; therefore his method quickly became dominant. Direct wafer bonding or fusion bonding should not be confused with anodic bonding, which involves diffusion of sodium ions and for that reason is unacceptable in any electronic device application. Several excellent reviews on the science and technology of wafer bonding have been published,^{54–56} so here we only address the fundamentals and the latest developments. The exact nature of the forces

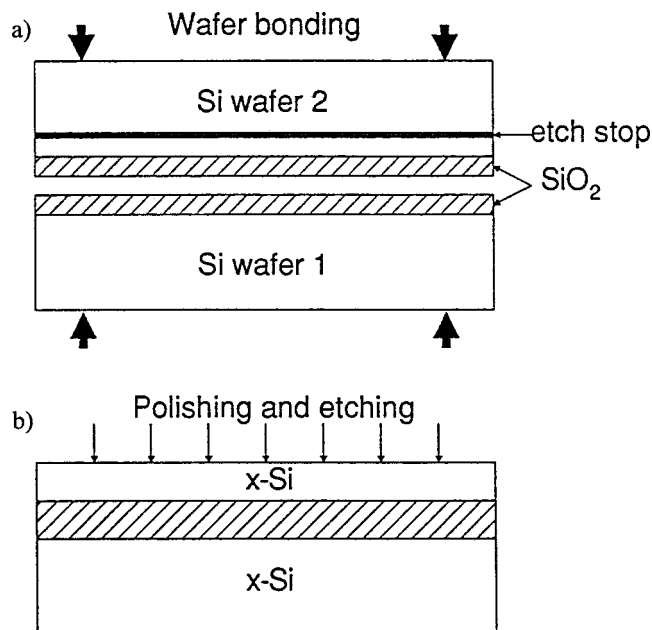


FIG. 7. A schematic representation of the bond-and-etchback SOI (BESOI) process.

that hold together two wafers that are placed in intimate contact depends on the surface preparation. Two very flat and very clean surfaces (for example in ultrahigh vacuum environment) are held together by Van der Waals forces, which depend on polarizability of atoms or molecules on the two surfaces placed very close (<1 nm) to each other. Spierings *et al.*⁵⁷ have estimated the surface bond energy of 0.0075 J/m² for two fused silica surfaces held together by Van der Waals interactions. In forming SOI wafers, it is much easier to take advantage of chemically assisted bonding through hydrogen bonds and water molecules. After wafer cleaning in an RCA solution⁵⁸ followed by a water rinse, the surfaces are coated with OH groups, which attract water molecules, in other words, the surfaces are hydrophilic. Two such surfaces are initially held together by hydrogen bridges and water molecules. Stengl⁵⁹ calculated the strength of “water” bonding of two oxidized Si surfaces at 0.104 J/m². The actual bond energy depends on surface preparation, bonding conditions, and the ambient in which the wafers are held after bonding.

Maszara *et al.* were the first group to systematically study the strength of the bonded interface between two wafers.⁶⁰ They utilized a double cantilever or crack opening method.⁶¹ In this approach, a wedge is pushed from one side between two bonded wafers and the length of the debonded area is correlated with the wedge thickness and elastic coefficients of the wafers that are being separated, as shown in Fig. 6. It was found that the bond energy immediately after bonding can vary across a large range, for example, between 40 and 70 mJ/m² for two oxidized Si wafers.⁵⁷ However, after 50 – 100 h in room ambient the bond energy saturated at a value of 130 ± 4 mJ/m². This is explained by hydrogen bridges gradually filling gaps between two somewhat imperfect surfaces.⁶² After the initial room temperature bonding, annealing at elevated temperatures fuses the wafers. Detailed

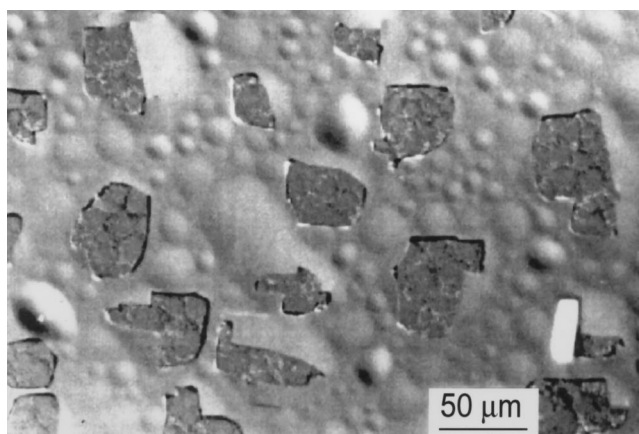
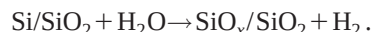


FIG. 8. SEM of a Si surface blistered by hydrogen implantation and annealing (from Aspar *et al.*, Ref. 69).

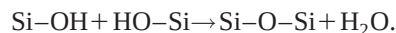
studies of the bond strength demonstrated that the bond energy peaks at about 1100 °C, with the bond energy of ~ 2 J/m².⁶⁰

Weldon *et al.*⁶³ studied the evolution of IR transmission spectra from the interface between two oxidized Si wafers as a function of thermal annealing. They looked in most detail at the case where both Si surfaces were coated just with a chemical (native) oxide that formed during a modified RCA. Spectra associated with Si–O, Si–H, and O–H stretching vibrations are clearly visible. Their analysis of these spectra led to the following conclusions.

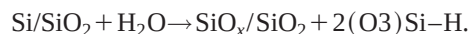
Immediately after the wafers are fused together at room temperature, there are 3 – 5 monolayers of water trapped between two oxide films, each ~ 4 Å thick. During a heating cycle that increases the temperature from 20 to 300 °C, about 75% of the water is lost (2×10^{15} O cm^{−2}) by diffusion through the thin oxides to the Si interfaces where an additional 4 Å of oxide (2×10^{15} O cm^{−2}) is formed. The oxidation reaction liberates molecular hydrogen:



When the bonded wafer pair is heated further, up to 800 °C, the remaining water diffuses away from the bond interface, so that interfacial hydroxyl groups on opposing surfaces can couple into bridging siloxane bonds that begin to fuse the two wafers together:



The water produced in the reaction above causes further oxidation of Si and the liberated H is trapped in the newly formed oxide



(O3)Si–H denotes Si in oxide with one O bond replaced by H.

After further heating of the samples up to 1100 °C a complete closure of the interface occurs by coupling of the remaining interface hydroxyl species and diffusion of the hydrogen into the Si bulk:

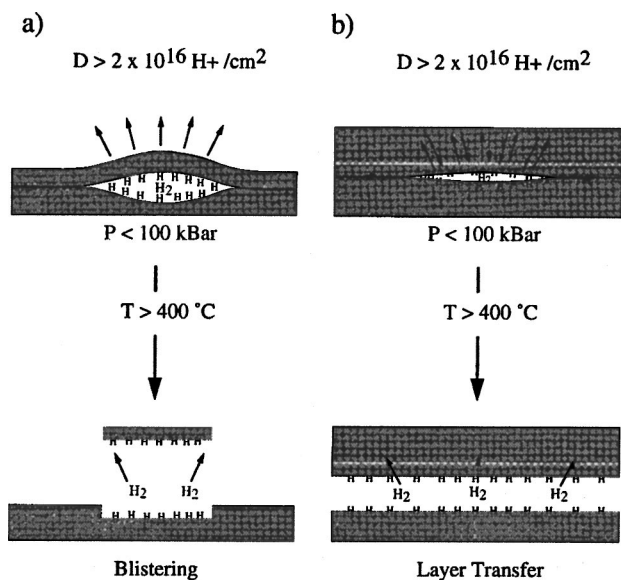


FIG. 9. A layer splitting in the presence of a stiffener is compared to blistering in the absence of such a layer (from Weldon *et al.*, Ref. 72).



The results for Si wafers with a thermal oxide instead of a chemical oxide are similar but about 40% less water is trapped initially between the wafers—possibly because the surface of the thermal oxide is smoother.

Several research groups observed that exposing either one or both surfaces to oxygen plasma before bonding them together can significantly enhance the room temperature bonding energy.^{64–66} More recent investigations show that approximately the same enhancement can be achieved with nitrogen or argon plasma. The mechanism of the enhancement appears to be related to the plasma-induced surface damage and not to surface-trapped charges, as some postulated. The damage increases surface porosity, which accelerates outdiffusion of water from the interface between two bonded wafers.

Bonding of two wafers is only the first stage in the process of making SOI structures. Afterwards one of the bonded

wafers must be transformed into a thin film of uniform thickness, low stress, and excellent crystallinity. The thinner the required film, the more difficult is this task. Many methods of forming SOI based on wafer bonding have been developed over the years. What differentiates them is how one of the wafers in the bonded couple is converted into a film. The important methods to accomplish this transformation are described in the following sections.

2. Bonding and Etchback: BESOI

The brute force approach is to mechanically grind, lap, and polish one of the wafers until only a desired film thickness remains. This is acceptable when a film of 10–100 μm is needed, but film uniformity deteriorates as the thickness is decreased further. An alternative is a bond-and-etchback SOI (BESOI) process (see Fig. 7), in which an etch stop is introduced in advance, before wafer bonding, typically by implanting a high dose of boron to produce a buried layer. Epitaxial layer growth on top of a boron doped surface layer is another alternative. Germanium or a combination of Ge and B can be used too. Ge atoms are larger than those of Si and compensate for B atoms that are much smaller, thus preventing strain induced slip in the lattice.

After wafer bonding, a combination of mechanical wafer thinning followed by a selective etch, which stops at a B- or Ge-rich region, and finally removal of this doped region, provide better uniformity than mechanical thinning alone. However, all these methods require two wafers to make one SOI wafer. In the BESOI approach there is an additional processing cost and some contamination of the final film with the etch-stop dopant.

3. Hydrogen implantation: Smart Cut™ process

a. Discovery of controlled exfoliation. In 1991 M. Bruel of LETI filed a patent application on a method of preparing thin silicon films that could be used to form SOI wafers. As applied to the fabrication of SOI, the method consisted of wafer bonding followed by splitting of a thin layer from one of the wafers.⁶⁷ Bruel's method utilizes various gas ions—most commonly, hydrogen—as an atomic scalpel that cuts through Si wafers. Hydrogen ions, when implanted to a dose of $>5 \times 10^{16} \text{ cm}^{-2}$, produce fine microcavities in the Si lat-

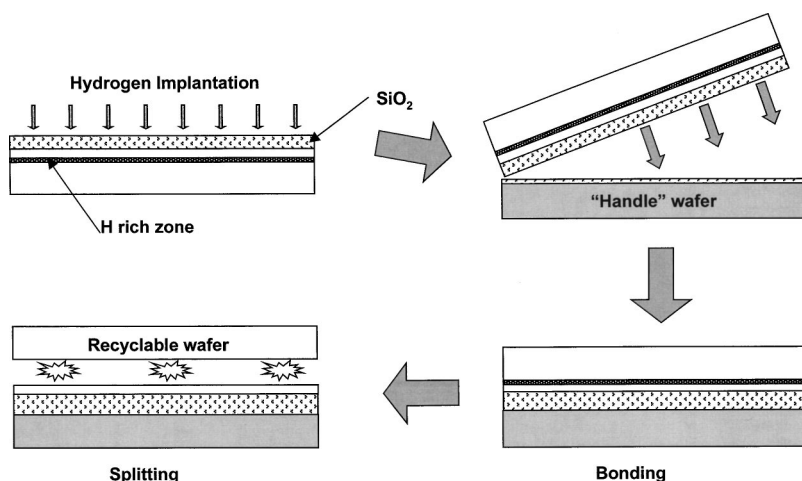


FIG. 10. Sequence of steps required to make SOI wafers by a preferred embodiment of the SmartCut™ process, using hydrogen as the implanted ions.

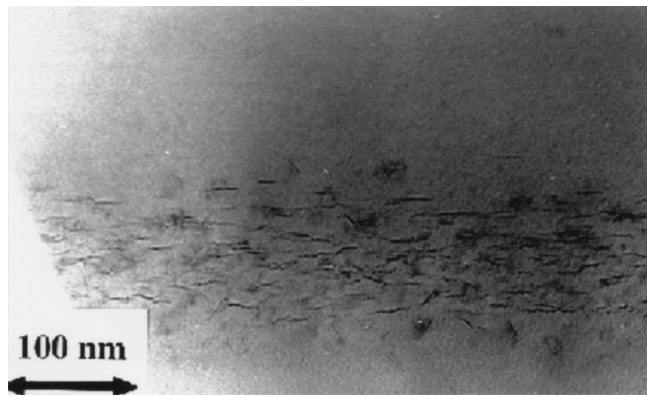


FIG. 11. XTEM of microcavities or platelets that formed near the implantation depth R_p . (from Aspar *et al.*, Ref. 69).

tice. Some hydrogen ions bond to the dangling Si bonds in the microcavities, while other fill these voids. If such an ion implanted wafer is heated up to 400–500 °C, more hydrogen segregates into the voids in the form of molecular hydrogen, H_2 , the pressure builds up to a point of fracture, and the surface of Si becomes pockmarked with blisters, as shown in Fig. 8. This is clearly an undesirable effect of ion implantation. For an implant dose exceeding approximately 10^{17} cm^{-2} , blistering may occur even without the heat treatment. Blistering phenomena caused by surface bombardment with hydrogen or inert gases have been seen in the past,⁶⁸ and all efforts were centered on preventing them. The brilliance of Bruel’s invention was to realize that the previously deleterious effect could be harnessed to accomplish a weakened plane or zone that makes it possible to attain a controlled cut through the crystalline lattice. The key to the new method was to introduce a stiffener—a thick and very stiff

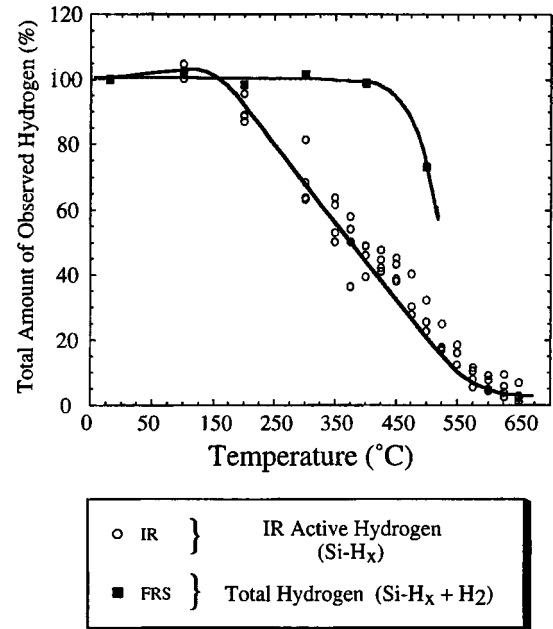


FIG. 13. The total amount of hydrogen, as measured by forward recoil spectroscopy (FRS), is compared to infrared-active hydrogen (from Weldon *et al.*, Ref. 72).

layer that prevents blistering and redirects the pressure that builds up in microcavities in a lateral direction, as shown schematically in Fig. 9. Heating of the wafer can split this weakened plane or zone or it can be cleaved by application of mechanical or other stress. In the Smart Cut™ process for making SOI wafers, the stiffener is a handle wafer.
b. Process description. The commercial version of the process for SOI formation by wafer bonding and ion implantation induced weakening or splitting is known as the Smart

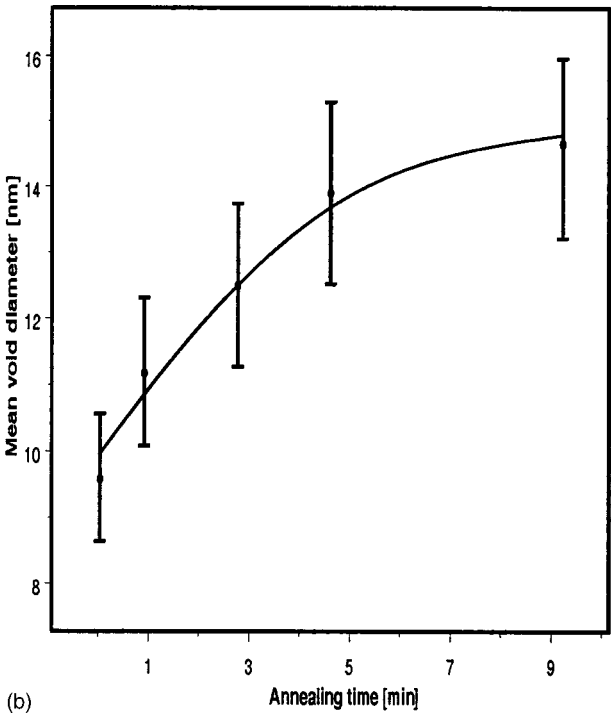
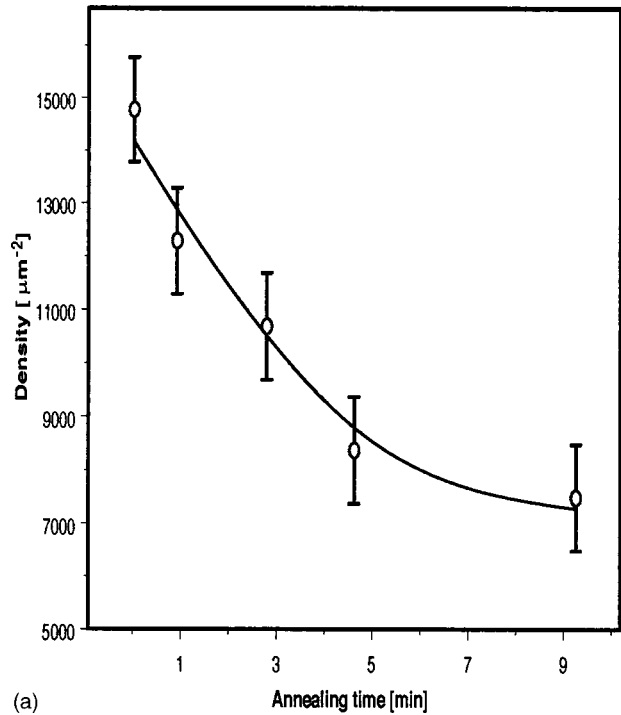


FIG. 12. The time evolution of the (100) platelet, (a) density and (b) size, are shown (after Aspar *et al.*, Ref. 69).

Cut™ process. The sequence of steps required to make SOI wafers by the commercial Smart Cut™ process using hydrogen as the implanted ions is shown in Fig. 10. A “seed” wafer, from which a layer of Si will be removed, is oxidized to a desired thickness. This oxide will become the buried oxide or BOX after bonding. The next step is hydrogen implantation through the oxide and into Si with a dose that is typically $>5 \times 10^{16} \text{ cm}^{-2}$. After implantation the seed wafer and the handle wafer are carefully cleaned in order to eliminate any particle and surface contaminants and to make both surfaces hydrophilic. Wafer pairs are aligned and contacted so that the fusion wave can propagate across the entire interface. A batch of bonded wafer pairs is loaded into a furnace and heated to a temperature of 400–600 °C, at which point the wafers split along the hydrogen implanted plane. The as-split wafer surface has a mean roughness of a few nanometers. A light touch-polish brings the same surface roughness as in standard bulk Si wafer, i.e., $R_a < 1 \text{ Å}$ across $1 \times 1 \mu\text{m}$ square. The seed wafer is reclaimed and, if necessary, repolished so that it can be used again.

There are several important practical aspects to the method of controlled transfer of a layer of Si, the thickness of which is defined by ion implantation energy, to a handle wafer. This approach makes it possible to reuse the seed wafer several times, thus reducing the final cost of the SOI wafer. It is the premium seed wafer that defines the quality of the SOI film, whereas the handle wafer only serves as a mechanical support and can have lower quality. Defining film thickness by implantation energy leads to a much better thickness control than is possible with either mechanical or chemical thinning. For that reason BESOI techniques are typically limited to films thicker than $5 \mu\text{m}$, where the absolute thickness control is easier. The thickness of the silicon film and/or buried oxide can be adjusted in the Smart Cut™ process by tuning the implant energy and oxidation time in a wide range. The thickness of the silicon in current applications typically runs from about 5 nm to $1.5 \mu\text{m}$. The thickness of the silicon dioxide in current applications runs from about 5 nm to $5 \mu\text{m}$. These wafers are thus adaptable to most device architectures, from ultrathin CMOS to thick-film power transistors and sensors. It is also worth noting that only conventional equipment is needed for mass production of 8 and 12 in. wafers.

c. Hydrogen splitting/separation mechanism. When hydrogen is used as the implanted ions, high dose hydrogen implantation into Si produces voids that tend to trap some hydrogen. For implantation doses $<2 \times 10^{16} \text{ cm}^{-2}$ at implant energies on the order of 60 keV, the void concentration in a standard silicon wafer is often insufficient to trap H for extended times at elevated temperatures. Under these conditions, during annealing the voids gradually dissolve and hydrogen diffuses away. For H implant doses $>2 \times 10^{16} \text{ cm}^{-2}$, the void density is high enough so that some of them survive and grow through the thermal cycle at the expense of smaller ones that are dissolved. This is a typical case of coarsening of the structure by means of Ostwald ripening.

Hydrogen plays many roles in this process. First, hydrogen implantation produces damage that is concentrated near

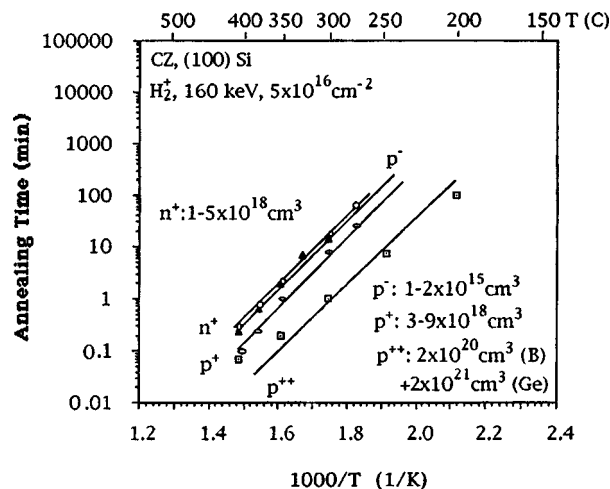


FIG. 14. The effect of boron concentration in Si on layer splitting (from Tong *et al.*, Ref. 78).

the mean projected range of the ions, R_p . The damage zone includes various defects, among them a significant density of voids, platelets, or microcavities.^{69,70} Second, after implantation but before any heat treatments, a large fraction of hydrogen is chemically bound to the dangling Si bonds at the internal surfaces of the defects, and it passivates these internal surfaces. This passivation effect prevents healing of the microcracks during the early phase of thermal annealing. In addition to H atoms that are tied to Si, some molecular hydrogen fills the microcracks and voids. The process evolves in the following way. Hydrogen implantation into Si produces some damage that is characteristic of light ions. In addition, high concentrations of microcavities or platelets form near the implantation depth R_p . These platelets, shown in Fig. 11, also sometimes called “hydrogen related cavities” or HRCs, are shaped like disks, with about 1 nm height and several nm in diameter.⁷¹

In (100) wafers, most of the platelets lie on the (100) planes parallel to the surface, and to a lesser extent on the (111) planes. The platelets can be observed by TEM before any heat treatment, but their diameter grows during annealing, while the density goes down and the total volume stays approximately constant. The time evolution of the (100) platelet size and density is shown in Fig. 12.

Hydrogen in the platelets exists in at least two forms. Some is chemically bound to the internal Si surfaces, the rest forms molecular hydrogen gas. Evolution of hydrogen from the first form to the second has been studied by Weldon *et al.*⁷² In Fig. 13, the total amount of hydrogen, as measured by forward recoil spectroscopy (FRS), is compared to infrared-active hydrogen. IR-active hydrogen, i.e., hydrogen that is bound to Si, starts decreasing at about 150 °C, while the total concentration remains constant until $>400 \text{ °C}$ is reached. This is interpreted as an increase in H_2 being released into the platelets, which leads to a pressure buildup.

The pressure of molecular hydrogen in the platelets is believed to cause these microcavities to propagate by growing microcracks. The microcracks provide a weakened plane that can be cleaved by the application of a mechanical stress, or they can be further propagated by heating to the point

where they will split the layer from the wafer. Freund analyzed propagation of microcracks from the initial disk-shaped platelets, utilizing simple mechanistic concepts of gas pressure opening the small cavities and microcracks that elongate if it is energetically favorable.⁷³ The pressure in the cavity is governed by the Sieverts' rule, which says that the concentration of H ions dissolved in the crystal is proportional to the square root of the hydrogen gas pressure on the boundary of the crystal at thermodynamic equilibrium. Since the implanted hydrogen concentration vastly exceeds the equilibrium solubility of H in crystalline Si, the pressure of gas trapped in the microcavities should be very high. Freund estimated that a $2.8 \times 10^{16} \text{ cm}^{-2}$ H dose, heated to 700 K, is the minimum required to cause a split, when any chemical or other lowering of the cohesive strength of Si and chemical binding of H to defects, are ignored. Grisolia *et al.*⁷¹ calculated pressure on the order of 10 GPa in a typical platelet at room temperature.

Recently, Höchbauer *et al.*⁷⁴ made a detailed study of the exact location of the cut induced by hydrogen implantation. They utilized secondary-ion-mass spectroscopy (SIMS), scanning electron microscopy, cross-section TEM, Rutherford backscattering spectroscopy (RBS), and elastic recoil detection to determine the relationship between the depth R_p of the maximum concentration of implanted hydrogen, the location of maximum implantation damage, and the location of the eventual split. Their conclusion is that for their specific implantation conditions the split occurs at the depth of maximum damage, which is slightly less than the R_p .

4. Variations on wafer bonding and hydrogen-related splitting

Brueel's invention set a new direction of research. After the concept of wafer splitting was disseminated within the scientific community, many other related variations were generated along the same vein, providing a weakened zone or plane that can be split or fractured upon application of a shearing stress or by the application of energy such as by heating to accomplish a layer transfer.

a. Hydrogen and helium. Separation of a thin film of the bulk crystal can be achieved with other implanted species, in particular with helium and other noble gases. However, hydrogen, either alone, or in tandem with another species, is preferred because of its reactivity with the internal surfaces of a semiconductor. For example, a study of coimplantation of H^+ and He^+ has demonstrated that each plays a somewhat different role. Hydrogen interacts chemically with the implantation damage to produce platelet-shaped microvoids. He^+ implanted after the hydrogen fills the voids and provides most of the pressure that causes separation of a Si film from the bulk substrate. Agarwal *et al.*⁷⁵ have shown that film separation could be achieved with doses as low as $7.5 \times 10^{15} \text{ cm}^{-2} \text{ H}^+$ and $10^{16} \text{ cm}^{-2} \text{ He}^+$. In contrast, under the same implantation and annealing conditions, He^+ alone requires a significantly higher dose of $2 \times 10^{17} \text{ cm}^{-2}$ and H^+ alone requires $6 \times 10^{16} \text{ cm}^{-2}$. As expected from the model, reversing the sequence of implants does not provide the same benefits as the "hydrogen first" case.

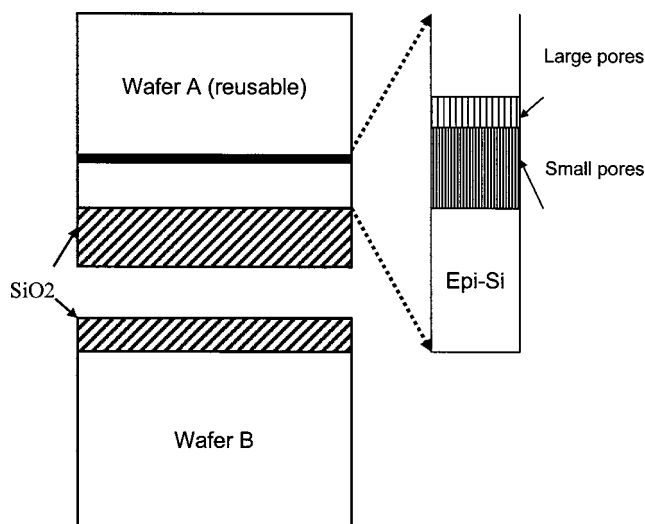


FIG. 15. A schematic of the ELTRAN process.

The microstructures observed after He^+ implantation is very different from that obtained after hydrogen implantation. A cross-sectional TEM of a H^+ implanted sample shows a band of platelets 3–10 nm in length, positioned along (100) and (111) planes. The He -implanted sample shows many large defects, greater than 300 nm. This is attributed to the lack of chemical bonding of He in Si, which results in more diffusion of He and its segregation into much larger defects. Even though He can be used alone to split layers in a similar manner to that of hydrogen, the combination of H followed by He is more effective.

b. Hydrogen and boron. The reaction of hydrogen with Si is influenced by the presence of Si dopants. Boron is particularly effective, since in addition to producing a large number of defects per implanted B ion, B atoms themselves may trap a cluster of hydrogen atoms. It is known that hydrogen in p -Si diffuses as H^+ ions, and the internal electric fields that are generated by p^+ layers attract these positive ions. However, at 200 °C, H^+ is attracted to p^+ layers even after all acceptors have been matched with H^+ , as shown by Marwick *et al.*⁷⁶ In another study, Borenstein *et al.* showed that as many as 8–12 hydrogen atoms are trapped by each boron atom.⁷⁷ Tong *et al.* have taken advantage of this affinity of hydrogen for boron to reduce the heating times and temperatures required for layer splitting and separation, as shown in Fig. 14.⁷⁸ This is particularly useful when a layer transfer of Si to a dissimilar material with a very different thermal expansion coefficient is attempted. The advantage of reduced process temperature is, however, counterbalanced by the risk of an excessive p -type doping of the film that is being transferred.

c. Hydrogen at heteroepitaxial interface. Stresses produced by ion implantation can be accompanied by additional stresses induced by heteroepitaxy. Application of the Brueel process to hydrogen implanted at or near the Si/SiGe interface is effective in splitting the wafers along this interface.⁷⁹

d. Strained Si on insulator (SSOI). Strained Si films on relaxed $\text{Si}_{1-x}\text{Ge}_x$ can provide enhanced carrier mobility in metal–oxide–semiconductor field effect transistors

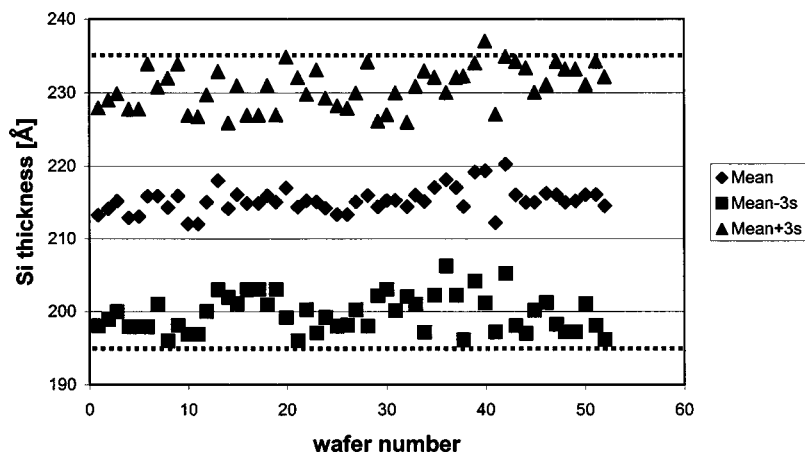


FIG. 16. Typical Si thickness data for a 300 mm wafer produced by the Smart Cut™ process.

(MOSFETs).⁸⁰ In the bulk Si version of strained Si, a thick $\text{Si}_{1-x}\text{Ge}_x$ layer is grown epitaxially on a Si wafer, with Ge concentration gradually increasing to about $x = 0.3$. A relaxed layer of $\text{Si}_{1-x}\text{Ge}_x$ of uniform Ge concentration is grown next, followed by a thin strained Si film that matches the lattice of $\text{Si}_{1-x}\text{Ge}_x$.

In one SOI implementation, the relaxed SiGe film of uniform composition is split from the substrate on which it was grown and transferred to an oxidized handle wafer. Then the strained Si film is grown, thus achieving a SOI-like structure that combines the advantages of higher mobility with those typical of SOI.⁸¹ The layer transfer process also eliminates the highly defective SiGe layer of graded concentration.

In another SOI version, SiGe has only a temporary role and is totally absent from the final structure. The entire stack of graded SiGe, followed by relaxed SiGe of uniform composition and a strained Si layer are grown first, and then bonded to an oxidized Si handle wafer. After splitting off of the seed wafer, the remaining SiGe is etched away in a selective etchant, leaving only the strained Si film on BOX.⁸²

Although the SIMOX process can also be used to make strained Si on relaxed SiGe on insulator, high temperature annealing that is integral to the SIMOX process typically limits Ge concentration to $<10\%$.⁸³ In the SIMOX case, the graded and uniform SiGe films are grown first on a Si wafer, followed by oxygen implantation into the uniform composition SiGe film. High temperature annealing leads to creation of a buried SiO_2 film. Ge tends to segregate out of the buried oxide, increasing Ge content of the SiGe films beyond the oxide interface. Mizuno *et al.* have recently shown that the Ge content of a SiGe on oxide structure can be increased subsequent to the SIMOX process by high temperature oxidation of the SiGe layer.⁸⁴

5. Porous Si based process: ELTRAN

Another approach to defining a thin layer, which is transferred from a seed wafer to a handle wafer, utilizes the properties of porous Si. This concept was developed by Yonehara *et al.* and is known as epitaxial layer transfer or ELTRAN.^{85,86}

Porous Si is formed by an electrochemical reaction when Si constitutes the anode of an electrolytic cell with an HF

solution as the electrolyte. The etching process cuts a random network of nanometer scale pores in Si, producing a porous layer that has a fraction of the density of Si and a very large surface-to-volume ratio ($200\text{--}1000\text{ m}^2\text{ cm}^{-3}$).^{87,88} In the early 1980s, there was much work done to utilize this surface area for rapid oxidation of porous regions under nonporous islands of Si, in order to form SOI—this was the full isolation with porous oxidized silicon (FIPOS) method listed in Table I. FIPOS and many other approaches that required pre-patterning of the wafers were largely abandoned when SI-MOX and bonded wafers became available.

The ELTRAN technique takes advantage of the fact that porous Si is mechanically weak, but still preserves the single crystalline quality of the wafer on which it was formed. Yonehara *et al.*⁸⁹ have improved epitaxial Si growth on top of the porous layer, which was previously shown by Baumgart *et al.*⁹⁰ To accomplish this, they had to seal the pores at the top of the porous Si layer using high temperature annealing in hydrogen ambient. An epitaxial Si layer is grown on top of the sealed porous Si, then a thermal oxide is grown on top of the epitaxial layer, and the wafer is bonded to a handle wafer. Since porous Si is mechanically weak, it can be cracked, for example, with a fine and powerful water jet. As a further refinement, instead of one porous Si layer, two layers are formed with different pore morphology. By suitably changing current flow conditions during anodic etching, a layer with very fine pores is formed at the surface, with a second layer that has coarser pores positioned deeper into the substrate, as shown schematically in Fig. 15. Since there is considerable interfacial stress at the boundary between these two porous layers, the water jet causes cracking along the planar interface, leading to more uniform cleavage.

After wafer cleavage, the residual porous Si on the SOI wafer is etched away, and the newly exposed SOI wafer surface is smoothed by a second application of hydrogen annealing at about 1100°C . The wafer that donated the epitaxial film can be reclaimed, polished if necessary, and then used again.

III. CHARACTERIZATION OF SOI WAFERS

The evaluation of SOI structures requires traditional techniques and some new ones. These techniques must be able to overcome difficulties that are intrinsic to SOI struc-

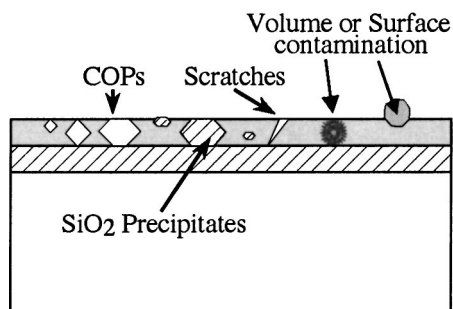


FIG. 17. COPs and other defects that can be observed in SOI. Threading dislocations and stacking faults are not shown.

tures: very thin Si films, BOX isolation, multiple Si/SiO₂ interfaces, defects unique to SOI, in-depth inhomogeneities, stress effects, etc. Most physical-chemical analyses (RBS, SIMS, Auger, ellipsometry, x rays) and microscopic observations (TEM, AFM, etc.) are still suitable after some degree of adaptation.

The electrical properties, which impact the performance of integrated circuits, are expected to be essentially the same as in bulk Si. Precise characterization is not straightforward because certain conventional methods are no longer applicable in very thin films. This limitation creates an opportunity for implementing novel techniques.

Below we review a few diagnostic measurements that are important for SOI wafer evaluation.

A. Si and BOX thickness measurements

Since an SOI wafer includes two films positioned on top of a bulk Si wafer handle and in most cases the devices of interest are contained within these films, characterization of these layers is of critical importance. Dimensional control of these films is of interest as well as their mechanical and electrical properties, crystalline defects, interfacial defects between the semiconductor and the oxide, etc.

Film thickness measurements are usually done optically, utilizing one of the following methods: variable-angle single-wavelength reflectometry, spectroscopic reflectometry, single-wavelength ellipsometry, and spectroscopic ellipsom-

etry. These methods involve fitting a set of data points to a computed multilayer model spectrum and each can in principle provide a correct answer. However, fitting of the data can lead to several possible local minima, and it is often easier to identify the true minimum by using more than one measurement technique. Since processing of conventional Si wafers also requires measuring of thin film stacks, many commercial tools are available for rapid evaluation of thin films on Si.

For films with well-characterized optical constants and atomically sharp, smooth interfaces, the measurements are relatively straightforward and accurate. However, such perfection is not always available. Early SIMOX structures had very rough interfaces on both sides of the BOX. Such roughness needed to be accounted for in the computational model. In spectroscopic ellipsometry, the effective medium approximation is often used, where a multiphase medium is assumed to compensate for the surface or interface roughness.⁹¹ The refractive index of the buried oxide in the case of SIMOX could differ considerably from the standard high temperature thermally grown oxide. Finally, Si islands buried inside the BOX were characteristic of SIMOX material until very recently. Since these Si inclusions are much smaller than the diameter of the probing beam, their main effect is to modify the space averaged refractive index n and the extinction coefficient k . Fortunately, the continuing progress in SIMOX technology has reduced these problems considerably. SOI wafers that are based on bonding feature a buried oxide that is thermally grown, and both buried Si/SiO₂ interfaces are reasonably smooth, so thickness measurements tend to be easier and more accurate. The optical measurements are quite precise for the top Si film with its high refractive index $n \approx 3.5$. Since SiO₂ has $n \approx 1.45$, data fitting is much less sensitive to small variations in the BOX thickness, but for most device applications this is a less critical parameter. Typical thickness uniformity data for 300 mm wafers produced by the Smart Cut™ process are shown in Fig. 16.

Depending on the application, different thicknesses of Si and BOX are required. CMOS circuits are built on SOI films that are getting progressively thinner, from 150 nm in the mid-1990s to about 50–80 nm in 2002.⁹² By 2012, films as thin as 5 nm may be required, as is discussed in Sec. VI. BOX thickness is not shrinking as rapidly, and in 2002 it is typically on the order of 100 nm, but thinner oxides will also be needed in the future. Bipolar and power devices require thicker films, on the order of 1 μm for both Si and the BOX. Some high voltage devices need up to 10 μm film thickness.

SOI wafers are very convenient for many MEMS applications—the requirements vary greatly, anywhere from 1 to 100 μm for Si, and 0.5 to 5 μm for the BOX. Photonic waveguides in SOI typically utilize Si films that are about 1 μm thick.

Films used in ULSI applications become thinner while the wafer diameter is now transitioning from 200 to 300 mm.⁹² In a few years SOI wafers will need to contain a monocrystalline layer that is 10 ± 0.5 nm thick and 300 mm in lateral dimension, with an aspect ratio of 3×10^7 to 1. Fabricating and measuring such thin and uniform layers is an important challenge for the SOI industry.

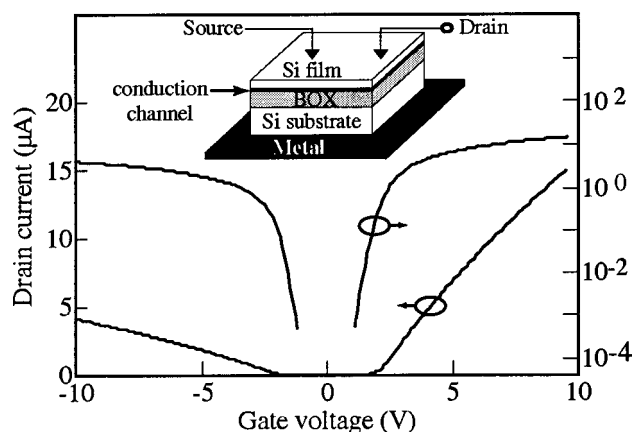


FIG. 18. Configuration of the pseudo-MOS transistor and typical drain current vs gate voltage characteristics (linear and semilogarithmic scales) in a thin SOI film.

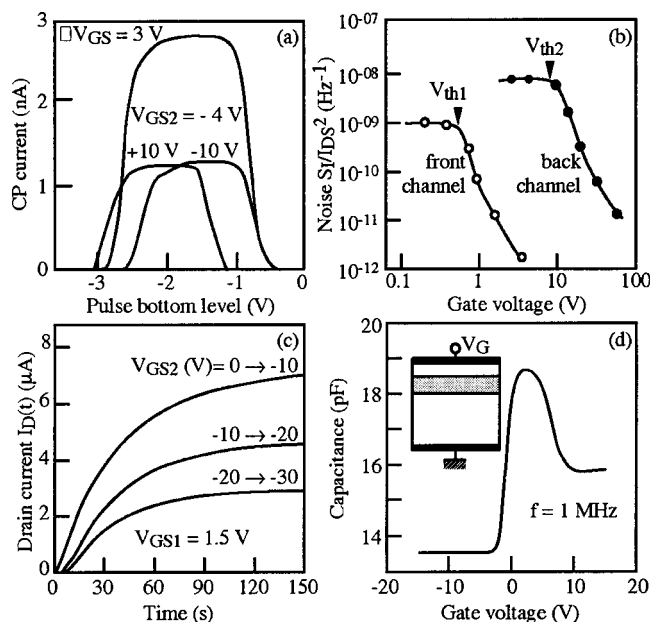


FIG. 19. Useful characterization techniques and typical signatures in SOI devices: (a) front-gate charge pumping for various back-gate bias, (b) normalized noise factor versus front/back gate voltage, (c) drain current transients, and (d) capacitance–voltage curve in a SIS structure.

B. Structural defects

Various defects can be observed in SOI structures, though improvements in processing have greatly reduced their frequency of occurrence. Some defects are of conventional nature, the same as encountered in bulk Si and in epitaxial Si films, e.g., dislocations and stacking faults. In SOI, the majority of dislocations are threading through the thickness of the film, terminating at the BOX and the surface. Dislocation densities in early SIMOX films were $>10^{10}$ cm⁻², but the advancements in fabrication technology brought the density down^{42,93} to 10^3 – 10^5 cm⁻². This was further facilitated by reductions in the implant dose required to form a BOX film. Many other defects are unique to the SOI and to the method of fabricating SOI wafers. Wafers produced by bonding can in principle have voids at the bond interface, even though in modern bonding operations in a class 1 cleanroom such defects—usually caused by dust particles—are exceedingly rare. Si pipes through the BOX, and to a lesser extent SiO₂ or silicide pipes through the Si film, occasionally happen in SIMOX wafers. Crystal originated particles, known as COPs, are actually octahedral voids that form within the Si boule during the conventional CZ (Czochralski) crystal growth through the process of vacancy condensation. Such voids reduce the device yield in conventional bulk Si technology, but are even more of a problem in SOI, which has two interfaces that can intersect the COP defects, as shown schematically in Fig. 17.

C. Electrical characterization of SOI material

1. Pseudo-MOSFET

Utilization of the pseudo-MOS transistor (Ψ -MOSFET) is an exciting approach that takes full advantage of the upside-down MOS structure of SOI materials (Fig. 18). The

Si substrate acts as a gate terminal and is biased to induce a conduction channel (inversion or accumulation, according to the polarity) at the interface. The BOX and Si film, respectively, play the roles of gate oxide and transistor body. To operate *in situ* the Ψ -MOSFET, low pressure probes are placed on the film and form source and drain point contacts.⁹⁴ The Ψ -MOSFET is very much like the transistor that Shockley and his group attempted to operate half a century ago, but at that time SOI was not available.

Figure 18 demonstrates that indeed very pure MOSFET-like characteristics are obtained, which in turn deliver invaluable information on the material parameters. In both strong inversion and accumulation regions, the linear drain current obeys the classic equation

$$I_D = f_g \mu C_{ox} V_D (V_G - V_{T,FB}), \quad (1)$$

where $f_g \approx 0.75$ is a form factor which accounts for the 2D distribution of current lines.

Increasing the probe pressure (up to 0.5–0.7 N) reduces the series resistance. The inversion region is identified by more sensitivity to pressure and transient effects, because the existence of a depletion region makes the probe-to-channel access resistance higher and the supply of minority carriers longer. The slope of $I_D/g_m^{0.5}$ vs V_G curves yields the mobility of electrons and holes, whereas the intercept with the V_G axis gives the threshold (V_T) or the flatband (V_{FB}) voltage. The density of traps at the film–BOX interface is calculated from the subthreshold slope in weak inversion, the fixed charge density from V_{FB} , and the film doping from the difference ($V_T - V_{FB}$). The carrier lifetime is evaluated by recording the transient drain current after the gate is pulsed in strong inversion.⁹⁵

The Ψ -MOSFET operation and parameter extraction techniques have been validated by 2D simulations. In order to avoid geometry-related corrections, the probes should be located far enough from the edges of the Si island and have a diameter much smaller than the channel length. The method was successfully tested on SOI films of variable thickness (from a few microns down to 10 nm) and is currently used to optimize the process and monitor the quality of SOI wafers. The Ψ -MOSFET has also been demonstrated on SOS films,⁹⁶ after thinning the substrates down to 30 μ m and applying 1 kV.

An intriguing aspect is that the metal–semiconductor Schottky contacts behave as ohmic terminals. We believe that this transformation is made possible by the defects generated when applying pressure on the probes. The Ψ -MOSFET can also be operated in circular, Corbino-like configuration, by using mercury probes.⁹⁷ In this case, the preparation of ohmic contacts is more difficult, and requires careful surface cleaning.

2. Other measurements

In principle, the Hall effect provides the carrier mobility and film doping. However, we have to be aware that thin films have a very large sheet resistance, $R_s = \rho/t_{si}$, and can be fully depleted or inhomogeneous. The solution is to use

the substrate bias, like in the Ψ -MOSFET, for separating the contributions of the film volume and interface.

Other methods that can be of interest, are:³

- (i) four-probe measurements of the average resistivity, and spreading resistance for the resistivity profile;
- (ii) surface photovoltage measurement to determine the diffusion length of minority carriers;
- (iii) photoconductivity for extraction of the carrier recombination lifetime;
- (iv) photoinduced current transient spectroscopy (PICTS) for investigation of deep-level traps; and
- (v) “nondestructive” detection of pinholes by using the decomposition of CuSO_4 solution when a leakage current flows through the BOX.

3. Device-based characterization

The properties of the starting SOI material are usually inferred indirectly from the characteristics of MOS test devices and from the performance of integrated circuits. Such an evaluation is necessary, but can be misleading because the original parameters of the wafer are modified during the CMOS process. We briefly review several efficient techniques that have been adapted to SOI.³

(i) Static characteristics in MOS transistors. While most parameter extraction methods are similar in SOI and bulk-Si transistors, the interpretation of the data should address SOI specifics (interface coupling and floating-body effects).

(ii) Charge pumping for characterization of fast interface traps in short-channel MOS devices. The adaptation to SOI requires a transistor with body contact or a gate-controlled p - i - n diode. In a typical CP curve [Fig. 19(a)], obtained by varying the bottom level of the gate pulse while keeping the pulse magnitude constant, the plateau level gives the trap concentration.

(iii) Low-frequency noise spectroscopy for analysis of slow traps located deeper in the oxide. These traps contribute to fluctuations in the minority carrier concentration, which is the primary source of $1/f$ noise in MOS transistors. The density of traps is determined from the plateau of the noise factor S_I/I_D^2 in weak inversion [Fig. 19(b)]. Excess noise can be induced by impact ionization and imperfect body contacts. In small area MOSFETs, the trapping of one carrier becomes detectable in the time domain as a random telegraph signal (RTS).

(iv) Lifetime measurements. Several transient techniques have been developed for SOI transistors, based on Zerbst principles, except that the drain current (not the capacitance) is monitored. The gate pulse is designed to induce a temporary excess or deficit of majority carriers, so that equilibrium is reached by recombination-generation mechanisms (see also Sec. VB). The duration of the transient [Fig. 19(c)] provides the carrier lifetime and surface velocity.

(v) In-depth profiling using a MOS-Hall device (depletion-mode transistor with additional side contacts). Magnetotransport measurements are performed as a function of gate bias. By gradually depleting the film, the conducting region shrinks and the average properties are modified. The

mobility and concentration profiles are calculated by differentiation with respect to V_G .

MOS capacitance and conductance are difficult to apply to SOI for extracting the parameters of Si-SiO₂ interfaces. Although the conventional MOS capacitor theory and equivalent circuit can be adapted, severe limitations arise due to the large number of parameters (two oxides and three interfaces). The formation of a body contact for independent probing of the front and back interfaces is only a partial solution. Not only is the contact useless in fully depleted films, but also the series resistance of the film comes into play and renders the interpretation of the data difficult. Atypical $C(V_G)$ curves are obtained for silicon-insulator-silicon (SIS) capacitors, where depletion regions can develop on each side of the buried oxide [Fig. 19(d)]. The BOX thickness can be deduced from the peak capacitance, and the doping levels in the film and substrate from the two minima.

This short introduction to evaluation techniques is obviously incomplete. The message we wish to convey is that SOI characterization offers new opportunities but is very challenging. We recommend two principles that can alleviate problems: (i) current-based measurements should be preferred to capacitance data; and (ii) for one interface to be accurately characterized, the opposite interface has to be maintained in accumulation (decoupling effect).

IV. SOI DEVICES

A. Motivations for SOI circuits

SOI chips consist of millions of single-transistor islands dielectrically isolated from each other and from the underlying silicon substrate. On one hand, the vertical isolation protects the thin active silicon layer from most parasitic effects induced by the very “bulky” substrate: leakage currents, radiation-induced photocurrents, latch-up effects, etc. On the other hand, the lateral isolation makes interdevice separation in SOI free of complicated schemes of trench or well formation. The overall technology and circuit design are, in this respect, highly simplified and result in more compact VLSI chips.

The source and drain regions extend down to the buried oxide (see Fig. 1), yielding reduced junction surface, lower leakage current, and junction capacitance. This offers the opportunity to fabricate CMOS circuits with lower power dissipation in standby and operating modes, improved speed, and wider temperature range. More innovative devices (multiple gate MOSFETs, power transistors, sensors, MEMS, etc.) can be conceived and combined in SOI that intrinsically is a flexible structure, with adjustable thickness for the film and buried oxide.

A second class of advantages is related to the superior capability of SOI transistors to face scalability challenges. The key feature is that, unlike the case of bulk Si, the SOI film thickness stands as a tunable parameter for device shrinking: the thinner the film, the lower the drain-to-body field penetration which causes drain-induced barrier lowering (DIBL) effects. Moreover, the limited extension of drain and source regions makes SOI devices less vulnerable to short-channel effects, originated from “charge sharing” be-

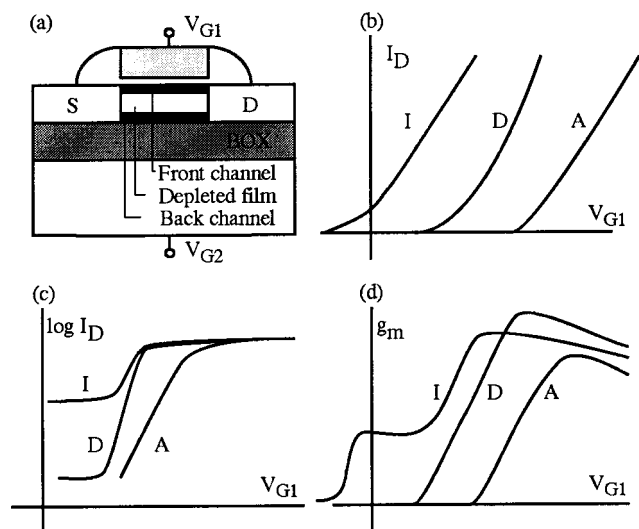


FIG. 20. Configuration of a fully depleted n -channel SOI MOSFET (a) and generic front-channel characteristics: (b) $I_D(V_{G1})$ in strong inversion, (c) $\log I_D(V_{G1})$ in weak inversion, and (d) transconductance $g_m(V_{G1})$. The back interface is biased in accumulation (A), depletion (D), or inversion (I).

tween gate and junctions. We will see in Sec. VIB that scaling problems can also be alleviated by replacing the standard MOSFET structure with novel architectures able to pass the frontier between microelectronics and nanoelectronics.

B. CMOS/SOI circuits

High performance CMOS circuits, integrated on SOI and compatible with low-power/low-voltage and/or high speed ULSI applications, have been frequently demonstrated with deep-submicron devices.^{98–100} For example, ring oscillators with 50 nm gate-lengths reach delay times below 10 ps/stage.¹⁰¹ Frequencies beyond 150 GHz have also been achieved. It is in the highly competitive domain of circuits operated with a single-cell battery supply (0.5–1 V) that SOI can fully express its potential. A small gate-voltage swing is suited to switch a transistor from an off-to on-state. CMOS/SOI devices exhibit superior performance because low leakage currents and quasi-ideal subthreshold slopes (60 mV/decade at room temperature) are achievable, hence the threshold voltage can be lowered below 0.3 V.

Complex circuits, with a major impact on mainstream microelectronics, include high performance (2 GHz)¹⁰² as well as low power (0.5 V–200 MHz) microprocessors,¹⁰³ Gbit-range DRAM and SRAM memories, rf circuits, etc. Including more specific examples is impractical because new records are frequently set: their ephemeral existence is the best proof of the dramatic growth in SOI technology. Repeated comparisons show that operation at similar voltage offers a gain in performance, as compared to bulk-silicon, of about 20%–30%, whereas operation at similar low-power dissipation yields more than doubles the gain. In other words, SOI circuits of generation n and bulk-Si circuits from the next generation ($n+1$) perform comparably. This argument is strong enough for major companies to include SOI technology in their strategy. IBM, Motorola, AMD, Sharp,

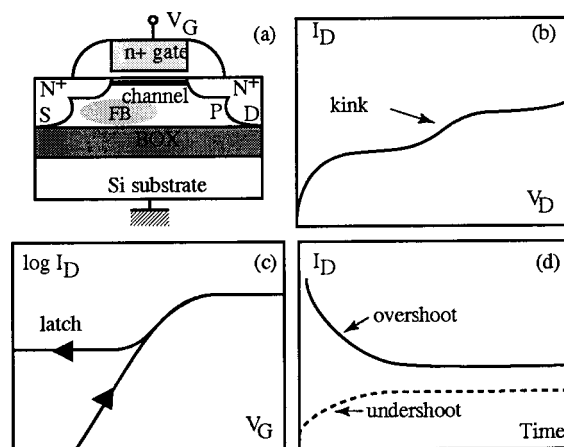


FIG. 21. Configuration of a partially depleted SOI MOSFET (a) and typical floating-body effects: (b) kink in $I_D(V_D)$ characteristics, (c) latch in $\log I_D(V_G)$ characteristics, and (d) drain current overshoot and undershoot.

Intel, etc., have announced the commercial development of SOI-enhanced PC processors and mobile communication devices.

Fully depleted CMOS/SOI circuits are still operational at temperatures beyond 300 °C, very attractive for oil, aeronautics, and automobile industries. The leakage current is much smaller and the threshold voltage is less temperature sensitive (≈ 0.5 mV/°C) than in bulk Si. SOI circuits can also be tailored for extreme environments, able to sustain doses above 10 Mrad for space applications.

SOI transistors with dynamic-threshold (DTMOSFETs) are interesting devices dedicated to low-voltage/low-power applications. The gate and body are interconnected so that increasing the gate voltage in weak inversion causes a simultaneous raise in body potential and a gradual decrease in threshold voltage (dynamic V_T): the coupling between gate voltage and inversion charge is excellent and results in improved subthreshold slope, drive current, transconductance, and short-channel behavior.¹⁰⁴

C. Bipolar and high-voltage SOI devices

Thin-film bipolar transistors, with lateral configuration, and BiCMOS circuits have high cutoff frequency. Hybrid MOS-bipolar transistors (gate connected to the floating body) show increased current drive and transconductance.⁴ Vertical bipolar transistors need thicker films; an alternative solution for thin-film SOI is to replace the buried collector by an inversion layer activated by the back gate.⁴

Lateral double-diffused MOS transistors (LDMOSFETs), with long drift region, were fabricated on 0.2–2 μm SOI films and showed 90 V–1.3 A capability.¹⁰⁵ Vertical DMOS can be accommodated in thick-film SOI. Using a local buried oxide (patterned SOI that was discussed in Sec. IIB 3), vertical power devices (LDMOS, IGBT, U MOS, etc.) are located in the non-SOI section of the wafer, whereas a neighboring low-power CMOS/SOI circuit infuses intelligence in the whole circuit. A variant of this bulk Si/SOI mixing is the “mezzanine” structure, used for the fabrication of 600 V/25 A smart-power devices.¹⁰⁶ The double-SIMOX

material has served to combine a power MOSFET/bulk with a double-shielded high-voltage lateral CMOS/SOI and an intelligent low-voltage CMOS/SOI circuit.¹⁰⁷

The family of SOI devices also includes optical switches, waveguides and modulators, microwave transistors integrated on high resistivity SOI wafers, and various 3D circuits such as inverters with superposed *n*- and *p*-channel transistors. An elaborated image-signal processor is organized in three levels with vertical interconnects: photodiode arrays in the upper SOI layer, fast analog-to-digital converters in the intermediate SOI layer, and arithmetic units and shift registers in the bottom bulk Si level.¹⁰⁸

V. TYPICAL MECHANISMS IN SOI TRANSISTORS

A. Fully depleted MOSFETs

In SOI MOSFETs [Fig. 20(a)], two inversion channels can be activated, one at the front Si–SiO₂ interface and the other at the back Si–BOX interface. Full depletion (FD) happens when the depletion region covers the whole transistor body. The depletion charge is constant and cannot extend further when the gate bias increases. The excellent coupling between the gate bias and the inversion charge offers improved current and subthreshold slope. The front-and back-surface potentials become inter-related. Interface coupling means that the electrical characteristics of one channel vary with the bias applied to the opposite gate. In practice, the front-gate measurements may include contributions from the BOX and from the BOX/bulk Si interface, and highly depend on the back gate bias.

The characteristics are complex (Fig. 20) and totally new $I_D(V_{G1})$ relations, controlled by both gate voltages $V_{G1,2}$, apply to fully depleted SOI-MOSFETs. Each curve can be explained by the variation of a dominant parameter.³

(i) The threshold voltage decreases linearly with increasing V_{G2} [Fig 20(b)] between two plateaus corresponding, respectively, to accumulation and inversion at the back channel.¹⁰⁹ The coupling factor is approximately equal to the thickness ratio between gate oxide and BOX.

(ii) The subthreshold slope reflects the contributions of front and back interface traps. It is a maximum for depletion at the back interface [Fig. 20(c)].¹¹⁰ The ideal value (60 mV/decade at room temperature) is approached when the trap densities are low and the BOX is much thicker than the gate oxide and silicon film.

(iii) The transconductance exhibits a plateau when the back channel is activated [Fig. 20(d)]. The effective mobility and series resistance depend on back-gate bias.¹¹¹ The worst case occurs for accumulation at the opposite interface: not only is the vertical field large enough to cause mobility degradation, but also the source/drain extensions can get depleted which increases the access resistance.

The qualitative features evoked above are well captured by conventional 2-interface models.^{109–111} Also available are 3-interface models which match better the modern trend of using thinner films and BOX. In this case, the influence of defects located at the bottom of the BOX, as well as the possible formation of a depletion region underneath the BOX, is accounted for.¹¹²

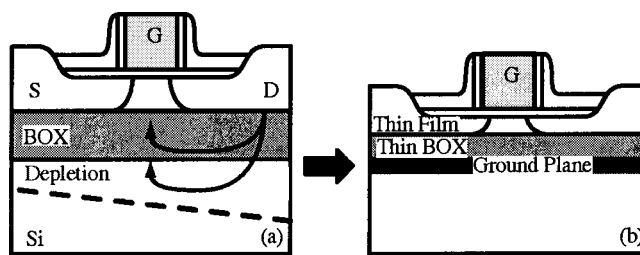


FIG. 22. (a) Schematics of field penetration from drain to body, via the film, BOX, and Si substrate; and (b) optimized MOSFET architecture using a ground plane.

Defect coupling in FD MOSFETs means that carriers flowing at one interface are influenced by the presence of defects at the opposite interface. In particular, an apparent degradation of the front channel properties can be induced by remote damage that is actually located at the back interface or in the buried oxide. This situation is frequently observed after back interface degradation via radiation or hot-carrier injection.^{3,113}

Self-heating, conveyed by the low thermal conductivity of the BOX, is responsible for current lowering and onset of negative output conductance in the saturation region. The dominant effect is the reduction of the carrier mobility with increasing channel temperature. However, more parameters (threshold voltage, saturation velocity, bipolar gain, interconnect temperature, etc.) have to be taken into account for accurate modeling.¹¹⁴ As the silicon layer is thinner, self-heating is accentuated; this is why FD SOI MOSFETs are more affected. The channel temperature is also raised with increasing the BOX thickness and the channel-to-contact separation.¹¹⁵ Fortunately, self-heating is highly reduced under dynamic and/or low-voltage operation.

B. Partially depleted MOSFETs

In partially depleted (PD) SOI MOSFETs, the depletion charge does not extend from one interface to another, and a neutral region subsists [Fig. 21(a)]. Interface coupling effects are cancelled, but instead floating-body effects arise. The kink effect [Fig. 21(b)] is triggered by majority carriers, generated by impact ionization, which collect in the neutral region. The body potential is raised and the threshold voltage is lowered. The kink is materialized in excess current and low-frequency noise in saturation. In weak inversion and for high drain bias, a similar positive feedback is responsible for negative resistance regions, hysteresis in $\log I_D(V_G)$ curves, and eventually for transistor latch [Fig. 21(c)].

The floating body may also induce transient variations of body potential, threshold voltage, and current. When the gate is switched on [Fig. 21(d)], majority carriers are expelled from the depletion region (instantly formed by capacitive coupling) and collect in the neutral body, giving rise to a drain current overshoot. The drain current decreases gradually with time during electron–hole recombination. A reciprocal undershoot occurs when the gate is switched from strong to weak inversion: the drain current increases with time [Fig. 21(d)] as the majority carriers are generated and allow the depletion depth to shrink.¹¹⁶

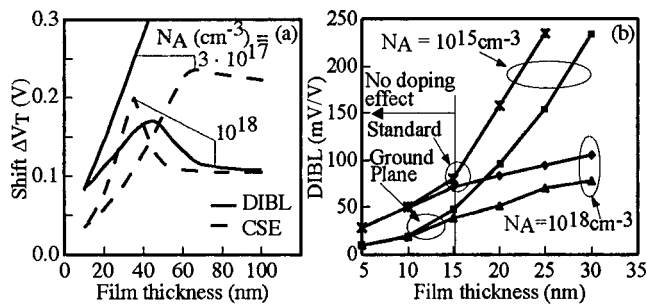


FIG. 23. Threshold voltage lowering vs film thickness: (a) charge sharing and DIBL effect in a 100 nm long SOI MOSFET, and (b) fringing field effect in a 80 nm long MOSFET with various doping levels and architectures (standard or ground plane) (Ref. 121).

More complex transients are observed, even in FD MOSFETs, by switching both gates: a temporary nonequilibrium condition is induced by one gate, whereas the overall effect is observed by monitoring the current flowing at the opposite channel.¹¹⁷ As a general rule, the amplitude of current overshoot or undershoot is proportional to the difference between the final and initial body charges, and the transient duration depends on the generation-recombination rate in the film volume, at interfaces and on the edges. Although the carrier lifetime has remarkably been improved, in state-of-the-art MOSFETs the transient time is dramatically reduced for several reasons:

- (i) In short channels, the source and drain junctions efficiently remove the majority carriers.
- (ii) In narrow channels, the edges, which are more defective, play a dominant role.¹¹⁸
- (iii) In ultrathin oxides, gate tunneling current becomes large enough to compensate the body charge.¹¹⁹

Transient effects are of particular concern at high drain bias, where impact ionization represents an additional source of majority carriers. During high-frequency switching of integrated circuits, the transistor body does not always reach equilibrium. Designers know how to use the extra overshoot current for improving the circuit speed. However, the charging and discharging of the body is an iterative process that may cause history and memory effects as well as dynamic instabilities. The solution for alleviating floating-body effects

is to design body contacts at the expense of an increased die size. In ultrathin films with large sheet resistance, the body contacts are far from being ideal (intrinsic resistance, potential barrier, and excess noise). This is why body contacts are provided only to selected transistors that play a critical role in the circuit.

VI. NEW DIRECTIONS IN SOI DEVICES

A. Short-channel effects (SCE)

In both fully and partially depleted MOSFETs with sub-micron length, the lateral bipolar transistor (source-body-drain) can be easily turned on. The basic mechanism is the raise in body potential, by impact ionization, which causes a forward bias of the source-body junction. The activation of the parasitic bipolar transistor has beneficial (extra current) or detrimental (premature breakdown, latch, etc.) consequences. Parasitic bipolar action is enhanced in *n*-type channels, shorter devices, thinner and wider films, and at higher temperatures.

The reliability of short-channel MOSFETs is affected by hot-carrier injection into the oxide. The degradation mechanisms are very complex in SOI, where two oxides and two channels are involved. In *n* channels, most defects are created at the interface where the electrons flow; exceptionally, when the transistor is biased in the breakdown region, injection into the opposite interface occurs and causes defect-coupling effects. The device aging is accelerated at low gate bias and when the back interface is accumulated.¹¹³ In *p* channels, electrons generated by front-channel impact ionization become trapped in the buried oxide. An apparent degradation of the front interface again occurs via coupling.¹¹³

A surprising short-channel effect in SOI transistors is the metamorphosis of partial depletion into full depletion. The lateral depletion regions, governed by the source and drain, not only cover a large portion of the body, but also reduce the *effective* doping in the body, so enabling full depletion by gate action. In addition, the lateral profile of the back interface potential can be highly inhomogeneous: from depletion in the middle of the channel to weak inversion near the channel ends. This localized weak inversion region explains the degradation of the swing.

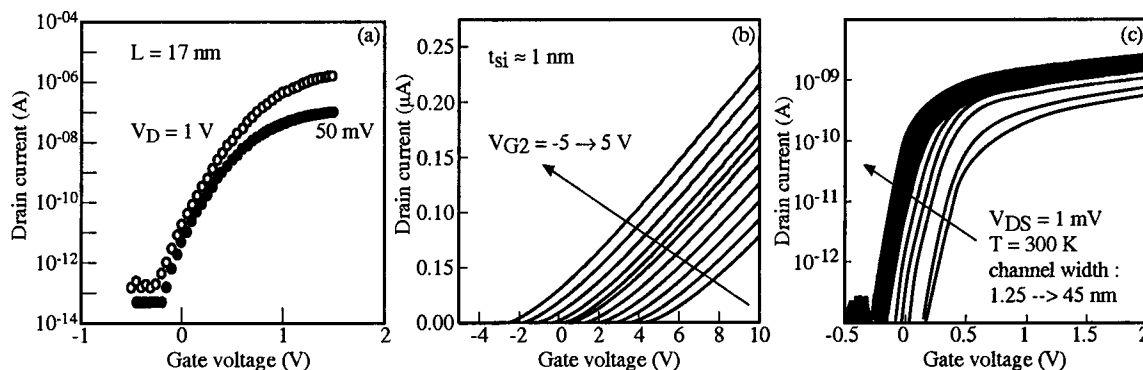


FIG. 24. Drain current vs gate voltage characteristics in record miniaturized SOI MOSFETs: (a) 17 nm long (Ref. 124), (b) 1 nm thick (Ref. 126), and (c) transistors with variable width including 1 nm wide MOSFET (Ref. 127) transistors.

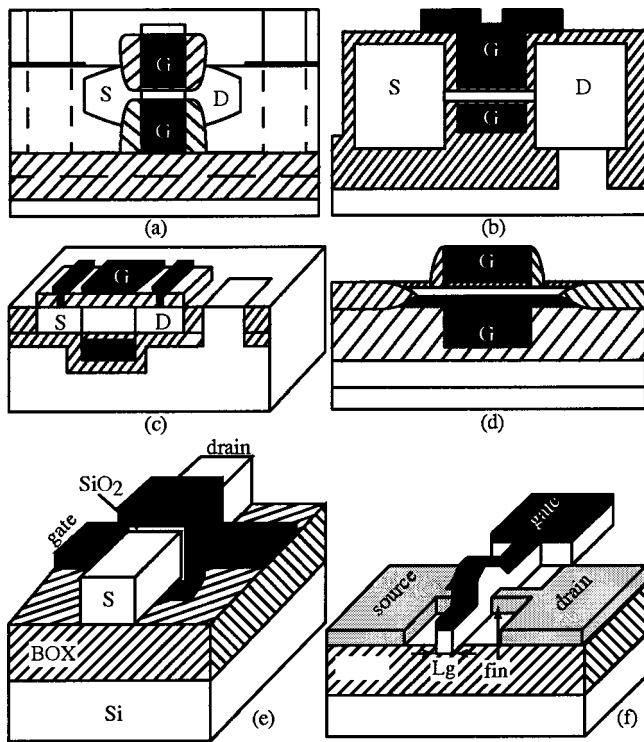


FIG. 25. Technological solutions demonstrated for double-gate SOI MOSFETs: (a) sacrificial SiGe layer, (b) tunnel epitaxy, (c) epitaxial lateral overgrowth, (d) bonding, (e) gate-all-around (GAA), and (f) FINFET.

More familiar short-channel effects, resulting in threshold voltage roll-off, are *charge sharing* (between gate and terminals) and *drain-induced barrier lowering* (DIBL). An extra DIBL effect is due to the lateral penetration of the electric field into the BOX and underlying substrate (Fig. 22).^{120,121} The fringing field causes an increase in the potential at the film–BOX interface, very much as if the back gate was positively biased: *drain-induced virtual substrate biasing* (DIVSB). Due to DIVSB and interface coupling, the front-channel threshold voltage and subthreshold slope are lowered.¹²¹

B. Scaling trends

The scaling principles for bulk-Si MOSFETs require a reduction in junction thickness and an increase in doping

level, which adversely affect the junction capacitance and carrier mobility. Doping related difficulties will probably terminate the scaling of bulk Si or partially depleted SOI MOSFETs at about 35–50 nm gate length. Fortunately, the scaling rules and design windows are more relaxed for fully depleted SOI transistors because additional tunable parameters (film and BOX thickness, substrate doping, and biasing) are available for device optimization.

The minimum channel length that can be envisioned is given by $L \approx 3\lambda$, where λ is a SCE-free length, calculated by solving the Poisson equation. Several expressions have been proposed:^{122,123}

$$\lambda_{FD} = [0.5(\epsilon_{Si}/\epsilon_{ox})t_{Si}t_{ox}]^{1/2}$$

or

$$\lambda_{FD} = [t_{Si} + (\epsilon_{Si}/\epsilon_{ox})t_{ox}]/\pi \quad (2)$$

and all deliver a clear message: the intrinsic length is dramatically reduced by using ultrathin Si films, whereas the doping impact becomes irrelevant. Figure 23(a) shows that SCE, such as charge sharing and DIBL, are rapidly vanishing in thinner films. Actually, below a critical film thickness (15 nm for 80 nm long MOSFETs), no doping is needed at all. This is extremely beneficial in terms of high carrier mobility, but implies using metal gates to control the threshold voltage.

The impact of the fringing fields (DIVSB) can be countered by using thin and/or low- k (low dielectric constant k) BOX, at the expense of increased parasitic capacitance, larger influence of the depletion regions underneath the BOX, and enhanced interface coupling effects. Moreover, a ground plane (GP), located below the BOX [Fig. 22(b)], is able to suppress the field penetration and the depletion region in the substrate. Figure 23(b) shows that DIBL is significantly improved with a GP. Combining a 50-nm-thick BOX with a ground plane allows using films 50% thicker (20–30 nm), which match the capability of current SOI processes.¹²¹ A GP can be achieved by ion implantation under the BOX or by bonding two wafers, one of which has a highly doped surface region or a metal overlay.

The optimized architecture of sub-50-nm-long FD MOSFETs will combine several recipes: very thin films with low doping, moderately thin or low- k BOX (including silicon-on-

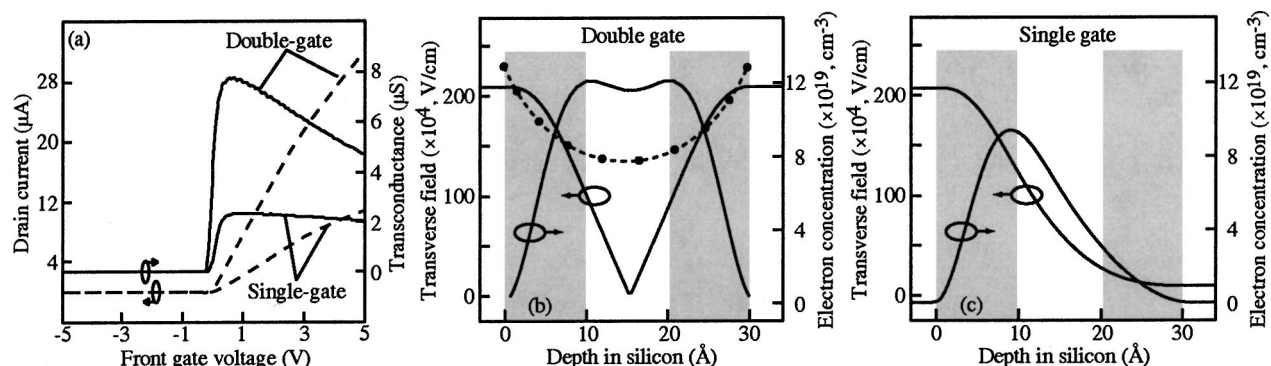


FIG. 26. Comparison of transconductance curves (a) and profiles of carrier and potential distributions in 3-nm-thick SOI MOSFETs with double-gate (b) and single-gate (c) operation (Ref. 126).

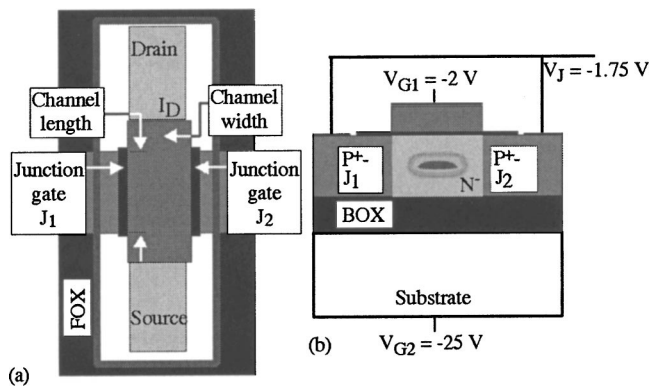


FIG. 27. (a) Aerial view of the four-gate SOI transistor and (b) numerical simulation showing the cross section of a quantum wire formed by depleting all gates (Ref. 143).

nothing or SON), mid-gap gate, and perhaps a ground plane. It is expected from Eq. (2) that FD MOSFETs will reach the limit of 20 nm long and 5-nm-thick bodies. Elevated source and drain terminals will be needed to answer the problem of series resistance in ultrathin films. A crucial challenge for wafer suppliers is to provide soon enough ultrathin films with excellent quality and uniformity. Otherwise, thickness fluctuations will be responsible for intolerable SCE, induced by DIBL and field penetration. The depletion charge variations caused by nonuniform film thickness are of lesser importance.

It is worth noting that a small-geometry device also implies a narrow channel. The parasitic current flowing on the sidewalls of the transistor depends on the isolation technology, local defects, stress, doping segregation, and lifetime degradation.¹¹⁸ Floating body effects tend to vanish whereas new coupling effects are triggered. A strong interaction develops between the three dimensions of the transistor: the scaling of the length or width is made easier when the body thickness is simultaneously reduced.

C. Ultimately small MOSFETs

Figure 24 reproduces $I_D(V_G)$ characteristics of the smallest transistors ever fabricated. The goal is to pass the 35 nm barrier, which looks reasonable from the SOI viewpoint, but not for bulk silicon technology. The 17 nm long transistor of Fig. 24(a) has double-gate configuration, but more conventional devices have been demonstrated in the same length range.^{124,125}

The absolute physical minimum thickness of an SOI transistor is one atomic plane. However, transport properties of a monolayer of Si would be very different than those of crystalline Si. Experimental results exist for 1-nm-thick MOSFET [Fig. 24(b)], where four monolayers of silicon do maintain MOS-like functionality.¹²⁶ Thickness-related effects on the carrier transport, interface coupling, and electrostatics become considerable and require full quantum mechanics treatment. A film thinner than 10 nm behaves as a vertical quantum well, the parameters of which can be modulated by the front and back gate voltages. The carrier and energy con-

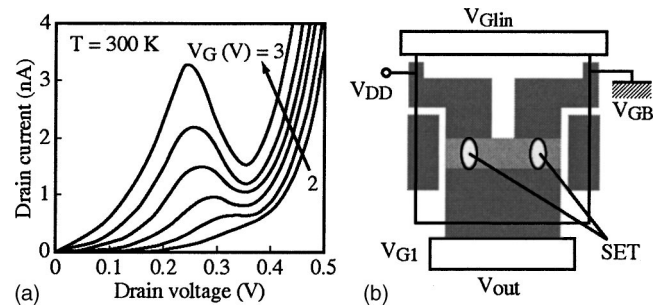


FIG. 28. (a) Characteristics of a p^+-n^+ tunneling diode on SOI (Ref. 133) and (b) configuration of a single-electron inverter on SOI (Ref. 146).

finement becomes significant below 10 nm, leading to an increase of the threshold voltage (although the depletion charge is reduced).

Also, the minimum channel width achieved so far is 1 nm.¹²⁷ Such a transistor is a quantum wire, where carrier confinement develops in the lateral direction. This again leads to an increased threshold voltage [Fig. 24(c)].

Let us now imagine an extremely miniaturized transistor, where the above dimensions would be combined. Instead of “short-channel effects,” we will have to use the new concept of *minimum-volume effects*. The body will not exceed 10^{-18} cm^3 and will contain just a few thousand silicon atoms. What would be the meaning of a doping level of 10^{16} cm^{-3} ? When dealing with less than one defect, one impurity or one trap, we will have to give up comfortable macroscopic notions (interface trap density, doping concentration, etc.).

D. Double-gate MOSFETs

Double-gate (DG) SOI MOSFETs have in principle two symmetrical gates interconnected, or a unique gate that surrounds the body (gate-all-around or GAA).⁴ DG MOSFETs can be planar, vertical, or mixed-mode (vertical film with side gates and horizontal transport). Fabrication was achieved with the Delta process,¹²⁸ epitaxial lateral overgrowth,¹²⁹ wafer bonding,¹³⁰ Fin process,¹³¹ tunnel epitaxy,^{132,133} SON,¹³⁴ etc. (Fig. 25). In the GAA process, a suspended Si membrane is formed by tunnel epitaxy, by etching a cavity in the BOX, or by growing a stack of sacrificial layers. The membrane is then oxidized and the gate is deposited around [Fig. 25(e)].

The DG concept was initially demonstrated, back in 1987 on conventional SOI MOSFETs by simultaneously biasing the front and back gates of a FD transistor. The formation of front and back inversion channels causes, by continuity, *volume inversion* in thin SOI films [see the dotted curve in Fig. 26(b), calculated with the Poisson equation].¹³⁵ The minority carriers flow in the middle of the film and experience less surface scattering, hence the mobility, transconductance, drive current, and $1/f$ noise are all improved.

The two gates exert ideal control on the potential and inversion charge, so that short-channel effects (charge sharing, DIBL, fringing field, and punchthrough) are highly reduced. Since the intrinsic length λ_{DG} is much lower in DG MOSFETs, as compared to single gate (SG) transistors [Eq.

(1)], they are now considered as the final metamorphosis of the MOS transistor,¹³⁶ especially beyond the 10 nm barrier. Fin technology has produced already 15–20 nm long DG MOSFETs with promising characteristics.¹²⁴ Numerical simulations including quantum effects, band-to-band tunneling, and direct source-drain tunneling tend to prove that transistors with 2 nm gate length still maintain acceptable characteristics.¹³⁷ Keeping in mind that the body thickness should be roughly 1/3 of its length, we conclude that the ultimate frontier for a DG MOSFET is 1 nm gate length, which would imply the use of one monolayer of silicon.

Measurements in 3-nm-thick transistor [Fig. 26(a)] show a large increase in transconductance for the DG mode,¹²⁶ which can be explained by the carrier distribution and mobility. Since the potential profile is symmetrical, the vertical field cancels in the middle of the film [Fig. 26(b)]. The self-consistent solution of Poisson and Schrödinger equations reinforces the volume inversion concept, indicating that most carriers flow far from the interfaces. However, the total inversion charge in the DG mode is just twice the value in the SG mode. The gain in transconductance beyond 200% [Fig. 26(a)] is due to a higher mobility in the middle of the film (negligible vertical field, less scattering) than near the interfaces.¹²⁶ Only in the DG mode can the carriers avoid the rough interface regions [Figs. 26(a) and 26(b)]. These empirical arguments have been confirmed by rigorous Monte Carlo simulations that reveal an increase of the electron mobility in DG MOSFETs 3–5 nm thick.¹³⁸ Direct mobility measurements have recently demonstrated the advantage of DG over single-gate MOSFETs.^{139,140}

An open question is the choice of symmetrical or asymmetrical gates. Different work functions for the front and back gates make easier the adjustment of the threshold voltage.¹⁴¹ In addition, a longer back gate, overlapping the source/drain extensions can also be beneficial. The back-gate biasing induces not only inversion in the channel but also accumulation in the extensions (electrical junctions).¹⁴² This field-effect management of the series resistance allows obtaining higher transconductance, while tolerating slight misalignments of the two gates.

E. From microelectronic to nanoelectronic devices

1. Four-gate transistor

The maximum number of gates in a transistor is not two, as claimed by DG MOSFET proponents, but four. The 4-gate transistor (G^4 MOSFET) is operated in accumulation mode and has the same structure as an inversion-mode partially depleted SOI MOSFET with two independent body contacts.¹⁴³ These lateral contacts play the role of source and drain in the G^4 MOSFET, whereas the former source and drain junctions now act as lateral gates [Fig. 27(a)]. The G^4 MOSFET has the standard front and back MOS gates plus the two lateral junctions that control the effective width of the body. The current flows perpendicular to the normal direction in the original PD MOSFET. The conductive path is modulated by mixed MOS JFET effects: from a tiny quantum wire, surrounded by depletion regions [Fig. 27(b)], to a strongly accumulated body. Each gate has the capability of

switching the transistor on and off. The independent action of the four gates opens new perspectives for mixed-signal applications, quantum wire effects, and quaternary logic schemes.

2. Tunneling devices

Since we will have to live with quantum and tunneling effects even in standard MOSFETs, a good approach is to take advantage of them, for constructing innovative types of transistors. It is also envisioned to import device concepts from III–V semiconductors into the Si family. For example, resonant tunneling transistors can be accommodated in ultrathin SOI films.¹⁴⁴ Fabricated in thicker SOI films, band-to-band tunneling diodes (n^+p^+), exhibit current–voltage characteristics with negative resistance [the curves have an N-shape, as shown in Fig. 28(a)]. SOI has the merit of providing excellent isolation that cancels the parasitic leakage current. In addition, the back gate can be used to increase, by accumulation, the local carrier concentration.^{144,145}

3. Single-electron transistors

The fabrication of tiny islands of semiconductors is greatly facilitated in SOI because the film is very thin and perfectly isolated in both lateral and vertical directions. In the family of more or less exotic nanoelectronic devices, the SET inverter is worth noting.¹⁴⁶ Nanometer-scale silicon islands are formed by anisotropic sacrificial oxidation controlled by stress effects. A special patterning of the silicon island, providing higher stress (lower oxidation rate) on the sidewalls is achieved prior to the oxidation. Two SET islands, properly interconnected and biased, give rise to an inverter with gain higher than unity [Fig. 28(b)].¹⁴⁶

VII. CONCLUSIONS

SOI substrates have become a vital part of Si technology. From its roots as specialized wafers for niche applications, SOI has moved into the mainstream, where it provides important enabling enhancements in circuit performance.

The future of SOI is even brighter, as device scaling into the sub-50 nm regime requires SOI architecture. It appears inevitable that the evolution of the MOS transistor will be continued in SOI structures. Shrinking the MOSFET size is the driving force and the possibility of using ultrathin films is the main SOI advantage. SOI transistors will follow the remaining stages of scaling by undergoing a gradual metamorphosis that will enhance the performance and infuse new functionality. Double-gate is the most efficient solution to break the 10 nm barrier, gain speed, and save energy. DG MOSFETs will probably be planar, extremely thin—for volume inversion—and fabricated with a bonding technology. Ultrathin SOI will continue to be a material of choice for conceiving new devices. Minimum-volume MOSFETs, SETs, quantum wires, and dots built in SOI will pave the transition from microelectronics to nanoelectronics.

ACKNOWLEDGMENT

Part of this work was performed at the Center for Advanced Projects in Microelectronics (CPMA, Grenoble), a multi-project institute operated by CNRS, LETI/CEA-Grenoble and universities.

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