

FABRICATION OF CMOS ON ULTRATHIN SOI OBTAINED BY EPITAXIAL LATERAL OVERGROWTH AND CHEMICAL-MECHANICAL POLISHING

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ABSTRACT

A new method to obtain ultra-thin, defect free silicon on insulator (SOI) film is introduced. This technique uses epitaxial lateral overgrowth of Si (ELO) [1, 2] and chemical-mechanical polishing (CMP) [3]. SOI films with thickness of 100 nm were obtained controllably. These films were used in fabrication of dual poly CMOS devices. The quality of the SOI film obtained is same as bulk silicon, and the device characteristics are comparable with that fabricated on bulk. Minimum geometry unloaded inverter ring oscillator on SOI film obtained by ELO and CMP had shown speed improvement of $3\times$ over the bulk devices.

INTRODUCTION

Silicon on insulator has attracted considerable attention recently as the substrate for CMOS devices. The primary attractions of SOI are resistance to soft error and elimination of parasitic capacitances. SIMOX, recrystallization of silicon over oxide, wafer bonding, and lateral epitaxial overgrowth are among the techniques used to obtain SOI films. The important issues in all these methods are the film quality, defect density, final thickness, and thickness control. Among these techniques, ELO can result in epitaxial quality film of Si over SiO_2 . The drawback has been the unacceptable surface topography, which makes the subsequent processing very difficult. We have combined the ELO with chemical-mechanical polishing to obtain thin planar SOI films. These films are defect free, except where the two epitaxial fronts meet each other: A defect line is formed between the two epitaxial fronts at the Si-SiO₂ interface. By proper mask design, these defect lines were placed in the non-critical device areas (i.e. contact) and thus avoided. These films were used in fabrication of dual poly CMOS process. Excellent device and inverter circuit characteristics were obtained.

SOI FILM FABRICATION

To obtain ultra-thin SOI films using ELO and CMP, first

an insulator oxide ($0.3\text{ }\mu\text{m}$) is grown and polish-stop film is formed (Fig. 1a). The polishing process is halted when the polish pad reaches the polish-stop film. The SOI film thickness is determined by the polish-stop film thickness. Large areas (for formation of SOI) are etched in the polish-stop film. Next narrow lines are opened in the exposed oxide to act as seed area for selective epitaxial silicon (Fig. 1b). These lines are along $\langle 100 \rangle$ so that defect free film can be obtained by ELO. A few microns of selective silicon is grown using SiCl_4 (Fig. 1c) [4]. The growth initiates in the seed area, grows vertically and laterally over the oxide. Using CMP, the ELO film was planarized and thinned down to about $0.1\text{ }\mu\text{m}$ (Fig. 1d). Areas up to $10\text{ }\mu\text{m}$ width were obtained using this technique. Thickness control of better than $\pm 10\text{ nm}$ over areas as large as a few cm^2 was obtained. A planar TEM of the final polished film is presented in Fig. 2. In the TEM picture, the SOI film, the seed area and the polish stop are shown. The film is defect free, except where the two fronts meet at zero degree. This defect must not lie in active device area (channel region). There is also a dislocation where the two films meet at 45° . Devices which had their channel over the 45° dislo-

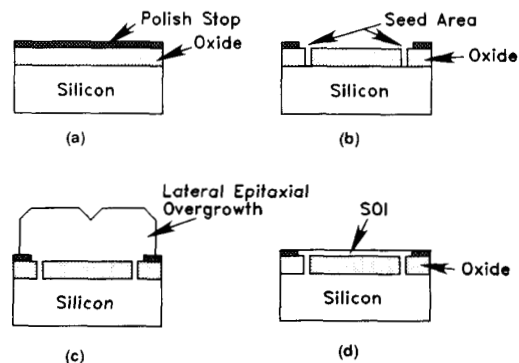


Figure 1: Fabrication sequence for obtaining SOI using epitaxial lateral overgrowth and chemical mechanical polishing.

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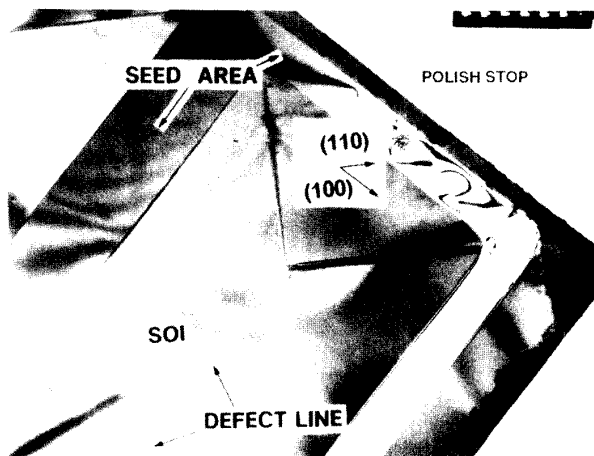


Figure 2: A planar TEM, indicating the quality of the SOI film. The seed area along $\langle 100 \rangle$, SOI film, and polish stop are indicated.

cation, did not show excess subthreshold leakage. To use films obtained by this technique for CMOS processing, the active area of the device (i.e. channel) was placed on the defect free part of the film. This was achieved by proper placement of the seed area and polish stop, as shown in Fig. 3: The seed area must be placed such that the defect line formed is away from the channel, in the contact area. Seed area can be oxidized after the film formation. This can be accomplished by incorporating the seed area in the isolation region. Figure 4 shows a cross sectional TEM of a finished device. The seed area, device poly over the channel, the isolation oxide, and the SOI film are indicated.

DEVICE DESIGN

In order to exploit the maximum potential of SOI, CMOS fabricated on SOI should be fully depleted i.e. the SOI

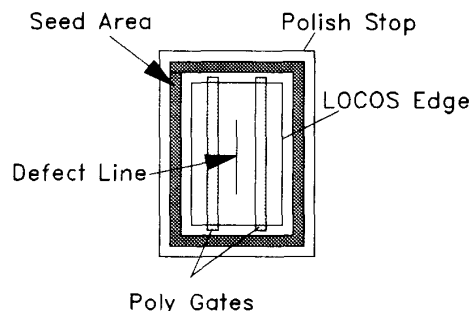


Figure 3: Placement of device channel on SOI to avoid the defect line formed when the two SOI fronts meet. The seed area is in isolation (LOCOS) area.

thickness should be less than the depletion width. The depletion width is set by the background doping and the back bias. If the silicon thickness is less than depletion width, the device threshold can be affected by variations in the film thickness. To find the proper design point, the trade-offs between the SOI film thickness, background concentration and short channel effects were investigated using FIELDAY device simulator [5]. Figure 5 shows the simulated threshold of nMOS device with n^+ poly gate as a function of the SOI doping and thickness. SOI doping must be high enough to control the short channel effects. SOI doping of 10^{17} was chosen for an acceptable short channel behavior at sub- $0.5 \mu\text{m}$ channel length. This sets the threshold of p and n channel devices on fully depleted SOI (with $t_{ox}=7 \text{ nm}$) at about 0.3 V and -0.3 V respectively. Higher doping would reduce the short channel behavior and result in higher V_T , but it would also make V_T a more sensitive function of SOI thickness.

RESULTS

Dual poly process with $t_{ox}=7 \text{ nm}$ and TiSi_2 salicide [6] was used to fabricate submicron CMOS devices on films with

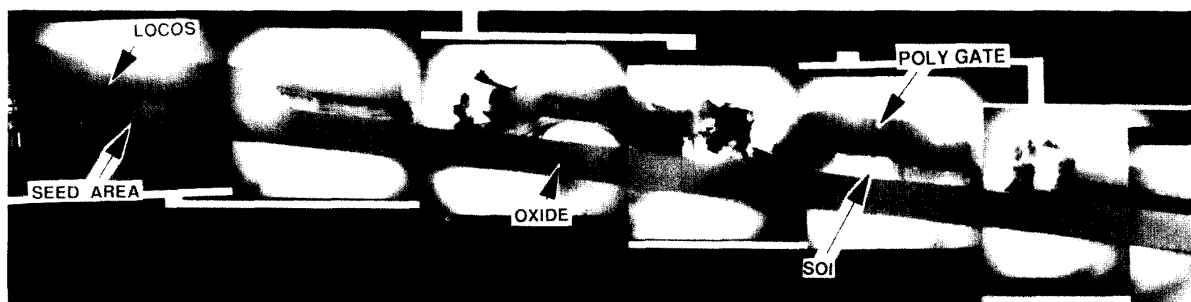


Figure 4: A cross-sectional TEM of CMOS on SOI. Seed area, LOCOS isolation, 150 nm SOI film and, the device poly gate are identified.

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thickness as low as 100 nm. Figure 6 and 7 show device characteristics of both pMOS and nMOS devices with $L_{MASK} = 0.55 \mu\text{m}$ over a 100 nm thick SOI. No back bias was applied. The characteristics are comparable to bulk devices. Source drain implants were As and B implants with abrupt profiles (no LDD). The breakdown voltage of devices on SOI was about one volt less than a comparable device on bulk (The breakdown voltage is about 4 volts for an nMOS of $L_{MASK} = 0.45 \mu\text{m}$). The measured breakdown voltage of devices on SOI with fully overlapped lightly doped drain structure was about one volt higher than the ones with abrupt junctions [7]. Figure 8 is the transconductance of $2 \mu\text{m}$ devices fabricated both on SOI and on bulk devices at low $V_{DS} = 0.1 \text{ V}$: Resulting p- and n-channel mobilities for devices on SOI and bulk Si are very close. Figure 9 shows the behavior of V_T vs. mask channel length. The effective channel length is about $0.15 \mu\text{m}$ shorter than the mask dimension. Symmetric threshold were obtained, without applying any back bias. Figure 10 is an oscilloscope trace of a 61-stage minimum geometry inverter ring oscillator on SOI. It has $L_n/L_p = 0.5/0.6 \mu\text{m}$ (L_{MASK}) $W_n/W_p = 10/20 \mu\text{m}$, and effective diffusion width of $0.8 \mu\text{m}$. At $V_{DD} = 2.5 \text{ V}$, the delay per stage is 33 psec. Figure 11 shows the delays of 1 and $0.5 \mu\text{m}$ ring oscillator on both bulk monitor and SOI film by ELO+CMP. Overall speed improvement of better than 3 was obtained in devices fabricated on SOI over ones made on bulk Si. Part of the improvement in speed is due to elimination of junction capacitances in SOI. The rest of the improvement could be due to current overshoot caused by the parasitic bipolar action of MOSFET during switching [8].

SUMMARY

A new method of obtaining defect free SOI using ELO and CMP is described. Sub- $0.5 \mu\text{m}$ dual poly CMOS devices

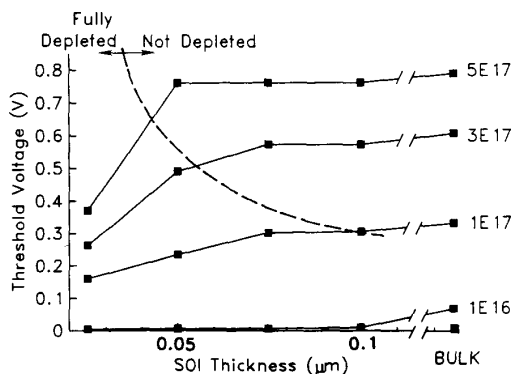


Figure 5: The simulation result showing the threshold voltage as a function of SOI thickness and doping for nMOS with gate oxide of 7 nm.

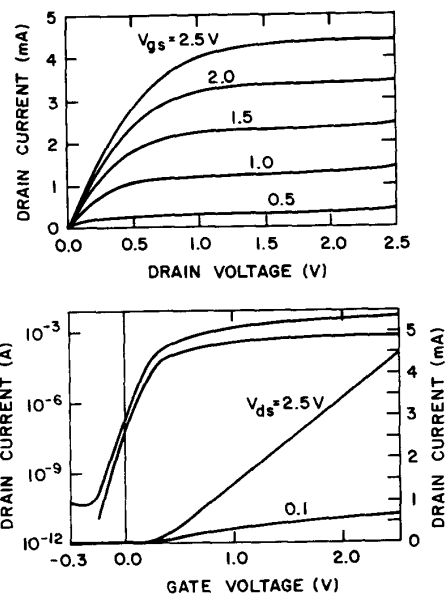


Figure 6: Device characteristics for nMOS with channel length $L_{MASK} = 0.55 \mu\text{m}$.

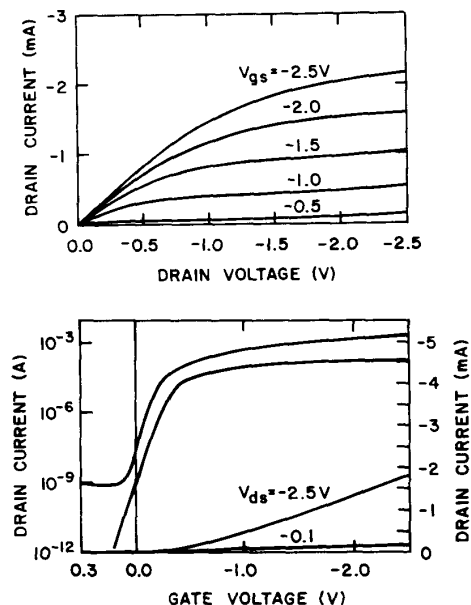


Figure 7: Device characteristics for pMOS with channel length $L_{MASK} = 0.55 \mu\text{m}$.

have been fabricated on these thin SOI films. Film quality is excellent and device characteristics are comparable to devices fabricated on bulk Si. Significant speed improvement has been demonstrated with low parasitic SOI CMOS ring oscillators.

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REFERENCES

- [1] L. Jastrzebski, "SOI by CVD: Epitaxial Lateral Overgrowth (ELO) Process - Review", *J. of Crystal Growth*, 63(1983), 493-526.
- [2] G. B. Bronner *et al.*, "Epitaxy Over Trench Technology for ULSI DRAMs" *Dig. of Tech. Papers, Symp. on VLSI Tech.*, pp. 21, (1988).
- [3] A. C. Bonora, "Silicon Wafer Process Technology: Slicing, Etching and Polishing" *Semiconductor Silicon 1977, Electrochem. Soc.*, Pennington, N.J., pp.154.
- [4] B. Ginzberg *et al.*, "Selective Epitaxial Growth of Silicon", *Extended Abstracts, ECS*, pp. 991, (1987).
- [5] E. M. Buttrula and P. Cottrell, "The FIELDAY Device Simulation Program", *IBM J. of Research and Dev.*, vol. 24, pp. 151, (1978).
- [6] B. Davari *et al.*, "A High performance 0.25 μm CMOS Technology", *IEDM Tech. Digest*, pp. 56, (1988).
- [7] T. Hori *et al.*, "A New Submicron MOSFET with LATID (Large Tilt Angle Implanted Drain) Structure", *Dig. of Tech. Papers, Symp. on VLSI Tech.*, pp. 15, (1988).
- [8] M. Yoshimi *et al.*, "Two-Dimensional Simulation and Measurement of High Performance MOSFET's Made on a Very Thin SOI Film" *IEEE Tran. On Elec. Dev.*, Vol. 36(3), pp 493 (1989).

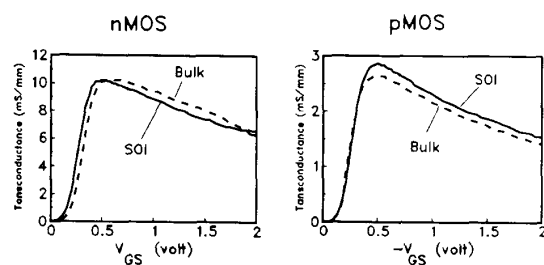


Figure 8: Transconductance of a $L_{M4SA}=2$, $W_{M4SA}=10$ μm nMOS and pMOS device fabricated on SOI and bulk wafer at $V_{DS}=0.1$ V.

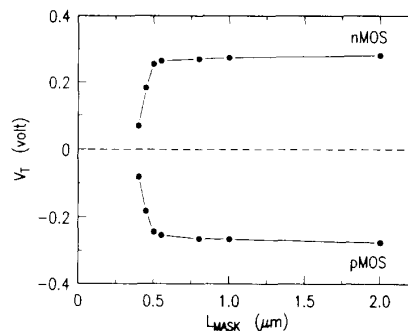


Figure 9: Threshold roll-off for both pMOS and nMOS.

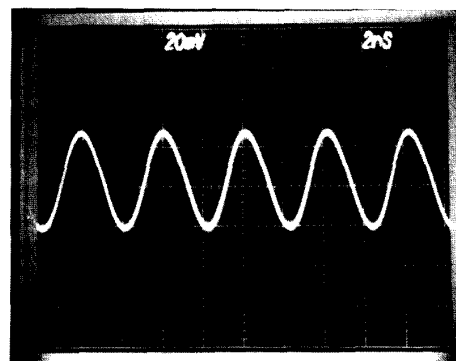


Figure 10: Oscilloscope trace of an unloaded inverter ring oscillator on 100 nm SOI at $V_{DD}=2.5$ V [61 stages, $L_n/L_p=0.5/0.6$ μm (L_{M4SA}), $W_n/W_p=10/20$ μm].

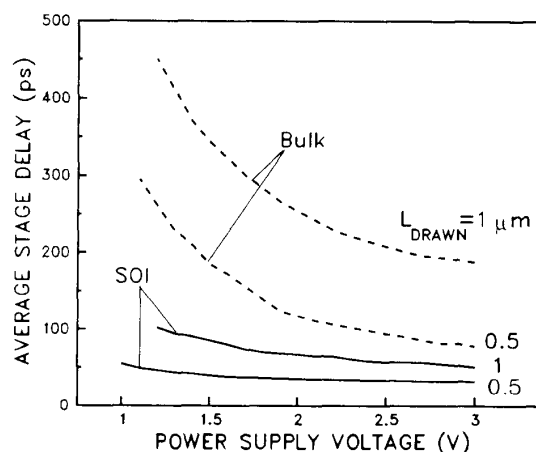


Figure 11: 1 μm and 0.5/0.6 μm channel length inverter ring oscillator delay per stage fabricated on bulk and SOI.

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