FURTHER PROCESSING OF SILICON WAFERS: SIO_2, SI_3N_4, METALLIZATION, EPITAXY AND DICING

The previous chapter described the process steps from quartz sand to silicon wafers manufactured for photolithography. Often, however, prior to the start of the further structuring, the wafers go through certain process steps such as, for example, thermal oxidation or coating with metals or dielectrics as described in this chapter.

Thermal Oxidation

Areas of Application

The electronic (resistivity 10^{14} - 10^{16} ohm cm, dielectric strength 10^6 - 10^7 V/cm, barrier for electrons and holes > 3 eV), mechanical (melting point approx. 1700 °C) and optical (transparent in the visible as well as near infrared and ultraviolet spectral range) properties of SiO_2 make it a suitable material for a multiple range of use:

As dielectric film in transistors, capacitors (DRAM) or flash-memories, as a hard mask for diffusion, implantation, wet or dry chemical etching; and generally as an isolator between integrated devices, or as an anti-reflective layer on e.g. solar cells.

Required SiO_2 film thicknesses range from a few nm (gate-oxide of state-of-the-art CMOS transistors) up to several µm for electrical insulation between components.

Oxidation Technique

Compared to (crystalline) quartz, native (= few nm grown at room temperature in air) and thermal (growth temperature 800 - 1200°C) silicon dioxide (schema of an oxidation Fig. 24) is amorphous (= without long-range atomic lattice order).

The silicon in native or thermally grown SiO_2 evolves from the Si substrate, which is partially consumed during SiO_2 growth: The growth of 100 nm SiO_2 requires approx. 46 nm Si, while the total wafer thickness simultaneously increases by approx. 54 nm.

A distinction is made between *dry oxide* ($Si + O_2 \rightarrow SiO_2$) and - with H_2O as a process gas - *wet oxide* ($Si + 2\ H_2O \rightarrow SiO_2 + 2\ H_2$). At the same process parameters, due to the higher growth rate, wet oxide reveals a higher porosity and HF etch rate.

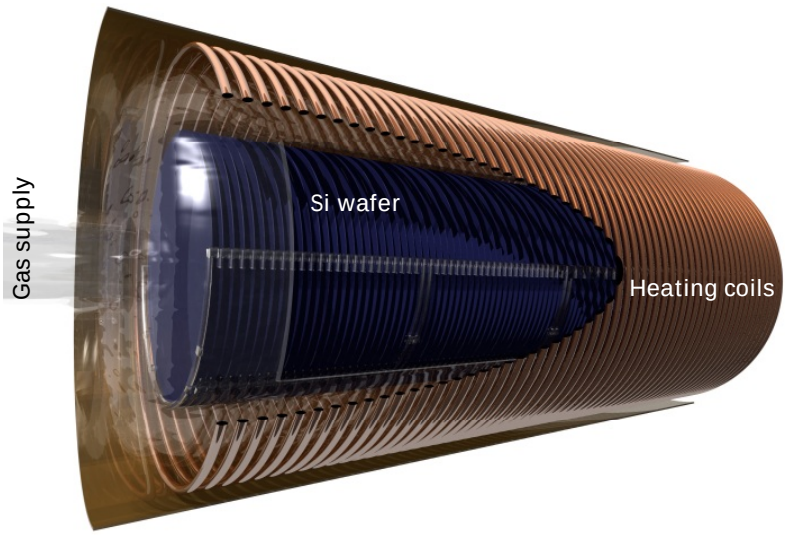


Fig. 24: Diagram of an oxidation furnace for Si wafers

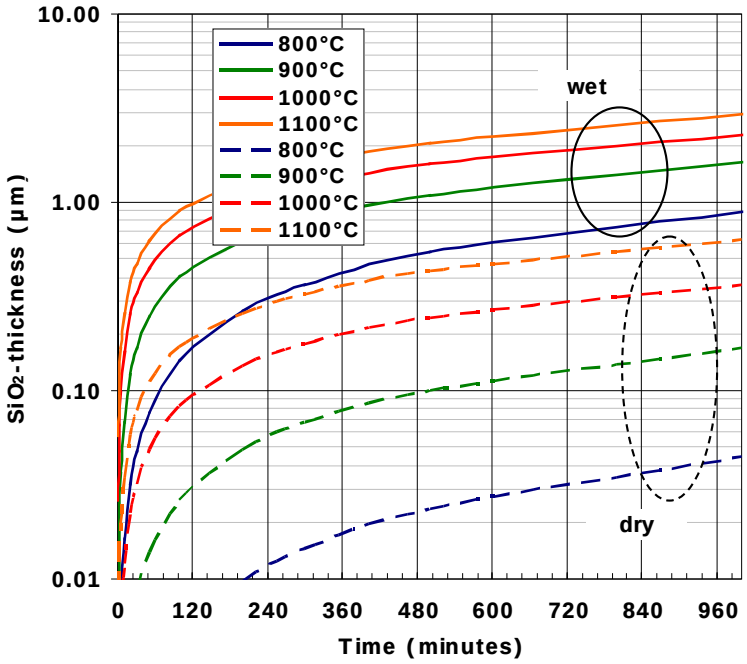


Fig. 25: The attained film thicknesses of wet and dry (dashed) SiO_2 as a function of the SiO_2 growth time and temperature.

Oxidation Rate and Attainable SiO_2 Film Thickness

At the beginning of thermal SiO_2 growth, the chemical reactions on the surface/interface limit the film thickness which increases linearly with time. With the SiO_2 thickness increasing, the more and more dominating oxygen diffusion through the already-grown film towards the Si/SiO_2 interface limits the growth rate. The SiO_2 thickness now increases with the square-root of growth time.

Besides the process gas composition (O_2/H_2O), their partial pressure as well as the substrate temperature (activation energy of oxygen diffusion and chemical reaction at the Si/SiO_2 interface), the SiO_2 growth rate also depends on the Si substrate crystal orientation, mechanical strain of the substrate (e.g. in case of already processed device layers), as well as on substrate doping (e.g. faster oxide growth on phosphorous doped silicon).

PECVD of SiO_2

Mechanism

As an alternative to thermal oxidation of silicon, SiO_2 layers can also be deposited on silicon from the gas phase (PECVD = *Plasma Enhanced Chemical Vapour Deposition*) via

$$SiH_4 + 2\ N_2O \rightarrow SiO_2 + 2\ N_2.$$

Advantages over Thermal SiO_2

Since the film thickness during the PECVD deposition increases linearly over time, very thick layers consisting of several µm can be grown significantly faster than via thermal oxidation. If only a few wafers are to be coated, the PECVD deposition is more favourable than the thermal oxidation process, where larger numbers (e.g. 100 wafers) can be processed simultaneously.

Thermal SiO_2 always contains the impurities (dopants) of the silicon substrate, while the composition of SiO_2 layers grown by PECVD is independent of the substrate.

Disadvantages over Thermal SiO_2

PECVD SiO_2 grows more amorphously with lots of pinholes than a thermal oxide, affecting the electrical and chemical properties:

Compared to thermal SiO_2, PECVD SiO_2 has a lower electrical breakdown strength, which is why the gate oxides, which are, in some cases, only a few nm thick, are preferably produced thermally.

The wet chemical etching rate of PECVD SiO_2 is also significantly higher than that of thermal oxide, which is why it is not well suitable as an etching mask, for example, for anisotropic Si etching.

Deposition of Silicon Nitride

Use of Silicon Nitride

In the field of toolmaking, stoichiometric silicon nitride (Si_3N_4) with its very high mechanical and thermal stability is used for tools such as roller bearings used under harsh conditions. For semiconductor devices, the chemical, electrical and optical properties of amorphous hydrogenated silicon nitride (SiN_x) make this material well-suited for different applications, such as for passivation or insulating layers in integrated circuits masking or etch stop material in wet and plasma etching processes due to its high chemical stability masking material in silicon oxidation processes due to the very low oxygen diffusion coefficient in SiN_x anti-reflective coating in photovoltaics due to its adjustable refractive index.

PECVD Silicon Nitride

The amorphous silicon nitride (SiN_x) deposited using PECVD (*Plasma Enhanced Chemical Vapour Deposition*) from SiH_4 and NH_3, depending on the deposition temperature and gas composition, typically contains 5 - 20 atom% hydrogen (thus sometimes called SiN_x:H) which saturates dangling bonds and thus chemically and mechanically stabilises the SiN_x lattice.

SiN_x can be etched via photoresist masks either with buffered or unbuffered HF or (selectively to SiO_2) with hot concentrated phosphoric acid. The HF etch rate of SiN_x depends on the SiN_x deposition temperature and its refractive index.

A hydrogen-rich SiN_x film deposited at 100°C with a refractive index of n = 1.9 shows an etch rate of several 100 nm/min in buffered HF (12.5 % HF). The etch rate drops to less than 10 nm/min for SiN_x films deposited at 400°C with a refractive index of n = 2.

LPCVD Silicon Nitride

LPCVD (*Low Pressure Chemical Vapour Deposition*) Silicon nitride is deposited via

$$3\ SiH_2Cl_2 + 4\ NH_3 \rightarrow Si_3N_4 + 6\ HCl + 6\ H_2$$

at significantly higher temperatures of around 700 - 850°C compared with the PECVD deposition. As a result, the layer is significantly lower in hydrogen and more stoichiometric than PECVD nitride and exhibits both very good electrical properties and edge coverage, high thermal stability and a low etching rate in hydrofluoric acid.

The deposition takes place via the sub-steps 1) gas supply of the reactants, 2) physical bonding of the molecules on the surface, 3) chemical bonding on the surface and 4) desorption and removal of the byproducts. The growth rate is limited almost exclusively by the chemical reaction on the growing layer and not by the supply and consumption of the raw materials. Significant depletion of the reactants is not attained by the lower growth rate compared to the PECVD deposition. Therefore many (such as 25 or 50) wafers can be simultaneously processed in the gas stream of a reactor with very high film thickness homogeneity on the wafer surface and from wafer to wafer in a batch.

The deposition can be controlled so that either mechanically and ideally low stress or nearly stoichiometric (SI_3N_4) silicon nitride is produced.

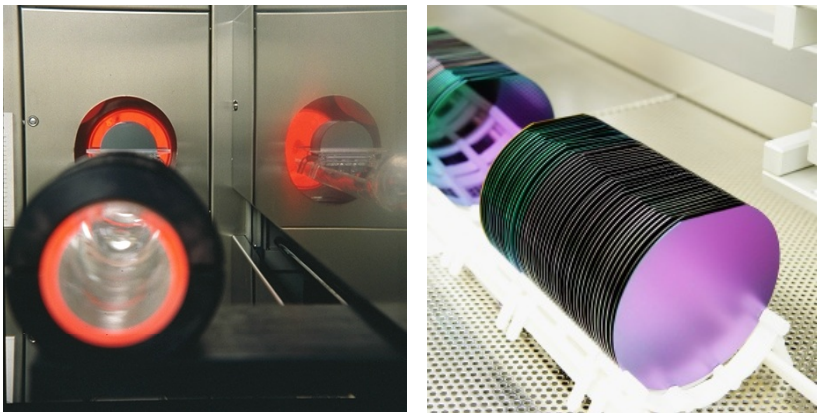


Fig. 26: A LPCVD reactor (left) and Si_3N_4 coated Si wafers (right). Both images kindly provided by IMSAS, University of Bremen.

Material Properties of Silicon Nitride and Silicon Dioxide

Material	Thermal expansion coefficient (10^{-6}/ K)	Refractive index (λ = 600 nm)	Dielectric strength (kV/mm)	Density (g/cm³)
PECVD SiO_2		1.45 - 1.47	600 - 700	
SiO_2 (mono-crystalline)	7.5 - 14	1.54	> 1000	2.65
PECVD SiN_x		> 2.01*	600 - 700	
LPCVD SiN_x		2.01 - 2.05*	> 1000	
SI_3N_4 (mono-crystalline)	3.3	2.01	> 1000	3.29

Table 1: A comparison of the material properties of silicon nitride and silicon oxide

**The refractive index increases with Si-rich deposits*

Metallisation

Surface metallisation of wafers is usually done by thermal evaporation or sputtering. Since the adhesion of many metals to silicon is comparatively poor, it is sometimes advisable to use a 10 - 20 nm chrome or titanium metallic adhesion layer between the substrate and the actual metallisation if the process allows for it. In the case of a subsequent coating of the metal film with photoresist, it should be noted that this usually results in a very poor adhesion on noble metals. Accordingly, a further adhesion layer of 10-20 nm

chromium or titanium film between the noble metal and the resist can make sense.

Epitaxy

Mechanism

In wafer fabrication, silicon epitaxy refers to the growth of a thin layer of single-crystalline silicon onto a single-crystalline silicon substrate, usually via chemical vapour deposition. Commonly used process gases are silicon tetrachloride ($SiCl_4$), dichlorsilan (SiH_2Cl_2), trichlorosilane ($SiHCl_3$) or silane (SiH_4), mixed with hydrogen, which are thermally decomposed to silicon on the surface of wafers heated up to typically 600 - 1000°C. The Si atoms released from the gaseous compounds form mono-crystalline silicon monolayer by monolayer on the silicon substrate.

Application Areas

The addition of dopants such as phosphine, arsine or diborane to the process gas allows the realisation of certain doping profiles in the epitaxial film which is required for, e.g. box-shaped doped structures or a low-doped layer on top of highly doped silicon which cannot be realised by diffusion.

Already realised films such as areas doped via ion implantation, or microelectronic devices can be buried under an epitaxial layer (*buried layer*).

Since the oxygen and carbon impurity concentrations in epitaxial layers are very low, the electronic quality of this film is better than for the silicon substrate underneath, which can be important for integrated devices.

SOI Wafers

Principle

SOI (*Silicon On Insulator*) wafers are wafers with a crystalline silicon film or devices lithographically made from this film located on an electrical insulator such as SiO2. There are two main fields of application for SOI wafers:

Application Areas

Transistors located on an electrically insulating film have a lower capacity and smaller electrical current leakage as compared to transistors directly sitting on the silicon substrate. Therefore, the transistors can be packed more densely, their energy consumption is lower, and the switching speed increased which allows higher clock rates and lower power demand.

In micro-optics, the insulating film allows integrated optical components including waveguides in which µm waves can be guided in silicon (refractive index = 3.5) embedded in SiO_2 (refractive index = 1.5) by total reflection.

Technique

One technique for producing SOI wafers is the SIMOX™ process (*Separation by Implantation of Oxygen*, Fig. 27), starting with oxygen implantation in silicon wafers, which allows an accurate control of the depth profile of the implanted O-atoms (described in more detail in Chapter 29 on page 131). Subsequently, a high temperature step forms the SiO_2 layer where the O-atoms have been captured in the silicon lattice,

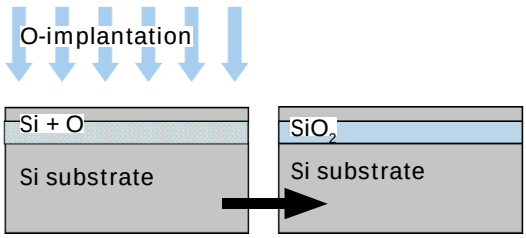


Fig. 27: One technique for producing SOI wafers is the SIMOX™ process (Separation by IMplantation of OXgen)

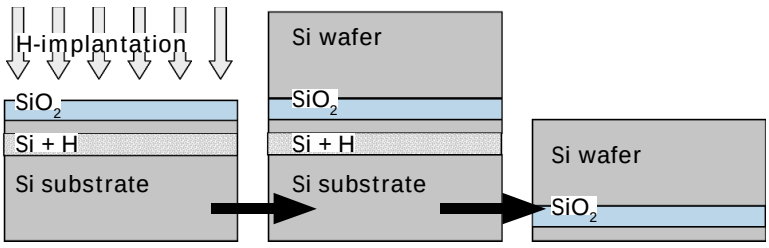


Fig. 28: Another possibility of manufacturing SOI wafers via the *Smart Cut* technique combines hydrogen ion implantation and wafer bonding.

and simultaneously thermally anneals the crystal structure of the silicon above distorted by the implantation process.

The Smart-Cut™ technique (Fig. 28) combines hydrogen ion implantation and wafer bonding. Hydrogen ions are implanted in an oxidized silicon wafer. This wafer is bonded with another wafer without SiO_2 layer, hereby completely and permanently bonded to each other. This wafer bonding is carried out either by high mechanical pressure with the aid of hydrogen bonds and Van der Waals interactions or by means of anodic bonding in which the formation of chemical bonds is induced by applying an electrical voltage to the contact surface of both wafers.

A baking step (> 500°C) splits the oxidized wafer along the depth of the implanted hydrogen atoms induced by mechanical stress.

Dicing of Wafers

Principle

Wafer dicing allows to cut rectangular pieces from circular wafers. Dicing can be accomplished by scribing and breaking, by mechanical sawing (using a blade or wire saw), or by laser cutting. The material of the substrate and the size of the diced pieces are limited less from technical than by economic boundaries: A dicing often only makes sense starting from 25 output wafers due to the relatively high set-up costs.

Realisable Parameters for Isolated Si Wafers Which We Can Supply

Material:	CZ-Si or FZ-Si, optionally with thermal SiO_2
Dimensions:	From 5 x 5 mm to 120 x 100 mm
Wafer thickness:	200 µm - 1 mm
Orientation:	<100> or <111>; <110> on request

Our Photoresists: Application Areas and Compatibilities

	Recommended Applications [1]	Resist Family	Photoresists	Resist Film Thickness [2]	Recommended Developers [3]	Recommended Removers [4]
Positive	Improved adhesion for wet etching, no focus on steep resist sidewalls	AZ® 1500	AZ® 1505 AZ® 1512 HS AZ® 1514 H AZ® 1518	≈ 0.5 µm ≈ 1.0 - 1.5 µm ≈ 1.2 - 2.0 µm ≈ 1.5 - 2.5 µm	AZ® 351B, AZ® 326 MIF, AZ® 726 MIF, AZ® Developer	AZ® 100 Remover, TechniStrip® P1316 TechniStrip® P1331
		AZ® 4500	AZ® 4533 AZ® 4562	≈ 3 - 5 µm ≈ 5 - 10 µm	AZ® 400K, AZ® 326 MIF, AZ® 726 MIF, AZ® 826 MIF	
		AZ® P4000	AZ® P4110 AZ® P4330 AZ® P4620 AZ® P4903	≈ 1 - 2 µm ≈ 3 - 5 µm ≈ 6 - 20 µm ≈ 10 - 30 µm	AZ® 400K, AZ® 326 MIF, AZ® 726 MIF, AZ® 826 MIF	
		AZ® PL 177	AZ® PL 177	≈ 3 - 8 µm	AZ® 351B, AZ® 400K, AZ® 326 MIF, AZ® 726 MIF, AZ® 826 MIF	
	Spray coating	AZ® 4999		≈ 1 - 15 µm	AZ® 400K, AZ® 326 MIF, AZ® 726 MIF, AZ® 826 MIF	
	Dip coating	MC Dip Coating Resist		≈ 2 - 15 µm	AZ® 351B, AZ® 400K, AZ® 326 MIF, AZ® 726 MIF, AZ® 826 MIF	
	Steep resist sidewalls, high resolution and aspect ratio for e. g. dry etching or plating	AZ® ECI 3000	AZ® ECI 3007 AZ® ECI 3012 AZ® ECI 3027	≈ 0.7 µm ≈ 1.0 - 1.5 µm ≈ 2 - 4 µm	AZ® 351B, AZ® 326 MIF, AZ® 726 MIF, AZ® Developer	
		AZ® 9200	AZ® 9245 AZ® 9260	≈ 3 - 6 µm ≈ 5 - 20 µm	AZ® 400K, AZ® 326 MIF, AZ® 726 MIF	
	Elevated thermal softening point and high resolution for e. g. dry etching	AZ® 701 MiR	AZ® 701 MiR (14 cPs) AZ® 701 MiR (29 cPs)	≈ 0.8 µm ≈ 2 - 3 µm	AZ® 351B, AZ® 326 MIF, AZ® 726 MIF, AZ® Developer	
Positive (chem. amplified)	Steep resist sidewalls, high resolution and aspect ratio for e. g. dry etching or plating	AZ® XT	AZ® 12 XT-20PL-05 AZ® 12 XT-20PL-10 AZ® 12 XT-20PL-20 AZ® 40 XT	≈ 3 - 5 µm ≈ 6 - 10 µm ≈ 10 - 30 µm ≈ 15 - 50 µm	AZ® 400K, AZ® 326 MIF, AZ® 726 MIF	AZ® 100 Remover, TechniStrip® P1316 TechniStrip® P1331
		AZ® IPS 6050		≈ 20 - 100 µm		
Image Reversal	Elevated thermal softening point and undercut for lift-off applications	AZ® 5200	AZ® 5209 AZ® 5214	≈ 1 µm ≈ 1 - 2 µm	AZ® 351B, AZ® 326 MIF, AZ® 726 MIF	TechniStrip® Micro D2 TechniStrip® P1316 TechniStrip® P1331
		TI	TI 35ESX TI xLift-X	≈ 3 - 4 µm ≈ 4 - 8 µm		
Negative (Cross-linking)	Negative resist sidewalls in combination with no thermal softening for lift-off application	AZ® nLOF 2000	AZ® nLOF 2020 AZ® nLOF 2035 AZ® nLOF 2070	≈ 1.5 - 3 µm ≈ 3 - 5 µm ≈ 6 - 15 µm	AZ® 326 MIF, AZ® 726 MIF, AZ® 826 MIF	TechniStrip® NI555 TechniStrip® NF52 TechniStrip® MLO 07
		AZ® nLOF 5500	AZ® nLOF 5510	≈ 0.7 - 1.5 µm		
	Improved adhesion, steep resist sidewalls and high aspect ratios for e. g. dry etching or plating	AZ® nXT	AZ® 15 nXT (115 cPs) AZ® 15 nXT (450 cPs)	≈ 2 - 3 µm ≈ 5 - 20 µm	AZ® 326 MIF, AZ® 726 MIF, AZ® 826 MIF	
			AZ® 125 nXT	≈ 20 - 100 µm	AZ® 326 MIF, AZ® 726 MIF, AZ® 826 MIF	TechniStrip® P1316 TechniStrip® P1331 TechniStrip® NF52 TechniStrip® MLO 07

[1] In general, almost all resists can be used for almost any application. However, the special properties of each resist family makes them specially suited for certain fields of application.

[2] Resist film thickness achievable and processable with standard equipment under standard conditions. Some resists can be diluted for lower film thicknesses; with additional effort also thicker resist films can be achieved and processed.

[3] Metal ion free (MIF) developers are significantly more expensive, and reasonable if metal ion free development is required.

Our Developers: Application Areas and Compatibilities

Inorganic Developers

(typical demand under standard conditions approx. 20 L developer per L photoresist)

AZ® Developer is based on sodium phosphate and –metasilicate, is optimized for minimal aluminum attack and is typically used diluted 1 : 1 in DI water for high contrast or undiluted for high development rates. The dark erosion of this developer is slightly higher compared to other developers.

AZ® 351B is based on buffered NaOH and typically used diluted 1 : 4 with water, for thick resists up to 1 : 3 if a lower contrast can be tolerated.

AZ® 400K is based on buffered KOH and typically used diluted 1 : 4 with water, for thick resists up to 1 : 3 if a lower contrast can be tolerated.

AZ® 303 specifically for the AZ® 111 XFS photoresist based on KOH / NaOH is typically diluted 1 : 3 - 1 : 7 with water, depending on whether a high development rate, or a high contrast is required

Metal Ion Free (TMAH-based) Developers

(typical demand under standard conditions approx. 5 - 10 L developer concentrate per L photoresist)

AZ® 326 MIF is 2.38 % TMAH- (TetraMethylAmmoniumHydroxide) in water.

AZ® 726 MIF is 2.38 % TMAH- (TetraMethylAmmoniumHydroxide) in water, with additional surfactants for rapid and uniform wetting of the substrate (e. g. for puddle development)

AZ® 826 MIF is 2.38 % TMAH- (TetraMethylAmmoniumHydroxide) in water, with additional surfactants for rapid and uniform wetting of the substrate (e. g. for puddle development) and other additives for the removal of poorly soluble resist components (residues with specific resist families), however at the expense of a slightly higher dark erosion.

Our Removers: Application Areas and Compatibilities

AZ® 100 Remover is an amine solvent mixture and standard remover for AZ® and TI photoresists. To improve its performance, AZ® 100 remover can be heated to 60 - 80°C. Because the AZ® 100 Remover reacts highly alkaline with water, it is suitable for this with respect to sensitive substrate materials such as Cu, Al or ITO only if contamination with water can be ruled out..

TechniStrip® P1316 is a remover with very strong stripping power for Novolak-based resists (including all AZ® positive resists), epoxy-based coatings, polyimides and dry films. At typical application temperatures around 75°C, TechniStrip® P1316 may dissolve cross-linked resists without residue also, e.g. through dry etching or ion implantation. TechniStrip® P1316 can also be used in spraying processes. For alkaline sensitive materials, TechniStrip® P1331 would be an alternative to the P1316. Nicht kompatibel mit Au oder GaAs.

TechniStrip® P1331 can be an alternative for TechniStrip® P1316 in case of alkaline sensitive materials. TechniStrip® P1331 is not compatible with Au or GaAs.

TechniStrip® NI555 is a stripper with very strong dissolving power for Novolak-based negative resists such as the AZ® 15 nXT and AZ® nLOF 2000 series and very thick positive resists such as the AZ® 40 XT. TechniStrip® NI555 was developed not only to peel cross-linked resists, but also to dissolve them without residues. This prevents contamination of the basin and filter by resist particles and skins, as can occur with standard strippers. TechniStrip® NI555 is not compatible with Au or GaAs.

TechniClean™ CA25 is a semi-aqueous proprietary blend formulated to address post etch residue (PER) removal for all interconnect and technology nodes. Extremely efficient at quickly and selectively removing organo-metal oxides from Al, Cu, Ti, TiN, W and Ni.

TechniStrip™ NF52 is a highly effective remover for negative resists (liquid resists as well as dry films). The intrinsic nature of the additives and solvent make the blend totally compatible with metals used throughout the BEOL interconnects to WLP bumping applications.

TechniStrip™ Micro D2 is a versatile stripper dedicated to address resin lift-off and dissolution on negative and positive tone resist. The organic mixture blend has the particularity to offer high metal and material compatibility allowing to be used on all stacks and particularly on fragile III/V substrates for instance.

TechniStrip™ MLO 07 is a highly efficient positive and negative tone photoresist remover used for IR, III/V, MEMS, Photonic, TSV mask, solder bumping and hard disk stripping applications. Developed to address high dissolution performance and high material compatibility on Cu, Al, Sn/Ag, Alumina and common organic substrates.

Our Wafers and their Specifications

Silicon-, Quartz-, Fused Silica and Glass Wafers

Silicon wafers are either produced via the Czochralski- (CZ-) or Float zone- (FZ-) method. The more expensive FZ wafers are primarily reasonable if very high-ohmic wafers (> 100 Ohm cm) are required.

Quartz wafers are made of monocrystalline SiO_2, main criterion is the crystal orientation (e. g. X-, Y-, Z-, AT- or ST-cut)

Fused silica wafers consist of amorphous SiO_2. The so-called JGS2 wafers have a high transmission in the range of ≈ 280 - 2000 nm wavelength, the more expensive JGS1 wafers at ≈ 220 - 1100 nm.

Our glass wafers, if not otherwise specified, are made of borosilicate glass.

Specifications

Common parameters for all wafers are diameter, thickness and surface (1- or 2-side polished). Fused silica wafers are made either of JGS1 or JGS2 material, for quartz wafers the crystal orientation needs to be defined. For silicon wafers, beside the crystal orientation (<100> or <111>) the doping (n- or p-type) as well as the resistivity (Ohm cm) are selection criteria.

Prime- ,Test-, and Dummy Wafers

Silicon wafers usually come as „Prime-grade“ or „Test-grade“, latter mainly have a slightly broader particle specification. „Dummy-Wafers“ neither fulfill Prime- nor Test-grade for different possible reasons (e. g. very broad or missing specification of one or several parameters, reclaim wafers, no particle specification) but might be a cheap alternative for e. g. resist coating tests or equipment start-up.

Our Silicon-, Quartz-, Fused Silica and Glass Wafers

Our frequently updated wafer stock list can be found here: **è** www.microchemicals.com/products/wafers/waferlist.html

Further Products from our Portfolio

Plating

Plating solutions for e. g. gold, copper, nickel, tin or palladium: **è** www.microchemicals.com/products/electroplating.html

Solvents (MOS, VLSI, ULSI)

Acetone, isopropyl alcohol, MEK, DMSO, cyclopentanone, butylacetate, ... **è** www.microchemicals.com/products/solvents.html

Acids and Bases (MOS, VLSI, ULSI)

Hydrochloric acid, sulphuric acid, nitric acid, KOH, TMAH, … **è** www.microchemicals.com/products/etchants.html

Etching Mixtures

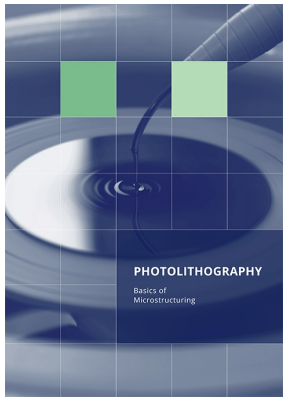
for e. g. chromium, gold, silicon, copper, titanium, ... **è** www.microchemicals.com/products/etching_mixtures.html

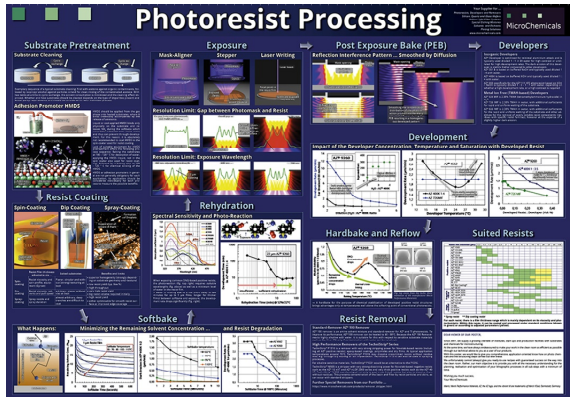
Further Information

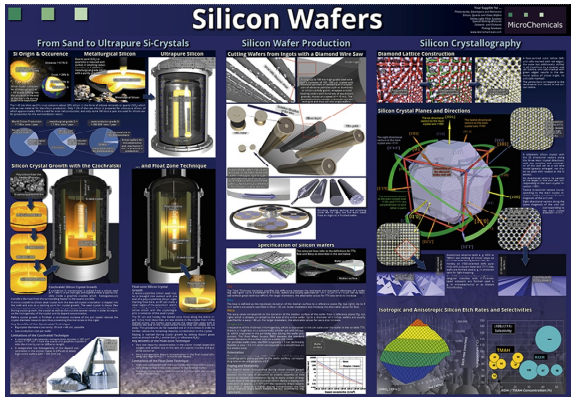
Technical Data Sheets: www.microchemicals.com/downloads/product_data_sheets/photoresists.html

Material Safety Data Sheets (MSDS): www.microchemicals.com/downloads/safety_data_sheets/msds_links.html

Our Photolithography Book and -Posters







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The safe sequence of mixing components of a recipe usually does not correspond to the order of their listing. We do not warrant the full disclosure of any indications (among other things, health, work safety) of the risks associated with the preparation and use of the recipes and processes. The information in this book is based on our current knowledge and experience. Due to the abundance of possible influences in the processing and application of our products, they do not exempt the user from their own tests and trials. A guarantee of certain properties or suitability for a specific application can not be derived from our data. As a matter of principle, each employee is required to provide sufficient information in advance in the appropriate cases in order to prevent damage to persons and equipment. All descriptions, illustrations, data, conditions, weights, etc. can be changed without prior notice and do not constitute a contractually agreed product characteristics. The user of our products is responsible for any proprietary rights and existing laws.

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