UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
MICRON SEMICONDUCTOR PRODUCTS, INC., and
MICRON TECHNOLOGY TEXAS, LLC,
Petitioner

v.

BESANG INC.,
Patent Owner.

Case No. IPR2023-00900
U.S. Patent No. 7,378,702

DECLARATION OF DR. JACK C. LEE IN SUPPORT OF PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 7,378,702

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3. Element 13[b]: a stackable add-on layer having a plurality of vertically oriented semiconductor memory cells; and 71

4. Element 13[c]: the stackable add-on layer being bonded to the dielectric layer; and 73

5. Element 13[d]: wherein the memory cells are nonvolatile memory cells having at least one transistor. 76

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LIST OF EXHIBITS[1]

Ex-1001	U.S. Patent No. 7,378,702 ("the '702 Patent")
Ex-1002	Declaration of Dr. Jack C. Lee
Ex-1003	Curriculum Vitae of Dr. Jack C. Lee
Ex-1004	Prosecution History of U.S. Patent No. 7,378,702 (App. No. 10/934,270)
Ex-1005	U.S. Patent No. 5,091,762 ("Watanabe")
Ex-1006	U.S. Patent Application Pub. No. US2002/0154556 ("Endoh")
Ex-1007	U.S. Patent No. 6,881,994 ("Lee")
Ex-1008	U.S. Patent No. 7,221,008 ("Matamis")
Ex-1009	G. Groeseneken et al., *Basics of Nonvolatile Semiconductor Memory Devices*, in *Nonvolatile Semiconductor Memory Technology: A Comprehensive Guide to Understanding and Using NVSM Devices* (William D. Brown & Joe Brewer eds., 1997)
Ex-1010	Philip M. Sailer et al., *Creating 3D Circuits Using Transferred Films*, IEEE Circuits & Devices (1997)
Ex-1011	U.S. Patent No. 5,808,938 ("Tran")
Ex-1012	U.S. Patent No. 6,982,905 ("Nguyen")
Ex-1013	U.S. Patent No. 6,807,098 ("Jeong")
Ex-1014	Kee-Ho Yu et al., *Real-Time Microvision System with Three-Dimensional Integration Structure*, IEEE Int'l Conference on Multisensor Fusion and Integration for Intelligent Sys. (1996)
Ex-1015	U.S. Patent No. 5,374,564 ("Bruel")
Ex-1016	Horacio Mendez, *Silicon-on-Insulator: SOI Technology and Ecosystem – Emerging SOI Applications*, SOI Indus. Consortium (2009)
Ex-1017	U.S. District Courts – Combined Civil and Criminal Federal Court Management Statistics (Dec. 31, 2022), available at: https://www.uscourts.gov/statistics-reports/federal-court-management-statistics-december-2022

[1] Four-digit pin citations that begin with 0 are the page stamps added by Samsung in the bottom right corner of the exhibits. All other pin citations are to original page, column, paragraph, or line numbers.

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Ex-1018	T. Mikolajick et al., *The Future of Charge Trapping Memories*, 2007 IEEE Int'l Symposium on VLSI Tech., Sys. & Applications (2007)
Ex-1019	Complaint, *BeSang Inc. v. Micron Tech., Inc.*, No. 2:23-cv-00028 (E.D. Tex. Jan. 23, 2023)
Ex-1020	Jim Handy, *3D NAND: Benefits of Charge Traps over Floating Gates*, The Memory Guy Blog (Nov. 22, 2013)
Ex-1021	E. Bertagnolli et al., *ROS: An Extremely High Density MASK ROM Technology Based on Vertical Transistor Cells*, IEEE (1996)
Ex-1022	Tetsuo Endoh et al., *Novel Ultrahigh-Density Flash memory with A Stacked-Surrounding Gate Transistor (S-SGT) Structured Cell*, 50 IEEE Transactions on Electron Devices 945 (2003)
Ex-1023	F. Nemati & J.D. Plummer, *A Novel High Density, Low Voltage SRAM Cell with A Vertical NDR Device*, IEEE (1998)
Ex-1024	K.W. Lee et al., *Three-Dimensional Shared Memory Fabricated Using Wafer Stacking Technology*, IEEE (2000)
Ex-1025	*NAND vs. NOR Flash Memory*, Toshiba America Electronic Components, Inc. (2006)
Ex-1026	G.K. Celler & Sorin Crisoloveanu, *Frontiers of Silicon-on-Insulator*, 93 J. Applied Physics 4955 (2003)
Ex-1027	Timeline, Soitec, available at: https://www.soitec.com/en/company/soitec-activity/history (last visited Apr. 25, 2023)
Ex-1028	G. Shahidi et al., *Fabrication of CMOS on Ultrathin SOI Obtained by Epitaxial Lateral Overgrowth and Chemical-Mechanical Polishing*, IEEE (1991)
Ex-1029	MicroChemicals, *Further Processing of Silicon Wafers:* SiO_2, Si_3N_4, *Metallization, Epitaxy and Dicing*, available at: https://www.microchemicals.com/technical_information/silicon_wafer_sio2_si3n4_metallization_epitaxy_soi.pdf (last visited Apr. 28, 2023)
Ex-1030	Hiroshi Sakuraba et al., *New Three-Dimensional High-Density Stacked-Surrounding Gate Transistor (S-SGT) Flash Memory Architecture Using Self-Aligned Interconnection Fabrication Technology Without Photolithography Process for Tera-Bits and Beyond*, 43 Japanese J. Applied Physics 2217 (2004)

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I, Jack C. Lee, declare as follows:

I. INTRODUCTION

1. I am an expert in the field of semiconductor process technology and semiconductor design. I have over 40 years of first-hand experience as a researcher, educator, and consultant in this field.

2. I have been retained by Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas, LLC ("Petitioner") as a technical expert witness in connection with the petition for *inter partes* review ("IPR") of U.S. Patent No. 7,378,702 (Ex-1001 or "the '702 Patent"). I have been informed by counsel that Patent Owner may allege that the priority date for the '702 patent is June 21, 2004. For purposes of my analysis herein, I have used this date as the relevant time period.

3. I have been asked by counsels for Petitioner to offer opinions regarding the '702 patent, which I understand is allegedly owned by BeSang Inc. ("Patent Owner"), including the patentability of Claims 13-17 ("the Challenged Claims") in view of certain prior art references and the knowledge of a person of ordinary skill in the art ("POSITA"), at the time of the alleged invention. It is my opinion that the Challenged Claims would have been obvious to a POSITA. My opinions and the bases for my opinions are set forth below.

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4. I am being compensated for my time in this matter at an hourly rate. I am also being reimbursed for reasonable and customary expenses associated with my work and testimony in this matter. My compensation is not contingent on the outcome of this matter or the specifics of my testimony. I have no personal or financial stake or interest in the outcome of the present proceeding.

5. I have no financial interest in Petitioner or any of its subsidiaries. I do not have any financial interest in the '702 Patent and have not had any contact with any of the named inventors of the '702 Patent.

6. Additional details about my employment history, fields of expertise, awards, publications, and other activities are further included in my curriculum vitae, attached as Ex-1003.

II. BACKGROUND AND QUALIFICATIONS

7. My qualifications for forming the opinions set forth in this Declaration are summarized here and explained in more detail in my curriculum vitae, which is attached as Ex-1003.

8. I received a B.S. degree in Electrical Engineering, with highest honors, in 1980, and an M.S. degree in Electrical Engineering in 1981, both from University of California, Los Angeles. I received a Ph.D. degree in Electrical Engineering in 1988 from University of California, Berkeley ("UC Berkeley").

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9. From 1979 to 1984, I was a Member of Technical Staff at the TRW Microelectronics Center, in the High-Speed Bipolar Device Program. I worked on bipolar device/circuit design, fabrication, and testing. I was promoted to Engineering Group Leader level in 1983.

10. I received several academic honors while at UC Berkeley. For example, I won the Best Paper Award from the Institute of Electrical and Electronics Engineers ("IEEE") International Reliability Physics Symposium in 1988. I was also awarded a Lectureship with my own teaching assistant from UC Berkeley.

11. After receiving my Ph.D. in August 1988, I joined the faculty at The University of Texas at Austin ("UT Austin"). As a faculty member, I have taught numerous courses in semiconductor device fabrication and design, at both the undergraduate and graduate levels. I have supervised over 40 students who received their doctoral degrees under my guidance. I am currently the Cullen Trust for Higher Education Endowed Professor in Engineering in the Department of Electrical and Computer Engineering at UT Austin.

12. My current research and teaching interests include semiconductor devices, semiconductor memory applications, fabrication processes, silicon-on-insulator technologies, electrical and material characterization, reliability and modeling, packaging technologies, dielectric and passivation processes, display

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technologies, photovoltaic and solar cell technologies, high-K gate dielectrics and electrode, and alternative channel materials. My research has been partially supported by grants from the National Science Foundation, the Texas Advanced Research Program, the Semiconductor Research Corporation (SRC), SEMATECH, Texas Emerging Technology Funds, and others.

13. I have authored over 600 journal publications and conference proceeding papers and have coauthored 8 books and book chapters on semiconductor technologies. I am a named inventor of 9 U.S. patents. I have also received numerous teaching and research awards, e.g., inventor recognition and best paper awards.

14. In 2002, I became an IEEE fellow for my "contributions to the understanding and development of ultra-thin dielectrics and their application to silicon devices." I was also an IEEE Electron Devices Society Distinguished Lecturer from 2004 to 2016.

15. I have served in various technology consulting and business advisor roles. For example, I have taught short courses on semiconductor device physics and technologies at various semiconductor companies and consortiums (e.g., SEMATECH). I have also organized several international conferences and have given lectures at numerous conferences and symposia, including the International Symposium on VLSI Technologies, the IEEE Symposia on VLSI Technology, and

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the IEEE International Electron Devices Meeting. These conferences are some of the most prestigious in the field.

III. INFORMATION CONSIDERED

16. In preparation for this declaration, I have considered the materials discussed in this declaration, including, for example, the '702 Patent, the references cited by the '702 Patent, the prosecution history of the '702 Patent and applications from which it derives (including the references cited therein), various background articles and materials referenced in this declaration, and the prior art references identified in this declaration.

17. In forming the opinions expressed below, I have considered: the documents listed above, any additional documents discussed below, and my education, training, experience, and knowledge in the relevant field of semiconductor technology.

IV. RELEVANT LEGAL STANDARDS

18. I am not an attorney and offer no legal opinions. For the purposes of this Declaration, I have been informed about certain aspects of the law that are relevant to my analysis, as summarized below.

A. Claim Interpretation

19. I have been informed and understand that in an IPR proceeding, claims are to be interpreted according to the *Phillips* claim construction standard. I have been informed and understand that claim construction is a matter of law and

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that the final claim constructions for this proceeding will be determined by the Patent Trial and Appeal Board ("PTAB").

B. Written Description

20. I understand that determining whether a particular patent or printed publication constitutes prior art to a challenged patent claim can require determining the effective filing date (also known as the priority date) to which the challenged claim is entitled. I understand that for a patent claim to be entitled to the benefit of the filing date of an earlier application to which the patent claims priority, the earlier application must have described the claimed invention in sufficient detail to convey with reasonable clarity to the POSITA that the inventor had possession of the claimed invention as of the earlier application's filing date. I understand that a disclosure that merely renders the claimed invention obvious is not sufficient written description for the claim to be entitled to the benefit of the filing date of the application containing that disclosure.

C. Perspective of One of Ordinary Skill in the Art

21. I have been informed and understand that a patent is to be understood from the perspective of a hypothetical "person of ordinary skill in the art" ("POSITA"). Such an individual is considered to possess normal skills and knowledge in a particular technical field (as opposed to being a genius). I understand that in considering what the claims of a patent require, what was known

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prior to that patent, what a prior art reference discloses, and whether an invention is obvious or not, one must use the perspective of such a POSITA.

D. Obviousness

22. I have been informed and understand that a patent claim is obvious under 35 U.S.C. § 103, and therefore invalid, if the claimed subject matter, as a whole, would have been obvious to a POSITA as of the priority date of the patent based on one or more prior art references and/or the knowledge of a POSITA.

23. I understand that an obviousness analysis must consider (1) the scope and content of the prior art, (2) the differences between the claims and the prior art, (3) the level of ordinary skill in the pertinent art, and (4) secondary considerations, if any, of non-obviousness (such as unexpected results, commercial success, long-felt but unmet need, failure of others, copying by others, and skepticism of experts).

24. I understand that a prior art reference may be combined with other references to disclose each element of the invention under 35 U.S.C. § 103. I understand that a reference may also be combined with the knowledge of a POSITA, and that this knowledge may be used to combine multiple references. I further understand that a POSITA is presumed to know the relevant prior art. I understand that the obviousness analysis may take into account the inferences and creative steps that a POSITA would employ.

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25. In determining whether a prior art reference would have been combined with other prior art or other information known to a POSITA, I understand that the following principles may be considered:

- whether the references to be combined involve non-analogous art;
- whether the references to be combined are in different fields of endeavor than the alleged invention in the Patent;
- whether the references to be combined are reasonably pertinent to the problems to which the inventions of the Patent are directed;
- whether the combination is of familiar elements according to known methods that yields predictable results;
- whether a combination involves the substitution of one known element for another that yields predictable results;
- whether the combination involves the use of a known technique to improve similar items or methods in the same way that yields predictable results;
- whether the combination involves the application of a known technique to a prior art reference that is ready for improvement, to yield predictable results;
- whether the combination is "obvious to try";
- whether the combination involves the known work in one field of endeavor prompting variations of it for use in either the same field or a different one

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based on design incentives or other market forces, where the variations are predictable to a POSITA;

- whether there is some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill in the art to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention;
- whether the combination requires modifications that render the prior art unsatisfactory for its intended use;
- whether the combination requires modifications that change the principle of operation of the reference;
- whether the combination is reasonably expected to be a success; and
- whether the combination possesses the requisite degree of predictability at the time the invention was made.

26. I understand that in determining whether a combination of prior art references renders a claim obvious, it is helpful to consider whether there is some teaching, suggestion, or motivation to combine the references and a reasonable expectation of success in doing so. I understand, however, that a teaching, suggestion, or motivation to combine is not required.

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V. RELIEF REQUESTED

27. For purposes of this proceeding only, Petitioner assumes that the '702 Patent is entitled to its earliest alleged domestic priority date, June 21, 2004, and thus applies pre-AIA 35 U.S.C. § 102.

28. It is my opinion that Claims 13-17 of the '702 Patent would have been obvious under 35 U.S.C. § 103 on the following grounds:

Ground	Summary
1	Claim 13 is obvious over Watanabe (Ex-1005).
2	Claims 14-17 are obvious over Watanabe in view of Endoh (Ex-1006).
3	Claims 13-15 are obvious over Lee (Ex-1007).
4	Claims 16 and 17 are obvious over Lee in view of Endoh.
5	Claims 13-15 are obvious over Lee in view of Watanabe.
6	Claims 16 and 17 are obvious over Lee in view of Watanabe and Endoh.

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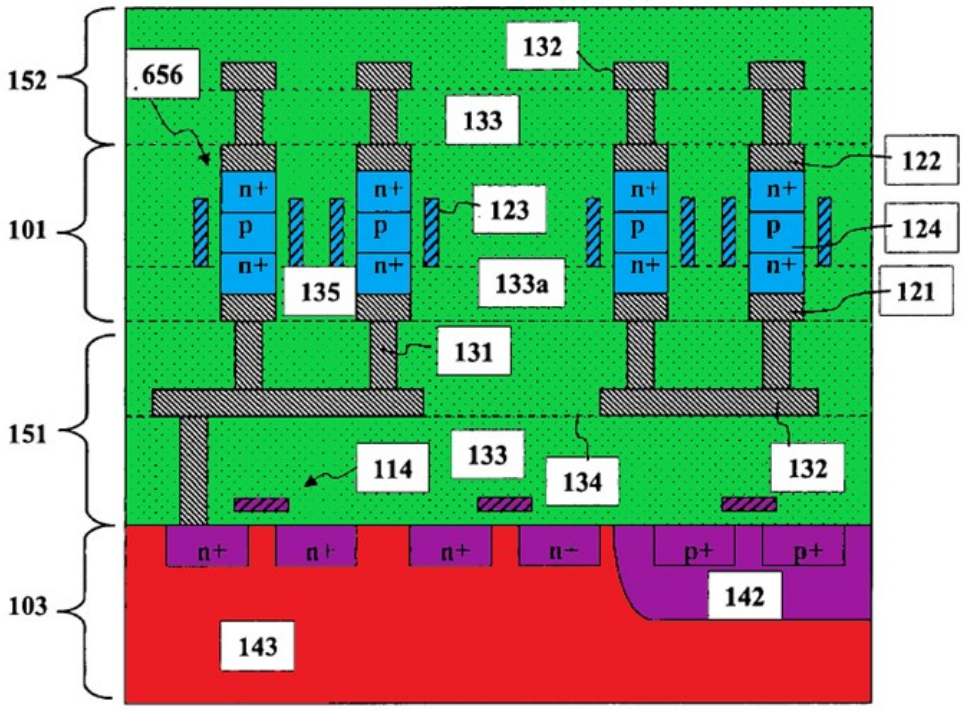
VI. THE CHALLENGED PATENT

A. The '702 Patent

29. The '702 Patent discloses that "[v]ertically oriented semiconductor memory cells are added to a separately fabricated substrate that includes electrical devices and/or interconnect." Ex-1001, code (57). "More particularly, the ['702 Patent] relates to a semiconductor substrate combined with a relatively thin add-on semiconductor layer in which various vertically oriented memory elements are fabricated." *Id.* 1:16-19. For example, Figure 1 below illustrates a "3-D integrated circuit arrangement," "that includes a semiconductor substrate [(red)] having devices [(purple)] and/or interconnect structures fabricated thereon." *Id.* 5:11-14. Base substrate 103 is bonded to "lower dielectric layer 151," comprising "[i]nter-layer dielectric (ILD) layers 133 [(green)]," which are disposed above the devices (purple) formed in the substrate. *Id.* 5:31-33, 5:37-41.

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Fig. 1



Id., Fig. 1.

30. The 3-D integrated circuit also has "at least one stackable add-on layer [(i.e., floating device layer (FLD) 101 with vertical memory devices 656 (blue) therein)], also having devices and/or interconnect, where the semiconductor substrate and the stackable add-on layer are stacked and bonded to each other." Ex-1001, 5:14-17. The '702 Patent describes forming "vertically oriented semiconductor memory cells" in a "stackable add-on layer," which is then bonded to the semiconductor substrate. *Id.* 5:5-7, 5:11-41. The '702 Patent does not describe the stackable add-on layer as built by sequentially depositing one layer (i.e., thin film) at a time directly on the semiconductor substrate to form vertically

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oriented memory cells within a multi-layer structure.[2] *See, e.g.*, *id.*, code (57), 1:47-50, 4:45-57. The '702 Patent further describes that each stackable add-on layer 101 has "interlayer dielectric (ILD) layers 133 [(green)] disposed above and below." *Id.* 3:51-54, 5:29-33, 5:11-17. Figure 1 also illustrates memory transistors (i.e., vertical memory devices 656 (blue)) with their source, channel, and drain regions oriented vertically or "substantially perpendicular to a major surface of a substrate." *Id.* 4:7-9, Fig. 1.

31. The '702 Patent further discloses that "Dynamic Random Access Memory (DRAM) cells, Static Random Access Memory (SRAM) cells, nonvolatile memory cells, and similar structures may be formed in a stackable add-on layer for use in conjunction with the separately fabricated substrate." Ex-1001, 2:4-9. Claims 1-12 are limited to DRAM and SRAM semiconductor memory

[2] Petitioner believes that the intrinsic record does not support any interpretation of Claim 13 that encompasses forming the "stackable add-on layer" by sequential deposition directly on the substrate. In its Complaint, however, Patent Owner appears to interpret "a stackable add-on layer" to cover sequential deposition. *See* Ex-1019 ¶¶71-76. For purposes of this petition, this issue need not be resolved because the prior art discloses or renders obvious forming a "stackable add-on layer" in the same manner as described in the '702 specification.

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structures, whereas Claims 13-17 recite nonvolatile semiconductor memory structures. "Vertical nonvolatile memory has a form of either dual-gate with floating gate [and control gate] or single-gate with charge trapping gate insulator." *Id.* 10:29-31; *see also id.* 9:65-10:1 ("FIG. 31 shows four vertical memory cells with serial connection of the four nonvolatile memory cells in the stackable add-on layer. The nonvolatile could be single-gate instead of dual-gates.").

32. The '702 Patent specifies that "vertical" "means substantially perpendicular to a major surface of a substrate." Ex-1001, 4:7-9. "SOI layer…refer[s] to a relatively thin, single crystal portion of a semiconductor wafer that can be cleaved and bonded to another previously fabricated wafer, or similar type of substrate." *Id.* 4:47-53. "[T]he SOI layer may be thought of as an attachment layer, or stackable add-on structure which is suitable for bonding to a semiconductor substrate already containing devices and/or interconnections." *Id.* 4:53-57. In addition, the '702 Patent states, "a FLD can be directly contacted by metal electrodes at top, bottom, and intermediate regions of the individual doped stack structures (i.e., pillar structures)." *Id.* 6:26-29.

B. Prosecution History of the '702 Patent

33. The '702 file history is submitted as Ex-1004. Although the Examiner's single Non-Final Office Action objected to the claims based on indefiniteness and rejected the claims for obviousness-type double patenting, the

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Examiner did not issue any substantive rejections based on prior art and cited only a single reference during prosecution. *See generally* Ex-1004; *id.* at 77 (citing only U.S. Patent 6,943,067). Remarkably, the inventor did not cite a single prior art reference. *See id.* Based on the limited information in the file history, the Examiner concluded that "[n]one of the references of record [of which there was *just one*] teaches or suggests the claimed SEMICONDUCTOR STRUCTURE." *Id.* at 122-23. Regarding claims 13-17 specifically, the Examiner stated that "a first stackable add-on layer, the first stackable add-on layer having a plurality of vertically oriented semiconductor memory cells; and the stackable add-on layer being bonded to the dielectric layer wherein the memory cells are nonvolatile memory cells having at least one transistor" was not taught by the *sole* reference of record, and on that basis allowed the patent to issue. *Id.* at 121-23. However, the subject matter of claims 13-17 was well known in the art, as shown below in Section VII.

C. Level of Ordinary Skill in the Art

34. A person of ordinary skill in the art at the relevant time ("POSITA") would have had a bachelor's degree in electrical engineering, computer engineering, or a related field, and at least two years of experience in the research, design, or development of semiconductor memory device structures, or the equivalent, with additional education substituting for experience and vice versa. I

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believe that I possessed and exceeded such experience and knowledge before and at the priority date and that I am qualified to opine on the '702 Patent.

VII. CLAIM CONSTRUCTION

35. I do not believe that any term requires explicit construction to resolve the issues presented in this Petition. I ascribe the plain meaning to each claim term, as that plain meaning would have been understood by a POSITA.

36. The '702 Patent includes a "Terminology" section (Ex-1001, 4:5-5:17) that defines certain terms, including certain terms recited by Claims 13-17: "vertical" (4:7-9), "device" (4:28-32), and "SOI" (4:45-5:7). In addition, the "Terminology" section defines "Vbias" (4:10-16), "chips, semiconductor device, integrated circuit, LSI device, monolithic integrated circuit, ASIC, SoC, microelectronic device, and similar expressions" (4:17-27), "FET" (4:33-44), "high dielectric constant" (5:8-10), and "3-D IC" (5:11-17).

37. I reserve the right to offer opinions on any claim constructions proposed in this proceeding or to offer opinions on additional constructions in the district court.

VIII. TECHNOLOGICAL BACKGROUND

A. It was well known to use vertically oriented memory cells to increase integration density.

38. A POSITA would have known to use vertically oriented memory cells to increase integration density (i.e., devices per unit area of wafer surface). For

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example, "vertical transistors are manufacturable far below channel lengths of 100 nm," so "the technology is very promising for mass storage and thus for the replacement of conventional mass storage devices by semiconductor-memories." Ex-1021; *see* Ex-1022 ("[T]o overcome the limitation of cell area of $4F^2$ per bit in conventional NAND Flash memory cells, stacked-surrounding gate transistor (S-SGT) structure cell is proposed."); *see also* Ex-1023 ("The new SRAM cell uses a thin vertical PNPN structure.").

B. It was well known to arrange a plurality of vertically oriented memory cells in a stackable add-on layer.

39. A POSITA would have known that arranging a plurality of vertically oriented memory cells in a stackable add-on layer would also increase integration density. For example, "to overcome the limitation of cell area of $4F^2$ per bit in conventional NAND Flash memory cells, stacked-surrounding gate transistor (S-SGT) structure cell is proposed." Ex-1022 at 945. "This newly structured cell achieves a cell area of $4F^2/N$ per bit, where *N* is the number of stacked memory cells in one silicon pillar." *Id.* "The S-SGT structured cell consisting of two stacked memory cells in one silicon pillar achieves a cell area per bit of less than 50% of the smallest reported NAND structured cell." *Id.*

40. A POSITA would have understood that a plurality of stackable add-on layers, each comprising a plurality of vertically oriented memory cells, could be stacked in a direction perpendicular to a substrate. A POSITA would have

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recognized that vertical transistors were "very promising for mass storage and thus for the replacement of conventional mass storage devices by semiconductor-memories." Ex-1021. For example, Watanabe describes forming planar members, comprising a plurality of memory cells, and repeating the process "the number of times equal to a necessary number of planar members" before stacking and bonding the layers. Ex-1005, 5:52-55, Figs. 2A, 5E, 6D. Similarly, Lee describes "an array of charge storage logic or memory devices," which "has a plurality of device levels 3104." Ex-1007, 12:17-25, Fig. 35; *see* Ex-1024 (describing a 3D shared memory consisting of stacks of device wafers each having a memory array).

41. A POSITA would have understood that arranging a plurality of vertically oriented memory cells in a stackable add-on layer would lead to creation of stacked memory layers with the shortest distance between them and low resistance interconnection wires. This, in turn, enables high interconnection densities and high-speed performance. A POSITA would have also known that another benefit of the 3D assembly technique in forming vertically oriented memory cells in a stackable add-on layer is that the stackable add-on layers are prefabricated separately, and in parallel, before they are stacked. Hence, each of them can be independently tested to verify functionality and performance prior to bonding, which further increases overall yield.

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C. It was well known to bond stackable add-on layers to a dielectric.

42. A POSITA would have known that for a memory device to function properly, a stackable add-on layer would need to be bonded to a dielectric above a substrate. It was well known that a 3D shared memory would require the stackable add-on layers to be bonded together. For example, "[t]he device wafer with the buried interconnections are bonded to the other device wafer…face-to-face through the micro-bumps. In this case, the bottom wafer is used as a supporting wafer for 3D integration as well as a device wafer." Ex-1024 at 0001. "After the temporary bonding using the micro-bumps, the liquid epoxy adhesive [(i.e., an insulator)] is injected into the gap between two wafers in a vacuum chamber to enhance the bondability of two wafers." *Id.* at 0001-02. Later, "another device wafer is glued to the thinned wafer stacked on the supporting wafer." *Id.* at 0002. Because the epoxy adhesive is an insulator, a POSITA would have understood that the device (i.e., a stackable add-on layer) is bonded to a dielectric above a substrate.

43. Similarly, Watanabe describes both a method of forming the stackable add-on layer through sequential deposition on top of a dielectric above a substrate and a method of forming the stackable add-on layers separately and stacking them on a dielectric layer above a substrate. Ex-1005, 5:3-6:14. A POSITA would have understood that the layers formed through the sequential deposition method were bonded to an insulating film or dielectric above a substrate. In addition, Watanabe

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explicitly discloses that the planar members formed separately for the stacking method are "bonded together" through a "thermal process of 900° to 1000° C." Ex-1005, 6:6-8. Thus, a POSITA would have understood that regardless of the formation method, stackable add-on layers would be bonded to a substrate to form a composite structure.

D. It was well known that nonvolatile memory cells have at least one transistor.

44. A POSITA would have known that a nonvolatile memory cell has at least one transistor. For example, "[t]he electrically programmable read-only memory (EPROM) was, in fact, the first nonvolatile memory that could be electrically programmed by the user and that could be erased afterward." Ex-1009 at 25. Specifically, "[o]ne floating gate transistor suffices to build an EPROM memory cell, as illustrated in Fig. 1.21 [below], and is, therefore called a single-transistor memory cell." *Id.* at 26.

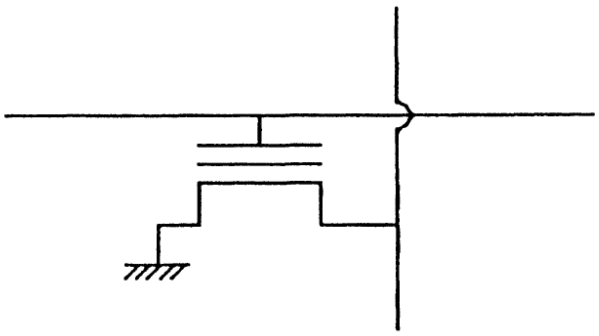


Figure 1.21 Single-transistor EPROM floating gate memory cell.

Id., Fig. 1.21. Similarly, electrically erasable programmable read-only memory (EEPROM) "consist[s] of a memory transistor and a select transistor [1.51] as

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shown in Fig. 1.24 [below], thus leading to the so-called two-transistor memory cell." *Id.* at 27-28.

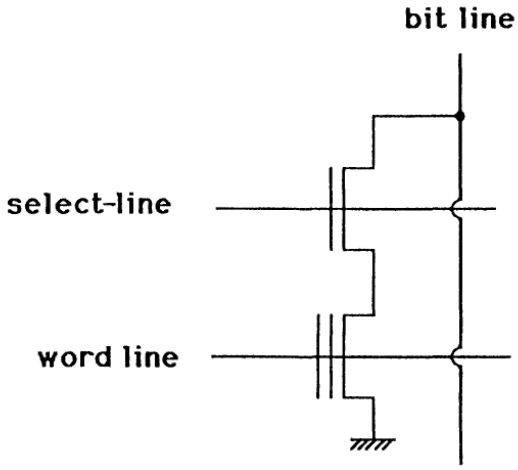


Figure 1.24 Two-transistor EEPROM memory cell. In order to allow byte selective write and erase, a select transistor is added to the memory cell.

Id., Fig. 1.24.

E. It was well known to form semiconductor structures on SOI pillars.

45. A POSITA would have known that forming a semiconductor structure on a Silicon-on-Insulator (SOI) substrate was common and offered several benefits. A SOI substrate offers several advantages, including better wafer utilization, improved power consumption, and reduced temperature dependency. *See, e.g.*, Ex-1016. Because the silicon pillars of a SOI substrate are completely isolated, the structure has fewer problems with interference and cross-communication between the memory devices and the isolation prevents charge leakage through the substrate. *See, e.g.*, Ex-1026. "SOI chips consist of millions of single-transistor islands dielectrically isolated from each other and from the underlying silicon substrate. On one hand, the vertical isolation protects the thin

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active silicon layer from most parasitic effects induced by the very 'bulky' substrate: leakage currents, radiation-induced photocurrents, latch-up effects, etc." Ex-1026 at 4969. "On the other hand, the lateral isolation makes interdevice separation in SOI free of complicated schemes of trench or well formation. The overall technology and circuit design are, in this respect, highly simplified and result in more compact VLSI chips." *Id.*

46. Further, stacking multiple layers using SOI wafers was well known in the art and offers the advantage of ease of manufacturing. *See, e.g.*, Ex-1014 at 834 ("In this paper, we propose more realistic 3D-LSI technology based on wafer bonding technique using micro-bumps." (footnote omitted)), Fig. 9 (showing the fabrication sequence of 3D-LSI); *see* Ex-1015 (enabling the transfer of fine layers of crystalline silicon material onto a mechanical support (i.e., producing SOI wafer substrates) on which integrated circuits are subsequently fabricated)); *see also* Ex-1010. For example, "[a]n SOI wafer consists of a bulk silicon substrate with a thin layer of single crystalline silicon on top, separated from the substrate by a silicon dioxide layer (buried oxide). The SOI wafer is used because the buried oxide layer acts as an etch-stop during a subsequent back-etch step." Ex-1010 at 28. Subsequently, the remaining thin SOI circuit can be transferred face down onto the top of the bulk silicon wafer. This leads to the formation of a multilayer 3D circuit.

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47. In fact, a POSITA would have known about commercial SOI wafer products sold for fabrication of integrated circuits (e.g., Soitec). *See* Ex-1027. In 1992, "engineers at Grenoble's CEA-Leti…, founded Soitec to manufacture SOI wafers on an industrial scale using the Smart Cut process, invented in 1991 within Michael Bruel's laboratory." Ex-1027 (explaining that Soitec partnered with Japanese manufacturer Shin-Etsu Handotai in 1997 and built its first production site in 1999); Ex-1015. Thus, a POSITA would have understood the advantages of forming or procuring a SOI wafer and using it as a substrate in forming a pillar-form semiconductor memory device and would have known that it was easy to do so with commercially available SOI products. A POSITA would also have known that such pillar-form semiconductor memory devices could readily be formed with commercially available SOI products.

F. It was well known that a vapor phase epitaxial method could be used for forming a single-crystal silicon layer on insulator.

48. A POSITA would have known that there were various ways to fabricate silicon-on-insulator (SOI) wafers. In addition to the Smart Cut process (as discussed above), vapor phase epitaxial technique was used. *See* Ex-1005, 3:31-54; *see also* Ex-1015. In this technique, an insulator, e.g., silicon dioxide, is first grown on a single crystal silicon wafer. *See, e.g.*, Ex-1029. Then, some precursor is delivered into the chamber where the wafer is in a gaseous state at high temperature (approximately or above 1000°C). Precursors such as silane (SiH_4)

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and silicon tetrachloride ($SiCl_4$) would decompose (or react with added hydrogen) to produce and transport silicon atoms on top of the wafer. Silicon atoms are absorbed and condensed onto the wafer to form SOI wafer. *See id.* In order to obtain single-crystal silicon (as opposed to polycrystalline or amorphous phase), narrow holes are etched in the insulator layer prior to the epitaxial growth step. *See* Ex-1028. The exposed silicon in the holes act as a seed for epitaxial growth. *See id.* The growth initiates in the seed area, grows vertically and laterally over the insulator, resulting in a SOI wafer. *Id.* In general, a polishing step such as CMP (chemical mechanical planarization) technique is used to planarize and thin down the silicon film. *See id.*

G. It was well known that floating gates and charge-trapping gates were interchangeable.

49. A POSITA would have known that floating gates and charge-trapping gates were interchangeable. "The storage of charges in the gate insulator of a MOSFET can be realized in two ways, which has led to the subdivision of nonvolatile semiconductor memory devices into two main classes"—floating gate devices and charge-trapping devices. Ex-1009 at 5. Floating gate devices are "based on the storage of charge on a conducting or semiconducting layer that is completely surrounded by a dielectric,…as shown in Fig. 1.5*a*. Since this layer acts as a completely electrically isolated gate, this type of device is commonly referred to as a floating gate device." *Id.* at 6. Alternatively, in charge-trapping devices,

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"the charge is stored in discrete trapping centers of an appropriate dielectric layer." *Id.*

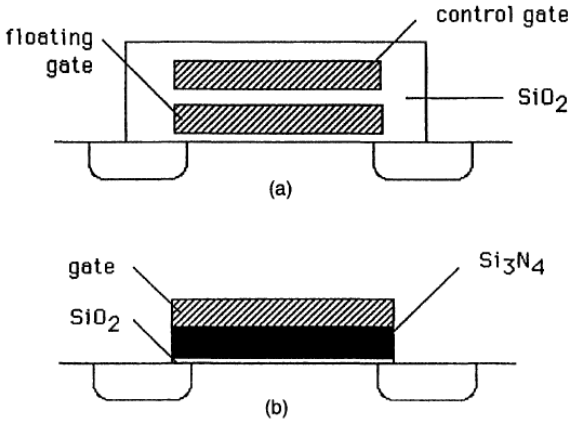


Figure 1.5 Two classes of nonvolatile semiconductor memory devices: (*a*) floating gate devices; (*b*) charge-trapping devices (MNOS device).

Id., Fig. 1.5. "Since the early day[s] of nonvolatile memories in the late 1960s, charge trapping transistors using silicon nitride as a charge storage layer have been an alternative to floating gate devices in EPROM, EEPROM, and later Flash memories." Ex-1018 at 0001.

50. Although a POSITA would have known that floating gates and charge-trapping gates were interchangeable, there are benefits of each method. For example, "the charge trapping concept has significant advantages when looking into advanced device structure like FinFET or 3D stacked memory cells." Ex-1018 at 0001. "In floating gate memories,…it becomes more and more difficult to maintain a high gate coupling ratio and keep floating gate interference limited." *Id.* "Replacing the floating cell by a charge trapping cell with Fowler Nordheim programming and erase can help to scale NAND devices further without significant changes in architecture and periphery circuits." *Id.* at 0002-03

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(explaining that charge trapping memory cells can be stacked and share periphery circuits in a NAND architecture); *see also* Ex-1009 at 7 (noting charge trapping devices "in commercial high-density nonvolatile memory circuits"). Ex-1020 ("[C]harge traps consume less energy during program and erase, so a 3D NAND that is based upon a charge trap is likely to be more energy-efficient than its floating gate counterpart.").

51. Similarly, "[c]harge traps require a lower programming voltage than do floating gates. This, in turn, reduces the stress on the tunnel oxide." Ex-1020. Because "stress causes wear in flash memories, the lower programming voltage gives charge trap flash greater endurance than conventional floating gate." *Id.* "Charge traps are also faster to program than conventional floating gate flash." *Id.*

52. In addition, in nitride or nanocrystal charge-trapping gate insulators, once the charge is trapped, the charge is far less likely to leak out as compared to a polysilicon layer. *See, e.g.*, Ex-1009 at 7 ("[A]n eventual pinhole in the thin tunneling oxide (I_1) will not lead to a complete discharge of the cell since the individual traps are isolated from each other by the nitride."). "3D NAND uses a charge trap because it's extremely difficult to create features, like a floating gate, sideways—lithography works from the top down." Ex-1020. "A charge trap, when used to replace a floating gate, doesn't need to be patterned, since the charge on one bit's charge trap will not leak through the insulating charge trap layer into an

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adjacent bit cell." *Id.* Because "the charge trap is an insulator[,] the charge in the trap can't flow from one side of the trap to the other, the way it would in a floating gate." *Id.* "Although stress-induced leakage can drain the charge off a floating gate, the same phenomenon would only drain the charge off of a portion of a charge trap without disturbing the charge on the remainder of the trap." *Id.* One potential drawback of the charge-trapping type of memory device is that the charge might be permanently stuck inside the nitride insulator which would lead to failed erase operations.

H. It was well known to connect memory cells using a NAND serial connection.

53. A POSITA would have known that a NAND connection would offer advantages for connecting a plurality of memory cells in a pillar. "Two common types of flash memory array architectures are the 'NAND' and 'NOR' architectures, so called for the logical form in which the basic memory cell configuration or each is arranged." Ex-1012, 1:29-32. In NOR architecture:

> the floating gate memory cells of the memory array are arranged in a matrix. The gates of each floating gate memory cell of the array matrix are coupled by rows to word select lines and their drains are coupled to column bit lines. The NOR architecture floating gate memory array is accessed by a row decoder activating a row of floating gate memory cells by selecting the word select line coupled to their gates.

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Id. 1:32-39. "A NAND array architecture also arranges its array of floating gate memory cells in a matrix…. However, each memory cell is not directly coupled to a column bit line by its drain." *Id.* 1:43-47. "Instead, the memory cells of the array are coupled together in series, source to drain, between a source line and a column bit line." *Id.* 1:47-49.

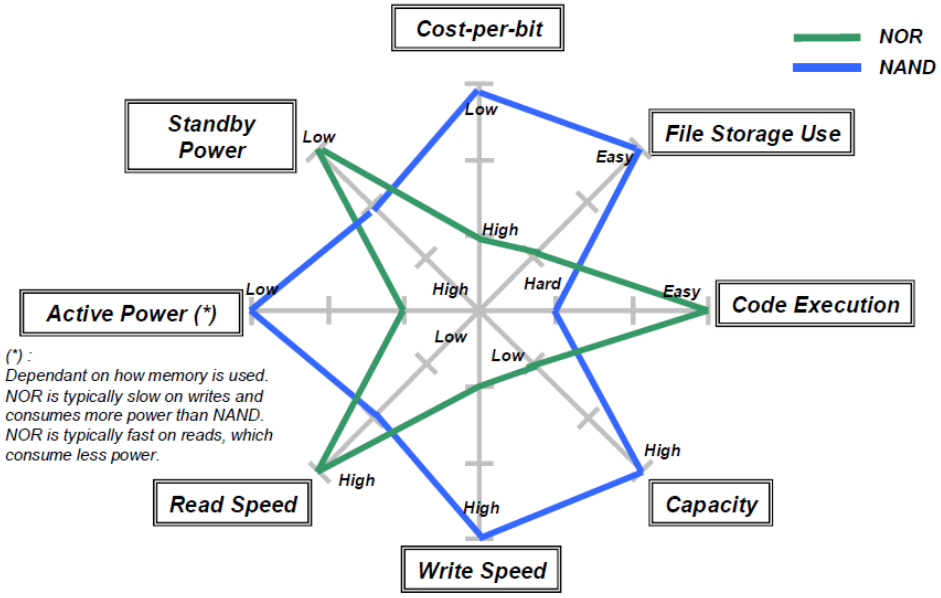
54. A POSITA would have found it obvious to use the NAND architecture because an entire NAND cell string uses only "one-half" of a bit line contact and "one-half" of a source line contact, which further increases the integration density of the memory design. Ex-1011, 2:59-65, 5:12-25 ("The primary purpose of using such a string structure is to reduce the number of contacts per memory cell…. The overall effect is a dramatic reduction in the chip area per memory cell.").

55. In addition, because NAND offers a higher integration density—among other advantages—than a NOR architecture, there is a large market for NAND architecture. "NAND Flash was developed as an alternative optimized for high-density data storage, giving up random access capability in a tradeoff to achieve a smaller cell size, which translates to a smaller chip size and lower cost-per-bit." Ex-1025 at 2. "Utilizing the NAND Flash architecture's high storage density and smaller cell size, NAND Flash systems enable faster write and erase by programming blocks of data. NAND Flash is ideal for low-cost, high-density,

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high-speed program/erase applications, often referred to as data-storage applications." *Id.* Not only will "the density of the NAND Flash memory array…always be higher than NOR Flash," but also "[f]or any write-intensive applications, NAND Flash will consume significantly less power." *Id.* at 3. "Figure 1 below provides a summary of how NAND and NOR Flash vary for a number of important design characteristics." *Id.* at 1.

Fig. 1 Comparison of NOR and NAND Flash



Id., Fig. 1.

I. It was well known that connecting memory cells on multiple SOI pillars using a NAND serial connection would increase the device density.

56. A POSITA would have known that connecting multiple SOI pillars—each comprising a plurality of memory cells—in series would further increase the integration density of the memory design. Ex-1011, 2:59-65, 5:12-25 ("The

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primary purpose of using such a string structure is to reduce the number of contacts per memory cell…. The overall effect is a dramatic reduction in the chip area per memory cell."). Specifically, an entire NAND cell string uses only "one-half" of a bit line contact and "one-half" of a source line contact. *Id.*

57. A POSITA would have known that a NAND string generally comprises eight, sixteen, or thirty-two memory cells connected in series. *See, e.g.*, Ex-1011 (illustrating an 8-cell NAND string); Ex-1013 (illustrating a 16-cell NAND string); Ex-1008, 3:8-16 (illustrating 16- and 32-cell NAND strings and explaining that the number of cells connected in series is expected to increase in the future). Further, because manufacturing and fabrication constraints generally limit the number of memory cells formed in the vertical direction, a POSITA would have found it obvious to connect multiple pillars in series to maximize the memory potential of the system. And a POSITA would have known that connecting multiple pillars in series requires interconnections between the pillars. Without an interconnection between pillars, "serially connected" pillars would have required the memory cells to be part of a single string.

58. For example, Watanabe illustrates vertically stacking two memory cells (Ex-1005, Figs. 5E and 6D), whereas Endoh illustrates NAND strings having more than four memory cells connected in series (Ex-1006, Fig. 65). Thus, a

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POSITA would have found it obvious to connect multiple pillars in series to achieve an eight, sixteen, or thirty-two memory cell system.

59. As discussed above, a POSITA would have understood that arranging a plurality of vertically oriented memory cells, i.e., NAND serial connection, in a stackable add-on layer would lead to high interconnection densities, high-speed performance and higher overall yield. A POSITA would also have known that the most suitable technology in fabricating these stackable add-on layers was (and still is today) silicon-on-insulator (SOI). In addition to the benefits and the flexibilities of SOI technology, memory cells integrated on multiple SOI pillars can offer significant advantages for high-speed performance, better isolation, lower leakage, and reduced interference between memory cells. In other words, it was well known for connecting memory cells on multiple SOI pillars using a NAND serial connection.

IX. BRIEF DESCRIPTION OF THE APPLIED PRIOR ART REFERENCES

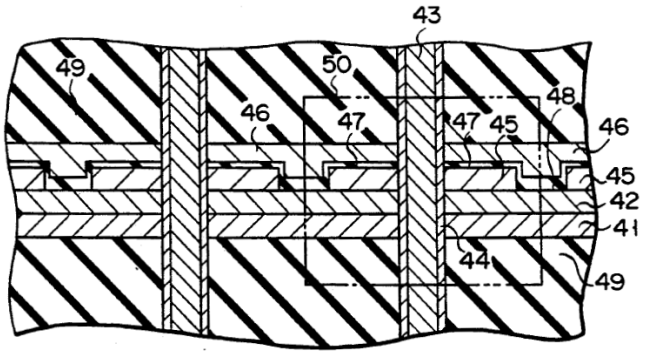
A. Watanabe (Ex-1005)

60. Watanabe was filed December 14, 1990, and issued February 25, 1992. Ex-1005. Watanabe qualifies as prior art under at least pre-AIA § 102(a), (b), and (e).

61. Watanabe discloses that "an object of the present invention is to provide a semiconductor memory device in which memory cells are arrayed three-

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dimensionally, thereby providing a high integration density." Ex-1005, 1:49-52. As shown in Figure 2A, Watanabe discloses stacks of vertically oriented semiconductor memory cells. *See id.* 3:12-15.



F I G. 2A

Id., Fig. 2A (showing one vertically oriented semiconductor memory cell consisting of layers 41 to 46).

62. Watanabe discloses two "method[s] used to manufacture a semiconductor memory device," Ex-1005, 5:68-6:19, in which "[t]he memory cell…is applicable to any type of memory device i.e., a SRAM, a PROM, or a DRAM." *Id.* 2:51-55 (including volatile and nonvolatile memory). "FIGS. 5A through 5E are sectional views showing a sequence of manufacturing process steps used in a method of manufacturing a semiconductor memory device according to the present invention, the method being called a 'laminating method.'" *Id.* 2:26-30. "FIGS. 6A through 6D are sectional views showing a sequence of manufacturing process steps used in another method of manufacturing a semiconductor memory

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device according to the present invention, the method being called a 'stacking method.'" *Id.* 5:31-35.

B. Endoh (Ex-1006)

63. Endoh was filed March 28, 2002, and published October 24, 2002. Ex-1006. Endoh qualifies as prior art under at least pre-AIA § 102(a), (b) and (e).

64. Endoh discloses pillar-form (i.e., vertical columnar-shaped) semiconductor memory devices and acknowledges that "[w]ith recent development in semiconductor technology, especially in micro-patterning techniques, the size reduction and the capacity increase of memory cells of EEPROM [(i.e., nonvolatile memory)] are rapidly progressing. Accordingly, it is important how large capacity can be ensured between the floating gate and the control gate." *Id.* ¶6. Like Watanabe, Endoh describes a process to form "transistors…in a direction vertical to the substrate." *Id.* ¶48. Endoh discloses forming semiconductor memory cells using "island-like semiconductor layers in a pillar form." *Id.* ¶¶527, 582, 617, 643, 657, 664, 700, 1007, 1039, 1291, 1322, 1348, 1359, 1381, 1385, 1415, 1421; *see id.* ¶¶183, 198, 220, Figs. 1, 2, 4. These "memory cells can be disposed in series in the direction vertical to the semiconductor substrate." *Id.* ¶831. In addition, Endoh discloses a SOI substrate, *id.* ¶329, a floating gate structure, *id.* ¶¶1205-07, a charge-trapping gate insulator structure, *id.* ¶40, and a serial NAND connection. *Id.* ¶1206.

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C. Lee (Ex-1007)

65. Lee was filed August 13, 2001, published March 7, 2002, and issued April 19, 2005. Ex-1007. Lee qualifies as prior art under at least pre-AIA § 102(a), (b), and (e).

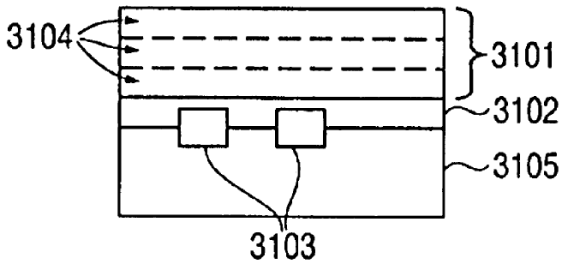
66. Lee discloses "a monolithic three dimensional array of charge storage devices which includes a plurality of device levels, wherein at least one surface between two successive device levels is planarized by chemical mechanical polishing." Ex-1007, code (57). "First, [Lee discloses] a substrate having an insulating surface (i.e., a Silicon-On-Insulator (SOI) substrate)…for the formation of the memory array." *Id.* 31:41-43. Lee discloses "a nonvolatile stackable pillar memory device and its method of fabrication," and "a three dimensional nonvolatile memory array, comprising a plurality of vertically separated device levels, each level comprising an array of TFT EEPROMs." *Id.* 5:28-56. Lee also discloses both "a dielectric isolated floating gate to store charge in the memory devices" and "a trapping layer formed in the dielectric stack," such as an ONO stack. *Id.* 18:61-19:5.

67. Lee's "FIG. 35 schematically illustrates an array of charge storage logic or memory devices 3101 formed above an interlayer insulating layer 3102 disposed above a monocrystalline substrate 3105." Ex-1007, 12:17-20. "The array 3101 has a plurality of device levels 3104, preferably separated by interlayer

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insulating layers. The driver circuits 3103, such as sense amps and charge pumps, are disposed in the monocrystalline substrate 3105, as CMOS or other transistors." Ex-1007, 12:23-27. As illustrated, device levels 3104 are vertically oriented semiconductor memory cells.

FIG. 35



Id., Fig. 35.

X. DETAILED EXPLANATION OF THE UNPATENTABILITY GROUNDS

68. The '702 Patent contains 17 claims of which Claims 13-17 are challenged in this Petition. Claims 1-7 are limited to DRAM semiconductor memory structures and Claims 8-12 are limited to SRAM semiconductor memory structures, whereas Claims 13-17 recite nonvolatile semiconductor memory structures. The subject matter of the challenged claims is disclosed by the prior art.

A. Ground 1: Claim 13 Is Obvious Over Watanabe

1. Element Claim 13[preamble]: A semiconductor memory structure, comprising:

69. To the extent that the preamble of Claim 13 is limiting, Watanabe discloses the preamble. Watanabe states, "The present invention relates to a

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semiconductor memory device." Ex-1005, 1:10-11; *id.* 1:49-52 (The present invention provides "a semiconductor memory device in which memory cells are arrayed three-dimensionally, thereby providing a high integration density.").

2. Element 13[a]: a substrate having electrical devices formed therein, and further having a dielectric layer disposed above the electrical devices;

70. Watanabe discloses claim element 13[a]. Watanabe discloses two methods of manufacturing a semiconductor memory device—a "stacking method" and "laminating method"—each of which discloses this element. Ex-1005, 5:1-6:14.

71. **Stacking Method:** Watanabe's "stacking method [is] described with reference to FIGS. 6A through 6D." Ex-1005, 5:56-57. "As shown in FIG. 6A [(annotated below)], a peripheral circuit and transistors 71 and 72 [(purple)] are formed in the surface region of an Si substrate [(red)]. An insulating film 100 [(green)] is applied to the entire surface of the structure." *Id.* 5:58-61; *see also id.*, Fig. 2A, 3:53-54 ("The bottom insulating film 49 [shown in Figure 2A] is formed on an Si substrate, for example."). A POSITA would have understood that components 72 are the gates of transistors 71 formed in the upper surface of the silicon substrate. Thus, Watanabe discloses an "Si substrate" having electrical devices (transistor components 71 and 72) formed therein, and further having a dielectric layer ("insulating film 100") disposed above the electrical devices. A

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POSITA would have recognized that transistor components 71 and 72 are field-effect transistors or FETs, which are examples of "devices" described by the '702 Patent. Ex-1001, 4:28-32. A POSITA would have understood peripheral circuits (e.g., sense amplifiers, drivers and decoder circuits) to include electrical devices such as transistor components 71 and 72.

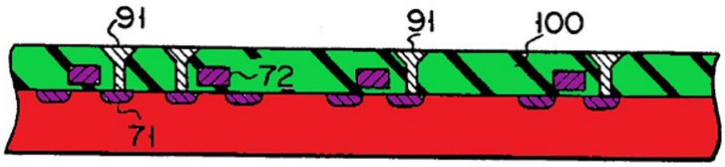


FIG. 6A

Id., Fig. 6A.

72. **Lamination Method:** Watanabe's "laminating method…[is] described[] with reference to FIGS. 5A through 5E." Ex-1005, 5:8-10. "As is shown in FIG. 5A [(annotated below)], insulating films [(green in Figure 5A)] are formed on transistor components 71 [(purple)] formed in the upper surface of a silicon substrate [(red)]." *Id.* 5:11-13. Although the insulating film (green) is unlabeled in Figure 5A, a POSITA would have understood that the green region in Figure 5A is an insulating film (as stated in the description at 5:11-12, but mistakenly referenced using numeral 72 (instead of 100), which is correctly identified as a transistor in Figure 6A). In comparing Figures 5 and 6, a POSITA would have understood that the green region, which is unlabeled in Figure 5A, corresponds to insulating film 100 of Figure 6A. Watanabe then teaches that

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"insulating film 80 [(green)] is layered over the resultant structure." Ex-1005, 5:23-25; *see also id.*, Fig. 2A, 3:53-54 ("The bottom insulating film 49 [shown in Figure 2A] is formed on an Si substrate, for example.").

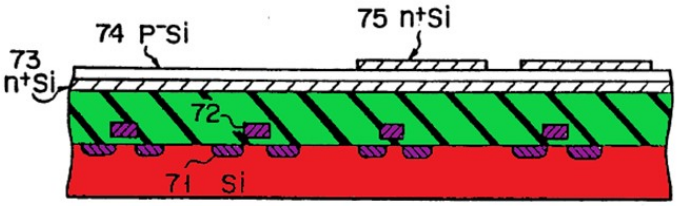


FIG. 5A

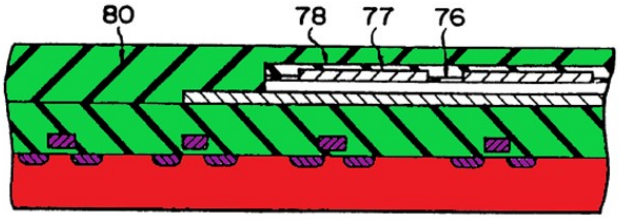


FIG. 5B

Id., Figs. 5A, 5B (annotated). Thus, Watanabe discloses a substrate having electrical devices formed therein, and further having a dielectric layer disposed above the electrical devices.

3. Element 13[b]: a stackable add-on layer having a plurality of vertically oriented semiconductor memory cells; and

73. Watanabe discloses claim element 13[b]. Watanabe states, "an object of the present invention is to provide a semiconductor memory device in which memory cells are arrayed three-dimensionally, thereby providing a high integration density." Ex-1005, 1:49-52. "In short, the present invention provides a 3-

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dimensional memory cell array in which memory cells [(green)] are respectively located at the cross points of a plurality of planar members (21, 22) [(orange)] arranged in parallel, and a plurality of wires (23, 26) pass through the planar members and are oriented orthogonal thereto." *Id.* 1:65-2:2. Thus, each planar member contains a plurality of semiconductor memory cells.

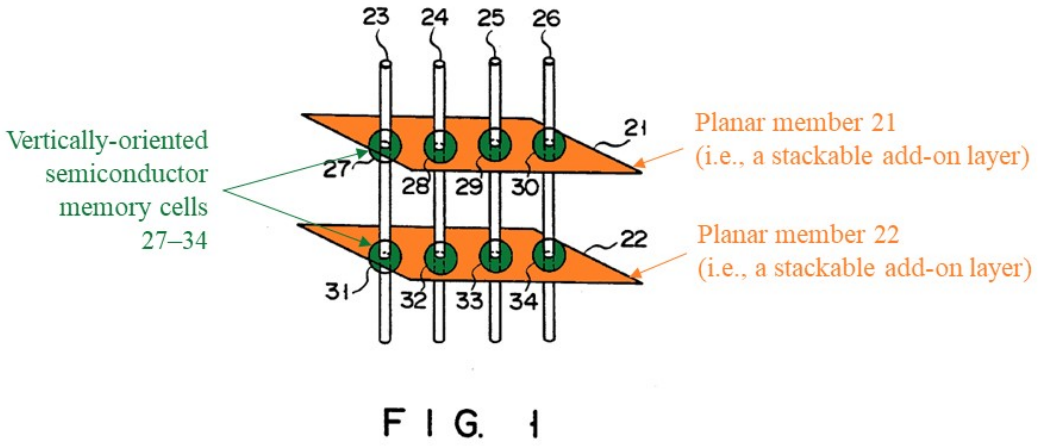


FIG. 1

Id., Fig. 1.

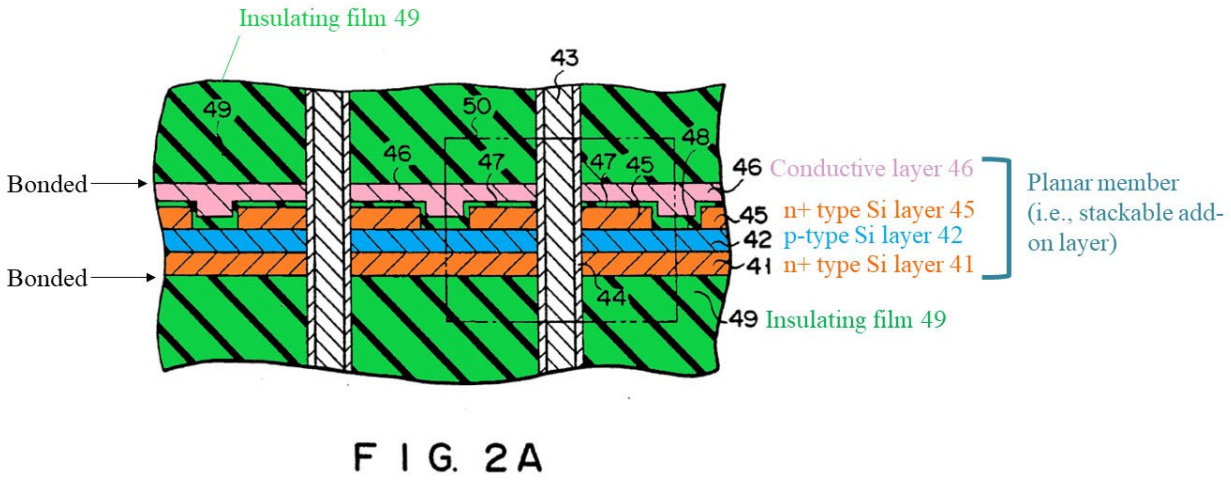
74. Further, Watanabe discloses that "FIG. 2A is a sectional view of a part of the semiconductor memory device shown in FIG. 1, and shows details of the memory device." Ex-1005, 2:11-13. Referring to Fig. 2A (annotated below):

> reference numeral 41 designates a conductive planar member in the form of an N+ type silicon (Si) layer [(orange)], this layer serving as the source of the MOSFET. Numeral 42 indicates a p-type Si layer [(blue)], while numeral 43 represents a wire oriented orthogonal to the planar member…, and which is separated from at least the layers 41, 42, 45, and 46 by an insulating film 44. Numeral 45 denotes an n+ type Si layer [(orange)]…. Preferably, a thick insulating film 48 fills the space between each of the

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> layers 45, and is itself overlaid with a conductive layer 46. *At least two stack structures (two layers)* [(i.e., two planar members)] *each consisting of layers 41 to 46 are provided*, which are insulated from each other by an insulting film 49 [(green)], and through which the wires 43 pass.

Id. 2:65-3:15 (emphasis added).



F I G. 2A

Id., Fig. 2A. Watanabe discloses the formation of semiconductor memory cells in which the transistors' source-channel-drain elements (e.g., elements 41, 42, and 45 of Figure 2A) are arranged vertically—i.e., "substantially perpendicular to a major surface of the substrate." Ex-1001, 4:7-9. Thus, Watanabe discloses vertically oriented semiconductor memory cells.

75. Watanabe further discloses two methods of manufacturing the stackable add-on layer having a plurality of vertically oriented semiconductor memory cells—a "stacking method" and "laminating method"—both of which disclose or render obvious this element. Ex-1005, 5:1-6:14.

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76. **Stacking Method:** "FIGS. 6A through 6D are sectional views showing a sequence of manufacturing process steps used in another method of manufacturing a semiconductor memory device," Ex-1005, 2:31-35, "in which memory cells are arrayed three-dimensionally, thereby providing a high integration density." *Id.* 1:50-52.

77. "As shown in FIG. 6B, a planar member is formed in a manner as shown in FIGS. 5A and 5B," Ex-1005, 5:64-65, which shows insulating films formed on transistor components 71 formed in the upper surface of a silicon substrate, an n+ type Si layer 73, a p-type Si layer 74, an n+ type Si layer 75, an insulating film 76, capacitor insulating films 77, capacitor electrodes 78, and a first insulating film 80 layered over the resultant structure. *Id.* 5:8-26. "The process is repeated by the number of times equal to a necessary number of planar members. Finally, the planar members thus formed [(i.e., previously fabricated on separate substrates)] are stacked and wired" onto the substrate having the peripheral circuit and transistors. *Id.* 5:52-55.

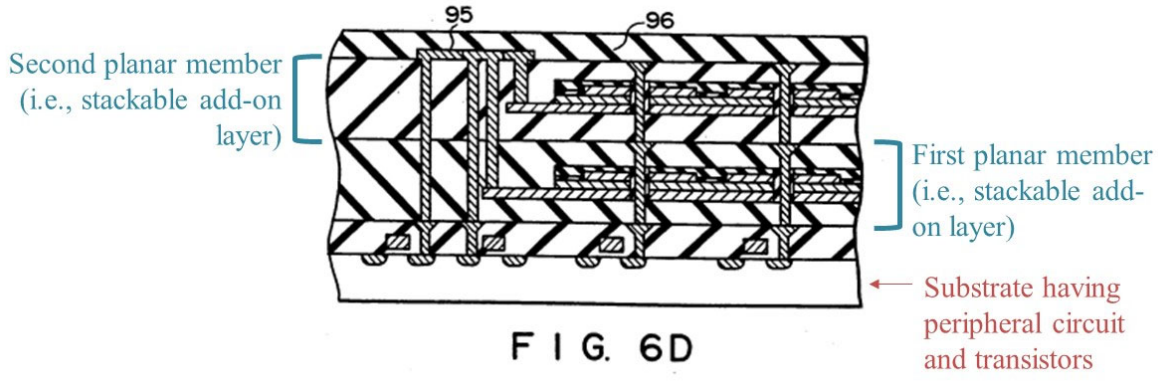


FIG. 6D

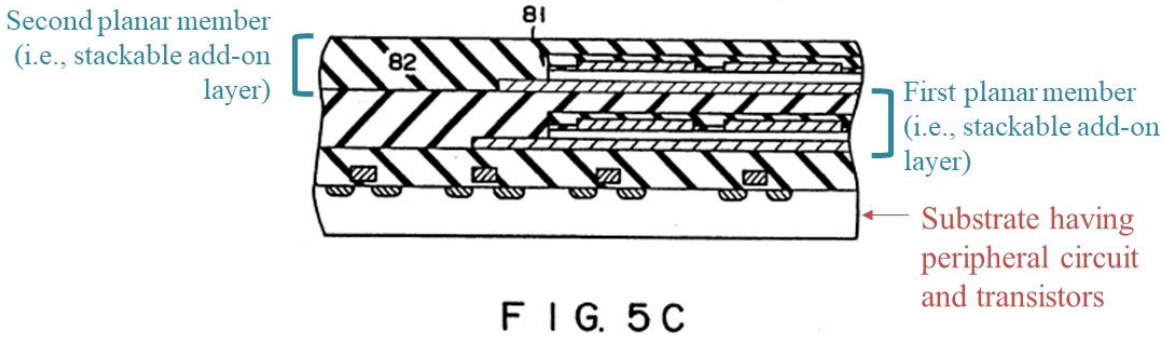
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Id., Fig. 6D. Because each of Watanabe's planar members contains a plurality of vertically oriented semiconductor memory cells, Watanabe's stacking method discloses a stackable add-on layer having a plurality of vertically oriented semiconductor memory cells.

78. **Lamination Method:** Watanabe's "laminating method" also discloses or renders obvious this element under PO's apparent construction (i.e., forming the "stackable add-on layer" by sequential deposition directly on the substrate). "FIGS. 5A through 5E are sectional views showing a sequence of manufacturing process steps used in a method of manufacturing a semiconductor memory device," Ex-1005, 2:26-30, "in which memory cells are arrayed three-dimensionally, thereby providing a high integration density." *Id.* 1:50-52. Watanabe's Figures 5A and 5B show the formation of planar members through sequential deposition of thin films on the substrate having the peripheral circuit and transistors. *See id.*, Figs. 5A, 5B. Unlike Watanabe's "stacking method," the planar members in the "laminating method" are not previously fabricated on separate substrates. Figures 5A and 5B show insulating films formed on transistor components 71 formed in the upper surface of a silicon substrate, an n+ type Si layer 73, a p-type Si layer 74, an n+ type Si layer 75, an insulating film 76, capacitor insulating films 77, capacitor electrodes 78, and a first insulating film 80 layered over the resultant structure. *Id.* 5:8-26.

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79. "As is shown in FIG. 5C [(annotated below)], a second planar member 81 is formed over the first planar member, and a second insulating film 82 is laid thereover, through a sequence of process steps similar to that used to form the first planar member." Ex-1005, 5:27-32. "[A]ccording to the laminating method [illustrated in Figures 5A-5E], a desired number of planar members are first formed into a stack of planar members." *Id.* 5:41-43.



F I G. 5 C

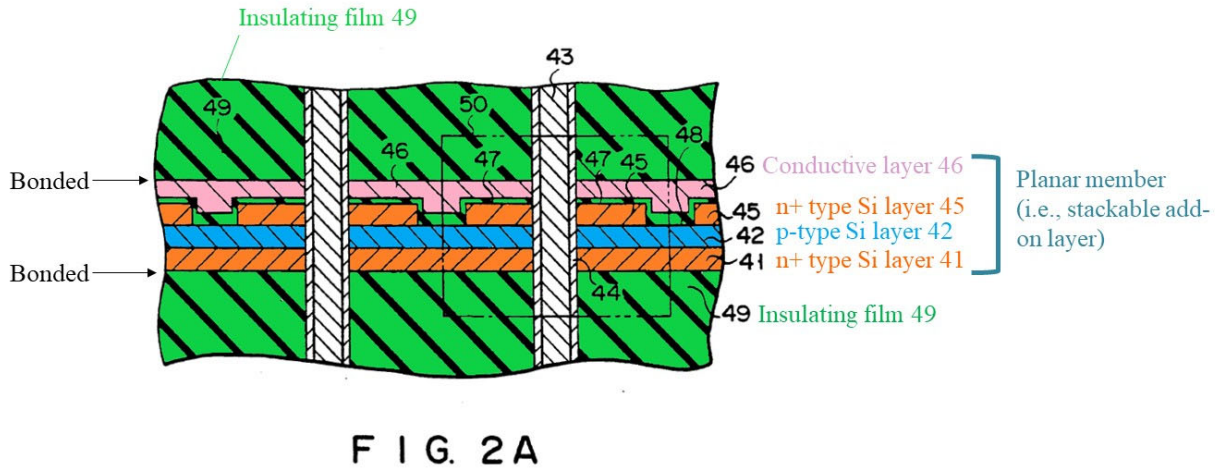
Id., Fig. 5C. Because each of Watanabe's planar members contains a plurality of vertically oriented semiconductor memory cells, Watanabe's laminating method discloses a stackable add-on layer having a plurality of vertically oriented semiconductor memory cells. Ex-1005, Fig. 7 (showing the source, channel, and drain in a vertical orientation).

4. Element 13[c]: the stackable add-on layer being bonded to the dielectric layer; and

80. Watanabe discloses claim element 13[c]. Watanabe discloses two methods of manufacturing a stackable add-on layer of a semiconductor memory device—a "stacking method" and "laminating method"—both of which disclose or

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render obvious this element. Ex-1005, 5:1-6:14. Under either method, Watanabe discloses "[a]t least two stack structures (two layers) [(i.e., two planar members)] each consisting of layers 41 to 46…, which are insulated from each other by an insulating film 49, and through which the wires 43 pass." *Id.* 3:9-15. Watanabe's Figure 2A (annotated below), illustrates one planar member consisting of layers 41 to 46 bonded to insulating film 49.



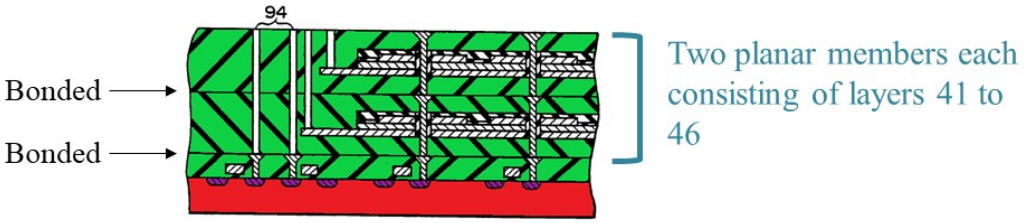
F I G. 2A

Id., Fig. 2A.

81. **Stacking Method:** In Watanabe's stacking method, the peripheral circuit of Figure 6A, including transistor components 71 with insulating film 100 formed thereover, is formed in the substrate in the same way as shown in Figure 5A. *See* Ex-1005, 5:64-65, 5:11-26. Next, "[a]s shown in FIG. 6B, a planar member is formed in a manner as shown in FIGS. 5A and 5B." *Id.* However, each planar member is formed on a *separate* substrate than the one shown in Figure 6A. *See id.*, Fig. 6B. It is only once the planar members are separately formed that they

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are stacked on the substrate of Figure 6A. "As shown in FIG. 6C [(annotated below)], the planar members thus formed are bonded together. The bonding is made by thermal process of 900° to 1000° C." Ex-1005, 6:6-8.



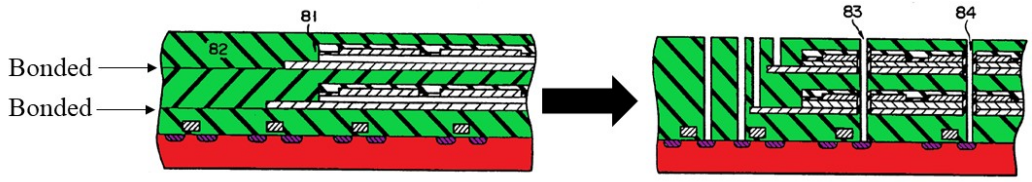
F I G. 6 C

Id., Fig. 6C. Thus, Watanabe's "stacking method" discloses a stackable add-on layer being bonded to the dielectric layer.

82. **Lamination Method:** Watanabe's "laminating method" also discloses or renders obvious this element under PO's apparent construction (i.e., forming the "stackable add-on layer" by sequential deposition directly on the substrate), with which I disagree. As shown in Figures 5A and 5B, Watanabe describes "the formation of a first planar member." Ex-1005, 5:11-26. "As is shown in FIG. 5C, a second planar member 81 is formed over the first planar member, and a second insulating film 82 is laid thereover, through a sequence of process steps similar to that used to form the first planar member. If necessary, third and subsequent planar members may be formed in similar ways." *Id.* 5:27-32. "In brief, according to the laminating method described above, a desired number of planar members are first formed into a stack of planar members." *Id.* 5:41-43. Because this method is described as "laminating," a POSITA would have understood that the planar

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members are bonded to the dielectric layer to form one structure.[3] *See supra* Section VIII.C; *compare* Ex-1005, Fig. 5C, *and* Ex-1005, Fig. 5D. If the layers were not bonded together, then the system would not function. *See supra* Section VIII.C.



F I G. 5C

F I G. 5D

Id., Figs. 5C, 5D. Thus, Watanabe's "laminating method" also discloses or renders obvious a stackable add-on layer being bonded to the dielectric layer.

[3] A POSITA would have understood that Watanabe's "lamination method" forms planar members (i.e., stackable add-on layers) that are bonded to the dielectric layer. The court has not yet construed the '702 Patent, and Petitioner does not concede that the term "bonded" should be construed as broadly as PO asserts in its complaint. To the extent this limitation requires the "stackable add-on layer" be fabricated *separately* and subsequently "bonded [to] the dielectric layer," this limitation is disclosed and rendered obvious by Watanabe's "stacking method."

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5. Element 13[d]: wherein the memory cells are nonvolatile memory cells having at least one transistor.

83. Watanabe discloses claim element 13[d]. Watanabe discloses, "The memory cell of the present invention is applicable to any type of memory device i.e., a SRAM, PROM, or a DRAM." Ex-1005, 2:51-53. A POSITA would have understood that PROM memory devices are nonvolatile. *See supra* Section VIII.D.

84. Watanabe further discloses, "An application of the present invention into an EPROM is illustrated in FIG. 7. In the figure, a reference numeral 106 designates a control gate; 107 a floating gate; 108 a source; 109 a channel region; and 110 a drain region." Ex-1005, 6:15-19. A POSITA would have understood that a source, channel, drain, floating gate, and control gate collectively form a nonvolatile memory cell transistor. *See, e.g.*, Ex-1009 at 4, 8-9. "The electrically programmable read-only memory (EPROM) was, in fact, the first nonvolatile memory that could be electrically programmed by the user and that could be erased afterward." Ex-1009 at 25.

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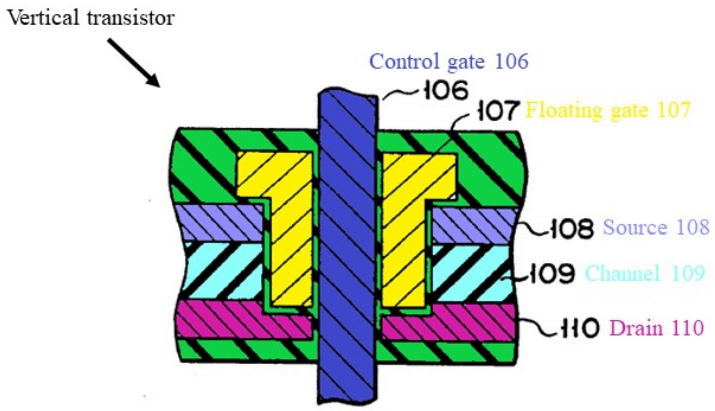


FIG. 7

Ex-1005, Fig. 7. Thus, Watanabe discloses that its invention is applicable to nonvolatile memory cells, which have at least one transistor. *See* Ex-1009 at 26 ("One floating gate transistor suffices to build an EPROM memory cell.").

B. Ground 2: Claims 14-17 Are Obvious Over Watanabe in View of Endoh

1. A POSITA would have been motivated to combine Watanabe with Endoh

85. A POSITA would have been motivated to combine Watanabe with Endoh and would have a reasonable expectation of success in doing so and achieving their stated objectives, because they are both from the same field and relate to the same well-known issues. Watanabe and Endoh provide complementary solutions for arranging memory cells three-dimensionally to provide a high integration density. *Compare* Ex-1005, 1:49-2:5, *with* Ex-1006 ¶151. A POSITA seeking to increase the integration density of semiconductor

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memory devices, and specifically nonvolatile memory devices, would have known of and consulted these proposed solutions.

86. Watanabe discloses techniques for manufacturing any type of semiconductor memory device—including nonvolatile memory—in which the memory cells are arrayed three-dimensionally to provide a high integration density. *See, e.g.*, Ex-1005, 1:49-52, 2:41-55, 5:1-6:19. Endoh provides additional well-known teachings of vertically oriented nonvolatile memory cells with a floating gate and control gate, or a charge-trapping gate insulator and gate, connected in series on a SOI pillar. *See, e.g.*, Ex-1006 ¶¶3, 6, 40, 151, 329, 662, 1138-72, 1205-07. A POSITA would have been motivated to modify Watanabe to obtain additional features and benefits from implementing the well-known teachings of a charge-trapping gate insulator, SOI pillar, and serial connection. *See* Ex-1006, ¶¶40, 329, 223, 257-58; *see infra* Sections X.B.2-X.B.5.

87. For example, Endoh states, "double the capacity of the prior-art memory device can be obtained if memory transistors in two tiers are formed per semiconductor substrate pillar." Ex-1006 ¶1659. "Thereby, the cell area per bit decreases, the size of chips can be decreased and the production costs can be reduced." *Id.* Similarly, Watanabe explains, "By virtue of such a 3-dimensional memory cell array, the integration density of the semiconductor memory device can be greatly increased." Ex-1005, 2:2-5. *Dystar Textilfarben GmbH & Co.*

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Deutschland KG v. C.H. Patrick Co., 464 F.3d 1356, 1368 (Fed. Cir. 2006) (A motivation to combine exists when the "improvement" results in a product or process that is "stronger, cheaper, cleaner, faster, lighter, smaller, more durable, or more efficient."). A POSITA would have had a reasonable expectation of success in achieving their objectives, e.g., arranging memory cells three-dimensionally to provide a high integration density, by combining the teachings of Watanabe and Endoh with no change in their respective functions because both references purport to solve these problems in similar and predictable ways, such as using the well-known teachings of vertical transistors and pillar structures. *See infra* Sections X.B.2-X.B.5.

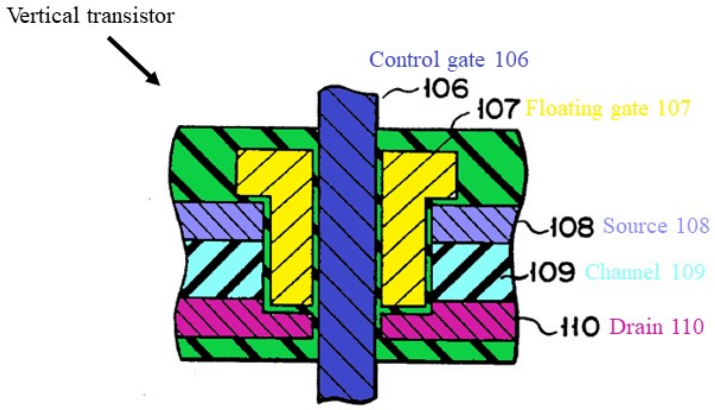
2. Dependent Claim 14: The semiconductor memory structure of claim 13, wherein the vertically oriented semiconductor nonvolatile memory cell comprises a vertical transistor having a floating gate and a control gate on a SOI pillar.

88. Watanabe alone or in view of Endoh discloses dependent Claim 14 or renders it obvious with the knowledge of one of ordinary skill in the art. Watanabe discloses a vertically oriented semiconductor memory cell for reasons set forth above for Element 13[d]. *See supra* Section VII.A.5; Ex-1005, 2:65-3:15, Fig. 2A.

89. Watanabe further discloses a vertical transistor having a floating gate and a control gate. Watanabe discloses, "An application of the present invention into an EPROM is illustrated in FIG. 7. In the figure, a reference numeral 106 designates a control gate; 107 a floating gate; 108 a source; 109 a channel region;

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and 110 a drain region." Ex-1005, 6:15-19, Fig. 7; Ex-1009 at 25-26 (explaining that EPROM is nonvolatile memory with at least one transistor).



F I G. 7

Id., Fig. 7 (showing the source, channel, and drain in a vertical orientation). Thus, Watanabe discloses a vertically oriented semiconductor nonvolatile memory cell comprising a vertical transistor having a floating gate and a control gate.

90. Second, Watanabe discloses or renders obvious forming a vertical transistor on a SOI pillar. As shown in Figure 7, Watanabe discloses a vertical transistor comprising a semiconductor layer (110, purple) on a planar insulator layer (green). *See* Ex-1005, 6:15-19, Fig. 7. Thus, a POSITA would have understood (or found it obvious) that Watanabe's vertical transistor can be formed on a SOI pillar. Ex-1001, 4:45-47. Moreover, Watanabe discloses that the "n+ type Si layer [45] is layered on an insulating film 49" and that "[w]hen a vapor phase epitaxial method is used for forming these layers, these may be successively

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formed by appropriately changing doping gases." Ex-1005, 3:33-37, Figs. 2A, 2B. A POSITA would have understood that epitaxial deposition is a common method of forming a SOI structure. *See supra* VIII.F. Although Watanabe discloses the epitaxial method with respect to a MISFET DRAM device, Watanabe explains that DRAM is used as an example and "[t]he memory cell of the present invention is applicable to any type of memory device." Ex-1005, 2:51-55. In addition, a POSITA would have understood that the vapor phase epitaxial method would apply equally to nonvolatile memory devices. *See supra* VIII.F.

91. It was well known in the art that a vapor phase epitaxial method would result in a single crystal grown layer and that this method was one of the methods to form SOI structures. *See supra* VIII.F. Because Watanabe discloses a vertical structure with "[a]t least two stack structures (two layers) [(i.e., two planar members)] each consisting of layers 41 to 46," Ex-1005, 3:12-13, a POSITA would have understood that Watanabe discloses a SOI pillar structure or renders it obvious with the knowledge of one of ordinary skill in the art. *See id.*, Figs. 1, 2A (showing individual doped structures forming vertical pillars above insulator 49). Thus, Watanabe discloses or renders obvious a vertically oriented semiconductor nonvolatile memory cell comprising a vertical transistor having a floating gate and a control gate on a SOI pillar.

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92. To the extent that Watanabe alone does not disclose the vertically oriented semiconductor nonvolatile memory cell on a SOI pillar structure, Watanabe in view of Endoh renders this limitation obvious. Endoh discloses, "Not only a bulk substrate but also an SOI substrate, a multi-layered SOI substrate and the like may be used." Ex-1006 ¶329. Endoh further discloses that "[t]he use of the SOI substrate as the semiconductor substrate can be applied to all the examples." *Id.* ¶662. In addition, Endoh's Production Example 52 discloses "a semiconductor memory device" in which "island-like semiconductor layers are formed in the form of *pillars* by selective epitaxial silicon growth." *Id.* ¶1206 (emphasis added). The example also explains that "a plurality of *floating gates* are formed as the charge storage layers," "two memory cells are arranged on each island-like semiconductor layer," "and the transistors are connected in series along the island-like semiconductor layer." *Id.* (emphasis added), Figs. 1, 1171, 1172 (illustrating "a memory cell array of an EEPROM"); Ex-1009 at 27-29, 32-33 (explaining that EEPROM is a form of nonvolatile memory and that "all floating gate memory cells have the same generic cell structure" with a floating gate and a control gate). Thus, Watanabe in view of Endoh discloses or renders obvious vertically oriented semiconductor nonvolatile memory cells comprising a vertical transistor having a floating gate and a control gate on a SOI pillar.

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93. A POSITA would have been motivated to combine Watanabe with Endoh's teachings of a SOI pillar. A SOI substrate offers several advantages, including better wafer utilization, improved power consumption, and reduced temperature dependency. *See generally* Ex-1016. Because the silicon pillars of a SOI substrate are completely isolated, the structure has fewer problems with interference and cross-communication between the memory devices and the isolation prevents charge leakage through the substrate. *See supra* Section VIII.E.

94. Further, stacking multiple layers using SOI wafers was well known in the art and offers the advantage of ease of manufacturing. *See, e.g.*, Ex-1014 at 834 ("In this paper, we propose more realistic 3D-LSI technology based on wafer bonding technique using micro-bumps." (footnote omitted)), Fig. 9 (showing the fabrication sequence of 3D-LSI); *see* Ex-1015. Stacking multiple layers using SOI wafers was discussed by many researchers, e.g., Sailer et. al. in 1997: "3D circuits are fabricated using standard bulk CMOS processing and are then transferred from one wafer to another. The transfer process allows alignment of the layers. The resulting structure consists of lower substrate and associated circuitry, with one or more thin-film circuit layers stacked on top, separated by bonding layers." *See* Ex-1010 at 27. For example, "[a]n SOI wafer consists of a bulk silicon substrate with a thin layer of single crystalline silicon on top, separated from the substrate by a silicon dioxide layer (buried oxide). The SOI wafer is used because the buried

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oxide layer acts as an etch-stop during a subsequent back-etch step." Ex-1010 at 28. Subsequently, the remaining thin SOI circuit can be transferred face down on the top of the bulk silicon wafer. This leads to the formation of a multilayer 3D-LSI circuit. *See supra* Section VIII.E.

95. Accordingly, a POSITA would have understood and been motivated to harness the benefits of a SOI substrate, such as the one proposed in Endoh. *See supra* Section VIII.E. Because SOI wafers were well known and commercially available, a POSITA would have had a reasonable expectation of success in forming Watanabe's pillar on a SOI wafer, as described in Endoh. *See supra* Section VIII.E (noting commercial SOI wafer products sold for fabrication of integrated circuits (e.g., Soitec)); *see* Ex-1006 ¶¶329, 1207, 1074, Fig. 1171 (disclosing a vertically oriented semiconductor memory cell with a floating gate, which can be formed on a SOI substrate). Thus, a POSITA would have been motivated to form or procure a SOI wafer and use it as a substrate in forming Watanabe's pillar structure and would have had a reasonable expectation of success in doing so.

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3. Dependent Claim 15: The semiconductor memory structure of claim 13, wherein the vertically oriented semiconductor nonvolatile memory cell comprises a vertical transistor having a charge-trapping gate insulator and a gate on a SOI pillar.

96. Watanabe in view of Endoh teaches dependent Claim 15. For reasons set forth above for Claim Element 13[d] and Claim 14, Watanabe discloses a "vertically oriented semiconductor nonvolatile memory cell" that comprises "a vertical transistor…on a SOI pillar." *See supra* Sections VII.A.5, VII.B.2. In the alternative, Watanabe in view of Endoh renders obvious forming vertically oriented semiconductor nonvolatile memory cells on a SOI pillar structure. *See supra* Section VII.B.2.

97. Moreover, a vertical transistor having a charge-trapping gate insulator and a gate would have been obvious over Watanabe. *See supra* Section VIII.G. A POSITA would have known that "[t]he storage of charges in the gate insulator of a MOSFET can be realized in two ways, which has led to the subdivision of nonvolatile semiconductor memory devices into two main classes," i.e., floating gate devices and charge-trapping devices. Ex-1009 at 5-6; *see supra* Section VIII.G.

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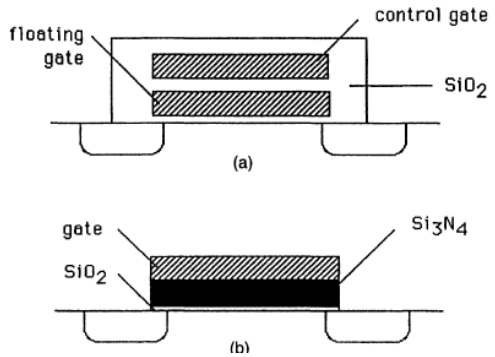


Figure 1.5 Two classes of nonvolatile semiconductor memory devices: (*a*) floating gate devices; (*b*) charge-trapping devices (MNOS device).

Id., Fig. 1.5. Although Watanabe's EPROM has a floating gate, Ex-1005, 6:15-19, Fig. 7, a POSITA would have understood that a charge-trapping gate insulator could replace the floating gate and offer significant advantages. *See supra* Section VIII.G.

98. "Since the early day[s] of nonvolatile memories in the late 1960s, charge trapping transistors using silicon nitride as a charge storage layer have been an alternative to floating gate devices in EPROM, EEPROM, and later Flash memories." Ex-1018 at 0001. "In floating gate memories,…it becomes more and more difficult to maintain a high gate coupling ratio and keep floating gate interference limited." *Id.* Accordingly, "the charge trapping concept has significant advantages when looking into advanced device structure like FinFET or 3D stacked memory cells." *Id.* For example, "[r]eplacing the floating cell by a charge trapping cell with Fowler Nordheim programming and erase can help to scale NAND devices further without significant changes in architecture and periphery circuits." *Id.* at 0002-03 (explaining that charge trapping memory cells can be stacked and share periphery circuits in a NAND architecture); *see also* Ex-1009 at

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7 (noting charge trapping devices "in commercial high-density nonvolatile memory circuits"). In addition, in nitride or nanocrystal charge-trapping gate insulators, once the charge is trapped, the charge is far less likely to leak out as compared to a polysilicon layer, thus improving memory retention. *See supra* Section VIII.G; *see also, e.g.*, Ex-1009 at 7 ("[A]n eventual pinhole in the thin tunneling oxide (I_1) will not lead to a complete discharge of the cell since the individual traps are isolated from each other by the nitride."). Thus, a POSITA would have found it obvious to implement Watanabe with a charge-trapping gate insulator instead of a floating gate. *See supra* Section VIII.G.

99. Alternatively, Watanabe in view of Endoh teaches "the storage of a charge…realized by a trap in a laminated insulating film" instead of "a floating gate structure." Ex-1006 ¶40. Endoh's Production Example 49 discloses:

> a *layered insulating film is used as the charge storage layer to realize charge storage by trapping in the layered insulating film*, as shown in FIGS. 1067 to 1093 and FIGS. 1094 to 1120. FIGS. 1067 to 1093 and FIGS. 1094 to 1120 are sectional views taken on line A-A' and line B-B', respectively, in FIG. 12 which illustrates a memory cell array of an EEPROM.

Id. ¶1139 (emphasis added), Figs. 1, 1171, 1172; Ex-1009 at 6, 27-29, 47-49 (explaining that EEPROM is a form of nonvolatile memory, "[c]harge-trapping as well as floating gate cells are used for EEPROM products," and that charge-

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trapping devices have a charge-trapping gate insulator and a gate). Endoh further discloses "a layered insulating film 1620" of MNOS or MONOS structure. Ex-1006 ¶1161; Ex-1009 at 6 ("In [charge-storage] devices, the charge is stored in discrete trapping centers of an appropriate dielectric layer…. The most successful device in this category is the MNOS device…structure."). Thus, Watanabe in view of Endoh discloses or renders obvious vertically oriented semiconductor nonvolatile memory cells comprising a transistor having a charge-trapping gate insulator and a gate on a SOI pillar.

100. A POSITA would have been motivated to combine Watanabe with Endoh's teachings of a transistor having a charge-trapping gate insulator and a gate on a SOI pillar. *See supra* Section VIII.G. As explained above, a POSITA would have known that the storage of charges in the gate insulator of a MOSFET can be realized through a floating gate or charge-trapping device. Ex-1009 at 5-6; *see supra* Section VIII.G. In addition, a POSITA would have known that charge trapping devices offer several advantages, including scalability for NAND devices without significant changes in architecture and periphery circuits. *See supra* Section VIII.G; Ex-1018 at 0002-03; *see also* Ex-1009 at 7. Thus, a POSITA would have understood and been motivated to harness the benefits of a charge trapping device, such as the one proposed in Endoh for 3D stacked memory cells.

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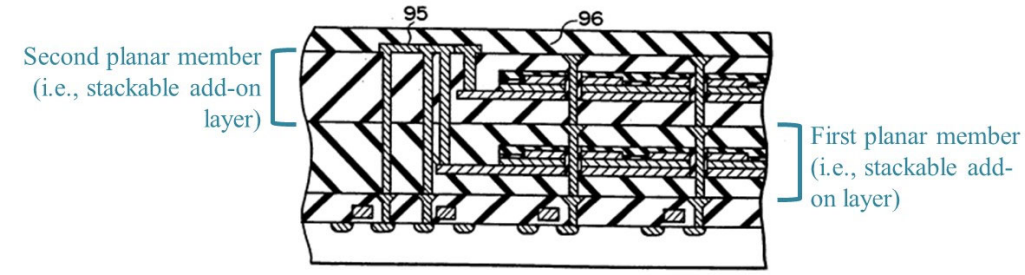
101. Because charge trapping devices were well known as the alternative to a floating gate, a POSITA would have had a reasonable expectation of success in implementing Watanabe with a charge trapping device, as described in Endoh. *See supra* Section VIII.G. In addition, a POSITA would have understood that "[c]harge-trapping as well as floating gate cells are used for EEPROM products," and other nonvolatile memory cells, and that these components were interchangeable. Ex-1009 at 6, 27-29, 47-49; *see* Ex-1006 ¶¶329, 1160, Fig. 1091 (disclosing a vertically oriented semiconductor memory cell with a charge-trapping gate insulator, which can be formed on a SOI substrate). Thus, a POSITA would have been motivated to implement Watanabe with a charge-trapping gate insulator and would have had a reasonable expectation of success in doing so.

4. Dependent Claim 16: The semiconductor memory structure of claim 13, wherein at least two nonvolatile memory cells are vertically oriented and serially connected together and formed with a first SOI pillar.

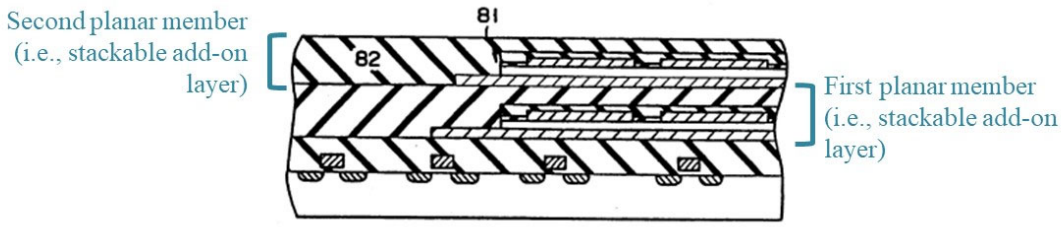
102. Watanabe in view of Endoh teaches dependent Claim 16. For reasons set forth above for Claim Element 13[d] and Claim 14, Watanabe discloses a "vertically oriented semiconductor nonvolatile memory cell" that comprises "a vertical transistor…on a SOI pillar." *See supra* Sections VII.A.5, VII.B.2. In the alternative, Watanabe in view of Endoh renders obvious forming vertically oriented semiconductor nonvolatile memory cell on a SOI pillar structure. *See supra* Section VII.B.2.

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103. Moreover, Watanabe discloses at least two vertically oriented nonvolatile memory cells. As shown in Figures 6D and 5C (annotated), Watanabe further discloses "[a]t least two stack structures (two layers) [(i.e., two planar members)] each consisting of layers 41 to 46." Ex-1005, 3:12-13.



F I G. 6D



F I G. 5 C

Id., Figs. 6D (showing two vertically oriented memory cells formed from Watanabe's "stacking" method), 5C (showing two vertically oriented memory cells formed from Watanabe's "laminating" method). Thus, Watanabe discloses at least two nonvolatile memory cells that are vertically oriented.

104. In addition, Watanabe in view of Endoh teaches two serially connected nonvolatile memory cells. "Two common types of flash memory array architectures are the 'NAND' and 'NOR' architectures, so called for the logical

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form in which the basic memory cell configuration or each is arranged." Ex-1012, 1:29-32. In NOR architecture:

> the floating gate memory cells of the memory array are arranged in a matrix. The gates of each floating gate memory cell of the array matrix are coupled by rows to word select lines and their drains are coupled to column bit lines. The NOR architecture floating gate memory array is accessed by a row decoder activating a row of floating gate memory cells by selecting the word select line coupled to their gates.

Id. 1:32-39. "A NAND array architecture also arranges its array of floating gate memory cells in a matrix…. However, each memory cell is not directly coupled to a column bit line by its drain." *Id.* 1:43-47. "Instead, the memory cells of the array are coupled together in series, source to drain, between a source line and a column bit line." *Id.* 1:47-49.

105. A POSITA would have found it obvious to use the NAND architecture because an entire NAND cell string uses only "one-half" of a bit line contact and "one-half" of a source line contact, which further increases the integration density of the memory design. Ex-1011, 2:59-65, 5:12-25 ("The primary purpose of using such a string structure is to reduce the number of contacts per memory cell…. The overall effect is a dramatic reduction in the chip area per memory cell."); *see supra* Section VIII.H. In addition, because NAND offers a higher integration density than a NOR architecture, there is a bigger market for

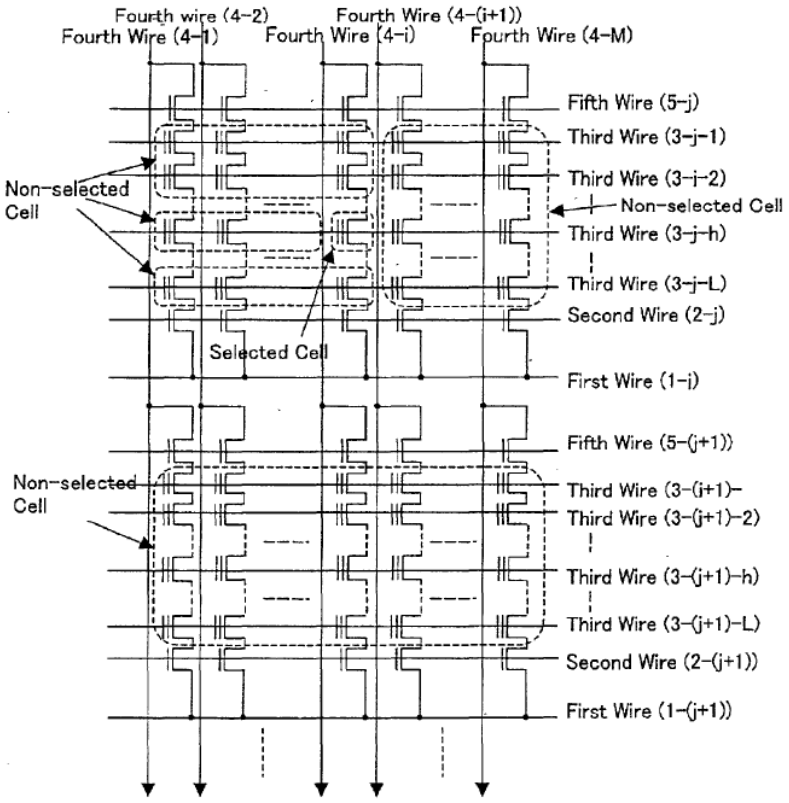
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NAND architecture. *See supra* Section VIII.H. Thus, a POSITA would have found it obvious to modify Watanabe's pillar structure to use the NAND architecture and a serial connection as taught by Endoh. *See, e.g.*, Ex-1006 ¶1205-07.

106. For example, Endoh's Production Example 52 discloses "a semiconductor memory device [having] a structure in which…island-like semiconductor layers are formed in the form of *pillars* by selective epitaxial silicon growth." Ex-1006 ¶1206 (emphasis added). The EEPROM memory cell array of Production Example 52 comprises "two memory cells…arranged on each island-like semiconductor layer…[with] the transistors…*connected in series* along the island-like semiconductor layer, as shown in FIG. 1171 and FIG. 1172." *Id.* ¶¶1206-07 (emphasis added), Figs. 1, 1171, 1172; *id.* ¶1074 (describing vertically oriented semiconductor memory cells); Ex-1009 at 27-29 (explaining that EEPROM is a form of nonvolatile memory). For example, "FIG. 65 shows the equivalent circuit diagram of the…memory cell array" having "a plurality of (e.g., M×N, wherein M and N are positive integers) island-like semiconductor layers." Ex-1006 ¶¶257-58.

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Fig. 65



Id., Fig. 65. Thus, Watanabe in view of Endoh teaches two vertically oriented nonvolatile memory cells serially connected and formed on a SOI pillar.

107. A POSITA would have been motivated to combine Watanabe with Endoh's teachings of a serial connection. *See supra* Section VIII.H. As explained above, NAND increases the integration density of a memory design by reducing the number of contacts per memory cell and, thus, reducing the chip area per memory cell. Ex-1011, 2:59-65, 5:12-25; *see supra* Section VIII.H. Because an object of Watanabe "is to provide a semiconductor memory device…providing a high integration density," a POSITA would have been motivated to modify

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Watanabe's pillar structures to use a serial connection as taught by Endoh. *See supra* Section VIII.H.

108. Further, a POSITA would have had a reasonable expectation of success in modifying Watanabe to use a NAND serial connection because the "[t]wo common types of flash memory array architectures"—NAND and NOR—both "arrange[] its array of…memory cells in a matrix such that the gates of each…memory cell of the array are coupled by rows to word select lines." Ex-1012, 1:29-46. Because the NAND architecture was well known and nonvolatile memory cell structure in NAND were (and still are today) similar to those in NOR architecture, a POSITA would have had a reasonable expectation of success in modifying Watanabe to use a NAND serial connection. *See supra* Section VIII.H. Thus, Watanabe in view of Endoh discloses or renders obvious at least two vertically oriented nonvolatile memory cells serially connected and formed with a SOI pillar.

5. Dependent Claim 17: The semiconductor memory structure of claim 16, wherein the at least two nonvolatile memory cells on the first SOI pillar are serially connected with an interconnect line disposed on a dielectric layer, to a nonvolatile memory cell formed with a second SOI pillar.

109. Watanabe in view of Endoh teaches dependent Claim 17. For reasons set forth above for Claim Element 13[d] and Claim 14, Watanabe discloses a "vertically oriented semiconductor nonvolatile memory cell" that comprises "a

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vertical transistor…on a SOI pillar." *See supra* Sections VII.A.5, VII.B.2. In the alternative, Watanabe in view of Endoh renders obvious forming vertically oriented semiconductor nonvolatile memory cell on a SOI pillar structure. *See supra* Section VII.B.2.

110. Moreover, Watanabe in view of Endoh teaches at least two nonvolatile memory cells on a first SOI pillar connected serially to a nonvolatile memory cell formed on a second SOI pillar via an interconnect line disposed on a dielectric layer. For reasons set forth above for Claim 16, Watanabe in view of Endoh discloses or renders obvious at least two vertically oriented nonvolatile memory cells serially connected and formed with a SOI pillar. *See supra* Section VII.B.4. Because an entire NAND cell string uses only "one-half" of a bit line contact and "one-half" of a source line contact, a POSITA would have understood that connecting a plurality of pillars of memory cells would further increase the integration density of the memory design. *See supra* Sections VIII.H, VIII.I; Ex-1011, 2:59-65, 5:12-25 ("The primary purpose of using such a string structure is to reduce the number of contacts per memory cell…. The overall effect is a dramatic reduction in the chip area per memory cell.").

111. A POSITA would have recognized the constraints of connecting individual devices in series vertically and found it obvious to form a first pillar with several memory devices formed in series and then connect in series the first

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pillar to additional pillars each with additional memory devices. *See supra* Sections VIII.H, VIII.H. A POSITA would have known that a NAND string generally comprises eight, sixteen, or thirty-two memory cells connected in series. *See supra* Sections VIII.H, VIII.I; *see also, e.g.*, Ex-1011 (illustrating an 8-cell NAND string); Ex-1013 (illustrating a 16-cell NAND string); Ex-1008, 3:8-16 (illustrating 16- and 32-cell NAND strings and explaining that the number of cells connected in series is expected to increase in the future). Further, because manufacturing and fabrication constraints generally limit the number of memory cells formed in the vertical direction, a POSITA would have found it obvious to connect multiple pillars in series to maximize the memory potential of the system. And a POSITA would have known that connecting multiple pillars in series requires interconnections between the pillars. *See supra* Sections VIII.H, VIII.I. Without an interconnection between the pillars, a POSITA would have understood the memory cells to be part of a single string. *See id.*

112. For example, Watanabe illustrates vertically stacking two memory cells (Ex-1005, Figs. 5E and 6D), whereas Endoh illustrates NAND strings having more than four memory cells connected in series (Ex-1006, Fig. 65). Thus, to form the NAND circuit shown in Endoh, a POSITA would have found it obvious to connect multiple pillars in series as disclosed by Watanabe. In addition, a POSITA would have found it obvious to connect the pillars using an interconnect line

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disposed on a dielectric layer to avoid shorting any of the devices. One common method, as described by Watanabe, is first forming vias (or holes) on the dielectric layer, followed by depositing interconnect line (wires) in the vias. *See, e.g.*, Ex-1005. Indeed, Watanabe discloses forming interconnect lines on a dielectric layer. *See, e.g.*, Ex-1005, Fig. 5E (interconnect 85), Fig. 6D (interconnect 95); *see also* Ex-1030 (describing pillars of memory cells connected via common select gates). Thus, Watanabe in view of Endoh teaches two nonvolatile memory cells on a first SOI pillar connected serially to a nonvolatile memory cell formed on a second SOI pillar via an interconnect line disposed on a dielectric layer.

113. A POSITA would have been motivated to combine Watanabe with Endoh's teachings of a serial connection. For example, an object of Watanabe "is to provide a semiconductor memory device…providing a high integration density." Ex-10052, 1:49-52. Because NAND offers a higher integration density than a NOR architecture, there is a bigger market for NAND architecture. *See supra* Sections VIII.H, VIII.I. Utilizing the high integration density of NAND, a POSITA can connect several memory cells and pillars in series to further increase the memory capacity in a single assembly. *Id.* Thus, a POSITA would have been motivated to connect a plurality of memory cells on a pillar in series and then connect a plurality of pillars in series, via interconnects, to further form an 8-, 16-, or 32-cell string. *See supra* Section VIII.I.

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114. Further, a POSITA would have had a reasonable expectation of success in modifying Watanabe to use a NAND serial connection between memory cells on a pillar and between pillars because the "[t]wo common types of flash memory array architectures"—NAND and NOR architectures—both "arrange[] its array of…memory cells in a matrix such that the gates of each…memory cell of the array are coupled by rows to word select lines." Ex-1012, 1:29-46. "However each memory cell [of a NAND architecture] is not directly coupled to a column bit line by its drain. Instead, the memory cells of the array are coupled together in series, source to drain, between a source line and a column bit line." *Id.* 1:46-49. Because the NAND architecture was well known and nonvolatile memory cell structures in NAND were (and still are today) similar to those in NOR architecture, a POSITA would have had a reasonable expectation of success in modifying Watanabe to use a NAND serial connection. *See supra* Sections VIII.H, VIII.I.

C. Ground 3: Claims 13-15 Are Obvious Over Lee

1. Element Claim 13[preamble]: A semiconductor memory structure, comprising:

115. To the extent that the preamble of Claim 13 is limiting, Lee discloses the preamble. Lee discloses, "The present invention relates to semiconductor devices in general and to a three dimensional TFT [(thin film transistor)] array in particular." Ex-1007, 1:25-26. A "preferred embodiment of the present invention provides a nonvolatile stackable pillar memory device and its method of

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fabrication." *Id.* 5:28-38; *see id.* 12:17-27 ("FIG. 35 schematically illustrates an array of charge storage logic or memory devices 3101.").

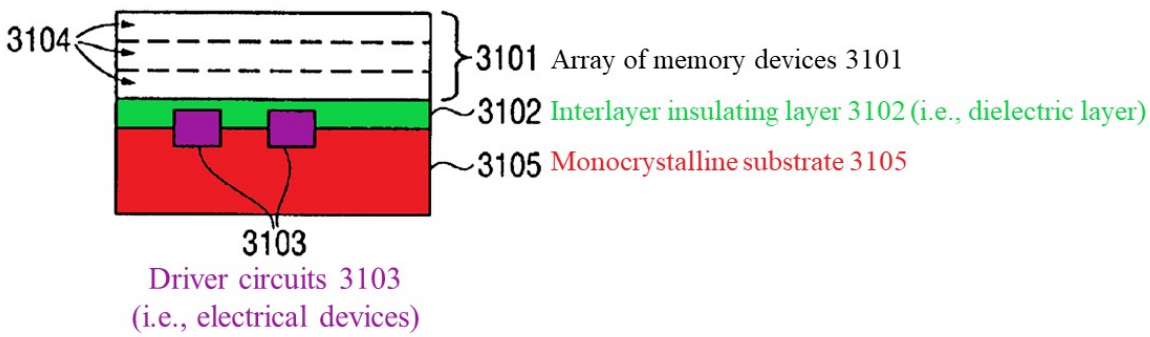
2. Element 13[a]: a substrate having electrical devices formed therein, and further having a dielectric layer disposed above the electrical devices;

116. Lee discloses claim element 13[a]. Lee discloses:

> FIG. 35 [(annotated below)] schematically illustrates an array of charge storage logic or memory devices 3101 formed above an interlayer insulating layer 3102 [(green)] disposed above a monocrystalline substrate 3105 [(red)]. The array of charge storage logic or memory devices 3101 are thus arranged as a three dimensional monolithic array thin film transistors or diodes in amorphous or polysilicon layers. The array 3101 has a plurality of device levels 3104, preferably separated by interlayer insulating layers. The driver circuits 3103 [(purple)], such as sense amps and charge pumps are disposed in the monocrystalline substrate 3105, as CMOS or other transistors.

Ex-1007, 12:17-27.

FIG. 35



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Id., Fig. 35. The '702 Patent describes "devices" broadly as including any "active and passive circuit elements." Ex-1001, 4:28-32. Thus, a POSITA would have understood driver circuits such as sense amps and charge pumps to constitute "electrical devices." Ex-1007, 12:13-15. Therefore, Lee discloses a substrate having electrical devices formed therein, and further having a dielectric layer disposed above the electrical devices.

3. Element 13[b]: a stackable add-on layer[4] having a plurality of vertically oriented semiconductor memory cells; and

117. Lee discloses claim element 13[b]. Lee discloses, "thin film transistors (TFTs) and diodes arranged in a pillar configuration (i.e., the vertical direction with respect to the substrate, where the length of the device is perpendicular to the substrate) and their method of fabrication." Ex-1007, 13:32-36; *see id.* 14:10-31 ("The first contact region 102 [(pink)], the body 104 [(blue)], and the second contact (source/drain) region 106 [(orange)] are each vertically aligned with one another to form a pillar 108."); *id.*, Fig. 1A; Ex-1001, 4:7-9 ("'[V]ertical'…means substantially perpendicular to a major surface of a substrate."). Thus, Lee discloses a plurality of vertically oriented semiconductor

[4] Lee discloses the subject matter of the '702 Patent under the interpretation Patent Owner appears to adopt. *See* Ex-1019 ¶¶71-76.

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memory cells wherein each cell is aligned substantially perpendicular to a major surface of the substrate. *Id.* 4:7-9.

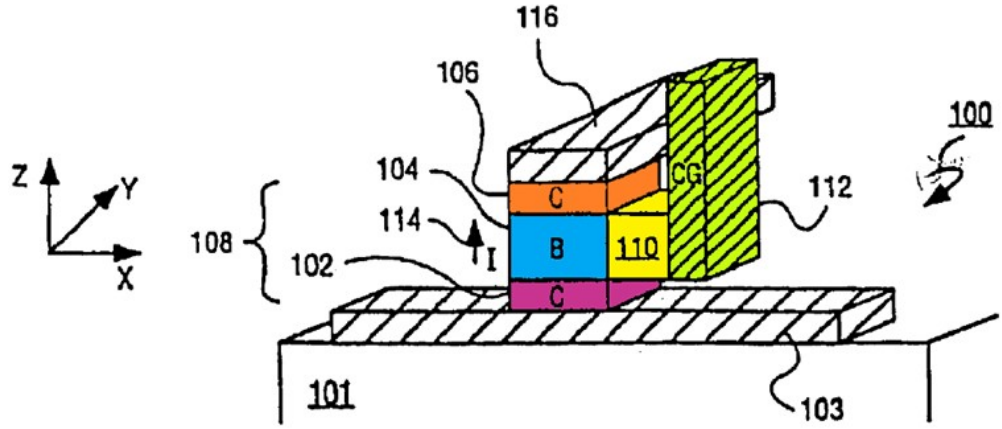


FIG. 1A

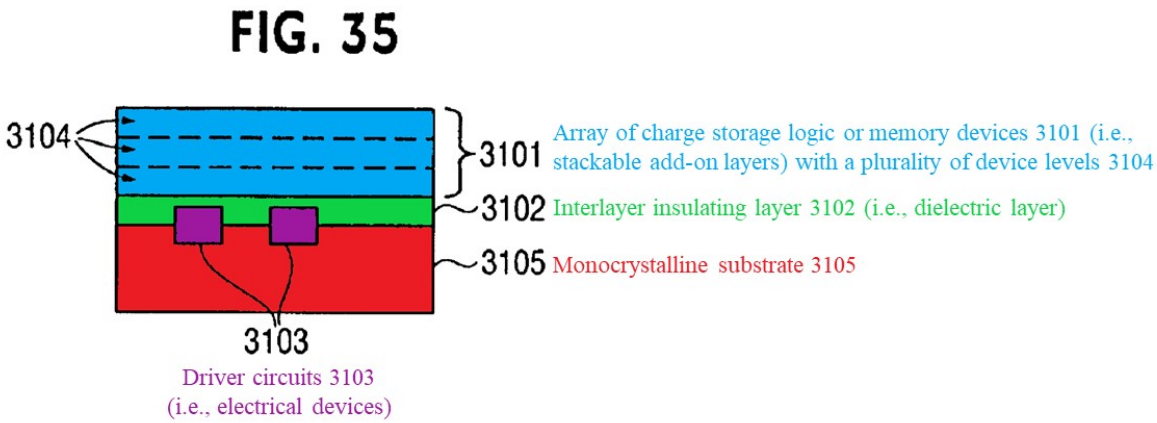
Ex-1007, Fig. 1A.

118. Lee further discloses:

> FIG. 35 [(annotated below)] schematically illustrates an array of charge storage logic or memory devices 3101 [(blue)] formed above an interlayer insulating layer 3102 [(green)] disposed above a monocrystalline substrate 3105 [(red)]. The array of charge storage logic or memory devices 3101 [(i.e., stackable add-on layers)] are thus arranged as a three dimensional monolithic array thin film transistors or diodes in amorphous or polysilicon layers. The array 3101 has a plurality of device levels 3104 [(blue)], preferably separated by interlayer insulating layers. The driver circuits 3103 [(purple)], such as sense amps and charge pumps are disposed in the monocrystalline substrate 3105, as CMOS or other transistors.

Ex-1007, 12:17-27; *see id.* 5:46-56.

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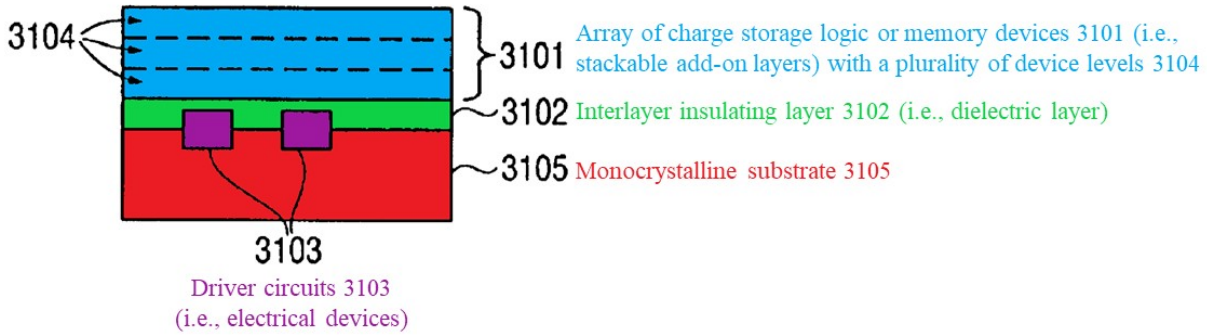
Id., Fig. 35. Because Lee discloses "a three dimensional nonvolatile memory array, comprising a plurality of vertically separated device levels," in which "each level compris[es] an array of TFT EEPROMs," the memory array is a stackable add-on layer having a plurality of vertically oriented semiconductor memory cells. *Id.* 5:46-49.

4. Element 13[c]: the stackable add-on layer being bonded to the dielectric layer; and

119. Lee discloses or renders obvious claim element 13[c]. Lee discloses that "FIG. 35 schematically illustrates an array of charge storage logic or memory devices 3101 [(i.e., stackable add-on layers)] formed above an interlayer insulating layer 3102 disposed above a monocrystalline substrate 3105…. The array 3101 has a plurality of device levels 3104, preferably separated by interlayer insulating layers." Ex-1007, 12:17-25. Thus, according to the preferred embodiment, each stackable add-on layer (e.g., each "array of charge storage logic or memory devices 3101") is bonded to a dielectric layer (e.g., "interlayer insulating layer").

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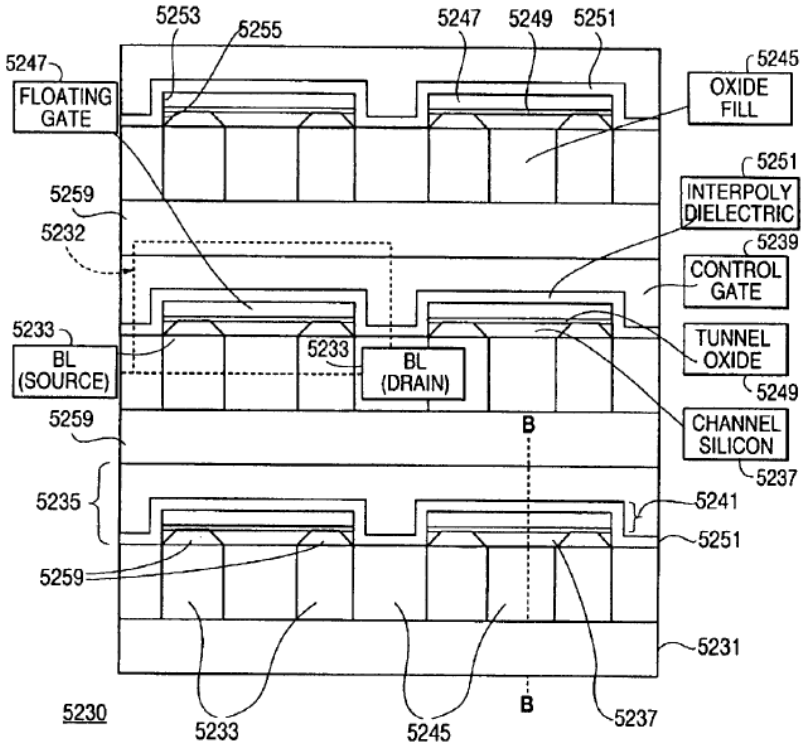
FIG. 35



Id., Fig. 35.

120. "In FIG. 83A [below], the flash memory array 5230 is preferably formed over a planarized interlayer insulating layer 5231, such as a CMP planarized silicon oxide layer." Ex-1007, 55:30-32.

FIG. 83A



Id., Fig. 83A. "Layer 5231 is formed over a substrate (not shown) as in the previous embodiments. Each device of the array (shown by dashed lines 5232 in FIG. 83A) is thus a TFT because it is formed over an insulating layer." *Id.* 55:32-36. Because the flash memory array 5230 (i.e., a stackable add-on layer) is formed over the planarized interlayer insulating layer 5231, a POSITA would have understood that the array is bonded to the planarized interlayer insulating layer 5231. *See supra* Section VIII.C.

121. Lee discloses:

> One method of improving device density is to arrange the devices in a monolithic three dimensional array of charge storage devices comprising a plurality of device levels. The term "monolithic" means that layers of each level of the array were directly deposited on the layers of each underlying level of the array. In contrast, two dimensional arrays may be formed separately and then packaged together to form a non-monolithic memory device.

Ex-1007, 11:24-31. Because the layers of the array are directly deposited on the layers of each underlying level, and the array is deposited on the interlayer insulating layer formed over a substrate, a POSITA would have understood that the array (i.e., a stackable add-on layer) is bonded to the interlayer insulating layer (i.e., a dielectric layer). *See supra* Section VIII.C.

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5. Element 13[d]: wherein the memory cells are nonvolatile memory cells having at least one transistor.

122. Lee discloses claim element 13[d]. Lee discloses:

> [A] three dimensional *nonvolatile memory array*, comprising a plurality of vertically separated device levels, *each level comprising an array of TFT EEPROMs*, *each TFT EEPROM comprising a channel, source and drain regions*, and a charge storage region adjacent to the channel, a plurality of bit line columns in each device level, each bit line contacting the source or the drain regions of the TFT EEPROMs, a plurality of word line rows in each device level, and at least one interlayer insulating layer located between the device levels.

Ex-1007, 5:46-56 (emphasis added); Ex-1009 at 27-29 (explaining that EEPROM is a form of nonvolatile memory). Lee also discloses "a three terminal *nonvolatile* stackable pillar memory device. A pillar memory device 100 in accordance with this embodiment of the present invention is broadly illustrated in FIG. 1A," which shows a transistor in which "[t]he first contact region 102, the body 104, and the second contact (source/drain) region 106 are each *vertically aligned with one another to form a pillar 108*." Ex-1007, 14:10-23 (emphasis added).

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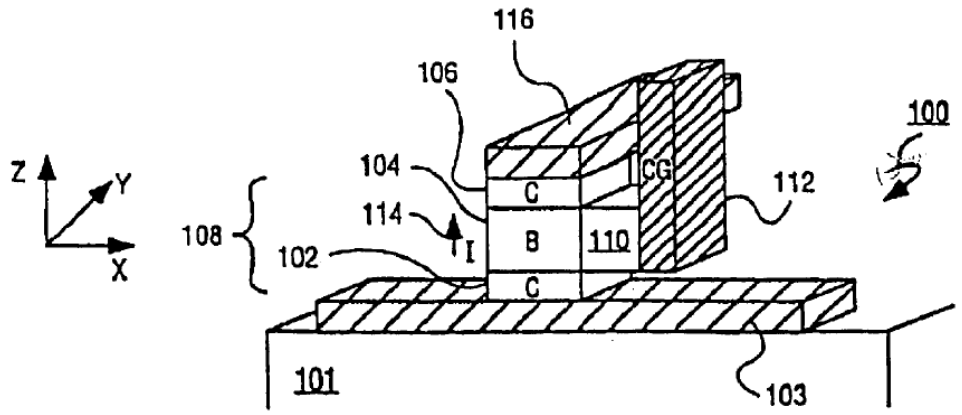


FIG. 1A

Ex-1007, Fig. 1A. Thus, Lee discloses a nonvolatile memory cell having at least one transistor.

6. Dependent Claim 14: The semiconductor memory structure of claim 13, wherein the vertically oriented semiconductor nonvolatile memory cell comprises a vertical transistor having a floating gate and a control gate on a SOI pillar.

123. Lee discloses dependent Claim 14. First, Lee's Figure 1A shows "a three terminal nonvolatile stackable pillar memory device [100]," that is vertically oriented and comprises a floating gate and control gate. Ex-1007, 14:10-13. Figure 1A illustrates a transistor in which "[t]he first contact region 102 [(pink)], the body 104 [(blue)], and the second contact (source/drain) region 106 [(orange)] are each *vertically aligned with one another to form a pillar 108*." *Id.* 14:10-23 (emphasis added).

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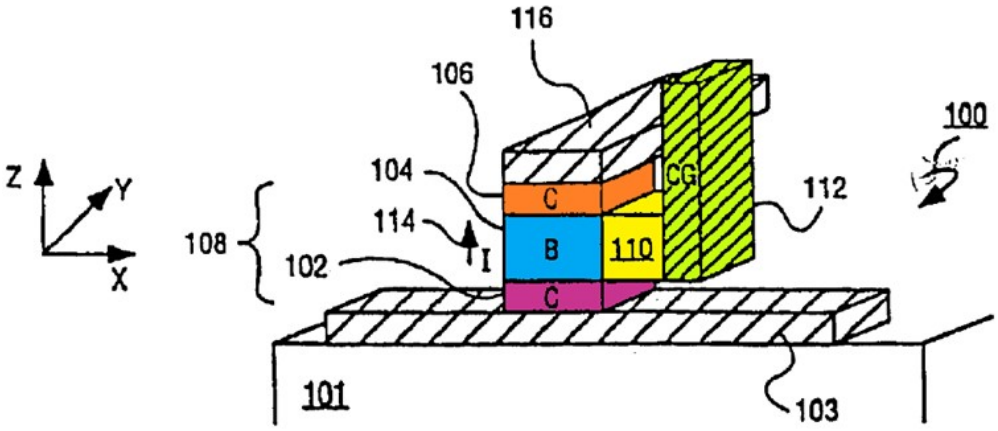


FIG. 1A

Id., Fig. 1A. Figure 1A further illustrates that:

> Adjacent to and in contact with body 104 is a charge storage medium 110 [(yellow)]. A control gate 112 [(green)] is formed adjacent to and in direct contact with charge storage medium 110. The control gate 112 and charge storage medium 110 are constructed so that they lie laterally adjacent to pillar 108 so that they may electrically communicate with pillar 108. The charge storage medium is the region that electrically screens the control gate and the channel region addressed by the control gate.

Id. 14:23-31.

124. Specifically, Lee's Figure 2 depicts "Pillar memory 200," which "has a charge storage medium 211 comprising a tunnel dielectric 212, a floating gate 214 [(yellow)], and a control gate dielectric 216…. Floating gate 214 comprises a conductor such as but not limited to doped silicon, such as N type silicon, or metal such as tungsten." Ex-1007, 15:41-49, Fig. 2; *see also id.* 18:19-30 ("[T]he floating

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gate need not necessarily be formed from a continuous conductive film of silicon or metal but can alternatively be formed from a plurality of…electrically isolated nanocrystals 602 as shown in FIG. 6."). Figure 2 also depicts "a control gate 218 [(blue)]…formed adjacent to and in direct contact with control gate dielectric 216. Control gate 218 is formed of a conductor such as but not limited to doped silicon or a metal such as tungsten." *Id.* 15:50-54.

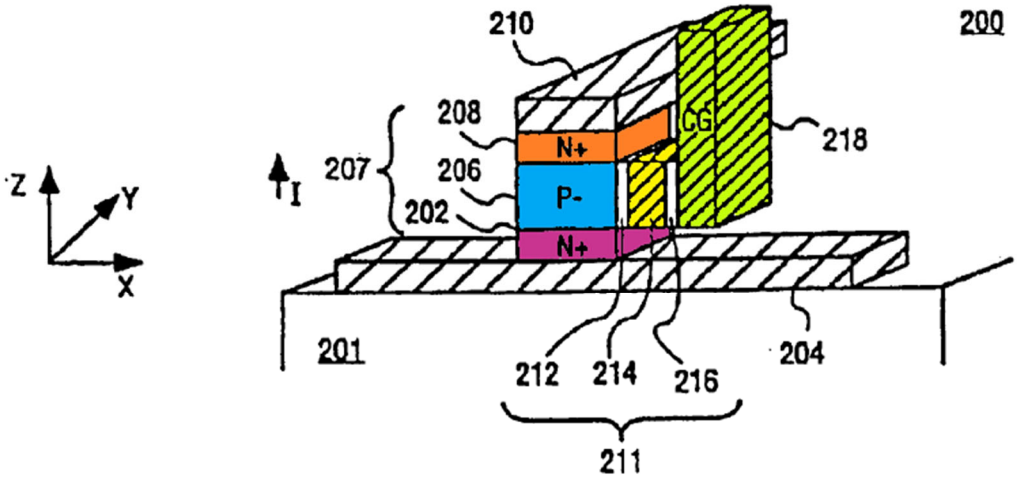


FIG. 2

Id., Fig. 2; *see also id.* 5:28-38, 5:57-65 (disclosing an EEPROM comprising a vertical transistor, floating gate, and control gate). Thus, Lee discloses a vertically oriented semiconductor nonvolatile memory cell comprising a vertical transistor having a floating gate and a control gate.

125. Second, Lee discloses a SOI pillar. Lee discloses "a substrate having an insulating surface (i.e., a Silicon-On-Insulator (SOI) substrate)…provided for the formation of the memory array. The substrate may comprise a semiconductor

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(i.e., silicon, GaAs, etc.) wafer covered with an insulating layer." Ex-1007, 31:41-45; Ex-1001, 4:45-5:7. Lee further discloses "a high temperature anneal step," which "gives the crystallized a-Si layer (i.e., a large grain polysilicon layer) performance characteristics similar to conventional SOI (silicon on insulator) CMOS technology." Ex-1007, 69:14-20. Accordingly, this "metal induced crystallization method may be used to recrystallize the active semiconductor layer of any of the above described devices." *Id.* 69:44-46. Thus, pillar TFTs, self-aligned TFTs, rail TFTs and diodes (i.e., an active semiconductor layer which contains one or more p-n junctions) of various configurations may be formed in the recrystallized a-Si or polysilicon." *Id.* 69:46-50. The '702 Patent recognizes that there are "a variety of ways" of forming Silicon-on-Insulator structures. Ex-1001, 4:45-47; *see supra* VIII.F. A POSITA would have understood that Lee's crystallization method is one method of forming a SOI structure that provides the same advantages and similar performance characteristics as "conventional SOI" technology. Ex-1001, 4:45-47; *see supra* VIII.F. In the alternative, because Lee compares its crystallization method to "conventional SOI," a POSITA would have found the use of "conventional SOI" as an obvious replacement to the disclosed crystallization method. Ex-1001, 4:45-47; *see supra* VIII.F. Thus, Lee discloses or renders obvious a vertically oriented semiconductor nonvolatile memory cell

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comprising a vertical transistor having a floating gate and a control gate on a SOI pillar.

7. Dependent Claim 15: The semiconductor memory structure of claim 13, wherein the vertically oriented semiconductor nonvolatile memory cell comprises a vertical transistor having a charge-trapping gate insulator and a gate on a SOI pillar.

126. Lee discloses dependent Claim 15. For reasons set forth above for Claim Element 13[d] and Claim 14, Lee discloses a "vertically oriented semiconductor nonvolatile memory cell" that comprises "a vertical transistor…on a SOI pillar." *See supra* Sections VII.C.5, VII.C.6.

127. Lee's Figure 7 shows that "N+ source/drain region 202, P type silicon body 206 and N+ source/drain region 208 are each substantially vertically aligned with one another to form [a] pillar." Ex-1007, 15:37-40. Moreover, Lee discloses, as an "alternative to the use of a dielectric isolated floating gate to store charge in the memory devices of the present invention, one can use a trapping layer formed in the dielectric stack 702 as shown in FIG. 7." *Id.* 18:61-64. Lee discloses:

> For example, the charge storage medium can be a dielectric stack 702 [(yellow)] comprising a first oxide layer 704 adjacent to the silicon body or channel, a nitride layer 706 adjacent to the first oxide layer and a second oxide layer 708 adjacent to the nitride layer and adjacent to the control gate 218 [(blue)].

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Id. 18:64-19:5. Lee's "FIG. 7 [(annotated below)] is an illustration of a pillar memory of an embodiment of the present invention having a charge trapping dielectric." *Id.* 8:40-42.

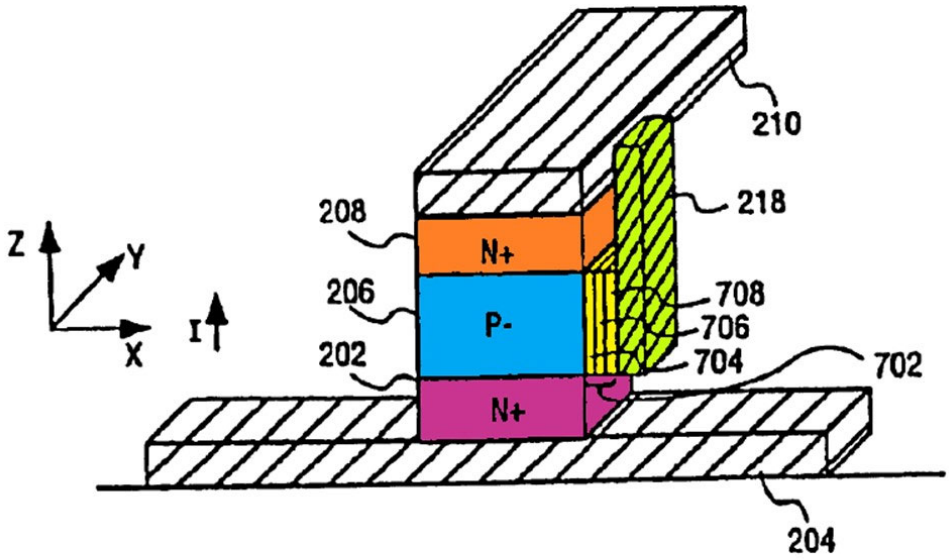


FIG. 7

Id., Fig. 7. Thus, Lee discloses a vertically oriented semiconductor nonvolatile memory cell comprising a vertical transistor having a charge-trapping gate insulator and a gate on a SOI pillar.

D. Ground 4: Claims 16 and 17 Are Obvious Over Lee in View of Endoh

1. A POSITA would have been motivated to combine Lee with Endoh

128. A POSITA would have been motivated to combine Lee with Endoh and would have a reasonable expectation of success in doing so and achieving their stated objectives, because they are both from the same field and relate to the same well-known issues. Lee and Endoh provide complementary solutions for arranging

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memory cells three-dimensionally to provide a high integration density. *Compare* Ex-1007, 11:18-32, *with* Ex-1006 ¶151. A POSITA seeking to increase the integration density of semiconductor memory devices, and specifically nonvolatile memory devices, would have known of and consulted these proposed solutions.

129. Lee discloses techniques for manufacturing semiconductor memory devices—including nonvolatile memory—in which the memory cells are arrayed three-dimensionally (i.e., vertically) to provide a high integration density. *See, e.g.*, Ex-1007, 5:28-56, 11:18-32, 13:32-38. Endoh provides additional well-known teachings of vertically oriented nonvolatile memory cells with a floating gate and control gate, or a charge-trapping gate insulator and gate, connected in series on a SOI pillar. *See, e.g.*, Ex-1006 ¶¶3, 6, 40, 151, 329, 662, 1138-72, 1205-07. A POSITA would have been motivated to modify Lee to obtain additional features and benefits from implementing the well-known teachings of NAND serial connections. *See, e.g.*, Ex-1006, ¶¶45, 46, 178 ("Hereinafter, are explained constructions in which a plurality of, for example, two memory cells are arranged in series on one island-like semiconductor layer."), 211, 223, 249, 250, 257, 263, 1206, Fig. 65; *see infra* Sections X.D.2-X.D.3.

130. For example, Endoh states, "double the capacity of the prior-art memory device can be obtained if memory transistors in two tiers are formed per semiconductor substrate pillar." Ex-1006 ¶1659. "Thereby, the cell area per bit

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decreases, the size of chips can be decreased and the production costs can be reduced." *Id.* Similarly, Lee explains, "the cost of memory and logic devices would be decreased if the device density was increased." Ex-1007, 11:18-20; *Dystar Textilfarben v. C.H. Patrick*, 464 F.3d at 1368. A POSITA would have had a reasonable expectation of success in combining the teachings of Lee and Endoh with no change in their respective functions because both references purport to solve these problems in similar and predictable ways, such as using the well-known teachings of vertical transistors and pillar structures. *See infra* Sections X.D.2-X.D.3.

2. Dependent Claim 16: The semiconductor memory structure of claim 13, wherein at least two nonvolatile memory cells are vertically oriented and serially connected together and formed with a first SOI pillar.

131. Lee in view of Endoh teaches dependent Claim 16. For reasons set forth above for Claim Element 13[d] and Claim 14, Lee discloses a "vertically oriented semiconductor nonvolatile memory cell" that comprises "a vertical transistor…on a SOI pillar." *See supra* Sections VII.C.5, VII.C.6.

132. Lee discloses "thin film transistors (TFTs) and diodes arranged in a pillar configuration (i.e., the vertical direction with respect to the substrate, where the length of the device is perpendicular to the substrate) and their method of fabrication." Ex-1007, 13:31-38. For example, Lee's Figure 12B "illustrate[s] a

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method of forming a common continuous film control gate between two or more levels of pillar memories" on a substrate (not shown). *Id.* 8:55-56.

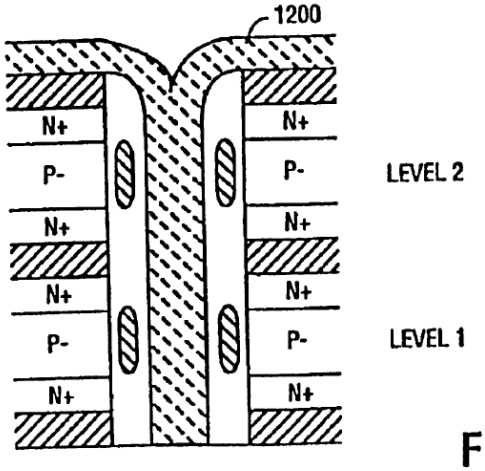


FIG. 12B

Id., Fig. 12B. Thus, Lee discloses "at least two nonvolatile memory cells are vertically oriented…and formed with a first SOI pillar."

133. Lee further discloses "a cross-point array of word lines and bit lines at a horizontal level and a method of making thereof." Ex-1007, 40:5-7. "This memory arrangement is known as the NOR Virtual Ground (NVG) Array (also referred to as VGA)." *Id.* 40:11-13. However, "the memory array may also be arranged in nonvolatile flash memory architectures other than VGA." *Id.* 40:13-15. As explained above in Section VII.B.4, "Two common types of flash memory array architectures are the 'NAND' and 'NOR' architectures." Ex-1012, 1:29-30. Although "[a] NAND array architecture also arranges its array of floating gate memory cells in a matrix," the key difference between a NOR and NAND arrangement is that in NAND, "each memory cell is not directly coupled to a

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column bit line by its drain." *Id.* 1:43-47. "Instead, the memory cells of the array are coupled together in series, source to drain, between a source line and a column bit line." *Id.* 1:47-49.

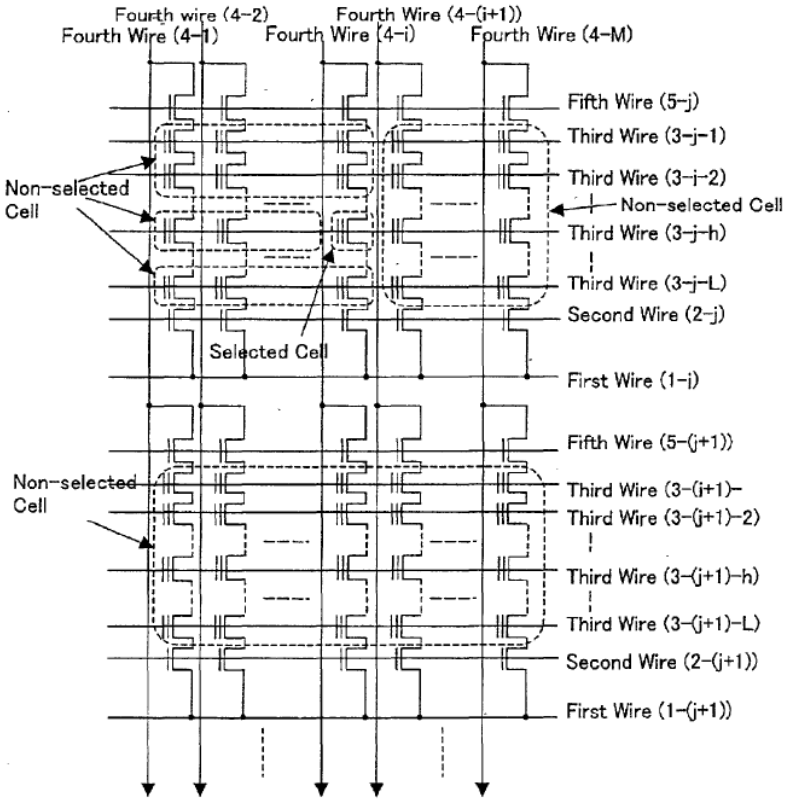
134. A POSITA would have found it obvious to use the NAND architecture because an entire NAND cell string uses only "one-half" of a bit line contact and "one-half" of a source line contact, which further increases the integration density of the memory design. Ex-1011, 2:59-65, 5:12-25 ("The primary purpose of using such a string structure is to reduce the number of contacts per memory cell…. The overall effect is a dramatic reduction in the chip area per memory cell."); *see supra* Section VIII.H. Thus, a POSITA would have found it obvious to modify Lee's pillar structure to use the NAND architecture and a serial connection as taught by Endoh. *See supra* Section VIII.H; *see also, e.g.*, Ex-1006 ¶1205-07.

135. For example, Endoh's Production Example 52 discloses "a semiconductor memory device [having] a structure in which…island-like semiconductor layers are formed in the form of *pillars* by selective epitaxial silicon growth." Ex-1006 ¶1206 (emphasis added). The EEPROM memory cell array of Production Example 52 comprises "two memory cells…arranged on each island-like semiconductor layer…[with] the transistors…*connected in series* along the island-like semiconductor layer, as shown in FIG. 1171 and FIG. 1172." *Id.*

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¶¶1206-07 (emphasis added), Figs. 1, 1171, 1172; *id.* ¶1074 (describing vertically oriented semiconductor memory cells); Ex-1009 at 27-29 (explaining that EEPROM is a form of nonvolatile memory). For example, "FIG. 65 shows the equivalent circuit diagram of the…memory cell array" having "a plurality of (e.g., M×N, wherein M and N are positive integers) island-like semiconductor layers." Ex-1006 ¶¶257-58.

Fig. 65



Id., Fig. 65. Thus, Lee in view of Endoh teaches at least two vertically oriented nonvolatile memory cells serially connected and formed on a SOI pillar.

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136. A POSITA would have been motivated to combine Lee with Endoh's teachings of a serial connection. *See supra* Section VIII.H. As explained above, NAND increases the integration density of a memory design by reducing the number of contacts per memory cell and, thus, reducing the chip area per memory cell. Ex-1011, 2:59-65, 5:12-25; *see supra* Section VIII.H. Because Lee recognizes "that the cost of memory and logic devices would be decreased if the device density was increased," an object of Lee is to "provide[] an ultra[-]dense matrix array of charge storage semiconductor devices which has an increased density and a lower cost." Ex-1007, 11:18-23. In addition, because NAND offers a higher integration density than a NOR architecture, there is a bigger market for NAND architecture. *See supra* Section VIII.H. Thus, a POSITA would have been motivated to modify Lee's pillar structures to use a serial connection as taught by Endoh.

137. Further, a POSITA would have had a reasonable expectation of success in modifying Lee to use a NAND serial connection because the "[t]wo common types of flash memory array architectures"—NAND and NOR—both "arrange[] its array of…memory cells in a matrix such that the gates of each…memory cell of the array are coupled by rows to word select lines." Ex-1012, 1:29-46. Because the NAND architecture was well known and nonvolatile memory cell structures in NAND were (and still are today) similar to those in NOR

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architecture, and Lee notes that alternative memory architectures can be used, a POSITA would have had a reasonable expectation of success in modifying Lee to use a NAND serial connection. *See supra* Section VIII.H; Ex-1007, 40:13-15. Thus, Lee in view of Endoh discloses or renders obvious at least two vertically oriented nonvolatile memory cells serially connected and formed with a SOI pillar.

3. Dependent Claim 17: The semiconductor memory structure of claim 16, wherein the at least two nonvolatile memory cells on the first SOI pillar are serially connected with an interconnect line disposed on a dielectric layer, to a nonvolatile memory cell formed with a second SOI pillar.

138. Lee in view of Endoh teaches dependent Claim 17. For reasons set forth above for Claim Element 13[d] and Claim 14, Lee discloses a "vertically oriented semiconductor nonvolatile memory cell" that comprises "a vertical transistor…on a SOI pillar." *See supra* Sections VII.C.5, VII.C.6.

139. Moreover, Lee in view of Endoh teaches at least two nonvolatile memory cells on a first SOI pillar connected serially to a nonvolatile memory cell formed on a second SOI pillar via an interconnect line disposed on a dielectric layer. For reasons set forth above for Claim 16, Lee in view of Endoh discloses or renders obvious at least two vertically oriented nonvolatile memory cells serially connected and formed with a SOI pillar. *See supra* Section VII.D.2. Because an entire NAND cell string uses only "one-half" of a bit line contact and "one-half" of a source line contact, a POSITA would have understood that connecting a plurality

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of pillars of memory cells would further increase the integration density of the memory design. *See supra* Sections VIII.H, VIII.I; Ex-1011, 2:59-65, 5:12-25 ("The primary purpose of using such a string structure is to reduce the number of contacts per memory cell…. The overall effect is a dramatic reduction in the chip area per memory cell.").

140. A POSITA would have recognized the constraints of connecting individual devices in series vertically and found it obvious to form a first pillar with several memory devices formed in series and then connect in series the first pillar to additional pillars each with several additional memory devices. *See supra* Sections VIII.H, VIII.I. A POSITA would have known that a NAND string generally comprises eight, sixteen, or thirty-two memory cells connected in series. *See supra* Sections VIII.H, VIII.I; *see also, e.g.*, Ex-1011 (illustrating an 8-cell NAND string); Ex-1013 (illustrating a 16-cell NAND string); Ex-1008, 3:8-16 (illustrating 16- and 32-cell NAND strings and explaining that the number of cells connected in series is expected to increase in the future). Further, because manufacturing and fabrication constraints generally limit the number of memory cells formed in the vertical direction, a POSITA would have found it obvious to connect multiple pillars in series to maximize the memory potential of the system. *See supra* Sections VIII.H, VIII.I. And a POSITA would have known that connecting multiple pillars in series requires interconnections between the pillars.

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See id. And a POSITA would have known that connecting multiple pillars in series requires interconnections between the pillars. *See id.* Without an interconnection between pillars, "serially connected" pillars would have required the memory cells to be part of a single string. *Id.*

141. For example, Lee illustrates vertically stacking two memory cells (Ex-1007, Figs. 12A-12B, 23A, 25A), whereas Endoh illustrates NAND strings having more than four memory cells connected in series (Ex-1006, Fig. 65). Thus, to form the NAND circuit shown in Endoh, a POSITA would have found it obvious to connect multiple pillars in series as disclosed by Lee. *See supra* Sections VIII.H, VIII.I. In addition, a POSITA would have found it obvious to connect the pillars using an interconnect line disposed on a dielectric layer to avoid shorting any of the devices. For example, Lee's Fig. 67 shows one such interconnect line (e.g., conductors 5080, 5082, 5084, 5086) disposed on a dielectric layer (insulating layer comprises regions 5088, 5090, 5092). Ex-1007, 49:4-33, Fig. 67. "Bit lines 5080, 5082, 5084, 5086 are preferably formed of N+ doped polysilicon although P+ doped polysilicon could also be used as could any suitable electrical conductor." *Id.* 49:11-14. "A deposition step is used to fill the regions 5088, 5090, 5092 between adjacent bit lines 5080, 5082, 5084, 5086 with a filler material. The filler material must be an electrical insulator. Again, silicon oxide is convenient although other materials could also be used." *Id.* 49:14-18. Also, as discussed above, one

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common method, as described by Watanabe, is first forming vias (or holes) on the dielectric layer, followed by depositing interconnect line (wires) in the vias. *See, e.g.*, Ex-1005; *see also* Ex-1030 (describing pillars of memory cells connected via common select gates). Thus, Lee in view of Endoh teaches two nonvolatile memory cells on a first SOI pillar connected serially to a nonvolatile memory cell formed on a second SOI pillar via an interconnect line disposed on a dielectric layer.

142. A POSITA would have been motivated to combine Lee with Endoh's teachings of a serial connection. *See supra* Sections VIII.H, VIII.I. Because Lee recognizes "that the cost of memory and logic devices would be decreased if the device density was increased," an object of Lee is to "provide[] an ultra[-]dense matrix array of charge storage semiconductor devices which has an increased density and a lower cost." Ex-1007, 11:18-23. In addition, because NAND offers a higher integration density than a NOR architecture, there is a bigger market for NAND architecture. *See supra* Sections VIII.H, VIII.I. Utilizing the high integration density of NAND, a POSITA can connect several memory cells and pillars in series to further increase the memory capacity in a single assembly. *Id.* Thus, a POSITA would have been motivated to connect a plurality of memory cells on a pillar in series and then connect a plurality of pillars in series, via interconnects, to further form an 8-, 16-, or 32-cell string. *See supra* Sections

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VIII.H, VIII.I. Because the NAND architecture was well known and nonvolatile memory cell structures in NAND were (and still are) similar to those in NOR architecture, and Lee notes that alternative memory architectures can be used, a POSITA would have had a reasonable expectation of success in modifying Lee to use a NAND serial connection. *See supra* Sections VIII.H, VIII.I; Ex-1007, 40:13-15.

E. Ground 5: Claims 13-15 Are Obvious Over Lee in View of Watanabe

143. To the extent Claim 13 is construed to exclude forming a "stackable add-on layer" through sequential deposition directly on a substrate, the subject matter of dependent Claims 13-15 is disclosed by Lee in view of Watanabe.

1. A POSITA would have been motivated to combine Lee with Watanabe

144. A POSITA would have been motivated to combine Lee with Watanabe and would have a reasonable expectation of success in doing so and achieving their stated objectives, because both references are from the same field and relate to the same well-known issues. Lee and Watanabe provide complementary solutions for arranging memory cells three-dimensionally to provide a high integration density. *Compare* Ex-1007, 11:18-32, *with* Ex-1005, 1:49-2:5. A POSITA seeking to increase the integration density of semiconductor

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memory devices, and specifically nonvolatile memory devices, would have known of and consulted these proposed solutions.

145. Lee discloses techniques for manufacturing semiconductor memory devices—including nonvolatile memory—in which the memory cells are arrayed three-dimensionally to provide a high integration density. *See, e.g.*, Ex-1007, 5:28-56, 11:18-32, 13:32-38. Similarly, Watanabe provides techniques for manufacturing any type of semiconductor memory device—including nonvolatile memory—in which the memory cells are arrayed three-dimensionally to provide a high integration density. *See, e.g.*, Ex-1005, 1:49-52, 2:41-55, 5:1-6:19. Although Lee discloses forming vertical memory devices through layer-by-layer sequential deposition on the substrate, a POSITA would have found it obvious to combine Lee and Watanabe because Watanabe discloses this same method as well as an alternative method of forming "stackable add-on layers" individually and then bonding them to the separately-fabricated substrate. *Compare* Ex-1007, 11:24-29, *with* Ex-1005, 5:1-6:14. Thus, a POSITA would have been motivated to modify Lee in view of Watanabe to use an alternative method of forming a stackable add-on layer and obtain the benefits associated with that method. *See* Ex-1005, 5:1-6:14; *see infra* Sections X.E.2-X.E.4.

146. These references acknowledge similar motivations for their respective teachings. For example, Lee explains, "the cost of memory and logic devices

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would be decreased if the device density was increased." Ex-1007, 11:18-20; *Dystar Textilfarben v. C.H. Patrick*, 464 F.3d at 1368. Similarly, Watanabe explains, "By virtue of such a 3-dimensional memory cell array, the integration density of the semiconductor memory device can be greatly increased." Ex-1005, 2:2-5. A POSITA would have had a reasonable expectation of success in combining the teachings of Lee and Watanabe with no change in their respective functions because both of these references purport to solve the same problems in similar and predictable ways, such as using the well-known teachings of vertical transistors and pillar structures. *See infra* Sections X.E.2-X.E.4. In addition, Watanabe discloses a benefit of using its "bonding method"—it "improves the accuracy of the wiring." Ex-1005, 5:64-6:3.

2. Elements 13[preamble], 13[a], and 13[d].

147. To the extent that the preamble of Claim 13 is limiting, Lee discloses the preamble. *See supra* Section VII.C.1; *see also supra* Section VII.A.1 (explaining that Watanabe discloses the preamble of Claim 13). In addition, Lee discloses Claim Elements 13[a] and 13[d]. *See supra* Sections VII.C.2, VII.C.5; *see also supra* Sections VII.A.2, VII.A.5 (explaining that Watanabe discloses Claim Elements 13[a] and 13[d]).

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3. Elements 13[b]/13[c]: a stackable add-on layer having a plurality of vertically oriented semiconductor memory cells; and the stackable add-on layer being bonded to the dielectric layer.

148. For reasons set forth above for Claim Elements 13[b] and 13[c], Lee and Watanabe both disclose "a stackable add-on layer having a plurality of vertically oriented semiconductor memory cells, and the stackable add-on layer being bonded to the dielectric layer." *See supra* Sections VII.C.3-VII.C.4, VII.A.3-VII.A.4.

149. To the extent Claim 13 is construed to exclude forming a "stackable add-on layer" through sequential deposition directly on a substrate, Lee in view of Watanabe discloses this limitation. Although Lee discloses forming vertically oriented memory devices through layer-by-layer sequential deposition on the substrate, a POSITA would have found it obvious to combine Lee and Watanabe because Watanabe discloses this same method as well as a "stacking method" of bonding completed "stackable add-on layers" (referred to as "planar members" in Watanabe) through high-temperature bonding. *Compare* Ex-1007, 11:24-29, *with* Ex-1005, 5:1-6:14; *see also supra* Section VIII.B. Watanabe explains that its "stacking method" forms wiring "for each planar member" individually, which "improves the accuracy of the wiring." Ex-1005, 6:1-3. In addition, Watanabe explains that its methods "provid[e] a semiconductor memory device with improved integration density and of a low interconnection wire resistance." *Id.*

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6:20-23. Thus, a POSITA would have been motivated to modify Lee in view of Watanabe to use its "stacking method" to form a stackable add-on layer and obtain the benefits associated with that method. *See* Ex-1005, 5:1-6:14; *see supra* Section VIII.B. Further, a POSITA would have had a reasonable expectation of success in combining Lee and Watanabe because Watanabe covers the method provided in Lee as well as an alternative method reaching the same objectives. *Compare* Ex-1007, 11:24-29, *with* Ex-1005, 5:1-6:14.

4. Dependent Claims 14-15.

150. As discussed above, Lee discloses dependent Claims 14 and 15. *See supra* Section VII.C.6-VII.C.7; *see also supra* Section VII.B.2-VII.B.3 (explaining that Watanabe in view of Endoh discloses dependent Claims 14-15).

F. Ground 6: Claims 16 and 17 Are Obvious Over Lee in View of Watanabe and Endoh

151. The subject matter of dependent Claims 16 and 17 is disclosed by Lee in view of Watanabe and Endoh. As discussed above, Lee in view of Endoh discloses Claims 16-17. *See supra* Section VII.D.2-VII.D.3; *see also supra* Section VII.B.4-VII.B.5 (explaining that Watanabe in view of Endoh discloses Claims 16-17).

152. A POSITA would have been motivated to combine Lee with Watanabe and Endoh and would have a reasonable expectation of success in doing so, because Lee, Watanabe, and Endoh provide complementary solutions for

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arranging memory cells—including nonvolatile memory—three-dimensionally to provide a high integration density. *See supra* Sections VII.B.1, VII.D.1, VII.E.1. As discussed above, a POSITA would have been motivated to modify Lee in view of Watanabe and Endoh to use an alternative method of forming a stackable add-on layer and obtain the additional features and benefits of implementing the well-known teachings of a charge-trapping gate insulator, SOI pillar, and serial connection. *See supra* Section VII.E.1. In addition, a POSITA would have had a reasonable expectation of success in combining Lee, Watanabe, and Endoh with no change in their respective functions because each of these references purport to solve the same problems in similar and predictable ways, such as using the well-known teachings of vertical transistors and pillar structures. *See id.*

XI. CONCLUSION

153. For at least these reasons, Claims 13-17 of the ’702 Patent are invalid over the prior art.

154. In signing this declaration, I understand that the declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I acknowledge that I may be subject to cross-examination in this case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for

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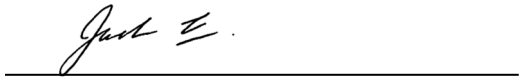
cross-examination within the United States during the time allotted for cross-examination.

155. I declare that all statements made herein of my knowledge are true, that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

156. I declare under penalty of perjury that the foregoing is true and correct.

Respectfully Submitted,

May 3, 2023



Dr. Jack C. Lee

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