

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
MICRON SEMICONDUCTOR PRODUCTS, INC., and
MICRON TECHNOLOGY TEXAS, LLC,
Petitioner

v.

BESANG INC.,
Patent Owner.

Case No. IPR2023-00900
U.S. Patent No. 7,378,702

**PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 7,378,702**

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LIST OF EXHIBITS¹

Ex-1001	U.S. Patent No. 7,378,702 (“the ’702 Patent”)
Ex-1002	Declaration of Dr. Jack C. Lee
Ex-1003	Curriculum Vitae of Dr. Jack C. Lee
Ex-1004	Prosecution History of U.S. Patent No. 7,378,702 (App. No. 10/934,270)
Ex-1005	U.S. Patent No. 5,091,762 (“Watanabe”)
Ex-1006	U.S. Patent Application Pub. No. US2002/0154556 (“Endoh”)
Ex-1007	U.S. Patent No. 6,881,994 (“Lee”)
Ex-1008	U.S. Patent No. 7,221,008 (“Matamis”)
Ex-1009	G. Groeseneken et al., <i>Basics of Nonvolatile Semiconductor Memory Devices</i> , in <i>Nonvolatile Semiconductor Memory Technology: A Comprehensive Guide to Understanding and Using NVSM Devices</i> (William D. Brown & Joe Brewer eds., 1997)
Ex-1010	Philip M. Sailer et al., <i>Creating 3D Circuits Using Transferred Films</i> , IEEE Circuits & Devices (1997)
Ex-1011	U.S. Patent No. 5,808,938 (“Tran”)
Ex-1012	U.S. Patent No. 6,982,905 (“Nguyen”)
Ex-1013	U.S. Patent No. 6,807,098 (“Jeong”)
Ex-1014	Kee-Ho Yu et al., <i>Real-Time Microvision System with Three-Dimensional Integration Structure</i> , IEEE Int’l Conference on Multisensor Fusion and Integration for Intelligent Sys. (1996)
Ex-1015	U.S. Patent No. 5,374,564 (“Bruel”)
Ex-1016	Horacio Mendez, <i>Silicon-on-Insulator: SOI Technology and Ecosystem – Emerging SOI Applications</i> , SOI Indus. Consortium (2009)
Ex-1017	U.S. District Courts – Combined Civil and Criminal Federal Court Management Statistics (Dec. 31, 2022), available at: https://www.uscourts.gov/statistics-reports/federal-court-management-statistics-december-2022

¹ Four-digit pin citations that begin with 0 are the page stamps added by Micron in the bottom right corner of the exhibits. All other pin citations are to original page, column, paragraph, or line numbers.

Ex-1018	T. Mikolajick et al., <i>The Future of Charge Trapping Memories</i> , 2007 IEEE Int'l Symposium on VLSI Tech., Sys. & Applications (2007)
Ex-1019	Complaint, <i>BeSang Inc. v. Micron Tech., Inc.</i> , No. 2:23-cv-00028 (E.D. Tex. Jan. 23, 2023)
Ex-1020	Jim Handy, <i>3D NAND: Benefits of Charge Traps over Floating Gates</i> , The Memory Guy Blog (Nov. 22, 2013)
Ex-1021	E. Bertagnolli et al., <i>ROS: An Extremely High Density MASK ROM Technology Based on Vertical Transistor Cells</i> , IEEE (1996)
Ex-1022	Tetsuo Endoh et al., <i>Novel Ultrahigh-Density Flash memory with A Stacked-Surrounding Gate Transistor (S-SGT) Structured Cell</i> , 50 IEEE Transactions on Electron Devices 945 (2003)
Ex-1023	F. Nemati & J.D. Plummer, <i>A Novel High Density, Low Voltage SRAM Cell with A Vertical NDR Device</i> , IEEE (1998)
Ex-1024	K.W. Lee et al., <i>Three-Dimensional Shared Memory Fabricated Using Wafer Stacking Technology</i> , IEEE (2000)
Ex-1025	<i>NAND vs. NOR Flash Memory</i> , Toshiba America Electronic Components, Inc. (2006)
Ex-1026	G.K. Celler & Sorin Crisoloveanu, <i>Frontiers of Silicon-on-Insulator</i> , 93 J. Applied Physics 4955 (2003)
Ex-1027	Timeline, Soitec, available at: https://www.soitec.com/en/company/soitec-activity/history (last visited Apr. 25, 2023)
Ex-1028	G. Shahidi et al., <i>Fabrication of CMOS on Ultrathin SOI Obtained by Epitaxial Lateral Overgrowth and Chemical-Mechanical Polishing</i> , IEEE (1991)
Ex-1029	MicroChemicals, <i>Further Processing of Silicon Wafers: SiO₂, Si₃N₄, Metallization, Epitaxy and Dicing</i> , available at: https://www.microchemicals.com/technical_information/silicon_wafer_sio2_si3n4_metallization_epitaxy_soi.pdf (last visited Apr. 28, 2023)
Ex-1030	Hiroshi Sakuraba et al., <i>New Three-Dimensional High-Density Stacked-Surrounding Gate Transistor (S-SGT) Flash Memory Architecture Using Self-Aligned Interconnection Fabrication Technology Without Photolithography Process for Tera-Bits and Beyond</i> , 43 Japanese J. Applied Physics 2217 (2004)

I. INTRODUCTION

Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas, LLC (collectively, “Petitioner”) request *inter partes* review (“IPR”) of Claims 13-17 of U.S. Patent No. 7,378,702 (“the ’702 Patent”) (Ex-1001), currently assigned to BeSang Inc. (“PO”).

II. MANDATORY NOTICES, STANDING, AND FEES

A. Mandatory Notices Under 37 C.F.R. §42.8

Real Parties-in-Interest: Petitioner identifies the following real parties-in-interest: Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas, LLC.

Related Matters: PO has asserted the ’702 Patent against the real parties-in-interest in *BeSang Inc. v. Micron Tech., Inc.*, No. 2:23-cv-00028 (E.D. Tex. Jan. 23, 2023).

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B. Grounds for Standing

Petitioner certifies that the '702 Patent is available for review, and Petitioner is not barred or estopped from requesting review.

C. Fee Authorization

The PTO is authorized to charge any fees due during this proceeding to Deposit Account No. 50-0639.

III. RELIEF REQUESTED

Petitioner requests cancellation of the challenged claims based on the following grounds:

Ground	Summary
1	Claim 13 is obvious over Watanabe (Ex-1005).
2	Claims 14-17 are obvious over Watanabe in view of Endoh (Ex-1006).
3	Claims 13-15 are obvious over Lee (Ex-1007).
4	Claims 16 and 17 are obvious over Lee in view of Endoh.

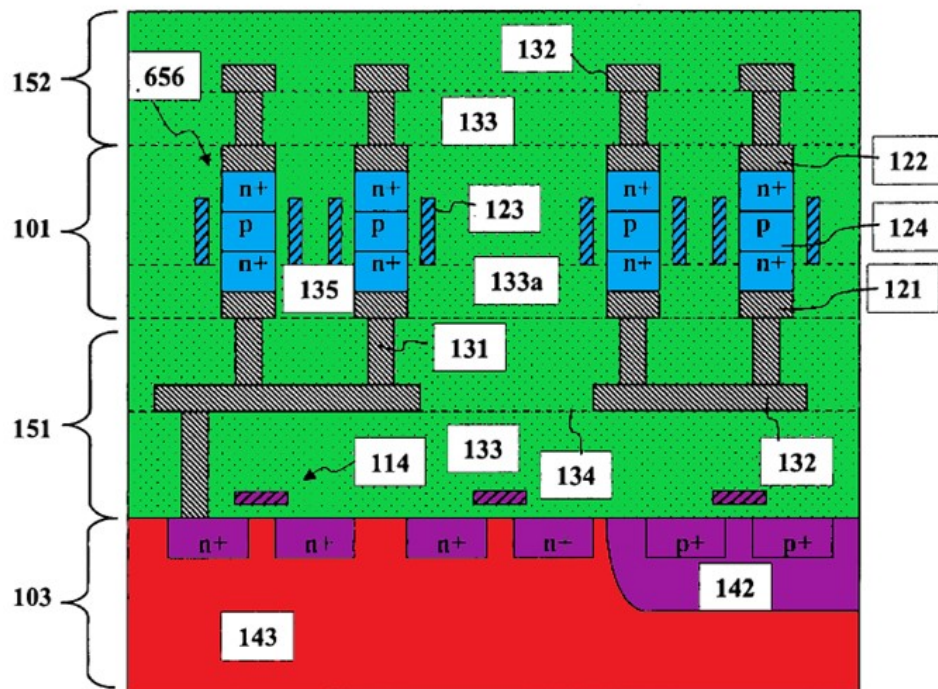
Ground	Summary
5	Claims 13-15 are obvious over Lee in view of Watanabe.
6	Claims 16 and 17 are obvious over Lee in view of Watanabe and Endoh.

IV. THE CHALLENGED PATENT

A. The '702 Patent

The '702 Patent discloses, “[v]ertically oriented semiconductor memory cells are added to a separately fabricated substrate that includes electrical devices and/or interconnect.” Ex-1001, code (57). “[T]he [’702 Patent] relates to a semiconductor substrate combined with a relatively thin add-on semiconductor layer in which various vertically oriented memory elements are fabricated.” *Id.* 1:16-19. Figure 1 [(annotated)] illustrates a “3-D integrated circuit arrangement,” “that includes a semiconductor substrate [(red)] having devices [(purple)] and/or interconnect structures fabricated thereon.” *Id.* 5:11-14. Base substrate 103 is bonded to “lower dielectric layer 151,” comprising “[i]nter-layer dielectric (ILD) layers 133 [(green)],” which are disposed above the devices (purple) formed in the substrate. *Id.* 5:31-33, 5:37-41.

Fig. 1



Id., Fig. 1.

The 3-D integrated circuit also has “at least one stackable add-on layer [(i.e., floating device layer (FLD) 101 with vertical memory devices 656 (blue) therein)], also having devices and/or interconnect, where the semiconductor substrate and the stackable add-on layer are stacked and bonded to each other.” Ex-1001, 5:14-17.

The '702 Patent describes forming “vertically oriented semiconductor memory cells” in a “stackable add-on layer,” which is then bonded to the semiconductor substrate. *Id.* 5:5-7, 5:11-41. The '702 Patent does not describe the stackable add-on layer as built by sequentially depositing one layer (i.e., thin film) at a time directly on the semiconductor substrate to form vertically oriented memory cells

within a multi-layer structure.² *See, e.g., id.*, code (57), 1:47-50, 4:45-57. The '702 Patent further describes that each stackable add-on layer 101 has “interlayer dielectric (ILD) layers 133 [(green)] disposed above and below.” *Id.* 3:51-54, 5:29-33, 5:11-17. Figure 1 also illustrates memory transistors (i.e., vertical memory devices 656 (blue)) with their source, channel, and drain regions oriented vertically or “substantially perpendicular to a major surface of a substrate.” *Id.* 4:7-9, Fig. 1.

The '702 Patent further discloses, “Dynamic Random Access Memory (DRAM) cells, Static Random Access Memory (SRAM) cells, nonvolatile memory cells, and similar structures may be formed in a stackable add-on layer for use in conjunction with the separately fabricated substrate.” Ex-1001, 2:4-9. Claims 1-12 are limited to DRAM and SRAM semiconductor memory structures, whereas Claims 13-17 recite nonvolatile semiconductor memory structures. “Vertical

² Petitioner believes that the intrinsic record does not support any interpretation of Claim 13 that encompasses forming the “stackable add-on layer” by sequential deposition directly on the substrate. In its Complaint, however, PO appears to interpret “a stackable add-on layer” to cover sequential deposition. *See* Ex-1019 ¶¶71-76. For purposes of this petition, this issue need not be resolved because the prior art discloses or renders obvious forming a “stackable add-on layer” under either interpretation.

nonvolatile memory has a form of either dual-gate with floating gate [and control gate] or single-gate with charge trapping gate insulator.” *Id.* 10:29-31; *see also id.* 9:65-10:1 (“FIG. 31 shows four vertical memory cells with serial connection of the four nonvolatile memory cells in the stackable add-on layer. The nonvolatile could be single-gate instead of dual-gates.”).

The ’702 Patent specifies that “vertical” “means substantially perpendicular to a major surface of a substrate.” Ex-1001, 4:7-9. “SOI layer...refer[s] to a relatively thin, single crystal portion of a semiconductor wafer that can be cleaved and bonded to another previously fabricated wafer, or similar type of substrate.” *Id.* 4:47-53. “[T]he SOI layer may be thought of as an attachment layer, or stackable add-on structure which is suitable for bonding to a semiconductor substrate already containing devices and/or interconnections.” *Id.* 4:53-57. In addition, the ’702 Patent states, “a FLD can be directly contacted by metal electrodes at top, bottom, and intermediate regions of the individual doped stack structures (i.e., pillar structures).” *Id.* 6:26-29.

B. Prosecution History of the ’702 Patent

The ’702 file history is submitted as Ex-1004. Although the Examiner’s single Non-Final Office Action objected to the claims based on indefiniteness and rejected the claims for obviousness-type double patenting, the Examiner did not issue any substantive rejections based on prior art and cited only a single reference

during prosecution. *See generally* Ex-1004; *id.* at 77 (citing only U.S. Patent No. 6,943,067).

C. Level of Ordinary Skill in the Art

A person of ordinary skill in the art at the relevant time (“POSITA”) would have had a bachelor’s degree in electrical engineering, computer engineering, or a related field, and at least two years of experience in the research, design, or development of semiconductor memory device structures, or the equivalent, with additional education substituting for experience and vice versa. Ex-1002 ¶34.

V. BRIEF DESCRIPTION OF THE APPLIED PRIOR ART REFERENCES

This petition presents three references, none of which were of record during prosecution. *See* Ex-1004.

A. Watanabe (Ex-1005)

Watanabe was filed December 14, 1990, and issued February 25, 1992. Ex-1005. Watanabe qualifies as prior art under at least pre-AIA §102(a)-(b), and (e). Ex-1002 ¶¶60-62.

Watanabe discloses, “an object of the present invention is to provide a semiconductor memory device in which memory cells are arrayed three-dimensionally, thereby providing a high integration density.” Ex-1005, 1:49-52. As shown in Figure 2A, Watanabe discloses stacks of vertically oriented semiconductor memory cells. *See id.* 3:12-15.

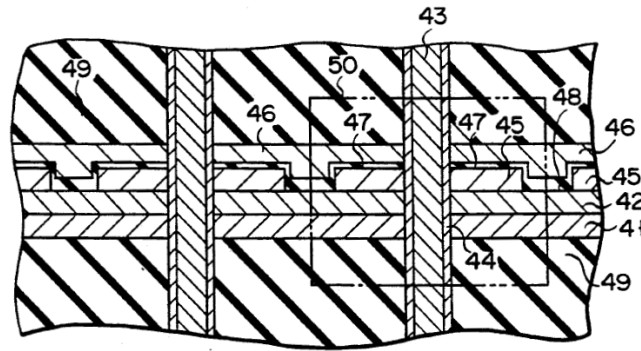


FIG. 2A

Id., Fig. 2A (showing one vertically oriented semiconductor memory cell consisting of layers 41 to 46).

Watanabe discloses two “method[s] used to manufacture a semiconductor memory device,” Ex-1005, 5:68-6:19, in which “[t]he memory cell...is applicable to any type of memory device i.e., a SRAM, a PROM, or a DRAM.” *Id.* 2:51-55 (including volatile and nonvolatile memory). “FIGS. 5A through 5E are sectional views showing a sequence of manufacturing process steps used in a method of manufacturing a semiconductor memory device according to the present invention, the method being called a ‘laminating method.’” *Id.* 2:26-30. “FIGS. 6A through 6D are sectional views showing a sequence of manufacturing process steps used in another method of manufacturing a semiconductor memory device according to the present invention, the method being called a ‘stacking method.’” *Id.* 5:31-35.

B. Endoh (Ex-1006)

Endoh was filed March 28, 2002, and published October 24, 2002. Ex-1006. Endoh qualifies as prior art under at least pre-AIA §102(a)-(b) and (e). Ex-1002 ¶¶63-64.

Endoh discloses pillar-form (i.e., vertical columnar-shaped) semiconductor memory devices and acknowledges that “[w]ith recent development in semiconductor technology, especially in micro-patterning techniques, the size reduction and the capacity increase of memory cells of EEPROM [(i.e., nonvolatile memory)] are rapidly progressing. Accordingly, it is important how large capacity can be ensured between the floating gate and the control gate.” Ex-1006 ¶6. Endoh describes a process to form “transistors...in a direction vertical to the substrate.” *Id.* ¶48. Endoh discloses forming semiconductor memory cells using “island-like semiconductor layers in a pillar form.” *Id.* ¶¶527, 582, 617, 643, 657, 664, 700, 1007, 1039, 1291, 1322, 1348, 1359, 1381, 1385, 1415, 1421; *see id.* ¶¶183, 198, 220, Figs. 1-2, 4. These “memory cells can be disposed in series in the direction vertical to the semiconductor substrate.” *Id.* ¶831. In addition, Endoh discloses a SOI substrate, *id.* ¶329, a floating gate structure, *id.* ¶¶1205-07, a charge-trapping gate insulator structure, *id.* ¶40, and a serial NAND connection. *Id.* ¶1206.

C. Lee (Ex-1007)

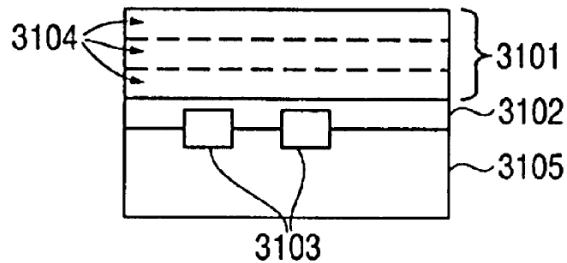
Lee was filed August 13, 2001, published March 7, 2002, and issued April 19, 2005. Ex-1007. Lee qualifies as prior art under at least pre-AIA §102(a)-(b), and (e). Ex-1002 ¶¶65-67.

Lee discloses “a monolithic three dimensional array of charge storage devices which includes a plurality of device levels.” Ex-1007, code (57). “First, [Lee discloses] a substrate having an insulating surface (i.e., a Silicon-On-Insulator (SOI) substrate)...for the formation of the memory array.” *Id.* 31:41-43. Lee discloses “a nonvolatile stackable pillar memory device and its method of fabrication,” and “a three dimensional nonvolatile memory array, comprising a plurality of vertically separated device levels, each level comprising an array of TFT [(thin film transistor)] EEPROMs.” *Id.* 5:28-56. Lee also discloses both “a dielectric isolated floating gate to store charge in the memory devices” and “a trapping layer formed in the dielectric stack,” such as an ONO stack. *Id.* 18:61-19:5.

Lee’s “FIG. 35 schematically illustrates an array of charge storage logic or memory devices 3101 formed above an interlayer insulating layer 3102 disposed above a monocrystalline substrate 3105.” Ex-1007, 12:17-20. “The array 3101 has a plurality of device levels 3104, preferably separated by interlayer insulating layers. The driver circuits 3103, such as sense amps and charge pumps, are

disposed in the monocrystalline substrate 3105, as CMOS or other transistors.” Ex-1007, 12:23-27. As illustrated, device levels 3104 are vertically oriented semiconductor memory cells.

FIG. 35



Id., Fig. 35.

VI. CLAIM CONSTRUCTION

Petitioner interprets the '702 Patent's claims according to the *Phillips* claim construction standard. 37 C.F.R. §42.100(b). The '702 Patent includes a "Terminology" section (Ex-1001, 4:5-5:17) that defines certain terms, including certain terms recited by Claims 13-17: "vertical" (*id.* 4:7-9), "device" (*id.* 4:28-32), and "SOI" (*id.* 4:45-5:7). In addition, the "Terminology" section defines "Vbias" (*id.* 4:10-16), "chips, semiconductor device, integrated circuit, LSI device, monolithic integrated circuit, ASIC, SoC, microelectronic device, and similar expressions" (*id.* 4:17-27), "FET" (*id.* 4:33-44), "high dielectric constant" (*id.* 5:8-10), and "3-D IC" (*id.* 5:11-17). To resolve the grounds presented herein, Petitioner does not believe that any term requires explicit construction because the prior art discloses the claim limitations in a manner consistent with the '702 Patent,

including its “Terminology” section.³ Ex-1002 ¶¶35-37.

VII. DETAILED EXPLANATION OF THE UNPATENTABILITY GROUNDS

The ’702 Patent contains 17 claims. This Petition challenges independent Claim 13 (requiring nonvolatile semiconductor memory structures) and Claims 14-17 that depend either directly or indirectly from Claim 13. The subject matter of the challenged claims is disclosed by the prior art as shown below. Ex-1002 ¶¶68.

A. Ground 1: Claim 13 Is Obvious Over Watanabe

As shown below, the subject matter of independent Claim 13 is disclosed by Watanabe alone. Ex-1002 ¶¶69-84.

³ Petitioner reserves all rights to raise claim construction and other arguments in district court. For example, Petitioner may demonstrate that “a stackable add-on layer having a plurality of vertically oriented semiconductor memory cells” and “the stackable add-on layer being bonded to the dielectric layer” require “vertically oriented semiconductor memory cells” to be formed in a separately fabricated “stackable add-on layer,” which is then “bonded [to] the dielectric layer.”

Petitioner will request leave to submit the district court’s claim construction when available.

1. Element 13[preamble]: A semiconductor memory structure, comprising:

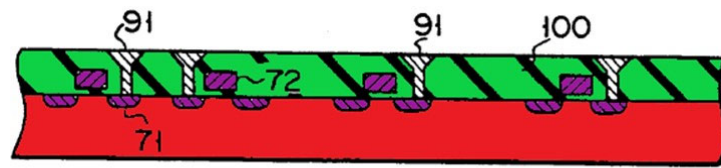
If Claim 13's preamble is limiting, Watanabe discloses the preamble. Ex-1002 ¶69. Watanabe states, "The present invention relates to a semiconductor memory device." Ex-1005, 1:10-11; *id.* 1:49-52 (providing "a semiconductor memory device in which memory cells are arrayed three-dimensionally, thereby providing a high integration density").

2. Element 13[a]: a substrate having electrical devices formed therein, and further having a dielectric layer disposed above the electrical devices;

Watanabe discloses two methods of manufacturing a semiconductor memory device—a "stacking method" and "laminating method"—each of which discloses this element. Ex-1005, 5:1-6:14.

Stacking Method: Watanabe's "stacking method [is] described with reference to FIGS. 6A through 6D." Ex-1005, 5:56-57. "As shown in FIG. 6A [(annotated below)], a peripheral circuit and transistors 71 and 72 [(purple)] are formed in the surface region of an Si substrate [(red)]. An insulating film 100 [(green)] is applied to the entire surface of the structure." *Id.* 5:58-61; *see also id.*, Fig. 2A, 3:53-54 ("The bottom insulating film 49 [shown in Figure 2A] is formed on an Si substrate, for example."); Ex-1002 ¶71 ("[C]omponents 72 are the gates of transistors 71 formed in the upper surface of the...substrate."). Thus, Watanabe discloses an "Si substrate" having electrical devices (transistor components 71 and

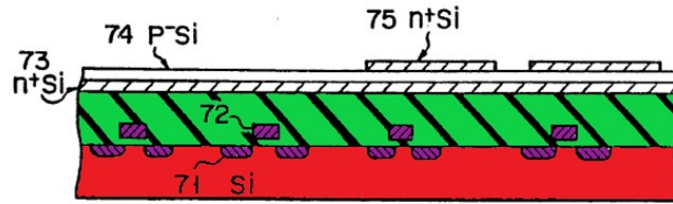
72) formed therein, and further having a dielectric layer (“insulating film 100”) disposed above the electrical devices. Ex-1002 ¶71. A POSITA would have recognized that transistor components 71 and 72 are field-effect transistors (FETs), which are examples of “devices” described by the ’702 Patent. Ex-1001, 4:28-32; Ex-1002 ¶71.



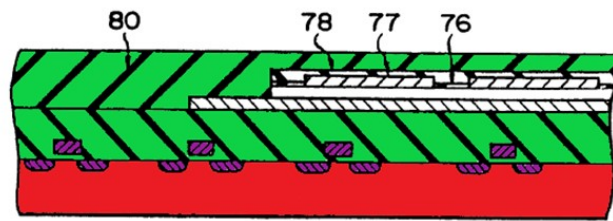
F I G. 6 A

Id., Fig. 6A.

Lamination Method: Watanabe’s “laminating method...[is] described[] with reference to FIGS. 5A through 5E.” Ex-1005, 5:8-10. “As is shown in FIG. 5A [(annotated)], insulating films [(green)] are formed on transistor components 71 [(purple)] formed in the upper surface of a silicon substrate [(red)].” *Id.* 5:11-13; Ex-1002 ¶72 (explaining the insulating film (green) is unlabeled in Figure 5A). A POSITA would have understood that the green region in Figure 5A is an insulating film (as stated in the description at 5:11-12, but mistakenly referenced using numeral 72 (instead of 100), which is correctly identified as a transistor in Figure 6A). Ex-1002 ¶72. Watanabe then teaches that “insulating film 80 [(green)] is layered over the resultant structure.” Ex-1005, 5:23-25; *see also id.*, Fig. 2A, 3:53-54.



F I G. 5A



F I G. 5B

Id., Figs. 5A-5B (annotated). Thus, Watanabe discloses a substrate having electrical devices formed therein, and further having a dielectric layer disposed above the electrical devices.

3. Element 13[b]: a stackable add-on layer having a plurality of vertically oriented semiconductor memory cells; and

Watanabe states, “an object of the present invention is to provide a semiconductor memory device in which memory cells are arrayed three-dimensionally, thereby providing a high integration density.” Ex-1005, 1:49-52. “In short, the present invention provides a 3-dimensional memory cell array in which memory cells [(green)] are respectively located at the cross points of a plurality of planar members (21, 22) [(orange)] arranged in parallel, and a plurality of wires (23, 26) pass through the planar members and are oriented orthogonal

thereto.” *Id.* 1:65-2:2. Thus, each planar member contains a plurality of semiconductor memory cells. Ex-1002 ¶73.

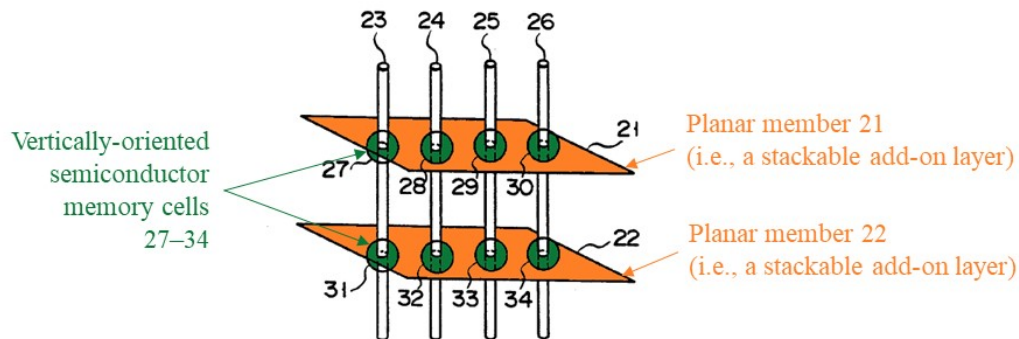


FIG. 1

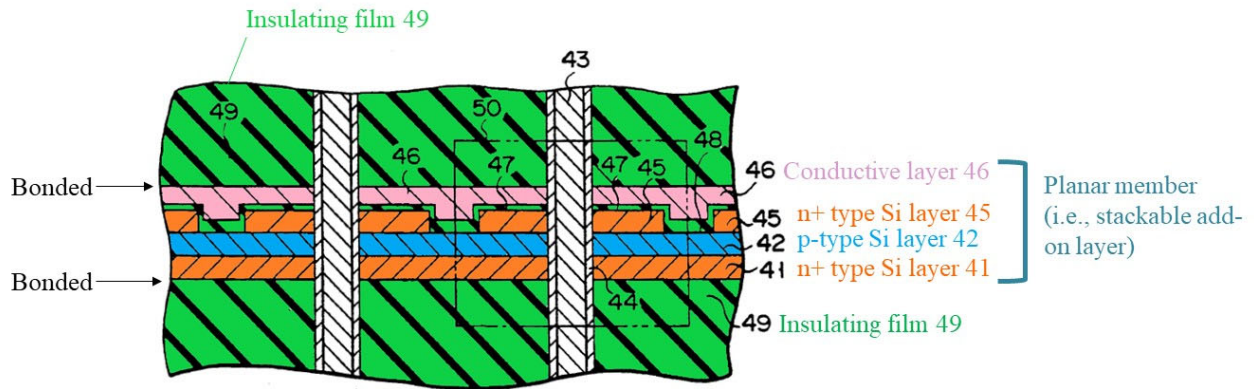
Id., Fig. 1 (annotated).

Further, Watanabe discloses, “FIG. 2A is a sectional view of a part of the semiconductor memory device shown in FIG. 1, and shows details of the memory device.” Ex-1005, 2:11-13. Referring to Fig. 2A (annotated):

reference numeral 41 designates a conductive planar member in the form of an N⁺ type silicon (Si) layer [(orange)], this layer serving as the source of the MOSFET. Numeral 42 indicates a p-type Si layer [(blue)], while numeral 43 represents a wire oriented orthogonal to the planar member..., and which is separated from at least the layers 41, 42, 45, and 46 by an insulating film 44. Numeral 45 denotes an n⁺ type Si layer [(orange)].... Preferably, a thick insulating film 48 fills the space between each of the layers 45, and is itself overlaid with a conductive layer 46. *At least two stack structures (two layers) [(i.e., two planar members)] each consisting of layers 41 to 46 are provided, which are insulated from*

each other by an insulting film 49 [(green)], and through which the wires 43 pass.

Id. 2:65-3:15 (emphasis added).



F I G. 2 A

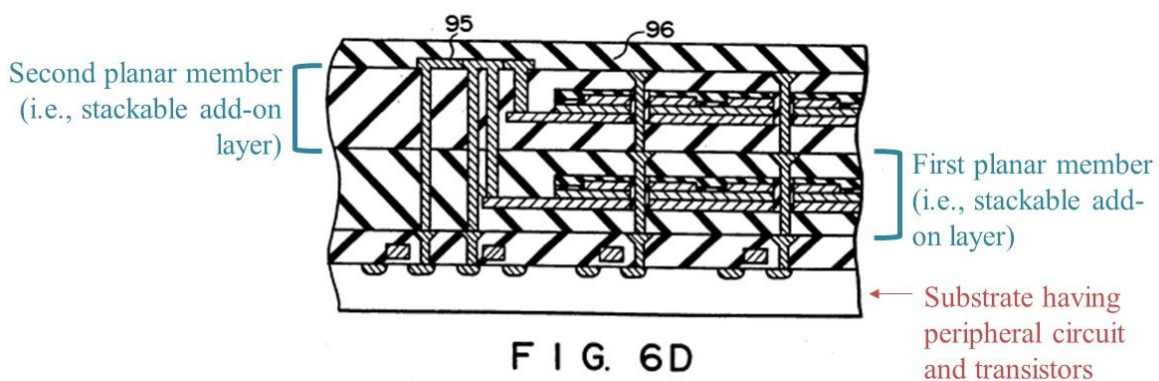
Id., Fig. 2A. Watanabe discloses the formation of semiconductor memory cells in which the transistors’ source-channel-drain elements (e.g., elements 41, 42, and 45 of Figure 2A) are arranged vertically—i.e., “substantially perpendicular to a major surface of the substrate.” Ex-1001, 4:7-9; Ex-1002 ¶74. Thus, Watanabe discloses vertically oriented semiconductor memory cells. Ex-1002 ¶74.

Watanabe further discloses two methods of manufacturing the stackable add-on layer having a plurality of vertically oriented semiconductor memory cells—a “stacking method” and “laminating method”—both of which disclose or render obvious this element. Ex-1005, 5:1-6:14.

Stacking Method: “FIGS. 6A through 6D are sectional views showing a sequence of manufacturing process steps used in another method of manufacturing

a semiconductor memory device,” Ex-1005, 2:31-35, “in which memory cells are arrayed three-dimensionally, thereby providing a high integration density.” *Id.* 1:50-52.

“As shown in FIG. 6B, a planar member is formed in a manner as shown in FIGS. 5A and 5B,” Ex-1005, 5:64-65, which shows insulating films formed on transistor components 71 formed in the upper surface of a silicon substrate, an n⁺ type Si layer 73, a p-type Si layer 74, an n⁺ type Si layer 75, an insulating film 76, capacitor insulating films 77, capacitor electrodes 78, and a first insulating film 80 layered over the resultant structure. *Id.* 5:8-26. “The process is repeated by the number of times equal to a necessary number of planar members. Finally, the planar members thus formed [(i.e., previously fabricated on separate substrates)] are stacked and wired” onto the substrate having the peripheral circuit and transistors. *Id.* 5:52-55.



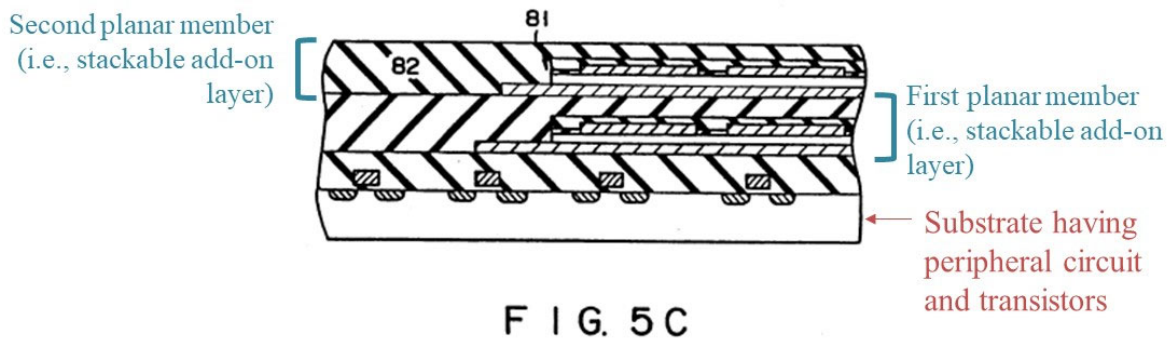
Id., Fig. 6D (annotated). Because each of Watanabe’s planar members contains a plurality of vertically oriented semiconductor memory cells, Watanabe’s stacking

method discloses a stackable add-on layer having a plurality of vertically oriented semiconductor memory cells. Ex-1002 ¶¶76-77.

Lamination Method: Watanabe's "laminating method" also discloses or renders obvious this element under PO's apparent construction (i.e., forming the "stackable add-on layer" by sequential deposition directly on the substrate). "FIGS. 5A through 5E are sectional views showing a sequence of manufacturing process steps used in a method of manufacturing a semiconductor memory device," Ex-1005, 2:26-30, "in which memory cells are arrayed three-dimensionally, thereby providing a high integration density." *Id.* 1:50-52. Watanabe's Figures 5A and 5B show the formation of planar members through sequential deposition of thin films on the substrate having the peripheral circuit and transistors. *See id.*, Figs. 5A-5B. Unlike Watanabe's "stacking method," the planar members in the "laminating method" are not previously fabricated on separate substrates. Figures 5A and 5B show insulating films formed on transistor components 71 formed in the upper surface of a silicon substrate, an n⁺ type Si layer 73, a p-type Si layer 74, an n⁺ type Si layer 75, an insulating film 76, capacitor insulating films 77, capacitor electrodes 78, and a first insulating film 80 layered over the resultant structure. *Id.* 5:8-26.

"As is shown in FIG. 5C [(annotated)], a second planar member 81 is formed over the first planar member, and a second insulating film 82 is laid

thereover, through a sequence of process steps similar to that used to form the first planar member.” Ex-1005, 5:27-32. “[A]ccording to the laminating method [illustrated in Figures 5A-5E], a desired number of planar members are first formed into a stack of planar members.” *Id.* 5:41-43.



Id., Fig. 5C. Because each of Watanabe’s planar members contains a plurality of vertically oriented semiconductor memory cells, Watanabe’s laminating method discloses a stackable add-on layer having a plurality of vertically oriented semiconductor memory cells. Ex-1005, Fig. 7 (showing the source, channel, and drain in a vertical orientation); Ex-1002 ¶¶78-79.

4. Element 13[c]: the stackable add-on layer being bonded to the dielectric layer; and

Watanabe discloses two methods of manufacturing a stackable add-on layer of a semiconductor memory device—a “stacking method” and “laminating method”—both of which disclose or render obvious this element. Ex-1005, 5:1-6:14. Under either method, Watanabe discloses “[a]t least two stack structures (two layers) [(i.e., two planar members)] each consisting of layers 41 to 46..., which are

insulated from each other by an insulating film 49, and through which the wires 43 pass.” *Id.* 3:9-15. Watanabe’s Figure 2A (annotated), illustrates one planar member consisting of layers 41 to 46 bonded to insulating film 49. Ex-1002 ¶80.

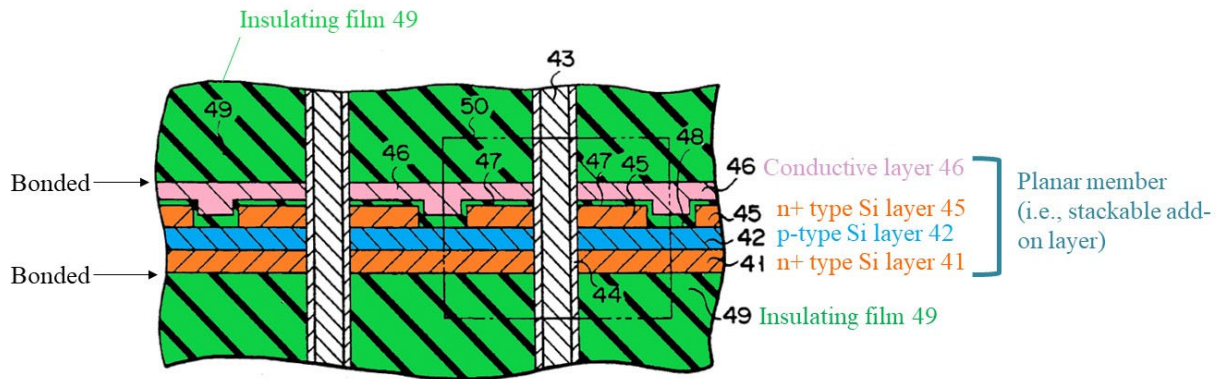
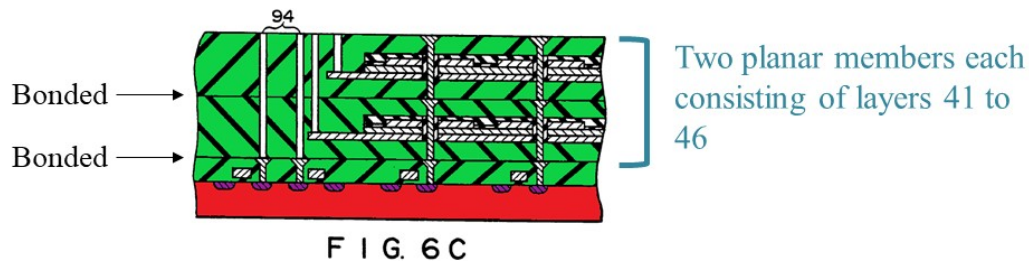


FIG. 2A

Ex-1005, Fig. 2A.

Stacking Method: In Watanabe's stacking method, the peripheral circuit of Figure 6A, including transistor components 71 with insulating film 100 formed thereover, is formed in the substrate in the same way as shown in Figure 5A. *See* Ex-1005, 5:64-65, 5:11-26. Next, "[a]s shown in FIG. 6B, a planar member is formed in a manner as shown in FIGS. 5A and 5B." *Id.* However, each planar member is formed on a *separate* substrate than the one shown in Figure 6A. *See id.*, Fig. 6B; Ex-1002 ¶81. It is only once the planar members are separately formed that they are stacked on the substrate of Figure 6A. Ex-1002 ¶82. "As shown in FIG. 6C [(annotated)], the planar members thus formed are bonded together. The bonding is made by thermal process of 900° to 1000° C." Ex-1005,

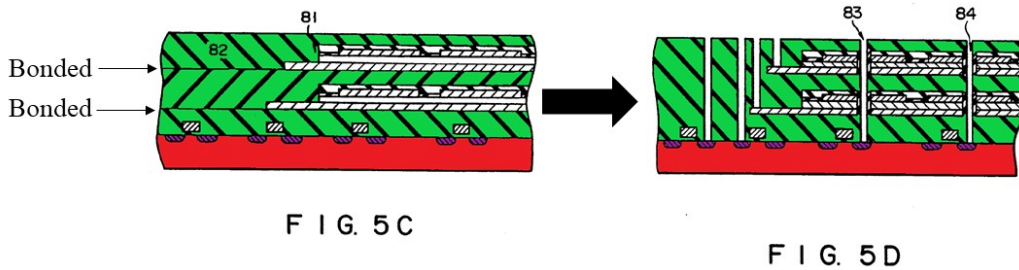
6:6-8.



Id., Fig. 6C. Thus, Watanabe’s “stacking method” discloses a stackable add-on layer being bonded to the dielectric layer. Ex-1002 ¶¶81-82.

Lamination Method: Watanabe’s “laminating method” also discloses or renders obvious this element under PO’s apparent construction (i.e., forming the “stackable add-on layer” by sequential deposition directly on the substrate). As shown in Figures 5A and 5B, Watanabe describes “the formation of a first planar member.” Ex-1005, 5:11-26. “As is shown in FIG. 5C, a second planar member 81 is formed over the first planar member, and a second insulating film 82 is laid thereover, through a sequence of process steps similar to that used to form the first planar member. If necessary, third and subsequent planar members may be formed in similar ways.” *Id.* 5:27-32. “In brief, according to the laminating method described above, a desired number of planar members are first formed into a stack of planar members.” *Id.* 5:41-43. Because this method is described as “laminating,” a POSITA would have understood that the planar members are bonded to the

dielectric layer to form one structure.⁴ Ex-1002 ¶82; *compare* Ex-1005, Fig. 5C, and Ex-1005, Fig. 5D. If the layers were not bonded together, then the system would not function. Ex-1002 ¶82.



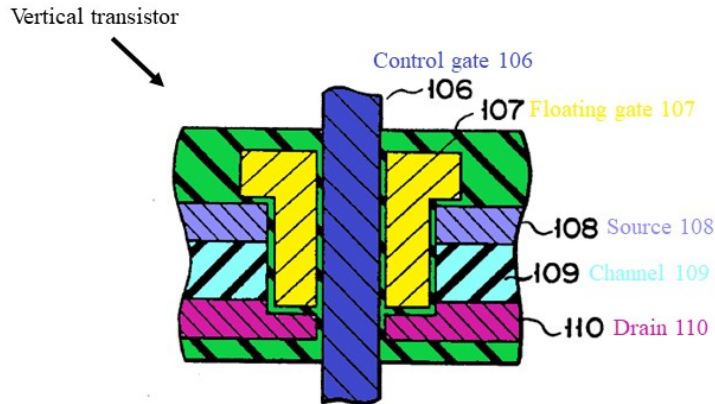
Ex-1005, Figs. 5C-5D (annotated). Thus, Watanabe’s “laminating method” also discloses or renders obvious a stackable add-on layer being bonded to the dielectric layer. Ex-1002 ¶82.

⁴ A POSITA would have understood that Watanabe’s “lamination method” forms planar members (i.e., stackable add-on layers) that are bonded to the dielectric layer. Ex-1002, n.3. The court has not yet construed the ’702 Patent, and Petitioner does not concede that the term “bonded” should be construed as broadly as PO asserts in its complaint. To the extent this limitation requires the “stackable add-on layer” be fabricated *separately* and subsequently “bonded [to] the dielectric layer,” this limitation is disclosed and rendered obvious by Watanabe’s “stacking method.” *Id.*

5. Element 13[d]: wherein the memory cells are nonvolatile memory cells having at least one transistor.

Watanabe discloses, “The memory cell of the present invention is applicable to any type of memory device i.e., a SRAM, PROM, or a DRAM.” Ex-1005, 2:51-53. A POSITA would have understood that PROM memory devices are nonvolatile. Ex-1002 ¶83.

Watanabe further discloses, “An application of the present invention into an EPROM is illustrated in FIG. 7. In the figure, a reference numeral 106 designates a control gate; 107 a floating gate; 108 a source; 109 a channel region; and 110 a drain region.” Ex-1005, 6:15-19. A POSITA would have understood that a source, channel, drain, floating gate, and control gate collectively form a nonvolatile memory cell transistor. Ex-1002 ¶84. “The electrically programmable read-only memory (EPROM) was, in fact, the first nonvolatile memory that could be electrically programmed by the user and that could be erased afterward.” Ex-1009 at 25.



F I G. 7

Ex-1005, Fig. 7 (annotated). Thus, Watanabe discloses that its invention is applicable to nonvolatile memory cells, which have at least one transistor. *See* Ex-1009 at 26 (“One floating gate transistor suffices to build an EPROM memory cell.”).

B. Ground 2: Claims 14-17 Are Obvious Over Watanabe in View of Endoh

As shown below, the subject matter of dependent Claims 14-17 is disclosed by Watanabe alone or in view of Endoh. Ex-1002 ¶¶85-114.

1. A POSITA would have been motivated to combine Watanabe with Endoh

A POSITA would have been motivated to combine Watanabe with Endoh and would have a reasonable expectation of success in doing so, because they are both from the same field and relate to the same well-known issues. Watanabe and Endoh provide complementary solutions for arranging memory cells three-dimensionally to provide a high integration density. *Compare* Ex-1005, 1:49-2:5,

with Ex-1006 ¶151. A POSITA seeking to increase the integration density of semiconductor memory devices, and specifically nonvolatile memory devices, would have known of and consulted these proposed solutions. Ex-1002 ¶85.

Watanabe discloses techniques for manufacturing any type of semiconductor memory device—including nonvolatile memory—in which the memory cells are arrayed three-dimensionally to provide a high integration density. *See, e.g.*, Ex-1005, 1:49-52, 2:41-55, 5:1-6:19. Endoh provides additional well-known teachings of vertically oriented nonvolatile memory cells with a floating gate and control gate, or a charge-trapping gate insulator and gate, connected in series on a SOI pillar. *See, e.g.*, Ex-1006 ¶¶3, 6, 40, 151, 329, 662, 1138-72, 1205-07. A POSITA would have been motivated to modify Watanabe to obtain additional features and benefits from implementing the well-known teachings of a charge-trapping gate insulator, SOI pillar, and serial connection. Ex-1002 ¶86; *see* Ex-1006 ¶¶40, 329, 223, 257-58; *see infra* Sections VII.B.2-VII.B.5.

Endoh discloses, “double the capacity of the prior-art memory device can be obtained if memory transistors in two tiers are formed per semiconductor substrate pillar.” Ex-1006 ¶1659. “Thereby, the cell area per bit decreases, the size of chips can be decreased and the production costs can be reduced.” *Id.* Similarly, Watanabe explains, “By virtue of such a 3-dimensional memory cell array, the integration density of the semiconductor memory device can be greatly increased.”

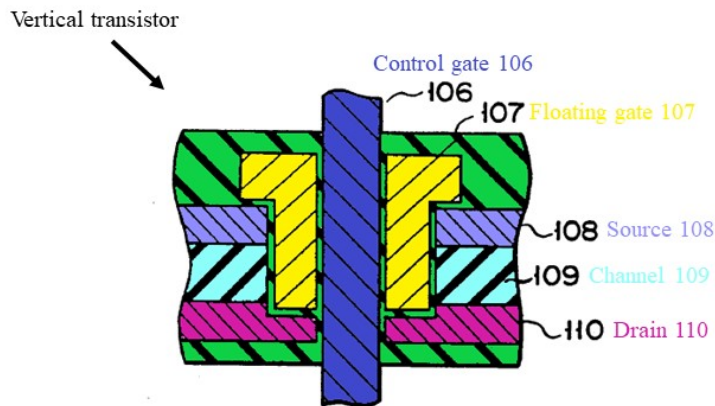
Ex-1005, 2:2-5; *Dystar Textilfarben GmbH & Co. Deutschland KG v. C.H. Patrick Co.*, 464 F.3d 1356, 1368 (Fed. Cir. 2006) (A motivation to combine exists when the “improvement” results in a product or process that is “stronger, cheaper, cleaner, faster, lighter, smaller, more durable, or more efficient.”). A POSITA would have had a reasonable expectation of success in achieving their objectives, e.g., arranging memory cells three-dimensionally to provide a high integration density, by combining the teachings of Watanabe and Endoh with no change in their respective functions because both references purport to solve these problems in similar and predictable ways, such as using the well-known teachings of vertical transistors and pillar structures. Ex-1002 ¶87; *see infra* Sections VII.B.2-VII.B.5.

2. Dependent Claim 14: wherein the vertically oriented semiconductor nonvolatile memory cell comprises a vertical transistor having a floating gate and a control gate on a SOI pillar.

Watanabe alone or in view of Endoh discloses dependent Claim 14 or renders it obvious with the knowledge of one of ordinary skill in the art. Ex-1002 ¶88. Watanabe discloses a vertically oriented semiconductor memory cell for reasons set forth above for Element 13[d]. *See supra* Section VII.A.5; Ex-1005, 2:65-3:15, Fig. 2A.

Watanabe further discloses a vertical transistor having a floating gate and a control gate. Watanabe discloses, “An application of the present invention into an EPROM is illustrated in FIG. 7. In the figure, a reference numeral 106 designates a

control gate; 107 a floating gate; 108 a source; 109 a channel region; and 110 a drain region.” Ex-1005, 6:15-19, Fig. 7; Ex-1009 at 25-26 (explaining EPROM is nonvolatile memory with at least one transistor).



F I G. 7

Id., Fig. 7 (annotated; showing the source, channel, and drain in a vertical orientation). Thus, Watanabe discloses a vertically oriented semiconductor nonvolatile memory cell comprising a vertical transistor having a floating gate and a control gate. Ex-1002 ¶¶89.

Second, Watanabe discloses or renders obvious forming a vertical transistor on a SOI pillar. As shown in Figure 7, Watanabe discloses a vertical transistor comprising a semiconductor layer (110, purple) on a planar insulator layer (green). *See* Ex-1005, 6:15-19, Fig. 7. Thus, a POSITA would have understood (or found it obvious) that Watanabe’s vertical transistor can be formed on a SOI pillar. Ex-1001, 4:45-47; Ex-1002 ¶¶90. Moreover, Watanabe discloses that the “n+ type Si

layer [45] is layered on an insulating film 49” and that “[w]hen a vapor phase epitaxial method is used for forming these layers, these may be successively formed by appropriately changing doping gases.” Ex-1005, 3:33-37, Figs. 2A-2B. A POSITA would have understood that epitaxial deposition is a common method of forming a SOI structure. Ex-1002 ¶90. Although Watanabe discloses the epitaxial method with respect to a MISFET DRAM device, Watanabe explains that DRAM is used as an example and “[t]he memory cell of the present invention is applicable to any type of memory device.” Ex-1005, 2:51-55. In addition, a POSITA would have understood that the vapor phase epitaxial method would apply equally to nonvolatile memory devices. Ex-1002 ¶90.

It was well known in the art that a vapor phase epitaxial method would result in a single crystal grown layer and that this method was one of the methods to form SOI structures. Ex-1002 ¶91. Because Watanabe discloses a vertical structure with “[a]t least two stack structures (two layers) [(i.e., two planar members)] each consisting of layers 41 to 46,” Ex-1005, 3:12-13, a POSITA would have understood that Watanabe discloses a SOI pillar structure or renders it obvious with the knowledge of one of ordinary skill in the art. *See id.*, Figs. 1, 2A (showing individual doped structures forming vertical pillars above insulator 49); Ex-1002 ¶91. Thus, Watanabe discloses or renders obvious a vertically oriented semiconductor nonvolatile memory cell comprising a vertical transistor having a

floating gate and a control gate on a SOI pillar. Ex-1002 ¶91.

To the extent that Watanabe alone does not disclose the vertically oriented semiconductor nonvolatile memory cell on a SOI pillar structure, Watanabe in view of Endoh renders this limitation obvious. Ex-1002 ¶92. Endoh discloses, “Not only a bulk substrate but also a SOI substrate, a multi-layered SOI substrate and the like may be used.” Ex-1006 ¶329. Endoh further discloses, “[t]he use of the SOI substrate as the semiconductor substrate can be applied to all the examples.” *Id.* ¶662. In addition, Endoh’s Production Example 52 discloses “a semiconductor memory device” in which “island-like semiconductor layers are formed in the form of *pillars* by selective epitaxial silicon growth.” *Id.* ¶1206 (emphasis added). The example also explains, “a plurality of *floating gates* are formed as the charge storage layers,” “two memory cells are arranged on each island-like semiconductor layer,” “and the transistors are connected in series along the island-like semiconductor layer.” *Id.* (emphasis added), Figs. 1, 1171-72 (illustrating “a memory cell array of an EEPROM”); Ex-1009 at 27-29, 32-33 (explaining EEPROM is a form of nonvolatile memory and “all floating gate memory cells have the same generic cell structure” with a floating gate and a control gate). Thus, Watanabe in view of Endoh discloses or renders obvious vertically oriented semiconductor nonvolatile memory cells comprising a vertical transistor having a floating gate and a control gate on a SOI pillar. Ex-1002 ¶92.

A POSITA would have been motivated to combine Watanabe with Endoh's teachings of a SOI pillar. Ex-1002 ¶93. A SOI substrate offers several advantages, including better wafer utilization, improved power consumption, and reduced temperature dependency. *See generally* Ex-1016. Because the silicon pillars of a SOI substrate are completely isolated, the structure has fewer problems with interference and cross-communication between the memory devices and the isolation prevents charge leakage through the substrate. Ex-1002 ¶93.

Further, stacking multiple layers using SOI wafers was well known in the art and offers the advantage of ease of manufacturing. Ex-1002 ¶94; *see, e.g.*, Ex-1014 at 834 (introducing "realistic 3D-LSI technology based on wafer bonding technique using micro-bumps." (footnote omitted)), Fig. 9 (showing the fabrication sequence of 3D-LSI); *see* Ex-1015; *see also* Ex-1010 at 27. For example, "[a]n SOI wafer consists of a bulk silicon substrate with a thin layer of single crystalline silicon on top, separated from the substrate by a silicon dioxide layer (buried oxide). The SOI wafer is used because the buried oxide layer acts as an etch-stop during a subsequent back-etch step." Ex-1010 at 28. Subsequently, the remaining thin SOI circuit can be transferred face down on the top of the bulk silicon wafer. This leads to the formation of a multilayer 3D-LSI circuit. Ex-1002 ¶94.

Accordingly, a POSITA would have understood and been motivated to harness the benefits of a SOI substrate, such as the one proposed in Endoh. Ex-

1002 ¶95. Because SOI wafers were well known and commercially available, a POSITA would have had a reasonable expectation of success in forming Watanabe's pillar on a SOI wafer, as described in Endoh. *Id.* ¶95 (noting commercial SOI wafer products sold for fabrication of integrated circuits (e.g., Soitec)); *see* Ex-1006 ¶¶329, 1207, 1074, Fig. 1171 (disclosing a vertically oriented semiconductor memory cell with a floating gate, which can be formed on a SOI substrate). Thus, a POSITA would have been motivated to form or procure a SOI wafer and use it as a substrate in forming Watanabe's pillar structure and would have had a reasonable expectation of success in doing so. Ex-1002 ¶95.

3. Dependent Claim 15: wherein the vertically oriented semiconductor nonvolatile memory cell comprises a vertical transistor having a charge-trapping gate insulator and a gate on a SOI pillar.

Watanabe in view of Endoh teaches dependent Claim 15. Ex-1002 ¶96. For reasons set forth above for Claim Element 13[d] and Claim 14, Watanabe discloses a “vertically oriented semiconductor nonvolatile memory cell” that comprises “a vertical transistor...on a SOI pillar.” *See supra* Sections VII.A.5, VII.B.2. In the alternative, Watanabe in view of Endoh renders obvious forming vertically oriented semiconductor nonvolatile memory cells on a SOI pillar structure. *See supra* Section VII.B.2; Ex-1002 ¶96.

Moreover, a vertical transistor having a charge-trapping gate insulator and a gate would have been obvious over Watanabe. Ex-1002 ¶97. A POSITA would

have known that “[t]he storage of charges in the gate insulator of a MOSFET can be realized in two ways, which has led to the subdivision of nonvolatile semiconductor memory devices into two main classes,” i.e., floating gate devices and charge-trapping devices. Ex-1009 at 5-6; Ex-1002 ¶97.

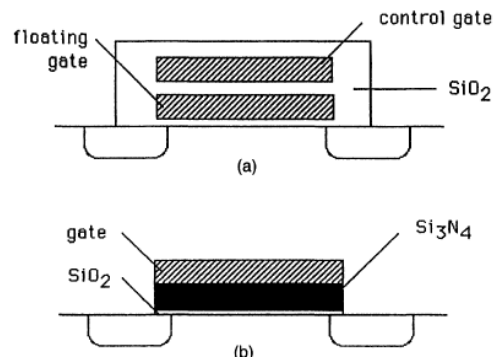


Figure 1.5 Two classes of nonvolatile semiconductor memory devices: (a) floating gate devices; (b) charge-trapping devices (MNOS device).

Id., Fig. 1.5. Although Watanabe’s EPROM has a floating gate, Ex-1005, 6:15-19, Fig. 7, a POSITA would have understood that a charge-trapping gate insulator could replace the floating gate and offer significant advantages. Ex-1002 ¶97.

“Since the early day[s] of nonvolatile memories in the late 1960s, charge trapping transistors using silicon nitride as a charge storage layer have been an alternative to floating gate devices in EPROM, EEPROM, and later Flash memories.” Ex-1018 at 0001. “In floating gate memories,...it becomes more and more difficult to maintain a high gate coupling ratio and keep floating gate interference limited.” *Id.* Accordingly, “the charge trapping concept has significant advantages when looking into advanced device structure like FinFET or 3D stacked memory cells.” *Id.* For example, “[r]eplacing the floating cell by a charge trapping cell with Fowler Nordheim programming and erase can help to scale

NAND devices further without significant changes in architecture and periphery circuits.” *Id.* at 0002-03 (explaining charge trapping memory cells can be stacked and share periphery circuits in a NAND architecture); *see also* Ex-1009 at 7 (noting charge trapping devices “in commercial high-density nonvolatile memory circuits”). In addition, in nitride or nanocrystal charge-trapping gate insulators, once the charge is trapped, the charge is far less likely to leak out as compared to a polysilicon layer, thus improving memory retention. Ex-1002 ¶98; *see, e.g.*, Ex-1009 at 7. Thus, a POSITA would have found it obvious to implement Watanabe with a charge-trapping gate insulator instead of a floating gate. Ex-1002 ¶98.

Alternatively, Watanabe in view of Endoh teaches “the storage of a charge...realized by a trap in a laminated insulating film” instead of “a floating gate structure.” Ex-1006 ¶40. Endoh’s Production Example 49 discloses:

a layered insulating film is used as the charge storage layer to realize charge storage by trapping in the layered insulating film, as shown in FIGS. 1067 to 1093 and FIGS. 1094 to 1120. FIGS. 1067 to 1093 and FIGS. 1094 to 1120 are sectional views taken on line A-A’ and line B-B’, respectively, in FIG. 12 which illustrates a memory cell array of an EEPROM.

Id. ¶1139 (emphasis added), Figs. 1, 1171-72; Ex-1009 at 6, 27-29, 47-49 (explaining EEPROM is a form of nonvolatile memory, which can be used with “[c]harge-trapping as well as floating gate cells,” and that charge-trapping devices

have a charge-trapping gate insulator and a gate). Endoh further discloses “a layered insulating film 1620” of MNOS or MONOS structure. Ex-1006 ¶1161; Ex-1009 at 6 (“In [charge-storage] devices, the charge is stored in discrete trapping centers of an appropriate dielectric layer.... The most successful device in this category is the MNOS device...structure.”). Thus, Watanabe in view of Endoh discloses or renders obvious vertically oriented semiconductor nonvolatile memory cells comprising a transistor having a charge-trapping gate insulator and a gate on a SOI pillar. Ex-1002 ¶99.

A POSITA would have been motivated to combine Watanabe with Endoh’s teachings of a transistor having a charge-trapping gate insulator and a gate on a SOI pillar. Ex-1002 ¶100. As explained above, a POSITA would have known that the storage of charges in the gate insulator of a MOSFET can be realized through a floating gate or charge-trapping device. Ex-1009 at 5-6. In addition, a POSITA would have known that charge trapping devices offer several advantages, including scalability for NAND devices without significant changes in architecture and periphery circuits. Ex-1002 ¶100; Ex-1018 at 0002-03; *see also* Ex-1009 at 7. Thus, a POSITA would have understood and been motivated to harness the benefits of a charge trapping device, such as the one proposed in Endoh for 3D stacked memory cells. Ex-1002 ¶100.

Because charge trapping devices were well known as the alternative to a

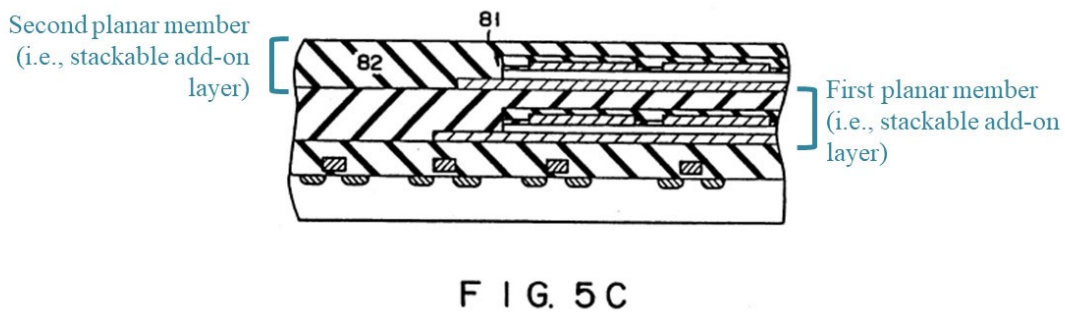
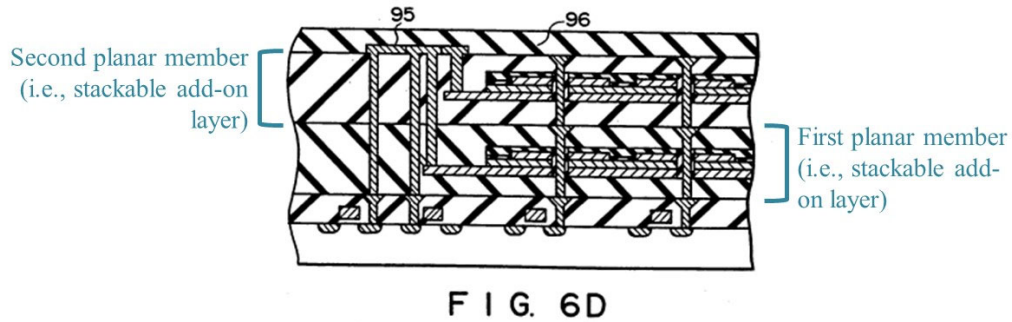
floating gate, a POSITA would have had a reasonable expectation of success in implementing Watanabe with a charge trapping device, as described in Endoh. Ex-1002 ¶101. In addition, a POSITA would have understood that “[c]harge-trapping as well as floating gate cells are used for EEPROM products,” and other nonvolatile memory cells, and that these components were interchangeable. Ex-1009 at 6, 27-29, 47-49; *see* Ex-1006 ¶¶329, 1160, Fig. 1091 (disclosing a vertically oriented semiconductor memory cell with a charge-trapping gate insulator, which can be formed on a SOI substrate). Thus, a POSITA would have been motivated to implement Watanabe with a charge-trapping gate insulator and would have had a reasonable expectation of success in doing so. Ex-1002 ¶101.

4. Dependent Claim 16: wherein at least two nonvolatile memory cells are vertically oriented and serially connected together and formed with a first SOI pillar.

Watanabe in view of Endoh teaches dependent Claim 16. Ex-1002 ¶102. For reasons set forth above for Claim Element 13[d] and Claim 14, Watanabe discloses a “vertically oriented semiconductor nonvolatile memory cell” that comprises “a vertical transistor...on a SOI pillar.” *See supra* Sections VII.A.5, VII.B.2. In the alternative, Watanabe in view of Endoh renders obvious forming vertically oriented semiconductor nonvolatile memory cell on a SOI pillar structure. *See supra* Section VII.B.2; Ex-1002 ¶102.

Moreover, Watanabe discloses at least two vertically oriented nonvolatile

memory cells. As shown in Figures 6D and 5C (annotated), Watanabe further discloses “[a]t least two stack structures (two layers) [(i.e., two planar members)] each consisting of layers 41 to 46.” Ex-1005, 3:12-13.



Id., Figs. 6D (showing two vertically oriented memory cells formed from Watanabe’s “stacking” method), 5C (showing two vertically oriented memory cells formed from Watanabe’s “laminating” method). Thus, Watanabe discloses at least two nonvolatile memory cells that are vertically oriented. Ex-1002 ¶103.

In addition, Watanabe in view of Endoh teaches at least two serially connected nonvolatile memory cells. “Two common types of flash memory array architectures are the ‘NAND’ and ‘NOR’ architectures, so called for the logical form in which the basic memory cell configuration or each is arranged.” Ex-1012,

1:29-32. In NOR architecture:

the floating gate memory cells of the memory array are arranged in a matrix. The gates of each floating gate memory cell of the array matrix are coupled by rows to word select lines and their drains are coupled to column bit lines. The NOR architecture floating gate memory array is accessed by a row decoder activating a row of floating gate memory cells by selecting the word select line coupled to their gates.

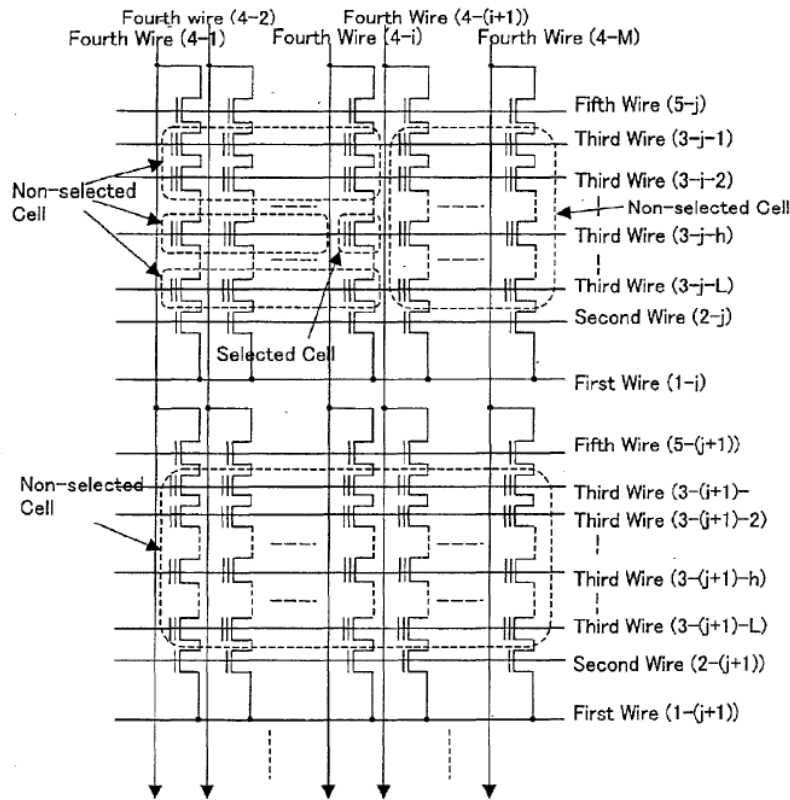
Id. 1:32-39. “A NAND array architecture also arranges its array of floating gate memory cells in a matrix.... However, each memory cell is not directly coupled to a column bit line by its drain.” *Id.* 1:43-47. “Instead, the memory cells of the array are coupled together in series, source to drain, between a source line and a column bit line.” *Id.* 1:47-49.

A POSITA would have found it obvious to use the NAND architecture because an entire NAND cell string uses only “one-half” of a bit line contact and “one-half” of a source line contact, which further increases the integration density of the memory design. Ex-1011, 2:59-65, 5:12-25 (“The primary purpose of using such a string structure is to reduce the number of contacts per memory cell.... The overall effect is a dramatic reduction in the chip area per memory cell.”); Ex-1002 ¶¶104-05. In addition, because NAND offers a higher integration density than a NOR architecture, there is a bigger market for NAND architecture. Ex-1002

¶¶104-05. Thus, a POSITA would have found it obvious to modify Watanabe's pillar structure to use the NAND architecture and a serial connection as taught by Endoh. Ex-1002 ¶¶104-05; *see, e.g.*, Ex-1006 ¶1205-07.

For example, Endoh's Production Example 52 discloses "a semiconductor memory device [having] a structure in which...island-like semiconductor layers are formed in the form of *pillars* by selective epitaxial silicon growth." Ex-1006 ¶1206 (emphasis added). The EEPROM memory cell array of Production Example 52 comprises "two memory cells...arranged on each island-like semiconductor layer...[with] the transistors...*connected in series* along the island-like semiconductor layer, as shown in FIG. 1171 and FIG. 1172." *Id.* ¶¶1206-07 (emphasis added), Figs. 1, 1171-72; *id.* ¶1074 (describing vertically oriented semiconductor memory cells); Ex-1009 at 27-29 (explaining EEPROM is a form of nonvolatile memory). "FIG. 65 shows the equivalent circuit diagram of the...memory cell array" having "a plurality of (e.g., $M \times N$...) island-like semiconductor layers." Ex-1006 ¶¶257-58.

Fig. 65



Id., Fig. 65. Thus, Watanabe in view of Endoh teaches at least two vertically oriented nonvolatile memory cells serially connected and formed on a SOI pillar. Ex-1002 ¶106.

A POSITA would have been motivated to combine Watanabe with Endoh’s teachings of a serial connection. Ex-1002 ¶107. As explained above, NAND increases the integration density of a memory design by reducing the number of contacts per memory cell and, thus, reducing the chip area per memory cell. Ex-1011, 2:59-65, 5:12-25; Ex-1002 ¶107. Because an object of Watanabe “is to provide a semiconductor memory device...providing a high integration density,” a

POSITA would have been motivated to modify Watanabe's pillar structures to use a serial connection as taught by Endoh.

Further, a POSITA would have had a reasonable expectation of success in modifying Watanabe to use a NAND serial connection because the "[t]wo common types of flash memory array architectures"—NAND and NOR—both "arrange[] its array of...memory cells in a matrix such that the gates of each...memory cell of the array are coupled by rows to word select lines." Ex-1012, 1:29-46. Because the NAND architecture was well known and nonvolatile memory cell structures in NAND were (and still are today) similar to those in NOR architecture, a POSITA would have had a reasonable expectation of success in modifying Watanabe to use a NAND serial connection. Ex-1002 ¶108. Thus, Watanabe in view of Endoh discloses or renders obvious at least two vertically oriented nonvolatile memory cells serially connected and formed with a SOI pillar. Ex-1002 ¶108.

5. Dependent Claim 17: wherein the at least two nonvolatile memory cells on the first SOI pillar are serially connected with an interconnect line disposed on a dielectric layer, to a nonvolatile memory cell formed with a second SOI pillar.

Watanabe in view of Endoh teaches dependent Claim 17. Ex-1002 ¶109. For reasons set forth above for Claim Element 13[d] and Claim 14, Watanabe discloses a "vertically oriented semiconductor nonvolatile memory cell" that comprises "a vertical transistor...on a SOI pillar." *See supra* Sections VII.A.5, VII.B.2. In the alternative, Watanabe in view of Endoh renders obvious forming vertically

oriented semiconductor nonvolatile memory cell on a SOI pillar structure. *See supra* Section VII.B.2; Ex-1002 ¶109.

Moreover, Watanabe in view of Endoh teaches at least two nonvolatile memory cells on a first SOI pillar connected serially to a nonvolatile memory cell formed on a second SOI pillar via an interconnect line disposed on a dielectric layer. For reasons set forth above for Claim 16, Watanabe in view of Endoh discloses or renders obvious at least two vertically oriented nonvolatile memory cells serially connected and formed with a SOI pillar. *See supra* Section VII.B.4. Because an entire NAND cell string uses only “one-half” of a bit line contact and “one-half” of a source line contact, a POSITA would have understood that connecting a plurality of pillars of memory cells would further increase the integration density of the memory design. Ex-1011, 2:59-65, 5:12-25; Ex-1002 ¶110.

A POSITA would have recognized the constraints of connecting individual devices in series vertically and found it obvious to form a first pillar with several memory devices formed in series and then connect in series the first pillar to additional pillars each with additional memory devices. Ex-1002 ¶111. A POSITA would have known that a NAND string generally comprises eight, sixteen, or thirty-two memory cells connected in series. Ex-1002 ¶111; *see, e.g.*, Ex-1011 (illustrating an 8-cell NAND string); Ex-1013 (illustrating a 16-cell NAND string);

Ex-1008, 3:8-16 (illustrating 16- and 32-cell NAND strings and explaining the number of cells connected in series is expected to increase in the future). Further, because manufacturing and fabrication constraints generally limit the number of memory cells formed in the vertical direction, a POSITA would have found it obvious to connect multiple pillars in series to maximize the memory potential of the system. Ex-1002 ¶111. However, a POSITA would have known that connecting multiple pillars in series requires interconnections between the pillars. *Id.* Without an interconnection between pillars, “serially connected” pillars would have required the memory cells to be part of a single string. *Id.*

For example, Watanabe illustrates vertically stacking two memory cells (Ex-1005, Figs. 5E, 6D), whereas Endoh illustrates NAND strings having more than four memory cells connected in series (Ex-1006, Fig. 65). Thus, to form the NAND circuit shown in Endoh, a POSITA would have found it obvious to connect multiple pillars in series as disclosed by Watanabe. Ex-1002 ¶112. In addition, a POSITA would have found it obvious to connect the pillars using an interconnect line disposed on a dielectric layer to avoid shorting any of the devices. *Id.* ¶112. One common method, as described by Watanabe, is first forming vias (or holes) on the dielectric layer, followed by depositing interconnect line (wires) in the vias. Ex-1002 ¶112; *see, e.g.*, Ex-1005. Indeed, Watanabe discloses forming interconnect lines on a dielectric layer. *See, e.g.*, Ex-1005, Fig. 5E (interconnect

85), Fig. 6D (interconnect 95); *see also* Ex-1030 (describing pillars of memory cells connected via common select gates). Thus, Watanabe in view of Endoh teaches two nonvolatile memory cells on a first SOI pillar connected serially to a nonvolatile memory cell formed on a second SOI pillar via an interconnect line disposed on a dielectric layer. Ex-1002 ¶112.

A POSITA would have been motivated to combine Watanabe with Endoh's teachings of a serial connection. Ex-1002 ¶113. An object of Watanabe "is to provide a semiconductor memory device...providing a high integration density." Ex-10052, 1:49-52. Because NAND offers a higher integration density than a NOR architecture, there is a bigger market for NAND architecture. Ex-1002 ¶113. Utilizing the high integration density of NAND, a POSITA can connect several memory cells and pillars in series to further increase the memory capacity in a single assembly. Ex-1002 ¶113. Thus, a POSITA would have been motivated to connect a plurality of memory cells on a pillar in series and then connect a plurality of pillars in series, via interconnects, to further form an 8-, 16-, or 32-cell string. Ex-1002 ¶113.

Further, a POSITA would have had a reasonable expectation of success in modifying Watanabe to use a NAND serial connection between memory cells on a pillar and between pillars because the "[t]wo common types of flash memory array architectures"—NAND and NOR architectures—both "arrange its array

of...memory cells in a matrix such that the gates of each...memory cell of the array are coupled by rows to word select lines.” Ex-1012, 1:29-46. “However each memory cell [of a NAND architecture] is not directly coupled to a column bit line by its drain. Instead, the memory cells of the array are coupled together in series, source to drain, between a source line and a column bit line.” *Id.* 1:46-49. Because the NAND architecture was well known and nonvolatile memory cell structures in NAND were (and still are today) similar to those in NOR architecture, a POSITA would have had a reasonable expectation of success in modifying Watanabe to use a NAND serial connection. Ex-1002 ¶114.

C. Ground 3: Claims 13-15 Are Obvious Over Lee

As shown below, the subject matter of independent Claim 13 and dependent Claims 14 and 15 is disclosed by Lee alone. Ex-1002 ¶115-27.

1. Element 13[preamble]: A semiconductor memory structure, comprising:

If Claim 13’s preamble is limiting, Lee discloses the preamble. Ex-1002 ¶115. Lee states, “The present invention relates to semiconductor devices in general.” Ex-1007, 1:25-26. A “preferred embodiment of the present invention provides a nonvolatile stackable pillar memory device and its method of fabrication.” *Id.* 5:28-38; *see id.* 12:17-27.

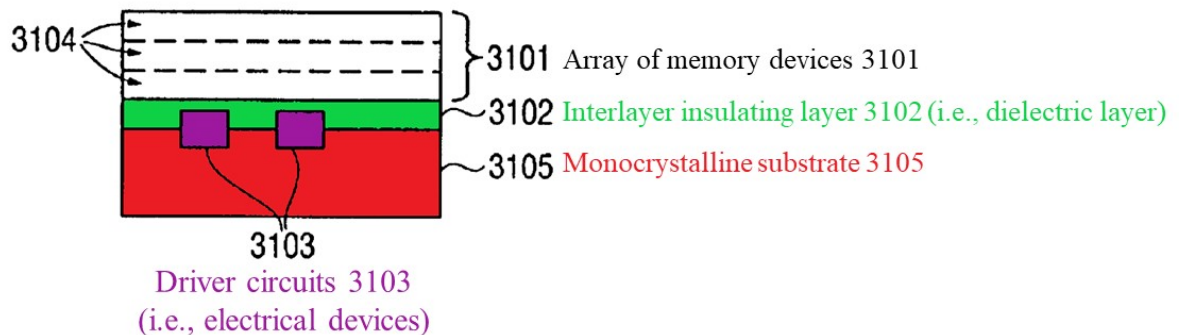
2. Element 13[a]: a substrate having electrical devices formed therein, and further having a dielectric layer disposed above the electrical devices;

Lee discloses:

FIG. 35 [(annotated)] schematically illustrates an array of charge storage logic or memory devices 3101 formed above an interlayer insulating layer 3102 [(green)] disposed above a monocrystalline substrate 3105 [(red)].... The array 3101 has a plurality of device levels 3104, preferably separated by interlayer insulating layers. The driver circuits 3103 [(purple)], such as sense amps and charge pumps are disposed in the monocrystalline substrate 3105, as CMOS or other transistors.

Ex-1007, 12:17-27.

FIG. 35



Id., Fig. 35. The '702 Patent describes “devices” broadly as including any “active and passive circuit elements.” Ex-1001, 4:28-32. Thus, a POSITA would have understood driver circuits such as sense amps and charge pumps to constitute “electrical devices.” Ex-1007, 12:13-15; Ex-1002 ¶116. Therefore, Lee discloses a

substrate having electrical devices formed therein, and further having a dielectric layer disposed above the electrical devices. Ex-1002 ¶116.

3. Element 13[b]: a stackable add-on layer⁵ having a plurality of vertically oriented semiconductor memory cells; and

Lee discloses, “[TFTs] and diodes arranged in a pillar configuration (i.e., the vertical direction with respect to the substrate, where the length of the device is perpendicular to the substrate) and their method of fabrication.” Ex-1002 ¶117; Ex-1007, 13:32-36; *see id.* 14:10-31 (“The first contact region 102 [(pink)], the body 104 [(blue)], and the second contact (source/drain) region 106 [(orange)] are each vertically aligned with one another to form a pillar 108.”); *id.*, Fig. 1A; Ex-1001, 4:7-9 (“‘[V]ertical’...means substantially perpendicular to a major surface of a substrate.”). Thus, Lee discloses a plurality of vertically oriented semiconductor memory cells wherein each cell is aligned substantially perpendicular to a major surface of the substrate. *Id.* 4:7-9; Ex-1002 ¶117.

⁵ Lee discloses the subject matter of the ’702 Patent under the interpretation PO appears to adopt. *See* Ex-1019 ¶¶71-76.

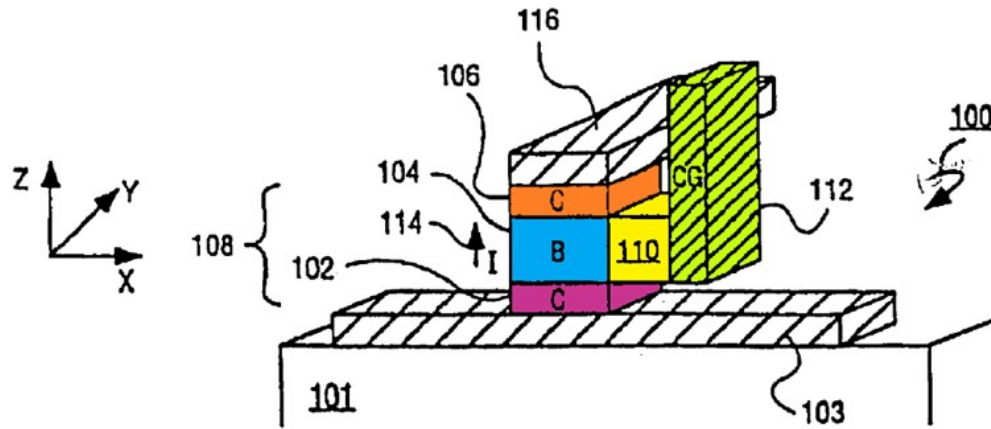


FIG. 1A

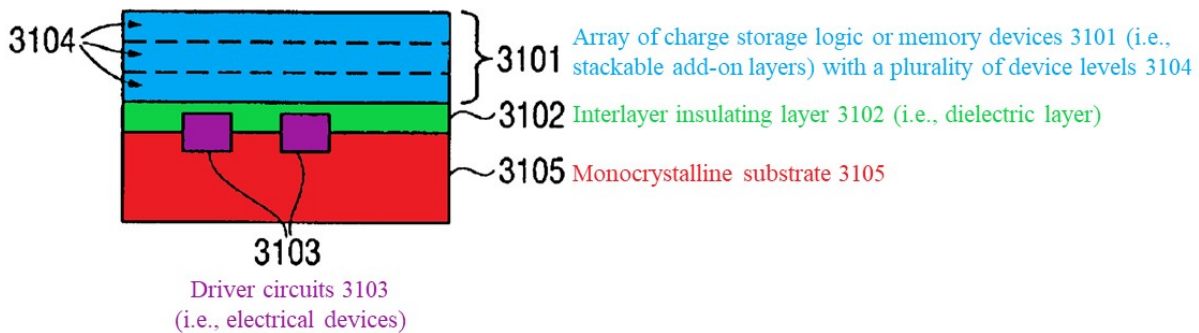
Ex-1007, Fig. 1A (annotated).

Lee further discloses:

FIG. 35 [(annotated)] schematically illustrates an array of charge storage logic or memory devices 3101 [(blue)] formed above an interlayer insulating layer 3102 [(green)] disposed above a monocrystalline substrate 3105 [(red)]. The array of charge storage logic or memory devices 3101 [(i.e., stackable add-on layers)] are thus arranged as a three dimensional monolithic array [TFTs] or diodes in amorphous or polysilicon layers. The array 3101 has a plurality of device levels 3104 [(blue)], preferably separated by interlayer insulating layers. The driver circuits 3103 [(purple)], such as sense amps and charge pumps are disposed in the monocrystalline substrate 3105, as CMOS or other transistors.

Ex-1007, 12:17-27; *see id.* 5:46-56.

FIG. 35

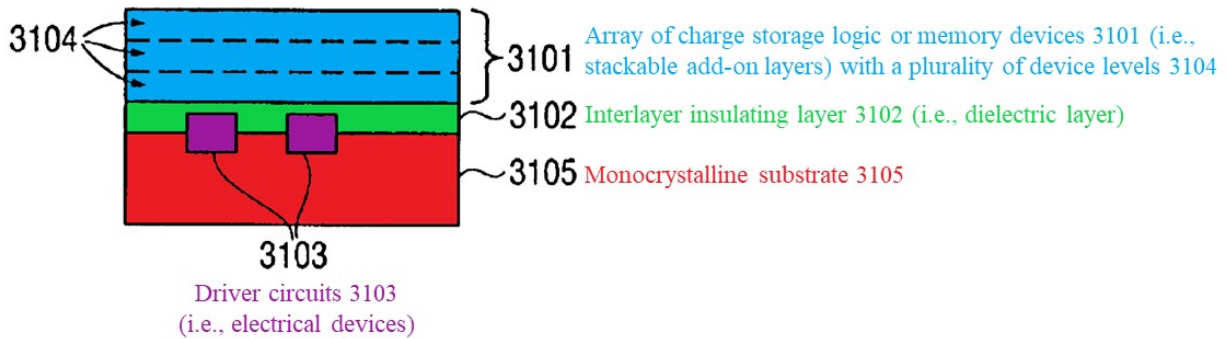


Id., Fig. 35. Because Lee discloses “a three dimensional nonvolatile memory array, comprising a plurality of vertically separated device levels,” in which “each level compris[es] an array of TFT EEPROMs,” the memory array is a stackable add-on layer having a plurality of vertically oriented semiconductor memory cells. *Id.* 5:46-49; Ex-1002 ¶118.

4. Element 13[c]: the stackable add-on layer being bonded to the dielectric layer; and

Lee states, “FIG. 35 schematically illustrates an array of charge storage logic or memory devices 3101 [(i.e., stackable add-on layers)] formed above an interlayer insulating layer 3102 disposed above a monocrystalline substrate 3105.... The array 3101 has a plurality of device levels 3104, preferably separated by interlayer insulating layers.” Ex-1002 ¶119; Ex-1007, 12:17-25. Thus, according to the preferred embodiment, each stackable add-on layer (e.g., each “array of charge storage logic or memory devices 3101”) is bonded to a dielectric layer (e.g., “interlayer insulating layer”). Ex-1002 ¶119.

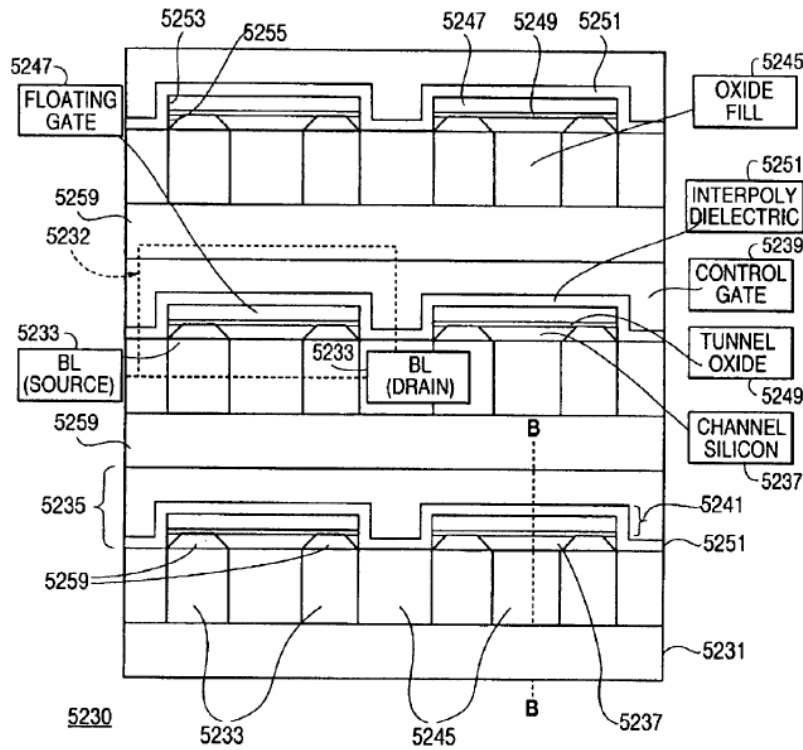
FIG. 35



Id., Fig. 35 (annotated).

“In FIG. 83A, the flash memory array 5230 is preferably formed over a planarized interlayer insulating layer 5231, such as a CMP planarized silicon oxide layer.” Ex-1007, 55:30-32.

FIG. 83A



Id., Fig. 83A. “Layer 5231 is formed over a substrate (not shown) as in the previous embodiments. Each device of the array (shown by dashed lines 5232 in FIG. 83A) is thus a TFT because it is formed over an insulating layer.” *Id.* 55:32-36. Because the flash memory array 5230 (i.e., a stackable add-on layer) is formed over the planarized interlayer insulating layer 5231, a POSITA would have understood that the array is bonded to the planarized interlayer insulating layer 5231. Ex-1002 ¶120.

Lee discloses:

One method of improving device density is to arrange the devices in a monolithic three dimensional array of charge storage devices comprising a plurality of device levels. The term “monolithic” means that layers of each level of the array were directly deposited on the layers of each underlying level of the array. In contrast, two dimensional arrays may be formed separately and then packaged together to form a non-monolithic memory device.

Ex-1007, 11:24-31. Because the layers of the array are directly deposited on the layers of each underlying level, and the array is deposited on the interlayer insulating layer formed over a substrate, a POSITA would have understood that the array (i.e., a stackable add-on layer) is bonded to the interlayer insulating layer (i.e., a dielectric layer). Ex-1002 ¶120.

5. Element 13[d]: wherein the memory cells are nonvolatile memory cells having at least one transistor.

Lee discloses:

[A] three dimensional *nonvolatile memory array*, comprising a plurality of vertically separated device levels, *each level comprising an array of TFT EEPROMs, each TFT EEPROM comprising a channel, source and drain regions, and a charge storage region adjacent to the channel,...*and at least one interlayer insulating layer located between the device levels.

Ex-1007, 5:46-56 (emphasis added); Ex-1009 at 27-29 (explaining EEPROM is a form of nonvolatile memory). Lee also discloses “a three terminal *nonvolatile* stackable pillar memory device. A pillar memory device 100 in accordance with this embodiment of the present invention is broadly illustrated in FIG. 1A,” which shows a transistor in which “[t]he first contact region 102, the body 104, and the second contact (source/drain) region 106 are each *vertically aligned with one another to form a pillar 108.*” Ex-1007, 14:10-23 (emphasis added); Ex-1002 ¶122.

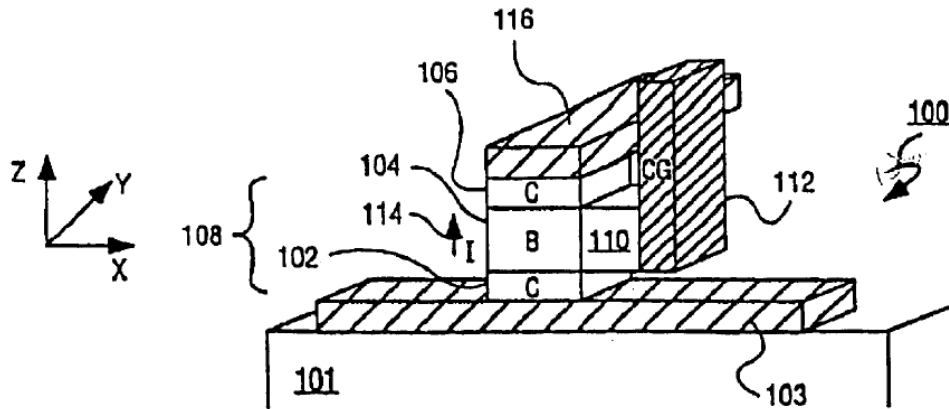


FIG. 1A

Ex-1007, Fig. 1A. Thus, Lee discloses a nonvolatile memory cell having at least one transistor.

6. **Dependent Claim 14: wherein the vertically oriented semiconductor nonvolatile memory cell comprises a vertical transistor having a floating gate and a control gate on a SOI pillar.**

First, Lee's Figure 1A (annotated) shows "a three terminal nonvolatile stackable pillar memory device [100]," that is vertically oriented and comprises a floating gate and control gate. Ex-1007, 14:10-13. Figure 1A illustrates a transistor in which "[t]he first contact region 102 [(pink)], the body 104 [(blue)], and the second contact (source/drain) region 106 [(orange)] are each *vertically aligned with one another to form a pillar 108.*" *Id.* 14:10-23 (emphasis added).

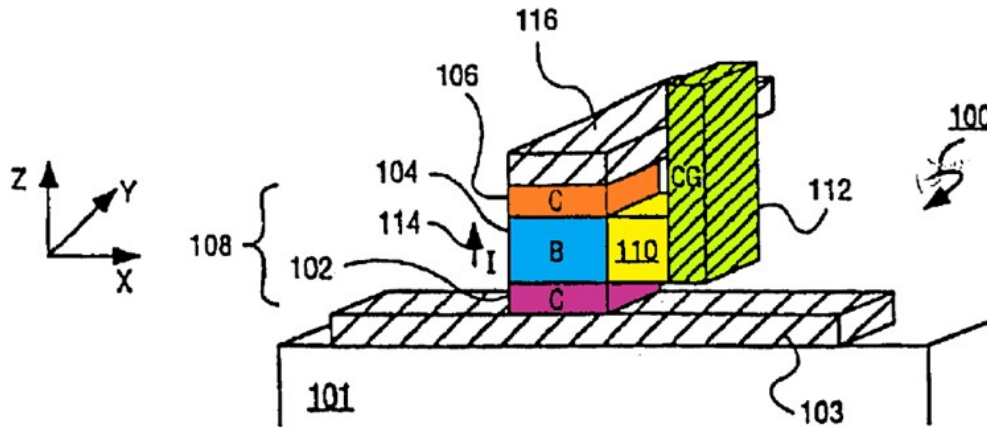


FIG. 1A

Id., Fig. 1A. Figure 1A further illustrates:

Adjacent to and in contact with body 104 is a charge storage medium 110 [(yellow)]. A control gate 112 [(green)] is formed adjacent to and in direct contact with charge storage medium 110. The control gate 112 and charge storage medium 110 are constructed so that they lie laterally adjacent to pillar 108 so that they may electrically communicate with pillar 108. The charge storage medium is the region that electrically screens the control gate and the channel region addressed by the control gate.

Id. 14:23-31.

Lee's Figure 2 depicts "Pillar memory 200," which "has a charge storage medium 211 comprising a tunnel dielectric 212, a floating gate 214 [(yellow)], and a control gate dielectric 216.... Floating gate 214 comprises a conductor such as but not limited to doped silicon, such as N type silicon, or metal such as tungsten." Ex-1007, 15:41-49, Fig. 2; *see*

also id. 18:19-30 (explaining the floating gate may be formed from a continuous conductive film of silicon or metal or a plurality of electrically isolated nanocrystals 602 as shown in FIG. 6). Figure 2 (annotated) also depicts “a control gate 218 [(blue)]...formed adjacent to and in direct contact with control gate dielectric 216. Control gate 218 is formed of a conductor such as but not limited to doped silicon or a metal such as tungsten.” *Id.* 15:50-54.

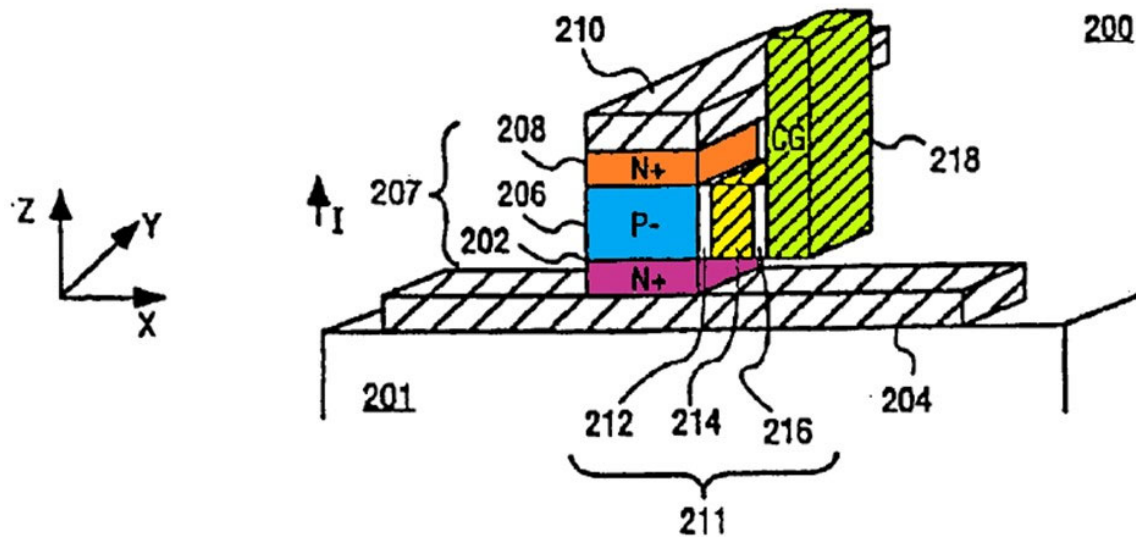


FIG. 2

Id., Fig. 2; *see also id.* 5:28-38, 5:57-65 (disclosing an EEPROM comprising a vertical transistor, floating gate, and control gate). Thus, Lee discloses a vertically oriented semiconductor nonvolatile memory cell comprising a vertical transistor having a floating gate and a control gate.

Second, Lee discloses a SOI pillar. Lee discloses “a substrate having an

insulating surface (i.e., a [SOI] substrate)...provided for the formation of the memory array. The substrate may comprise a semiconductor (i.e., silicon, GaAs, etc.) wafer covered with an insulating layer.” Ex-1007, 31:41-45; Ex-1001, 4:45-5:7. Lee further discloses “a high temperature anneal step,” which “gives the crystallized a-Si layer (i.e., a large grain polysilicon layer) performance characteristics similar to conventional SOI...CMOS technology.” Ex-1007, 69:14-20. Accordingly, this “metal induced crystallization method may be used to recrystallize the active semiconductor layer of any of the above described devices.” *Id.* 69:44-46. “Thus, pillar TFTs, self-aligned TFTs, rail TFTs and diodes (i.e., an active semiconductor layer which contains one or more p-n junctions) of various configurations may be formed in the recrystallized a-Si or polysilicon.” *Id.* 69:46-50. The ’702 Patent recognizes that there are “a variety of ways” of forming SOI structures. Ex-1001, 4:45-47. A POSITA would have understood that Lee’s crystallization method is one method of forming a SOI structure that provides the same advantages and similar performance characteristics as “conventional SOI” technology. Ex-1002 ¶123-25. In the alternative, because Lee compares its crystallization method to “conventional SOI,” a POSITA would have found the use of “conventional SOI” as an obvious replacement to the disclosed crystallization method. *Id.* Thus, Lee discloses or renders obvious a vertically oriented semiconductor nonvolatile memory cell comprising a vertical transistor having a

floating gate and a control gate on a SOI pillar.

7. Dependent Claim 15: wherein the vertically oriented semiconductor nonvolatile memory cell comprises a vertical transistor having a charge-trapping gate insulator and a gate on a SOI pillar.

For reasons set forth above for Claim Element 13[d] and Claim 14, Lee discloses a “vertically oriented semiconductor nonvolatile memory cell” that comprises “a vertical transistor...on a SOI pillar.” *See supra* Sections VII.C.5, VII.C.6; Ex-1002 ¶¶126-27.

Lee’s Figure 7 shows that “N+ source/drain region 202, P type silicon body 206 and N+ source/drain region 208 are each substantially vertically aligned with one another to form [a] pillar.” Ex-1007, 15:37-40. Moreover, Lee discloses, as an “alternative to the use of a dielectric isolated floating gate to store charge in the memory devices of the present invention, one can use a trapping layer formed in the dielectric stack 702 as shown in FIG. 7.” *Id.* 18:61-64. Lee discloses:

[T]he charge storage medium can be a dielectric stack 702 [(yellow)] comprising a first oxide layer 704 adjacent to the silicon body or channel, a nitride layer 706 adjacent to the first oxide layer and a second oxide layer 708 adjacent to the nitride layer and adjacent to the control gate 218 [(blue)].

Id. 18:64-19:5. Lee’s “FIG. 7 [(annotated)] is an illustration of a pillar memory of an embodiment of the present invention having a charge trapping dielectric.” *Id.* 8:40-42.

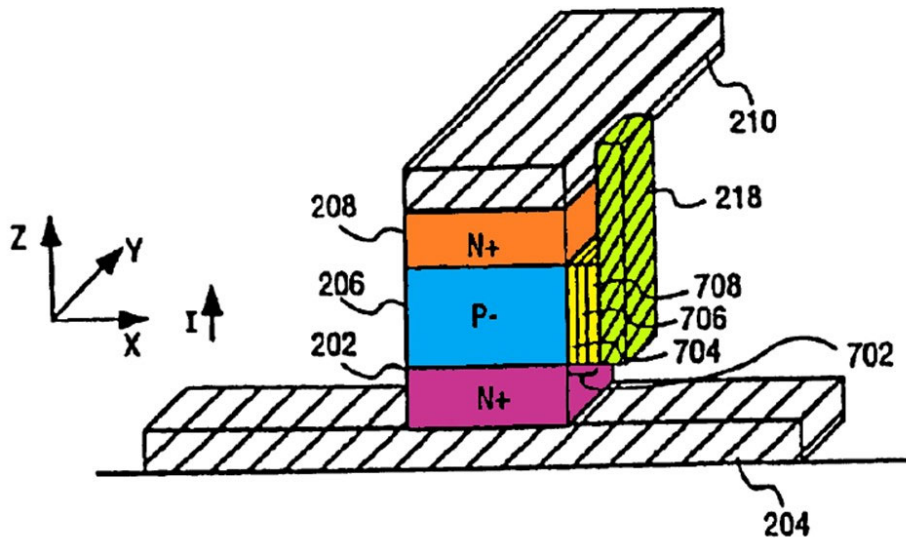


FIG. 7

Id., Fig. 7.

D. Ground 4: Claims 16 and 17 Are Obvious Over Lee in View of Endoh

The subject matter of dependent Claims 16 and 17 is disclosed by Lee in view of Endoh. Ex-1002 ¶¶128-42.

1. A POSITA would have been motivated to combine Lee with Endoh

A POSITA would have been motivated to combine Lee with Endoh and would have a reasonable expectation of success in doing so and achieving their stated objectives, because they are both from the same field and relate to the same well-known issues. Lee and Endoh provide complementary solutions for arranging memory cells three-dimensionally to provide high integration density. *Compare* Ex-1007, 11:18-32, *with* Ex-1006 ¶151. A POSITA seeking to make devices smaller by increase the integration density of semiconductor memory devices, and

specifically nonvolatile memory devices, would have known of and consulted these proposed solutions. Ex-1002 ¶128.

Lee discloses techniques for manufacturing semiconductor memory devices—including nonvolatile memory—in which the memory cells are arrayed three-dimensionally (i.e., vertically) to provide a high integration density. *See, e.g.*, Ex-1007, 5:28-56, 11:18-32, 13:32-38. Endoh provides additional well-known teachings of vertically oriented nonvolatile memory cells with a floating gate and control gate, or a charge-trapping gate insulator and gate, connected in series on a SOI pillar. *See, e.g.*, Ex-1006 ¶¶3, 6, 40, 151, 329, 662, 1138-72, 1205-07. A POSITA would have been motivated to modify Lee to obtain additional features and benefits from implementing the well-known teachings of NAND serial connections. Ex-1002 ¶129; *see, e.g.*, Ex-1006, ¶¶45, 46, 178 (describing “constructions in which a plurality of, for example, two memory cells are arranged in series on one island-like semiconductor layer”), 211, 223, 249, 250, 257, 263, 1206, Fig. 65; *see infra* Sections VII.D.2-VII.D.3.

Endoh states, “double the capacity of the prior-art memory device can be obtained if memory transistors in two tiers are formed per semiconductor substrate pillar.” Ex-1006 ¶1659. “Thereby, the cell area per bit decreases, the size of chips can be decreased and the production costs can be reduced.” *Id.* Similarly, Lee explains, “the cost of memory and logic devices would be decreased if the device

density was increased.” Ex-1007, 11:18-20; *Dystar*, 464 F.3d at 1368. A POSITA would have had a reasonable expectation of success in combining the teachings of Lee and Endoh with no change in their respective functions because both references purport to solve these problems in similar and predictable ways, such as using the well-known teachings of vertical transistors and pillar structures. Ex-1002 ¶130.

2. Dependent Claim 16: wherein at least two nonvolatile memory cells are vertically oriented and serially connected together and formed with a first SOI pillar.

Lee in view of Endoh teaches dependent Claim 16. Ex-1002 ¶131. For reasons set forth above for Claim Element 13[d] and Claim 14, Lee discloses a “vertically oriented semiconductor nonvolatile memory cell” that comprises “a vertical transistor...on a SOI pillar.” *See supra* Sections VII.C.5, VII.C.6.

Lee discloses “[TFTs] and diodes arranged in a pillar configuration (i.e., the vertical direction with respect to the substrate, where the length of the device is perpendicular to the substrate) and their method of fabrication.” Ex-1007, 13:31-38. For example, Lee’s Figure 12B “illustrate[s] a method of forming a common continuous film control gate between two or more levels of pillar memories” on a substrate (not shown). *Id.* 8:55-56.

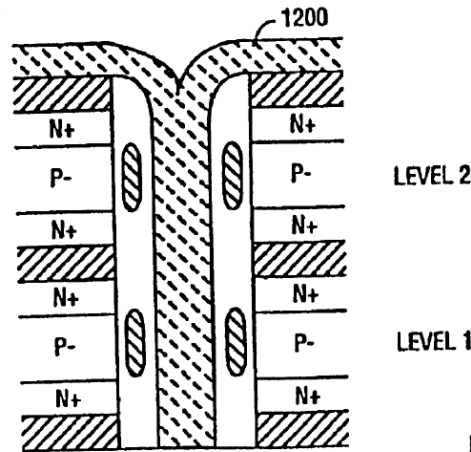


FIG. 12B

Id., Fig. 12B. Thus, Lee discloses “at least two nonvolatile memory cells...vertically oriented...and formed with a first SOI pillar.” Ex-1002 ¶132.

Lee further discloses “a cross-point array of word lines and bit lines at a horizontal level and a method of making thereof.” Ex-1007, 40:5-7. “This memory arrangement is known as the NOR Virtual Ground (NVG) Array (also referred to as VGA).” *Id.* 40:11-13. However, “the memory array may also be arranged in nonvolatile flash memory architectures other than VGA.” *Id.* 40:13-15. As explained above in Section VII.B.4, “Two common types of flash memory array architectures are the ‘NAND’ and ‘NOR’ architectures.” Ex-1012, 1:29-30.

Although “[a] NAND array architecture also arranges its array of floating gate memory cells in a matrix,” the key difference between a NOR and NAND arrangement is that in NAND, “each memory cell is not directly coupled to a column bit line by its drain.” *Id.* 1:43-47. “Instead, the memory cells of the array are coupled together in series, source to drain, between a source line and a column

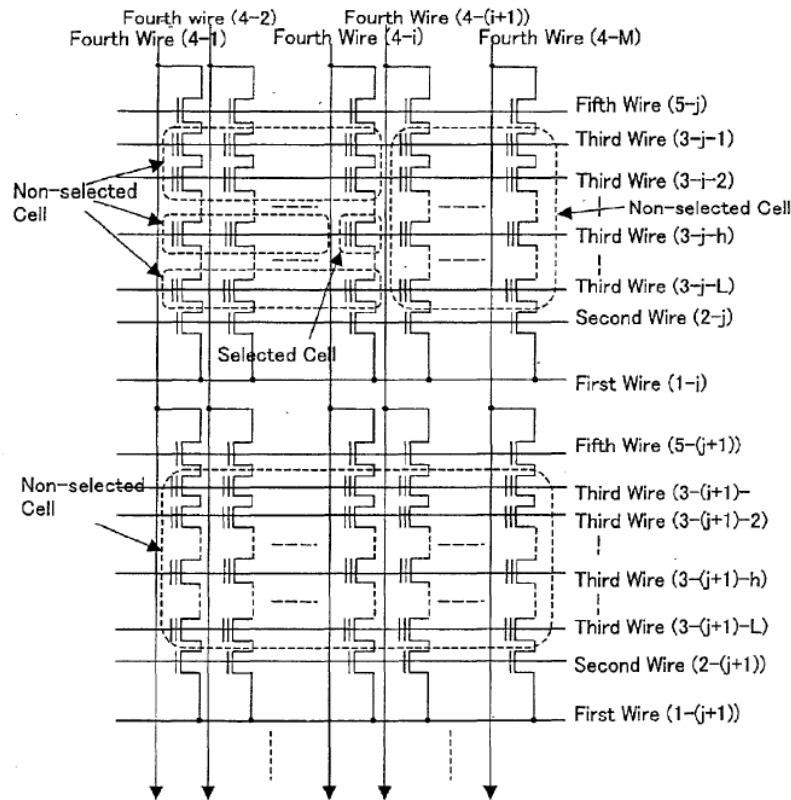
bit line.” *Id.* 1:47-49.

A POSITA would have found it obvious to use the NAND architecture because an entire NAND cell string uses only “one-half” of a bit line contact and “one-half” of a source line contact, which further increases the integration density of the memory design. Ex-1011, 2:59-65, 5:12-25 (“The primary purpose of using such a string structure is to reduce the number of contacts per memory cell.... The overall effect is a dramatic reduction in the chip area per memory cell.”); Ex-1002 ¶¶133-34. Thus, a POSITA would have found it obvious to modify Lee’s pillar structure to use the NAND architecture and a serial connection as taught by Endoh. Ex-1002 ¶¶133-34; *see, e.g.*, Ex-1006 ¶1205-07.

For example, Endoh’s Production Example 52 discloses “a semiconductor memory device [having] a structure in which...island-like semiconductor layers are formed in the form of *pillars* by selective epitaxial silicon growth.” Ex-1006 ¶1206 (emphasis added). The EEPROM memory cell array of Production Example 52 comprises “two memory cells...arranged on each island-like semiconductor layer...[with] the transistors...*connected in series* along the island-like semiconductor layer, as shown in FIG. 1171 and FIG. 1172.” *Id.* ¶¶1206-07 (emphasis added), Figs. 1, 1171-72; *id.* ¶1074 (describing vertically oriented semiconductor memory cells); Ex-1009 at 27-29 (explaining EEPROM is a form of nonvolatile memory). “FIG. 65 shows the equivalent circuit diagram of

the...memory cell array” having “a plurality of (e.g., $M \times N$...) island-like semiconductor layers.” Ex-1006 ¶¶257-58.

Fig. 65



Id., Fig. 65. Thus, Lee in view of Endoh teaches at least two vertically oriented nonvolatile memory cells serially connected and formed on a SOI pillar. Ex-1002 ¶135.

A POSITA would have been motivated to combine Lee with Endoh’s teachings of a serial connection. Ex-1002 ¶136. NAND increases the integration density of a memory design by reducing the number of contacts per memory cell and, thus, reducing the chip area per memory cell. Ex-1011, 2:59-65, 5:12-25; Ex-

1002 ¶136. Because Lee recognizes “that the cost of memory and logic devices would be decreased if the device density was increased,” an object of Lee is to “provide[] an ultra[-]dense matrix array of charge storage semiconductor devices which has an increased density and a lower cost.” Ex-1007, 11:18-23. In addition, because NAND offers a higher integration density than a NOR architecture, there is a bigger market for NAND architecture. Ex-1002 ¶136. Thus, a POSITA would have been motivated to modify Lee’s pillar structures to use a serial connection as taught by Endoh.

Further, a POSITA would have had a reasonable expectation of success in modifying Lee to use a NAND serial connection because the “[t]wo common types of flash memory array architectures”—NAND and NOR—both “arrange its array of...memory cells in a matrix such that the gates of each...memory cell of the array are coupled by rows to word select lines.” Ex-1012, 1:29-46. Because the NAND architecture was well known and nonvolatile memory cell structures in NAND were (and still are today) similar to those in NOR architecture, and Lee notes that alternative memory architectures can be used, a POSITA would have had a reasonable expectation of success in modifying Lee to use a NAND serial connection. Ex-1002 ¶137; Ex-1007, 40:13-15. Thus, Lee in view of Endoh discloses or renders obvious at least two vertically oriented nonvolatile memory cells serially connected and formed with a SOI pillar. Ex-1002 ¶137.

3. Dependent Claim 17: wherein the at least two nonvolatile memory cells on the first SOI pillar are serially connected with an interconnect line disposed on a dielectric layer, to a nonvolatile memory cell formed with a second SOI pillar.

Lee in view of Endoh teaches dependent Claim 17. Ex-1002 ¶138. For reasons set forth above for Claim Element 13[d] and Claim 14, Lee discloses a “vertically oriented semiconductor nonvolatile memory cell” that comprises “a vertical transistor...on a SOI pillar.” *See supra* Sections VII.C.5, VII.C.6.

Moreover, Lee in view of Endoh teaches at least two nonvolatile memory cells on a first SOI pillar connected serially to a nonvolatile memory cell formed on a second SOI pillar via an interconnect line disposed on a dielectric layer. For reasons set forth above for Claim 16, Lee in view of Endoh discloses or renders obvious at least two vertically oriented nonvolatile memory cells serially connected and formed with a SOI pillar. *See supra* Section VII.D.2. Because an entire NAND cell string uses only “one-half” of a bit line contact and “one-half” of a source line contact, a POSITA would have understood that connecting a plurality of pillars of memory cells would further increase the integration density of the memory design. Ex-1011, 2:59-65, 5:12-25; Ex-1002 ¶139.

A POSITA would have recognized the constraints of connecting individual devices in series vertically and found it obvious to form a first pillar with several memory devices formed in series and then connect in series the first pillar to additional pillars each with several additional memory devices. Ex-1002 ¶140. A

POSITA would have known that a NAND string generally comprises eight, sixteen, or thirty-two memory cells connected in series. *Id.*; *see, e.g.*, Ex-1011 (illustrating an 8-cell NAND string); Ex-1013 (illustrating a 16-cell NAND string); Ex-1008, 3:8-16 (illustrating 16- and 32-cell NAND strings and explaining the number of cells connected in series is expected to increase in the future). Further, because manufacturing and fabrication constraints generally limit the number of memory cells formed in the vertical direction, a POSITA would have found it obvious to connect multiple pillars in series to maximize the memory potential of the system. Ex-1002 ¶140. And a POSITA would have known that connecting multiple pillars in series requires interconnections between the pillars. *Id.* Without an interconnection between pillars, “serially connected” pillars would have required the memory cells to be part of a single string. *Id.*

For example, Lee illustrates vertically stacking two memory cells (Ex-1007, Figs. 12A-12B, 23A, 25A), whereas Endoh illustrates NAND strings having more than four memory cells connected in series (Ex-1006, Fig. 65). Thus, to form the NAND circuit shown in Endoh, a POSITA would have found it obvious to connect multiple pillars in series as disclosed by Lee. Ex-1002 ¶141. In addition, a POSITA would have found it obvious to connect the pillars using an interconnect line disposed on a dielectric layer to avoid shorting any of the devices. *Id.* ¶141. Lee’s Fig. 67 shows one such interconnect line (e.g., conductors 5080, 5082, 5084, 5086)

disposed on a dielectric layer (insulating layer comprises regions 5088, 5090, 5092). Ex-1007, 49:4-33, Fig. 67; Ex-1002 ¶141. Also, one common method, as described by Watanabe, is first forming vias (or holes) on the dielectric layer, followed by depositing interconnect line (wires) in the vias. *See, e.g.*, Ex-1005; *see also* Ex-1030 (describing pillars of memory cells connected via common select gates). Thus, Lee in view of Endoh teaches two nonvolatile memory cells on a first SOI pillar connected serially to a nonvolatile memory cell formed on a second SOI pillar via an interconnect line disposed on a dielectric layer. *Id.* ¶141.

A POSITA would have been motivated to combine Lee with Endoh's teachings of a serial connection. Ex-1002 ¶142. Because Lee recognizes "that the cost of memory and logic devices would be decreased if the device density was increased," an object of Lee is to "provide[] an ultra[-]dense matrix array of charge storage semiconductor devices which has an increased density and a lower cost." Ex-1007, 11:18-23. In addition, because NAND offers a higher integration density than a NOR architecture, there is a bigger market for NAND architecture. Ex-1002 ¶142. Utilizing the high integration density of NAND, a POSITA can connect several memory cells and pillars in series to further increase the memory capacity in a single assembly. *Id.* Thus, a POSITA would have been motivated to connect a plurality of memory cells on a pillar in series and then connect a plurality of pillars in series, via interconnects, to further form an 8-, 16-, or 32-cell string. *Id.* Because

the NAND architecture was well known and nonvolatile memory cell structures in NAND were (and still are) similar to those in NOR architecture, and Lee notes that alternative memory architectures can be used, a POSITA would have had a reasonable expectation of success in modifying Lee to use a NAND serial connection. *Id.*; Ex-1007, 40:13-15.

E. Ground 5: Claims 13-15 Are Obvious Over Lee in View of Watanabe

To the extent Claim 13 is construed to exclude forming a “stackable add-on layer” through sequential deposition directly on a substrate, the subject matter of dependent Claims 13-15 is disclosed by Lee in view of Watanabe. Ex-1002 ¶¶143-50.

1. A POSITA would have been motivated to combine Lee with Watanabe

A POSITA would have been motivated to combine Lee with Watanabe and would have a reasonable expectation of success in doing so and achieving their stated objectives, because both references are from the same field and relate to the same well-known issues. Lee and Watanabe provide complementary solutions for arranging memory cells three-dimensionally to provide a high integration density. *Compare* Ex-1007, 11:18-32, *with* Ex-1005, 1:49-2:5. A POSITA seeking to increase the integration density of semiconductor memory devices, and specifically

nonvolatile memory devices, would have known of and consulted these proposed solutions. Ex-1002 ¶144.

Lee discloses techniques for manufacturing semiconductor memory devices—including nonvolatile memory—in which the memory cells are arrayed three-dimensionally to provide a high integration density. *See, e.g.*, Ex-1007, 5:28-56, 11:18-32, 13:32-38. Similarly, Watanabe provides techniques for manufacturing any type of semiconductor memory device—including nonvolatile memory—in which the memory cells are arrayed three-dimensionally to provide a high integration density. *See, e.g.*, Ex-1005, 1:49-52, 2:41-55, 5:1-6:19. Although Lee discloses forming vertical memory devices through layer-by-layer sequential deposition on the substrate, a POSITA would have found it obvious to combine Lee with Watanabe because Watanabe discloses this same method as well as an alternative method of forming “stackable add-on layers” individually and then bonding them to the separately-fabricated substrate. *Compare* Ex-1007, 11:24-29, *with* Ex-1005, 5:1-6:14. Thus, a POSITA would have been motivated to modify Lee in view of Watanabe to use an alternative method of forming a stackable add-on layer and obtain the benefits associated with that method. Ex-1002 ¶145; *see* Ex-1005, 5:1-6:14; *see infra* Sections VII.E.2-VII.E.4.

These references acknowledge similar motivations for their respective teachings. For example, Lee explains, “the cost of memory and logic devices

would be decreased if the device density was increased.” Ex-1007, 11:18-20; *Dystar*, 464 F.3d at 1368. Similarly, Watanabe explains, “By virtue of such a 3-dimensional memory cell array, the integration density of the semiconductor memory device can be greatly increased.” Ex-1005, 2:2-5. A POSITA would have had a reasonable expectation of success in combining the teachings of Lee and Watanabe with no change in their respective functions because both of these references purport to solve the same problems in similar and predictable ways, such as using the well-known teachings of vertical transistors and pillar structures. Ex-1002 ¶146. In addition, Watanabe discloses a benefit of using its “bonding method”—it “improves the accuracy of the wiring.” Ex-1005, 5:64-6:3.

2. Elements 13[preamble], 13[a], and 13[d]

If Claim 13’s preamble is limiting, Lee discloses the preamble. *See supra* Section VII.C.1; Ex-1002 ¶147; *see also supra* Section VII.A.1 (explaining Watanabe discloses the preamble of Claim 13). In addition, Lee discloses Claim Elements 13[a] and 13[d]. *See supra* Sections VII.C.2, VII.C.5; *see also supra* Sections VII.A.2, VII.A.5 (explaining Watanabe discloses Claim Elements 13[a] and 13[d]).

3. Elements 13[b] and 13[c]

For reasons set forth above for Claim Elements 13[b] and 13[c], Lee and Watanabe both disclose “a stackable add-on layer having a plurality of vertically

oriented semiconductor memory cells, and the stackable add-on layer being bonded to the dielectric layer.” *See supra* Sections VII.C.3-VII.C.4, VII.A.3-VII.A.4.

To the extent Claim 13 is construed to exclude forming a “stackable add-on layer” through sequential deposition directly on a substrate, Lee in view of Watanabe discloses this limitation. Ex-1002 ¶¶148-49. Although Lee discloses forming vertically oriented memory devices through layer-by-layer sequential deposition on the substrate, a POSITA would have found it obvious to combine Lee with Watanabe because Watanabe discloses this same method as well as a “stacking method” of bonding completed “stackable add-on layers” (referred to as “planar members” in Watanabe) through high-temperature bonding. *Compare* Ex-1007, 11:24-29, *with* Ex-1005, 5:1-6:14. Watanabe explains that its “stacking method” forms wiring “for each planar member” individually, which “improves the accuracy of the wiring.” Ex-1005, 6:1-3. In addition, Watanabe explains that its methods “provid[e] a semiconductor memory device with improved integration density and of a low interconnection wire resistance.” *Id.* 6:20-23. Thus, a POSITA would have been motivated to modify Lee in view of Watanabe to use its “stacking method” to form a stackable add-on layer and obtain the benefits associated with that method. Ex-1002 ¶¶148-49; *see* Ex-1005, 5:1-6:14. Further, a POSITA would have had a reasonable expectation of success in combining Lee and Watanabe because Watanabe covers the method provided in Lee as well as an alternative

method reaching the same objectives. Ex-1002 ¶¶148-49; *compare* Ex-1007, 11:24-29, *with* Ex-1005, 5:1-6:14.

4. Dependent Claims 14-15

As discussed above, Lee discloses dependent Claims 14 and 15. *See supra* Section VII.C.6-VII.C.7; Ex-1002 ¶150; *see also supra* Section VII.B.2-VII.B.3 (explaining Watanabe in view of Endoh discloses dependent Claims 14-15).

F. Ground 6: Claims 16 and 17 Are Obvious Over Lee in View of Watanabe and Endoh

Lee in view of Watanabe and Endoh discloses dependent Claims 16 and 17. Ex-1002 ¶¶151-52. As discussed above, Lee in view of Endoh discloses Claims 16-17. *See supra* Section VII.D.2-VII.D.3; Ex-1002 ¶¶151-52; *see also supra* Section VII.B.4-VII.B.5 (explaining Watanabe in view of Endoh discloses Claims 16-17).

A POSITA would have been motivated to combine Lee with Watanabe and Endoh and would have a reasonable expectation of success in doing so, because Lee, Watanabe, and Endoh provide complementary solutions for arranging memory cells—including nonvolatile memory—three-dimensionally to provide a high integration density. *See supra* Sections VII.B.1, VII.D.1, VII.E.1. As discussed above, a POSITA would have been motivated to modify Lee in view of Watanabe and Endoh to use an alternative method of forming a stackable add-on layer and obtain the additional features and benefits of implementing the well-

known teachings of a charge-trapping gate insulator, SOI pillar, and serial connection. *See supra* Section VII.E.1. In addition, a POSITA would have had a reasonable expectation of success in combining Lee, Watanabe, and Endoh with no change in their respective functions because each of these references purport to solve the same problems in similar and predictable ways, such as using the well-known teachings of vertical transistors and pillar structures. *See id.*; Ex-1002 ¶¶151-52.

VIII. THE BOARD SHOULD NOT USE ITS DISCRETION TO DENY INSTITUTION UNDER *FINTIV*

The Board should not deny institution under §314(a). While Director Vidal’s June 21, 2022, Guidance made clear that “*Fintiv* is limited to facts of that case,” for completeness, Petitioner addresses the factors set forth in *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (PTAB Mar. 20, 2020) (precedential). The factors set out in *Fintiv* do not justify denying institution.

The **first *Fintiv* factor** is neutral because Micron has not yet moved to stay the district court proceedings, and the PTAB will not infer how the district court would rule should a stay be requested. *See, e.g., Hulu v. SITO Mobile*, IPR2021-00298, Paper 11 at 10-11 (PTAB May 19, 2021).

For the **second *Fintiv* factor**, the district court has not set a trial date, but trial is estimated for around November 2024. This timing does not tip in favor of denial. *See, e.g., Apple v. Koss*, IPR2021-00305, Paper 14 at 13 (PTAB June 3,

2021). This Petition is filed in May 2023. An institution decision should issue within six months of docketing, around November 2023. And an FWD should issue around November 2024, which is likely near the trial date. Recent PTAB cases analyzing similar schedules have weighed the second factor as neutral or, at most, slightly in favor of denial. *See, e.g., Google v. Parus*, IPR2020-00847, Paper 9 at 12 (PTAB Oct. 21, 2020); *Apple v. Koss*, IPR2021-00305, Paper 14 at 13-14 (PTAB June 3, 2021).

If the median time to trial for civil actions in the EDTX is used to estimate the trial date, per Director Vidal’s June 2022 Guidance, trial is expected November 2024, which coincides with an expected FWD. Ex-1017 at 35 (indicating median 19 months to trial in EDTX).

The **third *Fintiv* factor** weighs strongly against denial. The Court has not yet held a Case Management Conference or set a Markman or Trial date. No hearings have been set and no substantive activity has occurred in the case. Because the investment in the trial has been minimal and Petitioner acted diligently, this factor weighs strongly against discretionary denial. *See, e.g., Hulu*, Paper 11 at 13.

The **fourth *Fintiv* factor** also weighs against denial. As explained above, the median time to trial for civil actions in EDTX suggests that trial will not occur until around the time of FWD. Thus, “there is a reasonable likelihood that the

Board will address the overlapping validity issues prior to the district court reaching them at trial..., thereby providing the possibility of simplifying issues for trial.” *Juniper v. Packet Intel.*, IPR2020-0039, Paper 21 at 18 (PTAB Sept. 10, 2020); *see also MED-EL v. Sonova*, IPR2020-00176, Paper 13 at 15 (PTAB June 3, 2020) (overlap that exists between the invalidity issues in this case and in the district court “may inure to the district court’s benefit, however, by simplifying issues for trial....”).

Moreover, Petitioner is challenging more claims than asserted in the district court litigation. PO’s Complaint asserts only Claim 13. This Petition challenges Claims 13-17. Thus, this IPR is the only venue in which the invalidity challenges against several claims in the ’702 Patent will be adjudicated. Moreover, reviewing the challenged claims in this proceeding promotes efficiency because more claims will be addressed here, which will resolve disputes against future district court defendants. *See Fintiv*, Paper 11 at 4. Challenging additional claims further weighs against denial. *See, e.g., Vudu v. Ideahub*, IPR2020-01688, Paper 16 at 14-15 (PTAB Apr. 19, 2021).

On the **fifth *Fintiv* factor**, the Board should give little weight to the fact that Petitioner and PO are the same parties as in district court. Although Micron is both petitioner and litigation defendant, this factor does not outweigh the other factors that strongly weigh against discretionary denial. *See Weatherford v. Enventure*

Global, IPR2020-01684, Paper 16 at 11-13 (PTAB Apr. 14, 2021).

“Other circumstances” under the **sixth *Fintiv* factor** further weigh against discretionary denial. The Petition’s merits are strong with two primary references, Watanabe and Lee, alone or in combination with one secondary reference, rendering independent Claim 13 and dependent Claims 14-17 obvious. *See Align v. 3Shape*, IPR2020-01087, Paper 15 at 42-43 (PTAB Jan. 20, 2021); *see also supra* Section VII.

Taken together holistically, the *Fintiv* factors strongly weigh against exercising discretion to deny institution.

IX. CONCLUSION

The unpatentability grounds presented above are reasonably likely to prevail, and IPR should be instituted for Claims 13-17 of the ’702 Patent based on each of the grounds specified in this Petition.

Respectfully submitted,

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CERTIFICATE OF WORD COUNT

Under 37 C.F.R. §42.24(d), Petitioner certifies that this petition includes 13,997 words, as measured by Microsoft Word, exclusive of the table of contents, mandatory notices under §42.8, certificates of service, word count, and exhibits.

CERTIFICATE OF SERVICE (37 C.F.R. § 42.6(e)(1))

The undersigned hereby certifies that the above document was served on May 4, 2023, by filing this document through the Patent Trial and Appeal Board P-TACTS System, as well as delivering a copy via express mail upon the following attorneys of record for the Patent Owner:

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