

Filed on behalf of BeSang Inc.

By: Michelle E. Armond

Douglas R. Wilson

Joseph Li

Yue Han

ARMOND WILSON LLP

4685 MacArthur Court, Suite 390

Newport Beach, CA 92660

Telephone: (949) 932-0778

Email: ipr@armondwilson.com

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
MICRON SEMICONDUCTOR PRODUCTS, INC., and
MICRON TECHNOLOGY TEXAS, LLC,
Petitioners,

v.

BESANG INC.,
Patent Owner.

Case No. IPR2023-00900
U.S. Patent No. 7,378,702

PATENT OWNER'S PRELIMINARY RESPONSE

TABLE OF CONTENTS

I.	INTRODUCTION.....	1
II.	BACKGROUND.....	4
A.	Background Of The Invention	4
B.	The Invention Of The '702 Patent	9
C.	U.S. Patent No. 5,091,762 (“Watanabe”)	11
D.	U.S. Patent No. 6,881,994 (“Lee”)	11
E.	U.S. Patent Application Publication No. 2002/0154556 (“Endoh”).....	11
F.	Co-Pending Litigation On The '702 Patent	12
III.	LEVEL OF ORDINARY SKILL IN THE ART.....	12
IV.	CLAIM CONSTRUCTION IS NOT NECESSARY TO DENY INSTITUTION HERE	13
V.	THE PETITION’S CHALLENGES ARE NOT REASONABLY LIKELY TO PREVAIL	13
A.	Grounds 1 And 2 Based On Watanabe Are Not Reasonably Likely To Prevail	14
1.	Trial Should Not Be Ordered On Grounds 1 And 2 Because The Petition Makes No Showing Of A Motivation to Combine Watanabe’s Different Embodiments (Claims 13-17).....	14
2.	Trial Should Not Be Ordered On Grounds 1 And 2 Because There Is No Showing That Watanabe Discloses Or Renders Obvious Limitation 13[b] (Claims 13-17)	19
3.	The Ground 2 Challenge To Claims 14-17 Fails Because The Petition Has Not Established Watanabe Teaches Or Suggests An SOI Pillar	24

B.	Grounds 3-6 Based On Lee Are Not Reasonably Likely To Prevail	28
1.	Trial Should Not Be Ordered On Grounds 3-6 Because There Is No Showing That Combining Lee’s Different Embodiments Would Have Been Obvious (Claims 13-17).....	29
2.	The Ground 3 Challenge To Claim 15 Fails Because It Combines Alternative Embodiments With No Explanation Why Or How One Of Skill In The Art Would Have Done So	32
VI.	THE BOARD SHOULD EXERCISE ITS DISCRETION TO DENY INSTITUTION UNDER <i>FINTIV</i>	33
A.	Factor 1: Whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted.....	33
B.	Factor 2: The proximity of the court’s trial date to the Board’s projected statutory deadline for a final written decision.....	34
C.	Factor 3: Investment in the parallel proceeding by the court and the parties.....	34
D.	Factor 4: Overlap between issues raised in the petition and in the parallel proceeding.....	35
E.	Factor 5: Whether the petitioner and the defendant in the parallel proceeding are the same party.....	36
F.	Factor 6: Other circumstances that impact the Board’s exercise of discretion, including the merits.	36
G.	None Of The <i>Fintiv</i> Factors Supports Institution	37
VII.	CONCLUSION	37

TABLE OF AUTHORITIES

	Page No(s).
<i>Amazon.com, Inc. v. AlmondNet, Inc.</i> , IPR2022-01455, Paper 12 (P.T.A.B. Apr. 6, 2023)	33
<i>Apple Inc. v. Fintiv, Inc.</i> , IPR2020-00019, 2020 WL 2126495 (P.T.A.B. Mar. 20, 2020).....	33
<i>ATD Corp. v. Lydall, Inc.</i> , 159 F.3d 534 (Fed. Cir. 1998)	18, 31
<i>Belden Inc. v. Berk-Tek LLC</i> , 805 F.3d 1064 (Fed. Cir. 2015)	26
<i>Cheese Sys., Inc. v. Tetra Pak Cheese and Powder Sys., Inc.</i> , 725 F.3d 1341 (Fed. Cir. 2013)	3
<i>Code200 v. Luminati Networks Ltd.</i> , IPR2020-01266, 2020 WL 7682243 (P.T.A.B. Dec. 23, 2020)	33, 36
<i>CommScope Techs. LLC v. Dali Wireless, Inc.</i> , IPR2022-01242, 2023 WL 2237986 (P.T.A.B. Feb. 27, 2023)	36
<i>Dennison Mfg. Co. v. Panduit Corp.</i> , 475 U.S. 809 (1986)	26
<i>Fitbit, Inc. v. Philips N. Am. LLC</i> , IPR2020-00828, 2020 WL 6470312 (P.T.A.B. Nov. 3, 2020)	36
<i>Health Care Logistics, Inc. v. Kit Check, Inc.</i> , IPR2019-00394, 2019 WL 2461793 (P.T.A.B. July 11, 2019).....	27
<i>Hewlett Packard Enter. Co. v. Intellectual Ventures II LLC</i> , IPR2022-00115, 2022 WL 946244 (P.T.A.B. Mar. 29, 2022).....	18, 31
<i>Johnson & Johnson Surgical Vision, Inc. v. Alcon Inc.</i> , IPR2021-01003, 2021 WL 6338373 (P.T.A.B. Nov. 23, 2021)	12

Micron Technology v. BeSang Inc.
Patent No. 7,378,702 – IPR2023-00900

KeyMe, LLC v. Hillman Grp., Inc.,
IPR2020-01028, 2021 WL 129094 (P.T.A.B. Jan. 13, 2021) 35

Lumenis Be Ltd. v. BTL Healthcare Techs. A.S.,
IPR2021-01280, 2022 WL 946534 (P.T.A.B. Mar. 9, 2022)..... 17, 31

In re Magnum Oil Tools Int’l, Ltd.,
829 F.3d 1364 (Fed. Cir. 2016)..... 14, 29

Markforged Inc. v. Continuous Composites, Inc.,
IPR2022-01220, 2023 WL 157619 (P.T.A.B. Jan. 11, 2023) 17

Mylan Labs. Ltd. v. Janssen Pharmaceutica NV,
IPR2020-00440, 2020 WL 5580472 (P.T.A.B. Sept. 16, 2020) 33

Nabors Drilling Techs. USA, Inc. v. Motive Drilling Techs., Inc.,
IPR2022-00327, Paper 30 (P.T.A.B. July 5, 2023)..... 20

One World Techs., Inc. v. Chevron (HK) Ltd.,
PGR2020-00059, 2020 WL 7222691 (P.T.A.B. Dec. 7, 2020) 25

Panduit Corp. v. Dennison Mfg. Co.,
774 F.2d 1082 (Fed. Cir. 1985)..... 26

Polaris Indus. v. Arctic Cat,
882 F.3d 1056 (Fed. Cir. 2018)..... 4

Realtime Data, LLC v. Iancu,
912 F.3d 1368 (Fed. Cir. 2019)..... 13

SAS Inst., Inc. v. Iancu,
138 S. Ct. 1348 (2018) 23

South-Tek Sys., LLC v. Engineered Corrosion Sols., LLC,
748 F. App’x 1003 (Fed. Cir. Sept. 20, 2018)..... 23

In re Stepan Co.,
868 F.3d 1342 (Fed. Cir. 2017)..... 14, 15, 28, 30

TCO AS v. NCS Multistage Inc.,
PGR2020-00077, 2021 WL 662165 (P.T.A.B. Feb. 18, 2021)..... 35

Micron Technology v. BeSang Inc.
Patent No. 7,378,702 – IPR2023-00900

Unified Patents Inc. v. GE Video Compression, LLC,
IPR2019-00726, 2019 WL 3714386 (P.T.A.B. Aug. 6, 2019) 18, 28, 31

Unified Patents Inc. v. Multimedia Content Mgmt. LLC,
IPR2017-01934, 2019 WL 967806 (P.T.A.B. Feb. 25, 2019) 16

W.L. Gore & Assocs., Inc. v. Garlock, Inc.,
721 F.2d 1540 (Fed. Cir. 1983)..... 4

WhiteWater West Indus., Ltd. v. Am. Wave Machs., Inc.,
IPR2022-01035, 2022 WL 17071813 (P.T.A.B. Nov. 17, 2022) 17, 30, 33

Wolfspeed, Inc. v. The Trustees of Purdue Univ.,
IPR2022-00761, Paper 19 (P.T.A.B. July 20, 2023)..... 23

Xerox Corp. v. Bytemark, Inc.,
IPR2022-00624, 2022 WL 3648989 (P.T.A.B. Aug. 24, 2022) 26

OTHER AUTHORITIES

37 C.F.R. § 42.104..... 27

35 U.S.C. § 102 11

35 U.S.C. § 314 33, 37

35 U.S.C. § 316 14

TABLE OF EXHIBITS

Exhibit No.	Description
2001	First Amended Docket Control Order, <i>BeSang Inc. v. Micron Tech., Inc.</i> , Case No. 2:23-cv-00028, Dkt. 54 (E.D. Tex. June 21, 2023)
2002	Docket for <i>BeSang Inc. v. Micron Tech., Inc.</i> , Case No. 2:23-cv-00028 (E.D. Tex.) (as of Aug. 28, 2023)
2003	RESERVED
2004	Defendants' Patent Local Rule 3-3 Disclosure of Invalidity Contentions, <i>BeSang Inc. v. Micron Tech., Inc.</i> , Case No. 2:23-cv-00028 (E.D. Tex. July 11, 2023) (cover pleading)
2005	Ann S. Mutschler, <i>Stanford, Korean nanofab center, Oregon-based semi startup claim 3D IC breakthrough</i> , EDN (Aug. 13, 2008), https://www.edn.com/stanford-korean-nanofab-center-oregon-based-semi-startup-claim-3d-ic-breakthrough/
2006	Press Release, <i>Micron and Intel Unveil New 3D NAND Flash Memory Technology Advancements Enable Three Times More Capacity than Other NAND Technologies</i> , Intel (Mar. 26, 2015), https://download.intel.com/newsroom/2021/archive/2015-03-26-news-releases-micron-and-intelunveil-new-3d-nand-flash-memory.pdf
2007	Peter Clarke, <i>EE Times updates list of emerging startups to version 8.0</i> , EE Times (Feb. 2, 2009), https://www.eetimes.com/ee-times-updates-list-of-emerging-startups-to-version-8-0/
2008	<i>Exploring the Potential of Emerging Semiconductor Technology</i> , Global Semiconductor Alliance Forum, Vol. 18, No. 2 (June 2011), https://www.gsaglobal.org/wp-content/uploads/2019/04/201102_GSA_Forum.pdf
2009	<i>Looking Beyond TSV For 3D IC Technology</i> , Frost & Sullivan (Mar. 2009), http://www.growthconsulting.frost.com/web/images.nsf/0/EF8B206A32BBD551652575B4002F3CD5/\$File/TIAlert.htm

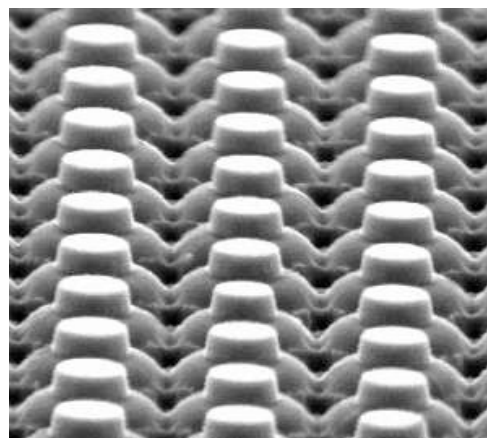
Micron Technology v. BeSang Inc.
Patent No. 7,378,702 – IPR2023-00900

Exhibit No.	Description
2010	Press Release, <i>Micron and Intel Extend their Leadership in 3D NAND Flash memory</i> , Globe News Wire (May 21, 2018), https://www.globenewswire.com/news-release/2018/05/21/1509614/14450/en/Micron-and-Intel-Extend-their-Leadership-in-3D-NAND-Flash-memory.html
2011	Micron Unveils 3D NAND (Mar. 26, 2015), https://www.youtube.com/watch?v=Lo-rsZ0vznw
2012	<i>Radar Scope</i> , Semiconductor Times, Vol. 12, No. 4 (Apr. 2007)
2013	RESERVED
2014	1/29/2007 Email from Peter Feeley to BeSang
2015	7/30/2007 Email exchange between Tom Arnold, Sang-Yun Lee, and others
2016	RESERVED
2017	RESERVED
2018	RESERVED
2019	U.S. District Courts – Combined Civil and Criminal Federal Court Management Statistics (June 30, 2023), https://www.uscourts.gov/statistics-reports/federal-court-management-statistics-june-2023

I. INTRODUCTION

Patent Owner BeSang Inc. is a pioneering fabless semiconductor company headquartered in Hillsboro, Oregon. BeSang was founded in 2003 with the mission of developing an innovative architecture for 3D memory. By 2008, it had done exactly that.

Collaborating with Stanford University and the National NanoFab Center, in 2008 BeSang achieved “a 3D IC technology breakthrough” by fabricating a 3D IC “on 8-inch wafers with industry standard 0.18 micron CMOS” memory cells “contain[ing] 128 million vertically oriented devices,” as shown at right. EX2005 at 1.



BeSang’s breakthrough received immediate industry praise and put the company on the map. The *EE Times* named BeSang to its prestigious Silicon 60 list of emerging startups. *See infra* § II.A.; EX2007 at 3. The Global Semiconductor Alliance called BeSang a “pioneer” in 3D solutions; *Semiconductor Times* complimented BeSang’s “single-chip, high-density 3D technology provid[ing] a low-cost, high-speed vertical memory solution”; and *Frost & Sullivan* lauded BeSang’s design as having “clear-cut winning edges” over existing technology. *See infra* § II.A.; EX2008 at 17; EX2012 at 1; EX2009 at 1.

Unsurprisingly, the big players in Silicon Valley noticed. Micron, Intel, and others met with BeSang about partnering with, or acquiring, BeSang’s technology. After in-depth discussions and meetings where Micron requested “specific information regarding the technology,” EX2015 at 1-2, and BeSang provided it, *see id.*, Micron decided to go its own way.

In 2015, Micron and Intel launched their first 3D commercial products, bragging and taking credit for “[t]his new 3D NAND technology, which was jointly developed by Intel and Micron, [and which] stacks layers of data storage cells vertically.” *See infra* § II.A.; EX2006 at 1. They extolled how “[t]his 3D NAND technology has the potential to create fundamental market shifts” and allowed for the “world’s highest-density flash memory.” EX2006 at 1. Their enthusiasm continued with the rollout of their follow-on 3D NAND products in 2018. *See infra* § II.A.; EX2010 at 1-2.

Five years later, after both were accused of patent infringement, Micron and Intel have changed their tune. Now slamming BeSang’s invention with two IPR petitions, they argue that BeSang’s 3D IC architecture would have been obvious. Paper 1 (“Pet.”) at 3-4; IPR2023-00991, Paper 2 at 3. But the 3D IC architecture that Micron and Intel were so eager to acquire was not obvious, and Micron’s Petition should be denied.

The Petition fails to meet its burden to show unpatentability on any ground. For the Watanabe Grounds 1 and 2, Micron relies on its own hindsight to pick and choose disparate features in volatile and non-volatile memory embodiments in an effort to satisfy the claim limitations. But the Petition is devoid of any explanation, let alone motivation, to combine these embodiments. Even if combined, Micron fails to show how its cobbled-together combination of embodiments satisfies the claim limitations. The Petition also does not meet its burden to show that Watanabe teaches an “SOI pillar,” rendering its arguments for Ground 2 moot.

The same problem unravels Grounds 3-6 based on the Lee reference. Again, Micron resorts to pointing to different features of Lee’s over one hundred pages of embodiments, which the patent says are mutually exclusive, with no articulated motivation to combine them.

Micron’s Petition is an archetype for hindsight bias. Obviousness requires consideration from “the perspective of one of ordinary skill in the art” at the time of the claimed invention. *Cheese Sys., Inc. v. Tetra Pak Cheese and Powder Sys., Inc.*, 725 F.3d 1341, 1352 (Fed. Cir. 2013). Since its inception, the Federal Circuit has warned against the creeping risk of hindsight in assessing obviousness:

To imbue one of ordinary skill in the art with knowledge of the invention in suit, when no prior art reference or references of record convey or suggest that knowledge, is to fall victim to the insidious

effect of a hindsight syndrome wherein that which only the inventor taught is used against its teacher.

W.L. Gore & Assocs., Inc. v. Garlock, Inc., 721 F.2d 1540, 1553 (Fed. Cir. 1983); *see also Polaris Indus. v. Arctic Cat*, 882 F.3d 1056, 1068 (Fed. Cir. 2018) (“We have observed that the prejudice of hindsight bias often overlooks that the genius of invention is often a combination of known elements which in hindsight seems preordained.” (citation and internal quotation marks omitted)).

As Micron itself recognized only five years ago, BeSang’s revolutionary 3D IC architecture is not obvious. The Board should reject Micron’s attempt to use hindsight to piece together isolated features in different embodiments without any motivation to combine them.

II. BACKGROUND

A. Background Of The Invention

Conventional CMOS technology relied on shrinking memory cells to obtain high-capacity storage devices. By the early 2000s, memory devices were approaching the constraints of Moore’s law, the 1965 prediction by Intel’s co-founder that the number of transistors that could be packed into a given area should be expected to double every two years. EX2006 at 1. An outside-the-box solution to further increase capacity was to go vertical. Much like skyscrapers increasing density by vertically stacking floors as compared to a single-story

building, stacking memory cells on top of each other could increase memory density in a given base area without shrinking individual memory cell size.

Compared to the high-temperature devices at the time, BeSang recognized the benefits of manufacturing its 3D integrated circuits at low process temperatures, *i.e.*, below 650°C, including gate oxidation at low temperatures. Among other benefits, BeSang discovered that if the gate dielectric layer has a combination of low temperature thermal oxide, high-K dielectric, and CVD dielectric, then device reliability increases, current-driving capability increases, and on-resistance decreases.

BeSang's innovative 3D IC technology received immediate praise. *Semiconductor Times* explained that "BeSang's 3D technology stacks multi-layer devices within a single chip" and that, "[a]s a result, this single-chip, high-density 3D technology provides a low-cost, high-speed vertical memory solution." EX2012 at 1. Stanford professor Dr. Yoshio Nishi said of BeSang's invention, "Conventional CMOS technology is facing its scaling limits. Therefore, this emerging 3D IC technology will extend the lifespan of CMOS technology, because it is an excellent alternative way to accommodate more devices on a given wafer area." EX2005 at 1. Dr. Simon Sze, the father of CMOS technology who co-invented the floating gate transistor at Bell Labs in 1967, praised "BeSang's

3D IC [as] a very attractive technology” and “one wonders why other companies have not thought about it.” *Id.* at 2.

BeSang’s innovative 3D architecture made the company famous. The following year, the *EE Times* named BeSang to its Silicon 60 list of emerging startups to watch. EX2007 at 3. The Global Semiconductor Alliance called BeSang a “pioneer in the design, development and delivery of unsurpassed three-dimensional (3D) IC solutions.” EX2008 at 17. Market research firm Frost & Sullivan lauded BeSang’s design as having “clear-cut winning edges” over existing technology and providing “freedom to build higher density IC chips by simply adding more layers in 3D directions in a cost-effective manner.” EX2009 at 1-2.

BeSang’s trajectory was not a forgone conclusion. Only a decade before founding BeSang, inventor Sang-Yun Lee immigrated from South Korea with a dream of completing his education in the United States. He first studied for a master’s degree at Washington University in St. Louis, then went on to the Ph.D. program at Arizona State University, eventually earning degrees in electrical engineering from both. After short stints as a low-level engineer at Motorola and Integrated Device Technology, he ventured out on his own in 2003 to found BeSang with the goal of pioneering 3D IC technology.

BeSang has been awarded over 20 U.S. patents for its innovative designs. One of those patents, U.S. Patent No. 7,378,702, is challenged here. The ’702 Patent was

Micron Technology v. BeSang Inc.
Patent No. 7,378,702 – IPR2023-00900

filed in 2004 and describes BeSang’s 3D IC invention. Titled “Vertical Memory Device Structures,” this foundational patent has been cited by more than 300 patents. The ’702 Patent describes increasing circuit density in ICs by using vertical memory cells to expand the memory array in a third dimension. EX1001 at 3:51-61, Fig. 1. It also teaches placing logic circuitry underneath the memory array to further increase density and achieve faster performance. *Id.* at 5:60-63. This invention not only reduces the cost per bit over existing memory architectures, but also improves reliability. EX2005 at 2.

After BeSang’s breakthrough and with patent applications filed, BeSang’s founder Sang-Yun Lee talked to Micron and Intel about partnering to commercially launch his 3D IC technology. Micron discussed acquiring the company, and Intel was interested in a joint venture. EX1019 ¶¶ 34-35; IPR2023-00991, EX1013 ¶ 29. In 2007, Micron asked BeSang for an “in-depth conversation about [its] technology and business.” EX2014 at 1. After BeSang met with Micron executives in person, Micron “found the technology very interesting” and asked for and received “specific information regarding the technology” including manufacturing details and testing data. EX2015 at 1-2.

Both companies instead decided to create 3D NAND products mimicking BeSang’s idea and introduced their own commercial offerings in 2015. EX2006 at 1-2; *see also* EX2011 (“rather than in prior technologies [that were] trying to cram

... more bits on one level of storage, we have now decided to go vertical”). With the launch, Micron and Intel were effusive with their praise of 3D NAND architecture:

- “This 3D NAND technology has the potential to create fundamental market shifts.” EX2006 at 1.
- “3D NAND technology [is] the world’s highest-density flash memory” that can “create storage devices with three times higher capacity than competing NAND technologies.” *Id.*
- The 3D NAND design “enables more storage in a smaller space, bringing significant cost savings, low power usage and high performance to a range of mobile consumer devices as well as the most demanding enterprise deployments.” *Id.*

Micron and Intel’s enthusiasm continued through its launch of more products in 2018:

- Their second-generation 3D NAND architecture “achieves 1 terabit (Tb) density per die, the world’s highest-density flash memory.” EX2010 at 1.
- “These advancements in the cell structure continue the companies’ leadership in producing the world’s highest Gb/mm² areal density.” *Id.*
- “We’re continuing flash technology innovation with our 96-layer structure, condensing even more data into smaller spaces, unlocking the possibilities of workload capability and application construction.” *Id.* at 2.

Just five years later, Micron and Intel challenge BeSang’s invention as obvious. *See* Pet. at 3-4; IPR2023-00991, Paper 2 at 3.

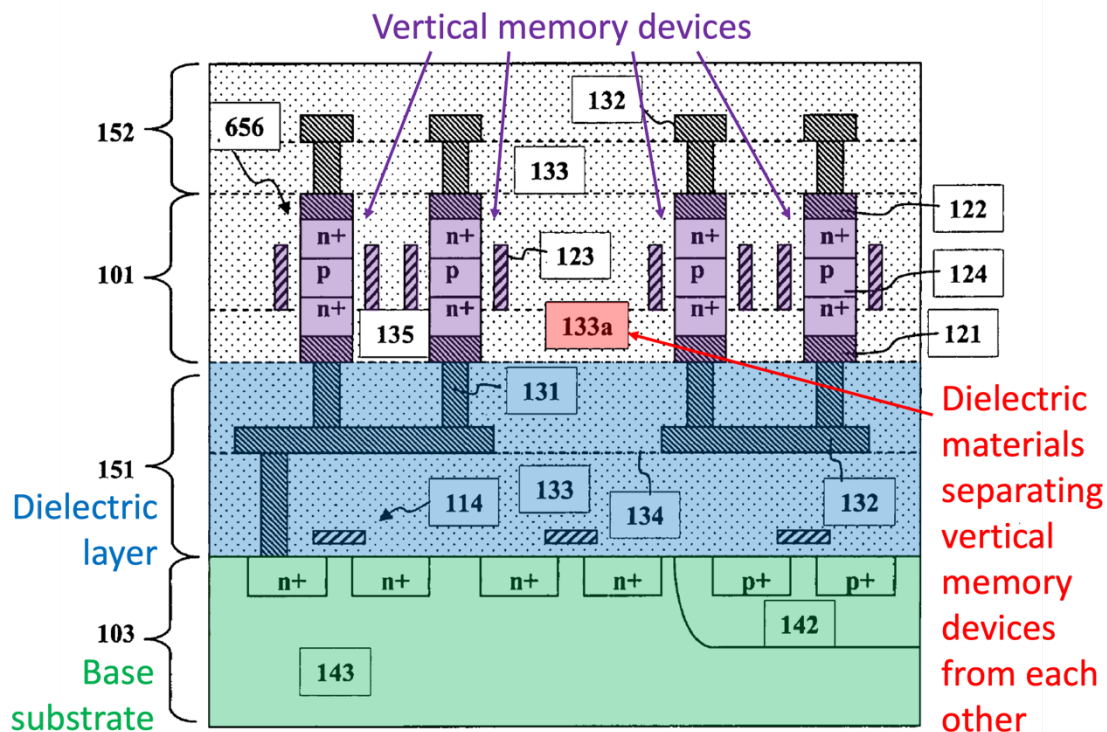
B. The Invention Of The '702 Patent

The '702 Patent is titled “Vertical Memory Device Structures.” The patent innovated by solving the significant practical challenges posed by scaling 2-dimensional memory technologies.

The '702 Patent recognized the need for “structures and methods that are suitable for providing increased circuit density in integrated circuits without necessarily requiring devices to be made smaller.” EX1001 at 1:40-43. It describes the use of vertical memory cells, which allows the memory array to expand in a third dimension, as well as putting logic circuitry underneath the memory array, which further increases density and helps achieve faster performance. *Id.* at 3:51-61, 5:60-63, Fig. 1.

Figure 1 of the '702 Patent, reproduced below, shows “vertical memory devices 656” that “are separated by isolation 135 and have floating structures in the filled dielectric materials 133a.” *Id.* at 5:18-21. Dielectric materials are those that are substantially nonconducting.

Fig. 1



Id. at Fig. 1 (annotated).

As shown in Figure 1, the vertical memory devices are separated from each other by dielectric materials 133a. *See id.* at 1:54-56 (“The regions around and between the vertically oriented memory devices, or cells may have dielectric material disposed therein.”), 6:6-8 (“Various embodiments of the present invention provide floating devices that are separated by dielectric isolation regions.”). Also shown in Figure 1 is dielectric layer 151 located above base substrate 103, *id.* at

Micron Technology v. BeSang Inc.
Patent No. 7,378,702 – IPR2023-00900

5:37-38, which can include electrical devices, such as transistors, *see, e.g., id.* at 10:8-9 (“The select transistors may be placed in base substrate 103”).

C. U.S. Patent No. 5,091,762 (“Watanabe”)

Watanabe pertained primarily to DRAM. EX1005 at 1:10-12 (“The present invention relates to a semiconductor memory device and, more particularly, to a semiconductor memory device used for a dynamic RAM.”). Watanabe disclosed nothing about a “pillar” semiconductor structure, much less an “SOI pillar.” *See generally* EX1005.

Micron asserts invalidity based on Watanabe both here and in the co-pending litigation. EX2004 at 5.

D. U.S. Patent No. 6,881,994 (“Lee”)

Lee issued on April 19, 2005, after the September 3, 2004 filing date of the ’702 Patent. EX1007 at 1. Lee is thus not prior art under 35 U.S.C. § 102(a) or (b) as the Petition asserts. Pet. at 11. Lee includes over one hundred figures reflecting numerous different embodiments. *See* EX1007 at 8:17-11:14, Figs. 1A-101.

Lee is used to assert invalidity both here and in the co-pending litigation. EX2004 at 6.

E. U.S. Patent Application Publication No. 2002/0154556 (“Endoh”)

The Petition relies on Endoh as a secondary reference solely for the challenged dependent claims. Pet. at 3-4.

Micron argues invalidity based on Endoh both here and in the co-pending litigation. EX2004 at 5.

F. Co-Pending Litigation On The '702 Patent

In January 2023, BeSang filed suit asserting the '702 Patent against Micron and Intel. *BeSang Inc. v. Micron Tech., Inc.*, No. 2:23-cv-00028 (E.D. Tex.); *BeSang Inc. v. Intel Corp.*, No. 3:23-cv-00113 (D. Or.). The Micron litigation is quickly advancing, and the Intel litigation is not far behind. Trial in the Micron case is set for November 18, 2024. EX2001 at 1. No stay pending IPR has been entered in either of the co-pending district court actions.

III. LEVEL OF ORDINARY SKILL IN THE ART

For purposes of denying institution and finding that Micron has not met its burden to show a reasonable likelihood of prevailing, BeSang submits that the Board need not determine the level of ordinary skill in the art. *Johnson & Johnson Surgical Vision, Inc. v. Alcon Inc.*, IPR2021-01003, 2021 WL 6338373, at *4 (P.T.A.B. Nov. 23, 2021) (denying institution: “For our analysis on whether to institute, we need not determine the level of ordinary skill in the art”).

BeSang reserves the right to address the level of ordinary skill in the event the Board institutes trial.

IV. CLAIM CONSTRUCTION IS NOT NECESSARY TO DENY INSTITUTION HERE

Micron asserts in the Petition that it “does not believe that any term requires explicit construction” in this proceeding. Pet. at 12. For purposes of denying institution because Micron has not met its burden to show a reasonable likelihood of prevailing, BeSang submits the Board need not construe any terms of the challenged claims. *Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (“The Board is required to construe ‘only those terms ... that are in controversy, and only to the extent necessary to resolve the controversy.’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

BeSang reserves the right to assert claim construction positions if trial is ordered.

V. THE PETITION’S CHALLENGES ARE NOT REASONABLY LIKELY TO PREVAIL

The Board should decline to institute trial because the Petition fails to show a reasonable likelihood of prevailing on any ground. Claim 13 is the sole independent claim challenged by Micron. All grounds rely on either Watanabe or Lee, and none of the Petition’s challenges are reasonably likely to prevail because Micron does not meet its burden to show obviousness based on either reference. Institution should therefore be denied.

A. Grounds 1 And 2 Based On Watanabe Are Not Reasonably Likely To Prevail

The Petition fails to demonstrate a reasonable likelihood of prevailing on its Grounds 1 and 2 challenges relying on Watanabe. The Petition never acknowledges, let alone satisfies its burden to show that it would have been obvious to combine Watanabe’s various embodiments to arrive at the claimed invention. *See, e.g., In re Stepan Co.*, 868 F.3d 1342, 1346 n.1 (Fed. Cir. 2017). Even if combined, the Petition does not show the combination meets the “memory cells” limitation for Grounds 1 and 2. Nor does Micron establish Watanabe taught or suggested the claimed “SOI pillar” in Ground 2. Neither Ground 1 nor 2 is reasonably likely to prevail.

1. Trial Should Not Be Ordered On Grounds 1 And 2 Because The Petition Makes No Showing Of A Motivation To Combine Watanabe’s Different Embodiments (Claims 13-17)

Micron fails to meet its burden to show obviousness of Claim 13 based on Watanabe. The Petition claims that a combination of Watanabe’s distinct embodiments teach or suggest the requirements of Claim 13, but never acknowledges its burden to show a motivation to combine them, let alone provides any argument or evidence supporting its combination.

“In an *inter partes* review, the burden of persuasion is on the petitioner to prove ‘unpatentability by a preponderance of the evidence,’ 35 U.S.C. § 316(e), and that burden never shifts to the patentee.” *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1375 (Fed. Cir. 2016) (quoting *Dynamic Drinkware, LLC v. Nat’l*

Graphics, Inc., 800 F.3d 1375, 1378 (Fed. Cir. 2015)). When a challenge is based on “combining multiple embodiments from a single reference ... there must be a motivation to make the combination and a reasonable expectation that such a combination would be successful, otherwise a skilled artisan would not arrive at the claimed combination.” *In re Stepan Co.*, 868 F.3d at 1346 n.1.

Ground 1 cherry-picks among various different embodiments in Watanabe with no articulated or credible motivation to combine them. *See* Pet. at 13-26. For the limitation the Petition labels as 13[b] (“a stackable add-on layer having a plurality of vertically oriented semiconductor memory cells”), *id.* at 16, the Petition’s Ground 1 challenge relies on Watanabe’s Figures 1 and 2A, which depict a DRAM cell. *E.g.*, *id.* at 16-18; EX1005 at 2:11-13 (“FIG. 2A is a sectional view of a part of the semiconductor memory device shown in FIG. 1”), 2:62-64 (“The structure of a MISFET, as an example of a DRAM cell, is shown in FIGS. 2A and 2B, FIG. 2A showing a sectional view of a part of the DRAM”). Yet, for limitation 13[d], which recites “wherein the memory cells are nonvolatile memory cells,” the Petition pivots to Watanabe’s Figure 7 depiction of an EPROM. Pet. at 25-26; EX1005 at 2:36-37 (“FIG. 7 is a sectional view showing a[n] application of the present invention into an EPROM.”). Thus, the Petition relies on separate embodiments to satisfy different limitations regarding the “memory cells.”

Despite relying on both the DRAM cell of Figures 1 and 2A for limitation 13[b] and the EPROM of Figure 7 for limitation 13[d], the Petition provides no explanation or teaching of how to combine Figure 7's embodiment with the Figure 2A embodiment in any way, much less a way that satisfies both limitations 13[b] and 13[d]. *See* Pet. at 16-18, 25-26. This shortcoming is fatal. *See, e.g., Unified Patents Inc. v. Multimedia Content Mgmt. LLC*, IPR2017-01934, 2019 WL 967806, at *2 (P.T.A.B. Feb. 25, 2019) ("For certain limitations, Petitioner cites only the embodiment shown in Figure 3A. But Petitioner cites all three embodiments, including the hypothetical embodiment, in support of other limitations Petitioner did not sufficiently explain how to combine these three embodiments in a way that teaches or suggests all of the limitations of claim 1." (internal citations omitted)).

Micron's proposed combination of embodiments, however, is fatal for another reason as well. The Petition fails to even allege, much less explain, why one of skill in the art would have been motivated to combine Watanabe's Figure 7 embodiment with the embodiment of Figures 1 and 2A or would have had a reasonable expectation of success. *See* Pet. at 25-26. Micron's citation to Watanabe's general statement that, "[t]he memory cell of the present invention is applicable to any type of memory device i.e., a SRAM, PROM, or a DRAM," *id.* at 25 (quoting EX1005 at 2:51-53), does not articulate a motivation to combine those different devices. It does not show why and how one of skill in the art would have combined the

structures of the DRAM cell of Figures 1 and 2A and the EPROM of Figure 7 to arrive at the claimed invention nor how the resulting combined structure would satisfy the claim limitations, and thus cannot save the Petitioner’s failure to make the required showing. *Cf. Markforged Inc. v. Continuous Composites, Inc.*, IPR2022-01220, 2023 WL 157619, at *9 (P.T.A.B. Jan. 11, 2023) (“Petitioner’s general assertion that ‘Lipsker discloses that combinations of the disclosed embodiments and features is proper,’ does not constitute a reasoned explanation regarding why the skilled artisan would have combined Lipsker’s precoating and non-precoating actuator embodiments to arrive at the claimed subject matter.” (internal citation omitted)).

Time and time again, the Board has explained that picking and choosing among features of disparate embodiments, with no motivation to combine them, does not meet Petitioner’s burden:

- *WhiteWater West Indus., Ltd. v. Am. Wave Machs., Inc.*, IPR2022-01035, 2022 WL 17071813, at *7 (P.T.A.B. Nov. 17, 2022) (“Petitioner does not acknowledge that it is relying on different embodiments for these claim limitations, much less explain how or why one of ordinary skill in the art would have combined them to achieve the claimed invention.”);
- *Lumenis Be Ltd. v. BTL Healthcare Techs. A.S.*, IPR2021-01280, 2022 WL 946534, at *8 (P.T.A.B. Mar. 9, 2022) (“Absent persuasive evidence

explaining how and why the embodiment of Figure 9B would be combined with the embodiment of Figure 35 with a reasonable expectation of success, it is not enough that Burnett '870 separately teaches an embodiment disclosing the claimed positioning of the applicator and an embodiment disclosing cooling an applicator.”);

- *Unified Patents Inc. v. GE Video Compression, LLC*, IPR2019-00726, 2019 WL 3714386, at *8 (P.T.A.B. Aug. 6, 2019) (“[W]e agree with Patent Owner that the Petition does not differentiate between the different embodiments disclosed in Howard nor does it provide any reason to combine the two.”).

The Petition’s picking and choosing among different features from disparate embodiments in Watanabe shows Micron’s impermissible hindsight reconstruction. Micron’s use of the claimed invention to cobble together an obviousness argument provides yet another basis to reject the Watanabe grounds. *See, e.g., Hewlett Packard Enter. Co. v. Intellectual Ventures II LLC*, IPR2022-00115, 2022 WL 946244, at *6 (P.T.A.B. Mar. 29, 2022) (denying institution and agreeing that “Petitioner’s combination of select features from Harari’s different embodiments to arrive at the invention of claim 1 is fraught with hindsight bias”); *see also ATD Corp. v. Lydall, Inc.*, 159 F.3d 534, 546 (Fed. Cir. 1998) (“Determination of obviousness

can not be based on the hindsight combination of components selectively culled from the prior art to fit the parameters of the patented invention.”).

Without any showing of a motivation to combine and a reasonable expectation of success, trial is futile because Micron cannot meet its burden on Ground 1. The Ground 2 challenge to dependent Claims 14-17 relies on, and thus suffers from the same deficiencies as, Ground 1. *See* Pet. at 26-46. Accordingly, the Board should find no reasonable likelihood of success on both Grounds 1 and 2.

2. Trial Should Not Be Ordered On Grounds 1 And 2 Because There Is No Showing That Watanabe Discloses Or Renders Obvious Limitation 13[b] (Claims 13-17)

Even if the Board combines the various Watanabe embodiments, Micron further fails to show that the DRAM embodiment it relies on satisfies the “memory cells” limitation in 13[b].

Limitation 13[b] requires a “plurality of vertically oriented semiconductor memory cells.” EX1001 at 12:29-30. Limitation 13[d] further requires that the “memory cells” be “nonvolatile memory cells.” *Id.* at 12:33-34. Thus, the “memory cells” in limitation 13[b] necessarily must be “nonvolatile memory cells” as well.

The Petition relies solely on DRAM memory for limitation 13[b]. *See* Pet. at 16-21. Micron does not assert that DRAM is nonvolatile memory, nor could it. *Id.* at 25 (“Watanabe discloses, ‘The memory cell of the present invention is applicable to any type of memory device i.e., a SRAM, PROM, or a DRAM.’

Ex-1005, 2:51-53. A POSITA would have understood that PROM memory devices are nonvolatile.”). Thus, Micron’s DRAM embodiment does not satisfy the nonvolatile “memory cells” requirement of Claim 13. *Cf. Nabors Drilling Techs. USA, Inc. v. Motive Drilling Techs., Inc.*, IPR2022-00327, Paper 30 at 29 (P.T.A.B. July 5, 2023) (“Petitioner has failed to establish that Pirovolou discloses or renders obvious the comparison recited by limitation [15.3] when read in context with limitation [15.4].”).

Micron’s alleged evidence of a “stackable add-on layer having a plurality of vertically oriented semiconductor memory cells” focuses on Watanabe’s Figures 1 and 2A as well as the methods shown in Figures 5 and 6. *See* Pet. at 16-21. The Petition quotes Watanabe’s description of Figure 2A as “a sectional view of a part of the semiconductor memory device shown in FIG. 1” *Id.* at 17 (quoting EX1005 at 2:11-13). The Petition also block quotes the paragraph beginning at column 2, line 62 of Watanabe, *id.* at 17-18, but Micron omits the beginning of that paragraph, which states, “The structure of a MISFET, as an example of a DRAM cell, is shown in FIGS. 2A and 2B” EX1005 at 2:62-63. Indeed, Watanabe plainly disclosed that Figures 1 and 2A depict a DRAM cell, which cannot be the “memory cells” required by limitation 13[b].

The Petition also relies on Figures 5 and 6, which depict the formation of DRAM cells as well. *See* Pet. at 18-21. Watanabe disclosed that creation of the

DRAM cell in Figure 2A involves the creation of a capacitor, which is the storage element in a DRAM: “Then, a thin insulating film 47 for the capacitor formation is formed on the layers 45, and a capacitor electrode material 46 is deposited over the surface of the resulting structure, followed by an insulating film 49.” EX1005 at 3:42-45; *see also* EX1006 ¶ 155 (“FIG. 13 is a plan view illustrating a memory cell array of DRAM structure having a MIS capacitor as a charge storage layer in a semiconductor memory device”).

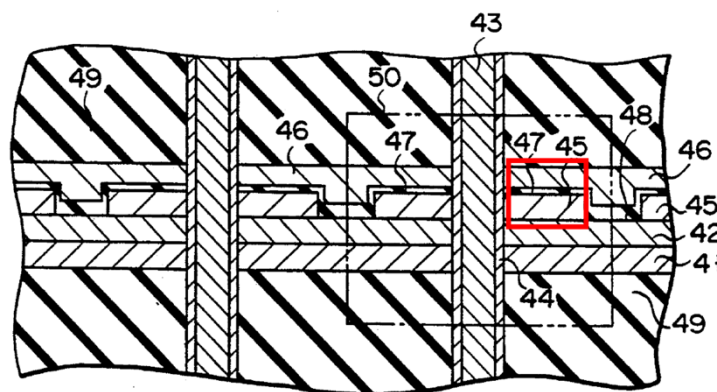
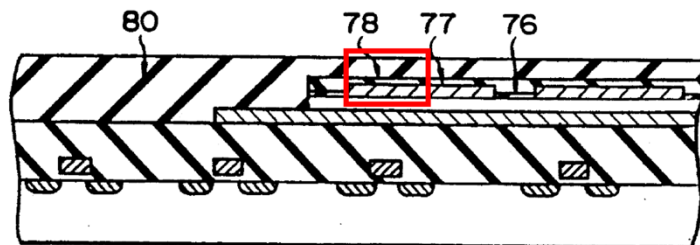


FIG. 2A

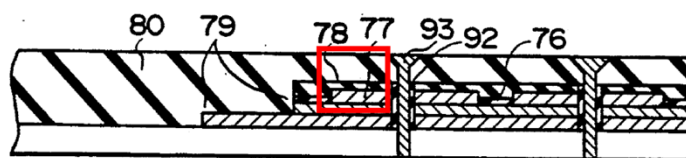
EX1005 at Fig. 2A (annotated).

Figures 5 and 6 of Watanabe depict formation of the same capacitor structure shown in Figure 2A and thus depict DRAM structures, which cannot satisfy limitation 13[b]. For example, Watanabe explains with reference to Figure 5B, “[C]apacitor insulating films 77 are formed, and additionally capacitor electrodes 78 are formed.” *Id.* at 5:20-22.



F I G. 5 B

Id. at Fig. 5B (annotated). Watanabe includes the same disclosure for Figure 6, stating, “As shown in FIG. 6B, a planar member is formed in a manner as shown in FIGS. 5A and 5B.” *Id.* at 5:64-65.



F I G. 6 B

Id. at Fig. 6B (annotated). Thus, Figures 1, 2A, 5, and 6 all depict the formation of DRAM cells, which cannot satisfy limitation 13[b]’s “memory cells” requirement as modified by limitation 13[d]’s requirement that the memory cells be “nonvolatile.”

The Petition’s only citation to anything other than DRAM in its discussion of limitation 13[b] is a brief citation in its “Lamination Method” section in which it simply cites Watanabe’s Figure 7 as follows: “Ex-1005, Fig. 7 (showing the source, channel, and drain in a vertical orientation).” Pet. at 21. This single citation provides no explanation or argument for how Figure 7 supplies a “stackable add-on layer

having a plurality of vertically oriented semiconductor memory cells” as required by limitation 13[b]. For example, there is no explanation or even argument as to how Watanabe disclosed the use of Figure 7 in a stackable add-on layer or whether such a hypothetical layer would have a plurality of memory cells of the type shown in Figure 7. *See id.*

Thus, to the extent Micron even relied on Figure 7, its showing there is deficient for institution as well. *See, e.g., Wolfspeed, Inc. v. The Trustees of Purdue Univ.*, IPR2022-00761, Paper 19 at 28 (P.T.A.B. July 20, 2023) (“We acknowledge that Petitioner, in a footnote ... alludes to an embodiment of Depetro’s source-region layout that includes the strongly doped p⁺ region of Figures 5, 6, and 7, but ultimately, we agree with Patent Owner that the Petition does not set forth a ground based on those figures with the clarity or particularity required to support institution of review.”). And, Micron cannot change theories after institution. *SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1348, 1358 (2018) (“The statute hinges inter partes review on the filing of a petition challenging specific patent claims; it makes the petition the centerpiece of the proceeding both before and after institution”); *South-Tek Sys., LLC v. Engineered Corrosion Sols., LLC*, 748 F. App’x 1003, 1007 (Fed. Cir. Sept. 20, 2018) (“South-Tek, however, waived this substitution theory by failing to argue it in its petition. ... Here, the Board recognized that South-Tek’s petition only argued that Wood’s condensate drain could be added to Viking, not that Wood’s

drain could replace Viking’s drum drip drains. Thus, the Board did not err by declining to consider South-Tek’s new theory that a person of ordinary skill would have been motivated to substitute Wood’s drain for Viking’s drains.” (internal citation omitted)).

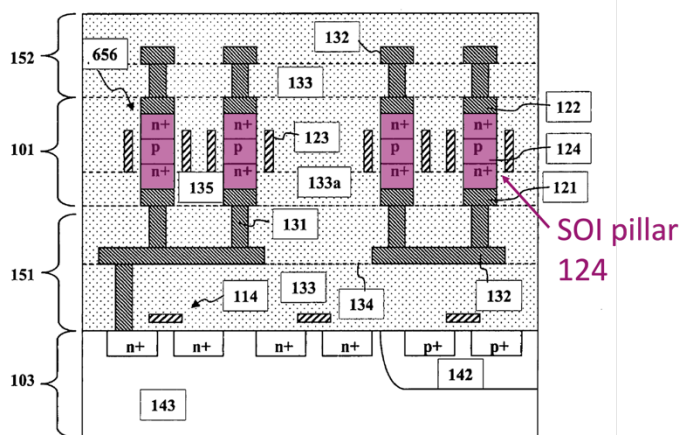
Because there is no showing that Watanabe discloses or renders obvious limitation 13[b], Watanabe Grounds 1 and 2 are not reasonably likely to prevail.

3. The Ground 2 Challenge To Claims 14-17 Fails Because The Petition Has Not Established Watanabe Teaches Or Suggests An SOI Pillar

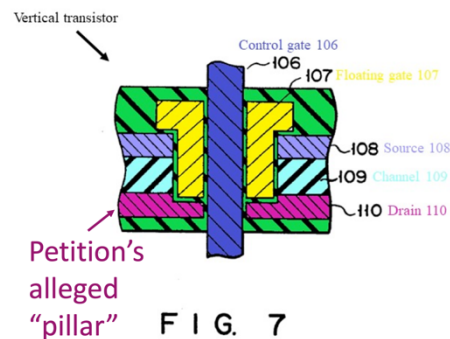
Ground 2 is additionally not reasonably likely to prevail because the Petition fails to show that Watanabe disclosed an “SOI pillar” required by each of dependent Claims 14-17. EX1001 at 12:35-52. For Claim 14, the Petition asserts that “Watanabe discloses or renders obvious forming a vertical transistor on a SOI pillar.” Pet. at 29. But Watanabe contains no disclosure of a “pillar,” and the Petition does not point to any. *See generally* EX1005; Pet. at 29-31.

The Petition cites Watanabe’s Figure 7 and asserts that “a POSITA would have understood (or found it obvious) that Watanabe’s vertical transistor *can be formed* on a SOI pillar.” Pet. at 29 (emphasis added). Below is a comparison of the ’702 Patent’s Figure 1, which shows pillars 124 (annotated in purple), EX1001 at 8:9, and Watanabe’s Figure 7 relied upon in the Petition.

Fig. 1



'702 Patent, Fig. 1 (annotated)



Pet. at 29 (label added)

The Petition asserts: “As shown in Figure 7, Watanabe discloses a vertical transistor comprising a semiconductor layer (110, purple) on a planar insulator layer (green). Thus, a POSITA would have understood (or found it obvious) that Watanabe’s vertical transistor can be formed on a SOI pillar.” Pet. at 29 (internal citations omitted). But the horizontal “layer” 110 relied upon by Micron is not in any way a pillar as required by the claim or as shown in the ’702 Patent’s Figure 1. Micron also cites a twin paragraph in Dr. Lee’s declaration which “merely parrots the words in the Petition.” *One World Techs., Inc. v. Chevron (HK) Ltd.*, PGR2020-00059, 2020 WL 7222691, at *16 (P.T.A.B. Dec. 7, 2020); compare Pet. at 29-30 with EX1002 ¶ 90. Offering “only a *verbatim* restatement of the assertion being supported, without any supporting evidence or technical reasoning” is insufficient and “particularly problematic in cases where, like here, expert testimony is offered

... to supply a limitation missing from the prior art.” *Xerox Corp. v. Bytemark, Inc.*, IPR2022-00624, 2022 WL 3648989, at *6 (P.T.A.B. Aug. 24, 2022) (precedential). For this reason alone, the Petition fails to demonstrate that Watanabe disclosed a “pillar.”

The Petition’s assertion that “a POSITA would have understood (or found it obvious) that Watanabe’s vertical transistor *can be formed* on a SOI pillar” fails to address whether Watanabe rendered a “pillar” obvious. Pet. at 29 (emphasis added); *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015) (“[O]bviousness concerns whether a skilled artisan not only *could have made* but *would have been motivated to make* the combinations or modifications of prior art to arrive at the claimed invention.”); *Panduit Corp. v. Dennison Mfg. Co.*, 774 F.2d 1082, 1092 n.16 (Fed. Cir. 1985) (“The question, however, is never whether an invention *could* be made, but whether there is anything in the prior art as a whole that would have rendered its making obvious to one skilled in the art when the invention was made”), *vacated and remanded on other grounds*, 475 U.S. 809 (1986).

For similar reasons, the Petition’s assertion that a “POSITA would have understood that epitaxial deposition is a *common method of forming* a SOI structure” also says nothing about a “pillar.” Pet. at 30 (emphasis added). The Petition’s reliance on Watanabe’s disclosure of an epitaxial method is also unhelpful because an epitaxial method can equally be used to form non-SOI structures. For example,

Watanabe disclosed that an “epitaxial method is used for forming” the layers in Figure 2, which does not show any “pillar.” EX1005 at 3:31-37; Figs. 2A and 2B. Neither of Micron’s assertions address the structural requirement of a “pillar.”

The Petition’s backup argument that “Watanabe in view of Endoh renders this limitation obvious” is also insufficient. Pet. at 31. The Petition relies on Watanabe in the proposed combination for the claimed “pillar,” stating that “a POSITA would have had a reasonable expectation of success in forming *Watanabe’s pillar* on a SOI wafer, as described in Endoh.” *Id.* at 33 (emphasis added). But as explained, Watanabe did not disclose a pillar structure, and therefore, the combination’s express reliance again on Watanabe providing a “pillar” cannot satisfy Micron’s obligation to “specify where each element of the claim is found” in the combination of Watanabe and Endoh. 37 C.F.R. § 42.104(b)(4).

Finally, the Petition’s vague reference to “combin[ing] Watanabe with Endoh’s teachings of a SOI pillar,” Pet. at 32, occurs in the context of its backup argument where it expressly relies on “forming Watanabe’s pillar on a SOI wafer,” *id.* at 33. Even if considered, the Petition’s ambiguity regarding where the alleged “pillar” teaching in the proposed combination originates unravels its challenge in Ground 2. *See, e.g., Health Care Logistics, Inc. v. Kit Check, Inc.*, IPR2019-00394, 2019 WL 2461793, at *5 (P.T.A.B. June 11, 2019) (denying institution where petition “does not clearly explain whether Petitioner contends that each reference

teaches the limitation, independently, or that only the combination of the two references teaches the limitation”).

Because the Petition makes no showing that Watanabe disclosed an SOI pillar, the Petition’s Ground 2 challenge to Claim 14 fails. The Petition’s Ground 2 challenges to Claims 15-17 rely on the same arguments for Claim 14 for “SOI pillar,” Pet. at 33, 37, 42-43, and thus fail for at least the same reasons.

B. Grounds 3-6 Based On Lee Are Not Reasonably Likely To Prevail

The Petition does not demonstrate a reasonable likelihood of prevailing on its Grounds 3-6 obviousness challenges relying on Lee. Micron has not shown it would have been obvious to combine Lee’s different embodiments in its Ground 3 challenge to Claim 13 to arrive at the claimed invention. As with the Watanabe grounds, the “Federal Circuit has held that the requirement to articulate specific reasoning for the combination similarly exists when combining multiple embodiments from a single reference.” *Unified Patents*, 2019 WL 3714386, at *8 (citing *Stepan*, 868 F.3d at 1346 n.1). The Petition’s Ground 3 challenge to Claim 15, which combines selected features of alternative embodiments, independently fails for similar reasons. Grounds 3-6 are riddled with hindsight and not reasonably likely to prevail.

1. Trial Should Not Be Ordered On Grounds 3-6 Because There Is No Showing That Combining Lee’s Different Embodiments Would Have Been Obvious (Claims 13-17)

Micron fails to meet its burden to show obviousness of Claim 13 based on Lee. *See Magnum Oil Tools*, 829 F.3d at 1375. The Petition’s Ground 3 challenge to Claim 13 relies on a collage of multiple different combinations of Lee’s embodiments to argue obviousness, as shown below.

Claim 13 Limitation	Embodiment(s)
13[a]	Figure 35 (Pet. at 47-48)
13[b]	Figures 1A and 35 (<i>Id.</i> at 48-50)
13[c]	Figures 35 and 83A (<i>Id.</i> at 50-52)
13[d]	Figure 1A (<i>Id.</i> at 53-54)

Grounds 3-6 are predicated on the same combinations to show obviousness of Claim 13. *See* Pet. at 54-74. Accordingly, they are defective for the same reasons.

Lee explains that it includes multiple discrete embodiments, including “a pillar TFT EEPROM, a pillar diode with a charge storage region, a self aligned TFT EEPROM, a rail stack TFT EEPROM, and various other configurations.” EX1007 at 12:55-57. For Claim 13, limitation 13[b], the Petition relies on Figure 1A, Pet. at 48-50, which is a “pillar memory device.” EX1007 at 14:11-13. For limitation 13[c], the Petition relies on Figure 83A, Pet. at 50-52, which is a “flash memory

array in a rail stack configuration.” EX1007 at 55:26-28. Lee explained that the “pillar” devices and “rail stack” devices are alternative embodiments. *Id.* at 55:8-12 (“The TFT EEPROMs may be arranged in the pillar, self-aligned TFT *or* rail stack configurations of the previous embodiments. Preferably, the TFT EEPROMs are arranged in the rail stack configuration.” (emphasis added)).

However, the Petition includes no showing why one of skill in the art would have been motivated to combine Lee’s assorted embodiments across Lee’s 128 pages and had a reasonable expectation of success, or even what such a hybrid structure might look like. *See* Pet. at 46-54. The Petition again cherry-picks features among Lee’s many embodiments to allegedly arrive at the claimed invention. *Id.* But the Petition provides no explanation of why or how Figure 83A’s “flash memory array in a rail stack configuration,” EX1007 at 55:26-28, would be combined with the “pillar” device of Figure 1A, *id.* at 14:11-13. Nor does the Petition explain what features the resulting combination would have, let alone how the resulting combination would satisfy all the limitations of Claim 13.

Absent the required showing of a motivation to combine and a reasonable expectation of success, the Petition’s challenge based on Lee must fail. *Stepan*, 868 F.3d at 1346 n.1; *see also WhiteWater*, 2022 WL 17071813, at *7 (“Petitioner does not acknowledge that it is relying on different embodiments for these claim limitations, much less explain how or why one of ordinary skill in the art would have

combined them to achieve the claimed invention.”); *Lumenis*, 2022 WL 946534, at *8 (“Absent persuasive evidence explaining how and why the embodiment of Figure 9B would be combined with the embodiment of Figure 35 with a reasonable expectation of success, it is not enough that Burnett ’870 separately teaches an embodiment disclosing the claimed positioning of the applicator and an embodiment disclosing cooling an applicator.”); *Unified Patents*, 2019 WL 3714386, at *8 (“[W]e agree with Patent Owner that the Petition does not differentiate between the different embodiments disclosed in Howard nor does it provide any reason to combine the two.”).

The Petition’s selection of disparate features from multiple, different embodiments in Lee is also evidence of Micron’s impermissible hindsight reconstruction, which is yet another basis to reject the Petition’s challenge based on Lee. *See, e.g., Hewlett Packard Enter.*, 2022 WL 946244, at *6 (denying institution and agreeing that “Petitioner’s combination of select features from Harari’s different embodiments to arrive at the invention of claim 1 is fraught with hindsight bias”); *see also ATD Corp.*, 159 F.3d at 546.

Because the Petition includes no showing that it would have been obvious to combine the different embodiments of Lee, the Petition’s Grounds 3-6 challenges are not reasonably likely to prevail.

2. The Ground 3 Challenge To Claim 15 Fails Because It Combines Alternative Embodiments With No Explanation Why Or How One Of Skill In The Art Would Have Done So

Ground 3’s challenge to Claim 15 is also not reasonably likely to prevail because the Petition attempts to combine even more alternative embodiments in Lee without any explanation why or how one of skill in the art would have done so. Claim 15 depends from Claim 13. EX1001 at 12:39-42. For limitation 13[c], the Petition’s Ground 3 challenge relies on Lee’s Figure 83A “flash memory array in a rail stack configuration,” EX1007 at 55:26-28, which shows a floating gate 5247. *Id.* at 56:8-10 (“[I]n the example of FIGS. 83A and B, the charge storage region 5241 comprises a polysilicon floating gate 5247”); Pet. at 51. For Claim 15, the Ground 3 challenge next relies on Lee’s Figure 7, which illustrates an embodiment of a “pillar memory ... having a charge trapping dielectric.” EX1007 at 8:40-42; Pet. at 58-59. The Petition provides no explanation why one of skill in the art would have combined the embodiments of Figures 7 and 83A, which disclose alternative structural arrangements (pillar versus rail stack) as well as alternative charge trap and floating gate approaches, much less attempt to explain how combining mutually exclusive technologies would have been possible.

The Board should thus find no reasonable likelihood of success on the Ground 3 challenge to Claim 15 for the additional reason that the Petition fails to explain its proposed combination of yet another alternative embodiment. *See, e.g.,*

WhiteWater, 2022 WL 17071813, at *7 (unclear “how or why the skilled artisan” would have combined embodiments where reference “appears to characterize SAS and ASCS as two distinct, mutually exclusive methods of dealing with compressor surge”); *Amazon.com, Inc. v. AlmondNet, Inc.*, IPR2022-01455, Paper 12 at 16 (P.T.A.B. Apr. 6, 2023) (“[T]he Petition relies on two alternative embodiments for its invalidity theory without sufficient explanation of how or why a person of ordinary skill in the art would have combined these embodiments.”).

The Board should decline to institute.

VI. THE BOARD SHOULD EXERCISE ITS DISCRETION TO DENY INSTITUTION UNDER *FINTIV*

The Board should also discretionarily deny institution under 35 U.S.C. § 314(a) because none of the *Fintiv* factors support instituting trial. *See Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, 2020 WL 2126495, at *2 (P.T.A.B. Mar. 20, 2020) (precedential); *see also Mylan Labs. Ltd. v. Janssen Pharmaceutica NV*, IPR2020-00440, 2020 WL 5580472, at *11 (P.T.A.B. Sept. 16, 2020) (“No factors in our analysis weigh towards institution.”).

A. Factor 1: Whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted.

Micron agrees that *Fintiv* factor 1 is neutral. Pet. at 74. The district court has not ruled on Micron’s opposed stay motion. EX2002 at 3-5; *see also Code200 v. Luminati Networks Ltd.*, IPR2020-01266, 2020 WL 7682243, at *3 (P.T.A.B. Dec.

23, 2020) (factor neutral where Judge Gilstrap had not yet ruled on petitioner’s opposed motion to stay filed after the IPR petition was filed).

B. Factor 2: The proximity of the court’s trial date to the Board’s projected statutory deadline for a final written decision.

Micron’s co-pending litigation in Texas will undoubtedly go to trial first. The median time to trial in the Eastern District of Texas predicts a June 2024 civil trial date—five months before the anticipated Final Written Decision deadline here. EX2019 at 35 (16.7 months median time from filing to trial); Paper 5. Even Petitioner’s outdated statistics predict an August 2024 trial date, months before the statutory deadline. EX1017 at 35 (19 months median time from filing to trial); Pet. at 75 (incorrectly asserting that “trial is expected November 2024” based on EX1017); *see also* Director’s Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation (June 21, 2022), at 8-9. The November 18, 2024 trial date is also before the statutory deadline. EX2001 at 1. Given the earlier trial date, Micron concedes that *Fintiv* factor 2 weighs “slightly in favor of denial.” Pet. at 75.

C. Factor 3: Investment in the parallel proceeding by the court and the parties.

The co-pending district court case has been moving forward since January 2023. Infringement and invalidity contentions have been exchanged, and discovery and depositions are underway. EX2001 at 5. By the Board’s institution

deadline on November 28, 2023, *see* Paper 5, the parties will be in the home stretch of discovery. EX2001 at 3 (showing completion of fact discovery by June 12, 2024). Based on the considerable resources already expended on contentions and discovery in the district court, *Fintiv* factor 3 weighs “in favor of denying institution.” *See, e.g., TCO AS v. NCS Multistage Inc.*, PGR2020-00077, 2021 WL 662165, at *5-6 (P.T.A.B. Feb. 18, 2021) (as of the preliminary response filing, the parties had “exchanged infringement contentions and invalidity contentions and exchanged substantial document productions”).

D. Factor 4: Overlap between issues raised in the petition and in the parallel proceeding.

Micron’s invalidity contentions in the parallel litigation plainly contradict its assertion that “this IPR is the only venue in which the invalidity challenges against several claims in the ’702 Patent will be adjudicated.” Pet. at 76. Micron’s invalidity contentions challenge the same Claims 13-16 based on the identical Watanabe, Lee, and Endoh references relied upon in the Petition. EX2004 at 1, 5-6, 9. Despite the overlap in issues raised in the Petition and at the district court, Micron provided no stipulation, much less a *Sotera* stipulation, to eliminate the duplication between the two proceedings, which weighs strongly in favor of denying institution. *See, e.g., KeyMe, LLC v. Hillman Grp., Inc.*, IPR2020-01028, 2021 WL 129094, at *6 (P.T.A.B. Jan. 13, 2021) (factor supports denial because “Petitioner

fails to stipulate that it will not pursue in the district court any ground raised or that could have reasonably been raised in this proceeding”); *Code200*, 2020 WL 7682243, at *4 (factor “strongly favors” denial notwithstanding that “the Petition challenges four claims that are not asserted in the Texas litigation”).

E. Factor 5: Whether the petitioner and the defendant in the parallel proceeding are the same party.

Factor 5 also supports denial of institution. Micron is both the Petitioner here and the defendant in the parallel Texas litigation. Micron does not dispute that this factor favors discretionary denial. *See* Pet. at 76.

F. Factor 6: Other circumstances that impact the Board’s exercise of discretion, including the merits.

Where “the Board’s analysis of *Fintiv* factors 1-5 favors denial of institution, the Board shall then assess compelling merits.” *CommScope Techs. LLC v. Dali Wireless, Inc.*, IPR2022-01242, 2023 WL 2237986, at *2 (P.T.A.B. Feb. 27, 2023). As explained, Micron’s patentability challenge is deeply flawed because the Petition is riddled with hindsight and fails to show obviousness for any grounds. The weakness of the Petition’s merits heavily favors discretionary denial. *See, e.g.*, *Code200*, 2020 WL 7682243, at *5 (“[W]e do not find that the merits outweigh the other *Fintiv* factors favoring denial of institution.”); *Fitbit, Inc. v. Philips N. Am. LLC*, IPR2020-00828, 2020 WL 6470312, at *9 (P.T.A.B. Nov. 3, 2020) (“[T]he merits of the proceeding weigh in favor of denying institution”).

G. None Of The *Fintiv* Factors Supports Institution

The weight of the *Fintiv* factors supports the Board exercising its discretion to deny review under Section 314(a) here, thereby conserving Board and party resources and preventing duplicative proceedings evaluating the same invalidity challenges against the same patent. None of the six *Fintiv* factors supports institution here.

VII. CONCLUSION

For any of these reasons, the Board should deny institution of the Petition.

ARMOND WILSON LLP

Dated: August 28, 2023

By: /Michelle E. Armond/
Michelle E. Armond (Reg. No. 53,954)
Douglas R. Wilson (Reg. No. 54,542)
Joseph Li (Reg. No. 74,998)
Yue Han (Reg. No. 80,950)
Attorneys for BeSang Inc.

CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(d), the undersigned certifies that foregoing **PATENT OWNER’S PRELIMINARY RESPONSE**, exclusive of the parts exempted as provided in 37 C.F.R. § 42.24, contains 7,788 words and therefore complies with the type-volume limitations of 37 C.F.R. § 42.24.

ARMOND WILSON LLP

Dated: August 28, 2023

By: /Michelle E. Armond/

Michelle E. Armond (Reg. No. 53,954)

Douglas R. Wilson (Reg. No. 54,542)

Joseph Li (Reg. No. 74,998)

Yue Han (Reg. No. 80,950)

Attorneys for BeSang Inc.

CERTIFICATE OF SERVICE

The undersigned certifies that pursuant to 37 C.F.R. § 42.6(e), a true copy of the foregoing **PATENT OWNER’S PRELIMINARY RESPONSE** is being served electronically on August 28, 2023 to the following lead counsel for Petitioner to the following email addresses:

John Kappos
jkappos@omm.com

Xin-Yi Zhou
vzhou@omm.com

Ben Haber
bhaber@omm.com

William M. Fink
tfink@omm.com

Patric Reinbold
preinbold@omm.com

OMMBESANGMICRON@omm.com

ARMOND WILSON LLP

Dated: August 28, 2023

By: /Michelle E. Armond/
Michelle E. Armond (Reg. No. 53,954)
Douglas R. Wilson (Reg. No. 54,542)
Joseph Li (Reg. No. 74,998)
Yue Han (Reg. No. 80,950)
Attorneys for BeSang Inc.