

Looking Beyond TSV For 3D IC Technology

Three-dimensional (3D) packaging is an integrated circuit (IC) packaging technique that takes IC technology a step ahead in the Moore's curve. With a lot spoken about difficulty into progressing ahead along the Moore's curve, there are a lot of development initiatives in a number of components of the IC technology. 3D IC technology is definitely a promise toward higher levels of miniaturization and integration, which focuses on portraying advances in interconnect technologies and reducing interconnect delays. 3D IC technologies promise significant increase of functionality and performance of components by heterogeneous integration of materials, devices, and signals. Interconnects and bonding technologies are two important aspects of development in the evolution of 3D technologies.

There are numerous efforts around 3D IC technologies and with the amount of focus it is gaining, evolving technological solutions have to essentially address critical challenges in this demanding space. The concept 3D IC was first introduced at the package level, which involves simply stacking multiple semiconductor chips and electrically connecting them using wires,. The industry then moved a step forward in introducing what was called through silicon vias (TSV), in an attempt to increase the number of feasible interconnects and enhance electrical performance. With the introduction of TSV, a 3D package was slowly evolving to become a 3D IC technology. TSV has in fact become the focus of the industry to an extent that the whole evolution of 3D IC is centered on TSV. It is an acceptable fact that TSV evolved as a very promising solution, but there are a few challenges restraining the industry from moving forward in actually commercializing 3D IC with TSV. Primarily, TSV demands for a precise alignment of chips, which eventually requires a highly accurate alignment controlled bonding technique or the usage of a large TSV pad. Secondly, TSV have not evolved to be very cost-efficient. In the current scenario, it would not be wrong to say that TSV is an expensive process. Industrial opinions cite that one must justify the need for using 3D IC from an application perspective.

Addressing needs in this direction, BeSang Inc., a semiconductor company has developed a proprietary Single Chip 3D IC technology, which enables the development of higher density memory arrays using vertically oriented transistors. One of the cited benefits of BeSang's 3D IC technology is that it can be cost-effectively implemented in existing complementary metal oxide semiconductor (CMOS) facilities without significant modification of existing equipment or process flows. The technology also can be used to produce low-cost stand-alone memories (volatile or nonvolatile) and high-performance embedded memories for system-on-a-chip (SoC), central processing unit (CPU), digital signal processor (DSP), and application-specific integrated circuits (ASIC) by separating embedded memories from neighboring logic circuits and fabricating the memories on top of the logics with the 3D technologies. BeSang's Single Chip 3D IC is very different from conventional package level 3D ICs. Instead of fabricating two separate chips (or wafers) and bonding, the single chip 3D IC technology transfers thin single crystalline silicon on top of first substrate and then builds device layers in it. BeSang successfully demonstrated a fully functioning single chip 3D IC in 0.18 micrometer technology on an 8-inch wafer recently.

From a benefit perspective, Besang's 3D IC solution has got clear-cut winning edges when compared to both conventional 3D packaging technologies and TSV-based 3D IC technologies. Primarily, the cost and size of the die is significantly low when compared to the competing 3D counterparts. Dramatic reductions in die size have been achieved because the devices are now implemented in two or more layers and through the reduction of memory cell size. Secondly, the ability to offer unrestricted 3D interconnects enables the development of high-speed 3D devices. Conventional 3D packaged devices have limited interconnects between top and bottom circuits because they require precise wafer alignment, large landing pads, and TSV. In general, the number of interconnects is less than 1000 per chip, which is insufficient for high-speed 3D IC operations. For BeSang's 3D ICs, there is no restriction of number of 3D interconnects because the donor wafer is not patterned before wafer bonding and 3D interconnects are implemented using conventional vias. Hence, millions of 3D interconnects can be implemented in BeSang's 3D IC. A reduced interconnect length is yet another attribute that makes Besang's single chip 3D IC solution a very competing solution in the emerging 3D IC space.

With the development of the Single Chip 3D IC solution, Besang Inc. has proved that it is feasible to

produce cost-efficient 3D IC devices. With this solution, the industry will no longer need to rely on reducing device dimensions for achieving miniaturization, which requires huge investment in expensive lithography tools. It will get freedom to build higher density IC chips by simply adding more layers in 3D directions in a cost-effective manner. With around six granted patents and 20 patents pending around this technology, BeSang Inc. single chip 3D IC solution is poised to carry 3D integration forward toward numerous applications that can be commercialized.

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