

Subject: RE: BeSang - Thank you

Date: Thursday, August 2, 2007 at 1:24:02 PM Pacific Daylight Time

From: ahill@micron.com

To: sangyun.lee@besang.com

Hello Sang-Yun

I would think your technology would also be very interesting for large ASICs requiring flash. You mentioned one specialty application. I could think of another one in the mobile area. E.g. mobile processors are stacking NAND using PoP or MCP packaging approaches. If you like I could introduce you to a person at TI who may be able to help if you don't have a contact already.

It was good to talk and meet with you

Keep in touch

Best

Achim

From: Sang-Yun Lee [mailto:sangyun.lee@besang.com]

Sent: Monday, July 30, 2007 5:16 PM

To: tjarnold

Cc: jpawlowski; jerryjohnson; ahill; pfeeley; spking

Subject: RE: BeSang - Thank you

Tom

Presentation slides that I used at the meeting are attached for your information.

Also, find my answers to your questions below. I hope my answers are clear to you. If not, please let me know.

Thank you very much.

Best regards,

Sang-Yun Lee

CEO at BeSang Inc.

From: tjarnold@micron.com [mailto:tjarnold@micron.com]

Sent: Monday, July 30, 2007 8:43 AM

To: sangyun.lee@besang.com

Cc: jpawlowski@micron.com; jerryjohnson@micron.com; ahill@micron.com; pfeeley@micron.com; spking@micron.com

Subject: RE: BeSang - Thank you

Sang-Yun,

Thanks for taking the time to visit us and present your technology. We found the technology very interesting, and if possible to implement in a manufacturable way, could create market opportunities. We would like to review your technology with some of our internal process technologists as a next step. I would appreciate it if you could provide me a copy of your presentation as well as any other specific information regarding the technology. Specifically, if you could share the following it would be helpful.

Top level process flow defining mask steps:

Step 1. Pillar photo, Step 2. Pillar (silicon) etch, Step 3. Gate oxidation (including sacrificial oxidation and cleaning) at low temp., Step 4. Gate deposition, Step 5. Gate etch (wordline forms automatically using spaces between pillars), Step 6. Dielectric layer depo & CMP, Step 7. Contact photo, Step 8. Contact etch, Step 9. Contact plug formation, Step 10. Metal depo, Step 11. Metal photo, Step 12. Metal etch

Process used to thin top NPN layer for transistor formation.

Step 1. Starting with p-epi on n+ wafer, Step 2. 10nm Pad oxidation, Step 3. n+ drain implantation, Step 4. Wafer anneal at high temperature

Description of vertical transistor formation, including flash cell, oxide composition and thickness.

Thickness of dielectric films are design parameter. So, the number can be changed if needed for certain device design. In case of the prototype, BeSang choose 9nm oxide for tunneling oxide because the channel

length was designed to be ~0.25um and operation voltage was 3V. For multi-bit, ONO was used. Find the slides for device characterization for more information.

Any device characterization or measurements.

In addition to the data shown in presentation, more characterization data are attached.

Once we review this with our technologists, I will provide you some feedback and we can discuss next steps.

Best Regards,

Tom Arnold

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From: Sang-Yun Lee [<mailto:sangyun.lee@besang.com>]
Sent: Sunday, July 29, 2007 3:43 AM
To: jpawlowski; tjarnold; jerryjohnson; ahill; pfeeley; spking
Subject: BeSang - Thank you

Hello all

It was very nice to introduce BeSang's 3D Enabling Technology to you.

Per Achim's request, data for low temp oxidation is attached. More data might be available directly from TEL.

If you have any question or any additional information is needed, please feel free to let me know. I can be also reached by cell phone at 503-502-3366.

I really appreciate your interest in BeSang.

Best regards,

Sang-Yun Lee
CEO of BeSang Inc.
Ph) 503-502-3366
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