

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
MICRON SEMICONDUCTOR PRODUCTS, INC., and
MICRON TECHNOLOGY TEXAS, LLC,
Petitioner

v.

BESANG INC.,
Patent Owner.

Case No. IPR2023-00900
U.S. Patent No. 7,378,702

**PETITIONER'S PRELIMINARY REPLY
IN SUPPORT OF
INTER PARTES REVIEW OF U.S. PATENT NO. 7,378,702**

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UPDATED LIST OF EXHIBITS¹

Ex-1001	U.S. Patent No. 7,378,702 (“the ’702 Patent”)
Ex-1002	Declaration of Dr. Jack C. Lee
Ex-1003	Curriculum Vitae of Dr. Jack C. Lee
Ex-1004	Prosecution History of U.S. Patent No. 7,378,702 (App. No. 10/934,270)
Ex-1005	U.S. Patent No. 5,091,762 (“Watanabe”)
Ex-1006	U.S. Patent Application Pub. No. US2002/0154556 (“Endoh”)
Ex-1007	U.S. Patent No. 6,881,994 (“Lee”)
Ex-1008	U.S. Patent No. 7,221,008 (“Matamis”)
Ex-1009	G. Groeseneken et al., <i>Basics of Nonvolatile Semiconductor Memory Devices</i> , in <i>Nonvolatile Semiconductor Memory Technology: A Comprehensive Guide to Understanding and Using NVSM Devices</i> (William D. Brown & Joe Brewer eds., 1997)
Ex-1010	Philip M. Sailer et al., <i>Creating 3D Circuits Using Transferred Films</i> , IEEE Circuits & Devices (1997)
Ex-1011	U.S. Patent No. 5,808,938 (“Tran”)
Ex-1012	U.S. Patent No. 6,982,905 (“Nguyen”)
Ex-1013	U.S. Patent No. 6,807,098 (“Jeong”)
Ex-1014	Kee-Ho Yu et al., <i>Real-Time Microvision System with Three-Dimensional Integration Structure</i> , IEEE Int’l Conference on Multisensor Fusion and Integration for Intelligent Sys. (1996)
Ex-1015	U.S. Patent No. 5,374,564 (“Bruel”)
Ex-1016	Horacio Mendez, <i>Silicon-on-Insulator: SOI Technology and Ecosystem – Emerging SOI Applications</i> , SOI Indus. Consortium (2009)
Ex-1017	U.S. District Courts – Combined Civil and Criminal Federal Court Management Statistics (Dec. 31, 2022), available at: https://www.uscourts.gov/statistics-reports/federal-court-management-statistics-december-2022

¹ Four-digit pin citations that begin with 0 are the page stamps added by Micron in the bottom right corner of the exhibits. All other pin citations are to original page, column, paragraph, or line numbers.

Ex-1018	T. Mikolajick et al., <i>The Future of Charge Trapping Memories</i> , 2007 IEEE Int'l Symposium on VLSI Tech., Sys. & Applications (2007)
Ex-1019	Complaint, <i>BeSang Inc. v. Micron Tech., Inc.</i> , No. 2:23-cv-00028 (E.D. Tex. Jan. 23, 2023)
Ex-1020	Jim Handy, <i>3D NAND: Benefits of Charge Traps over Floating Gates</i> , The Memory Guy Blog (Nov. 22, 2013)
Ex-1021	E. Bertagnolli et al., <i>ROS: An Extremely High Density MASK ROM Technology Based on Vertical Transistor Cells</i> , IEEE (1996)
Ex-1022	Tetsuo Endoh et al., <i>Novel Ultrahigh-Density Flash memory with A Stacked-Surrounding Gate Transistor (S-SGT) Structured Cell</i> , 50 IEEE Transactions on Electron Devices 945 (2003)
Ex-1023	F. Nemati & J.D. Plummer, <i>A Novel High Density, Low Voltage SRAM Cell with A Vertical NDR Device</i> , IEEE (1998)
Ex-1024	K.W. Lee et al., <i>Three-Dimensional Shared Memory Fabricated Using Wafer Stacking Technology</i> , IEEE (2000)
Ex-1025	<i>NAND vs. NOR Flash Memory</i> , Toshiba America Electronic Components, Inc. (2006)
Ex-1026	G.K. Celler & Sorin Crisoloveanu, <i>Frontiers of Silicon-on-Insulator</i> , 93 J. Applied Physics 4955 (2003)
Ex-1027	Timeline, Soitec, available at: https://www.soitec.com/en/company/soitec-activity/history (last visited Apr. 25, 2023)
Ex-1028	G. Shahidi et al., <i>Fabrication of CMOS on Ultrathin SOI Obtained by Epitaxial Lateral Overgrowth and Chemical-Mechanical Polishing</i> , IEEE (1991)
Ex-1029	MicroChemicals, Further Processing of Silicon Wafers: SiO_2 , Si_3N_4 , Metallization, Epitaxy and Dicing, available at: https://www.microchemicals.com/technical_information/silicon_wafer_sio2_si3n4_metallization_epitaxy_soi.pdf (last visited Apr. 28, 2023)
Ex-1030	Hiroshi Sakuraba et al., <i>New Three-Dimensional High-Density Stacked-Surrounding Gate Transistor (S-SGT) Flash Memory Architecture Using Self-Aligned Interconnection Fabrication Technology Without Photolithography Process for Tera-Bits and Beyond</i> , 43 Japanese J. Applied Physics 2217 (2004)
Ex-1031	Letter dated September 21, 2023 to counsel for Patent Owner from John Kappos

Petitioner submits this Preliminary Reply as authorized by the Board. Patent Owner (“PO”) requests the Board to deny institution of the Petition on the merits and, under *Fintiv*, based on the allegation that the “co-pending litigation in Texas will undoubtedly go to trial first.” Paper 6 (“POPR”) at 34. The PTAB should not exercise its discretion to deny institution under either theory.

I. THE BOARD SHOULD NOT DISCRETIONARILY DENY INSTITUTION OF THE PETITION BASED ON *FINTIV*

PO makes several misleading arguments in its *Fintiv* analysis. For example, PO contends that “[t]he median time to trial in the Eastern District of Texas predicts a June 2024 civil trial date—five months before the anticipated Final Written Decision deadline here.” POPR at 34. PO also argues that Petitioner misled the Board by “incorrectly asserting that ‘trial is expected November 2024’” and relying on “outdated statistics.” *Id.* PO is wrong on both counts. Petitioner relied on the most recent statistics available at the time of filing, and Petitioner’s estimate proved entirely accurate. Paper 1 (“Pet.”) at 74-75; Ex-2001 at 1. As Petitioner predicted, the district court trial is now set for November 18, 2024. Ex-2001 at 1; POPR at 12, 34. PO also fails to note that the scheduled trial date is only ten days before the statutory deadline for the Final Written Decision. *See* 35 U.S.C. § 314(b).

Although the PTAB takes the “courts’ trial schedules at face value absent some strong evidence to the contrary,” *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 15 at 13 (May 13, 2020) (informative), the PTAB should also consider

additional supporting factors such as the number of cases before the judge in the parallel litigation. *See In re Google LLC*, No. 2021-178, 2021 WL 5292267, at *3 (Fed. Cir. 2021). Here, the presiding judge in the district court case has scheduled ten trials to start on the same date—November 18, 2024.² Unless the other nine cases settle, some of the cases—and possibly this case—will move to later dates. Thus, the facts do not support PO's proposition that "co-pending litigation in Texas will undoubtedly go to trial" before the Final Written Decision. POPR at 34.

In addition, Petitioner has signed and served a stipulation not to pursue in the parallel district court proceeding any obviousness ground that includes the primary references in the Petition. Ex-1031. This stipulation mitigates concerns of potentially conflicting decisions and duplicative efforts between the district court and the PTAB. Thus, the PTAB should not exercise its discretion to deny institution.

II. THE PETITION DOES NOT COMBINE MULTIPLE EMBODIMENTS WITHIN A SINGLE REFERENCE

PO contends that the Petition fails to show that it would have been obvious to combine different embodiments within each of Watanabe and Lee and does not provide a motivation to do so. *See* POPR at 14-19, 29-31. As discussed below, PO's arguments are moot because no ground of the Petition combines disparate embodiments within Lee or Watanabe.

² A search on Bloomberg Law conducted on September 21, 2023 identifies ten trials before Judge Rodney Gilstrap beginning on November 18, 2024.

A. The Petition Relies on Watanabe's Nonvolatile Embodiment

Although PO argues that “Ground 1 cherry-picks among various different embodiments in Watanabe with no articulated or credible motivation to combine them,” POPR at 15, Ground 1 does not combine embodiments disclosing different memory types. As explained in the Petition, Watanabe discloses two “method[s] used to manufacture a semiconductor memory device.” Ex-1005, 5:68-6:19. Watanabe's semiconductor memory device has “memory cells arrayed three-dimensionally.” *Id.* 1:49-52. Watanabe further states, “[t]he memory cell...is applicable to any type of memory device i.e., a SRAM, a PROM, or a DRAM.”³ *Id.* 2:51-55. A POSITA would have understood this statement to mean that Watanabe's methods are applicable to any type of memory device, *i.e.*, volatile or nonvolatile memory. *Id.* 2:51-55; Ex-1002 ¶¶83-84, 86, 90. Despite depicting DRAM devices in several figures, Watanabe's description of the methods of manufacturing, and the representative figures, are explicitly “applicable to any type of memory device,” including nonvolatile memory such as PROM or EPROM. Ex-1005, 2:51-55.

In Grounds 1 and 2, the Petition does not combine embodiments disclosing different memory types. The Petition's reliance on figures in which “the memory cell is depicted as incorporated in a DRAM” would be understood in the context of

³ A POSITA would have understood that PROM memory devices are nonvolatile. Ex. 1002 ¶83.

Watanabe's explanation that the disclosed three-dimensional structures and manufacturing methods apply "to any type of memory device." *Id.* 2:51-55. Because Watanabe explicitly teaches the applicability of the described methods to any type of memory device, the Petition does not attempt to combine embodiments with different types of memory. POPR at 15-16. While PO relies on case law addressing a motivation to combine disparate embodiments from a specification that expressly differentiates between embodiments, those cases are inapposite. POPR at 14-19.

Watanabe's disclosure of methods of manufacturing semiconductor memory devices as applicable to different types of memory cells also parallels that of the '702 Patent. The '702 Patent describes manufacturing methods for memory devices applicable to "Dynamic Random Access Memory (DRAM) cells, Static Random Access Memory (SRAM) cells, non-volatile memory cells, and similar structures." Ex-1001, 1:14-16, 2:4-9. It is also telling that several of the '702 Patent's figures describe embodiments that "could work as a DRAM and a nonvolatile memory device." *Id.* 3:11-15, 3:18-24, 3:25-29; *see also* Figs. 23, 25, 27. The '702 Patent even explains the similarity between these structures: "Vertical nonvolatile memory has a form of either dual-gate with floating gate or single-gate with charge trapping gate insulator. Since the body of SOI pillar is usually floating, the nonvolatile [memory] could work as a DRAM device." *Id.* 10:29-32.

Properly understood, the Petition relies only on Watanabe's nonvolatile

embodiment for each of the claim limitations of Grounds 1 and 2. This proper reading negates PO's argument that Watanabe does not disclose limitation 13[b]. *See* POPR at 19-24. PO mistakenly argues that "[t]he Petition relies solely on DRAM memory for limitation 13[b]." *Id.* at 19. But all of Watanabe's disclosures and figures cited in the Petition for limitation 13[b] apply to "any type of memory device," including nonvolatile "PROM." Ex-1005 at 2:51-55. Furthermore, as discussed for limitation 13[d]—which is the limitation that specifies that the memory cells are "nonvolatile"—Watanabe discloses nonvolatile memory cells. Pet. at 25.

B. The Petition Relies on Lee's Pillar Structure Embodiment

Similarly, PO contends that the Petition provides no explanation for why or how Fig. 83A's flash memory array in a rail stack configuration would be combined with the pillar structure of Fig. 1A. POPR at 29-31. PO relies on *Whitewater* and *Amazon.com*. Both cases, however, require a motivation to combine because the embodiments are stated to be mutually exclusive. IPR2022-01035, Paper 8 at 16-17 (PTAB Nov. 17, 2022); IPR2022-01455, Paper 12 at 17 (Apr. 6, 2023). *Whitewater* and *Amazon* are therefore distinguishable because Petitioner here does not combine structures from mutually exclusive embodiments.

Rather, the Petition relies on the pillar structure of Fig. 1A and its associated embodiment throughout the Petition's analysis. The Petition references Fig. 83A's description only for claim limitation 13[c] to explain that a POSITA would have

understood that the memory arrays of Figs. 1A and 35 are bonded to the interlayer insulating layer formed over a substrate in the same manner as in Fig. 83A. Pet. at 52. Because the Petition references Fig. 83A only to show what a POSITA would have understood about the formation of Figs. 1A and 35, the Board does not need to find a motivation to combine embodiments. *See Realtime Data, LLC v. Iancu*, 912 F.3d 1368 (Fed. Cir. 2019) (motivation to combine unnecessary where second reference shows only POSITA's understanding about terminology in first reference).

Properly understood, the Petition relies only on Lee's pillar structure embodiment for each of the claim limitations of Grounds 3-6. This understanding negates PO's argument that Lee does not disclose dependent claim 15. *See* POPR at 32-33. PO contends that the Petition provides no explanation why a POSITA would have combined the embodiment of Fig. 7 having a charge trapping dielectric with that of Fig. 83A having a floating gate. POPR at 32-33. However, Petitioner does not combine the pillar structure of Fig. 1A and the rail stack configuration of Fig. 83A in its analysis of claim limitation 13[c] or dependent claim 15. Instead, as explained above, the Petition references Fig. 83A's description to demonstrate that a POSITA would have understood that the memory arrays of all of Lee's figures are "formed over" the interlayer insulating layer "formed over a substrate," meaning that the array is bonded to the dielectric in the same manner as in Fig. 83A. Ex-1002 ¶¶119-21. As to dependent claim 15, Lee explicitly acknowledges the alternative use

of a charge trapping layer, as shown in the pillar structure of Fig. 7, instead of a floating gate, as shown in the pillar structure of Fig. 1A. Pet. at 58-59 (citing Ex-1007, 15:37-40). Because the Petition does not combine embodiments in its analysis of claim limitation 13[c] or dependent claim 15, PO's argument is baseless.

III. WATANABE DISCLOSES A "PILLAR"

PO argues that Ground 2, covering dependent claims 14-17 only, should be rejected because the Petition does not explain how Watanabe discloses a "pillar." POPR at 24-28. PO misleadingly compares the "SOI pillar" of the '702 Patent's annotated Fig. 1 with a single layer of the pillar of Watanabe's Fig. 7. *Id.* at 24-25. PO seemingly finds fault with Watanabe's failure to use the word "pillar," while ignoring how the '702 Patent uses the term. *See* Ex-1001, 6:26-29 ("individual doped stack structures (i.e., pillar structures)"). As explained in the Petition, "Because Watanabe discloses a vertical structure with '[a]t least two stack structures (two layers) [(i.e., two planar members)] each consisting of layers 41 to 46,' Ex-1005, 3:12-13, a POSITA would have understood that Watanabe discloses a SOI pillar structure or renders it obvious.... *See id.*, Figs. 1, 2A (showing individual doped structures forming vertical pillars above insulator 49); Ex-1002 ¶91.'" Pet. at 30. Thus, Watanabe's description of individual doped stack structures matches the '702 Patent's description of a pillar structure and, alone or in view of Endoh, satisfies the "SOI pillar" limitation of dependent claims 14-17.

Respectfully submitted,

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CERTIFICATE OF SERVICE

The undersigned certifies pursuant to 37 C.F.R. §§ 42.6(e) and 42.105 that on September 21, 2023, a true and correct copy of this Preliminary Reply in connection to the Petition for *Inter Partes* Review was served in its entirety by filing this document through the PTAB P-TACTS System, as well as by email, on the counsel of record for the Patent Owner:

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