

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
MICRON SEMICONDUCTOR PRODUCTS, INC., and
MICRON TECHNOLOGY TEXAS, LLC,
Petitioner,

v.

BESANG INC.,
Patent Owner.

IPR2023-00900
Patent 7,378,702 B2

Before JON B. TORNQUIST, KIMBERLY McGRAW, and
ELIZABETH M. ROESEL, *Administrative Patent Judges*.

TORNQUIST, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. *Background and Summary*

Micron Technology, Inc., Micron Semiconductor Products, Inc. and Micron Technology Texas, LLC (“Petitioner”) filed a Petition (Paper 1, “Pet.”) requesting an *inter partes* review of claims 13–17 of U.S. Patent No. 7,378,702 B2 (Ex. 1001, “the ’702 patent”). BeSang Inc. (“Patent Owner”) filed a Preliminary Response to the Petition. Paper 6 (“Prelim. Resp.”). With authorization, Petitioner subsequently filed a reply to the Preliminary Response (Paper 7, “Prelim. Reply”) to which Patent Owner filed a sur-reply (Paper 8, “Prelim. Sur-reply”).

We have authority to determine whether to institute an *inter partes* review. 35 U.S.C. § 314 (2018); 37 C.F.R. § 42.4(a) (2023). The standard for institution is set forth in 35 U.S.C. § 314(a), which provides that an *inter partes* review may not be instituted “unless the Director determines . . . there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.”

For the reasons set forth below, Petitioner demonstrates a reasonable likelihood of prevailing with respect to claims 13–17 of the ’702 patent. Accordingly, we institute an *inter partes* review.

B. *Real Parties in Interest*

Petitioner identifies itself (the three parties identified in the caption) as the real party in interest. Pet. 1.

Patent Owner identifies itself as the real party in interest. Paper 3, 1.

C. *Related Matters*

The parties identify the following district court proceeding as a related matter: *BeSang Inc. v. Micron Tech., Inc.*, No. 2:23-cv-00028 (E.D. Tex. Jan 23, 2023) (“district court proceeding”). Pet. 1; Paper 3, 1. Patent Owner

also identifies *BeSang Inc. v. Intel Corp.*, No. 3:23-cv-00113 (D. Or.) as a related matter. Paper 3, 1.

D. The '702 Patent

The '702 patent is titled “Vertical Memory Device Structures,” and issued May 27, 2008, from an application filed September 3, 2004. Ex. 1001, codes (22), (45), (54).

The '702 patent explains that existing “integrated circuits contain transistors that are primarily implemented on a single major surface of a substrate, such as a semiconductor wafer.” *Id.* at 1:27–30. The '702 patent further explains that “[t]hese laterally oriented devices, consume significant amounts of chip area.” *Id.* at 1:30–31. One known method for reducing the lateral area consumed by the transistors was to reduce the lateral dimensions of the transistors and interconnects. *Id.* at 1:31–35. The '702 patent notes, however, that the equipment and technology needed to support the manufacture of such chips “becomes increasingly expensive with each new generation of smaller devices.” *Id.* at 35–39. To resolve this problem, the '702 patent discloses the use of “a plurality of vertically oriented semiconductor memory devices, or cells,” that may be added to a separately fabricated substrate that includes electrical devices and/or interconnect lines. *Id.* at 1:40–50.

Figure 1 of the '702 patent is reproduced below:

Fig. 1

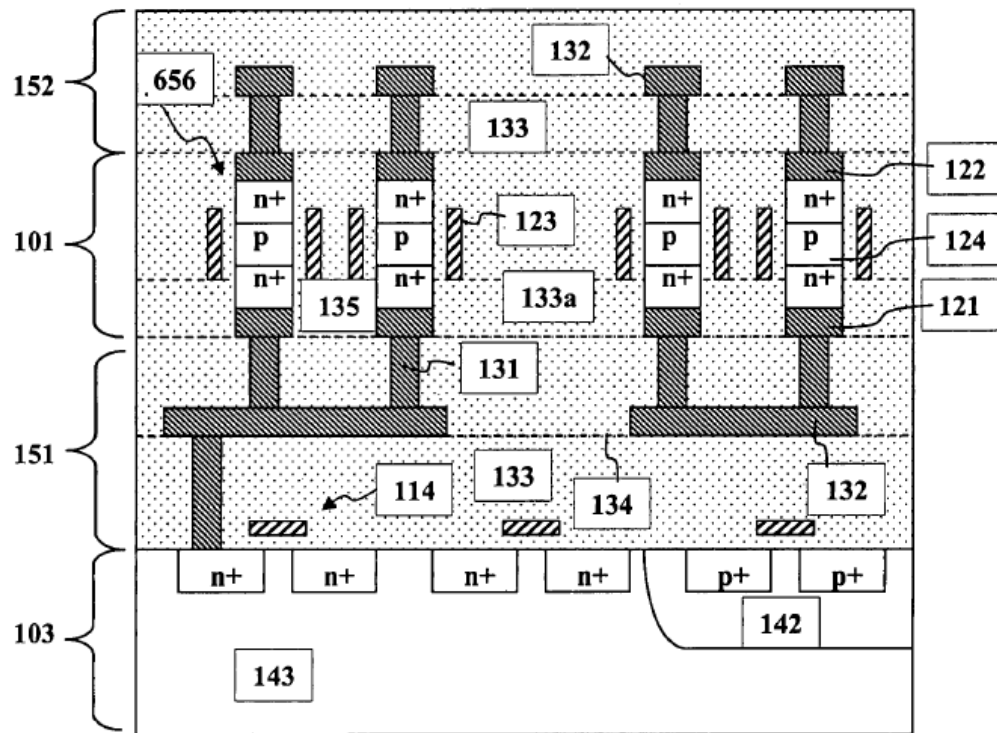


Figure 1 is a cross-sectional view of an embodiment that includes a base semiconductor substrate and add-on vertical memory devices. *Id.* at 2:13–15. As shown in Figure 1, vertical memory devices 656 are separated by isolation 135 and have floating structures in the filled dielectric materials 133a. *Id.* at 5:18–21. These vertical memory devices are referred to in the '702 patent as floating devices (FLD). *Id.* at 5:21–22. Inter-layer dielectric (ILD) layers 133 are disposed above and below each FLD layer. *Id.* at 5:29–32. Interconnect lines 132 and vias 131 connect FLDs directly or indirectly within an FLD layer, or connect devices from an FLD layer to another FLD layer or to a base substrate. *Id.* at 5:32–36.

In the embodiment shown in Figure 1, base substrate 103 is bonded to lower dielectric layer 151. *Id.* at 5:37–38. Dashed line 134 denotes a border, or interface, between two ILD layers. *Id.* at 5:43–44. The first ILD layer 151 has interconnections and vias, and base substrate 103 shares these interconnections and vias with first FLD layer 101. *Id.* at 5:44–47. The bottom of the FLD layer is connected to metal layer 121, which is also directly connected to vias 131 in ILD layer 151, thereby forming a preformed electrode and contact. *Id.* at 6:35–38. The top of the FLD layer may be connected to metal layer 122, which is also directly connected to vias 131 in ILD layer 152. *Id.* at 6:38–40. The ’702 patent notes that multiple FLD layers can be stacked, thereby increasing the effective device density. *Id.* at 6:41–42; *see also id.* at 5:38–41, 5:47–50 (disclosing a “second FLD layer” not shown in Figure 1).

E. Illustrative Claim

Petitioner challenges claims 13–17 of the ’702 patent. Pet. 3–4. Claim 13, reproduced below, is illustrative of the challenged claims:

13. A semiconductor memory structure, comprising:
 - [a] a substrate having electrical devices formed therein, and further having a dielectric layer disposed above the electrical devices;
 - [b] a stackable add-on layer having a plurality of vertically oriented semiconductor memory cells; and
 - [c] the stackable add-on layer being bonded to the dielectric layer; and
 - [d] wherein the memory cells are nonvolatile memory cells having at least one transistor.

Ex. 1001, 12:24–34 (paragraph identifications [a]–[d] are added to align with the parties’ arguments).

F. Prior Art and Asserted Grounds

Petitioner asserts that claims 13–17 of the ’702 patent would have been unpatentable on the following grounds (Pet. 3–4):

Claim(s) Challenged	35 U.S.C. §¹	Reference(s)/Basis
13	103	Watanabe ²
14–17	103	Watanabe, Endoh ³
13–15	103	Lee ⁴
16, 17	103	Lee, Endoh
13–15	103	Lee, Watanabe
16, 17	103	Lee, Watanabe, Endoh

In support of its grounds of unpatentability, Petitioner relies upon the declaration of Dr. Jack C. Lee. Ex. 1002.

II. ANALYSIS

A. Claim Construction

In this proceeding, the claims of the ’702 patent are construed “using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. [§] 282(b).” 37 C.F.R. § 42.100(b). Under that standard, the words of a claim are generally given their “ordinary and customary meaning,” which is the meaning the term would have had to a person of ordinary skill at the time of the invention, in the context of the

¹ The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. § 103, effective March 16, 2013. The ’702 patent issued May 27, 2008. Ex. 1001, code (45). Accordingly, on this record, we apply the pre-AIA version of § 103. *See* 35 U.S.C. § 100(i)(1)(B).

² US 5,091,762, issued February 25, 1992. Ex. 1005 (“Watanabe”).

³ US 2002/0154556 A1, filed March 28, 2002, and published October 24, 2002. Ex. 1006 (“Endoh”).

⁴ US 6,881,994 B2, filed August 13, 2001, and published April 19, 2005. Ex. 1007 (“Lee”).

entire patent including the specification. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc).

Both parties assert that no terms of the '702 require express construction for purposes of this decision. Pet. 12–13; Prelim. Resp. 13.

Upon review of the prior art and the parties' arguments, we determine that the term "a stackable add-on layer" requires discussion. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999) ("[O]nly those terms need be construed that are in controversy, and only to the extent necessary to resolve the controversy.")).

"stackable add-on layer"

Claim 13 requires "a stackable add-on layer" having a plurality of vertically oriented semiconductor memory cells that is "bonded to the dielectric layer." Ex. 1001, 12:29–32. Petitioner contends that Patent Owner's district court complaint appears to interpret this claim term to cover forming the "stackable add-on layer" by sequential deposition, but the intrinsic record of the '702 patent does not support such a construction. Pet. 6 n.2. According to Petitioner, "a stackable add-on layer having a plurality of vertically oriented semiconductor memory cells" and "the stackable add-on layer being bonded to the dielectric layer" require "vertically oriented semiconductor memory cells" to be formed in a separately fabricated "stackable add-on layer," which is then "bonded [to] the dielectric layer." *Id.* at 13 n.3.

On this preliminary record, we agree with Petitioner that the intrinsic record does not support a construction of "stackable add-on layer" that encompasses formation of memory cells by sequential deposition on a

substrate without being added to a separately formed substrate. First, the plain language of the claim does not require merely a “layer” having a plurality of vertically oriented semiconductor memory cells, but rather “a stackable add-on layer” having a plurality of vertically oriented semiconductor memory cells that is bonded to the dielectric layer. Ex. 1001, 12:29–32. The written description of the ’702 patent strongly suggests that such “a stackable add-on layer” is formed separately from the substrate and then stacked on and bonded to the substrate. *Id.* at 1:47–50 (“Briefly, a plurality of vertically oriented semiconductor memory devices, or cells, may be **added to a separately fabricated substrate** that includes electrical devices and/or interconnect lines.” (emphasis added)). It is unclear how memory cells sequentially deposited on a substrate could be considered to be a plurality of memory devices “added to a separately fabricated substrate.”

Generally supporting this understanding, the specification explains that a Silicon-on-Insulator (“SOI”) layer refers to “a relatively thin, single crystal portion of a semiconductor wafer that can be cleaved and bonded to another previously fabricated wafer, or similar type of substrate, such that a three dimensional stack is formed from the SOI layer and the previously fabricated wafer or similar type of substrate.” *Id.* at 4:47–53. According to the ’702 patent, “[i]n this context, the SOI layer may be thought of as an attachment layer, or stackable add-on structure which is suitable for bonding to a semiconductor substrate already containing devices and/or interconnections.” *Id.* at 4:53–57. Again, this suggests that a “stackable add-on layer” is a layer containing memory devices that is formed separately from the substrate and then bonded to the dielectric layer overlaying the substrate. We further note that we are directed to no embodiment of the

'702 patent wherein layers that are sequentially deposited on the substrate are identified as “stackable add-on layers.”

Based on the language of the claims and the disclosures found in the written description, we understand that a “stackable add-on layer” is a layer that is formed separately from the substrate and then bonded as whole to the dielectric layer positioned above the substrate. We do not understand a “stackable add-on layer” to include memory cells that are formed by sequential deposition on or above a substrate without being added to a separately formed substrate.⁵

B. Claim 13 over Watanabe

Petitioner contends the subject matter of claim 13 would have been obvious over Watanabe. Pet. 13–26.

1. Watanabe

Watanabe is titled “Semiconductor Memory Device With A 3-Dimensional Structure,” and issued February 25, 1992. Ex. 1005, codes (45), (54).

Watanabe explains that an object of its invention “is to provide a semiconductor memory device in which memory cells are arrayed three-dimensionally, thereby providing a high integration density.” *Id.* at 1:49–52. Figure 1 of Watanabe is reproduced below:

⁵ Neither party directs our attention to portions of the claims, specification, or prosecution history that would assist in construing the disputed claim term. The parties are encouraged to expressly construe this term during trial and to explain how a “stackable add-on layer” is structurally distinguishable from a layer that is sequentially deposited.

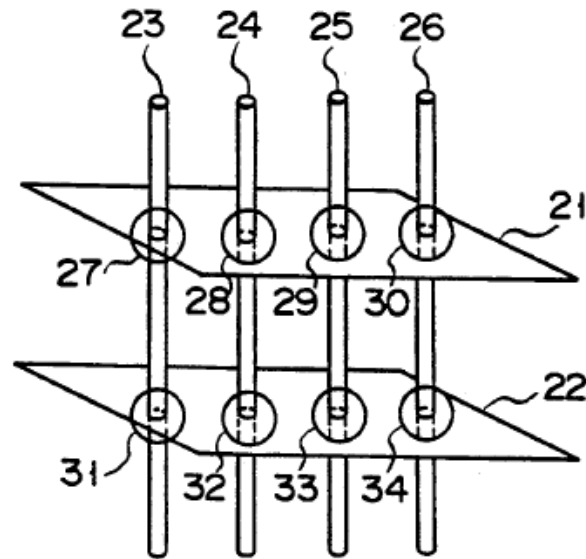


Figure 1 is a rough schematic illustration of a physical arrangement of a semiconductor memory device. *Id.* at 2:8–10. In Figure 1, the memory device is made up of two conductive planes 21 and 22 and four wires 23 to 26. *Id.* at 2:44–48. There are eight cross points where wires 23 to 26 pass through planar members 21 and 22. *Id.* at 2:50–51. Watanabe explains that “the conductive planar members 21 and 22 are used for inputting and outputting data (i.e., they serve as data planes), and wires 23 to 26 serve as word lines.” *Id.* at 2:58–61. Watanabe further explains that the memory cell depicted in Figure 1 “is applicable to any type of memory device, i.e., a SRAM, a PROM, or a DRAM,” but that the descriptions that follow in the patent are directed to a DRAM memory cell. *Id.* at 2:51–55.

Figure 2A is reproduced below:

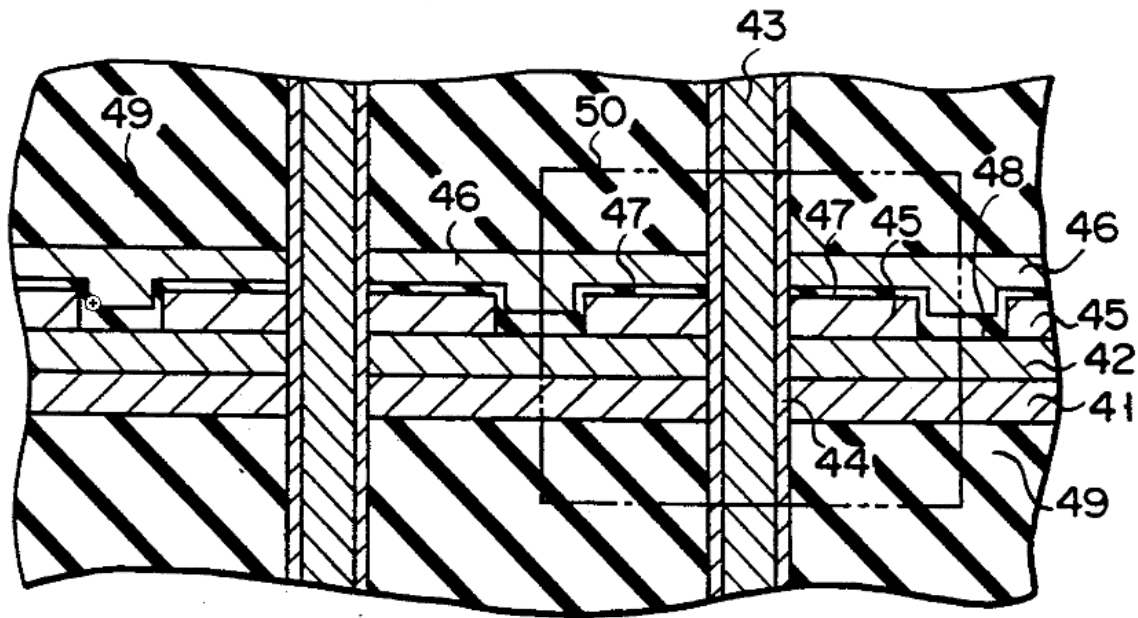


FIG. 2A

Figure 2A is a sectional view of a part of the semiconductor memory device shown in Figure 1, “and shows details of the structure of the memory device.” *Id.* at 2:11–13. In Figure 2A, conductive planar member 41 is in the form of an N+ type silicon layer and “serves as the source of the MOSFET.” *Id.* at 2:66–3:2. P-type Si layer 42 is above planar member 41. *Id.* at 3:2. N+ type Si layer 45 is above layer 42, with a portion surrounding each associated wire 43, and is overlaid by thin insulating film 47. *Id.* at 3:6–9. Thick insulating film 48 fills the spaces between each portion of layer 45 and is overlaid with conductive layer 46. *Id.* at 3:9–12. Wire 43 is oriented orthogonal to planar member 41 and is separated from layers 41, 42, 45, and 46 by insulating film 44. *Id.* at 3:2–5. Watanabe explains that in this embodiment “[a]t least two stack structures (two layers) each consisting

of layers 41 to 46 are provided, which are insulated from each other by insulating film 49, and through which wires 43 pass.” *Id.* at 3:12–15.

In operation, layer 41 serves as a data line for the input and output of data to and from the memory cell. *Id.* at 3:16–19. A potential is applied to layer 41 thereby placing wiring 43 in a high potential and inverting the conductivity of the portion of the p-type Si layer 42 that is in contact with the gate insulating film 44. *Id.* at 3:19–23. A charge is then transferred to the charge storage region 45 and stored in a capacitor located between region 45 and capacitor electrode 46. *Id.* at 3:23–27. “Then, if the potential of the wire 43 is decreased, the drain of the n+ Si layer 45 is electrically separated from the data plane 41.” *Id.* at 3:27–30.

Figure 7 is reproduced below:

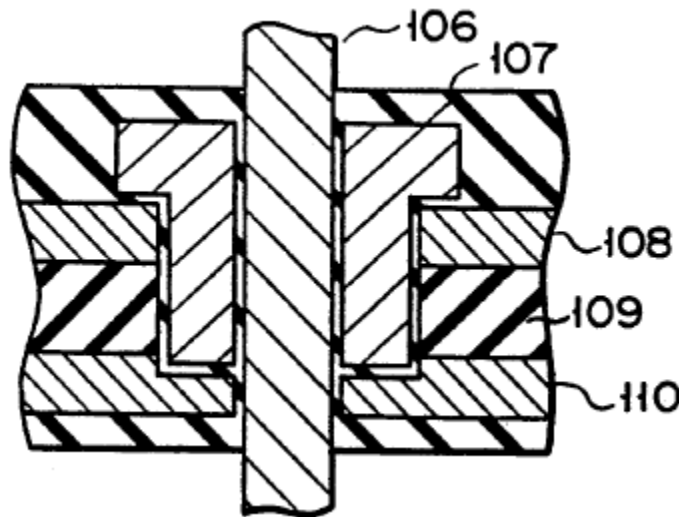


Figure 7 “is a sectional view showing a[n] application of the present invention into an EPROM.” *Id.* at 2:36–37. As shown in Figure 7, the disclosed EPROM includes control gate 106, floating gate 107, source 108, channel region 109, and drain region 110. *Id.* at 6:15–19.

Watanabe discloses two different methods of manufacturing its disclosed memory devices: a “laminating method” and a “stacking method.”

Id. at 5:1–7, 5:45–55. In the “laminating method,” “a plurality of planar members are formed and are laminated, and holes are formed in the laminated planar members, through which the wiring passes.” *Id.* at 5:1–7, Figs. 5A to 5E. In this method, a first planar member is completed in a sequence of process steps, and then a second planar member is formed over the first planar member in a sequence of process steps similar to that used to form the first planar member. *Id.* at 5:8–32. After “a desired number of planar members are first formed into a stack of planar members, . . . contact holes are formed and wires buried therein.” *Id.* at 5:31–44.

In the “stacking method,”

a first planar member is formed, and then wires are buried in the contact holes, respectively. A second planar member is formed, and the formed planar member is holed for contact hole, and wires are buried into the holes. The process is repeated by the number of times equal to a necessary number of planar members. Finally, the planar member thus formed are stacked and wired.

Id. at 5:45–55, Figs. 6A to 6D. According to Watanabe, “[i]n the stacking method, a number of process steps is increased, but a wiring accuracy is improved because the wiring is made [in] every planar member.” *Id.* at 6:11–14.

2. *Analysis: Claim 13*

Petitioner contends the subject matter of claim 13 would have been obvious in view of the disclosures of Watanabe. Pet. 13–26.

With respect to limitation 13[a], Petitioner contends that in each of the “laminating” and “stacking” embodiments of Watanabe, a Si substrate is used that has transistors formed in the upper surface thereof and a dielectric layer (“insulating film”) is formed on this Si substrate above the electrical devices. *Id.* at 14–16 (citing Ex. 1005, 5:1–6:14).

With respect to limitation 13[b], Petitioner contends that planar members 21 and 22 in Watanabe’s Figure 1 correspond to a “stackable add-on layer.” Pet. 16–17. Petitioner contends that Figure 2A of Watanabe discloses the formation of semiconductor memory cells in which the transistors’ source-channel-drain-elements (e.g., elements 41, 42, and 45) are arranged vertically. *Id.* at 18 (citing Ex. 1001, 4:7–9; Ex. 1002 ¶ 74; Ex. 1005, Fig. 2A).

Addressing limitations 13[b] and 13[c], Petitioner contends that Watanabe’s “stacking method” and “laminating method” teach or suggest a stackable add-on layer that is bonded to the dielectric layer under either Petitioner’s (“stacking”) or Patent Owner’s (“laminating”) (apparent) constructions of “stackable add-on layer.” *Id.* at 18–24 (citing Ex. 1005, 5:1–6:14, Figs. 5A–5E, 6A–6D; Ex. 1002 ¶¶ 76–82).

Finally, with respect to limitation 13[d], Petitioner contends that the EPROM memory device of Figure 7 is a vertically-oriented, “nonvolatile memory” cell having at least one transistor. *Id.* at 25.

Patent Owner contends that Petitioner’s challenge relies on different embodiments in Watanabe—Figures 1 and 2A (the DRAM embodiment) for claim element 13[b] and Figure 7 (the EPROM embodiment) for claim element 13[d]—without showing a motivation to combine these embodiments. Prelim. Resp. 14–19. Patent Owner further contends that, even if the embodiments are combined, Petitioner does not show that Watanabe’s DRAM embodiment satisfies the “memory cells” limitation of claim element 13[b]. *Id.* at 19–24. According to Patent Owner, the stackable add-on layer with a plurality of vertically oriented memory cells of claim 13[b] must, in view of claim 13[d], be a “nonvolatile memory cell.” *Id.* at 19. Patent Owner further contends that Petitioner does not assert that

the DRAM memory relied upon for limitation 13[b] is a “nonvolatile memory, nor could it.” *Id.* Patent Owner also contends that there is no explanation of how the EPROM memory cells of Figure 7 would teach or suggest the limitations of claim 13[b]. *Id.* at 22–23.

Petitioner argues in response that the Petition does not attempt to combine embodiments, and relies only on Watanabe’s nonvolatile embodiment for each of the limitations of claim 13. Prelim. Reply 4–5. Petitioner concedes that it cites to Figures 2A, 5, and 6, which are related to DRAM memory, but contends that Watanabe makes clear that these figures apply to “any type of memory device,” including nonvolatile PROM memory. *Id.* at 5–6 (citing Ex. 1005, 2:51–55).

Patent Owner argues in response that the PROM embodiment of Figure 7 and the DRAM embodiments of Figures 1 and 2A “are plainly alternative embodiments.” Prelim. Sur-reply 4.

Patent Owner’s arguments have merit. The vast majority of Petitioner’s arguments focus on explaining why the DRAM embodiments of Watanabe’s Figures 2A, 5, and 6 disclose the limitations of claims 13[a]–[c], and then Petitioner abruptly switches to the EPROM embodiment of Figure 7 to show where the limitations of claim 13[d] are disclosed. As noted by Petitioner, Watanabe indicates after its discussion of the rough schematic of Figure 1 that the memory cell of the invention “is applicable to any type of memory device, i.e., a SRAM, a PROM, or a DRAM.” Prelim. Reply 3 (quoting Ex. 1005, 2:51–55). We do not understand this statement to mean that every structure depicted in Figures 2A, 5, and 6 is applicable to “any type of memory device.” And, although it is evident that Watanabe contemplates using the EPROM structures depicted in Figure 7 in its invention, it is not clear what the resulting structure would look like,

including whether such a three-dimensional memory would use the same structure as the DRAM memory depicted in Figures 2A, 5A, and 6.

In view of the foregoing, we have concerns about the sufficiency of Petitioner's challenge based on Watanabe. The parties may further address this ground at trial.

C. Claims 14–17 over Watanabe and Endoh

Claims 14–16 each depend from independent claim 13, and claim 17 depends from claim 16. Ex. 1001, 12:35–52. Each of these claims requires one or more SOI pillars. *Id.*

Petitioner contends that “Watanabe discloses a SOI pillar structure or renders it obvious with the knowledge of one of ordinary skill in the art.” Pet. 30. Petitioner cites Watanabe Figures 1 and 2A as “showing individual doped structures forming vertical pillars above insulator 49.” And, to the extent Watanabe alone does not disclose the vertically oriented semiconductor nonvolatile memory cell on a SOI pillar structure, Petitioner contends that Watanabe in view of Endoh renders this limitation obvious. *Id.* at 31.

Beyond its arguments with respect to independent claim 13, Patent Owner contends Petitioner fails to demonstrate that Watanabe and Endoh teach or suggest an SOI pillar. Prelim. Resp. 24–28. First, Patent Owner contends that the horizontal layers of Watanabe relied upon in the Petition do not disclose a “pillar” structure. *Id.* at 25. Second, Patent Owner contends Endoh does not remedy this deficiency because in the proposed combination of Watanabe and Endoh, Petitioner only argues that there would have been a reasonable expectation of success in forming Watanabe's pillar on a SOI wafer, as disclosed in Endoh. *Id.* at 27.

Claims 14–17 depend from claim 13, and Petitioner’s arguments and evidence with respect to these claims do not remedy the deficiencies noted above with respect to claim 13. Moreover, on this record, Petitioner does not adequately demonstrate that Watanabe teaches or suggests a “pillar,” as that term is used in the ’702 patent.⁶ Petitioner and Dr. Lee appear to assume that any vertically stacked structure with at least two layers would be understood to disclose or render obvious a “pillar.” Pet. 30; Prelim. Reply 7; Ex. 1002 ¶ 91. We are directed to no explanation, however, why this is so. Indeed, both the ’702 patent and Lee refer to pillars where the height of the structure is substantially larger than its width, which stands in contrast to the doped, horizontal layers above insulator 49 Petitioner identifies in Watanabe Figure 2A. Ex. 1001, Figs. 1, 4, 8:5–11; Ex. 1005, Fig. 2A; Ex. 1007, 8:18–19. Watanabe’s layer 41, for example, is described as a “planar member” and extends across the entirety of insulator 49. Ex. 1005, 2:66–3:2; Figs. 2A, 2B.

The parties may further address this ground at trial, and to the extent they do, they are encouraged to provide an express definition of “SOI pillar,” including an explanation as to whether stacks of broad horizontal structures would be understood in the art to comprise a “pillar,” as that term is used in the ’702 patent.

D. Claims 13–15 over Lee

Petitioner contends the subject matter of claims 13–15 would have been obvious over the disclosures of Lee. Pet. 46–59.

⁶ In this ground, we understand Petitioner’s argument to be that one of ordinary skill in the art would have formed Watanabe’s pillar structure on a SOI wafer. Pet. 33.

1. *Lee*

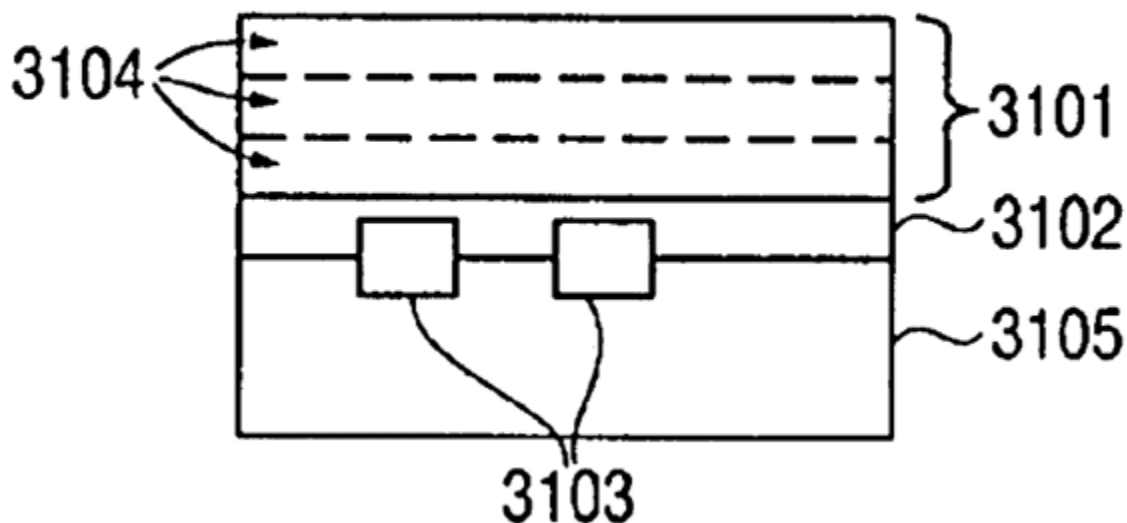
Lee is titled “Monolithic Three Dimensional Array of Charge Storage Devices Containing a Planarized Surface” and issued April 19, 2005.

Ex. 1007, codes (45), (54).

Lee notes that the cost of memory and logic devices is decreased by increasing device density and that one method of increasing device density “is to arrange the devices in a monolithic three dimensional array of charge storage devices comprising a plurality of device levels.” *Id.* at 11:18–27. In this context “monolithic” means that the layers of each level of the array are directly deposited on the layers of each underlying level of the array. *Id.* at 11:27–30. This is in contrast to two-dimensional arrays, which “may be formed separately and then packaged together to form a non-monolithic memory device.” *Id.* at 11:30–32.

Figure 35 is reproduced below:

FIG. 35



is formed on body 104. *Id.* at 14:16–19. A second I/O region 116 is formed on second contact region 106. *Id.* at 14:19–20. Lee explains that first contact region 102, body 104, and the second contact region 106 are each vertically aligned to form a pillar 108. *Id.* at 14:20–23. “Adjacent to and in contact with body 104 is a charge storage medium 110,” with control gate 112 formed adjacent to and in direct contact with charge storage medium 110. *Id.* at 14:23–26.

Lee explains that:

The programmed and unprogrammed state of the pillar memory device is determined by whether or not charge is stored in charge storage medium 110. The charge stored in the charge storage medium adds or subtracts from the voltage applied to the control gate, thereby altering the voltage required to form a conducting channel in body 104 to enable a current (e.g., read current I_R) to flow between the first and second contact (source/drain) regions.

Id. at 14:32–39.

Figure 2 is reproduced below:

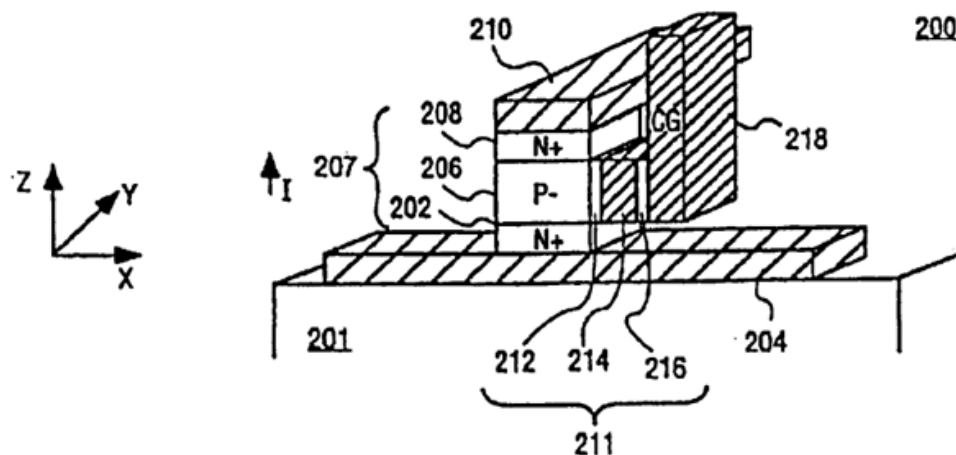


FIG. 2

Figure 2 is an illustration of a pillar memory. *Id.* at 8:27–28. In this embodiment, pillar 207 includes a first source/drain contact region 202 comprising a heavily doped N+ silicon film that is formed on a first input/output 204 (e.g. bit line) that is formed on or above a substrate 201. *Id.* at 15:16–22. Body 206 is composed of a lightly doped P- type silicon film 206 that is formed on and in direct contact with N+ source/drain contact region 202. *Id.* at 15:22–25. Second drain region 208 is composed of a heavily doped N+ silicon film and is formed on and in direct contact with P type silicon film 206. *Id.* at 15:25–30. “A second conductive input/output (e.g. word line/bit line) 210 is formed on the second N+ source/drain region 208.” *Id.* at 15:30–31. Charge storage medium 211 comprises a tunnel dielectric 212, floating gate 214, and control gate dielectric 216. *Id.* at 15:41–43. Control gate 218 is formed adjacent to, and in direct contact with, control gate dielectric 216. 15:50–52. “Control gate 218 is formed of a conductor such as but not limited to doped silicon or a metal such as tungsten.” *Id.* at 15:52–54.

2. Analysis – Claim 13

Petitioner contends that Lee discloses every limitation of independent claim 13. Pet. 46–54. With respect to claim 13[a], Petitioner contends that Figure 35 of Lee depicts driver circuits 3103 formed in monocrystalline substrate 3105, and a dielectric layer (interlayer insulating layer 3102) disposed on substrate 3105 and above the electrical devices. Pet. 47 (citing Ex. 1007, 12:17–27, Fig. 35; Ex. 1002 ¶ 116). With respect to claim 13[b], Petitioner contends that Figure 1A depicts TFTs and diodes arranged in a pillar configuration, i.e., vertically oriented with respect to the substrate, and Figure 35 shows an “[a]rray of charge storage logic or memory devices 3101 (i.e. stackable add-on layers) with a plurality of device levels 3104.” *Id.*

at 48–49 (citing Ex. 1007, 5:46–56, Figs. 1A, 35). Petitioner asserts, “[b]ecause Lee discloses ‘a three dimensional nonvolatile memory array, comprising a plurality of vertically separated device levels,’ in which ‘each level comprise[es] an array of TFT EEPROMs,’ the memory array is a stackable add-on layer having a plurality of vertically oriented semiconductor memory cells,” as apparently construed by Patent Owner. *Id.* at 50 (citing Ex. 1007, 5:46–56, Figs. 1A, 35); *see id.* at 48 n.5 (“Lee discloses the subject matter [of claim 13[b]] of the ’702 Patent under the interpretation [Patent Owner] appears to adopt.”). With respect to claim 13[c], Petitioner contends that memory devices 3101 are formed above interlayer insulating layer 3102 and one of ordinary skill in the art would have understood that the memory array of Figure 35 is bonded to interlayer insulating layer 3102. *Id.* at 50–52 (citing Ex. 1007, 12:17–25; Ex. 1002 ¶ 119). As support for its argument that Lee discloses a stackable add-on layer bonded to an insulating layer, Petitioner points to Lee’s description of a monolithic array, Lee’s disclosures relating to Figure 35, and Lee’s disclosures relating to Figure 83A. *Id.* at 51–52 (citing Ex. 1007, 11:24–31, 55:32–36, Figs. 35, 83A). With respect to claims 13[d], Petitioner contends that the memory device of Figure 1A is non-volatile and has at least one transistor. *Id.* at 53–54 (citing Ex. 1007, 14:10–23; Ex. 1002 ¶ 122).

Claim 13[c] requires a stackable add-on layer having a plurality of vertically oriented semiconductor memory cells. Lee is directed to a monolithic three-dimensional array of charge storage devices in which the “layers of each level of the array were directly deposited on the layers of each underlying level of the array.” Ex. 1007, 11:25–30, 12:17–23 (noting that the embodiment disclosed in Figure 35 is a monolithic array), 14:10–19 (noting that the individual layers of pillar memory device 100 are “formed

directly on” the proceeding layer). As discussed above and argued by Petitioner, we do not understand a “stackable add-on layer” to include layers of semiconductor memory cells that are formed through sequential deposition on a substrate without being added to a separately formed substrate. As such, Petitioner has not demonstrated a reasonable likelihood that claim 13 would have been obvious over Lee under the claim construction of “stackable add-on layer” advocated by Petitioner and preliminarily adopted above.

3. *Claims 14–17*

Claims 14–17 each depend, directly or indirectly, from claim 13. Petitioner’s arguments with respect to these claims do not resolve the deficiencies noted above with respect to claim 13. As such, Petitioner does not demonstrate a reasonable likelihood of prevailing with respect to these claims.

E. *Claims 13–15 over Lee and Watanabe*

1. *Analysis – Claim 13*

Petitioner asserts that, “[t]o the extent Claim 13 is construed to exclude forming a ‘stackable add-on layer’ through sequential deposition directly on a substrate,” the subject matter of claim 13 is disclosed by Lee in view of Watanabe. Pet. 69.

Petitioner contends that Lee discloses the subject matter of the preamble and claims 13[a] and 13[d]. *Id.* at 71 (relying on same contentions as presented for Lee alone). With respect to claims 13[b] and 13[c], Petitioner contends that Lee and Watanabe both disclose vertically oriented, non-volatile memory cells that are bonded to a dielectric layer that is deposited over the substrate. *Id.* at 71–72. Petitioner further contends that Watanabe and Lee both disclose forming the memory devices by layer-by-

layer sequential deposition and Watanabe also discloses an alternative “stacking method” in which stackable memory layers are formed individually and then bonded to a separately-fabricated substrate. *Id.* at 70, 72.

Petitioner contends one of ordinary skill in the art would have combined Watanabe and Lee because Watanabe discloses an alternate method of forming a memory device that is applicable to the memory devices of Lee and Watanabe, and Watanabe discloses that its “stacking method” improves the accuracy of the wiring and provides “a semiconductor memory device with improved integration density” and “low interconnection wire resistance.” *Id.* at 72.

Patent Owner does not address Petitioner’s reasons to combine Watanabe and Lee but asserts that Petitioner’s grounds based on Lee are “defective” because Petitioner relies on multiple embodiments of Lee without providing a reason to combine these embodiments. Prelim. Resp. 28–29. In particular, Patent Owner contends Petitioner’s combination relies on the embodiments depicted in Figures 1A, 35, and 83A, but the embodiment of Figure 1A is a “pillar memory device,” whereas the flash memory depicted in Figure 83A is a “rail stack” device, which is a different, alternative embodiment. *Id.* at 29–30 (citing Ex. 1007, 14:11–13, 55:8–12, 55:26–28). Patent Owner contends the Petition “includes no showing why one of skill in the art would have been motivated to combine Lee’s assorted embodiments across Lee’s 128 pages and had a reasonable expectation of success” and contains no explanation as to why or how Lee’s Figure 1A and Figure 83A embodiments would be combined. *Id.* at 30.

After considering Patent Owner’s arguments, we are persuaded that Petitioner’s contentions are sufficient for purposes of institution. Lee’s

Figure 35A is a high-level schematic that generally illustrates how the charge storage devices of the invention may be constructed, i.e., using multiple device layers deposited above a monocrystalline substrate and separated by insulating layers. Ex. 1007, 12:16–32. Figure 1A depicts an individual memory device that would be constructed in the manner shown in Figure 35. *Id.* at 12:50–60. As such, we do not understand Petitioner to be selecting or combining disparate or separate embodiments to arrive at the claimed invention.

As noted by Patent Owner, Petitioner does cite to Figure 83A and its “rail stack” device to support its argument that Lee discloses a stackable add-on layer bonded to a dielectric layer. Prelim. Resp. 29–30; Pet. 50–52. In this ground, however, we understand Petitioner to rely on Figure 83A to show what one of ordinary skill in the art would have understood about how the layers of Lee’s memory devices are formed/bonded. Pet. 50, 52. As such, on this record, Petitioner’s contentions based on Lee’s Figures 1A, 35, and 83A are sufficient for purposes of institution.

Upon review of the parties’ arguments and evidence, we determine that Petitioner identifies where Lee and Watanabe disclose every limitation of claim 13. Petitioner also explains why one of ordinary skill in the art would have sought to combine these disclosures to arrive at the claimed invention with a reasonable expectation of success. Accordingly, Petitioner demonstrates a reasonable likelihood that claim 13 would have been obvious over Lee and Watanabe.

2. *Analysis: Claim 14*

Claim 14 depends from claim 13 and further requires that the claimed memory cell “comprises a vertical transistor having a floating gate and a control gate on a SOI pillar.” Ex. 1001, 12:35–38.

Petitioner contends that Figures 1 and 2 of Lee disclose the memory cell of claim 14. Pet. 54–58.

Patent Owner does not address Petitioner’s arguments with respect to claim 14, apart from its arguments directed to independent claim 13.

Upon review of the parties’ arguments and evidence, we determine that Petitioner demonstrates a reasonable likelihood that claim 14 would have been obvious over Lee and Watanabe

3. *Analysis: Claim 15*

Claim 15 depends from claim 13 and further requires “wherein the vertically oriented semiconductor nonvolatile memory cell comprises a vertical transistor having a charge-trapping gate insulator and a gate on a SOI pillar.” Ex. 1001, 12:39–42.

Petitioner contends Figure 7 of Lee depicts a pillar memory embodiment having a charge-trapping dielectric and that this embodiment is an alternative to the memory device of Figures 1 and 2 of Lee. Pet. 58.

Patent Owner contends this ground is not persuasive because Petitioner is attempting to combine the embodiments disclosed in Lee’s Figures 7 and 83A without providing a reason to combine these embodiments. Prelim. Resp. 32–33. In particular, Patent Owner contends that Petitioner looks to Lee’s Figure 83A to support its argument that claim 13[c] is disclosed in Lee, yet for claim 15 relies on Lee’s Figure 7. *Id.* at 32.

As noted above, Petitioner contends that one of ordinary skill in the art would have understood that each add-on layer in Figures 7 and 35 is bonded to the dielectric layer based on Lee’s description of a monolithic array, the disclosures of Figure 35, and the disclosures of Figure 83A.

In view of the foregoing, we determine that Petitioner demonstrates a reasonable likelihood that claim 15 would have been obvious over Lee and Watanabe.

F. Claims 16 and 17 over Lee, Watanabe, and Endoh

Petitioner contends that dependent claims 16 and 17 would have been obvious over Lee, Watanabe, and Endoh. Pet. 73–74.

Patent Owner does not address these additional grounds based on Lee, apart from its arguments regarding combining multiple embodiments of Lee to arrive at the subject matter of claim 13. Prelim. Resp. 28–33.

Upon review of the parties’ arguments and evidence, we determine that Petitioner demonstrates a reasonable likelihood that claims 16 and 17 would have been obvious over Lee, Watanabe, and Endoh.

III. DISCRETIONARY DENIAL

Patent Owner contends we should exercise our discretion and not institute trial under 35 U.S.C. § 314(a). Prelim. Resp. 33. We address this argument below.

A. Discretionary Denial under 35 U.S.C. § 314(a)

Under 35 U.S.C. § 314(a) we have discretion to deny institution of an *inter partes* review. *Cuozzo Speed Techs., LLC v. Lee*, 579 U.S. 261, 273 (2016). We consider several factors when determining whether to deny institution under § 314(a) based on a parallel district court proceeding, specifically

1. whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted;
2. proximity of the court’s trial date to the Board’s projected statutory deadline for a final written decision;
3. investment in the parallel proceeding by the court and the parties;

4. overlap between issues raised in the petition and in the parallel proceeding;
5. whether the petitioner and the defendant in the parallel proceeding are the same party; and
6. other circumstances that impact the Board's exercise of discretion, including the merits.

Apple Inc. v. Fintiv, Inc., IPR2020-00019, Paper 11 at 5–6 (PTAB Mar. 20, 2020) (precedential) (“Fintiv”). We also consider “several clarifications” made by the Director of the United States Patent and Trademark Office (“USPTO”). See USPTO Memorandum, Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation, 2 (June 21, 2022), available at https://www.uspto.gov/sites/default/files/documents/interim_proc_discretionary_denials_aia_parallel_district_court_litigation_memo_20220621_.pdf (“Director’s Memo”).

1. Factor 1 – Whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted

Under the first *Fintiv* factor, we consider “whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted.” *Fintiv*, Paper 11 at 6. Petitioner argues that the first factor is neutral because Petitioner has not yet moved to stay the district court proceeding, “and the PTAB will not infer how the district court would rule should a stay be requested.” Pet. 74.

Patent Owner agrees that factor 1 is neutral. Prelim. Resp. 33.

Given that no stay is in place and there is no current indication in the record that the district court intends to grant a stay, we determine that the first *Fintiv* factor is neutral.

2. *Factor 2 – The proximity of the court’s trial date to the Board’s projected statutory deadline for a final written decision*

Under the second *Fintiv* factor, we consider the “proximity of the court’s trial date to the Board’s projected statutory deadline for a final written decision.” *Fintiv*, Paper 11 at 6. Petitioner contends that the district court has not set a trial date, but trial is estimated to begin around November 2024. Pet. 74–75. Thus, Petitioner contends this factor “is neutral or, at most, slightly in favor of denial.” *Id.* at 75.

Patent Owner contends the co-pending litigation “will undoubtedly go to trial first,” as the median time to trial in the Eastern District of Texas predicts a June 2024 civil trial date, i.e., five months before the deadline for issuing the Final Written Decision in this case. Prelim. Resp. 34. Patent Owner further contends that even if the currently scheduled November 18, 2024, trial date applied, this date is still before the statutory deadline in this case. *Id.*

Petitioner argues in reply that, although a November trial date has now been set by the district court, the presiding judge in that case has scheduled ten trials to start on the same date, and it is possible that the trial date will move to a later date. Prelim. Reply 2.

Patent Owner contends that Petitioner does not dispute that the current trial statistics predict a June 2024 jury trial or that trial is now set for November 18, 2024, “both of which would beat the anticipated Final Written Decision deadline here.” Prelim. Sur-reply 1. Patent Owner further contends that Petitioner’s speculation about the trial date in the district court case being pushed back due to the court’s current docket should be rejected

because “the PTAB takes the ‘courts’ trial schedules at face value absent some strong evidence to the contrary.” *Id.* at 2.

The trial date in the district court litigation is currently November 18, 2024. Ex. 2001, 1. Because the expected trial date is “at or around the same time” as the projected statutory deadline for a final written decision, *Fintiv* factor 2 is neutral. *Fintiv*, Paper 11 at 9 (noting that “[i]f the court’s trial date is at or around the same time as the projected statutory deadline, the decision whether to institute will likely implicate other” *Fintiv* favors, such as the resources that have been invested in the parallel proceeding).

3. *Factor 3 – Investment in the parallel proceeding by the court and the parties*

Under the third *Fintiv* factor, we consider the “investment in the parallel proceeding by the court and the parties.” *Fintiv*, Paper 11 at 6. Petitioner contends that, at the time of the filing of the Petition, the court had not yet held a case management conference or set a Markman or trial date, and that no hearings or substantive activities or hearings have occurred in the case. Pet. 75. “Because the investment in the trial has been minimal and Petitioner acted diligently” in filing the Petition, Petitioner contends “this factor weighs strongly against discretionary denial.” *Id.*

Patent Owner contends the co-pending district court case has been moving forward, with infringement and invalidity contentions being exchanged and discovery and deposition underway. Prelim. Resp. 34. Patent Owner further contends that by the institution deadline of November 28, 2023, the parties will be in the “home stretch of discovery.” *Id.* at 34–35. “Based on the considerable resources already expended on contentions and discovery in the district court,” Patent Owner argues that *Fintiv* factor 3 weighs in favor of denying institution. *Id.* at 35.

Although some activity has occurred in the district court case, we are directed to no substantive rulings by the district court to suggest that it has invested considerable resources in the case. Nor are we presented with evidence that the parties have expended significant resources in the district court litigation. Fact discovery is not scheduled to be completed until July 1, 2024, and expert discovery is to be completed by August 5, 2024, i.e., more than seven months after the institution deadline. Ex. 2001, 3. Accordingly, we determine that *Fintiv* factor 3 weighs against discretionary denial of institution.

4. *Factor 4 – Overlap between issues raised in the petition and in the parallel proceeding*

Under the fourth *Fintiv* factor, we consider the “overlap between issues raised in the petition and in the parallel proceeding.” *Fintiv*, Paper 11 at 6. Petitioner contends that in the district court litigation Patent Owner asserts infringement under only claim 13, whereas the Petition challenges claims 13–17. Pet. 76. Petitioner argues that because it is challenging more claims than are asserted in the district court litigation, this proceeding “is the only venue in which the invalidity challenges against several claims in the ’702 Patent will be adjudicated,” and this proceeding will promote efficiency because it “will resolve disputes against future district court defendants.” *Id.*

Patent Owner responds that Petitioner’s “invalidity contentions challenge the same Claims 13–16 based on the identical Watanabe, Lee, and Endoh references relied upon in the Petition.” Prelim. Resp. 35.

Petitioner responds that it has signed and served a stipulation “not to pursue in the parallel district court proceeding any obviousness ground that includes the primary references in the Petition.” Prelim. Reply 2.

According to Petitioner, “[t]his stipulation mitigates concerns of potentially

conflicting decisions and duplicative efforts between the district court and the PTAB.” *Id.*

Patent Owner argues in response that Petitioner’s “meager agreement not to assert obviousness based on two specific references falls far short of the Director’s Guidance requiring a broad *Sotera* stipulation renouncing ‘the same grounds or *any grounds that could have reasonably been raised* before the PTAB.’” *Id.* (quoting Director’s Memo at 3).

Although not dispositive given its narrower scope compared to a *Sotera*-type stipulation, Petitioner’s stipulation does serve to mitigate concerns of duplicative efforts between the PTAB and the district court. Director’s Memo at 7. Thus, we determine that the fourth *Fintiv* factor weighs against discretionary denial of institution.

5. *Factor 5 – Whether the petitioner and the defendant in the parallel proceeding are the same party*

Under the fifth *Fintiv* factor, we consider “whether the petitioner and the defendant in the parallel proceeding are the same party.” *Fintiv*, Paper 11 at 6. Petitioner concedes that Petitioner is the defendant in the parallel district court proceeding, but contends this factor should be given little weight because it “does not outweigh the other factors that strongly weigh against discretionary denial.” Pet. 76.

Patent Owner contends this factor supports denial of institution. Prelim. Resp. 36.

Because Petitioner is a defendant in the district litigation and the trial in that case is currently set to occur at or around the same time as the issuance of a final written decision, this fifth *Fintiv* factor is neutral. *See, e.g., Samsung Electronics Co., Ltd. v. MyPAQ Holdings Ltd.*, IPR2022-00307, Paper 10 at 13 (PTAB May 23, 2022).

6. *Factor 6 – Other circumstances that impact the Board’s exercise of discretion, including the merits*

Under the sixth *Fintiv* factor, we consider “other circumstances that impact the Board’s exercise of discretion, including the merits.” *Fintiv*, Paper 11 at 6. Petitioner contends this factor weighs against discretionary denial as the “merits are strong.” Pet. 77.

Patent Owner contends Petitioner’s “patentability challenge is deeply flawed because the Petition is riddled with hindsight and fails to show obviousness for any ground.” Prelim. Resp. 36. According to Patent Owner, “[t]he weakness of the Petition’s merits heavily favors discretionary denial.” *Id.*

On balance, we determine that *Fintiv* factors 1–5 do not favor discretionary denial of institution. In particular, we determine that Petitioner’s stipulation not to pursue any obviousness ground in the district court that includes Watanabe or Lee and the minimal investment by the parties and the district court in the parallel litigation weigh against discretionary denial, whereas the other factors are neutral. Accordingly, we do not address whether Petitioner presents a compelling unpatentability challenge. *See CommScope Techs. LLC v. Dali Wireless, Inc.*, IPR2022-01242, Paper 23 at 4–5 (PTAB Feb. 27, 2023) (decision on Director review) (precedential) (noting that the Board should reach the compelling merits issue only when *Fintiv* factors 1–5 favor discretionary denial).

7. *Summary*

For the reasons discussed above, upon a holistic review of the *Fintiv* factors, we decline to exercise our discretion under § 314(a) to deny the Petition.

IV. CONCLUSION

For the reasons discussed above, Petitioner demonstrates a reasonable likelihood of prevailing in showing that at least one claim of the '702 patent would have been obvious.

V. ORDER

Accordingly, it is:

ORDERED that, pursuant to 35 U.S.C. § 314(a), an *inter partes* review of claims 13–17 of the '702 patent is instituted with respect to all grounds set forth in the Petition; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4(b), *inter partes* review of the '702 patent shall commence on the date of this Decision, and notice is hereby given of the institution of trial.

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