

Filed on behalf of BeSang Inc.

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UNITED STATES PATENT AND TRADEMARK OFFICE

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**BEFORE THE PATENT TRIAL AND APPEAL BOARD**

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MICRON TECHNOLOGY, INC.,  
MICRON SEMICONDUCTOR PRODUCTS, INC., and  
MICRON TECHNOLOGY TEXAS, LLC,  
Petitioners,

v.

BESANG INC.,  
Patent Owner.

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Case No. IPR2023-00900  
U.S. Patent No. 7,378,702

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**PATENT OWNER'S RESPONSE TO  
PETITION FOR *INTER PARTES* REVIEW**

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| 2024        | U.S. Patent No. 6,881,994, Fig. 12B (annotated by Dr. Jack C. Lee)                                                                                                                                                                                                                                                                                                                                                               |

| Exhibit No. | Description                                                                                                                                                                                                                                                                                 |
|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2025        | U.S. Patent No. 6,881,994, Fig. 12B (annotated by Dr. Jack C. Lee)                                                                                                                                                                                                                          |
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## **I. INTRODUCTION**

BeSang achieved its paradigm-shifting invention for monolithic 3D memory only after summing the significant challenges of designing memory cells and control logic with a compatible and manufacturable architecture. The '702 Patent told the world how to build its architecture with low-temperature processing and how to align the layers. Its effort took years of creativity and hard work, and BeSang's breakthrough made the company famous.

Micron acknowledged this feat of engineering at the time. But its IPR Petition years later said the opposite—that a dilettante would have been motivated to use Watanabe's nonstarter "high-temperature bonding" technique with no instructions how to achieve its precise alignment, and then completely transform the pumpkin of Lee's NOR architecture into the modern fantasy of a NAND flash memory. None of Micron's fantastical claims have survived even the start of this trial.

Micron's own expert Dr. Jack Lee (of no apparent relation to the inventor of the Lee patent in Micron's grounds) added nothing at the pre-institution phase by submitting a declaration that did little more than parrot the attorney argument in Micron's Petition. His deposition only confirmed the undeniable truth: nothing about the elegant solution of the '702 Patent is as simple as the Petition promised.

Here the Board found facially insufficient the Petition's Grounds 1-4 based on Watanabe or Lee alone, and ordered trial on the combination of Lee and Watanabe

(plus Endoh) presented in Grounds 5-6. BeSang will start there before addressing Grounds 1-4.

Grounds 5-6 vaguely asserted that one of skill would have been motivated by unspecified “benefits” to fabricate Lee’s memory cells using the “high-temperature bonding” of 900° to 1000°C as specified by Watanabe’s stacking method. Pet. at 72. But that is pure fantasy. Both Dr. Lee and BeSang’s expert Dr. Przybylski agree that transistors are subject to a thermal budget, and Dr. Lee explained that exceeding 650°C even a single time risked frying the embedded transistors, yet Watanabe suggested repeating its bonding 100 times. Dr. Lee also testified that aligning layers was an important semiconductor processing step and having pads that did not touch the adjoining layer was a “no-no” in semiconductor design, resulting in missed electrical connections. Yet Watanabe provided no teaching on alignment, despite depicting small pads with tight alignment constraints. Micron’s argument for a motivation to combine Lee and Watanabe is devoid of support, and the combination falls apart under its own weight. For any of these reasons, all Challenged Claims 13-17 should be confirmed over Grounds 5-6.

The Petition does not improve for the dependent Claims 14-17 challenged in Grounds 5-6. It falls short of its burden, simply cross-referencing to other portions of the Petition and failing to show why and how the “alternative” and disparate embodiments in Lee and Endoh would be combined. The Petition does not specify

its grounds with particularity because it provides no detail on how to apply Watanabe to Lee (Claims 14-15) or how to transform Lee’s NOR architecture into a NAND memory based on Endoh (Claims 16-17). Indeed, when asked how to create a NAND architecture out of the Lee patent’s memory cell, Dr. Lee just could not do it. His failure dooms the combination for the poor skilled artisan.

For Grounds 3-4 based on the Lee patent, the Petition fails to show a motivation to combine Lee’s alternative and incompatible embodiments in Figures 1A and 83A (Claims 13-17) and in Figures 7 and 83A (Claim 15). Patentability also should be confirmed because Dr. Lee (and his blue pen) acknowledged at deposition that the Lee patent does not satisfy either Claim 13 or Claims 16-17.

Lastly, Grounds 1-2 are deficient because the Petition fails to establish both a motivation to combine Watanabe’s DRAM and EPROM embodiments and that Watanabe taught or suggested a non-volatile memory cell as required by Claim 13[b], as the Board correctly recognized at institution. Paper 9 (“I.D.”) at 14-16. The Board also correctly found that Watanabe did not teach or suggest the claimed “SOI pillar” required by Ground 2. *Id.* at 16-17. In addition, Dr. Lee’s admission confirmed that Watanabe’s high-temperature stacking method is not enabled.

As the Federal Circuit has recognized, semiconductor manufacturing has significant “complexity,” and, with good reason, the Board holds petitioners to the requirements of establishing a motivation to combine and “look[ing] for specific

evidence that a person of ordinary skill in the art would have reasonably expected success.” *Samsung Elecs. v. Elm 3DS Innovations*, 925 F.3d 1373, 1382-83 (Fed. Cir. 2019). Micron is no fairy godmother, and its wishful throwing together of random semiconductor features does not result in the invention of the ’702 Patent. Examined more closely, its Petition is just a pumpkin after all.

The Challenged Claims should be confirmed for any of these reasons.

## **II. BACKGROUND**

### **A. A New Breakthrough In 3D Memory**

Conventional CMOS technology relied on shrinking memory cells to obtain high-capacity storage devices. BeSang was trying to achieve an outside-the-box solution: further increasing memory capacity by going vertical. EX1001 at 1:23-2:3. Much like skyscrapers increase density by vertically stacking floors (as compared to a single-story building), stacking memory cells on top of each other could increase memory density in a given base area without shrinking individual memory cell size. The issue was how to design a chip that could be manufactured to realize the potential of this 3D memory.

In 2004, inventor Sang-Yun Lee filed the application that issued as U.S. Patent No. 7,378,702 (“’702 Patent”) containing his solution. In 2008, BeSang in collaboration with Stanford University had achieved “a 3D IC technology breakthrough” by fabricating a 3D IC “contain[ing] 128 million vertically oriented

devices.” EX2005 at 1. Start-up BeSang was suddenly famous: widely praised in the industry and called a “pioneer” in 3D solutions with a design presenting “clear-cut winning edges” over existing memories. EX2008 at 17; EX2009 at 1; *see also* Paper 6 (“POPR”) at 1, 5-6. It took the rest of the industry seven years to catch up, including Micron and Intel who had initially expressed a lot of interest in working with BeSang. EX2014 at 1; EX2015 at 1-2; EX1019 ¶¶ 34-35; IPR2023-00991, EX1013 ¶ 29; *see also* POPR at 7.

## **B. The Invention Of The ’702 Patent**

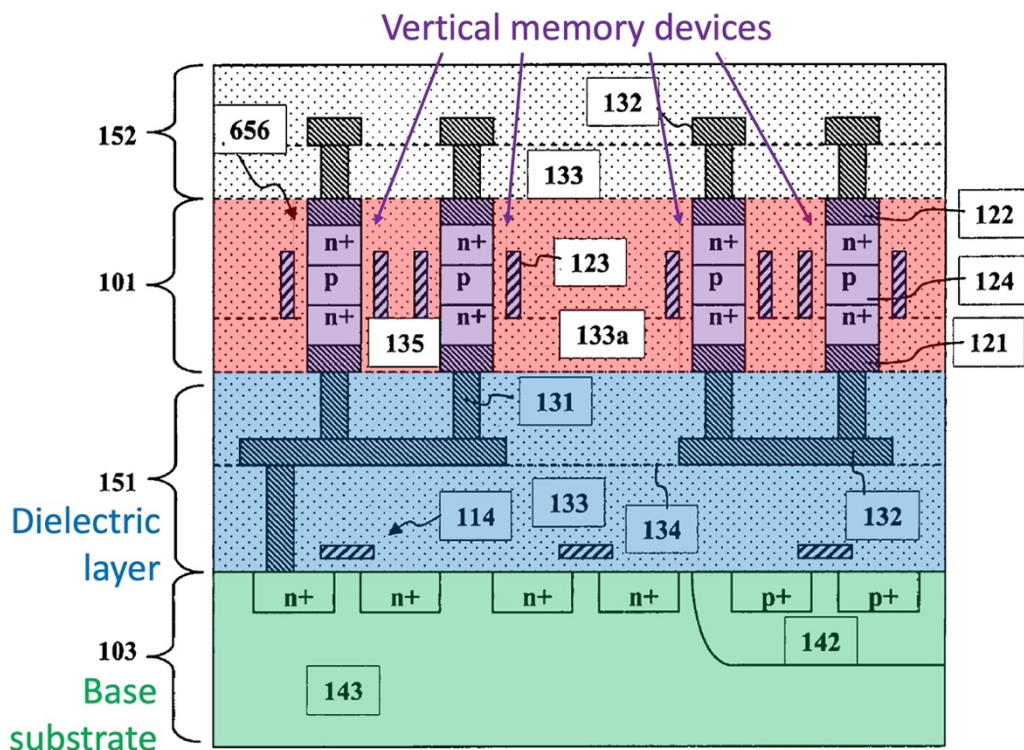
The ’702 Patent is titled “Vertical Memory Device Structures.” The patent innovated by solving the significant practical challenges posed by scaling two-dimensional memory technologies.

The ’702 Patent recognized the need for “structures and methods that are suitable for providing increased circuit density in integrated circuits without necessarily requiring devices to be made smaller.” EX1001 at 1:40-43. It describes the use of vertical memory cells, which allows the memory array to expand in a third dimension, as well as putting logic circuitry underneath the memory array, which further increases density and helps achieve faster performance. *Id.* at 3:51-61, 5:60-63, Fig. 1; *see also* EX2029 ¶¶ 38-47.

Figure 1 of the ’702 Patent, reproduced below, shows “vertical memory devices 656” that “are separated by isolation 135 and have floating structures in the

filled dielectric materials 133a.” EX1001 at 5:18-21. Dielectric materials are those that are substantially nonconducting. EX2029 ¶ 43.

Fig. 1



EX1001 at Fig. 1 (annotated).

Compared to the high-temperature devices at the time, the '702 Patent recognized the benefits of manufacturing its 3D integrated circuits at low process temperatures, *i.e.*, below 650°C, including gate oxidation at low temperatures. *See, e.g., id.* at 7:15-35. Among other benefits, BeSang discovered that if the gate dielectric layer has a combination of low temperature thermal oxide, high-K

dielectric, and CVD dielectric, then device reliability increases, current-driving capability increases, and on-resistance decreases.

The '702 Patent further explains that “combining the SOI layer with a semiconductor substrate does not require the same type of wafer alignment structures as are used in photolithographic processes” and that “rather, the wafer alignment structure may be implemented as a wafer alignment mark, or as a bump-type alignment structure.” *Id.* at 6:13-18. It teaches that, “without a wafer alignment structure, the SOI layer could be transferred along with a simple notch alignment” because the “transferred, unpatterned, SOI layer has only a vertically oriented stack of layers” and “does not have structures for multiple devices, such as isolation structure or interconnection lines, which are horizontally divided.” *Id.* at 6:18-25.

**C. U.S. Patent No. 5,091,762 (“Watanabe”)**

Watanabe shows a design for “a semiconductor memory device used for a dynamic RAM,” or DRAM. EX1005 at 1:10-12. Filed in 1990, the patent issued in 1992. *Id.* at 1.

Figure 2A below shows a sectional view of Watanabe’s DRAM. *Id.* at 2:63-64. Watanabe’s DRAM includes a planar capacitor formed between the charge storage region 45 and the capacitor electrode 46, with a capacitor insulating film 47 interlayered between them. *Id.* at 3:24-27. In Figure 2A, data flows horizontally through the “data plane 41.” *Id.* at 3:16-18 (“In operation, the planar

n+ type Si layer 41, or a data plane 41, serves as a wire for the input and output of data to and from the memory cell.”).

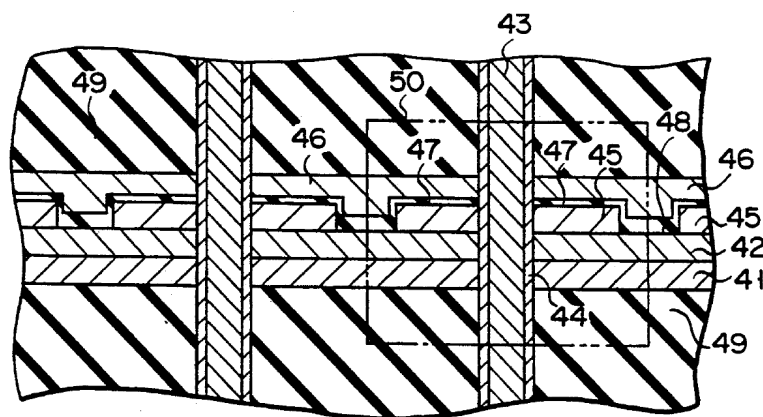


FIG. 2A

*Id.* at Fig. 2A.

Watanabe includes two “[m]ethods used to form wires passing through the planar members” of the data plane: the “laminating method” and the “stacking method.” *Id.* at 5:1-3; *see also id.* at 4:54-55 (“The data plane (or word plane) is planar, not a thin line.”), 5:8-11 (laminating method in Figures 5A-5E), 5:56-57 (stacking method in Figures 6A-6D); *see also* EX2029 ¶¶ 48-54.

Micron agrees that Watanabe’s stacking method is described in Figures 6A-6D (see below). *Pet.* at 14; *see also* EX1005 at 2:31-35, 5:56-57.

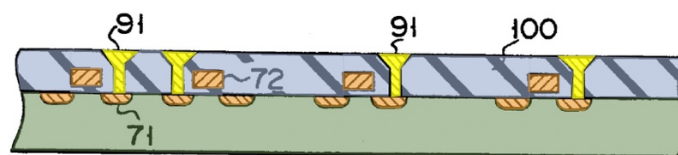
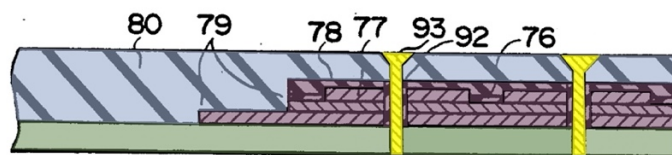


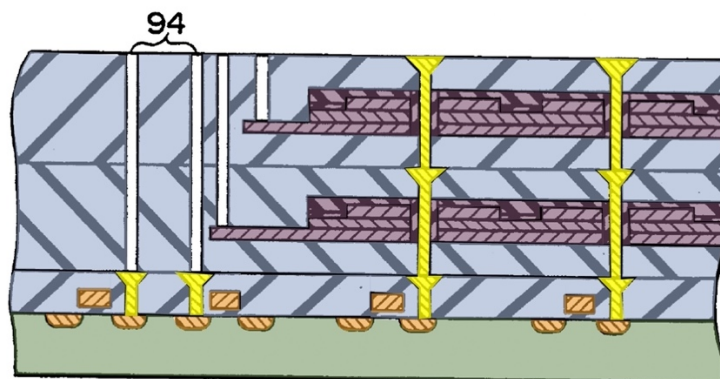
FIG. 6A

In Figure 6A of the stacking method, “a peripheral circuit and transistors 71 and 72 [orange] are formed in the surface region of an Si substrate.” EX1005 at 5:58-60. Next “insulating film 100” is applied, “contact holes 91” (yellow) are created and filled with “conductive material 91.” *Id.* at 5:60-63.



**F I G. 6 B**

Next Figure 6B shows a planar member formed in the same way as in Figures 5A-5B. *Id.* at 5:64-65. Figure 5A, like Figure 6A, shows transistors formed “in the upper surface of a silicon substrate.” *Id.* at 5:11-13. Figure 6B shows “[c]ontact holes 93 [yellow] are formed in the planar member, an oxide film 92 is applied to the inner side wall of each contact hole, and a first wire 93 is completed.” *Id.* at 5:65-68.



**F I G. 6 C**

After forming the planar members, Watanabe instructs bonding them as shown in Figure 6C: “the planar members thus formed are bonded together” using a “thermal process of 900° to 1000° C.” *Id.* at 6:6-8. Watanabe provides no further disclosure for bonding, or how to align its planar members for bonding. *See id.*

**D. U.S. Patent No. 6,881,994 (“Lee”)**

The Lee patent issued on April 19, 2005. EX1007 at 1. Lee sought to “provide[] an ultra dense matrix array” in a monolithic semiconductor memory device with “an increased density.” *Id.* at 11:20-23. Lee taught two techniques to achieve a denser “monolithic” architecture where “layers of each level of the array were directly deposited on the layers of each underlying level.” *Id.* at 11:26-29.

The inventors found “planariz[ing] by chemical mechanical polishing” could smooth the semiconductor surface and “achieve[] flatness on the order of 4000 Angstroms [400 nm] or less.” *Id.* at Abstract, 11:33-49; *see also* EX2029 ¶ 57; EX2033 at 61. Or, Lee taught that manufacturing accuracy was improved through precise “self-alignment and using the same photolithography step to pattern different layers” or “etch[ing] using the same photoresist mask” to minimize “misalignment tolerances” during chemical deposition. EX1007 at 12:34-49.

Lee includes over one hundred figures of disparate memory designs. *See id.* at 8:17-11:14, Figs. 1A-101.

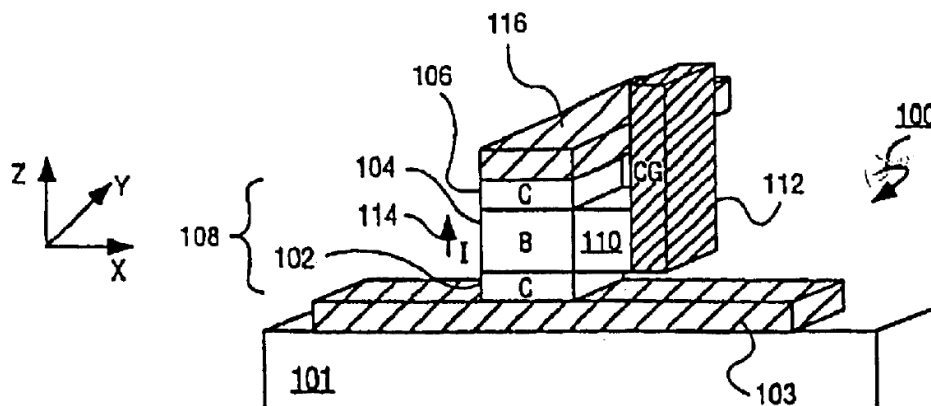


**FIG. 1A**

Lee's Figure 1A (above) shows a memory device from one of its embodiments. *Id.* at 14:11-13; *see also* EX2029 ¶ 56. Figure 1A shows a “vertical” read current path”:

During read operations of device 100, when a conductive channel is formed in body 104, current 114 flows vertically (z) (or perpendicular) with respect to the plane (x-y) of the substrate 101 above which pillar memory device is formed.

EX1007 at 14:51-56.

**E. U.S. Patent Application Publication No. 2002/0154556 (“Endoh”)**

The Petition relies on the 1,743-page Endoh as a secondary reference solely for the challenged dependent claims. Pet. at 3-4; *see generally* EX1006. Figure 65 shows a NAND memory array in one of Endoh's many embodiments. EX1006 ¶¶ 257-58; *see also* EX2029 ¶ 55.

### III. LEVEL OF ORDINARY SKILL IN THE ART

The parties agree that a person of ordinary skill in the art at the time of the invention would have had a bachelor's degree in electrical engineering, computer engineering, or a related field, and at least two years of experience in the research, design, or development of semiconductor memory device structures, or the equivalent, with additional education substituting for experience and vice versa. Pet. at 8; EX1002 ¶ 34; EX2029 ¶¶ 33-37.

### IV. CLAIM CONSTRUCTION

Despite bearing the “burden to explain how challenged claims are to be construed and how the claims read on the prior art,” Micron’s Petition offered no construction of any claim terms. *Maxlite, Inc. v. Jiaying Super Lighting*, IPR2020-00181, 2020 WL 5803082, at \*2 (P.T.A.B. Sept. 29, 2020) (citing 37 C.F.R. § 42.104(b)(3)-(5)); Pet. at 12 (“Petitioner does not believe that any term requires explicit construction....”).

#### A. “stackable add-on layer”

Micron and its expert Dr. Jack Lee knew when Micron filed its Petition that the construction of “stackable add-on layer” was determinative for some grounds. *E.g.*, Pet. at 48 n.5 (asserting that “Lee discloses the subject matter of the ’702 Patent *under the interpretation PO appears to adopt*” (emphasis added)); EX2028 at 180:9-183:4. Micron bore the burden of setting forth constructions for terms

requiring construction in its Petition. *Maxlite*, 2020 WL 5803082, at \*2. Yet Micron decided not to provide a construction of “stackable add-on layer.” *See* Pet. at 12-13.

The Board provided its interpretation of “stackable add-on layer” at institution:

a layer that is formed separately from the substrate and then bonded as whole to the dielectric layer positioned above the substrate. We do not understand a “stackable add-on layer” to include memory cells that are formed by sequential deposition on or above a substrate without being added to a separately formed substrate.

I.D. at 9.

BeSang respectfully disagrees with the Board’s preliminary construction of “stackable add-on layer” because it is incorrect. Although Micron must prove a construction of “stackable add-on layer” and establish that the construction is met by the asserted art to prove invalidity, the Board may confirm the patentability of the Challenged Claims for reasons unrelated to “stackable add-on layer.” *Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (“The Board is required to construe only those terms that are in controversy, and only to the extent necessary to resolve the controversy.” (cleaned up)).

## **B. “SOI pillar”**

Micron also decided not to proffer any construction of “SOI pillar.” *See* Pet. at 12-13. The Board noted that Micron and its expert “appear to assume that any

vertically stacked structure with at least two layers would be understood to disclose or render obvious a ‘pillar,’” and asked the parties to “provide an express definition of ‘SOI pillar.’” I.D. at 17.

If the Board deems construction necessary, “SOI pillar” should be construed according to its ordinary and customary meaning as “a silicon-on-insulator structure taller than it is wide.” EX2029 ¶¶ 58-63. This definition accords with well-understood concepts of pillar structures and the SOI pillar embodiments in the ’702 Patent.

Dictionaries define “pillar” as a structure that is “relatively slender in proportion to its height.” *E.g.*, EX2031 at 1469 (Webster’s: “pillar” defined as “an upright shaft or structure, of stone, brick, or other material, relatively slender in proportion to its height...”); EX2032 at 988 (same).

This definition is consistent with the ’702 Patent’s depictions and descriptions of SOI pillars. The below figures show proportionally slender pillars:

Fig. 4

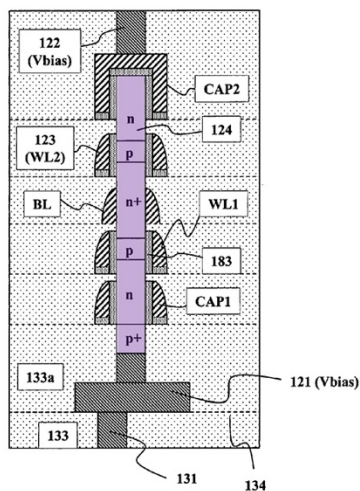


Fig. 20

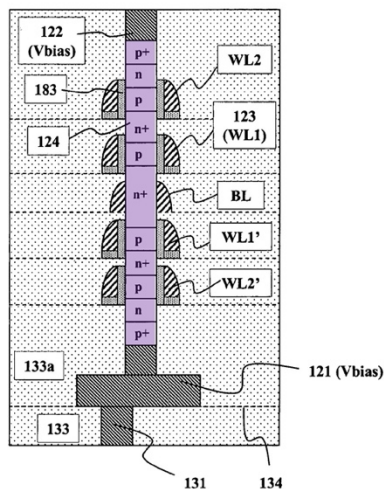
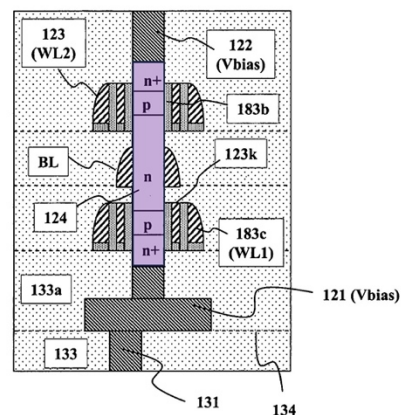


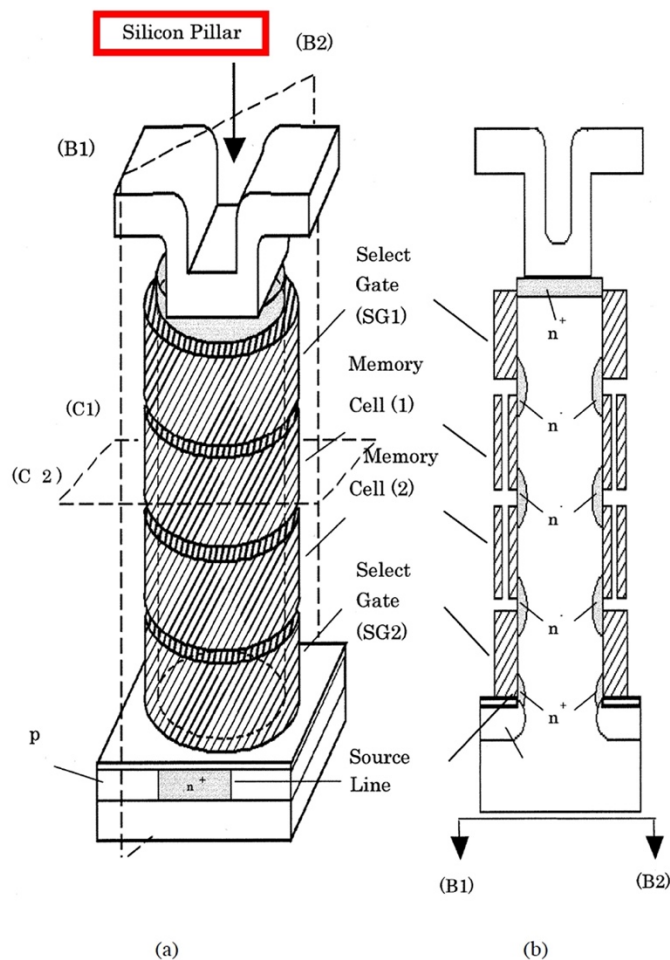
Fig. 27



EX1001 at Figs. 4, 20, 27 (depicting SOI pillars annotated in purple). For Figure 4, the '702 Patent explains that “the aspect ratio of SOI pillar 124 remains relatively small” given its larger height relative to its width. *Id.* at 8:5-10.

The Board correctly found that “both the '702 patent and Lee refer to pillars where the height of the structure is substantially larger than its width, which stands in contrast to the doped, horizontal layers above insulator 49 Petitioner identifies in Watanabe Figure 2A.” *I.D.* at 17 (citing EX1001 at Figs. 1, 4, 8:5-11; EX1005 at Fig. 2A; EX1007 at 8:18-19).

Micron’s own cited references support this construction. Exhibit 1022 depicts flash memories with “pillar” structures where the height is larger than the width:



EX1022 at Fig. 3(a)-(b) (annotated); *see also id.* at Fig. 5 (showing SEM photograph of S-SGT structured cell with silicon pillars). Exhibit 1030 also shows a “three-dimensional high-density S-SGT flash memory [that] is fabricated by arraying S-SGT *pillars*” in Figure 1:

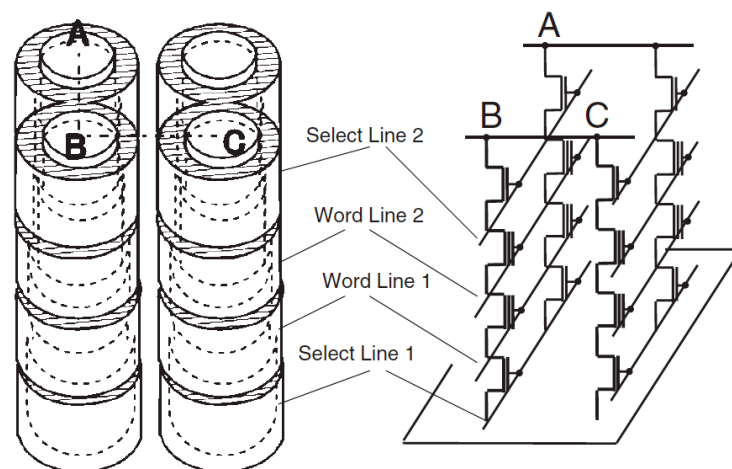


Fig. 1. Bird's eye view of the new three-dimensional high-density S-SGT flash memory and its equivalent circuit.

EX1030 at 2217 (emphasis added), Fig. 1.

Micron's expert Dr. Lee offers nothing helpful on "SOI pillar." Dr. Lee admitted: "I don't know what the plain and ordinary meaning is for 'pillar.'" EX2028 at 66:22-67:13. Given that claim terms are to be given their plain and ordinary meaning, *see* 37 C.F.R. § 42.100(b), Dr. Lee's testimony is legally irrelevant by his own admission.

Even if considered, Dr. Lee's ever-malleable opinion about "SOI pillar" cannot be credited. In his declaration, Dr. Lee initially opined that "pillar-form" meant "vertical columnar-shaped." EX1002 ¶ 64. Then at deposition, Dr. Lee disavowed his declaration and claimed that "pillar" means "dope stack structure" with no specific shape implied by the term. EX2028 at 65:13-66:21.

Dr. Lee based his new definition on the '702 Patent's reference to "individual doped stack structures (i.e., pillar structures)." *Id.* at 67:22-68:16 (quoting EX1001

at 6:26-29). Dr. Lee’s unnatural interpretation has it exactly backward—the Federal Circuit has held that using “i.e.” does not define what follows the “i.e.” based on what precedes it:

we are not proposing that the definition of “two-dimensions” (the term that follows “i.e.” here) be restricted to or defined as only “beads” (the word that precedes “i.e.”). We do the opposite: we read “beads” (the word that precedes “i.e.”) to be defined by “two-dimensions” (the term that follows “i.e.”). That is a natural interpretation of “i.e.”

*SkinMedica, Inc. v. Histogen Inc.*, 727 F.3d 1187, 1201 (Fed. Cir. 2013). Even Dr. Lee did not use “i.e.” his unnatural way in his own declaration. *Compare* EX1002 ¶ 64 (Dr. Lee: “pillar-form (i.e., vertical columnar-shaped)”) *with* EX2028 at 67:8-9 (also Dr. Lee: “I don’t know what the plain and ordinary meaning is for ‘pillar.’”). His testimony that “i.e.” meant “equal to” to a skilled artisan withstands no scrutiny. *See* EX2028 at 71:13-18.

Then Dr. Lee’s opinion on “SOI pillar” evolved again the moment his deposition was back on the record after lunch. *Id.* at 83:9-16 (“Excuse me. I would like to make a correction to my earlier answer.”). After spending lunch with counsel for Micron when he assured BeSang he did not discuss his testimony, *id.* at 114:11-17, Dr. Lee summoned “a lot more examples” in the ’702 Patent that he imagined supported his definition because they refer to vertical transistors as

“pillars,” *id.* at 83:6-86:9. Because not a single one of these additional passages supports Dr. Lee’s definition, they are irrelevant.

Despite construing “SOI” as silicon-on-insulator, *id.* at 79:20-80:3, and “pillar” as “dope stack structure,” *id.* at 65:13-66:21, Dr. Lee opined that “SOI pillar” should be defined as a 27-word tract: “a dope stack structure formed from a single-crystal portion of a semiconductor wafer transferred from one wafer to another previously fabricated wafer or similar type of substrate,” *id.* at 136:3-18. Dr. Lee’s made-up definition is a nonsensical hybridization of the ’702 Patent’s discussion of the “SOI layer.” EX1001 at 4:47-53; *see also* EX2028 at 136:7-10. Because it does not address the term “SOI pillar,” it is irrelevant.

Micron’s construction of “SOI pillar,” to the extent it aligns with Dr. Lee’s, is entirely baseless and should be rejected.

## **V. LEGAL REQUIREMENTS TO SHOW OBVIOUSNESS**

To prove obviousness, Micron must establish a motivation to combine the references and that one of ordinary skill would have had a reasonable expectation of success in making the combination. *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1367-68 (Fed. Cir. 2016). One of skill “would not have been motivated to combine... references to arrive at the claimed invention” where doing so “would be beyond the technical ability of a skilled artisan.” *MobileMedia Ideas LLC v. Apple Inc.*, 780 F.3d 1159, 1167-68 (Fed. Cir. 2015). An obviousness

analysis also requires a determination of “whether a person of ordinary skill in the art, having all the teachings of the references before him, is able to produce the structure defined by the claim.” *Samsung Elecs*, 925 F.3d at 1382 (citation omitted). In complex “integrated-circuit technology,” a petitioner should show “specific evidence that a person of ordinary skill in the art would have reasonably expected success in combining” the references. *Id.* at 1382-83.

**VI. THE PETITION DOES NOT MEET ITS BURDEN FOR  
CONTINGENT GROUNDS 5-6 COMBINING LEE WITH  
WATANABE’S “STACKING METHOD”**

The Board instituted trial principally to consider the combination of Lee and Watanabe in Grounds 5-6. *I.D.* at 25-27. On a full evidentiary record, Micron fails to establish obviousness under either ground: Ground 5 combining Lee and Watanabe for Claims 13-15, *Pet.* at 69, and Ground 6 adding Endoh to the combination for Claims 16-17, *id.* at 73-74.

Micron explained its Grounds 5-6 were contingent grounds, acknowledging that “Lee discloses forming vertically oriented memory devices through layer-by-layer sequential deposition on the substrate,” and asserting that one of skill instead would have used Watanabe’s “‘stacking method’ of bonding... through high-temperature bonding.” *Id.* at 72. These contingent grounds are unsupported, because the Petition has not established that one of skill “would have been motivated to modify Lee in view of Watanabe to use its ‘stacking method.’” *Id.*

It's not seriously disputed that one of ordinary skill would have steered clear of combining Watanabe's stacking method with Lee. Micron's Petition expressly acknowledged that Watanabe used "high-temperature bonding," Pet. at 72, which occurred at 900-1000°C, EX1005 at 6:6-8. Both parties' experts agree that subjecting transistors to temperatures over 650°C would have exceeded the transistors' thermal budget and risked frying the memory cells. EX2028 at 123:9-124:7; EX2029 ¶¶ 70-77. Because Watanabe's high-temperature bonding instructed getting much hotter than 650°C, one of skill would not have used its stacking technique with Lee.

And Watanabe says nothing about alignment, which is a fundamental flaw because Watanabe's design requires precisely aligning its layers within about two minimum feature sizes of a memory cell. The Petition ignores these foundational flaws and provides no actual reason why one of skill reading Lee would have gone back more than a decade to Watanabe's facially unworkable technique. Because the Petition musters no supported motivation to combine (let alone with any reasonable expectation of success), and Dr. Lee himself repudiated any motivation, Micron cannot meet its burden for Ground 5.

Ground 6 adds Endoh to the mix and fares no better. Micron's cross-referencing does not meet its burden to show unpatentability. Purporting to magically replace Lee's NOR configuration with a serial, NAND configuration from

Endoh is not an obvious tweak, but a fundamentally different semiconductor chip. With Dr. Lee himself unable to combine them at his deposition, EX2028 at 94:6-98:11, Micron can hardly argue a less experienced, non-expert person of ordinary skill would be motivated to make the combination. Micron fails to show a motivation to combine these disparate features, let alone with any reasonable expectation of success, again failing to meet its burden for Ground 6.

For any of these reasons, the Challenged Claims should be confirmed over Grounds 5-6.

**A. A Skilled Artisan Would Not Have Been Motivated To Combine Watanabe With Lee Nor Reasonably Expected Success (All Claims 13-17)**

The Petition does not establish a motivation for one of ordinary skill to combine Lee and Watanabe. “[O]bviousness concerns whether a skilled artisan not only *could have made* but *would have been motivated to make* the combinations or modifications of prior art to arrive at the claimed invention.” *Belden v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015) (emphasis in original). As the Board has explained:

It is not enough to assert that the prior art provides two options and that it would have been predictable to implement either. An obviousness rationale generally requires some identification of “a design need or market pressure to solve a problem” before looking at the “finite number of identified, predictable solutions.”

Micron Technology v. BeSang Inc.  
Patent No. 7,378,702 – IPR2023-00900

*Palo Alto Networks, Inc. v. Finjan, Inc.*, IPR2015-01979, 2017 WL 1040259, at \*24 (P.T.A.B. Mar. 15, 2017) (quoting *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 421 (2007)).

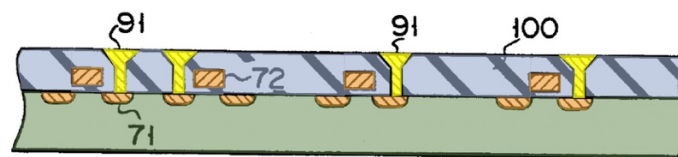
Establishing a reason or motivation to combine the prior art is a critical guardrail against “the distortion caused by hindsight bias” and the “temptation to read into the prior art the teachings of the invention in issue.” *KSR*, 550 U.S. at 421 (quoting *Graham v. John Deere Co.*, 383 U.S. 1, 36 (1966)). A motivation to combine requires “explain[ing] the *reason why* a PHOSITA would have been motivated to modify” a reference in view of another to include a feature taught by the claimed invention. *In re Nuvasive, Inc.*, 842 F.3d 1376, 1384 (Fed. Cir. 2016) (emphasis in original).

To meet limitations 13[b]-[c] in its contingent Ground 5, the Petition exclusively relied on Watanabe, asserting that its stacking method “discloses” them. Pet. at 71-72. But a skilled artisan would have understood that Watanabe’s stacking method simply would not work with Lee. Moreover, Watanabe provided no guidance for how a skilled artisan seeking to use its stacking method would align wafers being stacked—a critical oversight precluding successful manufacture of working devices. Also, the Petition’s hindsight-driven analysis, picking and choosing from hundreds of figures among Lee and Watanabe, should be vetoed. *KSR*, 550 U.S. at 421 (warning against “the distortion caused by hindsight bias”).

Given the overwhelming and undisputed evidence that Watanabe's stacking method was unworkable, all claims should be confirmed over Grounds 5-6.

**1. Watanabe's High-Temperature Bonding Would Exceed The Thermal Budget And Damage Lee's Transistors**

Watanabe's stacking method in Figure 6 taught high-temperature bonding after fabricating its transistors. EX1005 at 5:56-57. In the first step of "FIG. 6A, a peripheral circuit and transistors 71 and 72 are formed in the surface region of an Si substrate":



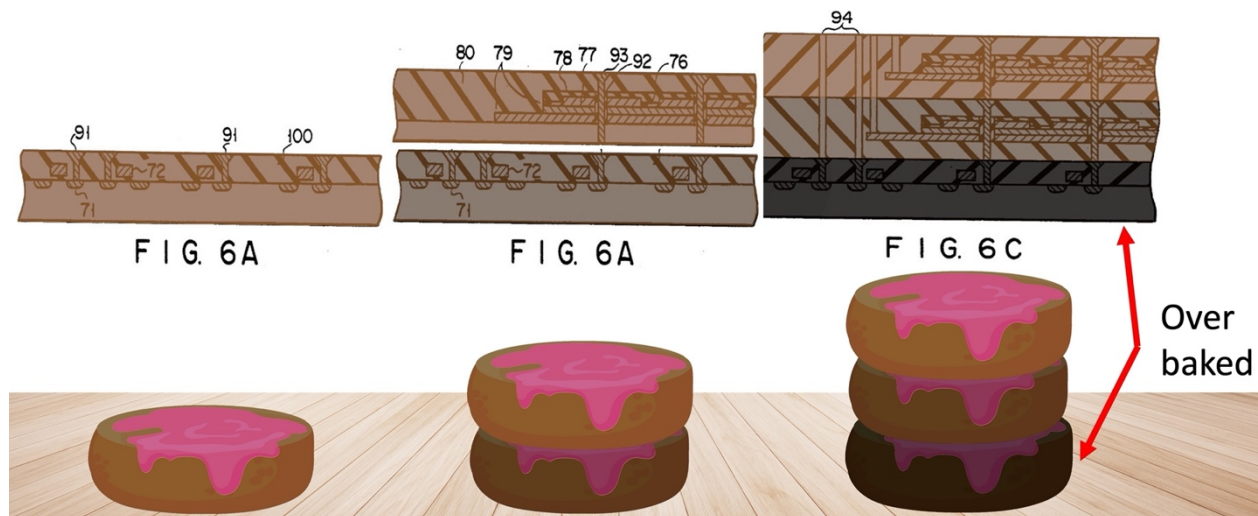
**F I G. 6 A**

*Id.* at 5:58-63, Fig. 6A (annotated); EX2029 ¶ 51. Then the planar members with memory cells are fabricated in Figure 6B. EX1005 at 5:64-68; EX2029 ¶¶ 52, 66. Finally the layers are then "bonded together" in Figure 6C where "[t]he bonding is made by thermal process of 900° to 1000° C." EX1005 at 6:6-8; EX2029 ¶¶ 53, 67.

Dr. Lee testified that one of skill would have known in 2004 that transistors embedded in the Figure 6A substrate are subject to a thermal budget that constrains subsequent high-temperature processing steps. EX2028 at 125:6-126:7; EX2027 at 715 ("[T]o avoid additional dopant diffusion or interfacial oxide growth on bottom transistor, LT (<650°C) top FETs process is mandatory."); *see also* EX2028 at

126:8-20 (explaining that these issues were known in 2004); EX2029 ¶¶ 70-72. Exposing the transistors' sources and drains to high temperatures risks further diffusion of doped ions, degrading the function of these doped regions away from the transistors' design parameters. EX2028 at 125:15-126:7; EX2029 ¶¶ 73-74. Both Lee and Watanabe's transistors were formed by sequential deposition. EX1005 at 5:58-63 (explaining sequential deposition formation of substrate in Figure 6A); Pet. at 70 ("Lee discloses forming vertical memory devices through layer-by-layer sequential deposition on the substrate...."); *id.* at 72 (same). Thus, they would have been subject to the thermal budget Dr. Lee described above requiring future processing to be low temperature—less than 650°C.

Because the thermal budget is cumulative (an integral of temperature over time), Watanabe's teaching of multiple bonding steps dangerously compounded the thermal damage risk. EX2029 ¶¶ 75-76; EX2028 at 125:6-126:7; EX1005 at 6:6-14 (explaining that the "number of process steps is increased" for each layer because each layer is first bonded, then wired). Indeed, Watanabe contemplated bonding 100 layers, with 100 high-temperature bonding steps. EX1005 at 4:35-38, 6:6-14; EX2029 ¶ 76. Much like bakers know that baking cake layers sequentially is a terrible idea because repeated baking would burn the initial layers, one of skill would have steered clear:



EX1005 at Figs. 6A-6C (annotated and illustrations added); EX2029 ¶ 76; EX2027 at 715. The situation is even more dire in semiconductors, because according to Dr. Lee even a single bad bake of high-temperature bonding at 900°C (as taught by Watanabe) would have risked frying the earlier transistors. EX2028 at 123:13-124:7 (“[T]he processing of the upper layer transistors cannot go above 650 degrees C, as described in [EX2027].”).

Both Micron’s Petition and Dr. Lee acknowledge and expressly rely on Watanabe’s “high-temperature bonding,” which requires temperatures at or above 900°C. Pet. at 72; EX1002 ¶ 149; EX1005 at 6:6-8 (“The bonding is made by thermal process of 900° to 1000° C.”). But at deposition, Dr. Lee admitted that such “high-temperature bonding” could not be safely used. See EX2028 at 123:13-124:7 (“[T]he processing of the upper layer transistors cannot go above 650 degrees C, as described in [EX2027].”); *see also* EX2029 ¶¶ 75-76. By contrast, the ’702 Patent

expressly provides for low temperature processing to avoid this issue. EX1001 at 7:15-35 (“The FLD, in accordance with the present invention, has a gate dielectric layer which may be implemented with process operations at temperatures below 650° C.... [T]he FLD architecture does not require a high temperature process....”); EX2029 ¶ 76.

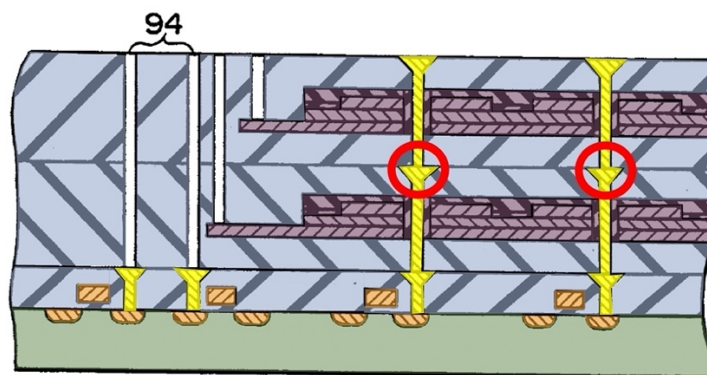
The Petition simply provides no motivation for using Watanabe’s dangerous high-temperature technique in Lee and cannot meet its burden to show obviousness in Grounds 5-6, particularly given Dr. Lee’s testimony that a skilled artisan would have known better than to use Watanabe’s “high-temperature bonding”—the very method the Petition proposed. EX2029 ¶¶ 75-77; *Redline Detection, LLC v. Star Envirotech, Inc.*, 811 F.3d 435, 453 (Fed. Cir. 2015) (affirming no motivation to combine: “A PHOSITA in July 1999 would have no reason to remove the ambient air from Gilliam and replace it with inert gas from Stoye” where it “can damage closed EVAP systems with volatile compounds.”); *Streck, Inc. v. Ravgen, Inc.*, IPR2021-01577, Paper 62 at 87 (P.T.A.B. Apr. 18, 2023) (no motivation to combine where modified method “could damage the cffDNA analyte in the sample itself, frustrating its detection and analysis”).

## **2. Watanabe Did Not Teach How To Align Its Layers**

The Petition further fails to meet its burden for showing one of skill would have modified Lee with Watanabe's stacking method for a second reason: Watanabe provided no teaching on how to correctly align the layers. *See* EX1005 at 6:6-14.

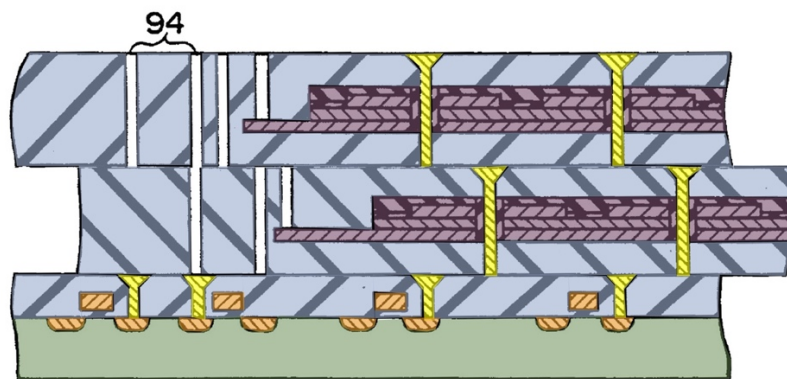
Both experts agree that alignment is an important step in semiconductor processing. EX2028 at 109:20-110:16 (Dr. Lee: alignment is an important step in semiconductor processing); EX2037 at 47 ("Providing adequate alignment may be the most challenging requirement to achieve the interconnect density necessary for 3D technology to replace on-die interconnects."); EX2029 ¶ 78. The '702 Patent's disclosures explicitly account for this critical concern in formulating aligned semiconductor structures. EX1001 at 6:13-25 ("[C]ombining the SOI layer with a semiconductor substrate does not require the same type of wafer alignment structures as are used in photolithographic processes...."), EX2029 ¶ 78. But Watanabe offers nothing, nor does Dr. Lee's tag-along declaration point to anything in Watanabe. *See* EX1005 at 6:6-14; EX1002 ¶¶ 148-49; EX2029 ¶¶ 78, 81.

Alignment is vital here because Watanabe itself requires high-precision alignment. EX2029 ¶¶ 78-80. Watanabe's Figure 6C shows small landing pads that vias in upper layers must contact to make necessary electrical connections for an operable chip:



F I G. 6 C

EX1005 at Fig. 6C (annotated with red circles denoting landing pad locations); EX2029 ¶ 80; EX2028 at 110:17-112:8. As shown, the landing pads are about twice the minimum feature size, which historically referred to the size of the transistor gate. EX2029 ¶¶ 79-80. The experts again agree that if the landing pads and vias do not align within those parameters, the device would not work. *Id.* ¶ 80 (explaining that a small misalignment would result in unintended open circuits or a non-functional device); EX2028 at 111:15-114:2 (Dr. Lee: “if the upper layer metal completely [did] not touch the underlying contact pad” then “the wire would not [] be connected together, that is a no-no”).



F I G. 6 C

EX1005 at Fig. 6C (annotated and modified to illustrate misaligned layers).

Because Watanabe says nothing about how to achieve such precise alignment of its layers, one of skill is essentially left flying blind when following its stacking method. The Petition did not rely on Lee's own alignment approach nor did it provide an alternative. *See* Pet. at 71-73. With no guidance on how to align these wafers, one of skill would not have been motivated to use Watanabe's stacking method in Lee. EX2029 ¶ 81; *MobileMedia Ideas*, 780 F.3d at 1167-68 (affirming no motivation to combine where "using that technique" "would be beyond the technical ability of a skilled artisan").

### **3. Micron's Cherry-Picking From Among Lee And Watanabe's Teachings Show The Combination Is Improperly Hindsight-Driven**

The purported motivation to combine here, devoid of any explanation or supporting evidence, can only be described as hindsight-driven. Here "Petitioner improperly works backwards from the challenged claims to cherry pick" features

from the reference in an “exercise [that] bears the unmistakable taint of impermissible hindsight reconstruction.” *3M Co. v. Bay Materials*, IPR2022-01214, 2024 WL 168075, at \*8 (P.T.A.B. Jan. 16, 2024); *see also ATD Corp. v. Lydall, Inc.*, 159 F.3d 534, 546 (Fed. Cir. 1998) (“Determination of obviousness can not be based on the hindsight combination of components selectively culled from the prior art to fit the parameters of the patented invention.”). The Petition’s obviousness analysis is insufficient on its face.

Lee includes more than 100 drawings of various semiconductor designs. *See* EX1007 at Figs. 1A-101. To satisfy Claim 13, the Petition picks only three (Figures 1A, 35, and 83A), with no explanation for their selection. *See* Pet. at 46-54; *see also*, e.g., EX1007 at 8:17-18 (“FIG. 1A is... a pillar memory....”), 13:23-26 (disclosing separate “pillar,” “self-aligned,” and “rail stack” alternative embodiments), 55:26-28 (“FIG. 83A illustrates... a rail stack configuration....”), 55:8-10 (“The TFT EEPROMs may be arranged in the pillar, self-aligned TFT *or* rail stack configurations of the previous embodiments.” (emphasis added)); EX2029 ¶¶ 113-122, 126-27. Then the Petition resorts to Watanabe’s ineffectual and dangerous teachings to cobble together the remaining two limitations 13[b]-[c] in Ground 5. Using the ’702 Patent as a roadmap to select among myriad embodiments amounts to nothing more than hindsight and falls far short of satisfying Micron’s burden. *3M*, 2024 WL 168075, at \*12 (“Petitioner, without adequate explanation,

begins its analysis with an assumption that the artisan would have been led to focus on embodiments from Hinz that are cherry-picked to meet the [claim] limitation.”); *ATD Corp.*, 159 F.3d at 546.

**B. The Petition Fails To Support The Combination Of Lee And Watanabe As A Matter Of Law (All Claims 13-17)**

**1. Micron’s Generic Statements Are Insufficient To Establish A Motivation To Combine**

Micron asserts a motivation to combine because Watanabe offers “an alternative method” and this would provide unspecified “benefits associated with that method.” Pet. at 70 (citing EX1002 ¶ 145). First, the Petition never identifies, let alone explains, what those “benefits” might be. *See* Pet. at 70; *see also Nuvasive*, 842 F.3d at 1384 (motivation to combine requires “explain[ing] the *reason why* a PHOSITA would have been motivated to modify” a reference). And Dr. Lee’s initial expert declaration may be disregarded because he offers nothing beyond reciting verbatim the Petition’s conclusory assertion of “the benefits associated with that method.” *Compare* EX1002 ¶ 145 *with* Pet. at 70; *Xerox Corp. v. Bytemark, Inc.*, IPR2022-00624, 2022 WL 3648989, at \*6 (P.T.A.B. Aug. 24, 2022) (precedential) (“verbatim” declaration testimony is “entitled to little weight”); *One World Techs., Inc. v. Chevron (HK) Ltd.*, PGR2020-00059, 2020 WL 7222691, at \*16 (P.T.A.B. Dec. 7, 2020) (expert testimony that “merely parrots the words in the Petition... is entitled to little or no weight”); 37 C.F.R. § 42.65(a).

However, even if the Petition had proffered some specific “benefits” to combining Lee and Watanabe, that would still be inadequate. The Federal Circuit explained: “Given the complexity involved in integrated circuit fabrication... testimony that PECVD had certain benefits and that [two references] are in the same technological field was insufficient to meet Petitioners’ burden.” *Samsung Elecs.*, 925 F.3d at 1381; *see also* EX2029 ¶¶ 64-69.

With no advantage presented to combine Lee and Watanabe, simply offering two “alternative method[s]” from the asserted art falls far short of Micron’s burden to show a *motivation* to combine them. Pet. at 70. “It is not enough to assert that the prior art provides two options and that it would have been predictable to implement either.” *Palo Alto Networks*, 2017 WL 1040259, at \*24 (finding no motivation to combine). The Petition has no answer to the truism: if it ain’t broke, don’t fix it. *See, e.g., Nuvasive*, 842 F.3d at 1384-85 (no motivation to combine established with no articulated reason to depart from primary reference to obtain “additional information”); *Winner Int’l Royalty Corp. v. Wang*, 202 F.3d 1340, 1349 (Fed. Cir. 2000) (“no motivation to combine” because “there was no apparent disadvantage to the dead-bolt mechanism of Johnson”).

As Micron’s own expert recognized, Lee itself expresses a preference for “monolithic” structures:

One method of improving device density is to arrange the devices in a *monolithic* three dimensional array of charge storage devices comprising a plurality of device levels. The term “monolithic” means that layers of each level of the array were directly deposited on the layers of each underlying level of the array. *In contrast*, two dimensional arrays may be formed separately and then packaged together to form a non-monolithic memory device.

EX1007 at 11:25-32 (emphases added); EX2028 at 59:12-61:2 (Dr. Lee: Lee’s passage is distinguishing “sequential deposition method” from “stacking method”). Although acknowledging that arrays may be formed separately, Lee reserves its recommendation for improving device density to “monolithic” structures. *See* EX1007 at 11:25-32. For example, when Lee describes Figure 35, it specifically refers to the structure as “a three dimensional *monolithic* array.” *Id.* at 12:17-23 (emphasis added).

With no alleged benefit to the combination, Micron baldly asserts that one of skill “would have been motivated to modify Lee in view of Watanabe” because they “are from the same field” and both teach “techniques for manufacturing semiconductor memory devices.” Pet. at 69-70. The Petition provides no answer for why one of skill would have looked more than a decade before Lee to select Watanabe’s facially unworkable “stacking method.” *See id.*; EX2029 ¶¶ 70-81; *supra* § VI.A.1-2. And Lee and Watanabe used incompatible data flows which were

not readily combinable. EX2029 ¶¶ 89-98. Simply being in the same field is insufficient. *See, e.g., Samsung Elecs.*, 925 F.3d at 1381 (asserting prior art “in the same technological field was insufficient to meet Petitioners’ burden” to show obviousness); *Markforged Inc. v. Continuous Composites, Inc.*, IPR2022-00679, 2023 WL 6534357, at \*14 (P.T.A.B. Sept. 26, 2023) (“Petitioner again asserts that the references are in the same field of additive manufacturing of three-dimensional objects. Even if true, that is not enough to establish” motivation to combine. (internal citation omitted)).

Finally, beyond these generic statements, the Petition asserts that one of skill “seeking to increase the integration density of semiconductor memory devices” would have combined these references. Pet. at 69-70 (citing EX1002 ¶ 144 (same)). That generic goal also cannot meet Micron’s heavy burden to establish a motivation to combine these specific disclosures. *Samsung Elecs.*, 925 F.3d at 1382. Watanabe’s planar capacitor design was among the least dense memory cell designs, particularly compared to denser vertical and trench capacitor designs for DRAM. EX2029 ¶¶ 82-88; *see also* EX2034 at 41-44 & Figs. 2.12-2.14 (showing tall and trench capacitors in conventional DRAMs). Even Watanabe acknowledges that its design required the word and data lines have a “2  $\mu\text{m}$ ” pitch horizontally and vertically, meaning the memory cells are placed a spacious 2000 nm apart. EX1005 at 4:31-41. This rationale also fails to pass muster.

**2. Micron Fails To Provide Any Evidence That The Lee/Watanabe Combination Had A Reasonable Chance Of Success**

Given Dr. Lee’s testimony that Watanabe’s stacking method would ruin the embedded transistors, EX2028 at 123:13-124:7, Micron’s own evidence shows not only that a skilled artisan would not expect combining Lee with Watanabe to work, but also that it in fact would fail.

Additionally, Micron failed to offer any evidence of a likelihood of success. In complex “integrated-circuit technology,” a petitioner should show “specific evidence that a person of ordinary skill in the art would have reasonably expected success in combining” the references. *Samsung Elecs.*, 925 F.3d at 1382-83. Yet the Petition offers one conclusory sentence saying combining Lee and Watanabe would have had “no change in their respective functions because both of these references purport to solve the same problems in similar and predictable ways.” Pet. at 71 (citing EX1002 ¶ 146 (Dr. Lee: ditto they have “vertical transistors and pillar structures”)). That is insufficient to meet Micron’s burden here.

As explained, Watanabe’s stacking technique is a nonstarter on its face. And even Micron’s expert admitted that Watanabe’s “high-temperature bonding” process at 900-1000°C would ruin transistors in lower levels of the stack, and a skilled artisan in 2004 would have known that. *Supra* § VI.A.1; EX2028 at 123:13-124:7, 126:8-20. Not only would one of skill have had no reason to apply Watanabe’s

stacking technique to Lee, but the Petition also never explains how one of skill would have had any reasonable expectation of success in making the combination that both risked over-baking the transistors and misaligning (and not electrically connecting) the layers resulting in an inoperable device. *See supra* § VI.A.1-2; EX2029 ¶¶ 70-81.

The Petition’s failure to meet its burden to show a reasonable expectation of success presents yet another, independent reason why the claims should be confirmed over Grounds 5-6.

**C. The Petition Does Not Establish Unpatentability of Claims 14-15**

**1. Ground 5’s Cross-Referencing Does Not Meet Micron’s Burden (Claims 14-15)**

The entirety of Ground 5 alleging Lee and Watanabe satisfy Claims 14-15 consists of two assertions: “[a]s discussed above, Lee discloses dependent Claims 14 and 15” and “Watanabe in view of Endoh discloses dependent Claims 14-15.” Pet. at 73 (citing Ground 3 at § VII.C.6-VII.C.7 and also “see also” cite to Ground 2, § VII.B.2-VII.B.3). Dr. Lee’s declaration says the same and adds nothing to the conversation. *Compare* EX1002 ¶ 150 *with* Pet. 73; *Xerox*, 2022 WL 3648989, at \*6; *One World*, 2020 WL 7222691, at \*16.

Cross-referencing here does not meet Micron’s statutory requirement to establish unpatentability “with particularity.” 35 U.S.C. § 312(a)(3). The ground is unparseable and nonsensical, referencing the Ground 2 Endoh combination when

Ground 5 does not even rely on Endoh. Pet. at 4; *see, e.g., C.R. Bard, Inc. v. Medline Indus., Inc.*, IPR2019-00208, 2020 WL 2974096, at \*14 (P.T.A.B. June 3, 2020) (“Petitioner’s cross-reference to other grounds [involving other secondary references] is unpersuasive in the context of the challenge based solely upon Solazzo and Nursing Standard.”). Saying that reference A alone (Lee), and also B+C (Watanabe+Endoh), establish obviousness based on A+B (Lee+Watanabe) logically fails because they are not the same combination, and Micron’s analysis-free allegation for Claims 14-15 falls far short of meeting its burden. For example, there is no explanation for how the embodiment resulting from the combination of Lee and Watanabe would satisfy Claims 14-15. *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016) (burden of demonstrating obviousness not met by conclusory argument that “the same analysis” for one combination of references applies to a different combination of references); *see also* EX2029 ¶¶ 99-100.

**2. The Petition Establishes No Motivation To Combine Lee’s Alternative Embodiments In Figures 7 And 83A (Claim 15)**

Even if the Board finds Ground 5’s cross-referencing adequate, the Petition would still fall short for Claim 15 for the same reason as the Ground 3 challenge to Claim 15. Ground 3 attempts to combine alternative embodiments in Lee to show unpatentability of Claim 15, without any explanation why or how one of skill would

have done so. Ground 3, and by incorporation Ground 5 (to the extent it relies solely on Lee), both fail for this reason.

For limitation 13[c], Ground 3 relies on Lee’s Figure 83A “flash memory array in a rail stack configuration,” EX1007 at 55:26-28, which shows a floating gate 5247. *Id.* at 56:8-10 (“[I]n the example of FIGS. 83A and B, the charge storage region 5241 comprises a polysilicon floating gate 5247....”); Pet. at 51; *see also* EX2028 at 53:7-13 (Dr. Lee testifying that in his opinion Lee’s Figure 83A “discloses a stackable add-on layer being bonded to the dielectric layer”). The same ground also cites Lee’s Figure 7 for Claim 15, which illustrates an embodiment of a “pillar memory... having a charge trapping dielectric.” EX1007 at 8:40-42; Pet. at 58-59. Micron provides no explanation why one of skill would have combined the alternative pillar and rail stack embodiments of Figures 7 and 83A, with their incompatible charge trap and floating gate, nor does it explain how combining mutually exclusive technologies would have been possible. Pet. at 58-59.

At institution, the Board found that Micron asserted for Claim 15 that “each add-on layer in Figures 7 and 35 is bonded to the dielectric layer based on Lee’s description of a monolithic array, the disclosures of Figure 35, and the disclosures of Figure 83A.” I.D. at 26. But the Petition never asserted this new theory, *see* Pet. at 50-52, and the Board “cannot rewrite the Petition to incorporate that analysis.” *Ebates Performance Mktg., Inc. v. Int’l Bus. Machs. Corp.*, IPR2022-00133, 2023

WL 5065209, at \*22 n.14 (P.T.A.B. May 24, 2023). Indeed, the Petition provides no explanation for the relationship between Figures 35 and 83A and Lee’s description of a monolithic array. *See* Pet. at 50-52. The Board is not free to supply that missing rationale. *Magnum Oil Tools*, 829 F.3d at 1381 (Board is not “free to adopt arguments on behalf of petitioners that could have been, but were not, raised by the petitioner during an IPR”).

Because the Petition never showed “how or why the skilled artisan” would have combined “distinct, mutually exclusive” embodiments, the Petition fails to meet its burden as to dependent Claim 15 in Grounds 3 and 5. *WhiteWater West Indus., Ltd. v. Am. Wave Machs., Inc.*, IPR2022-01035, 2022 WL 17071813, at \*7 (P.T.A.B. Nov. 17, 2022); *Markforged*, 2023 WL 6534357, at \*5-6 (combining alternative embodiments requires a motivation to combine).

**D. The Petition Fails To Establish Obviousness Based On Lee, Watanabe, And Endoh (Claims 16-17)**

Because Claims 16-17 in Ground 6 depend from Claim 13 challenged in Ground 5, the Petition does not meet its burden in Ground 6 for the same reasons explained for Ground 5. *Supra* § VI.A-B. Ground 6 additionally fails to show obviousness because: (1) its inadequate cross-referencing cannot show unpatentability of dependent Claims 16-17, and (2) it provides no motivation to

combine Lee and Endoh’s incompatible architectures or a reasonable expectation of success.

**1. Micron’s Cross-Referencing Does Not Meet Its Burden With Particularity**

The Petition again cuts corners on Claims 16 and 17 and cannot meet its burden to show unpatentability. The Petition’s sum total analysis for Ground 6 is two paragraphs. Pet. at 73-74. Ground 6 says that “Lee in view of Watanabe and Endoh discloses dependent Claims 16 and 17” because “Lee in view of Endoh” does, and then cross-references to Ground 4. Pet. at 73 (citing Ground 4 at § VII.D.2-VII.D.3 and “see also” cite to Ground 2 § VII.B.4-VII.B.5). Dr. Lee’s declaration again follows suit and adds nothing here. *Compare* EX1002 ¶¶ 151-52 *with* Pet. at 73-74; *Xerox*, 2022 WL 3648989, at \*6; *One World*, 2020 WL 7222691, at \*16.

Again, this falls far short of meeting Micron’s burden “with particularity.” 35 U.S.C. § 312(a)(3). Obviousness based on A+C (Lee+Endoh) is a different combination than A+B+C (Lee+Watanabe+Endoh), *Magnum Oil Tools*, 829 F.3d at 1380, and the Petition never accounts for the addition of Watanabe or explains how this specific combination would be accomplished, let alone with a reasonable expectation of success, *Microchip Tech. Inc. v. HD Silicon Sols. LLC*, IPR2021-00872, 2021 WL 6339555, at \*7 (P.T.A.B. Dec. 15, 2021) (petitioner did not “provide persuasive explanation as to how either reference would be modified to

accommodate the distinct architecture of the other reference... in a combination”);  
EX2029 ¶¶ 101-105.

**2. The Petition Provides No Showing How The Distinct Architectures Of Lee, Endoh, And Watanabe Would Be Combined, Let Alone Any Motivation To Combine Them**

Ground 6’s two-paragraph discussion fails to meet its burden to show a motivation to combine Lee, Watanabe, and Endoh. *See* Pet. at 73-74. Instead, it cross-references to its argument about combining Lee and Endoh in Ground 4. *See* Pet. at 73 (“Lee in view of Watanabe and Endoh discloses dependent Claims 16 and 17” because “Lee in view of Endoh” does, citing Ground 4 at § VII.D.2-VII.D.3); *see also* EX2029 ¶¶ 106-112. Because Micron never meets its burden to show one of skill would have been motivated to combine Lee and Endoh’s fundamentally incompatible memory architectures, Grounds 4 and 6 fail to show unpatentability.

Ground 4 gives short shrift in asserting one of skill would purportedly combine Lee and Endoh. Micron acknowledges Lee’s Figure 12B uses a NOR architecture. Pet. at 62 (citing EX1007 at 40:11-13 and asserting Lee’s “memory arrangement is known as the NOR Virtual Ground (NVG) Array”); EX2028 at 75:9-76:14 (Dr. Lee: acknowledging Fig. 12B “is a NOR architecture array”). But Endoh’s Figure 65 showed a “NAND architecture and a serial connection.” Pet. at 63. Micron magically asserts that because “memory cell structures in NAND were

(and still are today) similar to those in NOR architecture... a POSITA would have had a reasonable expectation of success in modifying Lee to use a NAND serial connection.” *Id.* at 65.

Micron’s approach of waving a magic wand and hoping one of skill can make it so falls flat when even its own expert could not make it happen. When asked how this alleged transformation of Lee’s Figure 12B into a NAND architecture could be accomplished, Dr. Lee had no answer. EX2028 at 94:6-98:11 (“I haven’t thought about it and I would like not to answer your questions without clearly thinking about all of the modification.”). Eventually, one change Dr. Lee offered was to “simply remove this oxide in between those two metals,” *id.* at 95:3-5, which he then circled with his blue pen in the figure below.

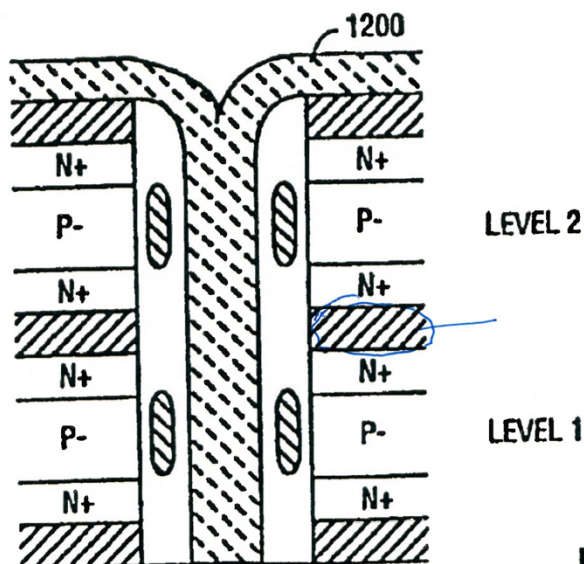


**FIG. 12B**

EX2026; EX2028 at 96:6-97:1. But that does not work: Dr. Lee’s “oxide” is actually a conductor because Lee uses hash marks to represent conductors. *E.g.*, EX1007 at 14:61-63 (referencing conductor 112 in Figure 1A), 15:33-37 (referencing “highly conductive material” forming 204 and 210 in Figure 2); EX2029 ¶¶ 131-37.

When Dr. Lee was asked in the same figure to identify the “insulator” in the silicon on insulator (SOI) pillar, he circled and labeled the following, identifying the same structure:

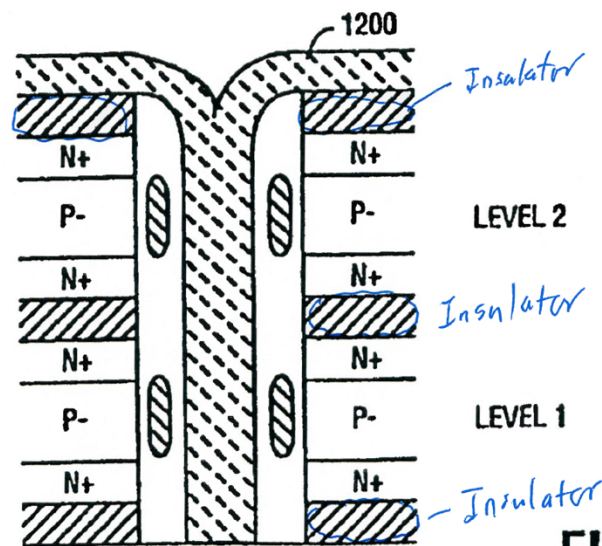


**FIG. 12B**

EX2025; EX2028 at 81:3-82:6. Not only could Dr. Lee not explain how to convert Figure 12B into a NAND serial connection, something he testified would have been obvious to a skilled artisan in 2004, EX1002 ¶¶ 132-34, but he himself did not understand Figure 12B. Nor did Dr. Lee recognize that if his “oxide” and “Insulator” actually been an oxide or insulator, the transistors in Figure 12B would have been

nonfunctional because they would have had no source or drain contacts. EX2029 ¶¶ 136-37. If Dr. Lee can't come up with a solution, he and Micron can hardly say one of skill would have been motivated to modify Lee into a NAND configuration in Ground 6, let alone with any reasonable expectation of success.

As even Micron's cited references acknowledge, nonvolatile NAND and NOR memory devices use distinctly different architectures with incompatible data flows, bit lines, sensing amplifiers, read and write protocols, and control circuitry. EX2029 ¶¶ 138-141; *see also* EX1012 at 1:29-63; EX2028 at 107:2-109:16 ("Q. I'm just asking whether it would have to change to go from NOR to NAND. A. Yeah, it does.").

Just like Dr. Lee, the Petition has no answer for how one of skill would combine Lee's NOR architecture with Endoh's NAND architecture, and supplies no motivation to do so with any reasonable expectation of success. *See* Pet. at 61-65, 73-74; EX2029 ¶¶ 128-143. Hinting that one of skill would replace Lee's parallel connections with a "serial connection" does not show motivation. *See, e.g., Hilti, Inc. v. Milwaukee Elec. Tool Corp.*, IPR2015-01166, Paper 81 at 18 (P.T.A.B. Nov. 14, 2016) ("Petitioner does not provide adequate specific reasoning as to why one of ordinary skill in the art would have been led to modify Takano to connect cells in parallel when Takano clearly discloses a series connection."). Micron cites Lee's passage at column 40, lines 13-15, *see* Pet. at 65, but that passage stated: "If desired,

the memory array may also be arranged in non volatile flash memory architectures other than VGA, such as NOR-type memory or Dual String NOR (DuSNOR) memory, for example.” EX1007 at 40:13-16. It did not propose using NAND architecture. EX2029 ¶ 142.

Because memory cell logic design, layout, and architecture are intimately intertwined, modification of the memory cells or design routinely results in an overhaul of the layout and chip architecture. *Id.* ¶¶ 138-141. Here, Micron’s proposed combination is not a small tweak—but would require building an entirely new chip from the ground up. *Id.* ¶¶ 141, 143.

Micron offers no explanation why a skilled artisan seeking a NAND architecture would start with Lee’s NOR architecture. Relying on the Tran reference (EX1011), Micron asserts that it would have been obvious to use a NAND architecture “because an entire NAND cell string uses only ‘one-half’ of a bit line contact and ‘one-half’ of a source line contact, which further increases the integration density of the memory design.” Pet. at 63 (quoting EX1011 at 5:12-25). But Micron does not explain why one of skill desiring NAND based on Tran’s recommendation would start with Lee (a NOR design). *See, e.g., Shire LLC v. Amneal Pharms.*, 802 F.3d 1301, 1308 (Fed. Cir. 2015) (affirming nonobviousness: defendants failed “to show a reason why one of skill in the art would decide to start with example 24 and remove the protecting group. They have shown no such

motivation.”). In fact, these are fundamentally different technologies with completely different architectures. EX2029 ¶¶ 129-141.

By purportedly switching out Lee’s NOR configuration with a NAND architecture, Micron’s vague proposal is not obvious but a wish list for a fundamentally different chip. *See* Pet. at 61-65. To begin considering these changes, one of skill would confront a cascading set of modifications to the entire memory device, including:

- redesigning memory cell pillars;
- replacing control gate structures to provide separate control gate signal for each memory cell in the stack;
- creating new routing paths for each of those control gates;
- redoing the bit lines;
- replacing the command interface for NAND;
- redesigning the control logic and command sequencing for reading, programming, and erasing the memory;
- redesigning sense amplifiers;
- redesigning address decoders; and
- redesigning voltage generators.

EX2029 ¶¶ 138-141, 143.

One of skill would have had no reasonable expectation of success carrying out Micron’s proposal, much less a motivation to combine fundamentally different memory architectures. *See* Pet. at 61-65, 73-74; *MobileMedia Ideas*, 780 F.3d at 1167-68 (one of skill “would not have been motivated to combine... references to arrive at the claimed invention” where doing so “would be beyond the technical ability of a skilled artisan”); *see also Microchip Tech.*, 2021 WL 6339555, at \*7 (petitioner did not “provide persuasive explanation as to how either reference would be modified to accommodate the distinct architecture of the other reference... in a combination”). Micron provides no evidence or explanation as to what the resulting conversion would look like, let alone how the resulting structure would satisfy the claim limitations. *See, e.g., Tri-Arc LLC v. Safe Rack LLC*, IPR2020-01566, 2021 WL 1156658, at \*11 (P.T.A.B. Mar. 25, 2021) (“we are not persuaded that the resulting structure would satisfy the requirement of” the claim). Dr. Lee admitted at deposition that he had not even “thought about” how to do it. EX2028 at 97:3-98:11 (Dr. Lee: “I have not thought about” the “change[s] you would make to Figure 12B to convert it to a serial NAND architecture.”).

Claims 16-17 should be confirmed patentable over Ground 6.

**VII. THE PETITION DOES NOT MEET ITS BURDEN FOR GROUNDS  
3-4 BASED ON LEE**

The Petition also has not met its burden for Grounds 3-4 based on the Lee patent. Neither ground survived the first stage of this trial. Even Micron’s expert Dr. Lee acknowledges that Lee does not satisfy Claim 13 (and thus its dependents) based on the claim construction he advocates.<sup>1</sup> EX2028 at 18:21-20:1. Further, Micron never acknowledges, let alone shows, a motivation to combine Lee’s pillar and rail stack embodiments in Figures 1A and 83A. *See, e.g., In re Stepan Co.*, 868 F.3d 1342, 1346 n.1 (Fed. Cir. 2017). The Petition suffers from the same defect in attempting to combine Figures 7 and 83A for Claim 15. Claims 16-17 should also be confirmed because of Dr. Lee’s admissions and drawings at his deposition that Lee’s Figure 12B did not include the claimed SOI pillar with “at least two nonvolatile memory cells.” Finally, Ground 4 never establishes one of skill would have been motivated to combine Lee’s NOR configuration with Endoh’s serial

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<sup>1</sup> BeSang does not concur with, nor is it relying upon, the proposed claim construction put forth by Micron and its expert. *Supra* § IV.A. It is Micron’s burden to prove the invalidity of the Challenged Claims applying its claim construction. *Maxlite*, 2020 WL 5803082, at \*2. The Board can confirm the patentability of the Challenged Claims based on the independent reasons set forth herein.

NAND architecture for Claims 16-17. The Board should confirm patentability for any of these reasons.

**A. The Petition Fails To Establish A Motivation To Combine Lee’s Different Embodiments (All Claims 13-17)**

**1. No Motivation To Combine For Claim 13 And Its Dependents**

At institution, the Board noted that “Petitioner points to Lee’s description of a monolithic array, Lee’s disclosures relating to Figure 35, and Lee’s disclosures relating to Figure 83A” to show obviousness of Claim 13. I.D. at 22; *see also id.* at 21-23. That is exactly right and Micron has not met its burden to show a motivation to combine these disparate embodiments. *Magnum Oil Tools*, 829 F.3d at 1375; *Stepan*, 868 F.3d at 1346 n.1. Below is how the Petition mapped Lee’s embodiments to Claim 13:

| <b>Claim 13 Limitation</b> | <b>Embodiments</b> |
|----------------------------|--------------------|
| 13[a]                      | Figure 35          |
| 13[b]                      | Figures 1A and 35  |
| 13[c]                      | Figures 35 and 83A |
| 13[d]                      | Figure 1A          |

Pet. at 47-54.

Lee’s Figure 1A is a “pillar memory device,” EX1007 at 14:11-13, and Figure 83A shows a “flash memory array in a rail stack configuration,” *id.* at 55:26-28. Lee describes a variety of memory cell embodiments, *id.* at 12:53-57,

and describes its “pillar” and “rail stack” devices as alternative embodiments. *Id.* at 55:8-10 (“The TFT EEPROMs may be arranged in the pillar, self-aligned TFT *or* rail stack configurations of the previous embodiments.” (emphasis added)). Yet the Petition points to the Figure 1A pillar for limitation 13[b], Pet. at 48-50, and then switches to the Figure 83A rail stack for the next limitation 13[c], *id.* at 50-52.

The Petition never acknowledges its sleight of hand, let alone establishes a motivation to combine these mutually exclusive embodiments with any reasonable expectation of success. *See* Pet. at 46-54. Nor does the Petition explain how they would be combined, much less how the resulting combination would satisfy all of Claim 13’s requirements. *See id.* The Petition’s discussion reads like a word search in the asserted art and reeks of hindsight. *Hewlett Packard v. Intellectual Ventures II*, IPR2022-00115, 2022 WL 946244, at \*6 (P.T.A.B. Mar. 29, 2022) (“Petitioner’s combination of select features from Harari’s different embodiments to arrive at the invention of claim 1 is fraught with hindsight bias.”); *ATD Corp.*, 159 F.3d at 546 (rejecting “hindsight combination of components selectively culled from the prior art”).

Such mixing and matching embodiments does not meet Micron’s burden. *See, e.g., WhiteWater*, 2022 WL 17071813, at \*7 (“Petitioner does not acknowledge that it is relying on different embodiments for these claim limitations, much less explain how or why one of ordinary skill in the art would have combined them to achieve

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the claimed invention.”); *Lumenis Be Ltd. v. BTL Healthcare Techs. A.S.*, IPR2021-01280, 2022 WL 946534, at \*8 (P.T.A.B. Mar. 9, 2022) (“Absent persuasive evidence explaining how and why the embodiment of Figure 9B would be combined with the embodiment of Figure 35 with a reasonable expectation of success,” petitioner did not meet burden.); *Unified Patents Inc. v. GE Video Compression, LLC*, IPR2019-00726, 2019 WL 3714386, at \*8 (P.T.A.B. Aug. 6, 2019). Nor does it satisfy Micron’s obligation to “set forth its contentions among the various embodiments with particularity.” *Nuance Commc’ns, Inc. v. MModal Servs. Ltd.*, IPR2019-00794, Paper 7 at 29-30 (P.T.A.B. Sept. 10, 2019); *see also* EX2029 ¶¶ 123-27.

On preliminary reply, Micron tried to paper over its error, claiming that “the Petition references Fig. 83A only to show what a POSITA would have understood about the formation of Figs. 1A and 35.” Paper 7 (“Pre-Reply”) at 6. But that theory was not presented in the Petition and cannot be considered now. *Netflix, Inc. v. DivX, LLC*, 84 F.4th 1371, 1377 (Fed. Cir. 2023) (“We have likewise reprimanded the Board for finding a claim unpatentable based on theories not presented in the petition.”); *SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1348, 1358 (2018) (“the petition [is] the centerpiece of the proceeding both before and after institution”).

This claim is also untrue. The Petition expressly relied on Lee’s Figure 83A to affirmatively show Claim 13’s requirement of a “stackable add-on layer being

bonded to the dielectric layer.” *See* Pet. at 50-52. Reproducing Figure 83A, the Petition asserted that “a POSITA would have understood that ***the array [5230] is bonded to the planarized interlayer insulating layer 5231,***” both shown in Figure 83A. *Id.* at 52 (emphasis added); *see also* EX2028 at 53:7-13 (Dr. Lee testifying that in his opinion Figure 83A “discloses a stackable add-on layer being bonded to the dielectric layer”). Micron cannot disavow its flawed approach now, and the Board should reconsider pages 51-52 of the Petition before accepting Micron’s re-characterization of its Petition at trial. *See* I.D. at 25 (citing Pet. at 50, 52).

For this reason, the Board should reject Grounds 3-4.

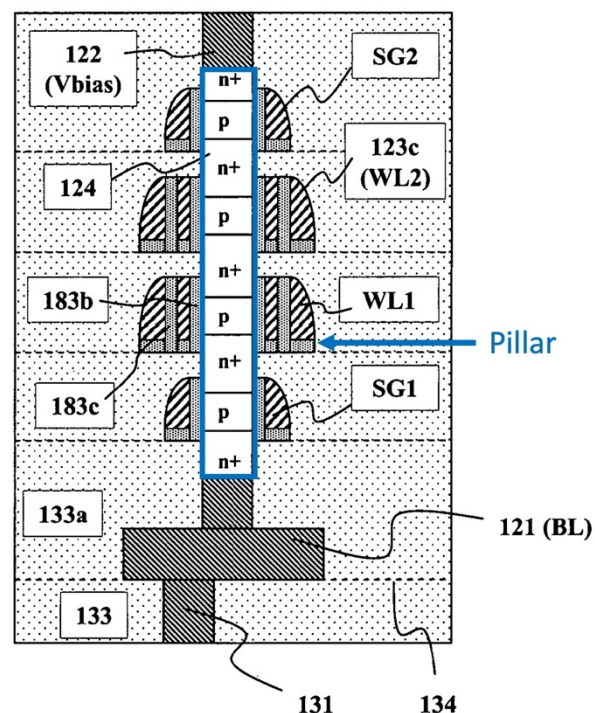
## **2. No Motivation To Combine For Claim 15**

Again, Micron attempts asserting obviousness of Claim 15 based on the embodiments in Figures 7 and 83A, without any explanation why or how one of skill would have done so. *See* Pet. at 51, 58-59. As explained for Ground 5, its Ground 3 challenge to Claim 15 cannot prevail. *See supra* § VI.C.2.

**B. Dr. Lee Conceded The Lee Patent Does Not Satisfy “Two Nonvolatile Memory Cells” (Claims 16-17)**

Dependent Claims 16-17 require “at least two nonvolatile memory cells are vertically oriented and serially connected together and formed with a first SOI pillar.” EX1001 at 12:45-47. For example, Figure 29 (annotated, right) shows two “vertical” transistor memory cells that are serially connected in the same pillar. EX1001 at 3:32-34, 9:59-64, Fig. 29; *see also id.* at Figs. 27-32; EX2029 ¶¶ 46-47.

Fig. 29



The Petition and Dr. Lee’s declaration asserted that Lee’s Figure 12B exclusively satisfies this requirement. Pet. at 61-62; EX1002 ¶ 132. But at deposition, Dr. Lee confirmed that Figure 12B actually does not. EX2028 at 76:15-79:19. Asked about his prior opinion, Dr. Lee used his blue pen to identify the Lee patent’s SOI pillars:

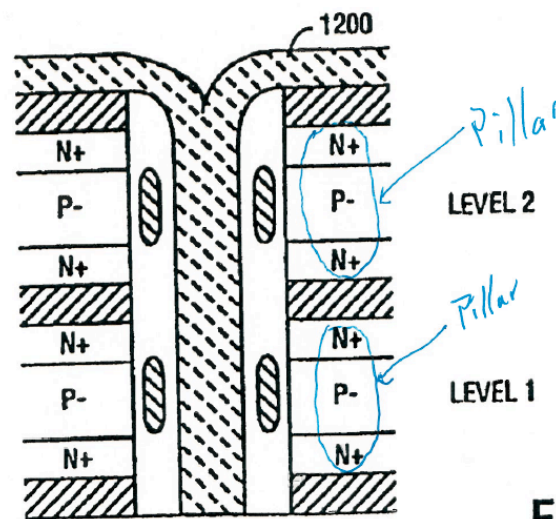


**FIG. 12B**

*Id.*; EX2024 (Dr. Lee’s annotations from original); *accord* EX2023. Each of his alleged SOI pillars included only a single npn memory cell. EX2024. He testified the “pillars in Figure 12B are just the n+, p-, n+ dope stack structures.” EX2028 at 79:15-19.

But Claims 16-17 require the pillar include “at least *two* nonvolatile memory cells.” EX1001 at 12:45-47 (emphasis added). Dr. Lee’s single-memory-cell pillars do not satisfy these two-memory-cell claims, and patentability of these claims should be confirmed for this additional reason.

**C. The Petition Fails To Show That It Would Have Been Obvious To Combine The Teachings Of Lee And Endoh (Claims 16-17)**

Ground 4 asserts that Claims 16-17 are obvious over Lee and Endoh. Pet. at 59-69. As already explained for the same argument Micron incorporated in Ground 6, one of skill would not have been motivated to modify Lee’s NOR chip

with Endoh’s serial NAND architecture, much less have had a reasonable expectation of success. *See supra* § VI.D.2; EX2029 ¶¶ 128-143.

## **VIII. THE PETITION DOES NOT MEET ITS BURDEN FOR GROUNDS 1-2 BASED ON WATANABE**

The Board correctly found that Micron failed to meet its burden in Grounds 1-2 based on Watanabe. I.D. at 13-17; *see also* POPR at 14-28.

The Petition failed to show a motivation to combine Watanabe’s volatile and nonvolatile memory embodiments (all Claims 13-17), that Watanabe teaches a non-volatile memory cell required by Claim 13[b] (all Claims 13-17), or that Watanabe satisfied the “SOI pillar” limitation (Claims 14-17). Trial has only further eroded Grounds 1-2. Dr. Lee’s testimony acknowledging thermal budgets further shows that Watanabe is not enabled and a skilled artisan would not have been motivated to use it for fear of over-baking the transistors. For any of these reasons, the Board should confirm patentability over these two grounds.

### **A. The Petition Fails To Establish A Motivation To Combine Watanabe’s Different Embodiments (All Claims 13-17)**

Micron failed to meet its burden that one of skill in the art would have combined Watanabe’s DRAM (Figs. 1, 2A, 5, 6) and EPROM (Fig. 7) embodiments. Pet. at 13-26; POPR at 14-19. At institution, the Board recognized how the Petition addressed the DRAM embodiments before “Petitioner abruptly switches to the

EPROM embodiment of Figure 7” and expressed its “concerns about the sufficiency of Petitioner’s challenge based on Watanabe.” I.D. at 15-16.

As explained, Micron relied on these disparate embodiments to satisfy different limitations in Claim 13, without acknowledging its sleight of hand or providing the required motivation to combine with a reasonable expectation of success. Pet. at 13-26; POPR at 14-19; Paper 8 (“Pre-SurReply”) at 3-5. Not only is Micron’s approach “fraught with hindsight bias,” *Hewlett Packard*, 2022 WL 946244, at \*6, it is plainly improper, *Stapan*, 868 F.3d at 1346 n.1; *WhiteWater*, 2022 WL 17071813, at \*7; *Lumenis*, 2022 WL 946534, at \*8; *Unified Patents*, 2019 WL 3714386, at \*8. The patentability of all Challenged Claims should be confirmed.

Micron’s attempt to remedy this issue on preliminary reply only underscores the deficiency of its Petition. Pre-Reply at 3-5. But it’s too late for Micron to fix its Petition now. Pre-SurReply at 3-5; *Intel Corp. v. Qualcomm, Inc.*, IPR2018-01154, 2021 WL 3553796, at \*2 (P.T.A.B. Aug. 11, 2021); *SAS Inst.*, 138 S. Ct. at 1358 (“the petition [is] the centerpiece of the proceeding both before and after institution”). Its belated reliance on Watanabe’s general statement that “[t]he memory cell of the present invention is applicable to any type of memory device i.e., a SRAM, PROM, or a DRAM,” Pre-Reply at 3-5 (citing EX1005 at 2:51-53), was never made in the Petition, *see* Pet. at 14-26.

Even if considered, it “lacks specificity and precision” and “falls short of describing why a person of ordinary skill in the art would have been motivated to combine such features,” much less how one would have done so to arrive at the claimed invention with a reasonable expectation of success. *Markforged*, 2023 WL 6534357, at \*6 (rejecting generic passage stating “various features” “may” be provided in a single embodiment as motivation to combine); Pre-SurReply at 3-4. Micron’s picking and choosing from Watanabe’s alternative embodiments and invocation of the ’702 Patent on preliminary reply shows its Petition is the product of impermissible hindsight. *Hewlett Packard*, 2022 WL 946244, at \*6 (“Petitioner’s combination of select features from Harari’s different embodiments to arrive at the invention of claim 1 is fraught with hindsight bias.”); *ATD Corp.*, 159 F.3d at 546; Pre-SurReply at 4-5.

Micron has not met its burden on Grounds 1-2.

**B. The Petition Fails To Establish That Watanabe Disclosed Or Rendered Obvious The “Nonvolatile” Limitation 13[b] (All Claims 13-17)**

All claims should be confirmed for a second reason: the Petition’s reliance on Watanabe’s DRAM embodiments fails to satisfy the “memory cells” limitation in 13[b]. POPR at 19-24; Pre-SurReply at 3-5. Claim 13 requires the claimed “memory cells” be “nonvolatile memory cells” as specified in limitation 13[d]. *Id.*; EX1001 at 12:29-34. Yet the Petition solely relies on Watanabe’s *volatile* DRAM

memory in Figures 1, 2A, 5, and 6 for limitation 13[b] as explained previously. *See* Pet. at 16-21. The Board correctly recognized “DRAM memory [is] depicted in Figures 2A, 5A, and 6.” I.D. at 15-16.

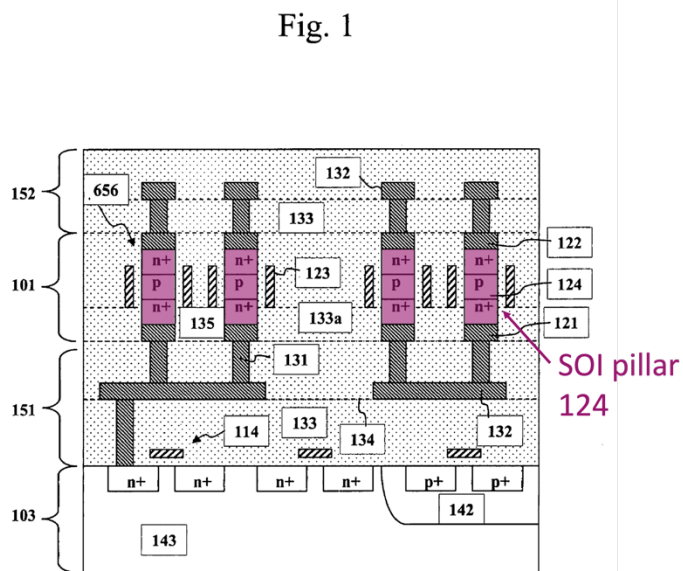
Micron did not seriously dispute any of this on preliminary reply, instead trying to undo its error by inaccurately asserting its “Petition relies only on Watanabe’s nonvolatile embodiment” for Grounds 1-2. Pre-Reply at 4-5; Pre-SurReply at 3-5. But Micron plainly did not, Pet. at 16-21, and again it’s too late to change theories now, *Netflix*, 84 F.4th at 1377 (“We have likewise reprimanded the Board for finding a claim unpatentable based on theories not presented in the petition.”); *SAS Inst.*, 138 S. Ct. at 1358. Even if it had relied on Watanabe’s Figure 7, Micron provided no explanation of how it would be combined with the volatile embodiments, let alone with any reasonable expectation of success. *Unified Patents*, 2019 WL 3714386, at \*8; *Oracle Am., Inc. v. Realtime Data LLC*, IPR2016-00375, Paper 8 at 11 (P.T.A.B. July 1, 2016); POPR at 22-24. The Board correctly recognized Watanabe’s general statement that its memory cell was “applicable,” did not “mean that every structure depicted in Figures 2A, 5, and 6 is applicable to ‘any type of memory device.’” I.D. at 15 (citing EX1005 at 2:51-55).

Patentability should be confirmed over Watanabe for this additional reason.

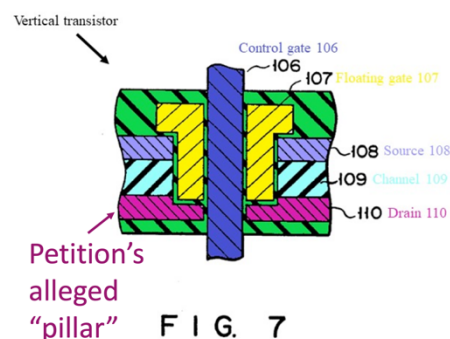
### C. Watanabe Is Missing An “SOI Pillar” (Claims 14-17)

Claims 14-17 should also be confirmed patentable over Ground 2 because the Petition fails to show that Watanabe taught or suggested the claimed “SOI pillar.” EX1001 at 12:35-52; POPR at 24-28; Pre-SurReply at 6-7. The Board correctly recognized that “Petitioner does not adequately demonstrate that Watanabe teaches or suggests a ‘pillar,’ as that term is used in the ’702 patent.” I.D. at 17. It noted that the Petition instead pointed to “doped, horizontal layers above insulator 49.” *Id.*

As previously explained, the Petition and Dr. Lee relied on Watanabe’s Figure 7 to assert that “a POSITA would have understood (or found it obvious) that Watanabe’s vertical transistor can be formed on a SOI pillar.” Pet. at 29 (citing EX1002 ¶ 90); POPR at 24-28. There is not much similarity between the ’702 Patent’s mauve pillar (left) and layer 110 in Watanabe (right):



’702 Patent, Fig. 1 (annotated)



Pet. at 29 (label added)

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Watanabe’s horizontal “layer” 110 can hardly be called a “pillar” as required by the claim or as shown in the ’702 Patent’s figures. EX2029 ¶¶ 92, 100; POPR at 24-26; Pre-SurReply at 6-7. Layer 110 certainly is not “a silicon-on-insulator structure taller than it is wide” under the correct construction of “SOI pillar” should the Board believe construction necessary to resolve Grounds 1-2. *Supra* § IV.B; EX2029 ¶¶ 58-63. Dr. Lee’s twin paragraph that “merely parrots the words in the Petition” does not help Micron show unpatentability. *One World*, 2020 WL 7222691, at \*16; *see also Xerox*, 2022 WL 3648989, at \*6; *compare* Pet. at 29-30 with EX1002 ¶ 90. Even if Micron had resorted to Endoh for this limitation, combining Endoh’s NAND architecture would be unworkable. EX2029 ¶¶ 147-48.

Again, Micron attempts to recast its Petition on preliminary reply by arguing for the first time that “Watanabe’s description of individual doped stack structures matches the ’702 Patent’s description of a pillar structure and... satisfies the ‘SOI pillar’ limitation.” Pre-Reply at 7 (citing EX1001 at 6:26-29). This pivot further shows Micron’s new argument was not in its Petition, *see* Pet. at 29-31, and it is too late to add it in now, *Netflix, Inc. v. Robocast, Inc.*, IPR2023-00081, 2023 WL 5162380, at \*14 n.8 (P.T.A.B. May 11, 2023) (rejecting “improper new argument” in preliminary reply under 37 C.F.R. § 42.23(b)); *MModal LLC v. Nuance Commc’ns, Inc.*, IPR2018-01355, 2020 WL 582392, at \*9 (P.T.A.B. Feb. 5, 2020).

Micron further scrambles to change course by citing the Petition’s statement that “Watanabe discloses a vertical structure with ‘at least two stack structures (two layers)... each consisting of layers 41 to 46,’” Pre-Reply at 7, but that sentence says nothing about whether those layers 41 to 46 are formed as a “pillar,” Pre-SurReply at 7. Indeed, the reference to them as “layers 41 to 46” in combination with Watanabe’s Figures 2A and 2B (depicting them as continuous layers) proves they are not. *Id.*; EX1005 at Figs. 2A, 2B.

The Board should confirm patentability over Ground 2.

**D. Watanabe’s Stacking Method Is Not Enabled (All Claims 13-17)**

Watanabe’s non-enabled high-temperature “stacking method” is yet another reason Grounds 1-2 cannot render BeSang’s 3D memory invention obvious. “To render a claim obvious, the prior art, taken as a whole, must enable a skilled artisan to make and use the claimed invention.” *Raytheon Techs. Corp. v. Gen. Elec. Co.*, 993 F.3d 1374, 1380 (Fed. Cir. 2021). “[I]f an obviousness case is based on a non-self-enabled reference, and no other prior art reference or evidence would have enabled a skilled artisan to make the claimed invention, then the invention cannot be said to have been obvious.” *Id.* at 1377.

Here, Watanabe’s stacking method that the Petition relies on to establish limitations 13[a]-[c], *see* Pet. at 14-15, 16-19, 21-23, included a “high-temperature bonding” step, *id.* at 72, where “the planar members thus formed are bonded” using

a “thermal process of 900° to 1000° C.” *Id.* at 22-23 (quoting EX1005 at 6:6-8). Dr. Lee confirmed that this “high-temperature bonding” shown in Watanabe’s Figure 6C would have exceeded the thermal budget of the transistors embedded in the substrate shown in Figure 6A, thus damaging the transistors. *See* EX2028 at 123:13-124:7 (“[T]he processing of the upper layer transistors cannot go above 650 degrees C, as described in [2027].”), 125:6-126:7; EX2027 at 715 (“[T]o avoid additional dopant diffusion or interfacial oxide growth on bottom transistor, LT (<650°C) top FETs process is mandatory.”); *see also supra* § VI.A.1; EX2029 ¶¶ 70-77, 144-46.

This evidence of record, including Dr. Lee’s own testimony, shows Watanabe’s stacking method is non-enabled. *See id.* Because Micron relies on Watanabe’s stacking method for Grounds 1-2, Watanabe’s “self-enablement (or lack thereof) is not only relevant to the enablement analysis, in this case it is dispositive” because Micron relies solely on Watanabe for Claim 13 in Grounds 1-2. *Raytheon*, 993 F.3d at 1382 (“GE does not contend that the ’751 patent’s turbofan engine is enabled by other prior art or evidence of record. Instead, GE relies solely on Knip’s disclosure.”).

Grounds 1-2 based on Watanabe also should be rejected for lack of enablement.

## **IX. CONCLUSION**

For each of the foregoing reasons, BeSang respectfully requests the Board confirm patentability of the Challenged Claims.

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Dated: February 16, 2024

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**CERTIFICATE OF COMPLIANCE**

Pursuant to 37 C.F.R. § 42.24(d), the undersigned certifies that foregoing **PATENT OWNER’S RESPONSE TO PETITION FOR *INTER PARTES* REVIEW**, exclusive of the parts exempted as provided in 37 C.F.R. § 42.24, contains 12,558 words and therefore complies with the type-volume limitations of 37 C.F.R. § 42.24.

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**CERTIFICATE OF SERVICE**

The undersigned certifies that pursuant to 37 C.F.R. § 42.6(e), a true copy of the foregoing **PATENT OWNER’S RESPONSE TO PETITION FOR *INTER PARTES* REVIEW** and **EXHIBITS 2021-2038** are being served electronically on February 16, 2024 to the following lead and backup counsel for Petitioners to the following email addresses:

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