

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
MICRON SEMICONDUCTOR PRODUCTS, INC., and
MICRON TECHNOLOGY TEXAS, LLC,
Petitioners,

v.

BESANG INC.,
Patent Owner.

Case No. IPR2023-00900
U.S. Patent No. 7,378,702

**DECLARATION OF STEVEN A. PRZYBYLSKI
IN SUPPORT OF PATENT OWNER'S RESPONSE
TO PETITION FOR *INTER PARTES* REVIEW**

I, Steven A. Przybylski, hereby declare as follows:

I. INTRODUCTION

1. I have prepared this Declaration in connection with Patent Owner's Response to the Petition for *Inter Partes* Review of U.S. Patent No. 7,378,702 ("the '702 Patent").

2. In the course of preparing this Declaration, I reviewed the '702 Patent, its prosecution file history, the asserted prior art, as well as the documents listed in Section III and/or discussed in this Declaration.

3. I have been retained by BeSang Inc. ("BeSang" or "Patent Owner") as an expert in the field of memory devices and semiconductor design. I am being compensated at my normal consulting rate for my time. My compensation is not dependent on and in no way affects the substance of my statements in this Declaration. I have no financial interest in BeSang, the '702 Patent or the owner of the '702 Patent.

II. BACKGROUND AND QUALIFICATIONS

4. Further details regarding my qualifications, including my employment and academic history, are set forth in my curriculum vitae. Ex. 2030.

5. I earned a Bachelor of Applied Science from the University of Toronto in 1980. I was enrolled in the Engineering Science program, completing a course of study combining the Electrical Engineer and Computer Science options.

6. I earned a Master of Science in Electrical Engineering degree and a Ph.D. in Electrical Engineering in 1982 and 1988 respectively, both from Stanford University.

7. I also earned a Masters of Business Administration from the Haas School of Business at the University of California at Berkeley in 2000.

8. I have extensive experience with memory semiconductor integrated circuits and the memory systems constructed of them. At Stanford, my dissertation was on the optimization of single- and multi-level cache hierarchies to maximize system-level performance. Also at Stanford, I was a member of the core team that architected, designed, built, and tested the seminal MIPS processor. I was responsible for the design of the instruction decode and control units as well as architecting the virtual memory support. I assembled and debugged the entire microprocessor design and oversaw its fabrication and testing. In 1984 and 1985, I took a leave of absence from Stanford to become a member of the founding team of MIPS Computer Systems, a startup in California that designed, built, and sold processors and computer systems. In 1989, after finishing my doctorate and brief post-doctorate at Stanford, I returned to MIPS Computer Systems. Throughout my two periods of employment at MIPS Computer Systems, I had a number of titles and worked on a variety of projects. Noteworthy were stints as processor architect, systems architect, hardware-software team liaison, and Chief Scientist of the High-

End Systems group. During the second period, I also served as a Consulting Assistant Professor in the Department of Electrical Engineering at Stanford. I designed and taught an advanced graduate level course on cache and memory system design.

9. In 1991, I left MIPS to become an independent consultant. In that capacity I have provided technical, strategic, marketing, and intellectual property services to a large number of clients both domestically and internationally.

10. The technical consulting I performed was principally related to advancements in semiconductor memories and their application in systems. Specifically with respect to non-volatile memories and Flash memories in particular, I advised companies on a variety of memory types and on trends in NAND and NOR Flash memories and the processes used in their manufacture. In the 2000's, in the time period relevant to the present matter, I helped develop a new NAND Flash architecture and separately a universal memory interface that was optimized for use in heterogeneous memory systems and that was equally applicable to DRAMs and to NAND Flash devices.

11. I am a member of both the Institute of Electrical and Electronics Engineers (IEEE) and the Association of Computing Machinery (ACM). In addition, in 1997 I became a registered patent agent. I am listed as the inventor on 11 domestic patents and their foreign counterparts. The subject matters include memory devices,

memory subsystems, networks, error detection and correction codes, processors and cache memories. Between 1994 and approximately 2000, I was a leading independent analyst following, writing, and teaching about both the technical and business aspects of the DRAM industry. Overall, I have written three books and over 25 articles in the areas of memory, processors, and computer systems. In particular, I wrote and revised an 850-page book entitled “New DRAM Technologies: A Comprehensive Analysis of the New Architectures.” I have presented many lectures, classes and seminars on semiconductor memories and their memory systems, processors and computer systems. I have presented full and half-day seminars on discrete and embedded DRAMs to over 2,500 engineers, marketers, managers, and financial analysts.

III. MATERIALS CONSIDERED

12. I have reviewed the '702 Patent (Ex. 1001) and its file history (Ex. 1004). Additionally, and in addition to any other documents cited or referenced herein, I have reviewed the following materials in preparing this Declaration:

- a. Micron’s Petition for Inter Partes Review (“Petition”) (Paper 1);
- b. Decision Granting Institution of Inter Partes Review (“Institution Decision”) (Paper 9);
- c. Intel’s Petition for *Inter Partes* Review, *Intel Corp. v. BeSang Inc.*, IPR2023-00091, Paper 2 (June 2, 2023) (“Intel Petition”);

- d. Intel’s Exhibit 1003 (Declaration of Dr. Carl Sechen), *Intel Corp. v. BeSang Inc.*, IPR2023-00091 (June 2, 2023);
- e. Declaration of Dr. Jack C. Lee (Ex. 1002);
- f. U.S. Patent No. 5,091,762 (“Watanabe”) (Ex. 1005);
- g. U.S. Patent Application Pub. No. US2002/0154556 (“Endoh”) (Ex. 1006);
- h. U.S. Patent No. 6,881,994 (“Lee”) (Ex. 1007);
- i. G. Groeseneken et al., Basics of Nonvolatile Semiconductor Memory Devices, in *Nonvolatile Semiconductor Memory Technology: A Comprehensive Guide to Understanding and Using NVSM Devices* (William D. Brown & Joe Brewer eds., 1997) (Ex. 1009);
- j. U.S. Patent No. 6,982,905 (“Nguyen”) (Ex. 1012);
- k. Tetsuo Endoh et al., Novel Ultrahigh-Density Flash memory with A Stacked-Surrounding Gate Transistor (S-SGT) Structured Cell, 50 *IEEE Transactions on Electron Devices* 945 (2003) (Ex. 1022);
- l. Hiroshi Sakuraba et al., New Three-Dimensional High-Density Stacked-Surrounding Gate Transistor (S-SGT) Flash Memory Architecture Using Self-Aligned Interconnection Fabrication Technology Without Photolithography Process for Tera-Bits and Beyond, 43 *Japanese J. Applied Physics* 2217 (2004) (Ex. 1030);

- m. U.S. Patent No. 6,881,994, Fig. 12B (annotated by Dr. Jack C. Lee) (Exs. 2025-2026);
- n. Perrine Batude et al., 3-D Sequential Integration: A Key Enabling Technology for Heterogeneous Co-Integration of New Function With CMOS, IEEE Journal on Emerging and Selected Topics in Circuits and Systems, Vol. 2, No. 4 (Dec. 2012) (Ex. 2027);
- o. Transcript of February 6, 2024 Deposition of Dr. Jack C. Lee (Ex. 2028);
- p. Webster's New Universal Unabridged Dictionary (Barnes & Noble Publ'g 2003) (excerpt) (Ex. 2031);
- q. Random House Webster's College Dictionary (2d ed. 1997) (excerpt) (Ex. 2032);
- r. Gary S. May, Ph.D. & Costas J. Spanos, Ph.D., Fundamentals of Semiconductor Manufacturing and Process Control (2006) (Ex. 2033);
- s. Brent Keeth et al., DRAM Circuit Design Fundamental and High-Speed Topics (IEEE Press Editorial Board eds., 2008) (Ex. 2034);
- t. Brent Keeth & R. Jacob Baker, DRAM Circuit Design: A Tutorial (Stuart K. Tewksbury & Joe E. Brewer eds., 2001) (Ex. 2035);
- u. Kiyoo Itoh, VLSI Memory Chip Design (Kiyoo Itoh & Takayasu Sakurai eds., 1st ed. 2001) (Ex. 2036); and

v. Interconnect, International Technology Roadmap for Semiconductors,
Semiconductor Industry Ass’n (2007),
[https://www.semiconductors.org/wp-content/uploads/2018/08/
2007Interconnect.pdf](https://www.semiconductors.org/wp-content/uploads/2018/08/2007Interconnect.pdf) (Ex. 2037).

IV. SUMMARY OF ASSERTED GROUNDS

13. The following table enumerates the Grounds found in Micron’s Petition and claims and references referred to accordingly.

Ground	Type	Claims	References
1	35 U.S.C. § 103	13	Watanabe
2	35 U.S.C. § 103	14-17	Watanabe, Endoh
3	35 U.S.C. § 103	13-15	Lee
4	35 U.S.C. § 103	16-17	Lee, Endoh
5	35 U.S.C. § 103	13-15	Lee, Watanabe
6	35 U.S.C. § 103	16-17	Lee, Watanabe, Endoh

V. RELEVANT LAW

14. I am not an attorney. For the purposes of this Declaration, I have been informed about certain aspects of the law that are relevant to my opinions. My understanding of the law is summarized below.

15. I have been informed and understand that determining whether a patent claim is valid requires a two-step analysis. First, the claim must be construed. Second, the properly construed claim must be compared to the prior art.

16. I have been informed and understand that claim construction is a matter of law and that the final claim constructions for this proceeding will be determined by the Patent Trial and Appeal Board.

17. I have been informed and understand that in the context of an *inter partes* review, claims are construed from the perspective of a person of ordinary skill in the art at the time of the purported invention (which is approximated based on the earliest priority date of the patent). I understand that absent disclaimer or express definition, claim terms are given their plain and ordinary meaning to a person of ordinary skill in the art in view of the specification and file history and knowledge of a person of skill in the art.

18. I have been informed and understand that a patent claim is invalid if it is anticipated by the prior art (*i.e.*, lacks novelty). I understand that anticipation requires the disclosure in a single prior art reference of every limitation of the claim, expressly or inherently, with the limitations arranged as specified in the claim.

19. I have been informed and understand that, although not expressly disclosed, subject matter may be inherently disclosed in a prior art reference where that subject matter is necessarily present in the expressly disclosed subject matter

and would be understood to be so by those of ordinary skill in the art. I understand that the fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic.

20. I have been informed and understand that a patent claim is obvious and therefore invalid if the claimed subject matter, as a whole, would have been obvious to a person of ordinary skill in the art as of the priority date of the patent based on one or more prior art references and/or the knowledge of one of ordinary skill in the art. I understand that an obviousness analysis must consider (1) the scope and content of the prior art, (2) the differences between the claims and the prior art, (3) the level of ordinary skill in the pertinent art, and (4) secondary considerations, if any, of non-obviousness (such as unexpected results, industry praise, commercial success, long-felt but unmet need, failure of others, copying by others, and skepticism of experts).

21. I understand that a prior art reference may be combined with other references to disclose each element of the invention under 35 U.S.C. § 103. I understand that a reference may also be combined with the knowledge of a person of ordinary skill in the art, and that this knowledge may be used to combine multiple references. I further understand that a person of ordinary skill in the art is presumed to know the relevant prior art. I understand that the obviousness analysis may take

into account the inferences and creative steps that a person of ordinary skill in the art would employ.

22. In determining whether a prior art reference could have been combined with other prior art or other information known to a person having ordinary skill in the art, I understand that the following principles may be considered:

23. (a) A combination of familiar elements according to known methods is likely to be obvious if it yields predictable results;

24. (b) The substitution of one known element for another is likely to be obvious if it yields predictable results;

25. (c) The use of a known technique to improve similar items or methods in the same way is likely to be obvious if it yields predictable results;

26. (d) The application of a known technique to a prior art reference that is ready for improvement, to yield predictable results;

27. (e) Any need or problem known in the field and addressed by the reference can provide a reason for combining the elements in the manner claimed;

28. (f) A person of ordinary skill often will be able to fit the teachings of multiple references together like a puzzle; and

29. (g) The proper analysis of obviousness requires a determination of whether a person of ordinary skill in the art would have a “reasonable expectation

of success” – not “absolute predictability” of success – in achieving the claimed invention by combining prior art references.

30. I am informed that whether a prior art reference invalidates a patent claim as obvious is determined from the perspective of a person of ordinary skill in the art. While there is no requirement that the prior art contain an express suggestion to combine known elements to achieve the claimed invention, a suggestion to combine known elements to achieve the claimed invention may come from the prior art as a whole, or individually, as filtered through the knowledge of one skilled in the art. In addition, the inferences and creative steps a person of ordinary skill in the art would employ are also relevant to the determination of obviousness.

31. When a work is available in one field, design alternatives and other market forces can prompt variations of it, either in the same field or in another. If a person of ordinary skill in the art can implement a predictable variation and would see the benefit of doing so, that variation is likely to be obvious. In many fields, there may be little discussion of obvious combinations, and in these fields market demand – not scientific literature – may drive design trends. When there is a design need or market pressure and there are a finite number of predictable solutions, a person of ordinary skill in the art has good reason to pursue those known options.

32. It is my understanding that there is no rigid rule that a reference or combination of references must contain a “teaching, suggestion, or motivation” to

combine references. But, I understand that the “teaching, suggestion, or motivation” test can be a useful guide in establishing a rationale for combining elements of the prior art. This test poses the question as to whether there is an express or implied teaching, suggestion, or motivation to combine prior art elements in a way that realizes the claimed invention, and it seeks to counter impermissible hindsight analysis.

VI. LEVEL OF ORDINARY SKILL IN THE ART

33. Petitioners propose a definition for a person of ordinary skill in the art as of June 2004 to be a practitioner with “a bachelor’s degree in electrical engineering, computer engineering, or a related field, and at least two years of experience in the research, design, or development of semiconductor memory device structures, or the equivalent, with additional education substituting for experience and vice versa.” Petition, p. 8; Ex. 1002 (Lee Declaration) ¶¶ 2, 34.

34. In the Intel IPR on the ’702 Patent, Intel proposes a definition for a person of ordinary skill in the art “at the relevant time” as having “a bachelor’s degree in electrical engineering, computer engineering, *materials science*, or a related field, and at least *three years* of experience in the research, design, or development of semiconductor memory device structures, or the equivalent, with additional education substituting for experience and vice versa.” Intel Petition, p. 9 (citing Intel Ex. 1003 (Sechen Declaration) ¶ 37).

35. Intel acknowledges the difference: “The IPR2023-00900 petitioner proposes a slightly different articulation of the level of skill. The unpatentability grounds below apply equally under that articulation.” Intel Petition, p. 9 at fn. 5.

36. In the above paragraphs I bolded the two differences in the definitions that Micron, Intel, and their experts propose. As Intel acknowledges, these definitions are “slightly different” adding one more year of experience and/or a background in materials science.

37. For purposes of this IPR, I adopt Micron’s definition. Micron’s low level of skill only confirms the non-obviousness of the claims. My analysis would be the same under Intel’s similar proposed definition.

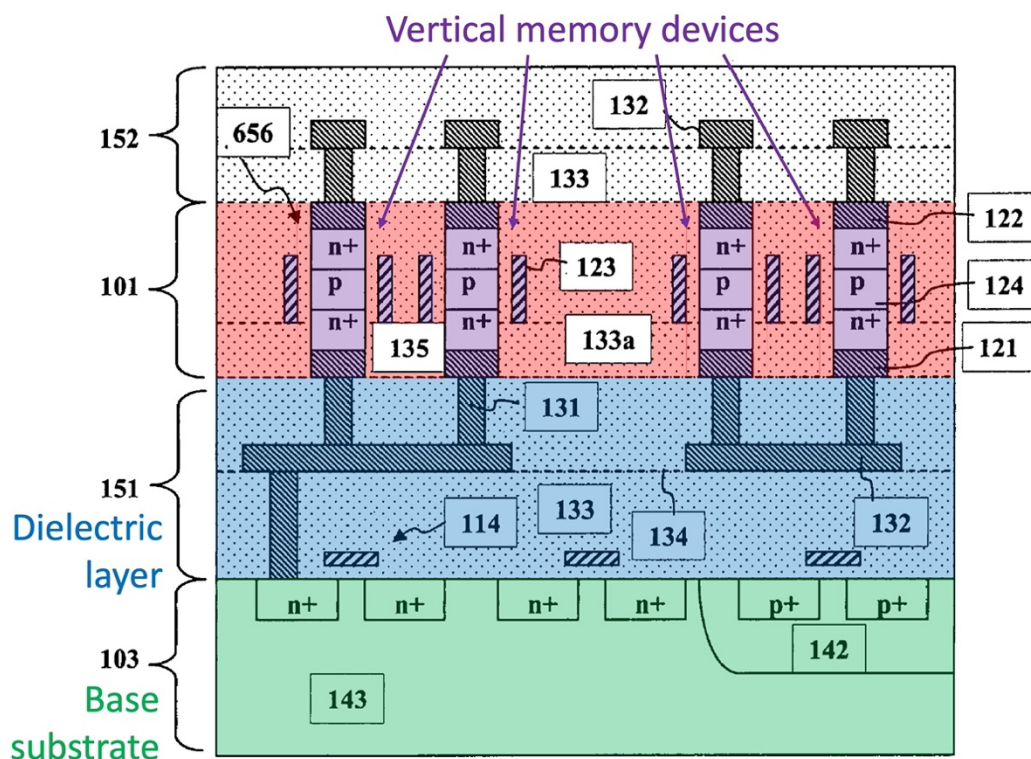
VII. OVERVIEW OF THE ’702 PATENT

38. Most integrated circuits (ICs) since their invention in 1958 have had the same physical structure: transistors are formed in a base substrate of a semiconductor material and the IC is mounted and packaged into a chip.

39. The ’702 patent discloses and claims a radically different physical structure in which not only are transistors formed in the base substrate, but additionally memory cells are fabricated in layers above the base substrate. These memory cells or “floating devices” are interconnected with each other and the transistors in the base substrate by interconnections provided in layers between base substrate and the floating devices layer and above the floating devices layer. The

resulting device is called a 3-D integrated circuit to differentiate it from traditional integrated circuits with transistors only in the substrate. Ex. 1001 ('702 Patent), 3:51-61, 5:18-36.

Fig. 1



Ex. 1001 ('702 Patent), Figure 1, annotated.

40. The embodiment of Figure 1 shows a number of layers.

41. Layer 103 is a base substrate, which includes CMOS circuitry comprising transistors. Ex. 1001 ('702 Patent), Figure 1 & 5:37-38.

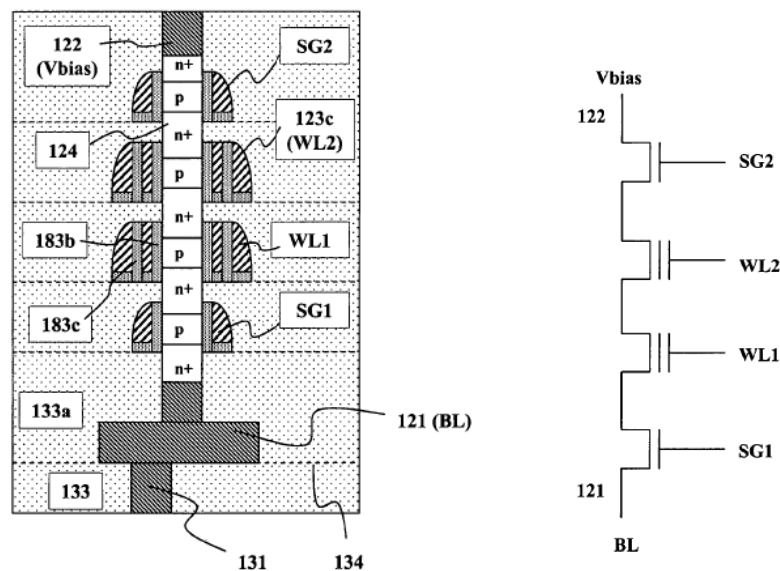
42. Layer 151 is a lower dielectric layer that comprises interconnect and gates for the transistors embedded in the base substrate. Ex. 1001 ('702 Patent), Figure 1 & 5:37-38, 5:56-59.

43. Layer 101 is a floating devices layer (FD) in which vertically oriented transistors are formed. These transistors are distinct from and in addition to the horizontally (i.e. traditionally) oriented transistors in the base substrate 103. Ex. 1001 ('702 Patent), Figure 1 & 5:18-22, 5:38-43. As shown in Figure 1, “vertical memory devices 656” that “are separated by isolation 135 and have floating structures in the filled dielectric materials 133a.” Ex. 1001 ('702 Patent), 5:18-21. Dielectric materials are those that are substantially nonconducting.

44. Layer 152 is a second interlayer dielectric layer comprising further interconnections. Ex. 1001 ('702 Patent), Figure 1 & 5:48-50.

45. The patent discloses that the vertically oriented transistors are in stacks, as depicted, for example in Figure 1. Ex. 1001 ('702 Patent), Figures 1, 4, 20, 27, 29.

46. The '702 Patent describes how memory cells can be formed in the floating device layer(s). In particular, nonvolatile memory cells can be formed in the device layers, such that a plurality of transistors can be formed in each of a plurality of pillar structures. Ex. 1001 ('702 Patent), 5:60-64.



Ex. 1001 ('702 Patent), Figures 29, 30 & 9:59-64.

47. In this embodiment the transistors are connected serially into a chain as found in NAND Flash memory integrated circuits. These structures are referred to in the specification as SOI (Silicon on Insulator) pillars. Ex. 1001 ('702 Patent), Figures 29, 30 & 9:59-64.

VIII. CHALLENGED CLAIMS IN THE '702 PATENT

A. Claim 13

13. A semiconductor memory structure, comprising:

13[a] a substrate having electrical devices formed therein, and further having a dielectric layer disposed above the electrical devices;

13[b] a stackable add-on layer having a plurality of vertically oriented semiconductor memory cells; and

13[c] the stackable add-on layer being bonded to the dielectric layer; and
13[d] wherein the memory cells are nonvolatile memory cells having at least one transistor.

B. Claim 14

14. The semiconductor memory structure of claim 13, wherein the vertically oriented semiconductor nonvolatile memory cell comprises a vertical transistor having a floating gate and a control gate on a SOI pillar.

C. Claim 15

15. The semiconductor memory structure of claim 13, wherein the vertically oriented semiconductor nonvolatile memory cell comprises a vertical transistor having a charge-trapping gate insulator and a gate on a SOI pillar.

D. Claim 16

16. The semiconductor memory structure of claim 13, wherein at least two nonvolatile memory cells are vertically oriented and serially connected together and formed with a first SOI pillar.

E. Claim 17

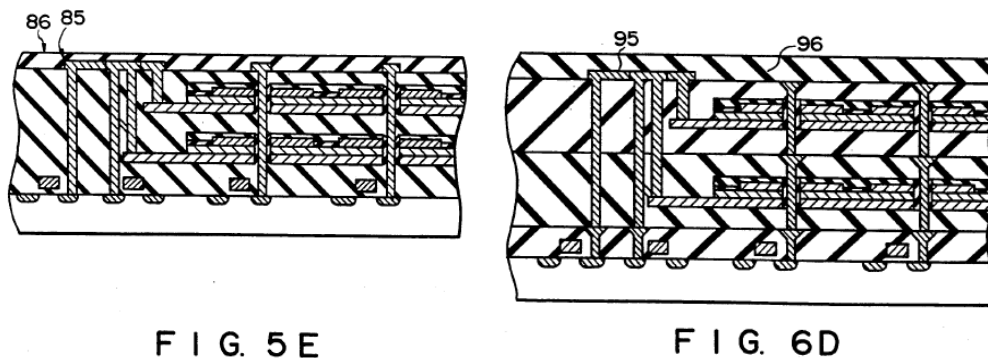
17. The semiconductor memory structure of claim 16, wherein the at least two nonvolatile memory cells on the first SOI pillar are serially connected with an interconnect line disposed on a dielectric layer, to a nonvolatile memory cell formed with a second SOI pillar.

IX. OVERVIEW OF THE CITED REFERENCES

A. WATANABE

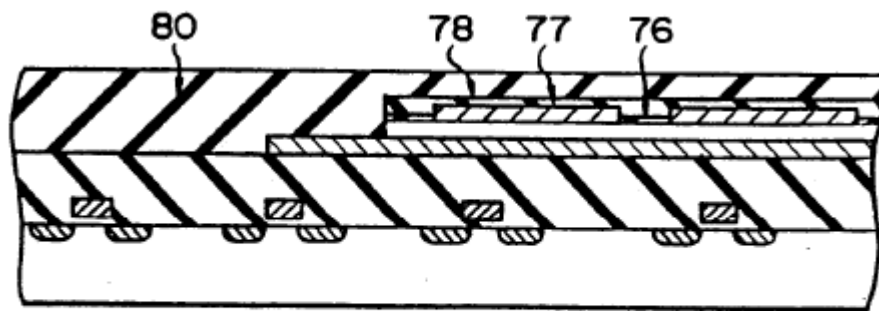
48. U.S. Patent No. 5,091,762 (“Watanabe”) was issued in February 1992.

For my analysis, I have been asked to assume that Watanabe is prior art. It relates principally to the construction of a DRAM semiconductor memory device in which a plurality of layers are constructed or placed on top of the base semiconductor substrate, each layer comprising a plurality of memory cells. Ex. 1005 (Watanabe), 1:10-12, 5:8-17. Two distinct but related methods are presented (the “laminating method” and the “stacking method”) and illustrated in Figures 5 and 6 respectively. Ex. 1005 (Watanabe), Figures 5A-5E & 6A-6D, 5:1-11, 5:56-57.



Ex. 1005 (Watanabe), Figures 5E, 6D.

49. Watanabe’s “lamination method” involves building up the entire integrated circuit of Figure 5E sequentially one layer at a time through standard semiconductor manufacturing techniques. Ex. 1005 (Watanabe), 5:1-44.



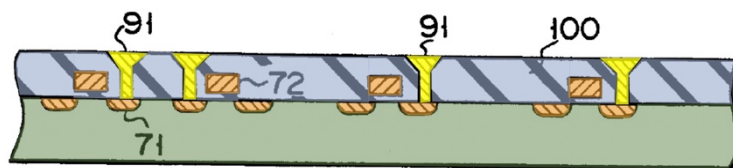
F I G. 5 B

Ex. 1005 (Watanabe), Figure 5B.

50. In contrast, Watanabe's "stacking method" shown in Figure 6 involved first constructing the peripheral circuitry in the silicon substrate then covering it with an insulating layer. Ex. 1005 (Watanabe), 5:58-61. Then each planar member, each comprising a number of layers and constructed with multiple processing steps, is separately constructed and then placed on and bonded to the previous layers. The first planar layer is constructed and placed as a unit on top of the insulating layer on top of the silicon substrate, and the second planar member is placed as a unit on top of the first planar member and bonded to it. Ex. 1005 (Watanabe), 5:61-6:8. Each planar layer is formed in a manner as shown in the embodiment of Figure 5. Ex. 1005 (Watanabe), 5:64-65.

51. Specifically, Watanabe discloses that the stacking method starts by forming peripheral circuits and transistors in the surface region of a silicon substrate. Ex. 1005 (Watanabe), 5:58-60. From this a POSITA would recognize that Figure 6A

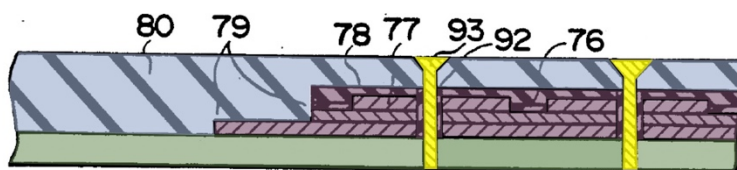
shows the top surface region of a silicon wafer and that for conventional bulk transistors, it shows each formed between a pair of diffusion regions in that silicon substrate and a gate above that surface. For example, a POSITA would recognize that item 71 points to a diffusion region that is connected to a contact 91. A POSITA would recognize item 72 as being the gate of the second transistor from the left. The four gates and three vias are in insulating layer 100. Ex. 1005 (Watanabe), 5:60-63.



F I G. 6 A

Ex. 1005 (Watanabe), Figure 6A, annotated.

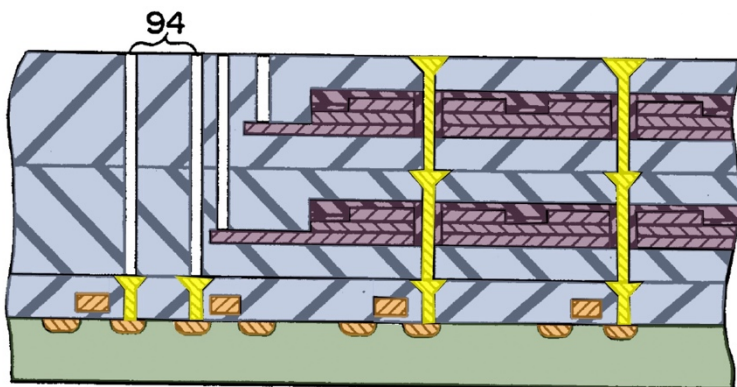
52. Separately, the “stacking method” involves constructing a plurality of very thin planar members, one of which is shown in Figure 6B. Ex. 1005 (Watanabe), Figure 6B, 5:64-6:5. Each is fabricated according to the laminating method. Ex. 1005 (Watanabe), 5:64-65. At this stage, each planar member is built on a silicon substrate. Ex. 1005 (Watanabe), 5:11-13 (green, below). On this are deposited the layers which make up transistors and circuitry (purple, below) as explained with respect to Figures 5A and 5B. Ex. 1005 (Watanabe), 5:8-26.



F I G. 6 B

Ex. 1005 (Watanabe), Figure 6B, annotated.

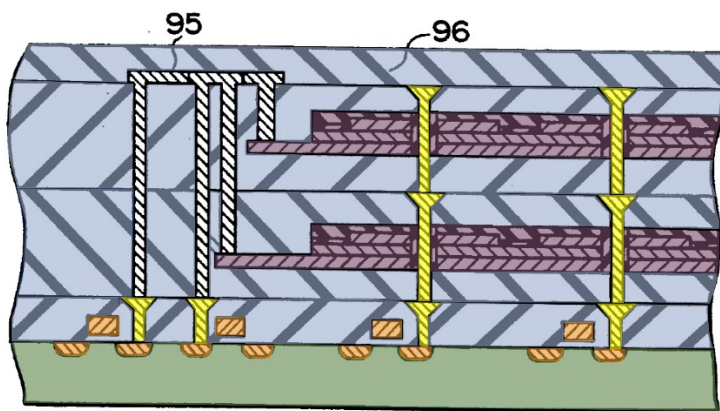
53. The next phase of the “stacking method” results in laying a plurality of these discrete planar members on top of each other and the base substrate layer with the peripheral circuitry and thermally bonding each one to the previous. Ex.1005 (Watanabe), 6:6-8.



F I G. 6 C

Ex. 1005 (Watanabe), Figure 6C, annotated.

54. Finally, additional contact holes are formed and filled with wires to interconnect the different layers and complete the circuitry as a whole. Ex. 1005 (Watanabe), 6:8-11.



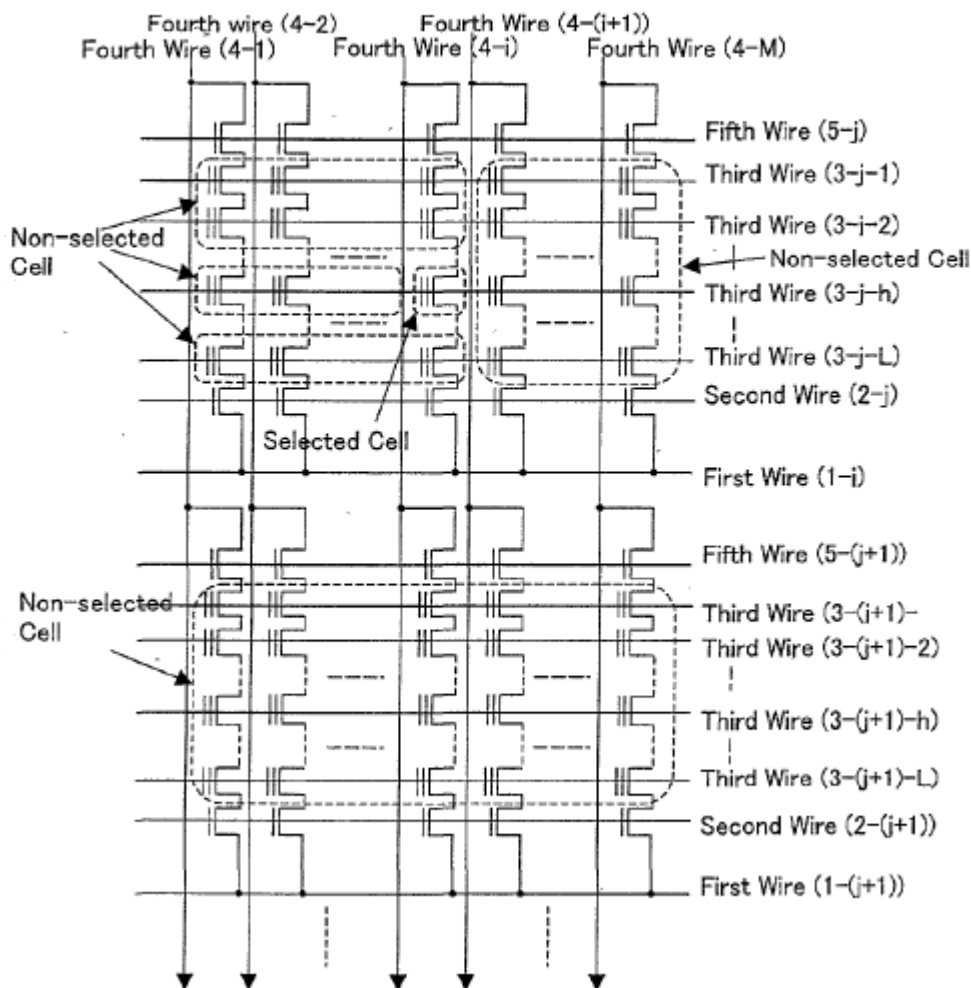
F I G. 6D

Ex. 1005 (Watanabe), Figure 6D, annotated.

B. ENDOH

55. U.S. Patent Application Publication No. 2002/0154556 (“Endoh”) is a massive application filed in 2002 with 1660 figures and 1664 paragraphs in the specification. For my analysis, I have been asked to assume that Endoh is prior art. The patent “relates to a semiconductor memory and its production process.” Ex. 1006 (Endoh) ¶ [0003]. The “Description of Related Art” states that: “As a memory cell of an EEPROM, is known a device of a MOS transistor structure having a charge storage layer and a control gate in a gate portion, in which an electric charge is injected into and released from the charge storage layer by use of a tunnel current.” Ex. 1006 (Endoh) ¶ [0004]. Endoh includes numerous sequences of figures and descriptions that describe the sequences of steps needed to fabricate the semiconductor memory and the circuitry implemented therein.

Fig. 65



Ex. 1006 (Endoh), Figure 65 above shows the NAND memory array implemented in an embodiment of Endoh.

C. LEE

56. U.S. Patent No. 6,881,994 (“Lee”) was filed in 2001 and issued in 2005. For my analysis, I have been asked to assume that Lee is prior art. Lee shows semiconductor memory devices with charge storage devices on a plurality of device

levels. Ex. 1007 (Lee), Abstract, Figure 1, 1:25-26, 14:8-31. The non-volatile memory cell is formed in a vertical structure, with the control gate optionally surrounding the middle portion of the stack, thereby forming a non-volatile EEPROM memory cell.

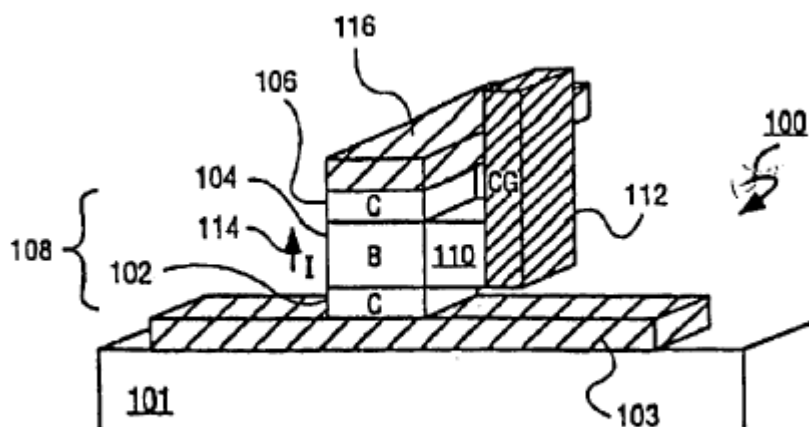


FIG. 1A

Ex. 1007 (Lee), Figure 1A.

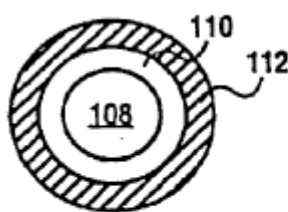


FIG. 1B

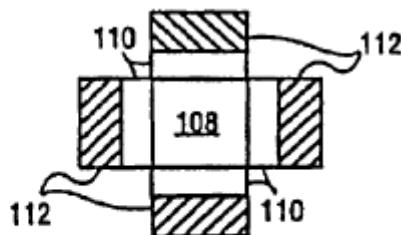


FIG. 1C

Ex. 1007 (Lee), Figures 1B, 1C.

57. Lee's process of creating the monolithic three-dimensional arrays relies heavily on chemical mechanical polishing or "CMP". This is a technique for leveling

the top surface of a wafer by grinding down all the undulations formed by the processing steps. Ex. 1007 (Lee), 11:33-65; Ex. 2033 (Fundamentals of Semiconductor Manufacturing), p. 61 (“The CMP process consists of moving the sample surface against a pad that carries slurry between the sample surface and the pad. Abrasive particles in the slurry cause mechanical damage on the sample surface, loosening the material for enhanced chemical attack or fracturing off the pieces of surface into a slurry where they dissolve or are swept away.”). For example, Lee (Ex. 1007, 65:7-16) describes how a polysilicon layer is added on top of and into the canyons of Figure 88C and then, using, for example, CMP, the top surface is made smooth again, as shown in Figure 88D.

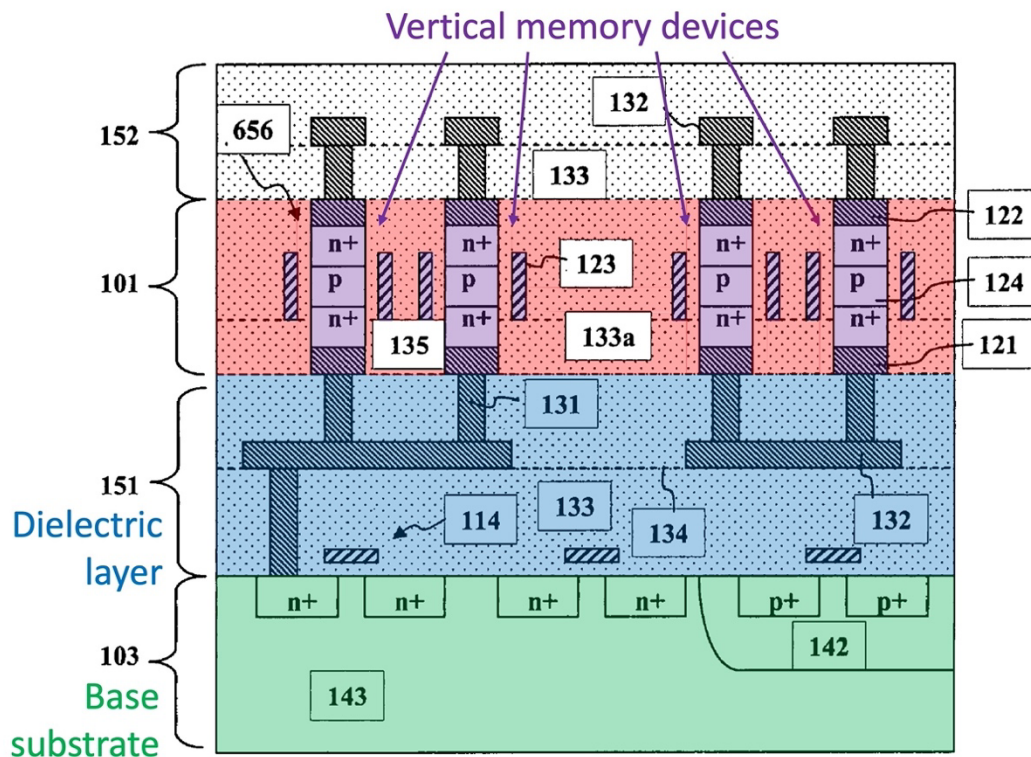
X. CLAIM CONSTRUCTION ANALYSIS

A. SOI Pillar

58. Despite bearing the burden to show unpatentability, Micron proffered no construction of “SOI pillar” in its Petition. Petition, p. 12 (“Petitioner does not believe that any term requires explicit construction ...”). In its decision instituting this review, the Board noted that Micron and its expert “appear to assume that any vertically stacked structure with at least two layers would be understood to disclose or render obvious a ‘pillar’” and asked the parties to “provide an express definition of ‘SOI pillar.’” Institution Decision, p. 17.

59. As explained in the '702 patent specification, "SOI" is an acronym for "Silicon-On-Insulator." Ex. 1001 ('702 Patent), 4:45-46. A POSITA would be familiar with this term and understand it to refer a semiconductor fabrication process in which silicon structures are fabricated on or above an insulating layer. A variety of different types of insulating layers were understood by artisans in 2004. One possibility was to have the insulating layer be an entire supporting wafer, such as sapphire wafer. In SOI embodiments of the '702 patent, the supporting wafer is a traditional silicon wafer and the insulation layer is a layer of silicon dioxide located above that substrate.

Fig. 1



Ex. 1001 ('702 Patent), Figure 1, showing silicon substrate 143, insulating layer 133, and SOI pillar 124, annotated.

60. Other figures show comparable structures that depict SOI pillars.

Fig. 4

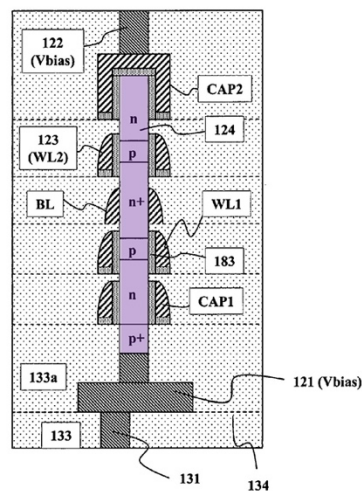


Fig. 20

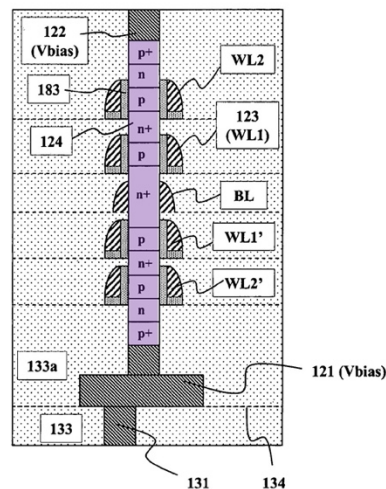
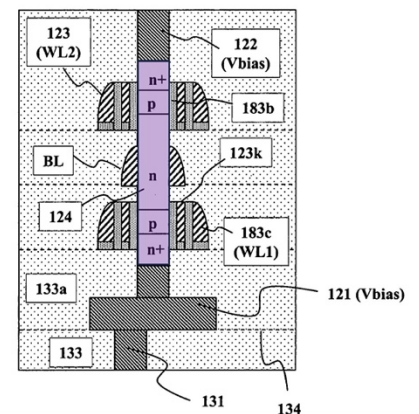


Fig. 27



Ex. 1001 ('702 Patent), Figs. 4, 20, 27 (depicting SOI pillars).

61. For Figure 4, the '702 patent explains that “the aspect ratio of SOI pillar 124 remains relatively small” given its larger height relative to its width. Ex. 1001 ('702 Patent), 8:5-10. Other references refer to similar structures as pillars. The Board correctly observed that “both the '702 patent and Lee refer to pillars where the height of the structure is substantially larger than its width, which stands in contrast to the doped, horizontal layers above insulator 49 Petitioner identifies in Watanabe Figure 2A.” Institution Decision, p. 17 (citing Ex. 1001 ('702 Patent), Figs. 1, 4, 8:5-11; Ex. 1005 (Watanabe), Fig. 2A; Ex. 1007 (Lee), 8:18-19). Micron’s own references also show flash memories with “pillars” depicted as structures where the height is larger than the width:

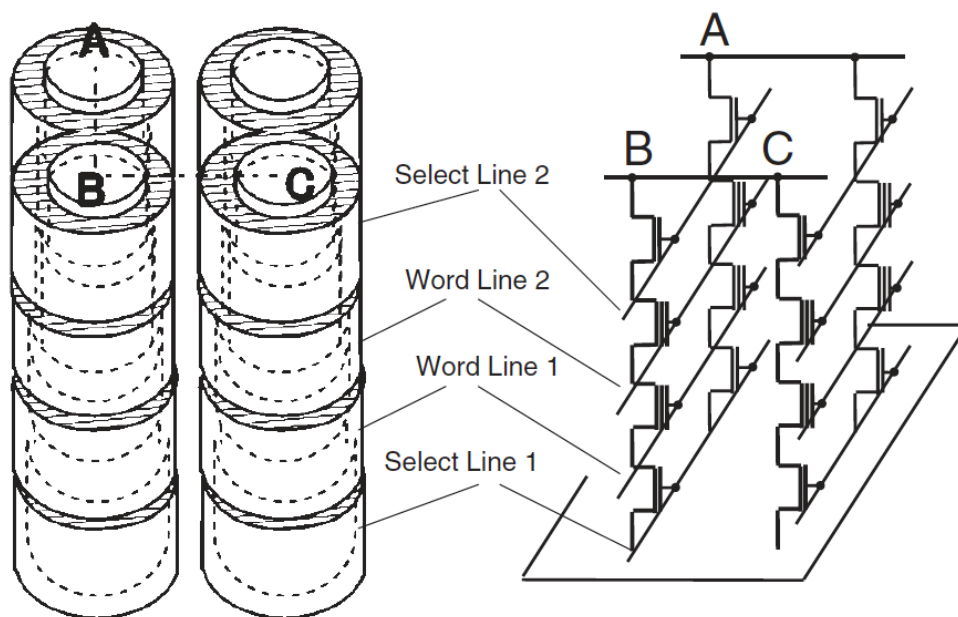
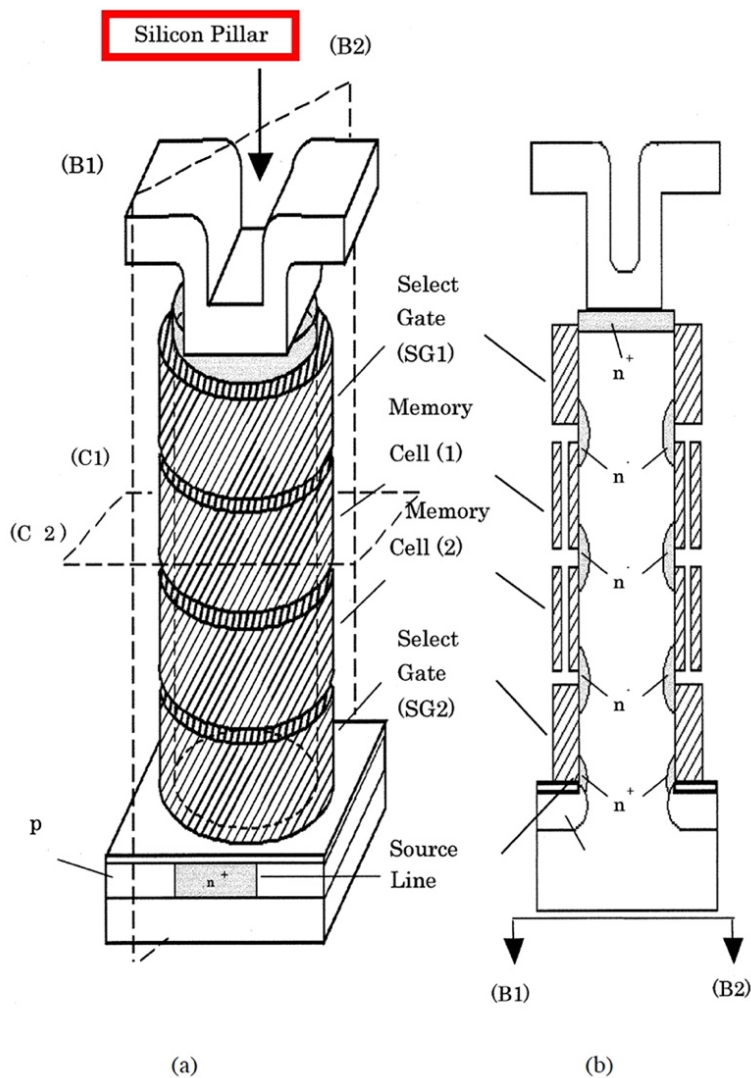


Fig. 1. Bird's eye view of the new three-dimensional high-density S-SGT flash memory and its equivalent circuit.

Ex. 1030 (Sakuraba), Fig. 1; *see also id.*, p. 2217 (“The new three-dimensional high-density S-SGT flash memory is fabricated by arraying S-SGT *pillars*. Figure 1 shows the architecture and the equivalent circuit of the new three-dimensional high-density S-SGT flash memory.” (emphasis added)).



Ex. 1022 (Novel Ultrahigh-Density Flash Memory), Fig. 3(a)-(b), annotated; *see also id.*, Fig. 5 (showing SEM photograph of S-SGT structured cell with silicon pillars).

62. The '702 Patent specification does not define what a pillar is but the English word has a plain and ordinary meaning. For example, Webster's New Universal Dictionary from 2003 defines "pillar" as "an upright shaft or structure, of stone, brick, or other material, relatively slender in proportion to its height...." Ex.

2031 (Webster’s), p. 1469. Random House Webster’s Dictionary from 1997 has the same definition. Ex. 2032 (Random House), p. 988. There is nothing in the ’702 Patent to suggest the inventor intended the use of pillar to have any connotation other than its plain and ordinary meaning. Thus the term “pillar” by itself means a structure that is taller than it is wide.

63. Thus, in the context of the present proceeding and the ’702 Patent, in my opinion an “SOI pillar” is “a silicon-on-insulator structure taller than it is wide.”

XI. REBUTTAL OF THE PETITION’S ARGUMENTS

A. Ground 5: Claims 13-15 Are Not Obvious Over Lee in View of Watanabe

64. Ground 5 of the Petition asserts that claims 13-15 of the ’702 Patent are obvious to one of skill in the art over Lee in view of Watanabe. I disagree.

1. No Motivation to Combine Lee and Watanabe

65. The Petition’s motivation to combine Lee and Watanabe is based on the assertion that “Lee and Watanabe provide complementary solutions for arranging memory cells three-dimensionally.” Petition, p. 69. Petitioners state that both Lee and Watanabe disclose “layer-by-layer sequential deposition” methods of constructing three-dimensional arrays. Petition, p. 70. Further they say that a POSITA would have found it obvious to substitute Watanabe’s “stacking method” for Lee’s sequential deposition method to meet the requirements of Claims 13-15. I disagree.

66. Specifically, Watanabe’s Figure 6B shows a “planar member” with a supporting substrate, completed contact holes 93 lined with an oxide film 92 and filled with a metal wire 93. Ex. 1005 (Watanabe), 5:64-6:1.

67. Watanabe next discloses that the layers are bonded together by a “thermal process of 900° to 1000° C.” Ex. 1005 (Watanabe), 6:6-8. Finally, the global vertical interconnect is formed by contact holes 94 being formed and “a second interconnection wire 95 is buried therein as shown in FIG. 6D, to complete a semiconductor memory device.” Ex. 1005 (Watanabe), 6:8-11.

68. Even Petitioners’ expert is not clear on the process flows and advantages disclosed in Lee and Watanabe and how these motivate the combination or not. Specifically, in his deposition, Petitioners’ expert acknowledged that in Watanabe’s embodiments of Figure 5 (lamination method), the sequential deposition technique uses polysilicon for the transistors in the upper layers. However, he went on to say that in the “upper layer of the stacking method is usually single-crystal semiconductor structure.” Ex. 2028 (Lee Deposition), 124:8-125:5. But in fact, Watanabe says that his planar members in the stacking method of Figure 6 are formed by the same techniques as the comparable layers in the lamination method of Figure 5. Ex. 1005 (Watanabe), 5:64-65. So both of the embodiments of Watanabe and the embodiments of Lee use polysilicon-based transistors in the upper layers. There is no improvement in performance or thermal budget, as implied by

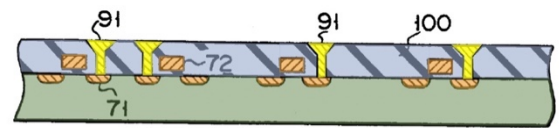
Petitioners' expert in his deposition, from the use of Watanabe's stacking method in Lee. Ex. 2028 (Lee Deposition), 122:19-126:7.

69. Watanabe's disclosure is inadequate to teach a POSITA how to construct the semiconductor memory device it shows in Figure 6 for at least four reasons explained below. The Petition only relies on Watanabe's "stacking method" to meet Claim 13[b] and 13[c]. Petition, p. 72. Since the teachings of Lee do not, and indeed cannot, fill in these gaps in Watanabe's "stacking method" shown in Figure 6, a POSITA would not be motivated to combine these embodiments of Watanabe with those of Lee or Endoh. Based on the knowledge and experience of a POSITA as defined by Petitioners, and the actual teaching of Watanabe and Lee cited in the Petition, it is my opinion that a POSITA would not have been motivated to make this combination or expected a reasonable likelihood of success given the numerous hurdles in front of him.

a. Exceeding Thermal Budgets

70. The first reason that a POSITA would not be motivated to combine the cited embodiments of Watanabe and Lee related to issues of thermal budgets in semiconductor manufacturing processes.

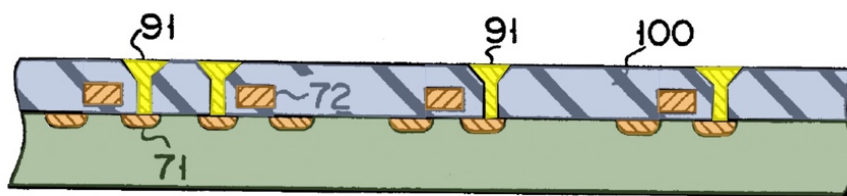
71. A POSITA would have understood that the manufacturing of integrated circuits with transistors formed in a silicon substrate (for example the base layer shown in Figure 6A of Watanabe shown at right) is



subject to a total thermal budget—the total amount of time spent at high temperatures during and after the formation of those transistors. Ex. 2027 (Batude), pp. 715-716.

72. A thermal budget exists because the dopant ions that form the source and drain move every time the device is raised to an elevated temperature. Ex. 2027 (Batude), p. 715 (“[T]o avoid additional dopant diffusion or interfacial oxide growth on bottom transistor, LT (Low Temperature) (<650° C) top FETs process is mandatory”; “Top MOSFETs are processed with an overall thermal budget of 650° C.”).

73. The formation of the source and drain regions are among the very first steps in the fabrication of an integrated circuit because these regions are in the silicon substrate (e.g. item 71 in Figure 6A of Watanabe) below all the metallization and interconnect, and planar members in Watanabe’s case. Ex. 1005 (Watanabe), 5:58-60 (“transistors 71 and 72 are formed in the surface region of an Si substrate”).



F I G. 6 A

Ex. 1005 (Watanabe), Figure 6A, annotated.

74. Once the source and drain have been formed, if the temperature is elevated then those dopants will diffuse further into the substrate than desired, altering the characteristics of the transistors. The higher the temperature or the longer the substrate is held at an elevated temperature the more the dopants will diffuse and the greater the degradation of the transistor characteristics **to the point that they can deviate from the design parameters**. Ex. 2027 (Batude), pp. 715-716.

75. Petitioners' expert specifically relied on Watanabe's stacking method involving "high temperature bonding" (Ex. 1002 (Lee Declaration) ¶ 149) but later acknowledged that such high temperature bonding involving temperatures of 900° to 1000° C is incompatible with the rest of Lee's and Watanabe's process flows. Ex. 2028 (Lee Deposition), 123:13-124:7 ("In other words, the processing of the upper layer transistors cannot go above 650 degrees C, as described in this reference. And the reason for that is because if you do that, if you use anything higher than 650 degrees C, then the transistor at the lower layers, particularly the CMOS transistor

in the ... substrate level ... would experience dopant diffusion and interfacial oxide glow, which is detrimental to the characteristics of the transistors.”).

76. Thus, by 2004 and as articulated by Petitioners’ expert, the general understanding of a POSITA at the time was that once those transistors are formed, no subsequent processing step should be conducted at temperatures above 650° C and certainly not above 900° C as disclosed by Watanabe. Ex. 2028 (Lee Deposition), 123:13-124:7, 125:6-126:7. This idea is corroborated by the new exhibit introduced during his deposition. Ex. 2027 (Batude), p. 715 (“[T]o avoid additional dopant diffusion or interfacial oxide growth on bottom transistor, LT (<650°C) top FETs process is mandatory.”). And yet Watanabe teaches that each of the plurality of stackable layers is bonded to the previous layer by means of a thermal process at temperatures of 900° to 1000° C. Ex. 1005 (Watanabe), 6:6-14. As a result, the more planar devices in his final design, the greater the total time spent at or above 900° C, and yet Watanabe contemplates vertical structures involving 100 planar members. Ex. 1005 (Watanabe), 4:35-38. Each time an additional planar member is added to the existing stack, the collection to that point is necessarily heated again aggravating the thermal budgets for the base substrate levels and the transistors of the peripheral circuitry there. Just like a multi-layer cake which is baked again each time a new layer is put on, the bottom layers will be overcooked by the time the entire cake is completed. By the Petitioners’ expert’s own admission,

Watanabe's high-temperature bonding process would severely impact the transistors in the substrate, even if only a few such planar members were added to the ensemble. In contrast, the specification of the '702 Patent expressly provides for low-temperature processing to avoid the whole issue of reduced thermal budgets at lower process geometries. Ex. 1001 ('702 Patent), 7:15-35.

77. Watanabe does not teach a POSITA how to reconcile the well-known design consideration of high-temperature processing steps diminishing or shattering thermal budgets with its statement at Ex. 1005 (Watanabe), 6:6-8 advising high-temperature thermal bonding. This teaching of a high-temperature thermal bonding as an integral part of the stacking method teaches away from the combination of Lee's memory cell layers with this embodiment of Watanabe, and at a minimum eviscerates any motivation to combine the two references.

b. Nothing About Alignment

78. Second, Watanabe provides no guidance or teaching regarding how the planar members that make up Figure 6C are to be formed, handled, and aligned prior to bonding them to the bottom layer (Figure 6A) or to each other. A POSITA would have known that alignment was necessary and would have found such guidance lacking in Watanabe. Ex. 2037 (ITRS 2007 Interconnect), p. 47 ("Providing adequate alignment may be the most challenging requirement to achieve the interconnect density necessary for 3D technology to replace on-die interconnects.").

Watanabe's Figure 6C shows the required precision of this alignment to be within a small multiple of the minimum feature size of the process being used. Petitioners' expert agreed in his deposition that ensuring proper alignment is critical to manufacturing a working device. Ex. 2028 (Lee Deposition) 110:8-16, 113:14-114:2. He also acknowledged that using either of the alignment methods available in a stacking method ("wafer alignment mark and bump-type") are less precise than the methods available if using a wafer deposition method. Ex. 2028 (Lee Deposition), 117:12-22. Watanabe does not teach any methods to account for the lack of precise alignment involved in the stacking method, for example, by potentially redesigning the circuitry to use substantially larger inter-planar member contact pads or to use other ways to achieve looser alignment requirements. Ex. 1005 (Watanabe), Figure 6C. In contrast, the specification of the '702 Patent explicitly addresses for this critical concern relating to the aggregation of precisely aligned semiconductor structures. Ex. 1001 ('702 Patent), 6:13-25 ("[C]ombining the SOI layer with a semiconductor substrate does not require the same type of wafer alignment structures as are used in photolithographic processes....").

79. Historically the "**minimum feature size**" was a term that was useful to characterize the manufacturing process, and was generally taken to be the size of the transistor gate, i.e. item 72 of Figure

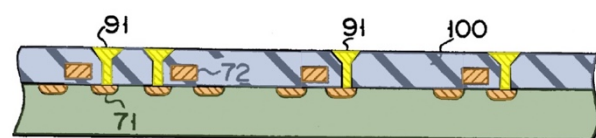


FIG. 6A

6A of Watanabe (shown at right). As processes continued to shrink, this rule of thumb became less reliable, but the term continues to be useful and used in the industry to describe memory cells.

80. From Watanabe's Figures 6A-6D, the landing pads at the top of each layer to which the vias from the next layer above have to make contact are small: less than 2x the minimum feature size. While I understand that patent figures are not necessarily drawn to scale, if the landing pads are much larger than the minimum metal spacing or the minimum via spacing, the pitch and the area of each of Watanabe's non-volatile memory cells (per Ex. 1005, Figure 7, 6:15:19) would have to increase accordingly, substantially impacting Watanabe's stated goal of improved integration density. Ex. 1005 (Watanabe), 1:65-2:5, 6:20-22. Any small misalignment in either direction of the first planar member with the substrate layer of Figure 6A, or between any two adjacent planar members, greater than the size of these tiny landing pads would result in unintended open circuits and thus non-functional devices.

81. Watanabe never mentions any processes or equipment that would be capable of completing the process steps of creating a stand-alone planar member of Figure 6B or of successfully aligning and bonding them together to form the intermediate result of Figure 6C. A POSITA in 2004 would have been particularly troubled by the lack of guidance on aligning the planar member to the base layer and

any previously deposited planar members. The lack of guidance would have indicated to a POSITA in 2004 that Watanabe's stacking method could not be successfully used or combined with Lee. Accordingly, a POSITA would not have been motivated to combine this embodiment of Watanabe with any teachings of Lee, much less had a reasonable expectation of success in doing so.

c. Watanabe's Sparse Memory Cells

82. Third, a POSITA trying to duplicate Watanabe's disclosure would find that the principal DRAM embodiments of Figures 2A, 2B, 5, and 6 are not consistent with Watanabe's stated goal of "providing a high integration density." Ex. 1005 (Watanabe), 1:10-12, 1:49-52, 2:44-3:30. Petitioners' expert expressly relies on this disclosure as a reason to combine Lee with Watanabe. Ex. 1002 (Lee Declaration) ¶ 144 ("Lee and Watanabe provide complementary solutions for arranging memory cells three-dimensionally to provide a high integration density.").

83. The storage of information in a DRAM cell is accomplished by storing charge on a capacitor, which is isolated from bit lines by an access transistor. In Watanabe's Figure 2A embodiment, the capacitor is formed between plates 46 and 45, separated by the capacitor dielectric 47. Ex. 1005 (Watanabe), 3:19-30. The capacitance of this capacitor is proportional to the area of the capacitor, illustrated in the top view of Figure 2B as item 45. Ex. 1005 (Watanabe), Figure 2B. When the access transistor is turned on, charge sharing occurs between this storage capacitor

and causes the voltage on the bit/data line to change a small amount. Ex. 2035 (DRAM Circuit Design Tutorial), pp. 27-29, 56; Ex. 2036 (VLSI Memory Chip Design), pp. 15-19.

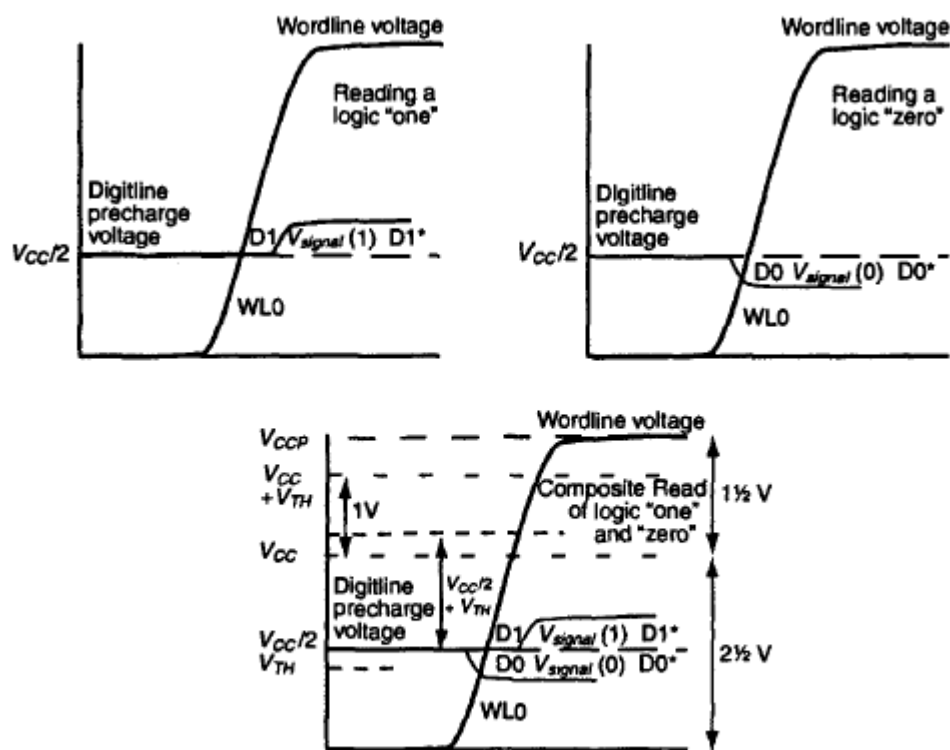


Figure 1.25 Cell access waveforms.

Ex. 2035 (DRAM Circuit Design Tutorial), p. 27, Figure 1.25.

84. The essential challenge of making high density, low cost DRAMs is to make the ratio of the capacitance of the storage capacitor to that of the bit line (or in the case of Watanabe, the data plane 41) as large as possible so that the change in voltage on the bit line is detectable by the sense amplifiers while simultaneously making the memory cell as small as possible so that more can be fit on an integrated

circuit. Ex. 1005 (Watanabe), 3:16-30; Ex. 2035 (DRAM Circuit Design Tutorial), pp. 26-29, 35-37. The essential problem with Watanabe's DRAM design is that the storage capacitor is planar, and the area of the data plane covers the area of as many memory cells as are coupled to a single data plane.

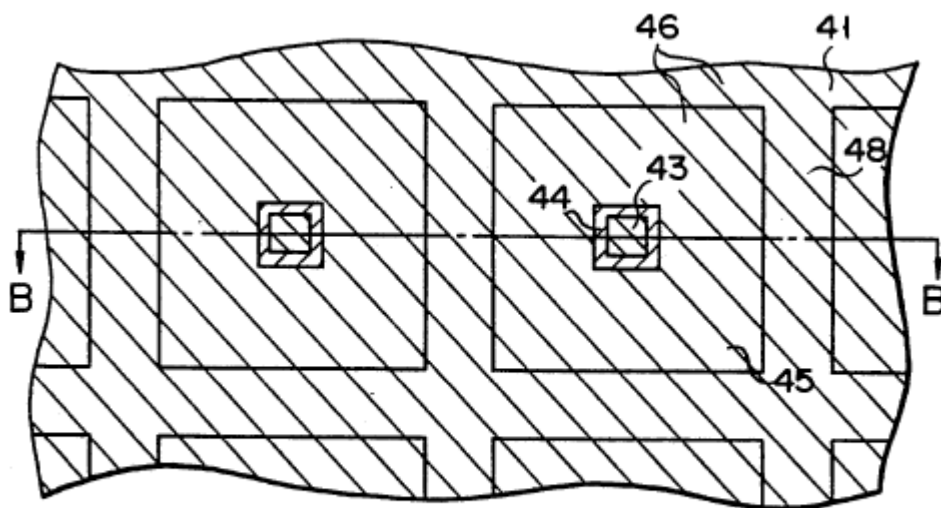


FIG. 2B

Ex. 1005 (Watanabe), Figure 5 (showing capacitive elements 45), 1:58, 3:19-45.

85. That means that the capacitance of the storage capacitor is small, and the capacitance of the data plane is large – the opposite of what is desirable. Increasing the size of Watanabe's storage capacitor would not improve matters because increasing the area of the memory cells has the inevitable side effect of increasing the area of the data plane and thus the ratio of capacitors would remain roughly the same. In order for the charge sharing to result in a detectable change in

the voltage on the data plane, the number of memory cells per data plane and per sense amplifier would have to be much smaller than is typical for a DRAM memory device. A consequence of having a small number of cells per sense amplifier is that the memory density is reduced to the point where Watanabe's multiple planar layers would not be able to increase the memory density sufficiently to compensate. Thus, one of skill in the art looking to increase the density of memory cells in DRAM would not look to Watanabe.

86. In conventional DRAMs, this critical ratio of capacitances is maximized by creating storage capacitors that extended vertically, either down into the substrate trenches or up into tall structures, as shown below:

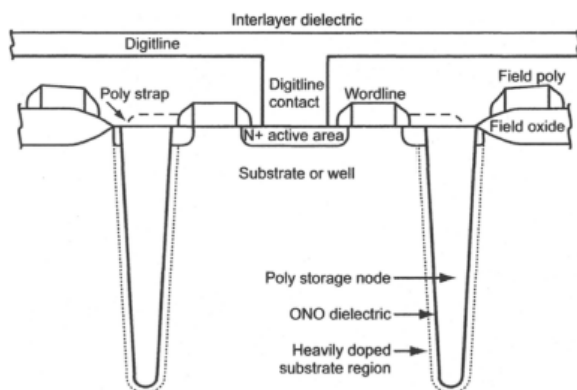


Figure 2.13 Trench capacitor Mbit process cross section.

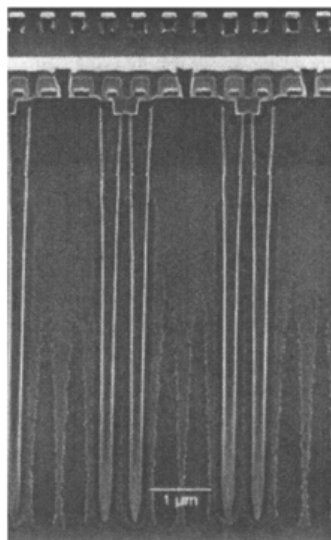


Figure 2.14 Trench capacitor Mbit process SEM image.

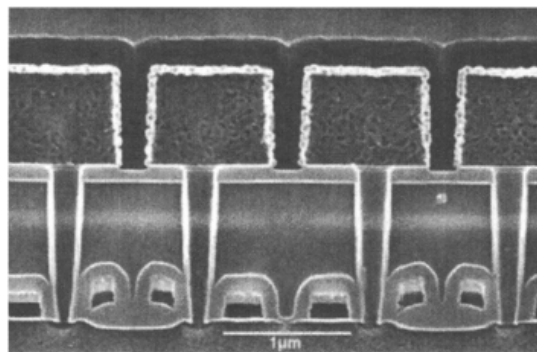


Figure 2.12 Buried digitline Mbit process SEM image.

DRAM Trench Capacitor

DRAM Tall Capacitor

Ex. 2034 (DRAM Circuit Design Fundamental), pp. 41-44, Figures 2.12–2.14.

87. In Watanabe's design of Figures 5 and 6, neither of these are possible because each planar layer is above the substrate and possibly below other planar layers.

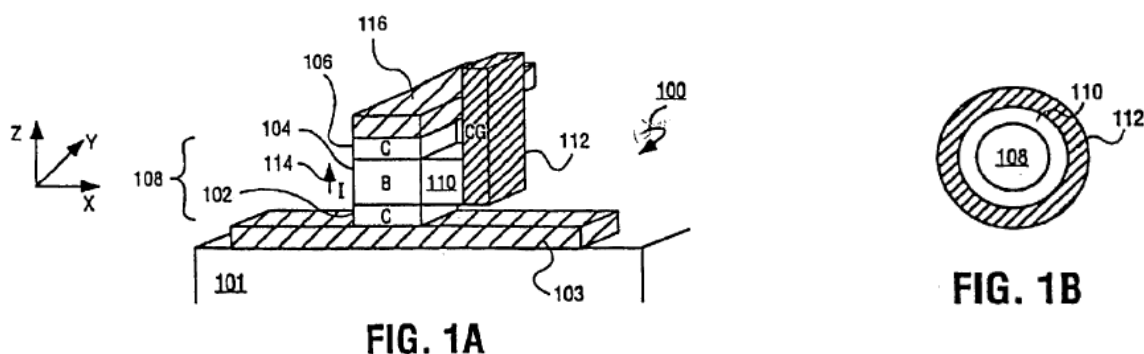
88. In summary, a POSITA, trying to duplicate Watanabe’s DRAM design would fail to create a working DRAM with increased integration density and increased wiring accuracy relative to conventional DRAMs. A POSITA would recognize that Watanabe’s disclosure did not provide a “high integration density” architecture and would not have looked to Watanabe for this purpose. This too presents yet another reason why a POSITA would not be motivated to combine Watanabe’s embodiments with Lee.

d. Incompatible Architectures

89. Fourth, the basic memory device architectures of Lee and Watanabe are incompatible with each other. With regard to Claim 13[b] in Ground 5, Petitioners state that “[a] POSITA would have had a reasonable expectation of success in combining the teachings of Lee and Watanabe with no change in their respective functions because both of these references purport to solve the same problems in similar and predictable ways, such as using the well-known teachings of vertical transistors and pillar structures.” Petition, p. 71. This is simply not true.

90. To support their statement with regard to element 13[b] (“a stackable add-on layer having a plurality of vertically oriented semiconductor memory cells”) in Ground 5, Petitioners refer back to Section VII.C.3 and Section VII.A.3 of the Petition. Section VII.C.3 of the Petition refers to Figure 1A of Lee to show a vertically oriented memory cell. Petition, pp. 48-49; Ex. 1007 (Lee), Figure 1A,

14:8-31. In Lee's Figure 1B cell the pillar structure comprises the source, channel, and drain regions of the TFT transistor made up of amorphous or polycrystalline silicon, appropriately doped, with the control gate wrapped around the outside of the pillar. Ex. 1007 (Lee), Figure 1B, 4:61-63, 8:19-22, 12:5-13, 14:64-15:3. In this embodiment the central pillar comprises silicon regions and the transistor.



Ex. 1007 (Lee), Figures 1A, 1B.

91. With regard to Watanabe, the Petition refers back to Section VII.A.3, which describes the DRAM memory cell embodiment of Figure 2A in conjunction with Figure 1 showing how these cells are organized into planar layers. Petition, pp. 16-18.

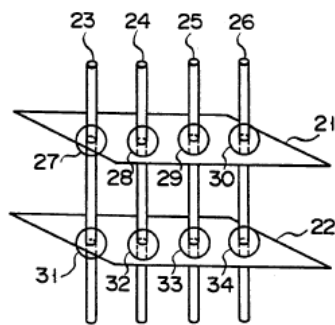


FIG. 1

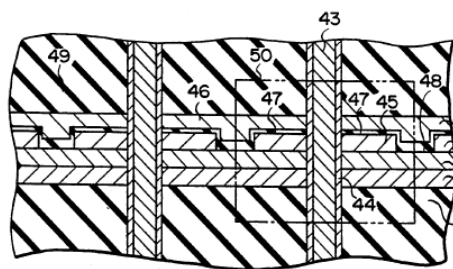


FIG. 2A

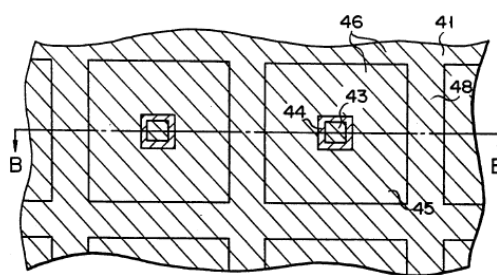
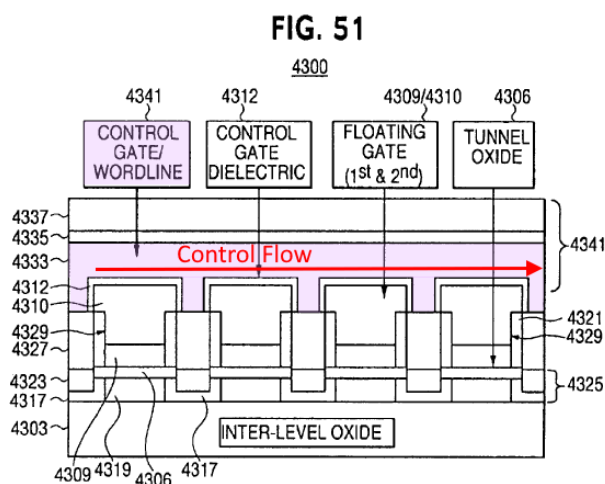


FIG. 2B

Ex. 1005 (Watanabe), Figures 1, 2A, 2B.

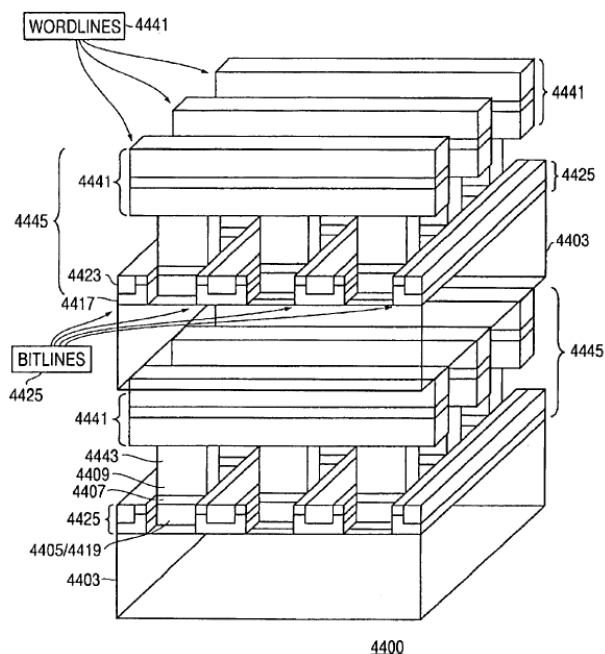
92. The embodiment of Watanabe's Figures 2A and 2B show a transistor for the memory cell formed with the source formed in layer 41 (the data plane), the channel formed in layer 42 right at the gate insulating film 44, and the drain formed by unit 45. Ex. 1005 (Watanabe), 2:16-19, 2:62-3:15. The word line is formed by a hole being lined by the insulating film 44 (the gate oxide of the access transistor) and then the center of the hole is filled with a wire 43. Ex. 1005 (Watanabe), 3:2-5. Indeed, Watanabe's insulated wire 43 does not include any silicon: Watanabe does not use or even disclose SOI pillars, as construed above.

93. So the embodiments of Figure 1A of Lee and Figure 2A of Watanabe are very different. From a data flow perspective, in the embodiment of Lee, data flows vertically, before transitioning to a horizontal bit line. The control flow (i.e. the signals on the word lines that determine the voltages on the control gates) flows horizontally to many memory cells. This is evident in several of the Figures that show completed structures and some that show only a portion of a memory device. For example, Figures 51 and 52 show word lines carrying control information horizontally to many memory cells:



Ex. 1007 (Lee), Figure 51, annotated.

FIG. 52



Ex. 1007 (Lee), Figure 52.

94. Figure 12B shows a portion of a cross section of a memory array. Placing two copies of it beside one another illustrates the control flow in conductor 1200:

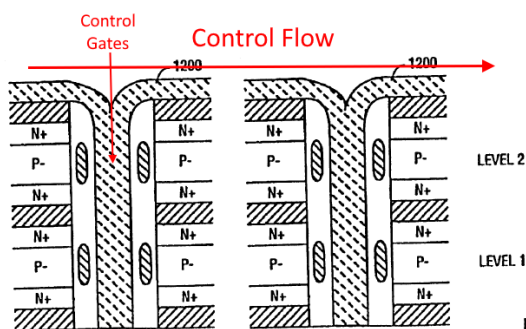


FIG. 12B

Ex. 1007 (Lee), Figure 12B (twice), annotated.

95. Further, many figures show traditional, linear bit lines (e.g. item 116) carrying data out of the memory cell:

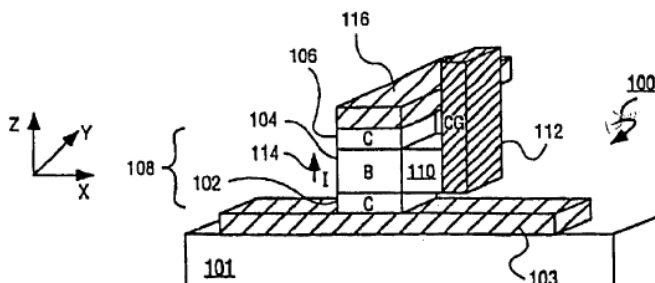
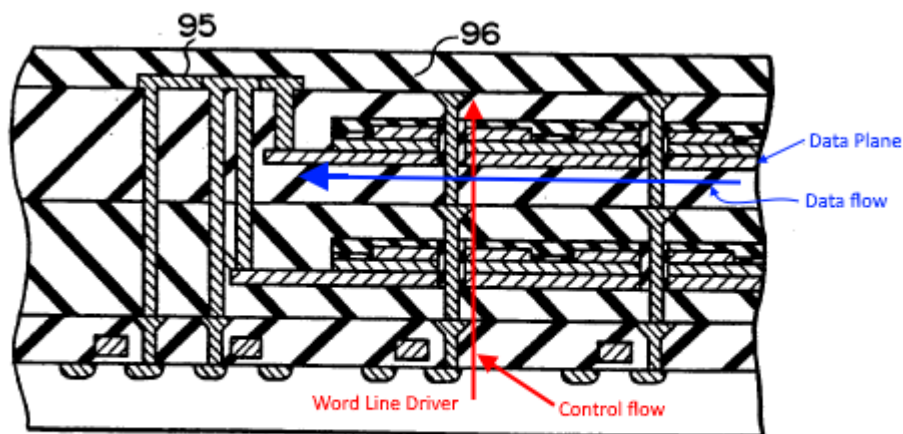


FIG. 1A

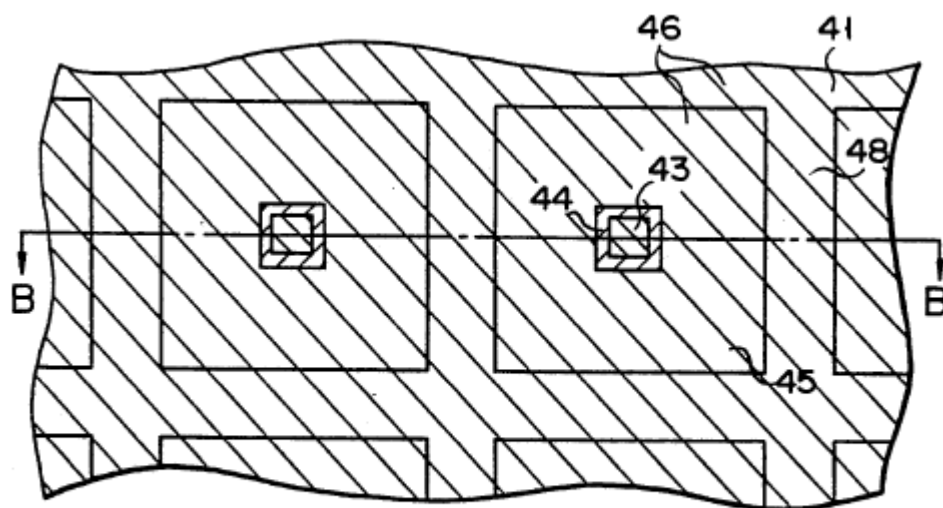
Ex. 1007 (Lee), Figure 1A.

96. In contrast, in Watanabe the embodiments of related Figures 2A and 6D show the word lines that carry the control signals are arranged vertically through the contacts 93 to the control gates of all of the memory cells in a stack. Further, Watanabe is unconventional in that data signals flow horizontally through a 2-dimensional data plane 41 (as opposed to the typical linear bit lines of Lee).



F I G. 6D

Ex. 1005 (Watanabe), Figure 6D, annotated.



F I G. 2 B

Ex. 1005 (Watanabe), Figure 2B.

97. This difference is profound because in both cases, the memory cells need to be aggregated into collections of cells that share a sense amplifier, and the placement of the sense amplifiers and routing of the data to those circuits is radically different with such disparate data flows. All of the placement and routing of the memory cells and the peripheral circuitry would also have to be completely changed to make any of the embodiments of Lee incorporate the stacking method of Watanabe. In short, many other aspects of Lee memory device would have to change to account for Watanabe's stacking method and Dr. Lee never accounts for this. Ex. 1002 (Lee Declaration) ¶¶ 148-49. Because the memory device architectures of Lee and Watanabe are architecturally orthogonal to and radically different from each

other (i.e. the direction of flow of select information and data are perpendicular to how these flow in the other reference), the two sets of teachings are not readily combinable. So, contrary to Petitioners' assertion a POSITA would not have had a reasonable expectation of success in combining the teachings of Lee and Watanabe, and would not have been motivated to make the combination.

98. In conclusion, the teachings of the recited embodiments of Lee and Watanabe are not combinable in a straightforward way that would be within the capabilities of a POSITA as suggested by Petitioners. The embodiment of Figure 6 of Watanabe is specifically the embodiment relied upon by Petitioners in their Ground 5 combination of Lee with Watanabe. Petition, p. 70; Ex. 1005 (Watanabe), 5:56-6:14. The substantial differences between Watanabe and Lee and their respective failures to explain the embodiments relied upon in the Petition would dissuade a POSITA from attempting to combine them as suggested by Petitioners and would ensure that a POSITA would not have any expectation of success in that attempted combination.

2. Claims 14 and 15

99. Dependent Claims 14 and 15 depend on Claim 13 and further recite two different types of nonvolatile memory cells (floating gate and charge trapping, respectively) formed on a SOI pillar. Ex. 1001 ('702 Patent), 12:35-42. Petitioners claim that Lee alone discloses dependent Claims 14 and 15. Petition, p. 73.

100. Petitioners also refer back to sections VII.B.2 and VII.B.3 here. These sections are from the analysis of Ground 2 which is based on the combination of Watanabe in view of Endoh. But Endoh is not part of the combination for Ground 5, and so these sections are irrelevant here. Indeed, Petitioners did not cite to any section of the Petition's analysis of Ground 1 (Watanabe alone) because they do not assert that Watanabe alone anticipates or renders obvious Claims 14 and 15. This is presumably because Watanabe fails to disclose any SOI pillars, a requirement for both Claims 14 and 15. Therefore, Petitioners have failed to meet their burden to show how the combination of Lee and Watanabe alone renders Claims 14 and 15 obvious.

B. Ground 6: Claims 16 and 17 Are Not Obvious Over Lee in View of Watanabe and Endoh

101. Ground 6 of the Petition asserts that Claims 16 and 17 of the '702 Patent are obvious to one of skill in the art over Lee in view of Watanabe and Endoh. I disagree.

1. Claims 16 and 17 Depend on Claim 13

102. Claims 16 and 17 depend on Claim 13. Ex. 1001 ('702 Patent), 12:43-52. This ground does not independently analyze this combination as anticipating or rendering obvious Claim 13. Instead, Petitioners refer back to Grounds 4 and 2, claiming that both Lee combined with just Endoh discloses Claims 16 and 17, and

also that Watanabe combined with just Endoh also discloses Claims 16 and 17, respectively. Petition, p. 73.

103. The sections of the analysis of Grounds 4 (Lee in view of Endoh) refer back to portions of the analysis of Ground 3 (Lee alone) that each discuss elements 13[d] and Claim 14 only having been disclosed by Lee. Petition, p. 61. The cited sections of Ground 3 (Lee) do not directly address or refer back to any other sections of the analysis of Ground 3 to show that any of the other elements of Claim 13 other than Element 13[d] are met by Lee alone.

104. Similarly, the portion of Ground 2 (Watanabe in view of Endoh) refers back to the analysis of Ground 1 (for Element 13[d]) and an earlier portion of the analysis of Ground 2 (for Claim 14). Petition, p. 37. The portion of the analysis of Ground 1 cited there does not address anything other than Watanabe's alleged disclosure of Element 13[d]. Petition, pp. 25-26. The portion of the analysis of Ground 2 cited there addresses Claim 14 as allegedly disclosed by Watanabe in view of Endoh. Petition, p. 28. It only addresses Claim 14 and indirectly Element 13[d].

105. Altogether, Petitioners have failed to properly address all of the antecedent elements of Claim 13 as a necessary part of the analysis of this Ground 6.

2. No Motivation to Combine Lee with Watanabe and Endoh

106. In the analysis of Ground 6, the Petition states that “A POSITA would have been motivated to combine Lee with Watanabe and Endoh and would have a

reasonable expectation of success in doing so, because Lee, Watanabe, and Endoh provide complementary solutions for arranging memory cells—including nonvolatile memory—three-dimensionally to provide a high integration density.” Petition, p. 73. As support for this statement, the Petition refers back to its discussions regarding the alleged motivations to combine with regard to Ground 2 (Watanabe in view of Endoh), Ground 4 (Lee in view of Endoh), and Ground 5 (Lee in view of Watanabe).

107. Paragraphs 64-98 of my declaration with respect to the alleged motivation to combine presented in Ground 5 (above) describe in detail why a POSITA would not have been motivated or even able to combine Lee and Watanabe for the purposes of rendering obvious Claim 13, and in particular how a POSITA would not have had a reasonable expectation of success in creating a working DRAM that achieved the stated motivations for the combination. As Claims 16 and 17 depend on Claim 13, those same arguments apply here with respect to the combination of Lee and Watanabe in the context of the present claims.

108. My opinions in Section XI.F below provide a comparable evaluation with respect to the alleged motivation to combine found in the analysis of Ground 2 (Watanabe in view of Endoh) in the context of Claims 14-17. Petition, pp. 26-28. The Petition’s analysis fails in the context of Ground 2 and fails here in the context of Ground 6 for the same reasons.

109. My opinions in Section XI.D below provide another comparable evaluation with respect to the alleged motivation to combine found in the analysis of Ground 4 (Lee in view of Endoh) in the context of Claims 16 and 17. Petition, pp. 59-61. The Petition’s analysis fails in the context of Ground 4 and fails here in the context of Ground 6 for the same reasons.

110. After citing to the flawed motivations to combine from Grounds 2, 4 and 5, the Petition states that “a POSITA would have been motivated to modify Lee in view of Watanabe and Endoh to use an alternative method of forming a stackable add-on layer and obtain the additional features and benefits of implementing the well-known teachings of a charge-trapping gate insulator, SOI pillar, and serial connection” and that “[i]n addition, a POSITA would have had a reasonable expectation of success in combining Lee, Watanabe, and Endoh with no change in their respective functions.” Petition, pp. 73-74.

111. This first conclusion implies that part of the combination that Petitioners presume renders these claims obvious involves the embodiment of Figure 6 in Watanabe. But as described in detail above, a POSITA would not have been motivated to use that embodiment of Watanabe or had any expectation of success in using it and so it cannot be used in a combination to render anything obvious.

112. Petitioners also say that the base embodiment is from Lee. With regard to Ground 4 and the combination of Lee and Endoh there, Petitioners say “Endoh

provides additional well-known teachings of vertically oriented nonvolatile memory cells with a floating gate and control gate, or a charge-trapping gate insulator and gate, connected in series on a SOI pillar.” Petition, p. 60.

113. Claim 16 combined with Claim 13 on which it depends requires:

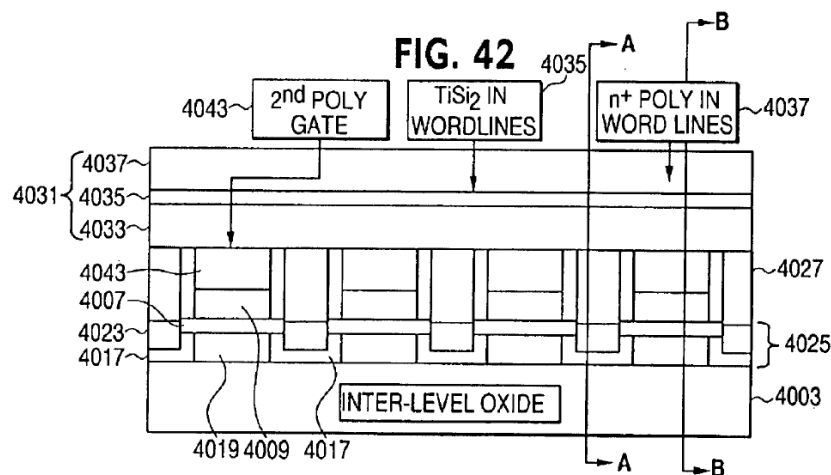
- a substrate having electrical devices formed therein, and further having a dielectric layer disposed above the electrical devices (13[a]);
- a stackable add-on layer having a plurality of vertically oriented semiconductor memory cells (13[b]);
- the stackable add-on layer being bonded to the dielectric layer (13[c]);
- wherein the memory cells are nonvolatile memory cells having at least one transistor (13[d]);
- wherein at least two nonvolatile memory cells are vertically oriented and serially connected together and formed with a first SOI pillar (16)

114. In asserting that these and the other aspects of Claim 16 are found in the combination of Lee, Watanabe and Endoh, the Petition refers to a great many embodiments across all three references, many of which show only one aspect of Claim 16 but which are incompatible with other embodiments pointed to for other aspects of the claim. Finding exactly which embodiments are being cited for which elements involves following several indirections across the Petition.

115. For example, Lee is said to disclose element 13[a]. Petition, p. 71. This passage points to Section VII.C.2. There, Petitioners show Lee's Figure 35 and the associated text. Petition, p. 47; Ex. 1007 (Lee), Figure 35, 12:17-27. But Lee says a lot more about the embodiment of Figure 35. For example, it says that Figure 35 shows an array of memory devices 3101 above the monocrystalline substrate 3105. Ex. 1007 (Lee), 12:27-30. It also says that layers 3104 containing the memory devices and that collectively form the memory device array 3101 are separated by interlayer insulating layers. Ex. 1007 (Lee), 12:23-25. Figures 37 through 44 continue this disclosure by showing the steps for forming a single one of the layers according to a first preferred embodiment. A POSITA would recognize the layers above interlayer oxide 4003 in Figure 42 as corresponding, for example, to one of the layers 3104. Figure 42 is the cross section through the Flash memory array along a word line and Figure 43 shows cross sections perpendicular to that of Figure 42 along cross section lines A-A' and B-B' respectively. Ex. 1007 (Lee), Figures 35-44, 5:46-56, 9:14-41, 12:16-33, 31:38-40, 31:41-35:42.

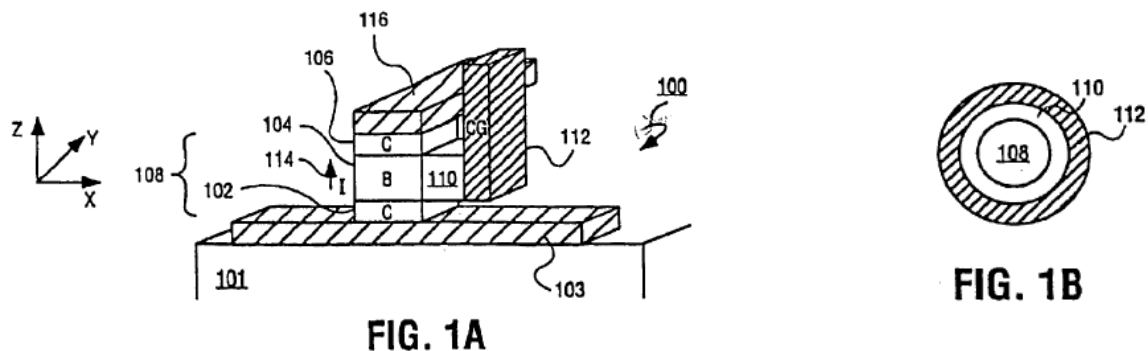
116. The important thing to understand about this first preferred embodiment is that the channel region of the TFT transistor that makes up the non-volatile memory cell is labelled 4019 and the source and drain regions are labelled 4017. This means that the channel and the current flow through the channel are horizontally oriented. Neither the memory cells nor the transistors within them are

vertically oriented. Though this first preferred embodiment, shown in implied form in Figure 35, does show an insulating layer above the monocrystalline substrate, it does not disclose the claimed vertically oriented memory cells found in the claims of the '702 Patent.



Ex. 1007 (Lee), Figure 42.

117. Further, for the purposes of asserting that the vertically oriented semiconductor memory cells of element 13[b] are found in Lee, the Petition identifies the embodiment of Figure 1A. Petition, pp. 48-49; Ex. 1007 (Lee), Figures 1A, 1B, 8:17-23, 14:10-31.



Ex. 1007 (Lee), Figures 1A, 1B.

118. However, this embodiment shows a “first input/output (I/O) 103 conductor formed on or above a plane (x-y) of a single crystal substrate 101.” Ex. 1007 (Lee), 14:15-16. There is no disclosure in the figure or the text of electrical devices formed in the substrate or of a dielectric layer disposed above the electrical devices in the substrate. This embodiment cannot by itself anticipate or render obvious the elements of Claim 13.

119. The Petition tries to solve this issue by juxtaposing this embodiment with the embodiment of Figure 35 in its analysis of Ground 3 (Lee) with regard to element 13[b]. Petition, pp. 49-50. The Petition states that “[b]ecause Lee discloses ‘a three dimensional nonvolatile memory array, comprising a plurality of vertically separated device levels,’ in which ‘each level compris[es] an array of TFT EEPROMs,’ the memory array is a stackable add-on layer having a plurality of vertically oriented semiconductor memory cells.” Petition, p. 50. But Petitioners fail to understand that Lee calls the memory cell of Figure 1A a pillar device, while the

term TFT EEPROM refers to a horizontally oriented memory cell of, for example, Figures 42-44. Ex. 1007 (Lee), Figures 42-44, 30:53-31:37, 31:38-40.

120. Merely referring to two embodiments from one reference in adjacent paragraphs is not sufficient to articulate a formal combination of those embodiments. Here Petitioners have failed to meet their burden with regard to the combination of multiple embodiments of Lee in an attempt to show that Lee by itself or in conjunction with other references anticipates or renders obvious any of the Claims 13-17.

121. This same type of error is made again with respect to Element 13[c] in the analysis of Ground 3 (Lee). Petition, pp. 50-52. In trying to show this element in Lee, Petitioners have juxtaposed a description of the embodiment of Figure 35 with a description of the embodiment of Figure 83A, thereby attempting to show a stackable add-on-layer being bonded to the dielectric layer. However, again, this analysis fails because the memory cells depicted in Figure 83A are horizontally oriented (the source, channel and drain of each of the floating gate transistors are all at the same level). This presumed and unmotivated combination of two distinct embodiments of Lee cannot anticipate or render obvious Claim 13 because it does not disclose the necessary vertically-oriented memory cells.

122. Throughout the Petition, Petitioners have failed to meet their burden with respect to combining separate embodiments from within a single reference by

failing to articulate any motivation for the combination and to explain how the combination would render obvious all the relevant elements of a claim in question.

C. Ground 3: Claims 13-15 Are Not Obvious Over Lee

123. Petitioners claim that Claims 13 through 15 are disclosed by Lee alone. Petition, p. 46 (“the subject matter of independent Claim 13 and dependent Claims 14 and 15 is disclosed by Lee alone”). I disagree, as explained below.

124. As a preliminary matter, this first sentence of Section VII.C of the Petition is at odds with the heading of Section VII.C and the analysis that follows. The former asserts that Lee anticipates Claims 13-15 of the ’702 patent. The section title indicates that Lee in view of the knowledge of a POSITA renders these claims obvious. The standards for proving these two assertions are different.

125. On five occasions within the analysis of Ground 3, Petitioners invoke that “a POSITA would have understood” (or the comparable “a POSITA would have found”) to find elements of the claims in question where no explicit disclosure of the item exists within Lee. Petition, pp. 47, 52, 57. In this case, Petitioners’ reliance on the knowledge of a POSITA is not only misguided but clearly takes their argument outside the bounds of anticipation of Claim 13 by Lee alone.

126. Section VII.C.2 of the Petition argues that Figure 35 of Lee and the associated description discloses a substrate having electrical devices formed herein, and further having a dielectric layer disposed above the electrical devices, i.e.

Element 13[a]. Petition, pp. 47-48. But as explained above (§§ 115-116), the entire first preferred embodiment that Figure 35 is a part of does not include the claimed vertically oriented semiconductor memory cells claimed in element 13[b]. To find these cells, the Petition looks to Figure 1A of Lee. Petition pp. 48-49. Thus, again, merely referring to two very different embodiments from one reference is not sufficient to articulate a formal combination of those embodiments for the purposes of showing obviousness. Petitioners have failed to meet their burden to show that Lee by itself renders obvious Element 13[a], Claim 13, or any of the claims dependent on Claim 13.

127. With regard to Element 13[c], the Petition similarly suggests that Lee alone discloses a “stackable add-on layer being bonded to the dielectric layer.” Petition, pp. 50-52. But again, as explained above (§ 121) Petitioners have juxtaposed the embodiment of Figure 35 with the embodiment of Figure 83A without explaining why these embodiments are combinable. In particular, the memory cells of the embodiment of Figure 83A are horizontally oriented. Consequently the presumed combination of these embodiments of Lee cannot disclose or render obvious Element 13[c], Claim 13, or any of the claims dependent on Claim 13.

D. Ground 4: Claims 16 and 17 Are Not Obvious Over Lee in View of Endoh

128. As a preliminary matter, Claims 16 and 17 depend on Claim 13. Ground 4 does not attempt to address the deficiencies of Ground 3 with respect to the non-obviousness of Claim 13 over Lee. The petition looks to Endoh only for the purposes of adding Endoh’s NAND architecture and Endoh’s serially connected memory cells. Petition, p. 63 (“Thus, a POSITA would have found it obvious to modify Lee’s pillar structure to use the NAND architecture and a serial connection as taught by Endoh.”). However, as explained above (§§ 106-122), the Petition’s disclosed motivation to combine Lee and Endoh is severely flawed for the same reasons that the combination of Lee, Watanabe and Endoh is flawed.

129. In particular, the idea that “a POSITA would have found it obvious to modify Lee’s pillar structure to use the NAND architecture and a serial connection as taught by Endoh” is flawed because the pillars of Lee’s Figure 12B are well suited to Lee’s NOR VGA memory array architecture but not at all appropriate to implement a NAND memory. Petition, pp. 62-63. This is because in Lee’s physical structure all the memory cell transistors share the same control gate 1200. Ex. 1007 (Lee), 8:55-57, 20:44-54. But this can’t work in a NAND memory array because in a NAND memory array, each transistor in a stack has to have a different control gate signal. Ex. 1006 (Endoh), Figure 65, ¶ [0258]. Applying different voltages to the

control gates of the various transistors in a string stack is central to the read, program and erase operations of NAND memory—none of which would be possible with Lee’s vertical configuration of Figure 12B. Ex. 1006 (Endoh) ¶ [0257]. The suggestion that a POSITA would have found it obvious to modify Lee’s pillars to implement a NAND memory array vastly oversimplifies the changes that would be necessary.

130. Juxtaposing the circuit diagram for a NOR Flash memory array as implemented in Lee’s cited embodiments with a NAND Flash memory array clarifies the incompatibility of the two.

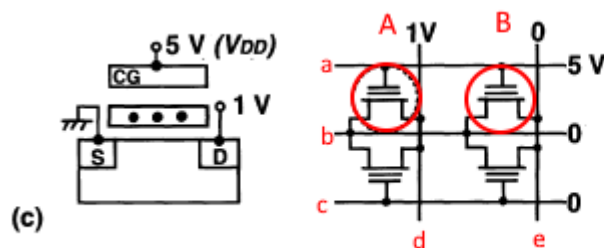
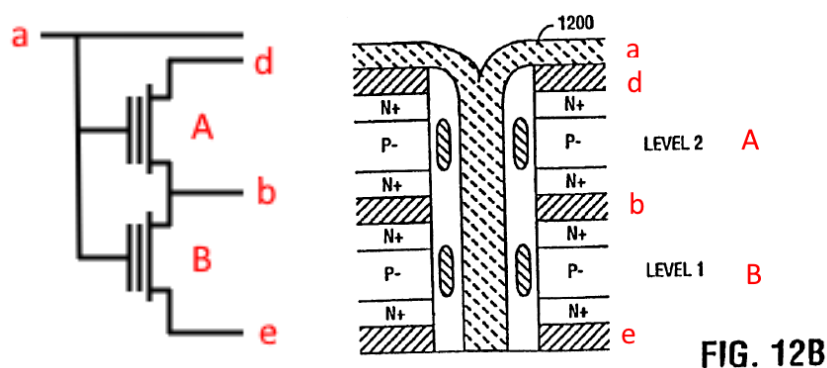


Fig. 1.33. The basic operation of the NOR cell [1.9]. (a) Erase; (b) write; (c) read

Ex. 2036 (VLSI Memory Chip Design), p. 39, Figure 1.33(c), annotated.

131. The schematic of this NOR memory array can be rearranged and placed beside Figure 12B of Lee to show how these two are equivalent:



Ex. 2036 (VLSI Memory Chip Design), p. 39, Figure 1.33 rearranged; Ex. 1007 (Lee), Figure 12B, annotated.

132. These two NOR Flash memory cells comprising floating gate transistors A and B respectively are not connected in series because in operation either transistor A or transistor B is operable at a given time and current does not ever flow from line d to line e through both transistors A and B. Instead, current flows between line d or line e to line b according to the voltages on their respective gates, which include the voltage of the control gate and the charge on the floating gate. Ex. 2036 (VLSI Memory Chip Design), pp. 38-40.

133. This structure of a vertical stack of memory cells controlled by a common control gate is found in multiple embodiments of Lee. Each of Figures 12B, 25A and 27A show a pair of NOR FLASH memory cells atop one another and in all three cases, the control gates of the vertically aligned transistors are controlled by the same conductive material in the volume between the vertical structures.

134. The symbology of the figures of Lee is clear and consistent. The fine diagonal hashing of the structures above and below and between the two illustrated levels are conductors. They form the wires that connect the source and drains of the two transistors (marked A and B above) with the rest of the memory array and the peripheral circuitry necessarily around the perimeter of the memory array. Lee's Virtual Ground Array arrangement necessarily connects the node between the two transistors. This is illustrated in Figure 1.28 of Ex. 1009 (Basics of Non-Volatile Semiconductor Memory Devices), as explained on p. 34.

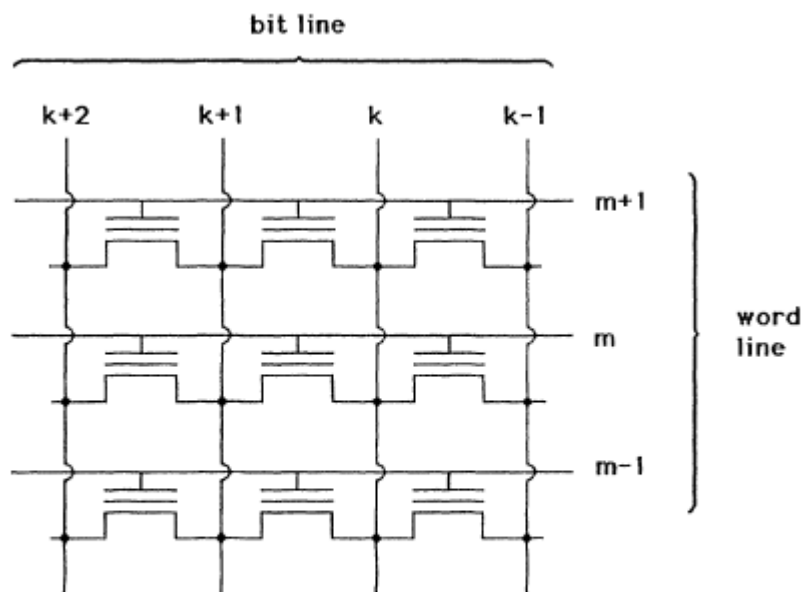


Figure 1.28 The virtual ground array architecture [1.70, 1.73, 1.74]. In this architecture, the common ground line in the array, as well as the drain contact in each memory cell, is eliminated.

Ex. 1009 (Basics of Non-Volatile Semiconductor Memory Devices), p. 35,
Figure 1.28.

135. In Lee, the conductors at the top and bottom of each vertically-oriented memory cell are oriented perpendicularly to each other, as illustrated in Figure 9B, which also shows the cross hatched metal wire 900 and 906. Ex. 1007 (Lee), 19:32 ("first I/O conductor 900"), 19:37 ("the second I/O 906"), 19:31-44 ("In this way, a pillar 908 is formed at the intersection of the first and second I/O's."). The same cross-hatching is used to illustrate conductors above and below the transistors in Figures 1, 2, 3, 4, 5, 6, 7, 8, 9, 13, 14, 15, 16 and so on. Many of these, such as Figure 25A, shows a comparable structure with identical hash marks but with M1 and M2 labelled. In the text, these layers are referred to as just conductors and in other cases (such as 204 in Figures 2 and 3) they are specifically referred to as being made of metal. Ex. 1007 (Lee), 15:33-35, 17:18.

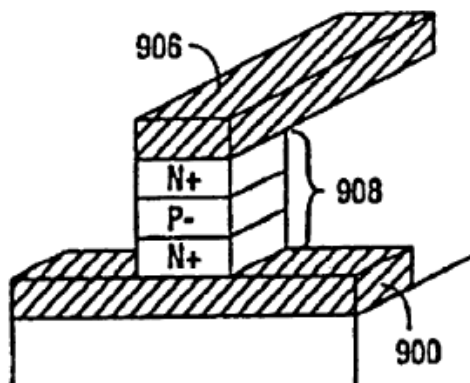
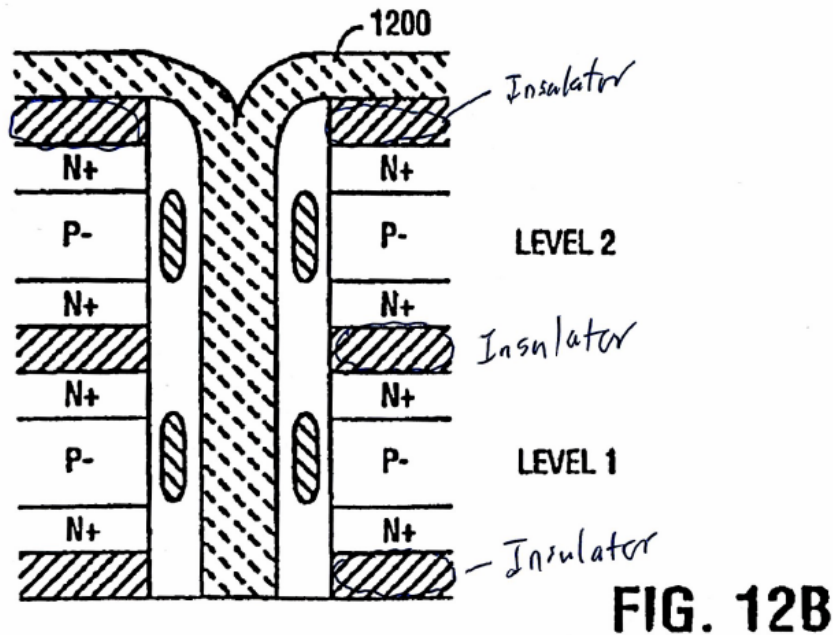


FIG. 9B

Ex. 1007 (Lee), Figure 9B.

136. As an aside, in his deposition, Petitioners' expert mischaracterized the teachings of Lee and of Figure 12B in particular. His mistaken understanding was that the cross hatched regions above and below the Level 1 and Level 2 transistors indicated insulators and that removing that middle "insulator" would transform the illustration of Figure 12B into to a NAND architecture. Ex. 2025 ('702 Patent Fig. 12b annotated by Petitioners' expert); Ex. 2026 ('702 Patent Fig. 12b annotated by Petitioners' expert); Ex. 2028 (Lee Deposition), 81:3-82:6. I disagree.



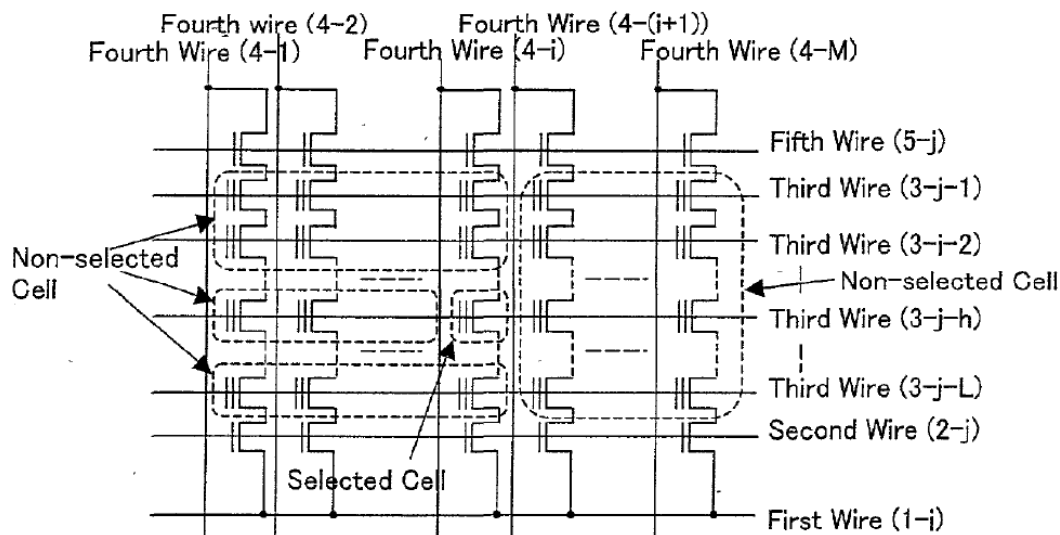
Ex. 2025 ('702 Patent Fig. 12B annotated by Petitioners' expert).

137. First of all, the layer he suggests removing is not an insulator but is the virtual ground connection of the two memory cells of the Virtual Ground Array. Removing it does not accomplish the change he suggests. The fact that the control gates on the first and second layer memory cells would still be the same means that

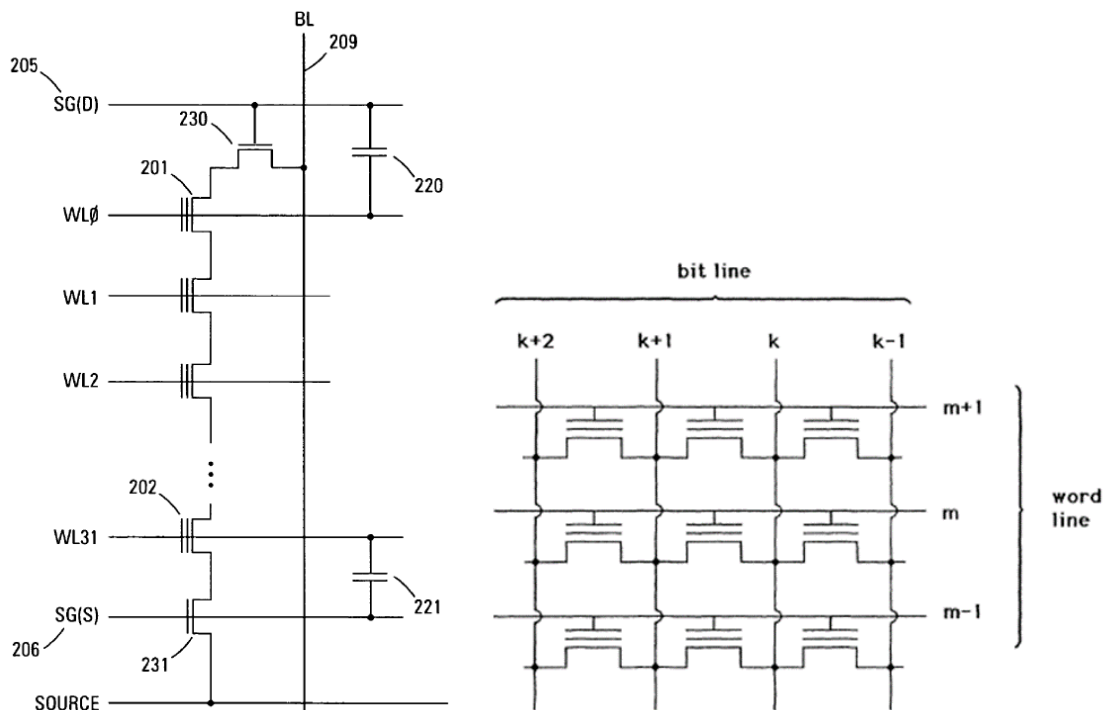
one cannot independently access or program the two memory cells. It would not be operable as a portion of a NAND memory array that would satisfy the requirements of Claim 16. Ex. 2028 (Lee Deposition) 93:16-96:20. Lee's complex interconnection of up to 4 transistors per level per pillar with bit lines traversing the arrays in orthogonal wires in M1 and M2 (and higher levels of metal in embodiments with additional levels of memory cells) which shared control gate signals across pillars and levels is pervasively a NOR VGA structure that is not simply transformed into a NAND organization.

138. Thus, what is clear is that this pillar structure of Figure 12B of Lee with its shared control gates (Ex. 1007 (Lee), 20:23-54) is not compatible with any implementation of a NAND Flash or EEPROM memory array. As illustrated in Figure 65 of Endoh and Figure 2 of Ex. 1012 (Nguyen), the memory cell transistors in a NAND Flash memory array are connected serially, and each transistor in such a string of transistors must have its own distinct control gate signal separate from those of the other transistors in the string. This aspect is vital for the read, program and erase functions to operate properly in this memory array. Ex. 1006 (Endoh), Figures 65, 67, 78, 79, 80, 84, ¶¶ [0255]-[0277].

Fig. 65



Ex. 1006 (Endoh), Figure 65 (partial).



Ex. 1012 (Nguyen), Figure 2 (NAND string); Ex. 1009 (Basics of Non-Volatile Semiconductor Memory Devices), p. 35, Figure 1.28 (NOR VGA array).

139. There is no connection to the nodes connecting the sources and drains of adjacent memory cell transistors in each string. All of the current in a string must flow through all of the transistors in the string. In other words, all of the memory cells in the string of a NAND flash/EEPROM memory array must be connected in series.

140. To change Lee's vertical VGA NOR memory device of Figure 12B into a NAND memory device with a vertical NAND structure as found in Endoh would involve a wholesale change of every aspect of the device—every physical, structural, electrical, and logical aspect would have to be completely redone. Specifically, Lee's pillar structures of Figure 12B would have to be modified to change the control gate structures to provide separate control gate signals for each memory cell in each level of the structure and include routing paths for each of those control gates. In addition, the NAND memory array has bit lines (i.e. data lines) (the "fourth wires" of Figure 65) that distinct from the strings that have no counterpart in a NOR memory array. In the NOR memory array, the data flow is along the wires (labelled "b" in the annotated version of Figure 1.33 above) that run parallel to the control gate signals (labelled "a" and "c", above).

141. Also, because the read, program, and erase procedures are closely coupled to the specific type and configuration of the memory array, the peripheral circuitry which includes the sense amplifiers, address decoders, and voltage

generators and control logic and sequencers are different between those of a NOR flash/EEPROM memory array as found in Lee's Figure 12B, and those interfacing with a NAND flash/EEPROM memory array as found, for example, in Endoh's Figure 65. Ex. 1006 (Endoh) ¶¶ [0255]-[0277]; Ex. 1007 (Lee), 31:1-32; Ex. 2036 (VLSI Memory Chip Design), Figure 1.33, pp. 38-40. NAND and NOR devices also have different exterior interfaces and command paradigms, meaning that these aspects of the memory devices would also have to change. Consequently, if an attempt were made to modify, for example, Lee's Figure 12B embodiment the Petition relies on into a NAND flash design, there would be no combination, just a replacement of Lee's device with a completely different NAND flash design. This would not be an inconsequential change as suggested by the Petition. The wholesale redesign of Lee's embodiment to change them from a NOR flash design to a NAND device would be massive and complicated and complete; and in no way an obvious modification of Lee or its Figure 12B embodiment to a POSITA.

142. Lee states "the memory array may also be arranged in non volatile flash memory architectures other than VGA." Ex. 1007 (Lee), 40:4-23. But it is clear from the above explanation that when Lee talks about other flash memory architectures he is referring to the other varieties of NOR-type Flash devices mentioned there (e.g. DuSNOR, but not NAND devices. Ex. 1007 (Lee), 31:18-37, 40:4-23.

143. In summary, Petitioners’ principal conclusion with respect to Ground 4 is that “[a] POSITA would have been motivated to combine Lee with Endoh’s teachings of a serial connection.” Petition, p. 64. They are not suggesting a replacement of Lee’s pillar structure or of any other wires of peripheral circuitry, just using Lee’s pillars with a serial connection. But as explained above, it is not possible to just change the connection configuration of the memory cells in Lee’s stack and have the device continue to operate. The changes that would be required by such a change would be pervasive across the entire memory device, to the point where it would not be obvious to a POSITA to attempt such a change.

E. Ground 1: Claim 13 Is Not Obvious Over Watanabe

144. Similar to the discussion above (¶¶ 123-127) with respect to Ground 3 based on Lee alone, here in Ground 1 Petitioners alternate between an obviousness argument and statements that suggest anticipation of Claim 13 by Watanabe alone. Petition, p. 15 (“A POSITA would have understood ...”, “A POSITA would have recognized ...”). Regardless, Watanabe neither anticipates nor renders obvious Claim 13 of the ’702 patent.

145. Specifically, with regard to Element 13[c] (“the stackable add-on layer being bonded to the dielectric layer”), the Petition states that both the embodiment of Figure 6 (the “stacking method”) and the embodiment of Figure 5

(“the lamination method”) disclose or render obvious this element. Petition, pp. 21-24.

146. With regard to Watanabe’s “stacking method” and as explained above (¶¶ 65-81), the disclosure in Watanabe would not motivate a POSITA to use Watanabe’s stacking method because a POSITA in 2004 would have understood that it would not work and would not have had a reasonable likelihood of success. Therefore this embodiment also does not disclose or render obvious Element 13[c] nor Claim 13 generally.

F. Ground 2: Claims 14-17 Are Not Obvious Over Watanabe in View of Endoh

147. As a preliminary matter, Claims 14-17 depend on Claim 13. Ground 2 does not attempt to address the deficiencies of Ground 1 with respect to the non-obviousness of Claim 13 over Watanabe. The Petition looks to Endoh only for the purposes of adding Endoh’s alternate disclosure of Claim 14’s and Claim 15’s vertically-oriented non-volatile memory cells on an SOI pillar with either a floating gate or a charge-trapping gate insulator (Petition, pp. 31, 33, 35-36, 37), and of Claim 16’s and Claim 17’s NAND memory array with its serially connected memory cells (Petition, pp. 39-40). These citations do not address the deficiencies of Watanabe with regard to Claim 13 (see ¶¶ 144-146).

148. Further the attempt to combine Endoh's NAND memory array with Watanabe's embodiments of Figure 5 or 6, would fail for the same reasons that Endoh's NAND memory array is incompatible with Lee's embodiments, including Figure 12B relied on in the Petition, as explained above (¶¶ 106-122, 128-143)—the memory cells of Watanabe that are vertically aligned share the same control gate and this is incompatible with any NAND memory array, such as that of Endoh's Figure 65. Therefore the Petition's attempt to show that Claims 16 and 17 are rendered obvious by the combination of Watanabe and Endoh necessarily fails because such a combination is unworkable in the context of Watanabe's fundamental disclosures.

XII. CONCLUSION

149. Based on the foregoing analysis, it is my opinion that Petitioners have failed to establish by a preponderance of the evidence that the Challenged Claims of the '702 Patent are unpatentable over the cited references.

150. In signing this Declaration, I recognize that the Declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I also recognize that I may be called upon to testify in deposition or before the Patent Trial and Appeal Board. If called upon to testify, I would testify truthfully and competently to all matters stated in this Declaration.

151. I reserve the right to supplement my opinions in the future to respond to any arguments that Petitioners raise and to take into account new information as it becomes available to me.

152. I hereby declare that all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true and that such statements are made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: February 15, 2024


Steven A. Przybylski