# INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

## 2007 EDITION

## INTERCONNECT

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# INTERCONNECT

## SCOPE

The *Interconnect* chapter of the 1994 National Technology Roadmap for Semiconductors (NTRS) described the first needs for new conductor and dielectric materials that would be necessary to meet the projected overall technology requirements. With the publication of the 1997 edition of the NTRS, the introduction of copper-containing chips was imminent. The 1999 International Roadmap for Semiconductors (ITRS) emphasized an ongoing change to new materials that were being introduced at an unprecedented pace. The 2001 ITRS described continued new materials introductions and highlighted the problem of increases in conductor resistivity as linewidths approach electron mean free paths. The slower than projected pace of low-κ dielectric introduction for microprocessors (MPUs) and application-specific ICs (ASICs) was one of the central issues for the 2003 ITRS Interconnect area. The 2005 ITRS shows the calculated electron scattering induced Cu resistivity rise for future technology generations, as well as the resultant effect on resistance and capacitance (RC) performance metrics. A new crosstalk metric is also introduced. The technical product driver for the smallest feature size remains the dynamic random access memory chip (DRAM); however, the Metal 1 pitch for MPUs is expected to equal that of DRAM by 2010. In recognition of the increasing importance of the dynamic power dissipated in the interconnect structure, a new power metric is included in the MPU and ASIC Technology Requirements Tables. The power metric is the power (measured in Watts) dissipated per GHz of frequency and $cm^2$ of metal layer. Although the power metric is seen to plateau for the long-term years due to aggressive introduction of low-κ dielectrics, the power dissipated in the interconnect structure will still increase dramatically due to higher frequencies and increases in the number of metal layers. The capacitance per unit length for Metal 1, intermediate, and minimum global wiring layers has also been added to the MPU and ASIC Technology Requirements Tables. The Cu resistivity of these layers had been added in prior years and, with the addition of capacitance, the RC values can easily be calculated.

Managing the rapid rate of materials introduction and the concomitant complexity represents the overall near-term challenge. For the long term, material innovation with traditional scaling will no longer satisfy performance requirements. Interconnect innovation with optical, radio frequency (RF), or vertical integration combined with accelerated efforts in design and packaging will deliver the solution.

The function of an interconnect or wiring system is to distribute clock and other signals and to provide power/ground, to and among, the various circuits/systems functions on a chip. The fundamental development requirement for interconnect is to meet the high-speed transmission needs of chips despite further scaling of feature sizes.

Although copper-containing chips were introduced in 1998 with silicon dioxide insulators, the lowering of insulator dielectric constant indicated by the ITRS has been problematic. Fluorine doped silicon dioxide ($\kappa = 3.7$) was introduced at 180 nm, however insulating materials with $\kappa = 2.7–3.0$ were not widely used until 90 nm. The reliability and yield issues associated with integration of these materials with dual damascene copper processing proved to be more challenging than expected. The integration of porous low-κ materials is expected to be even more challenging. Since the development and integration of these new low-κ materials is rather time invariant, the anticipated acceleration of the MPU product cycle (two versus three years until 2009) will shift the achievable κ to later technology generations. The various dielectric materials that are projected to comprise the integrated dual damascene dielectric stack for all years of the roadmap are depicted in the Dielectric Potential Solutions figure. The range of both the bulk κ values and effective κ values for the integrated dielectric stack are listed in the Technology Requirements tables. The introduction of these new low dielectric constant materials, along with the reduced thickness and higher conformality requirements for barriers and nucleation layers, is a difficult integration challenge. (For a more thorough explanation, the Appendix illustrates the calculation of the effective κ for various integration schemes.)

The conductor, barrier, and nucleation potential solutions have been grouped into sections for local, Metal 1, intermediate, and global wiring levels, as well as passive devices. Atomic layer deposition (ALD), characterized by excellent conformality and thickness control, is still receiving attention for applications in the deposition of conductors, barriers, nucleation layers and high-κ dielectric materials. The Cu resistivity rise due to electron scattering effects poses a critical challenge even in the near term, and is also an area of focus. Characterization shows significant contributions to resistivity by scattering from both grain boundaries and interfaces. Research to date has not identified any solutions that would have a large impact on this phenomenon.

The Planarization Potential Solutions section has been divided into sections for planarization of conductors and insulators. One of the primary integration challenges with low-κ materials is adhesion failure between barrier or capping materials


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and the dielectric during the planarization process. Porous low-κ materials are even more problematic and are therefore one of the key focus areas for planarization development efforts.

In the area of Etch Potential Solutions, dielectric etch challenges will still be dominant in logic technology where a variety of inorganic, organic, or hybrid materials will be used to meet $\kappa_{eff}$ requirements. It is expected that continuous improvement of existing source technologies will provide the solutions needed for the future scaling of CMOS logic and DRAM technology as well as new emerging classes of non-volatile memory devices, *i.e.,* PRAM, MRAM, and FeRAM, Interconnect Surface Preparation Potential Solutions includes post-etch photoresist stripping, post-strip residue removal, post-chemical mechanical polishing (CMP) cleaning for dielectrics and metals, pre-deposition cleaning for dielectrics and metals and post-deposition cleaning for dielectrics and metals. Interconnect structures based on copper and ultra low-κ materials continue to present difficult surface conditioning challenges. For example, etch-induced sidewall damage will increase κ and must be minimized. Post-etch resist strip has also been shown to cause damage to low-κ materials with a resultant increase in the effective κ of the structure.

## DIFFICULT CHALLENGES

Table INTC1 highlights and differentiates the five key challenges in the near term (≥ 22 nm) and long term (< 22 nm). In the near term, the most difficult challenge for interconnect is the introduction of new materials that meet the wire conductivity requirements and reduce the dielectric permittivity. In the long term, the impact of size effects on interconnect structures must be mitigated.

Future effective κ requirements preclude the use of a trench etch stop for dual damascene structures. Dimensional control is a key challenge for present and future interconnect technology generations and the resulting difficult challenge for etch is to form precise trench and via structures in low-κ dielectric material to reduce variability in RC. The dominant architecture, damascene, requires tight control of pattern, etch and planarization. To extract maximum performance, interconnect structures cannot tolerate variability in profiles without producing undesirable RC degradation. These dimensional control requirements place new demands on high throughput imaging metrology for measurement of high aspect ratio structures. New metrology techniques are also needed for in-line monitoring of adhesion and defects. Larger wafers and the need to limit test wafers will drive the adoption of more *in situ* process control techniques. Dimensional control, a challenge now, will become even more critical as new materials, such as porous low-κ dielectrics and ALD metals, play a role at the tighter pitches and higher aspect ratios (A/R) of intermediate and global levels.

*Table INTC1 Interconnect Difficult Challenges*

| *Difficult Challenges ≥ 22 nm* | *Summary of Issues* |
|---|---|
| Introduction of new materials to meet conductivity requirements and reduce the dielectric permittivity* | The rapid introductions of new materials/processes that are necessary to meet conductivity requirements and reduce the dielectric permittivity create integration and material characterization challenges. |
| Engineering manufacturable interconnect structures, processes and new materials* | Integration complexity, CMP damage, resist poisoning, dielectric constant degradation. Lack of interconnect/packaging architecture design optimization tool |
| Achieving necessary reliability | New materials, structures, and processes create new chip reliability (electrical, thermal, and mechanical) exposure. Detecting, testing, modeling, and control of failure mechanisms will be key. |
| Three-dimensional control of interconnect features (with it's associated metrology) is required to achieve necessary circuit performance and reliability. | Line edge roughness, trench depth and profile, via shape, etch bias, thinning due to cleaning, CMP effects. The multiplicity of levels combined with new materials, reduced feature size, and pattern dependent processes create this challenge. |
| Manufacturability and defect management that meet overall cost/performance requirements | As feature sizes shrink, interconnect processes must be compatible with device roadmaps and meet manufacturing targets at the specified wafer size. Plasma damage, contamination, thermal budgets, cleaning of high A/R features, defect tolerant processes, elimination/reduction of control wafers are key concerns. Where appropriate, global wiring and packaging concerns will be addressed in an integrated fashion. |



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*Table INTC1 Interconnect Difficult Challenges (continued)*

| *Difficult Challenges < 22 nm* | *Summary of Issues* |
|---|---|
| Mitigate impact of size effects in interconnect structures | Line and via sidewall roughness, intersection of porous low-κ voids with sidewall, barrier roughness, and copper surface roughness will all adversely affect electron scattering in copper lines and cause increases in resistivity. |
| Three-dimensional control of interconnect features (with it's associated metrology) is required | Line edge roughness, trench depth and profile, via shape, etch bias, thinning due to cleaning, CMP effects. The multiplicity of levels, combined with new materials, reduced feature size and pattern dependent processes, use of alternative memories, optical and RF interconnect, continues to challenge. |
| Patterning, cleaning, and filling at nano dimensions | As features shrink, etching, cleaning, and filling high aspect ratio structures will be challenging, especially for low-κ dual damascene metal structures and DRAM at nano-dimensions. |
| Integration of new processes and structures, including interconnects for emerging devices | Combinations of materials and processes used to fabricate new structures create integration complexity. The increased number of levels exacerbate thermomechanical effects. Novel/active devices may be incorporated into the interconnect. |
| Identify solutions which address 3D structures and other packaging issues* | 3 dimensional chip stacking circumvents the deficiencies of traditional interconnect scaling by providing enhanced functional diversity. Engineering manufacturable solutions that meet cost targets for this technology is a key interconnect challenge. |

** Top three challenges*

*CMP—chemical mechanical planarization* *DRAM—dynamic random access memory*

At < 22 nm, feature size effects, such as electron scattering from grain boundaries and interfaces, will continue to increase the effective Cu resistivity. Ultra low-κ dielectrics may be replaced by air gaps in selective areas. Coping with the thermal and mechanical implications of these changes is a key challenge.

Feature size reduction, new materials, and damascene structures are all challenges to on-chip metrology capability for interconnect development and manufacture. Critical dimension (CD) measurements are needed for very high aspect ratio features and ultra-thin barriers. Methods must be developed to accommodate the increased complexity of the wiring levels of future chips. Other metrology challenges include measuring resistivity and dielectric constant at high frequency, adhesion, and mechanical properties.

Three-dimensional chip stacking through the use of high density through silicon vias (TSV) is a key focus area for improving delay and power and providing increased functional diversity chip assemblies. Developing manufacturable and cost- effective solutions for these 3D IC processes is a key interconnect challenge.

## TECHNOLOGY REQUIREMENTS

To adequately describe the wiring needs of interconnect, near term (2007–2013) and long term (2014–2022) technology requirements and potential solutions are addressed for two specific classes of products: Logic (MPUs and ASICs) and DRAM. For MPUs, Metal 1, intermediate, and global wiring pitches/aspect ratios are differentiated to highlight a hierarchical scaling methodology that has been broadly adopted. The 2007 roadmap recognizes an acceleration of MPU product introduction to a two-year cycle for the next technology generation (2009) and reversion to a three-year cycle after 2009. It also projects that the Metal 1 pitch for MPUs will become equivalent to that of DRAM in 2010. In addition, there is now no difference in pitch between the MPU Metal 1 and intermediate wires. MPU Metal 1 "contacted pitch" refers to wires with staggered rather than side-by-side contacts. The use of staggered contacts has been the standard MPU design methodology for quite some time.

The accelerated scaling of MPU pitch has aggravated the copper electromigration problem. $J_{max}$ limits for current dielectric cap technologies for copper will be exceeded by 2013. Modification of the Cu surface to form CuSiN or use of alloys such as Cu-Al can yield significant electromigration improvements. Implementation of a selective metal cap technology for copper, such as CoWP, will result in even higher electromigration capability. However, there is still concern about yield loss due to metal shorts caused by these selective processes. Improved dielectric caps are also being explored.


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Electron scattering models have been improved and can now predict the Cu resistivity rise as a function of line width and aspect ratio. There is a significant contribution to the increase in resistivity from both grain boundary and interface electron scattering as shown in Figure INTC1. To date, research has not identified any potential solutions to this problem.

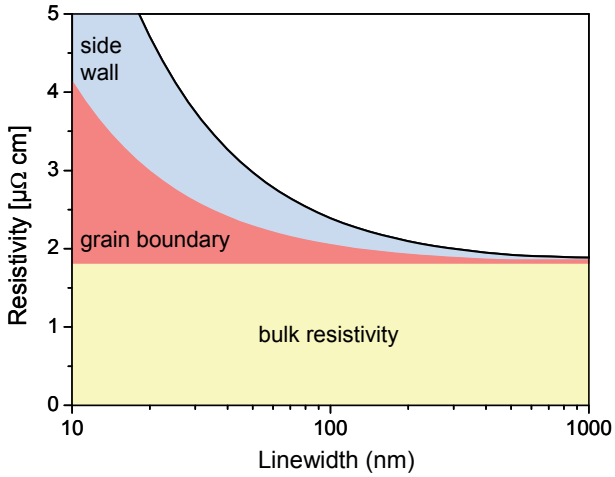


*Figure INTC1 Cu Resistivity*

Accordingly, Cu resistivity numbers for minimum Metal 1, intermediate and global wires are now listed for all the years of the roadmap. The effect of this resistivity increase on the RC performance metrics is also calculated and included in the technology requirements table. Three-dimensional control of critical dimension (3DCD) interconnect features has been listed as one of the critical challenges in several editions of the ITRS. The total variability of M1 wire resistance due to CD variation and scattering has been calculated and is also included in the MPU technology requirements table. Since the length of Metal 1 and intermediate wires usually shrinks with traditional scaling, the impact of their delay on performance is minor. Global interconnects, which have the greatest wire lengths, will be impacted most by the degraded delay. The benefit of materials changes or some amelioration of the Cu resistivity rise will be insufficient to meet overall performance requirements. The trend toward multi-core MPU design has alleviated some of the delay issues associated with ever increasing lengths of global interconnects

In the long term, new design or technology solutions (such as 3D IC, optical or carbon nanotubes) will be needed to overcome the delay, power, and bandwidth limitations of traditional interconnects. Refer to section on "New Interconnect Concepts and Radical Solutions." Inductive effects will also become increasingly important as the operating frequency increases, and additional metal patterns or ground planes may be required for inductive shielding. As supply voltages are scaled or reduced, crosstalk becomes an issue for all clock and signal wiring levels. A crosstalk metric was introduced in the 2005 ITRS for Metal 1, intermediate and minimum global wires. The metric calculates the line length where 25% of the switching voltage is induced on a minimum pitch victim wire. This critical line length for a minimum global wire in 2022 is less than 30% of the line length in 2007. Therefore joint efforts with the design community are needed to address crosstalk issues. In recognition of the increasing importance of dynamic power, a Power Metric and wire capacitance values were introduced in 2006 and have been updated for 2007. The 2007 Roadmap continues to reflect the ongoing reduction of dielectric constant for future technology generations as new porous low-κ dielectric materials and eventually air gap technology are introduced.

### *MPU Cross Section*

MPUs utilize a high number of metal layers with a hierarchical wiring approach of steadily increasing pitch and thickness at each conductor level to alleviate the impact of interconnect delay on performance. Refer to Figure INTC2.

To accommodate the need for ground planes or on-chip decoupling capacitors, the growth of metal levels is projected to increase beyond those specified solely to meet performance requirements.



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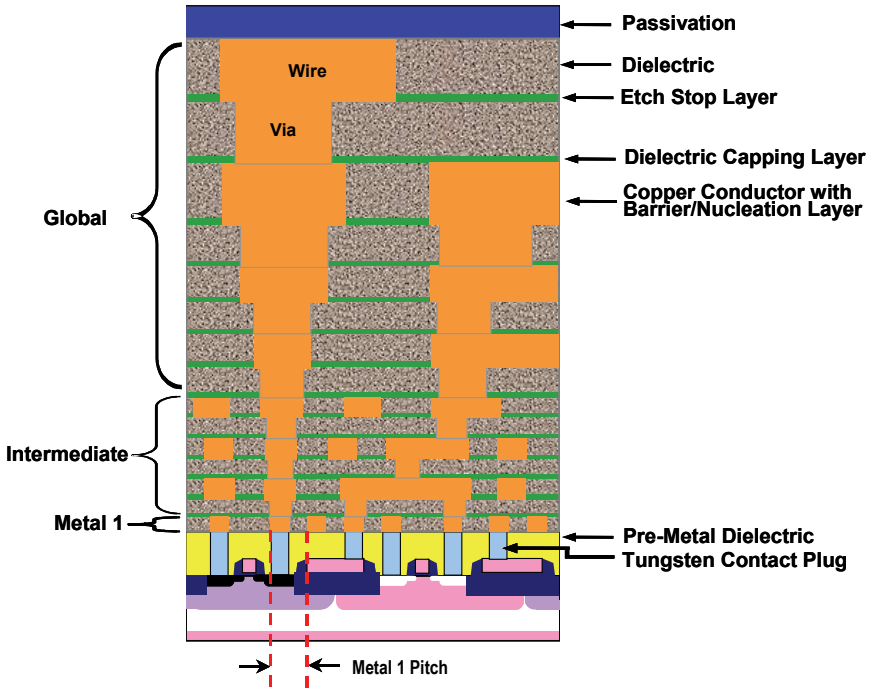


*Figure INTC2 Cross-section of Hierarchical Scaling—MPU Device*

### ASIC Cross Section

ASICs share many of the technology attributes of MPUs, for example, Cu wiring and low-κ dielectrics. ASIC design methodology is generally more regular, consisting of Metal 1, intermediate, semi-global (2× intermediate) and global (4× intermediate) wire pitches. An ASIC only, semi-global wiring pitch has been added to the MPU technology requirements table in 2005. A typical ASIC cross-section is shown in Figure INTC3 below.

Historically, DRAM interconnect technology reflected the most aggressive metal pitch and highest aspect ratio contacts; however, the MPU Metal 1 pitch is projected to equal that of DRAM in 2010. The introduction of low-κ dielectric materials (fluorinated silica glass (FSG)) is underway and the change from aluminum to copper at the 65 nm half pitch is occurring.

Damascene processing flows dominate MPU/ASIC fabrication methodologies and usage in DRAM is expected to broaden. Figure INTC4 illustrates several typical interlevel dielectric (ILD) architectures used in the creation of interconnect wiring levels. While current copper damascene processes utilize physically vapor deposited (PVD) Ta-based barriers and Cu nucleation layers, continued scaling of feature size requires development of other materials and nucleation layer deposition solutions. Continuous improvement of tools and chemistries will extend electrochemically deposited (ECD) Cu to the end of the forecasted roadmap (2022) but small, high A/R features necessitate the simultaneous development and subsequent selection of alternative filling techniques. A thin barrier is also needed to maintain the effective conductor resistivity in these features. Nucleation layer conformality requirements become more stringent to enable Cu ECD filling of damascene features. Surface segregated, chemical vapor deposition (CVD), ALD, and dielectric barriers represent intermediate potential solutions; zero thickness barriers are desirable but not required.

Near-term dielectric needs include lower permittivity materials for wire insulators and etch stops, higher permittivity materials for decoupling and metal-insulator-metal (MIM) capacitors and materials with high remnant polarization for ferroelectric memories. The thermal, mechanical, and electrical properties of these new materials present a formidable challenge for process integration. In the longer term, dielectric characteristics at high frequency will become more important, and optical materials will be required which have sufficient optical contrast to serve as low-loss waveguides.


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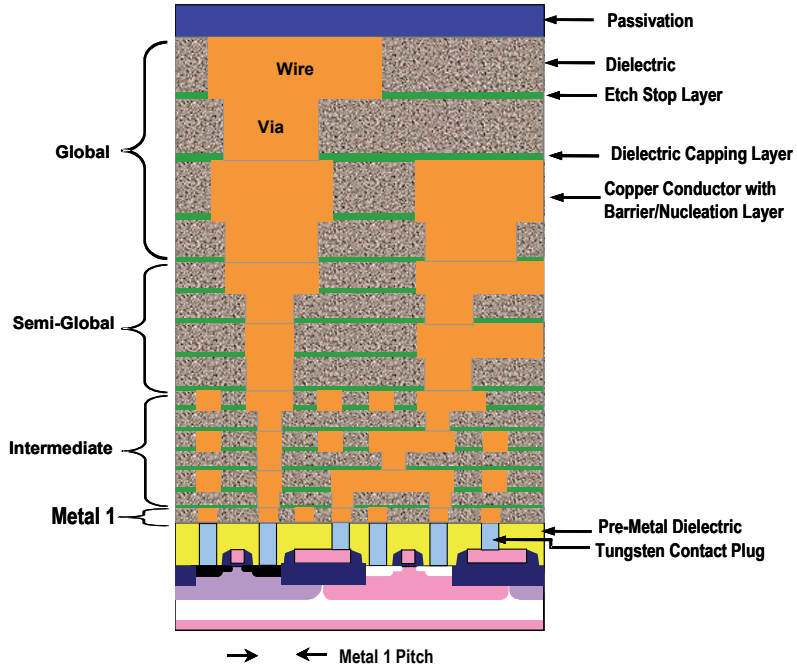


*Figure INTC3 Cross-section of Hierarchical Scaling—ASIC Device*

Continuous improvement in dielectric CMP and post-CMP defect reduction will be needed in the near term. The development of alternative planarization techniques is a potential long-term solution. For copper CMP, minimization of erosion and dishing will be necessary to meet performance needs as the wiring thickness is scaled. Further research is needed to improve planarization processes (with associated end-point) which are compatible with low-κ dielectrics characterized by low density and poor mechanical strength. Improvements in post-CMP clean will be critical in achieving the low defect densities required for future devices. Etch, resist strip, and post-etch cleans must be developed which maintain the desired selectivity to etch stop layers and diffusion barriers, but which do not degrade low-κ dielectrics. Low or no device damage during etch and deposition processes is the goal, especially as thinner gate oxides and/or new gate dielectric materials are introduced.

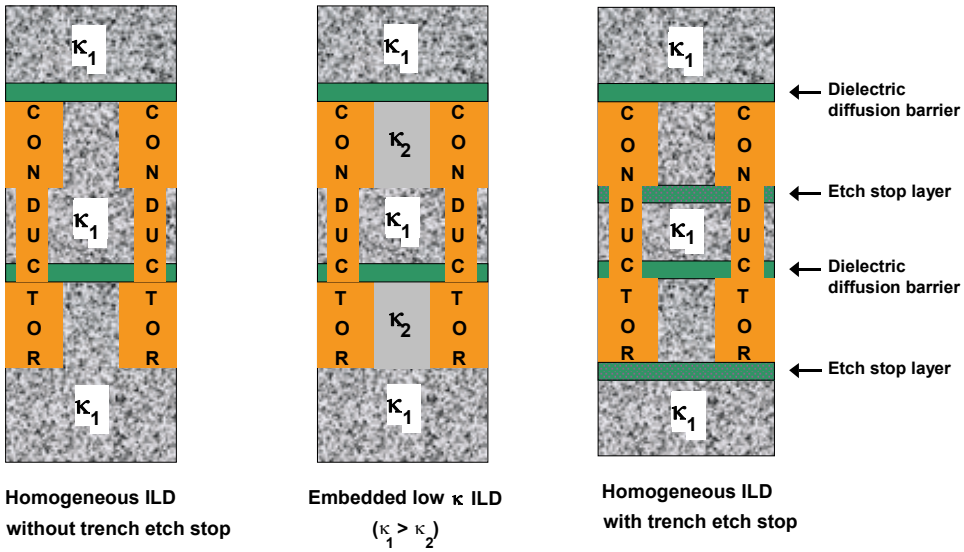


*Figure INTC4 Typical ILD Architectures*



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*Table INTC2a MPU Interconnect Technology Requirements—Near-term Years*

| *Year of Production* | *2007* | *2008* | *2009* | *2010* | *2011* | *2012* | *2013* | *2014* | *2015* |
|---|---|---|---|---|---|---|---|---|---|
| *MPU/ASIC Metal 1 ½ Pitch (nm)(contacted)* | *68* | *59* | *52* | *45* | *40* | *36* | *32* | *28* | *25* |
| *MPU Physical Gate Length (nm)* | *25* | *22* | *20* | *18* | *16* | *14* | *13* | *11* | *10* |
| Number of metal levels (includes ground planes and passive devices) | **11** | **12** | **12** | **12** | **12** | **12** | **13** | **13** | **13** |
| Total interconnect length (m/cm$^2$) – Metal 1 and five intermediate levels, active wiring only [1] | **1439** | **1712** | **2000** | **2222** | **2500** | **2857** | **3125** | **3571** | **4000** |
| FITs/m length/cm$^2$ × 10$^{-3}$ excluding global levels [2] | **3.5** | **2.9** | **2.5** | **2.3** | **2** | **1.8** | **1.6** | **1.4** | **1.3** |
| Interlevel metal insulator – effective dielectric constant (κ) | **2.9–3.3** | **2.9–3.3** | **2.6–2.9** | **2.6–2.9** | **2.6–2.9** | **2.4–2.8** | **2.4–2.8** | **2.4–2.8** | **2.1–2.5** |
| Interlevel metal insulator – bulk dielectric constant (κ) | **2.5–2.9** | **2.5–2.9** | **2.3–2.7** | **2.3–2.7** | **2.3–2.7** | **2.1–2.5** | **2.1–2.5** | **2.1–2.5** | **1.9–2.3** |
| Copper diffusion barrier and etch stop – bulk dielectric constant (κ) | **4.0–4.5** | **4.0–4.5** | **3.5–4.0** | **3.5–4.0** | **3.5–4.0** | **3.0–3.5** | **3.0–3.5** | **3.0–3.5** | **2.6–3.0** |
| Metal 1 wiring pitch (nm) * | **136** | **118** | **104** | **90** | **80** | **72** | **64** | **56** | **50** |
| Metal 1 A/R (for Cu) | **1.7** | **1.8** | **1.8** | **1.8** | **1.8** | **1.8** | **1.9** | **1.9** | **1.9** |
| Barrier/cladding thickness (for Cu Metal 1 wiring) (nm) [3] | **4.8** | **4.3** | **3.7** | **3.3** | **2.9** | **2.6** | **2.4** | **2.1** | **1.9** |
| Cu thinning at minimum pitch due to erosion (nm), 10% × height, 50% area density, 500 µm square array | **12** | **11** | **9** | **8** | **7** | **6** | **6** | **5** | **5** |
| Conductor effective resistivity (µΩ-cm) Cu Metal 1 wiring including effect of width-dependent scattering and a conformal barrier of thickness specified below | **3.51** | **3.63** | **3.80** | **4.08** | **4.30** | **4.53** | **4.83** | **5.20** | **5.58** |
| Capacitance per unit length for M1 wires (pF/cm) - assumed PMD $\kappa_{eff}$ = 4.2 [6] | **1.9–2.0** | **1.9–2.1** | **1.8–2.0** | **1.8–2.0** | **1.8–2.0** | **1.7–1.9** | **1.7–1.9** | **1.7–1.8** | **1.5–1.7** |
| Interconnect RC delay (ps) for a 1 mm Cu Metal 1 wire, assumes no scattering and an effective ρ of 2.2 µΩ-cm | **558** | **717** | **848** | **1132** | **1433** | **1695** | **2075** | **2710** | **3128** |
| Interconnect RC delay (ps) for 1 mm Cu Metal 1 wire, assumes width-dependent scattering and a conformal barrier of thickness specified below | **890** | **1183** | **1465** | **2100** | **2801** | **3491** | **4555** | **6405** | **7935** |
| Line length (µm) where τ = RC delay (Metal 1 wire) no scattering | **34** | **27** | **25** | **19** | **15** | **13** | **11** | **9** | **8** |
| Line length (µm) where 25% of switching voltage is induced on victim Metal 1 wire by crosstalk [4] | **104** | **89** | **89** | **82** | **78** | **64** | **57** | **49** | **46** |
| Total Metal 1 resistance variability due to CD erosion and scattering (%) | **28** | **29** | **30** | **30** | **31** | **32** | **32** | **31** | **33** |
| Intermediate wiring pitch (nm) | **136** | **118** | **104** | **90** | **80** | **72** | **64** | **56** | **50** |
| Intermediate wiring dual damascene A/R (Cu wire/via) | **1.8/1.6** | **1.8/1.6** | **1.8/1.6** | **1.8/1.6** | **1.8/1.6** | **1.9/1.7** | **1.9/1.7** | **1.9/1.7** | **1.9/1.7** |
| Barrier/cladding thickness (for Cu intermediate wiring) (nm) [3] | **5.2** | **4.3** | **3.7** | **3.3** | **2.9** | **2.6** | **2.4** | **2.1** | **1.9** |
| Semi-global wire pitch (nm) (ASIC only) | **280** | **236** | **208** | **180** | **160** | **144** | **128** | **112** | **100** |
| Cu thinning at minimum intermediate pitch due to erosion (nm), 10% × height, 50% area density, 500 µm square array | **12** | **11** | **9** | **8** | **7** | **7** | **6** | **5** | **5** |
| Conductor effective resistivity (µΩ-cm) Cu intermediate wiring including effect of width-dependent scattering and a conformal barrier of thickness specified below | **3.43** | **3.63** | **3.80** | **4.08** | **4.30** | **4.49** | **4.83** | **5.20** | **5.58** |



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*Table INTC2a MPU Interconnect Technology Requirements—Near-term Years*

| *Year of Production* | *2007* | *2008* | *2009* | *2010* | *2011* | *2012* | *2013* | *2014* | *2015* |
|---|---|---|---|---|---|---|---|---|---|
| *MPU/ASIC Metal 1 ½ Pitch (nm)(contacted)* | *68* | *59* | *52* | *45* | *40* | *36* | *32* | *28* | *25* |
| *MPU Physical Gate Length (nm)* | *25* | *22* | *20* | *18* | *16* | *14* | *13* | *11* | *10* |
| Capacitance per unit length for intermediate wires (pF/cm) [6] | **1.8-2.0** | **1.8-2.0** | **1.6-1.8** | **1.6-1.8** | **1.6-1.8** | **1.5-1.8** | **1.5-1.8** | **1.5-1.8** | **1.3-1.6** |
| $J_{max}$ (A/cm$^2$) – intermediate wire (at 105ºC) [7] * | **9.95E+05** | **1.20E+06** | **1.37E+06** | **1.72E+06** | **1.91E+06** | **1.85E+06** | **2.25E+06** | **2.57E+06** | **2.57E+06** |
| Interconnect RC delay (ps) for a 1 mm Cu intermediate wire, assumes no scattering and an effective ρ of 2.2 μΩ-cm | **475** | **669** | **764** | **1020** | **1291** | **1455** | **1842** | **2406** | **2670** |
| Interconnect RC delay (ps) for 1 mm Cu intermediate wire, assumes width-dependent scattering and a conformal barrier of thickness specified below | **741** | **1104** | **1320** | **1892** | **2524** | **2970** | **4044** | **5687** | **6771** |
| Line length (μm) where τ = RC delay (intermediate wire) no scattering | **37** | **28** | **26** | **20** | **16** | **14** | **12** | **9** | **8** |
| Line length (μm) where 25% of switching voltage is induced on victim intermediate wire by crosstalk [4] | **148** | **125** | **124** | **115** | **102** | **80** | **72** | **62** | **60** |
| Minimum global wiring pitch (nm) | **210** | **177** | **156** | **135** | **120** | **108** | **96** | **84** | **75** |
| Ratio range (global wiring pitches/intermediate wiring pitch) | **1.5–14** | **1.5–17** | **1.5–20** | **1.5–22** | **1.5–25** | **1.5–29** | **1.5–31** | **1.5–36** | **1.5–40** |
| Global wiring dual damascene A/R (Cu wire/via) | **2.3/2.1** | **2.3/2.1** | **2.4/2.2** | **2.4/2.2** | **2.4/2.2** | **2.5/2.3** | **2.5/2.3** | **2.5/2.3** | **2.6/2.4** |
| Barrier/cladding thickness (for min. pitch Cu global wiring) (nm) [3] | **5.2** | **4.3** | **3.7** | **3.3** | **2.9** | **2.6** | **2.4** | **2.1** | **1.9** |
| Cu thinning of maximum width global wiring due to dishing and erosion (nm), 10% × height, 80% area density | **230** | **230** | **240** | **240** | **240** | **250** | **250** | **250** | **260** |
| Cu thinning global wiring due to dishing (nm), 100 μm wide feature | **24** | **20** | **19** | **16** | **14** | **14** | **12** | **11** | **10** |
| Conductor effective resistivity (μΩ-cm) minimum pitch Cu global wiring including effect of width-dependent scattering and a conformal barrier of thickness specified below | **2.73** | **2.85** | **2.94** | **3.10** | **3.22** | **3.34** | **3.52** | **3.73** | **3.93** |
| Capacitance per unit length for global wires (pF/cm) [6] | **2.0-2.3** | **2.0-2.3** | **1.8-2.0** | **1.8-2.0** | **1.8-2.0** | **1.7-2.0** | **1.7-2.0** | **1.7-2.0** | **1.5-1.8** |
| Interconnect RC delay (ps) for a 1 mm minimum pitch Cu global wire, assumes no scattering and an effective ρ of 2.2 μΩ-cm | **183** | **258** | **288** | **385** | **487** | **557** | **705** | **921** | **1004** |
| Interconnect RC delay (ps) for 1 mm Cu min pitch global wire, assumes width-dependent scattering and a conformal barrier of thickness specified below | **227** | **334** | **385** | **542** | **713** | **846** | **1129** | **1562** | **1794** |
| Line length (μm) where τ = RC delay (global wire at minimum pitch – no scattering) | **59** | **46** | **42** | **32** | **26** | **23** | **19** | **15** | **13** |
| Line length (μm) where 25% of switching voltage is induced on victim minimum global wire by crosstalk [4] | **127** | **110** | **116** | **107** | **112** | **86** | **81** | **71** | **68** |
| Power index (W/GHz-cm$^2$) [5] | **1.4-1.6** | **1.4-1.6** | **1.4-1.6** | **1.6-1.8** | **1.8-2.0** | **1.6-1.8** | **1.7-2.0** | **2.0-2.3** | **1.5-1.8** |



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*Table INTC2b MPU Interconnect Technology Requirements—Long-term Years*

| *Year of Production* | *2016* | *2017* | *2018* | *2019* | *2020* | *2021* | *2022* |
|---|---|---|---|---|---|---|---|
| *MPU/ASIC Metal 1 ½ Pitch (nm)(contacted)* | *22* | *20* | *18* | *16* | *14* | *13* | *11* |
| *MPU Physical Gate Length (nm)* | *9* | *8* | *7* | ***6.3*** | ***5.6*** | ***5.0*** | ***4.5*** |
| Number of metal levels (includes ground planes and passive devices) | **13** | **14** | **14** | **14** | **14** | **15** | **15** |
| Total interconnect length (m/cm$^2$) – Metal 1 and five intermediate levels, active wiring only [1] | **4545** | **5000** | **5555** | **6250** | **7143** | **7692** | **9091** |
| FITs/m length/cm$^2$ × 10$^{-3}$ excluding global levels [2] | **1.1** | **1** | **0.9** | **0.8** | **0.7** | **0.7** | **0.5** |
| Interlevel metal insulator – effective dielectric constant (κ) | **2.1–2.5** | **2.1–2.5** | **2.0–2.3** | **2.0–2.3** | **2.0–2.3** | **1.7–2.0** | **1.7–2.0** |
| Interlevel metal insulator – bulk dielectric constant (κ) | **1.9–2.3** | **1.9–2.3** | **1.7–2.1** | **1.7–2.1** | **1.7–2.1** | **1.5–1.9** | **1.5–1.9** |
| Copper diffusion barrier and etch stop – bulk dielectric constant (κ) | **2.6–3.0** | **2.6–3.0** | **2.4–2.6** | **2.4–2.6** | **2.4–2.6** | **2.1–2.4** | **2.1–2.4** |
| Metal 1 wiring pitch (nm) * | **44** | **40** | **36** | **32** | **28** | **26** | **22** |
| Metal 1 A/R (for Cu) | **2** | **2** | **2** | **2** | **2** | **2.1** | **2.1** |
| Barrier/cladding thickness (for Cu Metal 1 wiring) (nm) [3] | **1.7** | **1.5** | **1.3** | **1.2** | **1.1** | **1** | **0.9** |
| Cu thinning at minimum pitch due to erosion (nm), 10% × height, 50% area density, 500 µm square array | **4** | **4** | **4** | **3** | **3** | **3** | **2** |
| Conductor effective resistivity (µΩ-cm) Cu Metal 1 wiring including effect of width-dependent scattering and a conformal barrier of thickness specified below | **6.01** | **6.33** | **6.70** | **7.34** | **8.19** | **8.51** | **9.84** |
| Capacitance per unit length for M1 wires (pF/cm) - assumed PMD $\kappa_{eff}$ = 4.2 [6] | **1.6–1.8** | **1.6–1.8** | **1.6–1.7** | **1.6–1.7** | **1.6–1.7** | **1.4–1.6** | **1.4–1.6** |
| Interconnect RC delay (ps) for a 1 mm Cu Metal 1 wire, assumes no scattering and an effective ρ of 2.2 µΩ-cm | **3899** | **4718** | **5569** | **7048** | **9206** | **9369** | **13085** |
| Interconnect RC delay (ps) for 1 mm Cu Metal 1 wire, assumes width-dependent scattering and a conformal barrier of thickness specified below | **10652** | **13575** | **16960** | **23515** | **34271** | **36239** | **58525** |
| Line length (µm) where τ = RC delay (Metal 1 wire) no scattering | **6** | **5** | **4** | **4** | **3** | **3** | **2** |
| Line length (µm) where 25% of switching voltage is induced on victim Metal 1 wire by crosstalk [4] | **39** | **35** | **32** | **27** | **23** | **22** | **18** |
| Total Metal 1 resistance variability due to CD erosion and scattering (%) | **32** | **33** | **35** | **33** | **33** | **32** | **33** |
| Intermediate wiring pitch (nm) | **44** | **40** | **36** | **32** | **28** | **26** | **22** |
| Intermediate wiring dual damascene A/R (Cu wire/via) | **2.0/1.8** | **2.0/1.8** | **2.0/1.8** | **2.0/1.8** | **2.0/1.8** | **2.1/1.9** | **2.1/1.9** |
| Barrier/cladding thickness (for Cu intermediate wiring) (nm) [3] | **1.7** | **1.5** | **1.3** | **1.2** | **1.1** | **1** | **0.9** |
| Semi-global wire pitch (nm) (ASIC only) | **88** | **80** | **72** | **64** | **56** | **52** | **44** |
| Cu thinning at minimum intermediate pitch due to erosion (nm), 10% × height, 50% area density, 500 µm square array | **4** | **4** | **4** | **3** | **3** | **3** | **2** |
| Conductor effective resistivity (µΩ-cm) Cu intermediate wiring including effect of width-dependent scattering and a conformal barrier of thickness specified below | **6.01** | **6.33** | **6.70** | **7.34** | **8.19** | **8.51** | **9.84** |
| Capacitance per unit length for intermediate wires (pF/cm) [6] | **1.3-1.6** | **1.3-1.6** | **1.3-1.5** | **1.3-1.5** | **1.3-1.5** | **1.1-1.3** | **1.1-1.3** |
| $J_{max}$ (A/cm$^2$) – intermediate wire (at 105ºC) [7] * | **3.06E+06** | **2.97E+06** | **3.23E+06** | **3.81E+06** | **4.25E+06** | **3.65E+06** | **4.47E+06** |
| Interconnect RC delay (ps) for a 1 mm Cu intermediate wire, assumes no scattering and an effective ρ of 2.2 µΩ-cm | **3341** | **4043** | **4665** | **5905** | **7712** | **7482** | **10450** |
| Interconnect RC delay (ps) for 1 mm Cu intermediate wire, assumes width-dependent scattering and a conformal barrier of thickness specified below | **9127** | **11632** | **14208** | **19700** | **28711** | **28942** | **46741** |
| Line length (µm) where τ = RC delay (intermediate wire) no scattering | **7** | **6** | **5** | **4** | **3** | **3** | **3** |
| Line length (µm) where 25% of switching voltage is induced on victim intermediate wire by crosstalk [4] | **48** | **43** | **38** | **34** | **30** | **30** | **22** |
| Minimum global wiring pitch (nm) | **66** | **60** | **54** | **48** | **42** | **39** | **33** |
| Ratio range (global wiring pitches/intermediate wiring pitch) | **1.5–45** | **1.5–50** | **1.5–56** | **1.5–63** | **1.5–71** | **1.5-80** | **1.5-90** |
| Global wiring dual damascene A/R (Cu wire/via) | **2.6/2.4** | **2.6/2.4** | **2.8/2.5** | **2.8/2.5** | **2.8/2.5** | **2.9/2.6** | **2.9/2.6** |
| Barrier/cladding thickness (for min. pitch Cu global wiring) (nm) [3] | **1.7** | **1.5** | **1.3** | **1.2** | **1.1** | **1** | **0.9** |



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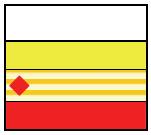
*Table INTC2b MPU Interconnect Technology Requirements—Long-term Years*

| *Year of Production* | *2016* | *2017* | *2018* | *2019* | *2020* | *2021* | *2022* |
|---|---|---|---|---|---|---|---|
| *MPU/ASIC Metal 1 ½ Pitch (nm)(contacted)* | *22* | *20* | *18* | *16* | *14* | *13* | *11* |
| *MPU Physical Gate Length (nm)* | *9* | *8* | *7* | ***6.3*** | ***5.6*** | ***5.0*** | ***4.5*** |
| Cu thinning of maximum width global wiring due to dishing and erosion (nm), 10% × height, 80% area density | **260** | **260** | **280** | **280** | **280** | **300** | **290** |
| Cu thinning global wiring due to dishing (nm), 100 µm wide feature | **9** | **8** | **8** | **7** | **6** | **5** | **5** |
| Conductor effective resistivity (µΩ-cm) minimum pitch Cu global wiring including effect of width-dependent scattering and a conformal barrier of thickness specified below | **4.20** | **4.38** | **4.58** | **4.92** | **5.38** | **5.59** | **6.30** |
| Capacitance per unit length for global wires (pF/cm) [6] | **1.5-1.8** | **1.5-1.8** | **1.5-1.8** | **1.5-1.8** | **1.5-1.8** | **1.3-1.5** | **1.3-1.5** |
| Interconnect RC delay (ps) for a 1 mm minimum pitch Cu global wire, assumes no scattering and an effective ρ of 2.2 µΩ-cm | **1297** | **1569** | **1759** | **2226** | **2907** | **2860** | **3994** |
| Interconnect RC delay (ps) for 1 mm Cu min pitch global wire, assumes width-dependent scattering and a conformal barrier of thickness specified below | **2476** | **3124** | **3661** | **4978** | **7110** | **7266** | **11437** |
| Line length (µm) where τ = RC delay (global wire at minimum pitch – no scattering) | **11** | **9** | **8** | **7** | **5** | **5** | **4** |
| Line length (µm) where 25% of switching voltage is induced on victim minimum global wire by crosstalk [4] | **62** | **56** | **53** | **45** | **41** | **39** | **31** |
| Power index (W/GHz-cm$^2$) [5] | **1.8-2.1** | **1.5-1.8** | **1.6-1.8** | **1.8-2.1** | **2.1-2.4** | **1.6-1.9** | **1.9-2.3** |

** Refer to Executive Summary for definition of M1 pitch and on-chip local clock for $J_{max}$ estimation*

*Manufacturable solutions exist, and are being optimized*
*Manufacturable solutions are known*
*Interim solutions are known*
*Manufacturable solutions are NOT known*



*Notes for Tables INTC2a and b:*
*[1] Calculated by assuming that only one of every three minimum pitch wiring tracks for Metal 1 and five intermediate wiring levels are populated. The wiring lengths for each level are then summed to calculate the total interconnect length per square centimeter of active area.*
*[2] This metric is calculated by assuming that a 5 FIT (failure in time) reliability budget is apportioned to interconnect for the highest reliability grade MPUs. This number is then divided by the total interconnect length to arrive at the FITs per meter of wiring per one square centimeter of active area.*
*[3] Calculated for a conformal layer to meet minimum effective conductor resistivity with no scattering.*
*[4] Crosstalk is a calculated value. This metric will be managed by IC Design.*
*[5] Power index = C $V_{dd}^2$ a (1 GHz) $e_w$ (1 cm$^2$)/p; p = pitch; $V_{dd}$ = supply voltage; $e_w$ = wiring efficiency = 1/3; a = activity factor = 0.03. The calculated values are an approximation for the "power per GHz per cm$^2$ of metallization layer." This index scales with the critical parameters that determine the interconnect dynamic power. NOTES: the values provided are an average for M1, Intermediate and Global interconnects. The range of values results from the maximum and minimum effective dielectric constants.*
*[6] The capacitance range reflects the maximum and minimum effective dielectric constants.*
*[7] No change in $J_{max}$ calculation model. Only frequency input was changed.*



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*Table INTC3a DRAM Interconnect Technology Requirements—Near-term Years*

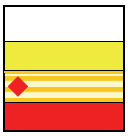
| *Year of Production* | *2007* | *2008* | *2009* | *2010* | *2011* | *2012* | *2013* | *2014* | *2015* |
|---|---|---|---|---|---|---|---|---|---|
| *DRAM ½ Pitch (nm) (contacted)* | *65* | *57* | *50* | *45* | *40* | *36* | *32* | *28* | *25* |
| Number of metal layers | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 |
| Contact A/R – stacked capacitor | 16 | 17 | 17 | >20 | >20 | >20 | >20 | >20 | >20 |
| Metal 1 wiring pitch (nm)* | 130 | 114 | 100 | 90 | 80 | 72 | 64 | 56 | 50 |
| Specific contact resistance ($\Omega$-cm$^2$) for n+ Si | 2.00E-08 | 1.70E-08 | 1.40E-08 | 1.20E-08 | 9.80E-09 | 8.20E-09 | 6.90E-09 | 5.80E-09 | 4.80E-09 |
| Specific contact resistance ($\Omega$-cm$^2$) for p+ Si | 3.20E-08 | 2.70E-08 | 2.20E-08 | 1.80E-08 | 1.50E-08 | 1.30E-08 | 1.10E-08 | 9.20E-09 | 7.40E-09 |
| Specific via resistance ($\Omega$-cm$^2$) | 5.00E-10 | 4.00E-10 | 3.50E-10 | 2.90E-10 | 2.50E-10 | 2.10E-10 | 1.70E-10 | 1.40E-10 | 1.20E-10 |
| Conductor effective resistivity ($\mu\Omega$-cm) assumes no scattering for Cu | 2.2 | 2.2 | 2.2 | 2.2 | 2.2 | 2.2 | 2.2 | 2.2 | 2.2 |
| Interlevel metal insulator – effective dielectric constant ($\kappa$) | 3.6–4.1 | 3.6–4.1 | 3.1–3.4 | 3.1-3.4 | 2.7–3.0 | 2.7–3.0 | 2.7–3.0 | 2.5–2.8 | 2.5–2.8 |

*Table INTC3b DRAM Interconnect Technology Requirements—Long-term Years*

| *Year of Production* | *2016* | *2017* | *2018* | *2019* | *2020* | *2021* | *2022* |
|---|---|---|---|---|---|---|---|
| *DRAM ½ Pitch (nm) (contacted)* | *22* | *20* | *18* | *16* | *14* | *13* | *11* |
| Number of metal layers | 4 | 4 | 4 | 4 | 4 | 4 | 4 |
| Contact A/R – stacked capacitor | >20 | >20 | >20 | >20 | >20 | >20 | >20 |
| Metal 1 wiring pitch (nm)* | 44 | 40 | 36 | 32 | 28 | 26 | 22 |
| Specific contact resistance ($\Omega$-cm$^2$) for n+ Si | 4.00E-09 | 3.40E-09 | 2.80E-09 | 2.34E-09 | 1.96E-09 | 1.65E-09 | 1.37E-09 |
| Specific contact resistance ($\Omega$-cm$^2$) for p+ Si | 6.20E-09 | 5.10E-09 | 4.30E-09 | 3.60E-09 | 3.01E-09 | 2.52E-09 | 2.11E-09 |
| Specific via resistance ($\Omega$-cm$^2$) | 1.00E-10 | 8.40E-11 | 7.00E-11 | 5.81E-10 | 4.82E-10 | 4.00E-10 | 3.32E-10 |
| Conductor effective resistivity ($\mu\Omega$-cm) assumes no scattering for Cu | 2.2 | 2.2 | 2.2 | 2.2 | 2.2 | 2.2 | 2.2 |
| Interlevel metal insulator – effective dielectric constant ($\kappa$) | 2.5–2.8 | 2.3–2.6 | 2.3–2.6 | 2.3–2.6 | 2.3–2.6 | 2.3–2.6 | 2.3–2.6 |

** Refer to Executive Summary for the definition of Metal 1 pitch*

*Manufacturable solutions exist, and are being optimized*
*Manufacturable solutions are known*
*Interim solutions are known*
*Manufacturable solutions are NOT known*





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# POTENTIAL SOLUTIONS

## DIELECTRIC POTENTIAL SOLUTIONS

The industry has continued to gain experience with the integration nuances of the respective low-κ ILD material platforms since their insertion in the 130nm technology generation in 2002. Although this has continued to be a very difficult transition from silicon dioxide and the relatively simple copper dual damascene integration process of full via first (FVF), the time spent on the learning curve should be leveragable for many future technologies inclusive of low-κ ILD materials. The FVF integration process still requires the fewest number of deposition layers to integrate, creates the fewest number of interfaces and yields the lowest effective dielectric constant value relative to the integrated bulk dielectric constant of the ILD layer. The homogeneous ILD process flow continues to be the dominant integration process for low-κ ILD materials through 65nm. To continue to implement a homogeneous low-κ dielectric process flow, the use of multi-layer (2, 3 or 4) patterning schemes which contain combinations of dielectric as well as conductor layers, has become common to achieve the dual damascene structure. These multi-layer patterning schemes still do not fully address the variability associated with the copper trench cross-sectional area (trench depth control) and its' direct influence on variability in RC delay. The hybrid ILD process flow, which is also in commercial manufacturing, directly addresses this source of variability in trench depth control and subsequently in RC delay. A growing interest in exploring the challenges associated with the ultimate performance Cu back-end of the line (BEOL) ILD structure, $\kappa_{eff}$ of < 2.0, which incorporates air as the dielectric medium, has resulted in the inclusion of a detailed section in the Appendix that discusses the state of the art for this integration technology.

For the future, a continual growth in the number of individual dielectric layers constituting the total BEOL ILD stack (cap, via, trench, etch stop, CMP stop) will grow both as a function of the projected increase in the total number of interconnect layers within the BEOL as well as the individual optimization of unique layers with single or specific functionality. This growth will present both adhesive and cohesive challenges associated with the increasing number of interfaces of dissimilar materials with differences in chemical bonding, diffusivity, modulus, hardness, strain and expansion coefficient (CTE). Advancement in chip packaging technology can be a means of extending the manufacturing process window for these low-κ ILD material challenges. The ability to cluster the deposition processing of sequential layers to minimize contamination and reduce cost of ownership (CoO) will be an industry goal but will become increasingly more difficult as individually optimal film solutions are sought to improve manufacturability and reliability continually. Alternate curing technologies are being introduced to address a combination of deficiencies in adhesion and cohesion strength, porogen removal, chemical robustness and remediation of materials damaged during processing.

The industry continues to implement a successful evolutionary path for the adoption and introduction of progressively lower-κ ILD materials instead of the revolutionary path contemplated in the 2001 ITRS document and certainly earlier roadmaps. This evolutionary path chosen by companies may either be associated with a single materials platform (plasma enhanced chemical vapor deposition, PECVD, with incremental reductions of κ value by increases in porosity) coupled with a preferred integration process (homogeneous ILD) or the combination of two materials platforms (organic at trench and inorganic at via) with a preferred integration process (hybrid ILD), inclusive of independent roadmaps for each dielectric layer, analogous to a mix and match strategy.

There is a new focus on creation of a roadmap for the introduction of progressively lower dielectric constant materials at the PMD level, to acknowledge the ongoing development activities of candidate materials and deposition technologies currently on-going at both IC manufacturing companies and suppliers. The Dielectric Potential Solutions (Figure INTC5) indicates that existing commercial manufacturing technologies are capable of delivering PMD materials at approximately κ=4.0 with the requirements for the next few technology generations, ultimately approaching κ=3.0.

New dielectric materials requirements must encompass the needs of both conventional, novel FEOL device architectures as well as BEOL Integrated Passives or advanced interconnect solutions discussed within the Interconnect section of this document. Some dielectric materials are finding additional uses in alternate locations of the BEOL structure with a new emphasis on the required combination of electrical, mechanical, and processing properties. Even with new and ever more stringent requirements for future technology generations, the lifetime of the existing class of silica-based dielectric materials will be extended because of the challenges with the material properties and/or integration schemes required of all new ILD materials.

The following three overall BEOL dielectric challenges remain valid throughout the fifteen-year scope of this 2007 roadmap:



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- Development of low-κ materials and manufacturing processes capable of achieving the minimum effective permittivity ($\kappa_{eff}$) possible, for maximum device performance and reliability at a viable performance/reliability/price ratio, for Cu dual damascene technology with emerging packaging options
- Continued understanding of the current and future reliability / failure modes associated with emerging low-κ ILD materials, dielectric barrier materials, environmental effects and packaging structures
- Development of moderate (κ >20) to high (κ >100) permittivity materials and manufacturing processes capable of achieving continually higher bit density at a viable bit/price ratio for stand-alone memory applications, decoupling and MIM capacitors for MPU/ASICs and system-on-a-chip (SOC).

To address the range of dielectric material requirements and add focus to each specific application within the BEOL, Figure INTC5, Dielectric Potential Solutions, shows the dielectric families which could be used at each level and for the various deposition/cure technologies, as well as a timeline addressing the current development status of each material.

The values reported in Table INTC2a and b for the "Interlevel metal insulator—effective dielectric constant" and "Interlevel metal insulator (minimum expected)—bulk dielectric constant" have been derived from a generic electrical simulation model for three mainstream ILD integration schemes with parameters specific to the years defined in this 2007 roadmap. The methodology employed a standard simulation model and incorporated the most realistic parameters for Cu cap, hardmask (dielectric protection layer), trench ILD, via ILD, and geometries specific to each year detailed in this roadmap. The simulation was performed for each of the three generic ILD integration schemes (homogeneous, homogeneous with hardmask / dielectric protection layer and hybrid) multiplexed with a materials set which represents both the most aggressive dielectric values projected to be available for manufacturing in the given year as well as a more realistic materials set available for manufacturing in the given year. The lowest values in the reported range for both the "Interlevel metal insulator—effective dielectric constant" and the "Interlevel metal insulator (minimum expected)—bulk dielectric constant" for a given year are derived from the input parameters and simulation results for the aggressive case while the highest values for a given year are derived from the input parameters and simulation results for the "realistic case".

By way of example, in the Appendix of this chapter, Figure A1—65nm Dielectric Potential Solutions (2007, 2008) Aggressive Case shows the simulation inputs and calculated results specific to the 65nm ground rules and the implementation of an aggressive set of dielectric materials. The lowest value in the range for "Interlevel metal insulator—effective dielectric constant" is derived from this figure (2.9) for the hybrid ILD scenario as well as the lowest value in the range for the "Interlevel metal insulator (minimum expected)—bulk dielectric constant" being 2.5 for the hybrid ILD scenario also. The maximum values for the 2007, 2008 columns of Table INTC2a and b for the corresponding range of "Interlevel metal insulator—effective dielectric constant" and "Interlevel metal insulator (minimum expected)—bulk dielectric constant" are 3.3 for the hybrid ILD scenario and 2.9 for the homogeneous ILD scenario respectively. These are derived from the input variables and output results found in Figure A2—65 nm Dielectric Potential Solutions (2007, 2008) Realistic Case.

Many electrical simulation models exist to extrapolate the effective κ values from well-controlled test structures within a die. Figures A1–A4 in the Dielectric Appendix show simulated effective κ results for representative low-κ integration schemes for the current and next two technology generations (65, 45 nm). The model inputs are specific to the 2007 ITRS targets for layer thicknesses, aspect ratios, and dielectric materials, projected to be commercially available, concurrent with proposed manufacturing ramp timings. Three values of effective κ are indicated, corresponding to their integration schemes, for each technology generation. The logical basis of κ-value derivation is clarified in this roadmap and appropriate interconnect parameters are presented, based on a logical model as shown in Figure A5, Critical Path in High-end SOC and RC Scaling Scenario. The critical path is assumed to consist of typical circuits such as 2NAND+Inverter connected with average long intermediate wires having multiple stages and long intermediate/global wires. Both long intermediate and global wires are divided by optimized repeaters in order to reduce RC delays, and long global wires have reverse-scaled width and thickness. The model assumptions are summarized in Table A1. Under the assumption, scaling of both wiring resistance and capacitance should be completely implemented so as to reduce the delay time of high-end SOC by 30% to 20% per technology generation as a result of κ value relaxation. The effective κ scaling curve calculated by this theoretical approach is shown compared with the above effective κ simulation extraction results in Figure A6. These figures are in good agreement with each other.


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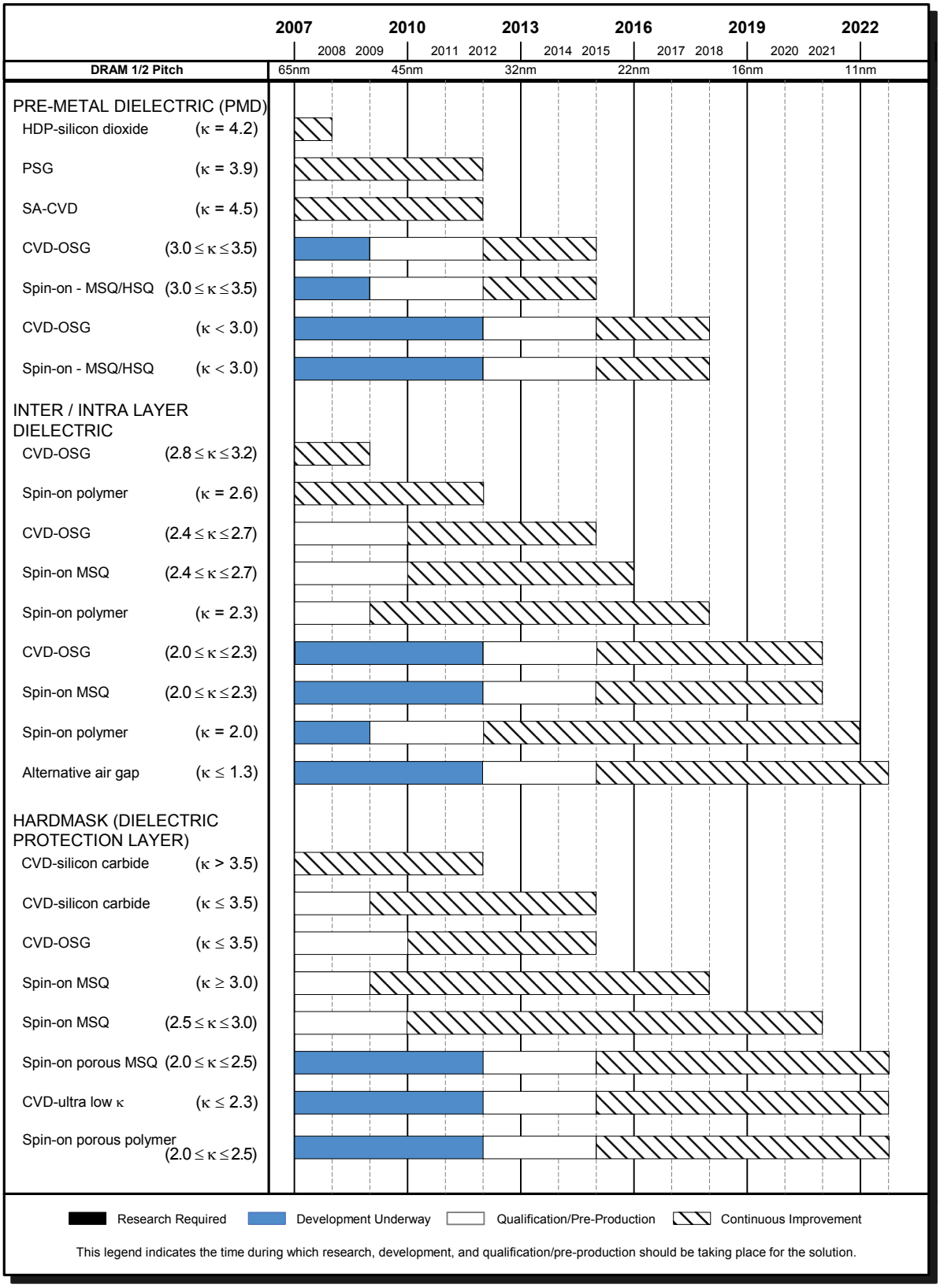


*Figure INTC5 Dielectric Potential Solutions*



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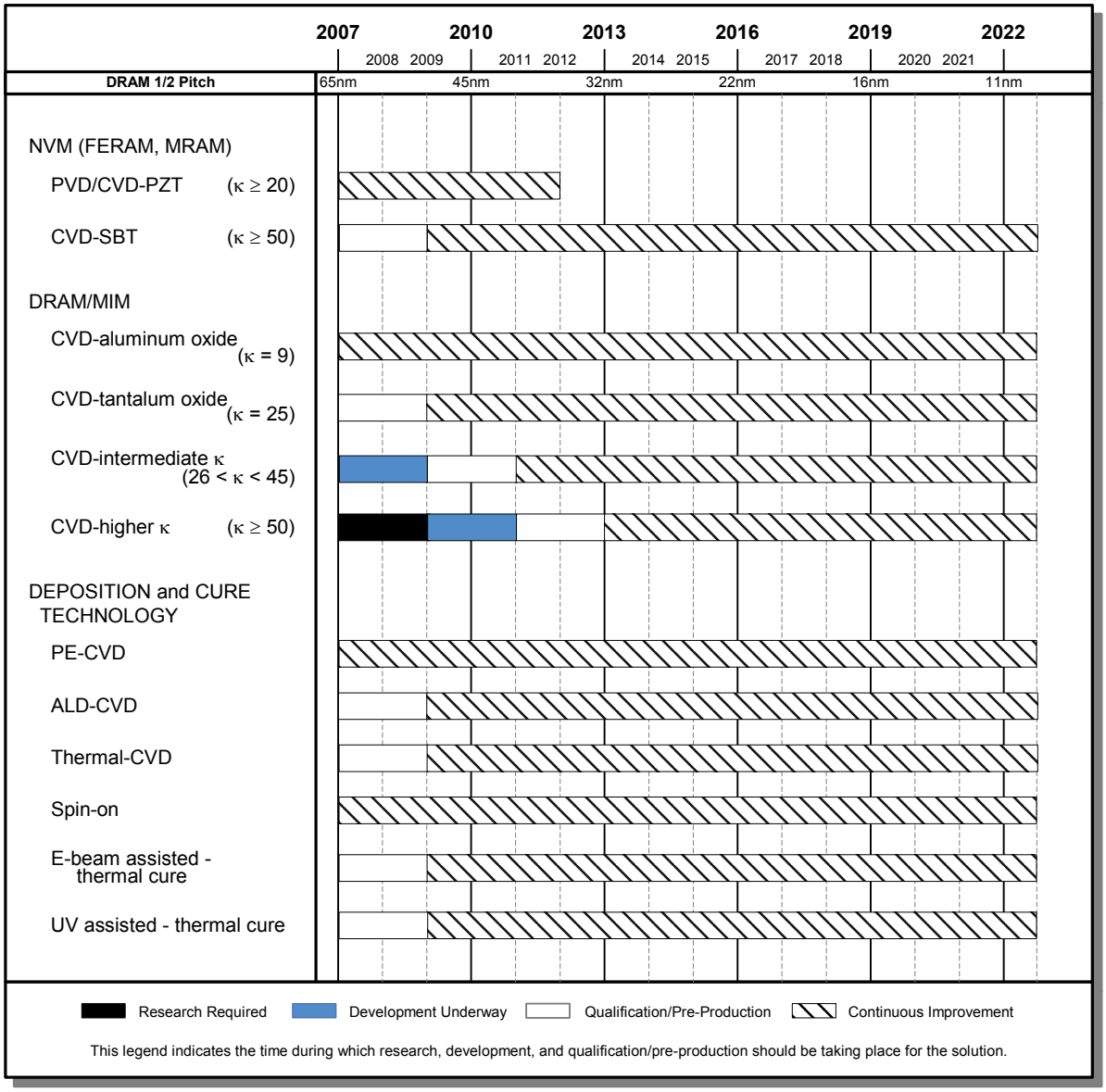


*Figure INTC5 Dielectric Potential Solutions (continued)*

## PRE-METAL DIELECTRIC (PMD)

Improvements in the reduction of the dielectric constant or changes in the technology used to deposit pre-metal dielectric (PMD) layers continue to evolve. These changes are driven for high performance logic chips by the growing negative influence the dielectric constant of the PMD material is having on the interconnect RC delay for Metal 1. The "Capacitance per unit length for M1 wires" C and consequently the other electrical parameters including the factor C as the RC delay and the cross-talk parameters have been calculated by assuming a constant value of the PMD dielectric constant equal to 4.2 in Table INTC2a and b, MPU Interconnect Technology Requirements. A detailed roadmap specific to PMD materials for Logic is in discussion for the 2008 Update. Additionally, the move to high κ, metal gates, and NiSi, in tandem with the increases in the aspect ratios of spaces between adjacent gates in DRAMs, and the simultaneous requirement for high phosphorous doping concentrations and low thermal budgets in NOR-type flash memories will drive considerable development of more optimum PMD materials. PMD development efforts will be focused on performance attributes, lower dielectric constant materials and manufacturability (lower deposition temperature, better gapfill and planarization). The increasing use of NiSi doped junctions and gate conductors in logic circuits will challenge those deposition technologies, which require anneals in the 450ºC to 490ºC range. Fortunately, the thermal budget for the recently announced introduction of high κ in combination with the introduction of metal gates continues to fall within the same temperature range dictated by the previously adopted NiSi technology. This problem is intensified when high


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phosphorous doping concentrations are also required. Some NOR-type flash memories already incorporate NiSi while requiring PMD phosphorous concentrations as high as 10% to meet charge retention requirements. The aspect ratios of the spaces between adjacent gates in DRAMs are expected to be greater then 16:1 by 2007 and will increase thereafter. As a result, DRAM PMD deposition by plasma-based processes could become increasingly problematic. Plasma induced damage (PID) of thin gate dielectrics by plasma-based PMD deposition processes continue to be insignificant but could become an area of concern as gate dielectrics grow thinner and/or are replaced by new high κ materials. Finally, low-κ dielectrics will be required in DRAMs to reduce capacitance in the layer incorporating bit lines. For example, $\kappa_{eff}$ values ranging from 2.7 to 3.1 will be required by 2010, decreasing to 2.3 to 2.6 by 2020. It is conceivable that future PMD deposition processes will incorporate multiple steps, and possibly multiple process types, to satisfy the requirements of gap fill, thermal budget, and doping concentration. Combinations of spin-on and plasma deposition are already being reported at the technical conferences with manufacturing introductions planned in a few years.

### *INTRA-METAL DIELECTRIC*

Concurrent with low-κ materials introduction is a planned migration of metal barrier deposition technologies (PVD→CVD→ALD) as well as a continued reduction in barrier thickness to maintain the targeted Cu resistivity. The combination of these integration challenges, coupled with design improvements to alternately address projected crosstalk and RC delay problems, has postponed the industry-wide implementation of low-κ ILD material past that proposed in the last four ITRS documents.

The preferred integration scheme for silicon-based dielectric materials continues to be the original "full via first" process, already implemented with silicon dioxide. While a hybrid scheme is usually adopted with organic-based dielectrics, both of these integration paths provide a cost-effective manufacturing process and also yield the lowest $\kappa_{eff}$. The $\kappa_{eff}$, paramount to the design community, is the parameter indicative of the composite dielectric permittivity experienced by an electrical signal traveling along the Cu interconnects within a chip. Many electrical simulation models exist to extrapolate these values from well-controlled test structures within a die. The figures in the Dielectric Appendix simulation present extraction results for representative low-κ integration schemes for several technology generations. The model inputs are specific to the ITRS targets for layer thicknesses, aspect ratios, and dielectric materials projected to be commercially available, concurrent with future proposed manufacturing ramp timings. Extreme low-κ dielectrics ($\kappa < 2.0$) will be required after 2015. Novel integration schemes may be required, such as air gap architecture a (hybrid dielectric stack utilizing air with $\kappa = 1.0$).

Integration challenges associated with etch selectivity/damage, 193 nm photoresist, Cu CMP, and packaging process compatibility are still areas of significant effort across almost all low-κ dielectric materials. Physical, mechanical, and electrical properties and their inter-relationship has not been sufficient to date to determine integration and reliability success; the industry is still on the learning curve. The technical community still entertains a healthy debate about microstructure requirements for porous dielectric materials with respect to pore size, pore shape, aspect ratio, and degree of interconnectivity (open versus closed).

### *HARDMASK (DIELECTRIC PROTECTION LAYER)*

Hardmask is a generic term used to describe the dielectric film deposited on top of the trench level intra-metal dielectric. It has two main functions: to assist in patterning of the dual damascene structure for subsequent metal fill and as a highly selective CMP stop layer. In addition, this layer is called upon to prevent fast diffusion of acid or base moieties that could interact detrimentally with the traditional acid-catalyzed photoresist systems employed at 248 nm and 193 nm. Depending on the efficiency of CMP and acid/base moiety inhibition, this layer could be either inconsequential to the overall $\kappa_{eff}$ or a significant contributor. For most integration schemes, the composition of this layer can be chosen independently of most other dielectric layer choices. However, in the case of the hybrid integration scheme, the etch sequence is simplified if the hardmask dielectric material and the via layer dielectric material are similar. There are both spin-on and CVD deposited solutions available with dielectric constant values down to at least 3.0. Some spin-on offerings are available with a dielectric constant as low as 2.2.

### *ETCH STOP –VIA*

The via etch stop layer continues to have two main, equally important functions. It must have adequate etch selectivity, with respect to the via dielectric layer material, so that etching of the underlying IMD adjacent to non-landed vias is avoided. It also serves as the cap for the underlying Cu wiring layer. It must be a Cu diffusion barrier and have acceptable adhesion and interface properties for Cu electromigration requirements to be met. The via etch stop layer can also be a significant contributor to overall $\kappa_{eff}$ so its thickness and κ value should both be minimized. If a selective conductive Cu diffusion barrier layer is implemented, the requirements of etch selectivity and diffusion barrier may be all or partially or completely satisfied by the conductive barrier layer without the negative (increasing) contribution to the overall $\kappa_{eff}$.



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### *ETCH STOP – TRENCH*

The primary function of the trench etch stop is to use etch selectivity for reliable definition of trench bottoms, as opposed to reliance on a timed etch. Additionally, it is increasingly important, with the introduction of higher porosity low-κ ILD materials, that the trench etch process form a smooth well-defined trench bottom to accommodate ever thinner copper barrier films. Significant trench bottom roughness can be a reliability issue if it affects metal barrier coverage continuity. Variability in trench depth can be a significant contributor to variation in metal line resistance and overall circuit timing distribution margins. In alternate integration schemes such as hybrid ILD structures, the need for discrete trench etch stop layers is eliminated because of the implementation of dielectrics with different etch characteristics.

### *DRAM*

DRAM technology has continued with the arduous process of implementing an assortment of medium dielectric constant materials ($5<\kappa<40$) in stacked and trench capacitor structures. Trench-defined DRAM technology may delay the implantation of these medium dielectric materials, for at least one generation, because of the enhanced active area available. Both DRAM technologies are developing an understanding of these medium dielectric constant materials and will leverage this understanding to the higher κ (>40) alternatives of the future.

### *DEPOSITION AND CURE TECHNOLOGIES*

Deposition technology for ILD materials have been historically based on PECVD technology with a small but growing group dedicated to both organic and inorganic-based spin-on materials. PECVD remains the dominant deposition technology, based on incumbency and continued success in lowering the dielectric constant and enhancing modulus and hardness of the films.

There is growing interest in alternate cure technologies that can assist or replace the incumbent thermal cure technologies, typically implemented by either furnace or hotplate. The goal is to either accelerate the chemical reactions of existing functionality or enable the incorporation of alternate (additional) functionality within the dielectric film that can efficiently absorb these alternate forms of energy such as photon (UV lamp) or energetic electrons and thereby initiate reactions not available within the thermal budget of current Cu BEOL processing. Alternate UV or E-beam cure technologies of have already been demonstrated as an efficient means of improving mechanical properties of low and ultra-low-κ ILD inorganic materials. The enhanced mechanical properties have resulted in expanded manufacturing process windows for CMP and packaging. In addition, for ultra-low-κ ILD matrix materials, removal of the porogen after templating (of closed pores) has been enhanced by these developing cure technologies. Investigations into the use of both broadband and wavelength-specific ultraviolet (UV) energy have been reported and continue to be developed and commercially implemented. Previously developed E-beam sources are now being applied to dielectric materials to enhance mechanical properties, remove porogen materials, and improve adhesion between the many dielectric layers that now compose the ILD stack.

### *AIR GAP TECHNOLOGIES*

The integration of porous low-κ materials into copper dual-damascene structures is accompanied by a tremendous number of challenges, delaying introduction of these dielectrics from initial roadmap indications. Since the associated IMD κ value is close to 1, air gap appears as the ultimate hybrid architecture leading to dramatic interline capacitance reduction and very low effective κ values. Different air gap integration approaches are being developed to fabricate multi-level interconnects. All approaches can be classified into one of two categories: (1) partial or complete material removal between metal lines followed by non-conformal CVD deposition and (2) damascene integration of metal lines in a sacrificial material which can be selectively removed through a dielectric cap. Each of these methods has benefits and trade-offs. (Additional information on the formation, challenges, and performance advantages of air gaps is available at this link).

## BARRIER POTENTIAL SOLUTIONS

Ti/TiN films [1] will continue to be used as barriers for tungsten local wiring and contact fill in the near term. There will be continuous improvement of established deposition techniques such as long throw and ionized PVD and CVD to improve compatibility with the new seamless W technology and high aspect ratio contacts for DRAM. Development of ALD TI/TiN is underway and is likely to improve the overall W fill process by improving barrier conformality and reducing the top of contact "pinch-off" that leads to difficulty in W filling. Even with improvements, the Ti/TiN barrier is expected to be a significant contributor to future contact plug resistivity because of film thickness requirements and high resistivity. Development of alternative ALD barriers for W contact plugs, such as WN [2, 3], is underway and it appears that barrier resistivity and thickness can both be reduced versus Ti/TiN. Therefore the barrier contribution to the overall contact plug resistance is reduced. Conventional PVD and CVD barrier technologies will be continuously improved to allow Al fill to be extended to higher aspect ratio structures, however if this technology is to be extended, ALD barriers


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will need to replace the PVD and CVD technology. Research is also underway to explore alternate materials and fill techniques for high aspect ratio contact structures that would allow simplification of the current contact/barrier/conductor film stack. Since one of the primary functions of the TiN barrier is to prevent interaction of Ti with F from the $WF_6$ precursor, a change to non-fluorine containing tungsten precursors could allow for elimination of the barrier film entirely. Serious consideration is also being given to use of Cu to replace W in contact studs. In this case the standard PVD TaN/Ta or ALD Cu barrier alternatives would be used for the barrier technology. Electroplated Rh [4] is also being considered as a potential solution for the contact plug application with Ti as the proposed barrier. Other materials such as electroless Ni are also being considered for contact plug applications.

Barrier materials used for Cu wiring must prevent its diffusion into the adjacent dielectric but in addition must form a suitable, high quality interface with Cu to limit vacancy diffusion and achieve acceptable electromigration lifetimes. TaN/Ta [5] has become the predominant industry solution but other nitrides and silicon nitrides and carbides of Ta, Ti, and W [6, 7] have also shown promise. Long throw, ionized PVD, and CVD depositions continue to be improved to meet the challenging sidewall coverage requirements of future dual damascene structures. In fact, it appears that improvements in ionized PVD technology will continue to be used at 32 nm. In addition, since the critical dimensions and aspect ratios for the upper global wiring levels for logic products remain relatively unchanged for future technology generations, they will continue to be compatible with PVD barrier technology. However, even the most advanced of these PVD deposition techniques tend to narrow the upper part of the dual damascene trench and limit the fill capability of the ECD Cu process.

A great deal of effort is underway to develop ALD [8-11] barriers that are expected to become the predominant future solution for copper. ALD TaN and WNC are furthest along in development but questions remain concerning their interface properties with Cu and whether adequate electromigration performance can be ensured. One potential solution to this issue is the use of a PVD Ta flash layer followed by PVD Cu to provide the required interface to ECD Cu. ALD Ru appears to be compatible with direct plating of ECD Cu and also provides a good Cu interface, however its barrier properties are suspect. Two advanced potential solutions are ALD TaN/ALD Ru and ALD WNC/ALD Ru bi-layer barriers. One major obstacle to the adoption of ALD for barriers is penetration of the precursor materials into the porous low-κ dielectrics targeted for future technology generations. *In situ* modification of the etched low-κ sidewalls may be used either with ALD or as a stand-alone barrier to resolve this issue. The other major obstacle regarding adoption of ALD barriers is the low throughput of ALD chambers. This results in a significant increase in the factory floor space and cost of ownership needed for ALD barrier/seed technology versus PVD barrier/seed solutions.



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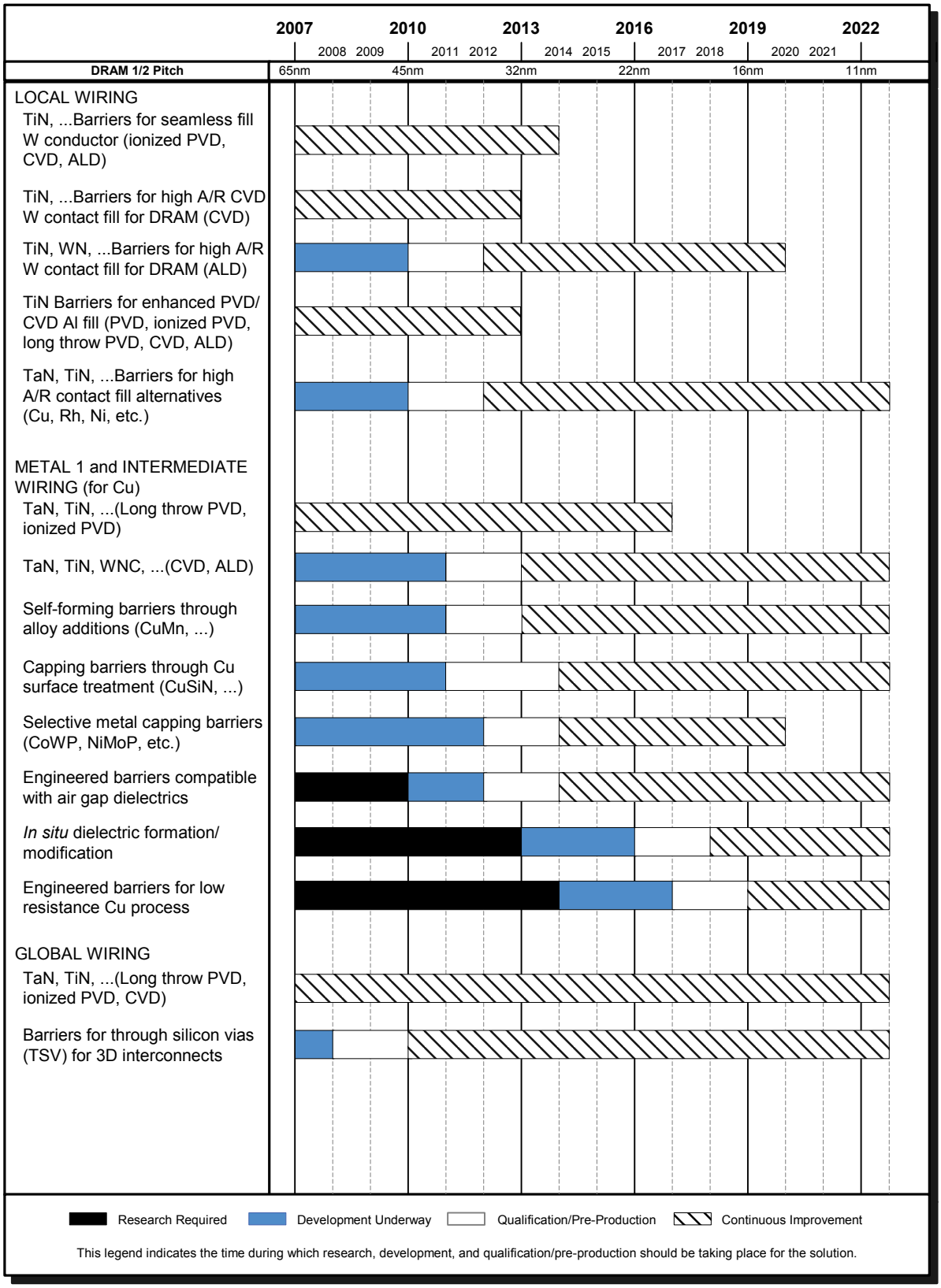


*Figure INTC6 Barrier Potential Solutions*



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One very promising area of development for Cu wiring technology is self forming barriers and specifically the Cu-Mn alloy system [12]. This process eliminates the PVD barrier and instead utilizes a PVD Cu-Mn alloy seed layer. After ECP Cu deposition, an anneal causes the Mn to diffuse to the Cu surface and form a thin barrier. The Mn at the top surface of the annealed Cu is removed by the subsequent CMP operation. Another advantage of this process is that the Mn does not form a barrier in the underlying via region. This results in a Cu – Cu via interface with very low via resistance.

Another focus area for metal barriers is the Cu top interface. Plasma enhanced chemical vapor deposition dielectric Cu barriers such as $Si_3N_4$, SiCN, and SiC are predominately used for this application. Their disadvantages are degraded Cu electromigration properties and a rise in overall $\kappa_{eff}$ of the structure because of their higher κ values. It is projected that some modification to the top Cu interface for improved electromigration lifetime will be needed by the 32 nm MPU/ASIC half pitch. Selective metal capping barriers such as W, CoWP [13], or NiMoP are being explored and have resulted in improvements in Cu electromigration properties. The industry has been slow to adopt selective metal capping processes because of the risk of yield loss from metal shorts. The other major candidate for a capping process is formation of a CuSiN layer at the top Cu surface [14]. This is accomplished by sequential exposure of the surface to $SiH_4$ and $NH_3$. While the degree of electromigration improvement is not as large as with CoWP, there is also a much decreased risk for reliability issues due to metal shorts or leakage.

A great deal of research and development in the area of advanced barrier materials and deposition techniques will be needed, since engineering the smoothness and other properties, such as the lattice mismatch between the barrier and the Cu interface, may help to ameliorate the expected Cu resistivity increase from electron scattering effects.

## CONDUCTOR POTENTIAL SOLUTIONS

Local wiring, which is sometimes called metal zero, is limited to very short lengths and usually contacts adjacent transistors. Tungsten will continue to be used for local wiring and for the contact level to the devices in microprocessors, ASICs and DRAMs. ALD, in conjunction with CVD techniques, is being utilized first in the W deposition area to accomplish a seamless W fill. The absence of seams at the local wiring or contact level is especially important when the subsequent wiring level is ECD copper in order to avoid defect issues associated with retained plating solution. There is a problem associated with the standard silane nucleation step in the CVD W process in that this Si-rich film takes up an ever-larger portion of the plug and will result in unacceptably high resistance for future technology generations. Modification of the process to minimize or eliminate this layer is an area of focus. Alternative materials and processes such as electroplated Rh [4] and electroplated Cu [15] which both exhibit superfilling behavior are also being investigated as a replacement for W contact plugs. Continued development of ALD tungsten deposition will be needed to accomplish W fill of high aspect ratio (17:1 in 2009) contacts for stacked capacitor DRAM designs. Alternate materials and techniques may ultimately be needed to address the long-term requirements of DRAM stacked capacitor contacts, which are projected to have aspect ratios greater than 20:1 by 2010. Aluminum may continue to be used for local wiring and enhanced CVD/PVD flow techniques [16] will continue to be improved for damascene architectures.

Cu will be the preferred solution for the Metal 1 and intermediate wiring levels in MPUs and ASICs and electrochemical deposition will continue to dominate the market in the near term [17-19]. There will be continuous improvement in the plating chemistry and ECD tool design to allow seamless fill of smaller geometry higher A/R structures. Development is also underway to accomplish both deposition and planarization in a single tool by combining ECD with CMP, a form of chemically enhanced planarization (CEP). However, not having the Cu overburden present during the post deposition anneal is detrimental to grain growth and may impact reliability. This may limit the use of this CEP technology. It has been reported that even with the normal Cu overburden, there is ever increasing difficulty in transforming ECD Cu in minimum feature size damascene wires into the large-grain bamboo structures desired for good electromigration performance. As a consequence, Cu grain boundaries as well as surface diffusion must both be considered as potential failure modes for electromigration in the future. One potential solution to improve the electromigration lifetime of the Cu conductor is through the use of Cu alloys such as Cu-Al [20]. The alloying element is introduced through the use of PVD Cu alloy seed layers and then diffused through the entire conductor with a post-plating anneal. Use of this Cu-Al alloy along with an optimized Cu to dielectric cap interface resulted in a 50× improvement in electromigration lifetime. One downside of the use of alloying elements is an increase in resistivity when compared to the pure conductor.

Minimum feature size Metal 1 and intermediate Cu wiring in MPUs and ASICs have already experienced a resistivity increase due to electron scattering [21-23]. The line lengths of these wiring levels tend to scale with technology generation so the impact to performance is minimal. Global wiring levels, with their much larger linewidths, will be the last to be impacted by size effects in Cu. The resistivity of the smallest pitch global wiring level is expected to increase about 40% by the end of this decade. This is more problematic, since global wiring traverses longer lengths and is more likely to impact performance than Metal 1 and intermediate wiring. Cu interfaces, microstructures, and impurity levels will need to be engineered to alleviate the impact of this resistivity rise. MPUs use a hierarchical wiring approach in



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which the pitch and thickness of the global wires are increased at each level. Indeed the final global wiring level is little changed from one generation to the next and so will not be affected by electron scattering effects. The resistivity of metals is a function of temperature and therefore cooling of IC chips is one potential solution to improve wire conductivity. However, this is probably not practical for most consumer and portable devices.

Other design alternatives are the use of repeaters or oversized drivers, both of which impact chip size and power. The most likely near-term solution is the use of very high density TSVs as an enabling technology for three dimensional chip stacking (3D IC). This technology can reduce overall interconnect wire lengths and also allow incorporation of non-Si solutions for improved functional diversity. The other near-term solutions are judicious use of design and signaling options and packaging to minimize the effect of the narrower more resistive global wires. A great deal of research is also underway on the use of either RF or optical techniques to resolve this issue. More radical solutions include superconductors, carbon nanotubes etc. A full discussion of 3D IC, a proposed roadmap for high density TSV and other alternatives is contained in the New Interconnect Concepts and Radical Solutions section.

The increasing market for wireless devices and telecom applications will spur a focus on processes and materials for passive devices within the interconnect structure. In particular, there will be a focus on new processes and materials for forming the electrodes of MIM capacitors to improve yield and reliability. Both Al and Cu are in use for standard spiral inductors, but various magnetic materials may emerge with different inductor designs to reduce the area of these devices.


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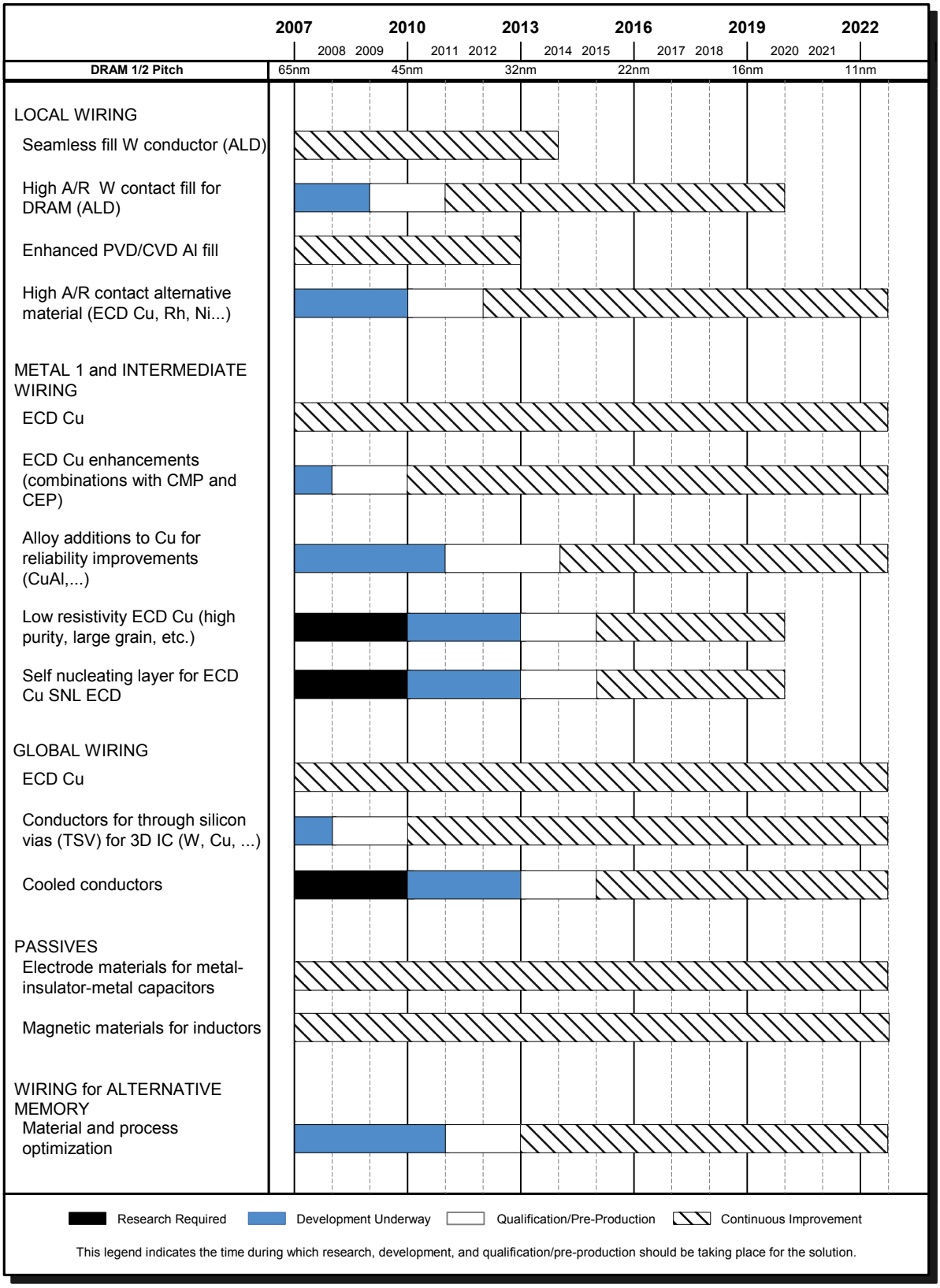


*Figure INTC7 Conductor Potential Solutions*



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## NUCLEATION POTENTIAL SOLUTIONS

The conformality and coverage of the nucleation layer is often the critical factor in determining whether the subsequent conductor deposition will be seamless or free of voids. For local wiring and contact fill, there will be continued improvement in ALD W nucleation layers that have been used to enable seamless or high aspect ratio W fill. These ALD nucleation layers must are usually extremely thin so that the overall conductivity of the plug is generally improved.

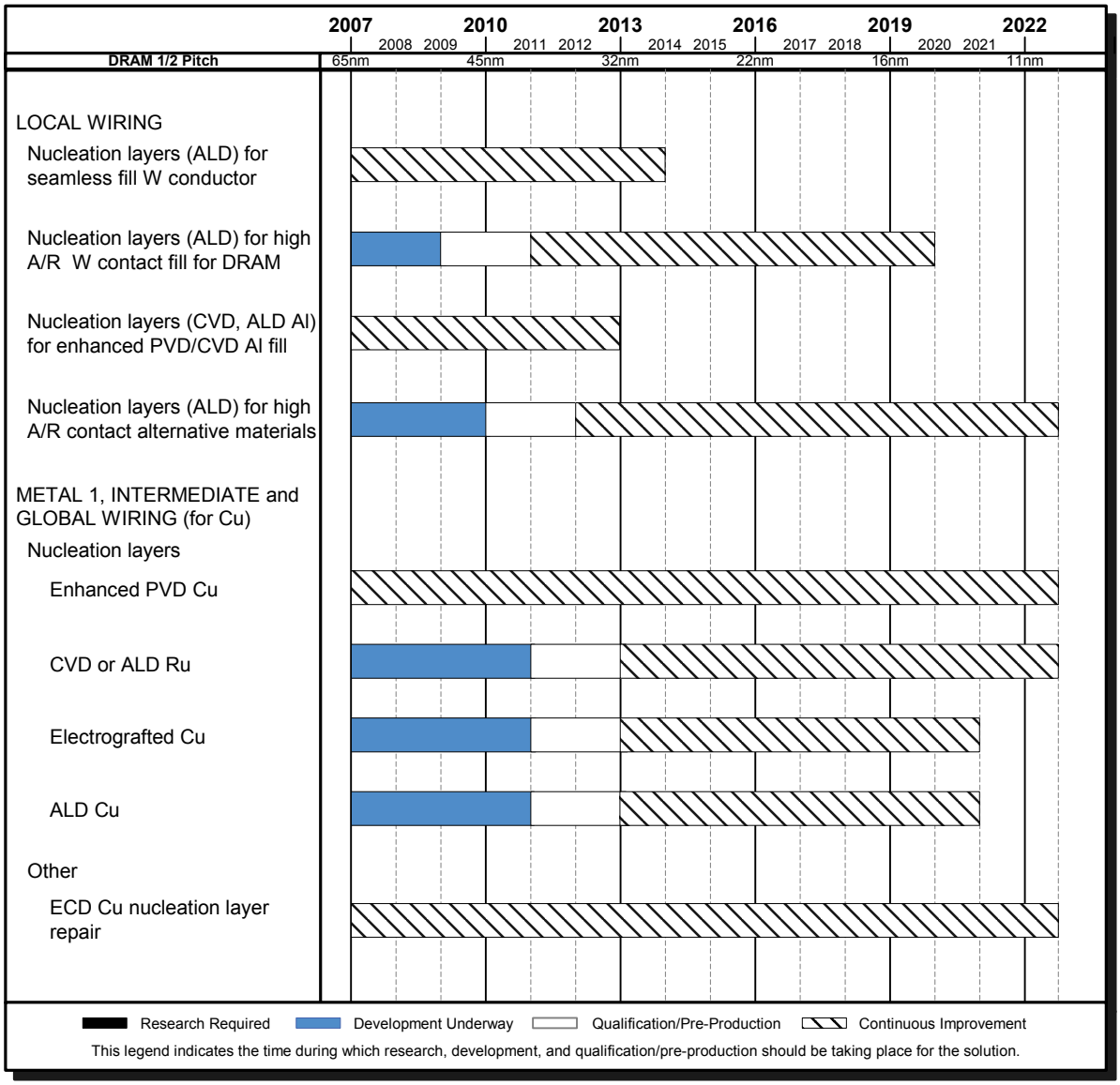


*Figure INTC8 Nucleation Potential Solutions*

An ALD WN [2, 3] process is being developed as a combined barrier and nucleation layer as an alternative to CVD TiN. The alternatives to W as a contact plug include both ECD Cu and ECD Rh. The potential nucleation layers for Cu are discussed below while Ru [4] has been proposed as a nucleation layer for Rh. In the area of Al fill, the CVD Al nucleation layer may be extended to ALD to allow continuous improvement in the fill characteristics of this technology. Development is still underway for alternative materials and processes for high aspect ratio DRAM contacts but ALD nucleation layers will likely be needed for this technology. For Metal 1, intermediate and global wiring, enhanced PVD Cu [24, 25] deposited through either long throw or various ionized techniques continues to be the dominant nucleation layer for ECD Cu. Improvement has been made in the sidewall coverage and uniformity of these layers, which will allow their use at the tightest dimensions of the 45 nm and potentially 32 nm technology. In addition, PVD Cu nucleation layers will continue to be used on the global wiring levels with larger critical dimensions. Eventually, these enhanced PVD techniques will not be able to provide reliable nucleation layers at the M1 and intermediate wiring levels and they will be


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replaced by ALD technology. Several nucleation layer options, including electroless [26], ALD, and electrografted Cu technology [27], continue to be researched. Although ALD Ru [28] seems to be only a marginal barrier to Cu diffusion, it does appear to be a very good nucleation layer for ECD Cu. Therefore it may be used in conjunction with other barriers, such as either ALD TaN or ALD WNC. Another potential solution to the problem of marginal PVD Cu sidewall coverage is repair of the nucleation layer [29] through ECD techniques. A more elegant solution involves modification of the ECD process and/or barrier to be self-nucleating, thereby eliminating the need for a Cu nucleation layer.

## PLANARIZATION POTENTIAL SOLUTIONS

Planarization is an integral part of the process flow for advanced interconnects. Chemical mechanical polishing and near alternatives remain the leading planarization technologies of interest. The number of unique planarization applications continues to increase with the introduction of new materials and new structures created from existing materials. With the increased use and maturity of CMP, there has been more focus on control of defects, cost, and dimensional variation for each application. The needs for each application drive the needs for specifically tuned consumables and flexible equipment that are combined to produce a process resulting in the desired planarization and control.

The planarization potential solutions chart, Figure INTC9, is broken into three sections. The first details a timeline for the Major Applications. This timeline serves as a preface to the potential solutions described in the Equipment and Consumables sections that follow. The applications are categorized as dielectrics or conductors.

For the dielectric applications, shallow trench isolation (STI) is included. Though not part of the interconnect process, it shares similar needs with other CMP steps and is not covered in detail in other sections of the roadmap. The need for STI will likely be reduced in future technology generations as new raised transistor structures are implemented that can be isolated using the pre-metal dielectric (PMD) film. The current PMD planarization step is being used with both a target method (stopping in the bulk film at a target thickness) primarily for logic, and a selective method (stopping on an underlying film) primarily for DRAM. Interlevel dielectric CMP is no longer required for advanced logic and is being phased out of memory as copper interconnects are implemented.

The evolution of new planarization applications is a certainty; however, planning for them is difficult. The use of PMD CMP steps with relatively to low or even reverse selectivity between oxide and nitride will be driven in logic technologies by new transistor schemes. The requirements of non-volatile memory schemes are leading to other needs, such as CMP of GeSbTe alloys.

For the conductor applications, polysilicon CMP is used for DRAM and flash memory today and will eventually be replaced. Tungsten CMP has been the mainstay for contacts and also for DRAM vias. Its use will drop as new contact metals are implemented for some devices and as memory completes the transition to copper interconnects. Copper and barrier CMP is seeing change as the barrier metals, dielectric films, and hardmask materials are all changing over time. The challenges of achieving planarity and controlling film loss will continue to drive innovation. Additional challenges to defectivity, effective κ value, and sheet resistance in more complex film stacks involving porous ultra-low-κ materials is receiving more attention. The impact of the exponential rise in the resistivity of the narrowest lines due to electron scattering will drive tighter film loss control. In addition, the dielectrics between metal lines are increasingly fragile and prone to liquid absorption as well as damage. The adoption of ALD technology for barriers will result in more conformal depositions that will dramatically reduce the amount of barrier material that can be used as a CMP stop during copper planarization. The choice of materials used for the barrier will also change over time. All these factors are leading to the need for research and development into new generations of copper and barrier processes. Factories are also faced with supporting the use of a variety of dielectric films across the interconnect levels within a technology generation.

New planarization applications for conductors will also be required. Planarization of noble metals for memory capacitors has been delayed, but is still likely. The need for planarization for metal gates is possible as materials and integration schemes are decided. Tungsten contacts in some devices will be replaced with a better conductor. Interest in aluminum damascene wiring has also resurfaced. A variety of metals and alloys are being utilized in non-volatile memory (NVM) chips. Self-aligned top diffusion barriers, such as CoWP, are being investigated for reliability benefits and to support air-gap integration. They have imperfect deposition selectivity today and may require a CMP buff step. 3D IC's are also driving new needs.

Development will continue in equipment. Integrated wafer buffing and cleaning are standard on polishing equipment and will need to be able to handle tailored solutions. Post-CMP wafer cleaning is becoming more closely integrated with the planarization process. In the future, cleaning solutions will be increasingly tailored to the planarization application that they follow. This customized cleaning approach results from the presence of unique combinations of chemistries, particles, and films present. The mechanical energy for cleaning will continue to be applied by buff pads, brushes, and contact-less methods. Various polish endpoint detection techniques are used today, with inline film thickness metrology



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as an available option. Next generation tools may include a range of inline metrology to measure forces, temperatures, planarity, and defectivity and also allow for automatic process control (APC). Equipment, especially for copper and barrier, will need to operate at lower stress levels in order to minimize the damage to fragile films. The stress will have to be radially tunable in order to achieve excellent non-uniformities in removal rate and recess.

Development of alternative planarization techniques has gained in importance. These options today include concepts being developed such as chemically enhanced planarization and electro-chemical-mechanical planarization for conductors in order to obtain removal with low stress. More concepts will be required over time to achieve very low stress levels.

Consumables are the largest contributor to many planarization performance metrics, so significant advances will be required. High solids slurries utilized today are being driven to increased consistency, especially in defectivity. Development of slurries with lower defectivity is critical to the simultaneous achievement of improved productivity with better planarity and defectivity and cost. Novel chemistries that shift to more chemically-driven removal will help defray the productivity loss associated with decreasing mechanical stresses. The abrasives used will have to be engineered to fit their applications.

Significant advances will also be needed from both hard and soft pads, usually made with urethanes, and used across the applications. Pads that contain abrasives are used mainly for STI today. There is a strong need for development of a wide range of pad types that can be paired with slurries by application. Many of the alternative planarization techniques will need robust manufacturing-ready fluids in order to enable the technique. Advanced pad conditioning methods are also needed. Technologies need to be developed that can simultaneously offer consistent performance in planarity, defectivity, and productivity. To respond to large numbers of planarization applications and different integration schemes for each, formulations will be increasingly optimized from tunable platforms to offer unique performance.


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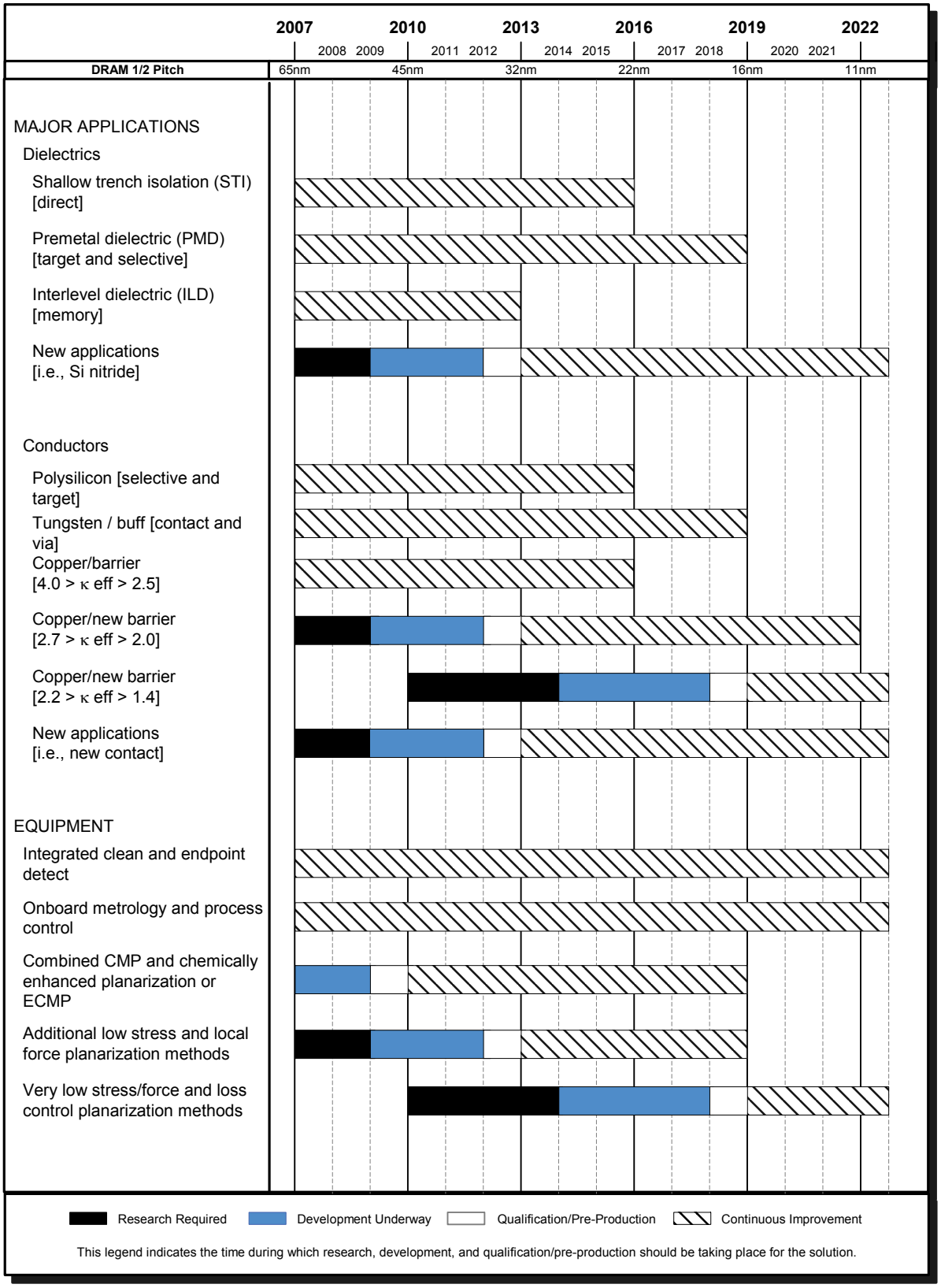


*Figure INTC9 Planarization Potential Solutions*



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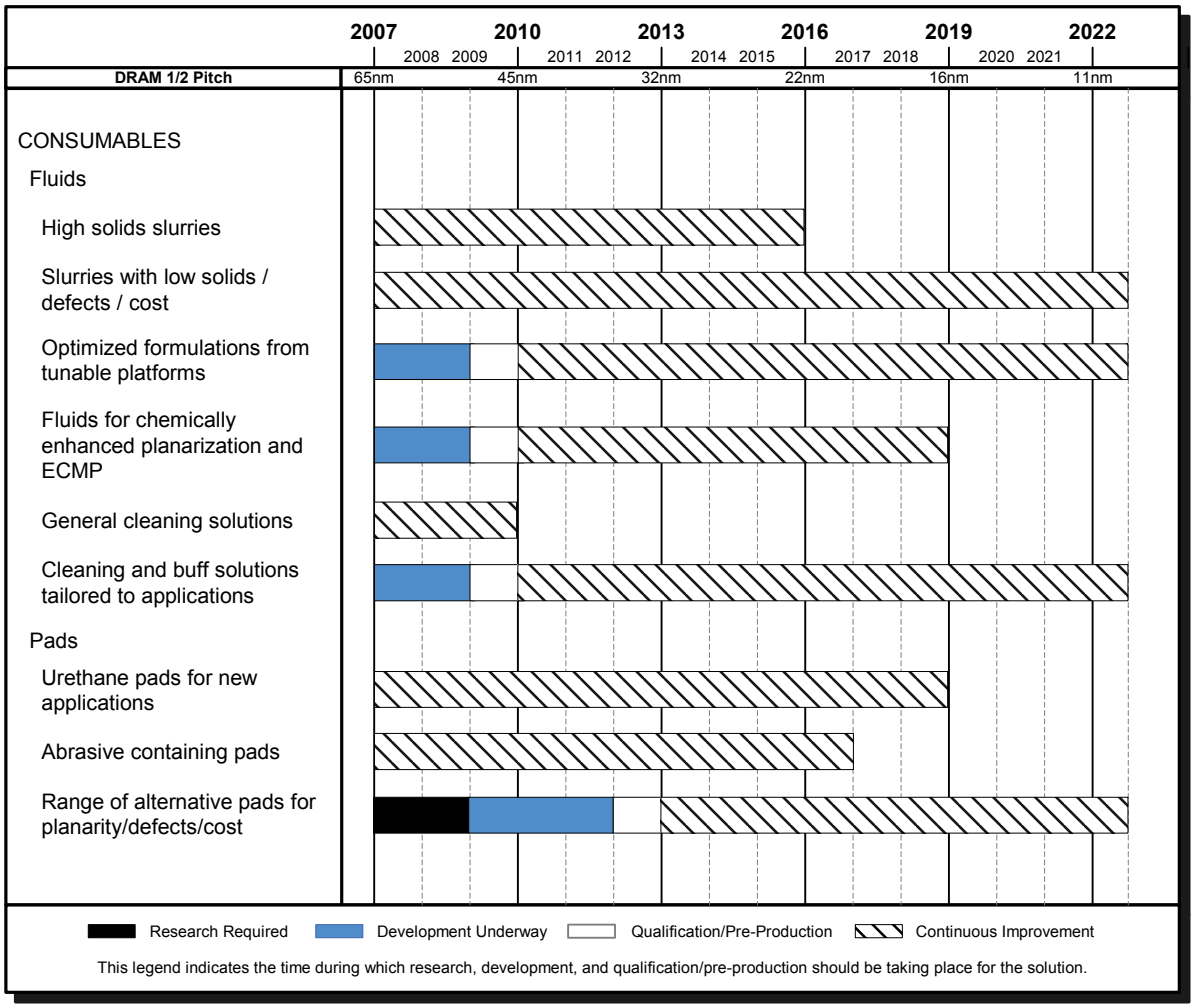


*Figure INTC9 Planarization Potential Solutions (continued)*

## ETCH POTENTIAL SOLUTIONS

At the 45 nm half-pitch technology generation and beyond, copper interconnect is likely to become the unified BEOL technology for both logic and memory devices. As the aluminum interconnect suffers from high resistance because of narrow width effect and poor fidelity pattern transfer, their applications will likely fall from the mainstream and into a niche for a limited number of specialty memory devices. The interconnect design rules are likely to be identical for both memory and logic devices. The impact of these consolidations of BEOL technology requirements could be profound. One could foresee jumbo size back-end only factories that support high volume manufacturing of both logic and memory devices. Future factory investments may take advantage of this synergy to maximize factory utilization by investing in cost effective back-end-only facilities for mixed logic and memory manufacturing.

On the etch technology front, dielectric etch challenges will still be dominant in logic technology where a variety of inorganic, organic, or hybrid materials will be used to meet $\kappa_{eff}$ requirements. Combinations of these materials will also be employed to take advantage of material dependant etch selectivities to improve the three dimensional (3D) critical dimension (CD) control, *i.e.,* widths and depth. A multiple layer resist scheme will be required for better dimensional control regardless of whether a hard mask integration scheme is employed. These advances will improve the line edge roughness (LER) and allow thinner resist requirements for high fidelity image transfer. Continual refinement of current capacitively coupled plasma (CCP) source technology is expected to be able to address the material challenges adequately as well as shrinking trench and via dimensions at nearly constant aspect ratios. With the advances of porous low dielectric constant materials, ULK materials, and selective air-gap technology, metal hard mask implementation to reduce the ash damage is gaining momentum. Continual refinement of the current inductively coupled plasma (ICP) technology is


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expected to be able to meet the metal hard mask requirements. With metal hard mask material exposure in the CCP chamber, process cleanliness and process stability could be a challenge due to the low volatility of the bi-products of the etch chemistry, chamber material, and the hard mask material. Advanced chamber material selection and chemistry optimization are required for high yield and excellent uptime and utilization. On the other hand, interconnect embedded implementations of MIM capacitors with high dielectric constant materials, inductors and ground plane design for signal integrity may favor a subtractive method for structural formation. This may ensure a long-term dependency on ICP source technology and could more than off-set the reduction in demands for aluminum interconnect etch.

If hard mask technology is not used, resist strip will be a constant challenge for low-κ and ULK integration. Damage free photoresist and residue removal would be facilitated by the development of etch processes that produce less deposited residue and/or re-deposited sputtered material, such as Cu sputtered during etch stop open. Low damage photo resist and residue removal is facilitated by source technology that provides more directionality than is available from conventional high-pressure strip systems. Additional damage repair and/or pore sealing steps might be required for porous ULK dielectric etching. These requirements might force the expansion of etch or strip tools into multi-station systems. Problems such as moisture absorption or the reaction of moisture with damaged dielectrics could require *in situ* process flows that include etch, dry strip, wet strip, damage repair, degas, and pore sealing steps. Ultimately, etch or strip tools could come to resemble PVD cluster platforms. Such platforms might also facilitate other processes where a mixed variety of materials are present or where exposure of residue to the atmosphere would make it more difficult to remove. The extendibility of plasma-based dry strip technology is a concern. It might be necessary to replace it with alternative technologies at very advanced technology generations.

Beyond the 45 nm half-pitch technology generation, new classes of multi-gigabit non-volatile memory devices *, i.e.,* PRAM, RRAM, MRAM, FeRAM, etc., will be introduced and compete to become the mainstream devices. These new devices will confound the separation between memory and logic technologies and further reinforce the convergence of the BEOL technology. These devices employ a standard CMOS FEOL while the memory elements are embedded between BEOL interconnects. The number of metallization layers for these new classes of memory will rival that of the most advanced logic devices. These technologies will fit in very well with the megafactories of the future. These devices typically employ refractory, noble or near-noble metal electrodes*, i.e.,* platinum, nickel, silver, and iridium. The dielectric materials are typically, GeSbTe, refractory metal oxides, perovskites, and rare earth metal oxides. The most aggressive configurations of these devices are in the cross-point memory array configuration*, i.e.,* 1D-1R (one diode/rectifier and 1 resistor). The rectifier is likely to be a metal-insulator-metal MIM-type diode device. The processes currently used for these refractory metal electrodes, dielectric materials and ferroelectric materials have high sputter components and the profile is not desirable. Unacceptable leakage can result from the re-deposition of etch products on memory structure sidewalls and therefore new etch chemistries that produce higher volatility products are desirable. Source cathode/chuck designs capable of operating at 500ºC might also be required. A vertical memory stack profile is an enabler for future scaling and is a major challenge. However, it is anticipated that current source technology will address future needs with continual refinement and chemistry innovations.

Continued scaling for current memory technology is anticipated with ever increasing aspect ratio with the memory capacitor elements. However, it is anticipated that current source technologies for dielectric trench and silicon trench will also be continually improved to address future needs. Due to the high cost of lithography tooling, lower cost pitch doubling technology is expected to play a major role in the back-end process, especially in memory technology. Multiple portable film layers will need to be etched to define the final pattern. Current source technologies are anticipated to be able to fill these requirements.

3D IC stacking technologies require etching vias through the entire depth of a thin wafer. Such etch processes have been demonstrated using current source technologies. These technologies, with continuous improvement, are expected to be able to meet future requirements. Through wafer via etching removes relatively large amounts of material per wafer, therefore high atomic weight inert gases are being investigated as a means to accelerate etch rates. Reactor availability is also affected by the large amounts of etched materials. More effective means of reducing reactor down time will have to be investigated for high volume manufacturing.

Unintended side effects of plasma etch on global warming is always a concern and cannot be ignored. Plasma etching and cleaning in the IC industry contribute an insignificant amount of greenhouse gas emissions relative to the total. However, the industry is subject to new environmental laws, therefore, development and introduction of more environmentally friendly etch chemistries is anticipated.



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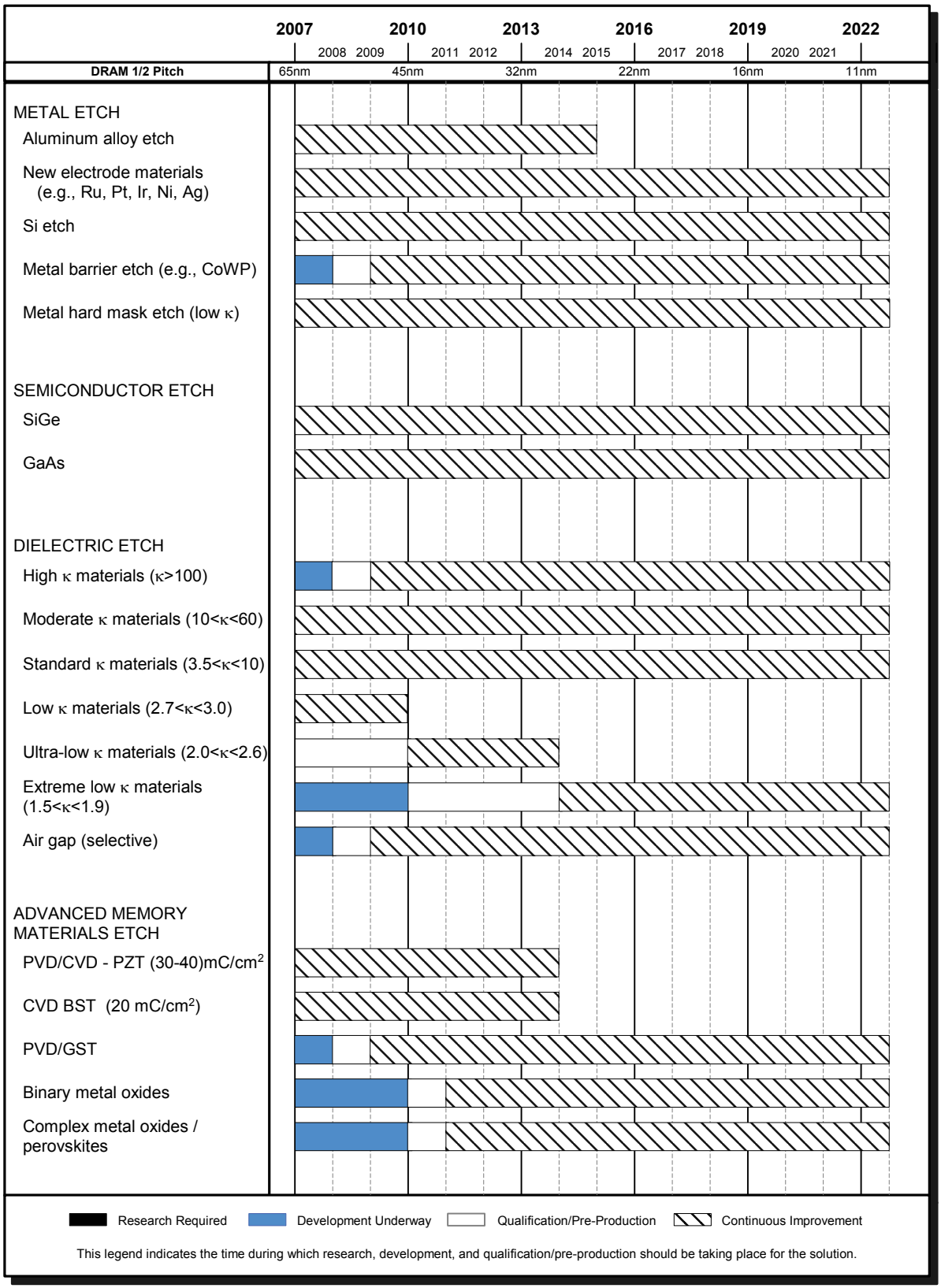


*Figure INTC10 Etch Potential Solutions*



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## INTERCONNECT SURFACE PREPARATION

Interconnect structures based on copper and ultra low-κ materials continue to present difficult surface conditioning challenges which are exacerbated by the high aspect ratio structures for contacts and capacitors. Interconnect surface preparation includes post-etch photoresist stripping, post-strip residue removal, post-CMP cleaning for dielectrics and metals, pre-deposition cleaning for dielectrics and metals and post-deposition cleaning for dielectrics and metals. New requirements for surface preparation include improving interfacial adhesion, improving dielectric and barrier reliability, repairing etch damage, and sealing pores in dielectric sidewalls. Etch and ash damage may take the form of surface chemistry changes, film densification, and sidewall and trench bottom roughness. The main focus in Table INTC4a and b is dual damascene processing involving copper metal and low dielectric constant insulators. Interconnect necessarily involves several other metallic films as barriers and seed layers as well as silicon oxide and silicon nitride dielectric films as etch stops and hardmasks.

Wet cleaning, plasma cleaning, UV/laser cleaning, and other dry cleaning methods, such as cryogenic aerosols, are all being considered as potential solutions. No one technique or technology has solved all the technical challenges for surface conditioning. For example, plasma stripping is cost-effective for removing photoresist and residue, but is unable to remove metallic contamination. Wet cleaning is effective for removing metallic contamination, but drying of high aspect ratio features has proven challenging. It is also evident that plasma stripping can induce damage to dielectrics making them more vulnerable to CD loss during wet clean.

Although surface conditioning is generally considered as a separate, stand-alone process, in some cases, *e.g.,* CMP, a technical advantage is achieved when the surface conditioning step is incorporated into the process tool. The combination of various surface-conditioning methods has proven successful for cleaning the wafer surface. For example, a typical post-etch cleaning sequence for the trench step of dual damascene and then the subsequent dielectric barrier removal includes the trench etch, an *in situ* post-etch photoresist strip and dielectric barrier removal all in one etch/clean cluster tool chamber. For porous low-κ materials, additional damage repair and pore sealing processes may be included *in situ*, to limit increases in $\kappa_{eff}$ and to prevent penetration of the barrier metal into the porous low-κ dielectric.

As DRAM manufacturing migrates to copper interconnect, it must address the same surface conditioning issues that logic faces. Additionally, high aspect ratio features such as contacts and cylindrical capacitors are difficult both to clean and to dry. The front surface, back surface, and edge of the wafer must be effectively cleaned of particles, metallic and organic contamination. The surface must not be roughened and the materials must not be affected. Some remediation may be necessary to limit sidewall roughness (resulting from either plasma or cleans processes) and its concomitant impact on barrier and line resistivities.

Challenges and potential solutions for interconnect surface preparation are primarily based on copper and low-κ integration schemes. Refer to Figure INTC11. For the near term, the low-κ dielectrics will be dense or nano-porous materials. For these materials, sidewall damage that may occur during etch, resist strip and clean can have a major impact on the effective κ-value of the dielectric, as well as the reliability and yield. Cleaning (residue and particle removal) on extremely hydrophobic, high aspect ratio structures, presents unique challenges. Copper films must be cleaned without corrosion, especially around the barrier-copper interface, and the final surface must assure electrical contact by being free of thick oxide layers. Copper from the edges and backside of the wafer must be cleaned to prevent undesirable migration of the copper to the transistor.

Meso-porous low-κ dielectrics—expected to be integrated by 2012—present extreme surface preparation challenges because their large pore density allows etch and surface preparation chemistries/plasmas to penetrate deeply into the dielectric. This can result in deep, sub-surface damage with subsequent increases in the dielectric constant, decreased dielectric breakdown, dielectric voiding, and reduced reliability. Porous, carbon-containing ultra-low-κ dielectrics integration may prove especially difficult. Surface preparation and cleaning techniques being investigated for this generation may extend beyond wet and plasma cleaning to supercritical fluids, cryogenic aerosols, and laser cleaning. Advanced wet, plasma, and thermally activated techniques are believed to be extendable into the future, as improvements to these technologies are expected. Sealing of surface pores may be needed to enable use of thin ALD barriers and prevent barrier penetration into the dielectric. Several wet and dry techniques are being investigated.

Wet cleaning will continue to be the method of choice for post-CMP, post-strip, and pre-deposition cleaning for at least the foreseeable future. Cleaning of copper and low-κ dielectric materials can be accomplished by wet methods or wet plus dry combinations. Dilute acid-based formulations with additions of fluorine-based chemicals, surfactants, chelating agents, and/or corrosion inhibiting agents will be used. Other advanced wet cleaning techniques, such as the use of dilute solutions of ozone, supercritical fluids, or other unique approaches are still in the research stage and may be used should the conventional techniques fail to deliver adequate performance.

Carbon-containing low-κ dielectric films present the problem of a hydrophobic surface, which is difficult to rinse and dry without creating watermarks or leaving undesirable surfactant residue. This challenge might be addressed with front end



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surface preparation techniques such as surface tension drying or may drive the introduction of new processes and new chemicals that can replace 2-propanol. In addition, shrinking critical dimensions are creating more fragile structures and will require cleaning processes that are damage-free.

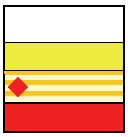
Particle removal is becoming more important as geometries continue to shrink. Backside, edge, and front-side particle removal must be accomplished to clean a wafer successfully. New methods being investigated include the extension of megasonics, brush, and other physical methods that minimize wafer damage. Edge and backside particles are known to cause yield degradation, however, quantification is difficult. New tools are being developed that can measure the particles on the edge and backside, and will allow correlation to the yield impact.

Cleaning processes and chemical formulations will address environmental, health, and safety issues by using less concentrated, less hazardous, and more environmentally friendly chemicals. Fluorine-based chemicals and chelating agents in particular have disposal issues. Reducing water usage is also a goal.

*Table INTC4a Interconnect Surface Preparation Technology Requirements—Near-term Years*

| *Year of Production* | *2007* | *2008* | *2009* | *2010* | *2011* | *2012* | *2013* | *2014* | *2015* | *Driver* |
|---|---|---|---|---|---|---|---|---|---|---|
| *DRAM ½ Pitch (nm) (contacted)* | *65* | *57* | *50* | *45* | *40* | *36* | *32* | *28* | *25* | *D ½* |
| *MPU/ASIC Metal 1 ½ Pitch (nm)(contacted)* | *68* | *59* | *52* | *45* | *40* | *36* | *32* | *28* | *25* | *M* |
| *MPU Physical Gate Length (nm)* | *25* | *22* | *20* | *18* | *16* | *14* | *13* | *11* | *10* | *M* |
| *Wafer diameter (mm)* | **300** | **300** | **300** | **300** | **300** | **300** | **300** | **450** | **450** | *D ½, M* |
| *Wafer edge exclusion (mm)* | **2** | **2** | **2** | **2** | **2** | **2** | **2** | **2** | **2** | *D ½, M* |
| *Front surface particles* | | | | | | | | | | |
| Killer defect density, $D_pR_p$ (#/cm$^2$) [A] | **0.023** | **0.016** | **0.02** | **0.025** | **0.016** | **0.02** | **0.025** | **0.016** | **0.02** | *D ½* |
| Critical particle diameter, $d_c$ (nm) [B] | **32.5** | **28.5** | **25** | **22.5** | **20** | **17.5** | **16** | **14** | **12.5** | *D ½* |
| Critical particle density, $D_{pw}$ (#/wafer) [C] | **80** | **54** | **68** | **86** | **123.3** | **155** | **195** | **123.1** | **155** | *D ½* |
| *Back surface particles* | | | | | | | | | | |
| Back surface critical particle diameter (nm) [D] | **0.16** | **0.16** | **0.14** | **0.14** | **0.14** | **0.14** | **NA** | **NA** | **NA** | *D ½* |
| Back surface critical particle density (#/wafer) [E] | **200** | **200** | **200** | **200** | **200** | **200** | **NA** | **NA** | **NA** | *D ½* |
| *Edge bevel particles* | | | | | | | | | | |
| Edge bevel critical particle diameter (nm) [F] | **130** | **114** | **100** | **90** | **80** | **70** | **64** | **56** | **50** | *M* |
| Particles (cm$^{-2}$) (G) | **TBD** | **TBD** | **TBD** | **TBD** | **TBD** | **TBD** | **TBD** | **TBD** | **TBD** | *M* |
| Particles (#/wafer) (G) | **TBD** | **TBD** | **TBD** | **TBD** | **TBD** | **TBD** | **TBD** | **TBD** | **TBD** | *M* |
| *Metallic Contamination* | | | | | | | | | | |
| *Critical front surface metals ($10^9$ atoms/cm$^2$) (H)* | **10** | **10** | **10** | **10** | **10** | **10** | **10** | **10** | **10** | |
| *Critical back surface metals (Cu) ($10^9$ atoms/cm$^2$) (I)* | **500** | **500** | **500** | **250** | **250** | **250** | **100** | **100** | **100** | |
| *Mobile ions ($10^{10}$ atoms/cm$^2$) [J]* | **2.5** | **2.5** | **2.5** | **2.5** | **2.5** | **2.5** | **2.4** | **2.4** | **2.4** | |
| *Organic contamination ($10^{13}$ C atoms/cm$^2$) [K]* | **1.2** | **1** | **0.9** | **0.9** | **0.9** | **0.9** | **0.9** | **0.9** | **0.9** | |
| *Cleaning Effects on Dielectric Material* | | | | | | | | | | |
| Maximum dielectric constant increase due to Etch, Strip + Clean [L] | **2.50%** | **2.50%** | **2.50%** | **2.50%** | **2.50%** | **2.50%** | **2.50%** | **2.50%** | **2.50%** | |
| Maximum dielectric constant increase due to rework [L] | **2.50%** | **2.50%** | **2.50%** | **2.50%** | **2.50%** | **2.50%** | **2.50%** | **2.50%** | **2.50%** | |
| Maximum effect on dielectric critical dimension due to dry Strip [M] | **1%** | **1%** | **1%** | **1%** | **1%** | **1%** | **1%** | **1%** | **1%** | |
| Maximum effect on dielectric critical dimension due to Strip + Clean [M] | **1.50%** | **1.50%** | **1.50%** | **1.50%** | **1.50%** | **1.50%** | **1.50%** | **1.50%** | **1.50%** | |

*Manufacturable solutions exist, and are being optimized*
*Manufacturable solutions are known*
*Interim solutions are known*
*Manufacturable solutions are NOT known*





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*Notes for Tables INTC4 and b:*

*[A] Killer defect density is calculated from the formula for 99% yield, $Y=0.99=exp[-D_pR_pA_{eff}]$. $A_{eff}$ is the effective chip area, $D_p$ is the defect density, and $R_p$ is a defect kill factor indicating the probability that a given defect will kill the device. The product $D_pR_p$ is the density of device-killing defects on the wafer. $R_p$ is dependent on numerous things including the size and shape of the particle, the composition of the particle, and specifics of the device layout. In previous years, $R_p$ was assumed to be 0.2 for any particle > the critical particle size, $d_c$. $A_{eff}$ is assumed to be the same as for Front End Surface Preparation. For DRAM, $A_{eff}=2.5F^2T+(1-aF^2T/A_{chip})*0.6A_{chip}$. where F is the minimum feature size, a is the cell fill factor, T is the number of DRAM bits (transistors) per chip, and $A_{chip}$ is the DRAM chip size. For MPUs, $A_{eff}=aT(GL)^2$, where GL is the gate length. Because $A_{eff}$ can increase or decrease with each successive technology generation, $D_pR_p$ does not always decrease over time.*

*[B] Critical particle diameter, $d_c$, is defined by Yield Enhancement as ½ of the metal ½-pitch dimension. This should be considered an "effective" particle diameter as most particulate contamination is irregular in shape.*

*[C] An example is provided which assumes that the kill factor, $R_p$, is 0.2 for all particles larger than the critical particle size. This is the assumption made in previous versions of the roadmap, but is not universally valid and is included only for purposes of an example calculation. Particles/wafer is calculated using $[R_p*3.14159*(\text{wafer radius-edge exclusion})^2]$. To convert from particles/wafer at the critical particle size to particles/wafer at an alternative size, a suggested conversion formula is: $D_{alternate}=D_{critical}*(d_{critical}/ d_{alternate})^2$.*

*[D] and [E] Metrics for Backside particle critical diameter and count have been taken from the requirements from table from the FEOL surface preparation document. .*

*[F] and [G] Edge bevel critical particle size is taken as 2* DRAM ½ Pitch. The size was determined to be particles that could be shed and then distributed onto the wafer surface causing detrimental yield reduction. Few references exist correlating edge defects with yield, however, minimization of the particle size and density is important. The levels are still under evaluation, however, and no values are presented here, although current practices indicate edge bevel particle adders for any interconnect process step, in particular CMP, should be less than 4 defects per quadrant of the wafer. Again, this value should be treated as guidance, not a specification.*

*[H] Front surface metallic contamination levels are based on degradation of yield from metallic diffusion into the transistor or leakage of the device from metal migration. Data shows that Cu levels <1E+13 can cause interconnect leakage and <1E+10 can cause transistor degradation. The ability of the Cu to diffuse into the dielectric and then through the silicon to the transistors is questionable as many references site the fact that Cu cannot diffuse though thick silicon, nevertheless, the lower the Cu contamination the better. The levels are still under evaluation, however, and the values presented here should be treated as guidance, not a specification.*

*[I] Back surface Cu contamination levels are based on degradation of electrical parameters of the transistor caused by Cu diffusion through the silicon. Many studies have been undertaken that evaluate the effects of backside Cu contamination on the transistors. The most profound affect is TDDB due to electric field drift. Oxygen on the back surface prevents the diffusion into the silicon. However, once in the silicon the Cu will diffuse and precipitate, dependent on thermal treatments. Various references quote a concentration as high as 1E+15 and others quote as low as 1E+11 as degrading device performance, dependent on test device structures and film thicknesses. Again, the levels are still under evaluation and the values presented here should be treated as guidance, not a specification. Reference: A. A. Isrtatov and E. R. Weber, J. Electrochem. Soc. 149(1) G21(2002).*

*[J] Mobile ions for interconnect are less stringent than the front end line metrics. Although the mobile ions can lead to the same electrical degradation and do the same damage from migration through the dielectric, the oxide does getter some of the sodium. For backside contamination levels, use the front end values. For interconnect, the causes shown here are guidance as to allowable levels, approximately twice the value of the front end metrics.*

*[K] Organic contamination is usually in the form of a thin layer of hydrocarbon remaining on the wafer after resist strip and clean and after post-CMP clean. Leaving this film may result in undesirable delamination of subsequently deposited layers or "carbon spots" caused by a monolayer or more of BTA (benzotriazole)-copper complex. A monolayer, about 1 nm of BTA on copper yields a carbon atom density of about 4E+14 atoms/$cm^2$. Carbon residues may also come from inadequately stripped resist or shedding of particles from process chambers. The same metric is used for interconnect as the front end, $D_c$ at the 180 nm corresponded to 10% carbon atom coverage of a bare silicon wafer (7.3E+13atoms/$cm^2$). $D_c$ for subsequent generations was scaled linearly with the ratio of CD to 180 nm. $D_c = (CD/180)(7.3E+13)$.*

*[L] Etching, stripping and cleaning processes are known to have a detrimental effect on the dielectric constant of insulating layers. This is especially true for porous dielectric materials. It is essential to minimize and eventually eliminate this effect. Rework of photolithographic patterning involves stripping and cleaning and can have similar effects on the dielectric constant. These values are guidance for allowable degradation of the dielectric constant. Changes to the dielectric constant need to be measured (at a minimum) by interdigitated trench test structures, as measurements on planar films through MIS capacitor measurements are generally not representative of integrated structures. One common approach is to compare measured RC products with those from computer simulations assuming bulk dielectric constant values. The difference between the measurement from the simulation can be representative of the etch/strip/clean damage. The color change from Yellow to Red in 2012 reflects the dielectric change to a κ-value of < 2.1.*

*[M] Current etch and strip methods can damage porous low-κ films through the removal of carbon species; however, the extent of this damage may not be fully determined until after subsequent wet cleans. The CD loss after etch and strip may be negligible, but, following wet clean, the CD loss may become significant. Because the clean can remove film thicknesses rendered vulnerable by the etch, the extent of CD loss after wet cleans can be the result of both the etch and cleans processes. While not explicit in measurable CD loss, bowing of the trench and via structures should be minimized to allow conformal liners and plating base deposition and to reduce copper voiding effects. The color change from Yellow to Red in 2012 reflects the dielectric change to a κ-value of < 2.1.*



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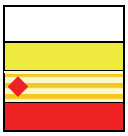
*Table INTC4b Interconnect Surface Preparation Technology Requirements—Long-term Years*

| *Year of Production* | *2016* | *2017* | *2018* | *2019* | *2020* | *2021* | *2022* | *Driver* |
|---|---|---|---|---|---|---|---|---|
| *DRAM ½ Pitch (nm) (contacted)* | *22* | *20* | *18* | *16* | *14* | *13* | *11* | *D ½* |
| *MPU/ASIC Metal 1 ½ Pitch (nm)(contacted)* | *22* | *20* | *18* | *16* | *14* | *13* | *11* | *M* |
| *MPU Physical Gate Length (nm)* | *9* | *8* | *7* | *6* | *6* | *5* | *4* | *M* |
| *Wafer diameter (mm)* | **450** | **450** | **450** | **450** | **450** | **450** | **450** | *D ½, M* |
| *Wafer edge exclusion (mm)* | **2** | **2** | **2** | **2** | **2** | **2** | **2** | *D ½, M* |
| *Front surface particles* | | | | | | | | |
| Killer defect density, $D_pR_p$ (#/cm$^2$) [A] | **0.014** | **0.017** | **0.022** | **0.02** | **0.018** | **0.017** | **0.016** | *D ½* |
| Critical particle diameter, $d_c$ (nm) [B] | **11** | **10** | **9** | **9** | **8** | **8** | **7** | *D ½* |
| Critical particle density, $D_{pw}$ (#/wafer) [C] | **106** | **133.4** | **168** | **150** | **150** | **150** | **150** | *D ½* |
| *Back surface particles* | | | | | | | | |
| Back surface critical particle diameter (nm) [D] | **NA** | **NA** | **NA** | **NA** | **NA** | **NA** | **NA** | *D ½* |
| Back surface critical particle density (#/wafer) [E] | **NA** | **NA** | **NA** | **NA** | **NA** | **NA** | **NA** | *D ½* |
| *Edge bevel particles* | | | | | | | | |
| Edge bevel critical particle diameter (nm) [F] | **44** | **40** | **36** | **32** | **32** | **30** | **30** | *M* |
| Particles (cm$^{-2}$) (G) | **TBD** | **TBD** | **TBD** | **TBD** | **TBD** | **TBD** | **TBD** | *M* |
| Particles (#/wafer) (G) | **TBD** | **TBD** | **TBD** | **TBD** | **TBD** | **TBD** | **TBD** | *M* |
| *Metallic Contamination* | | | | | | | | |
| *Critical front surface metals ($10^9$ atoms/cm$^2$) (H)* | **10** | **10** | **10** | **10** | **10** | **10** | **10** | |
| *Critical back surface metals (Cu) ($10^9$ atoms/cm$^2$) (I)* | **100** | **100** | **100** | **100** | **100** | **100** | **100** | |
| *Mobile ions ($10^{10}$ atoms/cm$^2$) [J]* | **2.3** | **2.3** | **2.3** | **2.3** | **2.3** | **2.3** | **2.3** | |
| *Organic contamination ($10^{13}$ C atoms/cm$^2$) [K]* | **0.9** | **0.9** | **0.9** | **0.9** | **0.9** | **0.9** | **0.9** | |
| *Cleaning Effects on Dielectric Material* | | | | | | | | |
| Maximum dielectric constant increase due to Etch, Strip + Clean [L] | **2.50%** | **2.50%** | **2.50%** | **2.50%** | **2.50%** | **2.50%** | **2.50%** | |
| Maximum dielectric constant increase due to rework [L] | **2.50%** | **2.50%** | **2.50%** | **2.50%** | **2.50%** | **2.50%** | **2.50%** | |
| Maximum effect on dielectric critical dimension due to dry Strip [M] | **1%** | **1%** | **1%** | **1%** | **1%** | **1%** | **1%** | |
| Maximum effect on dielectric critical dimension due to Strip + Clean [M] | **1.50%** | **1.50%** | **1.50%** | **1.50%** | **1.50%** | **1.50%** | **1.50%** | |

*Manufacturable solutions exist, and are being optimized*
*Manufacturable solutions are known*
*Interim solutions are known*
*Manufacturable solutions are NOT known*

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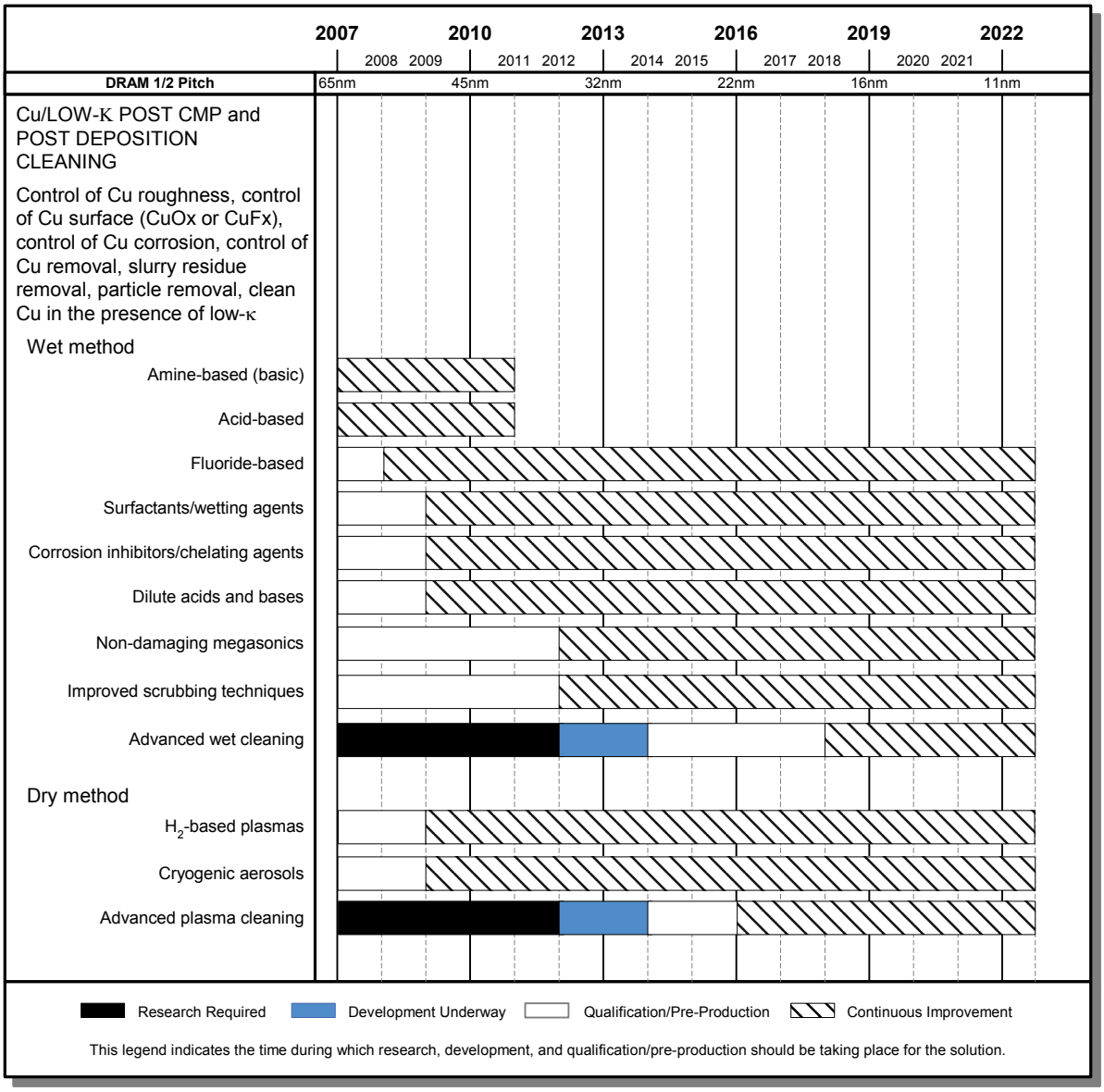


*Figure INTC11 Interconnect Surface Preparation Potential Solutions*



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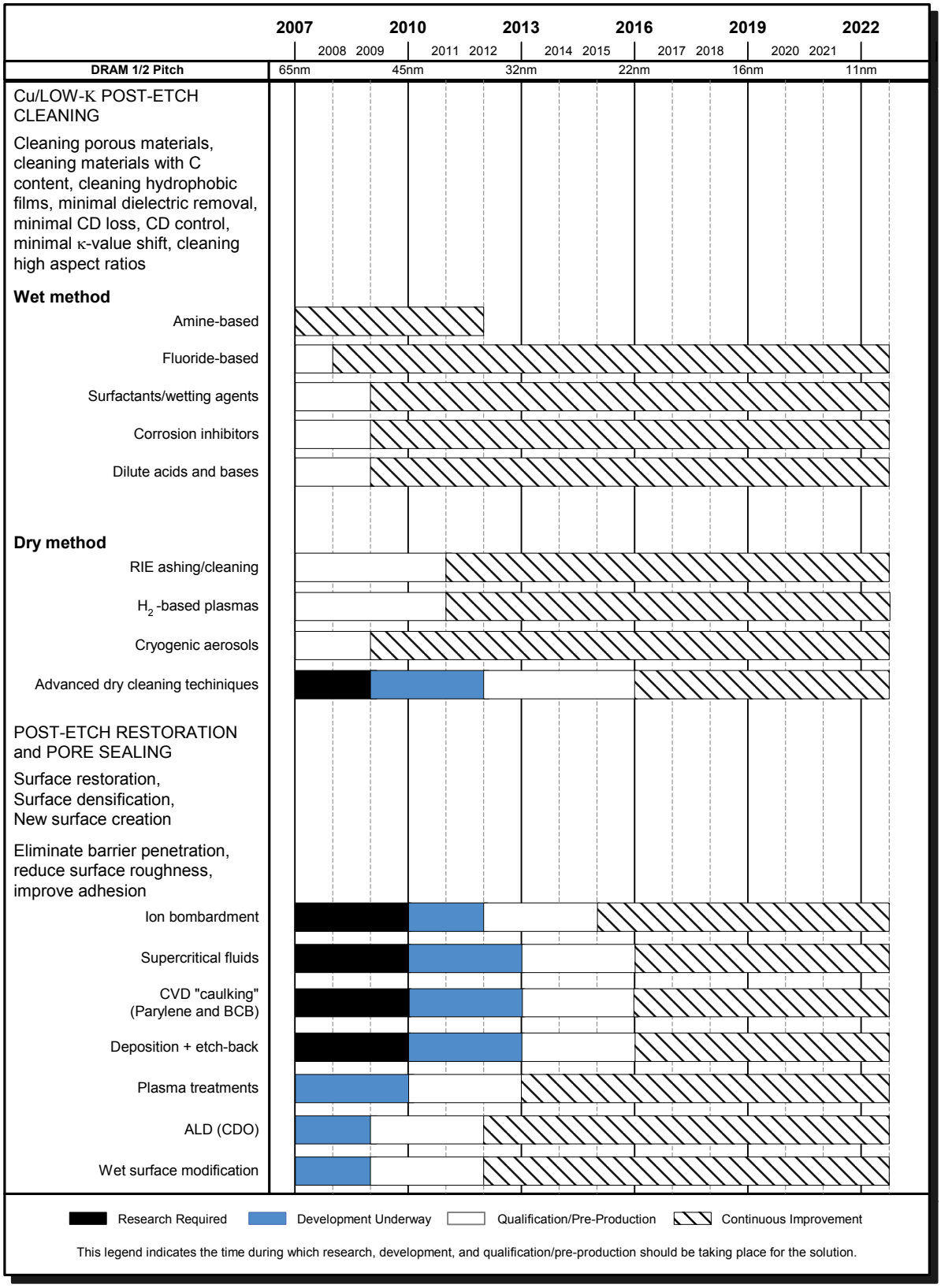


*Figure INTC11 Interconnect Surface Preparation Potential Solutions (continued)*



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# PASSIVE DEVICES

## INTRODUCTION

An increasing trend to move discrete passive devices from board level to chip level is a demanding new challenge for current and future on-chip interconnect architectures. The request for precision and high quality capacitors, inductors, and resistors is mainly driven by advanced mixed-signal, high frequency (RF) and system-on-a-chip (SOC) applications. Reduction and control of substrate coupling noise and other parasitics for mixed-signal and RF CMOS applications is one of the major tasks. From an application point of view the most important requirements for passives are listed in the *RF and Analog/Mixed-signal Technologies for Wireless Communications* chapter. In the past, the traditional method of realizing passive circuit elements (for example, capacitors, resistors) on ICs was integration during front end processing. In this case doped monocrystalline Si substrates, polycrystalline Si and Si-oxides or Si-oxynitrides are used. Because of their proximity to the Si substrate, those passive devices fabricated during front end processing suffer increased performance degradation especially when used at high frequencies. Therefore, there is an increasing demand for low loss, low parasitics, but high quality passive devices in the interconnect levels.

For interconnect integration the key challenge is to achieve this goal in a modular and cost-effective way, without sacrificing overall interconnect performance and reliability. Currently two fundamentally different approaches are pursued for on-chip integration. One is the introduction of optional or additional interconnect levels in combination with new materials to accomplish the necessary functions and attributes with the highest Q-factors and a minimum usage of additional chip area. In general, this approach has the disadvantage of higher process complexity and potentially higher manufacturing cost. The alternative is simply to use native or "parasitic" properties, *e.g.,* capacitance, inductance, and resistance, of existing interconnect levels. This second approach is the least demanding for wafer manufacturing, but suffers typically from reduced Q-factors of passive devices and a larger chip area consumption. Another approach makes use of the post-passivation redistribution layers of the wafer-level package or integrates the passive devices directly into the package.

## MIM CAPACITORS

High quality MIM capacitors are seeing increased use in CMOS, BICMOS and bipolar chips. Typical applications are filter and analog capacitors (for example, in A/D or D/A converters), RF coupling, and RF bypass capacitors in RF oscillators, resonator circuits, and matching networks. Key attributes of MIM capacitors are high linearity over broad voltage ranges (low voltage coefficients), low series resistance, good matching properties, small temperature coefficients of capacitance, low leakage currents, high breakdown voltage, and sufficient dielectric reliability.

The economic demand for small chip area consumption leads directly to the request for higher MIM charge storage densities. Above a capacitance density of 1.5–2 $fF/\mu m^2$ a further thinning of the traditionally used Si-oxide or Si-nitride dielectrics is no longer useful because of increased leakage currents and reduced dielectric reliability. Therefore new high-κ dielectric materials, such as $Al_2O_3$, $Ta_2O_5$, $HfO_2$, $Nb_2O_5$, TiTaO, BST, STO, etc. or laminated layer stacks of different materials are being evaluated as MIM dielectrics and may be used in future applications.

As always, the introduction of new materials leads to new challenges in material processing (such as advanced PVD, CVD, or ALD deposition methods), process integration, and reliability. High quality films with excellent thickness uniformity, low defect densities and high dielectric constants need to be deposited below 450°C to be compatible with the overall interconnect architecture. To reduce parasitic substrate coupling and allow for high quality factors of the MIM capacitors, integration into upper metallization levels is preferred.

Low resistive capacitor electrodes and perfectly engineered electrode-dielectric interfaces are necessary to achieve high MIM quality factors and the required reliability targets. Some promising integrations of high κ materials in MIM capacitors have been demonstrated in the literature. However, improvements are still necessary in order to come to cost-effective and manufacturable solutions with a minimum of additional process steps.

## INDUCTORS

High quality on-chip inductors are critical components in analog/mixed signal and high frequency (RF) applications. Currently they are widely used in RF circuits especially for impedance matching, RF filters, RF transceivers, voltage controlled oscillators (VCO), power amplifiers and low noise amplifiers (LNA). Key attributes are high quality factors, Q, at high inductance, high self-resonance frequency, low Ohmic losses, low eddy currents, and low capacitive substrate losses.

Today, spiral inductors in the upper thick Al- or Cu-metallization levels are most widely used in order to fabricate low resistive coils with sufficient spacing from the Si-substrate to achieve optimized quality factors. These simple spiral



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inductors can be fabricated relatively easily using standard interconnect processes. But they may not in every case be good enough to fulfill all future RF requirements. Therefore, some more advanced constructions and approaches are being pursued.

Examples such as shunted coils, realized in several metallization levels, the use of metallic or even magnetic ground planes, suspended spiral inductors in air-gaps, post passivation add-on modules with coils in fat redistribution metal layers (several µm metal thickness) or solenoidal inductors with and without ferro-magnetic core fillings have been successfully demonstrated. Other possibilities for reducing substrate losses are the use of high Ohmic Si substrates, SOI substrates or localized semi-insulating Si-substrate areas after ion- or proton- bombardment.

However, not all of these alternative fabrication schemes are suitable for manufacturing, because of integration and process complexity issues or incompatibilities with device or product requirements. These approaches are an expression of the constant struggle for improved performance with higher inductance at higher frequencies or improvements in quality factor by reducing the Ohmic losses in the coil and/or the parasitic substrate.

### RESISTORS

Precision thin film resistors are widely used in analog and mixed signal circuits and specific SOC applications. Key attributes are precise resistance control, excellent matching properties, high voltage linearity, low temperature coefficients, low 1/f noise, and low parasitics resulting in high Q values. Today the most widely used Si-substrate-, polysilicon, or silicide- resistors fabricated during front end processing suffer mainly from poor 1/f noise performance and substrate losses.

Thin film resistors in the metallization levels can significantly improve the 1/f noise performance and other substrate losses. Key challenges for resistors in the interconnect are finding materials with moderate and tunable sheet resistance compatible with the standard interconnect materials and integration schemes, excellent thickness control and good etch selectivity to dielectrics with a modular integration scheme. Especially for Cu-metallization schemes, TaN has been found to be a promising candidate; however, other materials may see use in the near future.

More details on the applications, typical requirements, the processing and integration challenges of the different passive devices (MIM capacitors, inductors and resistors), including a list of recent references, can be found in this link.

## RELIABILITY

### INTRODUCTION

Rapid changes are occurring in interconnect materials and structures resulting in significant new reliability challenges. Understanding failure mechanisms in Al and $SiO_2$ technology grew incrementally over some 35 years. In the last ten years the industry has moved to copper, and is now also attempting to install a series of new and/or significantly modified low-κ interlayer dielectric materials. All of these changes are expected to occur with no reduction in the reliability afforded from the previous mature materials sets. Failures are further exacerbated by continued increases in interconnect density, number of layers, and power consumption. This section presents a short description of the reliability concerns that have been identified with Cu/low-κ metallization.

Copper was adopted partly due to the expectation that it would have higher reliability than aluminum. Under equivalent circumstances that could be true. However, the industry has continued to reduce feature sizes and increase line current densities, as well as the overall number of metal lines on the die to the point that maintaining reliability of copper is just as challenging as it was for aluminum. Metal reliability of copper is strongly dependent on the properties of the surrounding barrier and seed layers as well as the surrounding dielectric. Reliability of Cu/low-κ interconnects must be viewed as reliability of a system, which is now known to have three high level differences from its predecessors:

1. The physics of metal migration are somewhat different than for aluminum
2. In low-κ dielectrics the metal is more likely to be in tension rather than compression
3. As the 'κ' of the dielectric is reduced, so is mechanical strength

### CU METALLIZATION

Electromigration failures are generally described with Black's equation [1], which determines the maximum current density ($J_{EM}$) that can flow safely in a copper wire during its targeted lifetime. However, since the current density scales inversely with the cross-section of the interconnect wire, the safety margin to prevent electromigration failures decreases with each technology generation. The net result of this decreased cross section and changes in current throughout the


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roadmap years is shown by the $J_{max}$ metric in Table INTC2 a and b. The coloring scheme depicts when technology improvements must be implemented to meet electromigration failure rate requirements.

In an interconnect portion subjected to an electrical current, the Cu atomic drift velocity is determined with an effective diffusion coefficient. The effective Cu diffusion coefficient takes into account the possible atomic diffusion paths existing in a metal [2]. Experimental and theoretical results [3] have shown that the drift velocity remained almost constant for a large variety of Cu interconnect fabrication processes. This is consistent with a similar diffusion path (*i.e.,* interface diffusion) as the mechanism for the failures. Moreover the void geometry which also determined the interconnect lifetime was found to be in the Cu line for the strong electromigration failure mode (via voiding is shown as a weak failure mode and is expected to vanish with via process improvement [4]). As a consequence, the interconnect lifetime and the allowed current density scale versus the Cu line cross-section = w*h where w and h are respectively the Cu line width and thickness). To maintain the $J_{EM}$ specification for future technology generations, the Cu diffusion path needs to be changed. Moving from interface diffusion to grain boundary diffusion is not expected to provide significant improvement in $J_{EM}$ because similar drift velocity has been reported [5]. In conclusion, process improvement should be oriented towards the suppression of surface diffusion and/or grain boundary diffusion to reach a bulk-like diffusion value. Research has shown that much lower drift velocity was obtained when a CoWP [3] metal cap was employed or when alloys of Cu such as Cu-Al [6] are used in Cu interconnect.

From the early studies of electromigration, it has been shown that short lengths of interconnect (also called the Blech length) $L_B$ could be immortal [7]. The condition of immortality is reached for any current density or wire length below the critical product of $J_{EM}$ * $L_B$. This critical product is a consequence of the mechanical confinement of the metal in the interconnect structure [8] Moreover, the role of the Young modulus of the dielectric surrounding the metal and the energy of adhesion between the metal and its top interface have been highlighted [9] showing indications of the process improvements needed to maximize the immortality condition. Experimental research indicates that the critical product of $J_{EM}$ * $L_B$ ranges between 1500 and 5000 A/cm.

## ULTRA LOW-K MATERIALS

The industry transition to low-κ (defined roughly as those having bulk $\kappa \leq 3.0$) materials has taken longer than any prior roadmap has forecasted. This transition has been paced first by the ability to assemble structures using materials that are inherently less mechanically and chemically robust, and then by the reliability of those structures in their end product use.

Silicas, with backbone modifications that include carbon (SiOC), are the material family of choice. There are however, still some manufacturers using organic polymers in certain applications. The dense forms of these materials will afford bulk κ-values reaching as low as ~2.5. To go lower in κ, porosity is added. In comparison to $SiO_2$, all of the low-κ candidates present common reliability challenges:

- All have thermal expansion coefficients that in general place the metallization in tension resulting in "via popping" failures that may not appear until after packaging and test. The more carbon in the material backbone the higher the expansion coefficient and more stress applied to the metals.
- All have lower mechanical and yield strength offering less capability to maintain the structure under the strains induced in processing, packaging, and field use. Cracking and delamination failures in bonding are the current challenges for the industry. Finally the lower κ materials are less resistant to metal extrusion forces that arise from either stress or electromigration.

## ULTRA LOW-K (POROUS LOW-K)

The inclusion of porosity into dielectric films exacerbates most of the above effects. Films become mechanically weaker, which reduces the constraints that the dielectric applies against thermal stresses, external mechanical forces, or metal extrusion. To achieve benefits from the ultra low-κ materials, dielectric assist layers such as hardmasks, CMP and etch stops, and diffusion barriers must either be eliminated and/or lowered in κ-value which reduces their integrity as well.

Process gases and chemicals are absorbed into the bulk of the porous films. Here again, as in the case of damage, the industry is striving to eliminate them for fabrication reasons or to achieve lower κ, but the reliability impact of any residuals in the layers is largely unknown

The physical mechanisms responsible for dielectric breakdown in porous low-κ dielectrics are not well understood. Failure is generally attributed more to the integration scheme than to the intrinsic material properties of the dielectrics. Contributing factors include the thickness and composition of the diffusion barrier and assist layers (hardmasks, CMP/etch stops) and the quality of the interfaces. Reliability also depends on the integrity of edge seals and passivation during and after assembly and packaging operations in order to prevent oxygen from moving through the porous material.



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### CU/LOW-Ḳ MATERIALS AND PROCESSES

The work devoted to low-κ materials research indicates that the challenges outlined above cannot be met by developing a revolutionary new low-κ material that is orders of magnitude more robust than its predecessors. Modifications to all of the unit processes and their integration must prevent or ameliorate low-κ damage. Dry stripping alone usually is insufficient to remove residues and particles from structures with high aspect ratios without attacking the low-κ dielectrics or copper and its barriers, so an additional wet process is usually required. No single set of strip tools, chemistries, and combinations will work for all low-κ's and all low-κ and assist layer combinations.

Lower levels of damage have been observed resulting from CMP and pre-metallization sputter etch. The industry will work to ameliorate this damage to reduce κ, but the detailed reliability implications of any combination of processes and materials will need to be understood. All of these unit processes bring their own specific yield loss mechanisms as well as susceptibility to longer-term reliability problems.

### MODELING AND SIMULATION

Cost-effective first pass design success requires computer-aided design (CAD) tools that incorporate contextual reliability considerations in the design of new products and technologies. It is essential that advances in failure mechanism understanding and modeling, which result from the use of improved modeling and test methodologies, be used to provide input data for these new CAD tools. With these data and smart reliability CAD tools, the impact on product reliability of design selections can be evaluated. New CAD tools need to be developed that can calculate degradation in electrical performance of the circuit over time. The inputs used would be the predicted resistance increases in interconnect wires and vias in the circuit based on the following:

- Wire length
- Current densities expected for the currents required by the circuit
- Calculated local operating temperature, which includes the effects of Joule heating in the circuit and elsewhere

These tools must become an integral part of the circuit designer's tool set to help predict product reliability before processing begins and to develop solutions that anticipate technology and thereby accelerate their introduction.

### FUTURE RELIABILITY DIRECTIONS

The sections above discuss only reliability concerns that have been identified thus far for the Cu/low-κ system. Continuing research is needed to understand the multi-variable nature of copper and low-κ interconnect reliability and provide accurate models for designed-in reliability. Many of the problems that result in Cu reliability issues will be more severe as feature sizes scale, as surface area to volume ratio of the metallization increases; as geometries scale to feature sizes where electron surface scattering effects become a significant contributor to resistivity, and as current densities rise. The fundamental reliability limits of copper/low-κ metallization must be identified to assess technology extendibility in these ranges, and to identify any unique failure modes that may arise.

It is expected that one or more alternate interconnect approaches such as package- intermediated interconnect, 3D IC or optical will begin to be used within the next five years. It appears that carbon nanotube approaches are even further into the future. Although it is too early to know the full integration scheme for these approaches, and also too early for complete reliability investigations, it is critical for the research community to use reliability requirements as one of the key considerations in alternate interconnect process and design selection.

## SYSTEMS AND PERFORMANCE ISSUES

### INTERCONNECT PERFORMANCE

The adequacy of near-term interconnect technology (copper wires and low-κ dielectrics) to continue meeting the performance requirements for ICs fabricated for succeeding technology generations varies with the intended function of the interconnect net and the technology used to fabricate the Cu wires. As requirements increase, it is increasingly necessary that interconnect be considered as part of a system that includes the package and the silicon chip to satisfy the total technology need for the IC.

The increasing RC delay is one of the most crucial parameters especially for high performance products. While scaled wires in the local and intermediate wiring levels are less critical and show only a moderate increase in RC, the fixed length interconnects in the semiglobal and global wiring levels are much more sensitive and need the introduction of repeating inverters to keep the RC delay within viable limits. However, the introduction of these repeaters requires additional chip area and increases the power consumption. In some designs this increased RC delay can be handled by


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modifications such as modular architectures to reduce the need for fixed length lines. One recent approach in this direction is the dual- or multi-core architecture in state-of-the-art microprocessors. Parallel data processing in the multi-cores allows comparable or even higher processor performance at lower core frequencies and reduced power consumption as compared to a single core high performance processor. However, such significant modifications to circuit architecture suffer from the disadvantages of needing new design tools and new software and are not generally applicable to all designs.

While RC delay is a major factor for many digital applications, capacitive coupling in the local and intermediate levels is a highly sensitive issue for low power applications. Crosstalk and noise associated with decreasing geometries and increasing currents are becoming a larger problem for both digital and analog circuits. These trends are a strong function of design strategy, and should be considered in that context.

In addition to the problems with scaled wires for clock and signaling, an equally difficult problem for interconnect is circuit power distribution. Increasing supply current, related to the decreasing $V_{dd}$, causes an increased voltage drop between the power supply and the bias point for fixed length wires. This problem cannot be solved as easily as the repeater solution for the fixed length clock and signal wires.

### SYSTEM LEVEL INTEGRATION NEEDS

The interconnect problems identified in the prior section, along with other increasing demands due to new applications, require a system-level integration viewpoint for interconnect that encompasses electrical performance as well as the physical and functional assembly of macro functions to achieve desired operating characteristics. Assembly of individual components (such as bare chip or block functions on a single chip) must encompass all the performance and reliability requirements imposed on the system. For interconnect, the requirements are currently met through the distinctly separate functions of on-chip interconnect, package, silicon chip, and board-level technologies. In the future, this viewpoint will not be adequate because it is now widely conceded that interconnect technology alone cannot solve the on-chip global interconnect problem with current design methodologies. Rather, the current view is that design, process technology, packaging, and board construction will all need to come together to provide an optimized integrated system-level solution for interconnect requirements.

The current projection for evolution of interconnects is that in the short term interconnect delay problems in new ICs will be met by circuit design within the constraints of planar technology with special attention to minimizing the lengths of critical paths. This will be done in concert with a substantial push in Cu/low-κ technology, as well as more innovative packaging, 3D-chip stacking and board approaches, to minimize the changes needed in design architectures while still meeting the continued advances in performance anticipated by the ITRS.

In the intermediate term, Cu/low-κ will be pushed to its limits, and new design architectures as well as chip-package co-design will be achieved with new CAD tools to facilitate needed performance advances significantly. Beyond these extrapolations of current practices, radically new design, packaging, and interconnect technology options will be needed. These new options will demand the total systems view of the IC, and will combine the package, the interconnect, and the silicon chip in the solution. A view of various options for combining the package, the interconnect, and the silicon chip into a complete solution is presented in the next section.

## NEW INTERCONNECT CONCEPTS AND RADICAL SOLUTIONS

### INTRODUCTION

*Overview:* The discussion of interconnect concepts beyond the conventional metal/dielectric system that has served the industry for the first four decades of its existence was brought about by the need for dramatically increased performance and lower power requirements for ICs, and the continued push to smaller geometries to satisfy Moore's law. The difficulties for interconnect technology resulting from technology scaling and material changes can be easily validated by observing that in the older 1.0 µm $Al/SiO_2$ technology generation the transistor delay was ~20 ps and the RC delay of a 1 mm line was ~ 1.0 ps, while in a projected 35 nm Cu/low-κ technology generation the transistor delay will be ~1.0 ps, and the RC delay of a 1 mm line will be ~250 ps. [1] In addition, at 0.13µm approximately 51% of microprocessor power was consumed by interconnect, with a projection that without changes in design philosophy, in the next five years up to 80% of microprocessor power will be consumed by interconnect [2]. This dramatic increase of the interconnect impact on performance and power shows clearly the challenges created by the scaling of the conventional metal/dielectric system. In the last few years IC manufacturers have recognized the difficulty of addressing interconnect performance limitations by technology means alone. In response, they have implemented design and architecture improvements to address interconnect limitations. Even with these advances, however, interconnect remains a critical bottleneck for many



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applications, which creates an ever increasing opportunity for developing and introducing alternative technology solutions beyond metal/dielectric interconnects.

*Functional Diversity:* Although this section of the interconnect roadmap was started to address interconnect delay/power issues associated primarily with on-chip global interconnects, it has become apparent that the alternate interconnect technology options being considered offer more far-reaching opportunities than this original intent. These additional opportunities include the use of alternate interconnects to reduce cost, to improve performance or utility, and other features of current IC applications. The use of 3D interconnects to reduce packaging cost and improve form factor is an example of this direction. These additional opportunities also include the use of the novel features of alternate interconnect solutions to address IC functional diversity. This direction includes examples such as the use of appropriately functionalized CNTs in an interconnect structure to serve as chemically selective resistors, forming an integrated interconnect-sensor array. Optical interconnects might also be used with multiple wavelengths in a single waveguide (wavelength-division multiplexing (WDM)) to provide not only higher bandwidth density for global interconnects, but also in combination with on-chip, voltage variable gratings to provide selective routing possibilities that can be used for radically different signal processing functions from those currently available. These exciting possibilities, and many others offered by alternate interconnects, provide significantly expanded product opportunities for the IC industry.

## INTERCONNECTS BEYOND THE METAL/DIELECTRIC SYSTEM

Multiple options have been proposed as alternatives to the metal/dielectric system to solve the delay/power problem. These alternatives have included possible replacements for the on-chip wiring, or parts thereof, as well as significant extensions of the conventional view of on-chip interconnect. These extensions have spread the solutions from the on-chip power/delay problem to the package and even into the design space. A list of the predominant possibilities is shown in Table INTC5. Although some of these approaches are relatively mature from a technology standpoint, it appears that in contrast to Al/$SiO_2$ or Cu/low-κ, there is not a single solution that will be used universally over all IC product types. The list in Table INTC5 is the Interconnect ITRS working group view of increasing complexity of implementation, based on the current status of these technologies. Since very few of these radical approaches are in prototype device development, and none are in volume production by major integrated device manufacturers (IDMs), there is not a formal roadmap for their associated technology parameters. Not all of these alternatives are expected to prove viable for production. Even if they are shown to be technically feasible, they may not be used for a number of reasons, both operational and economic. The appearance of a formal roadmap of specific parameters as a function of time will be evidence for a particular approach being selected for product implementation. Such roadmaps should appear at a time near the transition from "Narrowing Options" to "Implementation." The following sections describe some of these options in more detail, as well as describing issues that need to be addressed to increase the viability of the approach. Three of the options for Interconnects Beyond the Metal/Dielectric System listed in Table INTC5 are shown in bold letters. These three options have received the most recent attention as potentially viable replacements for parts of the metal/dielectric system or for functional diversity applications, and are described more fully than other options in the following sections. The beginnings of a roadmap are provided for 3D because it is anticipated to be used in high density interconnect manufacturing in the relatively near future, although the specific implementations and dates are still in the formative stages. (It should be noted that lower density 3D interconnects at the packaging level are in production, and are covered in the Assembly and Packaging sections of the 2007 Roadmap.)


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*Table INTC5 Options for Interconnects Beyond the Metal/Dielectric System*

| |
|---|
| *Use Different Signaling Methods* |
| – Signal design |
| – Signal coding techniques |
| *Use Innovative Design and Package Options* |
| – Interconnect-centric design |
| – Package intermediated interconnect |
| – Chip-package co-design |
| *Use Geometry* |
| **– 3D** |
| *Use Different Physics* |
| **– Optics (emitters, detectors, free space, waveguides)** |
| – RF/microwaves (transmitters, receivers, free space, waveguides) |
| – Terahertz photonics |
| *Radical Solutions* |
| **– Nanowires/nanotubes** |
| – Molecules |
| – Spin |
| – Quantum wave functions |

## DIFFERENT SIGNALING METHODS

This approach utilizes available technology with innovative approaches to signal format and circuit operation to produce current and voltage waveforms that are more compatible with high-speed global interconnects than the usual square wave approaches. Several options for this approach have been proposed; two are described below.

*Raised Cosine Signaling [1]*—Raised cosine signaling advocates assert that the noise crosstalk due to inductive and capacitive coupling effects will become increasingly important, and will eventually become the dominant problem over local and global propagation delays. This potential increase of crosstalk by various sources is due to 1) higher near-field coupling via capacitive, inductive and resistive links, a result of device scaling and close proximity of wires and metal layers; 2) increased coupling between distant parts via substrate and power rails; 3) increased noise coupling from intrinsic device noise such as flicker, thermal, and shot noise, and 4) high frequency radiation effects due to interconnect discontinuities. Aggressive clock distribution designs require the amount of skew and jitter for a clock signal to be less than 3–4% of the clock period. As an example, in the ITRS roadmap, the on-chip local clock is targeted for 10 GHz and global clock rates are approaching 3 GHz. This implies that the jitter/skew must be controlled to within 4 ps and 13 ps, respectively. The raised cosine technique addresses the noise crosstalk problem by using raised cosine pulses instead of square pulses as the basis functions of high-speed buses, as well as high efficiency current-mode drivers to minimize both power consumption and noise crosstalk. This approach has been shown to reduce the crosstalk noise in specific technology applications by as much as 40%.

*Resonant Clocking* [2]—In the resonant clock approach, traditional tree-driven grids are combined with on-chip inductors to "resonate" the clock capacitance at the fundamental frequency of the clock node. The energy of the fundamental will "slosh" back and forth between electric and magnetic forms and not be dissipated as heat. The clock drivers only need to provide the energy at the fundamental necessary to overcome losses and inject the higher frequencies required to provide sharper (not sinusoidal) clock edges. Power and clock latency are also improved because the effective capacitance of the grid is lower and fewer pre-driver stages are necessary to drive the grid. Power reduction of almost 40% in the global clock distribution network is projected to be possible, depending on the Q of the resonant system. However, since the global clock distribution power is a fraction of the total power, the net power savings may not be significant. Potential skew and jitter reductions come about because of the reduced buffer latency and the bandpass characteristics of the resonant network.

*CRITICAL CHALLENGES*

- Manufacturing issues such as testing, cost, Si area consumed, etc.
- Extending the limited scalability of these approaches
- Providing high Q on-chip components for resonant circuits



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- Increasing design flexibility: clock is delivered to a few, pre-determined points arranged on a regular grid
- Extending the range of frequencies over which this technique is operable
- Reducing the consumption of interconnect area using these techniques

## INNOVATIVE DESIGN AND PACKAGE OPTIONS

Among the most effective short term solutions to the difficulties in IC manufacturing posed by increasing frequency and increasing power have been approaches that leverage areas of technology other than materials and processing. These other areas are predominantly design and packaging. The promise of this approach, already fulfilled in recent technology generations, is to forestall the requirement for very low-κ dielectrics or more radical approaches to global interconnect. The liability of this approach is that few design tools are available to do the multi-scale, multi-phenomenon, modeling and simulation necessary for design optimization when radical circuit architectures and packaging structures are combined. A few of the options in this approach are described below.

*Interconnect-centric Design [1]*—A procedure that has already been used for critical path design for several technology generations is interconnect-centric design. In this approach, interconnect design—including interconnect planning, interconnect synthesis, and interconnect layout—are optimized (often at the expense of other circuit features) at every level of the design process. This approach has the distinct advantage of using current technology to optimize performance in the design areas where interconnect is a bottleneck. It suffers from two specific disadvantages. First, appropriate interconnect design tools and design models are not available to implement this approach over all designs, so much of this work becomes custom. Second, to carry this approach to its fullest benefit often requires a major revision of standard design and layout practices, which are inconsistent with the advantages offered by scaling and technology changes that have been used in the past to follow Moore's law.

*Package Intermediated Interconnect [2]*—an option for reducing the global interconnect problem is to move some of the interconnects from the primary chip to thicker metallization and higher performance levels on the package. This approach is labeled "Package Intermediated Interconnect." The signals would then be transferred back to the primary chip at an appropriate point. This approach would greatly benefit from improvements in the input/output (I/O) capabilities of microprocessors. For example, a "Sea of Leads" approach might be used to provide the needed density increases in I/O to benefit not only global interconnect, but at the same time, power and ground connections. The basic components of most of the package intermediated approaches have been demonstrated at the laboratory level. Additional research in areas such as power requirements, manufacturing issues, and cost is needed. Creative development is also needed to provide implementations of this approach that will circumvent the inherent cost and reliability limitations introduced by added elements and connections. Among the serious challenges for this concept are the following:

- Cost and complexity: a revolutionary change to packaging may be required to make this cost effective.
- Significant increases in the quality and uniformity of package-related dielectrics, with no increase in cost.
- Clear understanding of design trade-offs—the power needed to switch such large interconnects could be larger than that of equivalent on-die wires.
- The pitches of current package interconnect needs to be reduced significantly to eliminate possible severe routing issues and limited bandwidth.

*Chip Package Co-Design [3]*—Chip package co-design is the unification of models and design tools that allows global optimization and characterization of the IC/package system under development. In the optimum case this design approach would allow combined electrical, thermal, and mechanical simulation and optimization. In this approach the design trade-off complexities between various parts of the design would be captured, distributed, and managed using a co-design model. This approach needs to encompass the chip, the package, and the board (if it provides a significant interaction).

*CRITICAL CHALLENGES*

- Availability of design tools to do the multi-scale, multi-phenomenon, modeling and simulation necessary for design optimization for radical circuit architectures, or for combined circuits and packaging structures
- Cost and reliability of additional interconnects between chip and package
- Cost of supplemental chip (if used)
- Design issues associated with division of interconnects between chip and package
- Probing and testing of total structure


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## 3D ICs

A simple yet elegant way to reduce the burden of high frequency signal propagation across monolithic ICs is to reduce the line length needed by employing stacking of active devices using 3D interconnects. Such 3D interconnects have been proposed to supplement or replace on-die interconnects for both performance and density reasons. This section discusses the current status of 3D as a replacement for long lines in the on-chip global interconnect. It also discusses other alternative applications offered by 3D integration. The following discussion of 3D interconnects is self-contained. The references are numbered in the section text and listed at the end of the chapter.

### *INTRODUCTION*

For interconnect, the primary interest in 3D is to circumvent the delay and power limitations of on-chip 2D interconnects that restrict the continued ability of the IC industry to follow Moore's law. A second interconnect interest in 3D is to exploit the significant advantages allowed by 3D, and combinations of 3D with other "Interconnects Beyond Cu/low-κ" options, to provide functionally diverse solutions to critical consumer needs. This second interest of the IC companies thus drives the Interconnect Roadmap to include 3D interconnects between die with incompatible process flows, and between die connected by novel interconnects such as RF, nanowires, or nanotubes. Given these specific interests, the Interconnect roadmap addresses 3D implementations with die-to-die interconnect densities significantly beyond those associated with bond pads on the IC. The "Interconnects Beyond Cu/low-κ" applications considered will require 3D connectivity at the function level and below, with the possibility of connections down to the transistor level being considered. The processes and structures required for these high-density 3D interconnects differentiates the challenges of the 3D Interconnect roadmap from those of the Assembly and Packaging (A&P) roadmap. Because of the distinct difference between the Interconnect and A&P densities for chip-to-chip connections being considered at present, the Interconnect chapter designates the high density through silicon vias as HDTSVs.

### *PERFORMANCE ADVANTAGES*

The primary advantage of 3D interconnect that replaces on-die interconnect is reduced delay and reduced power. While the potential delay and power advantages will depend on the details of a specific 3D implementation, it is generally true that for long lines typical of global interconnect, power and delay of interconnects including optimized repeaters depends linearly on line length. Calculations [1] show reductions in global interconnect length of as much as 50% using 3D, corresponding to a 4× increase in clock frequency and a 2× reduction in interconnect power dissipation. An added advantage of the 3D architecture is a reduction in die area of almost 50%. Although these calculations are based on a simple model, and there are many factors that could reduce these advantages in practice, it is clear that major improvements are likely possible using 3D interconnects. A second major performance advantage of 3D interconnect is the flexibility that it allows in communication between circuit functions. This is aptly illustrated by the case of memory-intensive processor operations [2]. A 3DIC solution allows positioning the memory closer to the processor, and by shortening the wires, an additional power savings can potentially be realized. The 3D integration method chosen for this application will require high-density die-to-die connections. These tight geometry die-to-die connections are part of the device interconnect structure, and as such, are thus described in the Interconnect chapter of the ITRS.

### *3D INTEGRATION OPTIONS*

Industry activity around 3D is rapidly gaining momentum. Many different 3D approaches are being considered, including wafer-to-wafer bonding, die-to-wafer processing, and the more traditional die-to-die SiP approaches. A variety of bond layer methodologies are also being considered, including direct metal fusion bonding [3–5], adhesive polymer bonding [6], and dielectric fusion bonding [7, 8]. Wafers or die can be bonded face up or face down. There are advantages and disadvantages inherent in each process flow, and the choice of process flow will likely be product-dependent. It is thus important to start to define the roadmap for 3D integration, and to understand the risks, costs, and challenges of the various process options.

### *WAFER-TO-WAFER PROCESS FLOW*

A wafer-to-wafer 3D flow bonds one wafer on top of another. This has the advantage of utilizing wafer-level batch-type processing. In this case processing costs can potentially be lowered for high volume, high yield products. Potential disadvantages of this approach include the critical alignment accuracy required across a wafer, caused by temperature non-uniformity from a thermal expansion mismatch across the wafers in the bonded pair. Yield of the stacked pair is degraded when good die on the bottom tier are bonded to "bad" die on the top tier, or vice-versa. Other critical process details exist, such as control of the wafer bow and stress of the bonded wafer pair, the requirement that die sizes match on each of the bonded wafers, and elimination of particles at the interface between bonded wafers.

### *DIE-TO-WAFER PROCESS FLOW*



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Die-to-wafer 3D processes have a potential yield advantage compared to wafer-to-wafer processes, due to the ability to pre-select "known good die" (KGD) for bonding. Die-to-wafer process flows are particularly attractive for lower yielding or lower volume codes, and when only two active layers are needed. In large volumes, the cost of the die-to-wafer assembly will be strongly affected by the align and bond step. Current technology uses a "pick-and-place" tool to align the die. Depending on the bond type chosen, the process may need heat and/or pressure to form a strong bond layer, thus a key challenge for die-to-wafer processing is understanding the trade-offs between alignment accuracy, bond formation, and throughput. Die-to-wafer process flows become much more challenging when stacking more than two active layers together.

### *Face-Up versus Face-Down Wafer Bonding*

Another key process decision for 3D is whether the donor die or wafer will be bonded face up, (face-to-back, F2B) or face down (face-to-face, F2F) [9]. The advantage of F2F bonding is that it can potentially provide the greatest die-to-die interconnect density, with the pad or via size and pitch limited only by the alignment accuracy. In addition, face-to-face bonding allows the back of the bonded top wafer to be thinned without the process complications of handle wafers [10]. A major disadvantage of F2F bonding is that it is limited to two device layers or strata, and additional processing must be performed on the bonded stacked pair to provide I/O connection. Face-to-back (F2B) bonding will be required when stacking more than two device layers. One potential advantage of F2B bonding is that the I/O connections are available through the top layer of the existing donor wafer. Achievable die-to-die via density is reduced, however, and the via must also be etched through the active device layer of the donor die.

### *High Density Through-Silicon Via Formation Options*

High density through-silicon vias used to electrically connect the wafers may be formed before or after the wafers are bonded. If the vias are formed after the wafers have been bonded together (via last), a sufficient exclusion area must be set aside in the design to accommodate the HDTSVs. The HDTSV etch can also be challenging, as several different dielectric materials (with different etch rates and chemistries) are typically used in modern ICs. Barrier dielectric deposition and metallization also present challenges, given the high aspect ratios and metal volumes involved. A potential advantage to post-bond HDTSV formation is that a variety of bond layer materials such as benzocyclobutene (BCB) [10] can be considered.

If the vias are formed before wafer bonding (via first), using existing steps in the process flow can potentially reduce cost. Additional steps must be added after wafer bonding to provide electrical contact to the vias. One option involves attaching the wafer with the filled via to a handle wafer and thinning the backside to expose the buried via. If the wafers have been F2F bonded and the bond strength is sufficient, a handle wafer is not required for wafer thinning.

The design and processing of HDTSVs is a key enabling technology for both assembly and packaging options as well as high performance interconnect 3D integration technologies. Several companies are now beginning to produce high density vias, and some users are making projections of capabilities that will be needed in the future. A draft roadmap for high density HDTSVs needed for interconnect applications is shown in Table INTC6. Note that this draft roadmap contains values representative of current development status, and projections for development in the future. The 2007 values are representative of values available in current prototype devices, and are anticipated to be available in production quantities soon. When such production happens, this table will be included with the primary tables of this chapter or the A&P chapter, as appropriate.

A range of via diameters and pitches is shown in the table. In addition, a separate category for a high-density face-to-face bonded structure is included. Aggressive thinning targets are also included, as the overall dimensions of the HDTSV will depend on a combination of etch depth, thinning capability, and fill capability. It should be noted that HDTSVs of these dimensions are not in high volume production today, though they have been demonstrated, and are expected to ramp into high volume. Figure INTC12 [11] includes both a face-to-face bonded structure as well as a small diameter via-first contact in the upper right corner.


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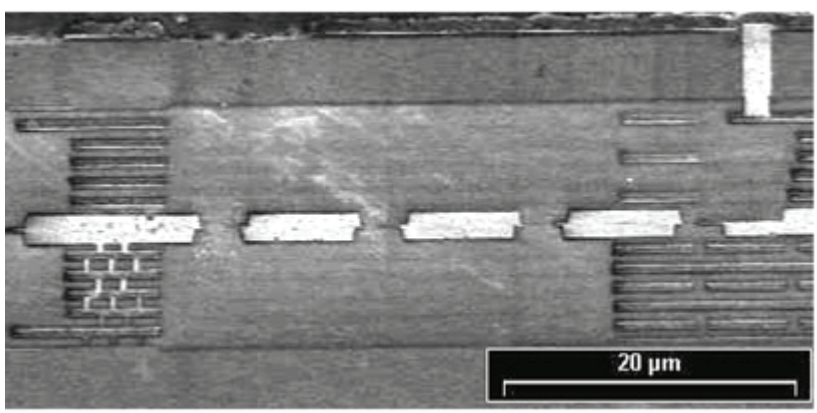
*Table INTC6 High Density Through Silicon via Draft Specification*

| *Year of Production* | *2007* | *2008* | *2009* | *2010* | *2011* | *2012* | *2013* | *2014* | *2015* |
|---|---|---|---|---|---|---|---|---|---|
| *DRAM ½ Pitch (nm) (contacted)* | *65* | *57* | *50* | *45* | *40* | *36* | *32* | *28* | *25* |
| *MPU/ASIC Metal 1 ½ Pitch (nm)(contacted)* | *68* | *59* | *52* | *45* | *40* | *36* | *32* | *28* | *25* |
| *MPU Physical Gate Length (nm)* | *25* | *22* | *20* | *18* | *16* | *14* | *13* | *11* | *10* |
| *Minimum Interlayer HDTSV Contact Pitch (µm)* | | | | | | | | | |
| High Density | **3.2–5.0** | **2.9–4.4** | **2.6–3.8** | **2.2–3.4** | **2.0–3.0** | **1.6–2.6** | **1.4–2.2** | **1.3–2.0** | **1.0–1.7** |
| | | | | | | | | | |
| *HDTSV Diameter (µm)* | | | | | | | | | |
| High Density | **1.6–2.5** | **1.4–2.2** | **1.3–1.9** | **1.1–1.7** | **1.0–1.5** | **0.8–1.3** | **0.7–1.1** | **0.6–1.0** | **0.5–0.9** |
| | | | | | | | | | |
| *Maximum Via Density ($cm^2$)* | | | | | | | | | |
| High Density | **9.77E+0.6** | **1.21E+07** | **1.53E+07** | **1.99E+07** | **2.31E+07** | **3.91E+00** | **4.82E+07** | **6.10E+07** | **9.61E+07** |
| | | | | | | | | | |
| *Minimum Face-to-Face Pitch (µm)* | | | | | | | | | |
| High Density | **5.00** | **4.38** | **3.83** | **3.35** | **2.93** | **2.56** | **2.24** | **1.96** | **1.72** |
| | | | | | | | | | |
| *Maximum Layer Thickness (µm)* | | | | | | | | | |
| High Density | **7–25** | **7–25** | **7–25** | **6–20** | **6–20** | **6–20** | **5–15** | **5–15** | **5–15** |
| *Total Thickness Variation (µm)* | **<1** | | | **<0.75** | | | **<0.5** | | |




*SEM Courtesy Of Tezzaron [11]*

*Figure INTC12 Two Wafers Stacked and Bonded Face-to-Face with a High Density Via Contact*

## CHALLENGES

### WAFER THINNING

Wafers can be thinned using a combination of bulk silicon grinding, CMP, dry polishing, wet chemical etching, or plasma etching. A typical process uses a combination of steps. Control of the final thickness and total thickness variation (TTV) across the wafer is critical for subsequent processes. Handling of the thinned wafer becomes a critical issue below about 100 µm for a 300 mm wafer (75 µm for 200 mm). Thinner wafers may require a temporary handle wafer to use existing chucks, cassettes, and transfer arms. A special front opening unified pod (FOUP) design may be needed to handle the double thickness wafer stack before thinning.

### HDTSV FORMATION

HDTSV etch is one of the most critical enabling steps for 3D interconnect integration. The challenge is to provide a viable HDTSV etch that has high etch rates, smooth sidewalls, controllable sidewall angle, and minimal mask undercut.



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In addition, a viable HDTSV etch will meet the cost and throughput constraints associated with high volume, competitively sold products.

HDTSVs are typically formed by plasma etch, but can also be formed using focused beam YAG lasers [11–13]. HDTSVs with diameters ranging from 25–150 µm and depths from 50–150 µm have been successfully demonstrated using this technique. A key benefit to this process is that it eliminates the need for the lithography step to define the via dimensions and replaces the etch with laser drilling. The challenge is to eliminate the debris or splatter resulting from the laser ablation. The ability to shrink the via diameter may also be limited in this approach. Cost of the process is also challenging, since laser drilling is a serial process. Unless creative solutions to these challenges are found, laser processing may be limited to products with a fairly low density of HDTSVs.

#### *Bond Layers*

Several different bond layers are currently being investigated for 3D, each with its own unique advantages and challenges. Typical 3D bonded materials include metal-to-metal bonds, such as copper-to-copper or copper-tin eutectic alloys, low temperature dielectric fusion bonds, adhesive layer bonds using a polymer material such as BCB, and finally temporary bond layers for use with a handle wafer. The generic challenges that each of these bonding methods must meet are to provide a strong, stable, etchable bond material that can withstand any further processing required, as well as providing a high reliability interface for final device applications.

#### *Alignment*

The ability to align the donor die or wafer to the substrate wafer determines the allowable density of vias and the manner in which the 3D technology may be used. Providing adequate alignment may be the most challenging requirement to achieve the interconnect density necessary for 3D technology to replace on-die interconnects. The achievable face-to-face pitch will be limited by the ability to align accurately at a cost-effective throughput. The pitch limits noted in Table INTC6 are driven by the need to improve alignment accuracy. Typical alignment capability is better for wafer-to-wafer than for die-to-die because of the time one can afford to allocate to the alignment. However, differential thermal expansion of the wafers can contribute to misalignment, and must be tightly controlled. Alignment can be performed by looking through the top wafer using infrared light to find the lower wafer's alignment keys. It can also be done *ex situ*, by registering the two wafers to their respective chucks, then moving them into place without further alignment. Some processes may create alignment keys earlier in the process that are subsequently exposed prior to the alignment sequence.

Die-to-wafer alignment is generally done in modified flip-chip align-bond equipment. Manual, high-precision alignment is possible, but is time consuming. The high rate pick-and-place required for good wafer level throughput may degrade the alignment from the best possible that is attained with "active" alignment. At the highest throughput rates, only passive alignment can be done.

#### *Other Challenges*

There are several additional challenges that must be addressed for 3D integration methods to be readily made in volume. These include, but are not limited to, the following:

- Models of manufacturing costs and yields of 3D integration methods that allow intelligent selection of the appropriate 3D process for specific product applications
- Thermal modeling and routing placement for heat removal
- Probing and test for a stacked structure
- Reliability of the 3D stacks
- Limited standardization of 3D processes
- CAD tools for optimal 3D system design

## Different Physics for Signal Propagation

Options for continued progress of interconnect performance significantly beyond that provided by the options described above will require employing approaches that introduce materials and structures beyond the conventional metal/dielectric system, and may require information carriers other than charge. Three examples of approaches being considered are included below.

## CMOS-compatible Optical Interconnects

Optical interconnects have been used in the long-line communications industry for many years. Reducing this capability to IC geometries, and making it compatible with CMOS technology, presents new and exciting challenges. The following


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discussion of CMOS compatible interconnects is self-contained. The references are numbered in the section text and listed at the end of the chapter.

### INTRODUCTION

Optical solutions have been proposed for on-die interconnects (signaling and clock distribution) and I/O. The driver for on-chip optical interconnects is the utilization of the speed-of-light signal propagation and the large bandwidth of waveguides. For I/O applications, optical solutions focus on increasing the aggregate bandwidth and/or distance while decreasing the power per bit, by overcoming the limitations imposed by losses in present package interconnects (metal and dielectric) and by avoiding or minimizing the need for high power equalization and pre-emphasis. Since I/O, signaling and clock distribution require similar optical components, research and production costs are shared.

Because of pitch constraints, as well as delay and power considerations, optical interconnects are not expected to fully replace the lower metal-dielectric interconnect layers in microprocessors. Instead, the focus is on cost efficient implementations that take advantage of the unique properties of optical architectures to increase overall system performance (*i.e.,* not on total Cu/low κ replacement). For such optical solutions to be viable, the development of CMOS-compatible optical components is of paramount importance. Although significant progress has been made, this area is not yet sufficiently mature to define an intersection to the existing interconnect roadmap.

### ADVANTAGES OF OPTICAL INTERCONNECTS

The basic advantages of optical interconnects are speed-of-light signal propagation and large bandwidth, as noted above. However, other potential advantages also exist. Among these are the minimum crosstalk between signal transmission paths, ability to be readily converted between transmission within a waveguide or free space, and multi-wavelength capability. The minimum crosstalk between signal paths, due to minimum interaction between photons and ability for light to propagate in waveguides or free space, provides significant design flexibility for optical circuits. The capability for a single optical path to accommodate multiple wavelengths increases the data carrying capacity manifold, providing bandwidth densities not achievable by electrical means.

### INTEGRATION OPTIONS

#### OPTICAL ARCHITECTURES FOR ON-DIE OPTICAL INTERCONNECTS:

Although a large number of optical architectures have been proposed, most of them fall into one of the following two categories:

1. *Integrated light source architectures*: In this case there are multiple on-die directly modulated light sources (*e.g.,* VCSELS) and on-die detectors. The main disadvantage is the large on-die power consumption/heat dissipation of the sources, and the significant challenges for integrating fast, efficient CMOS-compatible light sources.
2. *External light source architectures*: These are implementations that utilize one or a few off-die light sources on the package or the board, and on-die modulators and detectors. The main advantage of this family of architectures is that the laser power is off-die (*i.e.,* does not have to be delivered through the die). The main disadvantage is the coupling losses to bring the light into the chip.

In both cases above, wavelength-specific filters/modulators can be used to implement multiplexing, which enables multiple independent signals to be transmitted in each channel.

Expected advantages

- *Delay*: For the case of on-die signaling, it is possible to define a critical length above which optical interconnects are faster than their metal-dielectric counterpart. The critical length, which depends on the quality of the optical components, has been assessed to be on the order of millimeters [1].
- *Signal integrity*: Optical interconnects have the potential for simplifying design and layout constraints arising from undesirable crosstalk in metal-dielectric interconnects.
- *Skew and Jitter*: It has been proposed that the low latency and the absence of crosstalk in optical interconnects can potentially result in low skew and jitter clock distribution. However, advanced clock distribution designs implemented in conventional metal-dielectric systems are expected to meet microprocessor needs.

Potential disadvantages: Power, cost, complexity.

Potential usage in the interconnect hierarchy: Long interconnects in upper metal layers.

#### ARCHITECTURES FOR OPTICAL INPUT/OUTPUT

Most of the proposed implementations of optical I/O can be grouped into one of the following two architectures:



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- *Integrated I/O*: In this case, optical components are integrated into the digital logic chip. Part or all of the communications between the chip and the external world are done through optical signals.
- *Discrete I/O die*: These architectures use an optical I/O chip that receives electrical signals from the digital logic chip and transforms them into optical signals. Equivalently, the optical I/O chip receives optical signals that are transformed into electrical signals that are then provided to the digital logic chip.

The main advantage of integrated I/O is that it can potentially save power with respect to discrete I/O. On the other hand, discrete architectures remove some of the design and integration constraints that would be otherwise imposed if optical components were integrated on the microprocessor die.

Expected advantages: High aggregate bandwidth and low power per bit, potential for long-distance I/O, removal or minimization of need for pre-emphasis and equalization

Potential disadvantages: Cost, complexity

#### CHALLENGES

The primary challenges for optical interconnects at the present time are producing cost-effective, low-power components that are compatible with CMOS fabrication. Some of these components, and the associated challenges, are contained in the listing below.

#### COMPONENTS

On-chip implementation of optical interconnects for signaling, clock distribution and/or I/O require some or all of the following components:

- *Light sources*: From a modulation perspective, light sources can be *directly modulated* or *non-modulated*. In the first case, the light sources can be turned on/off with an electrical signal; in the latter case, the light source is used in conjunction with modulators that can be controlled with electrical signals. From a location perspective, lasers can be off-die (package or board) or on-die. Key parameters are output power, efficiency, cost, thermal stability, cooling requirements, and speed for directly modulated sources. Examples of light sources include VCSELS, quantum dot lasers, and edge emitting semiconductor diode lasers. The most widely used wavelengths are 850, 1310 and 1550 nm.
- *Photodetectors*: As in the case of lasers, photodetectors can be integrated either on-die or off-die. Metal-Semiconductor-Metal photodetectors have received significant attention since they have the potential for been CMOS compatible [2], and can be fabricated using Si, Ge and SiGe [3–6]. Key technical parameters include responsivity, operation voltage, input capacitance, ratio of photocurrent to dark current, ratio of photocurrent to input capacitance, light coupling efficiency, and dimensions. A key design parameter is the coupling of light into the photodetector. Recently, detectors that take advantage of plasmons to enhance the coupling of light into the photodetector have been proposed [7].
- *Modulators/filters*: Modulators and filters are used in combination with a non-modulated light source, typically located off-die. The main purpose of a modulator is the control of the flow of light into a particular waveguide with a standard digital signal. A frequency-dependent filter can be used to introduce multiplexing, which enables the transmission of multiple signals in a single waveguide. A large variety of CMOS compatible modulators have been proposed in the literature, including resonators and Mach Zehnders. The key performance parameters include coupling efficiency, operation voltage, switching time, waveguide loss, overall power, modulation depth/extinction ratio, and area.
- *Waveguides*: Waveguides provide the means for light propagation on the chip with minimum losses. They also need to enable implementation of "bends" and "turns," as well as an efficient coupling of the light into the detectors. A large refractive index contrast between the waveguide and the surrounding materials enables tight turn radii and small pitches, but at the expense of lower light speed, which decreases with the inverse of the effective refractive index. Reported on-die waveguides using materials already common in the industry include, for example, Si, $Si_3N_4$, or $Si_3O_xN_y$ cores on $SiO_2$ cladding [8]. Key technical parameters include loss per unit length, refractive index contrast, and pitch.
- *Couplers/splitters*: Couplers are used to bring light from an external source into the package and die. The key merit metrics are coupling efficiency, cost, and alignment requirements. Power losses in couplers can potentially dominate the optical budget in optical systems. Splitters are used to divide a light source (laser or single waveguide) into two or more waveguides. Power losses and size are the two most important quality metrics of splitters.

Significant progress has been made towards developing CMOS-compatible optical components, especially in the case of waveguides and detectors. However, additional progress is still necessary to develop modulators, light sources, and couplers to deliver the potential of optical interconnect fully.


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## RF/MICROWAVE INTERCONNECTS

A relatively radical alternative to the usual metal/dielectric interconnect is to use transmission of signals from one part of a chip to another via RF or microwaves [1], [2].This option essentially takes the form of a LAN on a chip, with transmitters, receivers, antennas and appropriate signal generation and signal detection circuitry. Transmission in this case has been proposed to be a "free-space transmission" through the package and IC structures. Another possibility is that the RF signal is capacitively coupled through a waveguide in the package lid. The transmission has been proposed as a sinusoidal signal or as a coded digital signal, depending on the specific system concept employed. Each option has its own particular advantages and disadvantages, as well as its own unique requirements. The basic concepts of this approach to global interconnects have been demonstrated.

### *CRITICAL CHALLENGES*

- Complete characterization of total system concept for cost and performance comparison with alternative solutions
- Full design rules for the electrical and electromagnetic portions of RF and microwave interconnect
- Identification of appropriate IC substrate and packaging materials for optimized transmission of RF and microwaves
- Full understanding of the power and design complexity trade-offs associated with this approach

## GUIDED TERAHERTZ WAVES AND PLASMONS

Terahertz waves [1] and plasmons [2] are hybrids of RF and optical signaling, using transmission frequencies from around $10^{12}$ Hz to optical. These are propagated through micro-stripline waveguides possibly built with Cu/low $\kappa$ or $SiO_2$. This approach is attractive because it provides the opportunity to extend significantly the bandwidth of interconnect systems without changing the material set. This technology may lend itself to smaller feature sizes than optical or RF and may be usable in intermediate interconnect layers.

### *CRITICAL CHALLENGES*

- High efficiency sources capable of monolithic integration into Si CMOS (at low cost)
- Low power terahertz or optical modulators that can be monolithically integrated into Si CMOS (at low cost)
- Low power, monolithically integrated into Si CMOS (at low cost) detectors of small feature size need to be developed. (The small terahertz detectors that are currently available are largely bolometric, and do not afford the bandwidth promised by the terahertz carrier.)
- A study of micro-stripline scalability to determine such parameters as impedance, losses, dispersion, mode stability, power handling capability, electrical reliability, "microstrip-to-microstrip crosstalk," and others, needs to be performed with a resulting set of design rules

## CARBON NANOTUBES

Carbon nanotubes have been proposed as solutions to many problems in various industries. Their high electrical and thermal conductivity, as well as their ability to be deposited in either metallic or semiconducting states, has attracted interest for possible applications in interconnect structures. The following section describes features of carbon nanotubes important to the interconnect application. This section is self-contained. The references are numbered in the section text and listed at the end of the chapter.

### *INTRODUCTION*

Carbon nanotubes (CNTs) are considered a potential solution to improve the performance of on-chip interconnects in terms of speed, power dissipation and reliability. Carbon nanotubes are rolls of graphene sheets, which are one atom thick carbon layers. CNTs have aroused major research interest in their applicability as very-large-scale integration (VLSI) interconnects for future generations of technology because of their desirable properties such as large electron mean free paths, mechanical strength, high thermal conductivity, and large current carrying capacity. As interconnect dimensions scale and copper resistivity increases due to size effects, CNT interconnects become more attractive.

CNTs can be either single-wall (SWCNT) or multi-wall (MWCNT). SWCNTs consist of only one graphene shell, and their diameter may vary from 0.4 nm to 4 nm with a typical diameter of 1.4 nm [1, 2]. MWCNTs consist of several concentric graphene cylinders, and their outer diameters may vary from a few to 100 nm [2, 3], and the spacing between the walls is 0.32 nm, the same as the spacing between graphene sheets in graphite [2]. Graphene cylinders, SWCNTs or shells forming MWCNTs, can be either metallic or semiconducting, depending on their geometrical structure (chirality). However, large diameter semiconductor shells (D >5 nm) have bandgaps comparable to or smaller than the thermal energy of electrons and act like conductors at room temperature [2–4].



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For bundles of SWCNTs, it has been proven experimentally and theoretically that increasing diameter always lowers conductivity [1, 5–7] . This is because the number of nanotubes decreases quadratically with increasing diameter whereas electron mean free path increases only linearly with diameter. For MWCNTs, theoretical models suggest that increasing diameter increases the conductivity of long MWCNTs while decreasing the conductivity of short MWCNTs [6]. These predictions have not yet been fully proven experimentally.

### ADVANTAGES OF CNTS

CNTs offer several advantages compared to Cu/low-κ interconnects because of their one dimensional nature, the peculiar band-structure of graphene, and the strong covalent bonds among carbon atoms:

#### 1. HIGHER CONDUCTIVITY (LOWER RESISTANCE):

Due to their one-dimensional nature, the phase space for electron scatterings in CNTs is quite limited, and electron mean free path is in the micron range for high quality nanotubes in contrast to 40 nm in bulk copper [8]. The conductivity of densely-packed CNTs is higher than Cu interconnects for large lengths. Conductivity of short CNT bundles, however, is limited by their quantum resistance, the minimum resistance of a quantum wire in the absence of reflections at the CNT-metal electrode interface or scattering along their length. Quantum resistance is a fundamental limit whose value depends on the number of conduction channels. Metallic SWCNTs have two conduction channels, and their quantum resistance is 6.5 kΩ [2, 9].

#### 2. RESISTANCE TO ELECTROMIGRATION:

The strong sp2 carbon bonds in graphene lead to an extraordinary mechanical strength and a very large current conduction capacity for CNTs; $10^9$ A/cm$^2$ in contrast to $10^6$ A/cm$^2$ in Cu before damage or breakdown of the material is observed. Current densities higher than $10^9$ A/cm$^2$ have also been reported for MWCNTs at high temperature conditions (250C) [10]. In practice, the maximum current density in CNT interconnects, however, may become limited by the contacts.

#### 3. THERMAL CONDUCTIVITY:

The longitudinal thermal conductivity of an isolated CNT is expected to be very high, on the order of 6000 W/mK, as suggested by theoretical models [11] and extrapolations on measured data from porous bundles [12]. From the experiments of CNT thermal and source bumps for flip-chip high power amplifiers [13], the thermal conductivity of MWCNTs exhibits 1400 W/mK, which is calculated using the experimentally obtained thermal resistance, an area of CNT bundle, and the site density of CNTs. For comparison, the thermal conductivity of Cu is 385 W/mK, and the thermal conductivity of diamond is 900-2300W/mK. The thermal conduction in CNTs is highly non-isotropic, and the transverse conduction is orders of magnitude lower than the longitudinal conduction.

### INTEGRATION OPTIONS

CNTs can potentially replace Cu/low-κ interconnects at most levels of interconnect hierarchy [13] except in places where low-resistance short interconnects are needed. For instance, to distribute power and ground in the first interconnect level, CNT interconnects would be significantly more resistive than minimum-size copper wires since nanotubes as short as the gate pitch would be needed. They can bring significant performance advantages when replacing the long global interconnects where the RC delay of interconnects is important. SWCNTs can be integrated for on-chip interconnect applications in the following forms:

#### 1. SWCNT-BUNDLES

A bundle of densely packed SWCNTs with the same dimensions as Cu/low-κ interconnects with high-quality contacts with the electrodes would be an ideal candidate for replacing Cu/low-κ interconnects to lower the interconnect resistance and address the problem of size effects in copper wires. This integration option provides significant delay improvements for long interconnects where the RC delay is dominant [1, 14–16].

#### 2. FEW-LAYER SWCNT INTERCONNECTS

A few-layer arrangement of SWCNTs can reduce the capacitance of the CNT-based interconnects by as large as 50% and can significantly decrease the electrostatic coupling between adjacent interconnects. This helps to reduce the delay and power dissipation of local interconnects. This arrangement is particularly interesting for short local interconnects where the delay is dominated by capacitive loading of interconnects and not their resistance [14].

#### 3. LARGE-DIAMETER MWCNTS


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It has been proven both theoretically and experimentally that all shells within MWCNTs can conduct if proper connections are made to all of them [3, 4, 17]. There are reports of very large mean free paths in high-quality MWCNTs [3, 18], and theoretical models suggest that long large-diameter MWCNTs can potentially outperform Cu and even SWCNTs if the level of disorder in these tubes can be kept as low as those in SWCNTs and all shells can be properly connected to metal contacts [6]. Such MWCNTs would be suitable for semi-global and global interconnects.

#### 4. GRAPHENE NANORIBBONS (GNR)

Graphene nanoribbons can be considered as unrolled CNTs. They share many of the fascinating properties of CNTs while conventional top-down lithography can be used to pattern them [19–23]. There may also be ways to control the chirality and hence their metallic or semiconductor nature[19]. If edges are not perfect, electrons can get scattered at the edges and the mean free path becomes a function of GNR width and propagation mode [19, 23]. This would be a disadvantage for GNRs compared to CNTs that have no edges.

### CHALLENGES

Initial research and predictive studies have shown a promising outlook towards a possible replacement of conventional Cu/low-κ technology by CNTs, but there are numerous technical challenges that remain to be addressed. The important challenges facing the CNT integration are the following:

#### 1. ACHIEVING A HIGH-DENSITY INTEGRATION WITH CNTS

CNT-bundles can outperform copper wires in terms of conductivity only if they are dense enough. While dispersed SWCNTs form dense regular arrays with constant 0.34 nm inter-tube spacing [24], in-place grown CNTs reported to date have been quite sparse. Table INTC7 gives the minimum densities of metallic SWCNTs required to outperform minimum-size copper wires in terms of conductivity. As technology advances and size effects become more severe for Cu wires, the required minimum density becomes smaller. The material and size of catalyst particles are the key parameters determining diameter and density of nanotubes.

The diameter of SWCNTs is assumed to be 1 nm, at which the phonon-limited electron mean free path is 1 μm at room temperature [25–27]. Contact resistance is assumed to be less than 10% of the intrinsic resistance of SWCNTs which means longer bundles can tolerate larger contact resistances. Ideal density for a densely-packed all-metallic bundle of SWCNTs with 1 nm diameter is 0.66 $nm^{-2}$.

*Table INTC7 Minimum Density of Metallic SWCNTs Needed to Exceed Minimum Cu Wire Conductivity*

| *Technology Year* | *2007* | *2008* | *2009* | *2010* | *2011* | *2012* | *2013* | *2014* | *2015* |
|---|---|---|---|---|---|---|---|---|---|
| *Wire Pitch (nm)* | **136** | **118** | **104** | **90** | **80** | **72** | **64** | **56** | **50** |
| *Cu Resistivity (μΩ-cm)* | **3.51** | **3.63** | **3.80** | **4.08** | **4.30** | **4.53** | **4.83** | **5.20** | **5.58** |
| *Minimum Density ($nm^{-2}$)* | **0.204** | **0.197** | **0.188** | **0.175** | **0.166** | **0.158** | **0.148** | **0.138** | **0.128** |

| *Technology Year* | *2016* | *2017* | *2018* | *2019* | *2020* | *2021* | *2022* |
|---|---|---|---|---|---|---|---|
| *Wire Pitch (nm)* | **44** | **40** | **36** | **32** | **28** | **26** | **22** |
| *Cu Resistivity (μΩ-cm)* | **6.01** | **6.33** | **6.70** | **7.34** | **8.19** | **8.51** | **9.84** |
| *Minimum Density ($nm^{-2}$)* | **0.119** | **0.113** | **0.107** | **0.097** | **0.087** | **0.084** | **0.073** |

#### 2. SELECTIVE GROWTH OF METALLIC SWCNTS

SWCNT growth processes developed to date have no control on chirality. Statistically, only one third of SWCNTs with random chirality are metallic [2]. Improving the ratio of metallic to semiconductor tubes would proportionally increase the conductivity of SWCNT-bundles. Semiconductor SWCNTs are not fatal for interconnect applications, and in contrast to transistor applications of CNTs, perfect control on chirality is not necessary.

#### 3. DIRECTIONAL GROWTH IN CNTS

At this time, a very challenging step is the growth of horizontal CNTs in a controlled way. The placement of catalysts on a vertical surface makes the horizontal growth much more challenging than the vertical growth. Some progress has however been made in this regard [28].

#### 4. ACHIEVING LOW-RESISTANCE CONTACTS



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The metal electrode contact with CNTs may cause reflection effects and cause contact resistance. These reflections occur due to inefficient coupling of the electron wavefunction from the electrode into the CNT. A promising close-to-ideal contact has been realized experimentally [4, 30]. But the large number of publications reporting large contact resistances indicates a technological challenge in making good contacts. Because of the weak inter-tube coupling between SWCNTs in a bundle [24] and also between shells inside MWCNTs [2, 17], direct connections between all graphene shells and metallic contacts are required. This is especially challenging for horizontal bundles. CMP for CNT bundles maybe the solution for this requirement [21, 31]

#### *5. Achieving Defect Free CNTs*

CNTs are very sensitive to adsorbed molecules. It is found that adsorbed molecules on the surface of CNTs affect the electrical resistance [18, 32]. This imposes additional technical challenges to produce CNTs with stable characteristics.

#### *6. Back-End-of-the-Line Compatible CNT Growth*

Most high-quality CNTs reported in the literature are grown at temperatures above 600°C which is not acceptable for the silicon technology. Promising progress is reported that involves the growth of CNTs at temperatures as low as 400°C [20]. However, defect density typically increases as growth temperature is lowered. Furthermore, CNT interconnects are unlikely to replace all copper interconnects. CNT interconnect fabrication technology, therefore, needs to be compatible with Cu/low-κ technology.

Although CNT interconnects have been separately shown to be promising, there have been few efforts to successfully combine them in realistic circuits. There are still several process and reliability related challenges that need to be addressed before CNT-based devices and interconnects can enter mainstream VLSI processing. This makes it an exciting and open field for research. Problems like purification, separation of carbon nanotubes; control over nanotube length; chirality and desired alignment; and low thermal budget as well as high quality contacts are yet to be fully resolved.

## Radical Solutions

In addition to the aforementioned options for global interconnect solutions, there are several more radical options that may offer unique advantages. These radical alternatives include such areas as molecular interconnects [1], spin coupling [2], and quantum waves.[3] These options are in their early stages of development, and have a common critical need for a total system concept that demonstrates their utility in the interconnect function as well as a manufacturing methodology for their fabrication. In addition, continuing research has uncovered new and unexpected features of some of these radical alternatives.[4] Although many important features of radical solutions to the interconnect problem have been realized, there is still a critical need for additional creative approaches that will provide the defined roadmap capabilities while meeting the difficult challenges of cost and manufacturability.

The discussions above have described several *new concepts and radical alternatives* for providing interconnect solutions compatible with the increasing requirements needed to continue the progression of IC technology. Although several independent approaches are described, it is expected that the solutions used will be different for different applications, and that the ultimate solutions may require a combination of several of the approaches described above. This realization makes it imperative that cross-functional research is emphasized to ensure that the best approaches using all of the possible techniques are fully evaluated.

Interconnect technology has been following an evolutionary path ever since its inception by Robert Noyce in his 1959 patent. Even the difficult transitions to Cu/low κ are relatively minor technology transitions in comparison to some of the disruptive technologies proposed above. There are many technology issues to be dealt with but before the industry will embrace a large investment to arrive at solutions, some strategic questions need to be addressed:


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1. How does the approach fit in the solution of the overall interconnect problem?
2. How much of the problem does it solve? (for which products?)
3. When will the technology be ready for implementation?
4. How does the capability of this technology match needs at the projected time of implementation?
5. How extendable or for how many generations will it provide benefit?
6. What other technologies will need to be developed to implement the solution effectively?
7. What changes in software, hardware, manufacturing, applications, or business will need to be in place to implement the solution effectively?
8. What technical problems need to be solved before implementation and what is their current state?
9. What needs to be done/added to provide the implementation on time?
10. How will the technology be transferred into the mainstream?

## CROSS-CUT CHALLENGES

### INTERCONNECT AND DESIGN AND MODELING AND SIMULATION

The interconnect performance needed for future technology generations can no longer be provided by material and technology improvements alone. Therefore the interaction between material science, wafer technology, design, and modeling and simulation is becoming of even greater importance in supporting continued interconnect scaling. Current interconnect design tools cannot accurately predict the performance of an entire multilevel interconnect system. Further, the models are largely based on RC not RLC parameters. Optimization of designs for maximum performance is often effected by a trial and error method. As frequencies and the number of interconnect layers increase, time to market of many leading edge parts is being impacted by the ability to lay out and chose the correct interconnect routing (function block placement, interconnect level and corollary line size) to achieve an overall device performance target. The design capability must be significantly expanded to allow users to utilize both the near term and far term proposed interconnect systems effectively. Specific upcoming interconnect challenges include:

1. RLC capable models will be needed for systems with 10 GHz and above operation. (30 GHz in free space wavelength is ~1 cm). This capability will also be needed for systems using RF or terahertz wave interconnections.
2. The impact of the Cu resistivity increase on delay time must be considered in realistic models. These models need to take into account linewidth, line aspect ratio, sidewall roughness, metal grain size, and the respective coefficients for grain boundary-, surface-, and impurity-scattering.
3. The impact of plasma-induced sidewall damage, and other non-idealities induced in the dielectrics by processing needs to be modeled.
4. Signal delay uncertainties because of crosstalk effects between neighboring interconnects and the impact of dummy metal features need to be considered in appropriate models. Because of increasing line aspect ratios these effects may become major issues.
5. Process variations (*e.g.,* CD tolerances, line height variations, sidewall roughness, etc.) will become of ever increasing importance with further shrinking of interconnect line and via sizes. Therefore variation tolerant designs and variation sensitive models and simulations are needed to support the upcoming technology generations.
6. A means to optimally place function blocks will be needed for the 3D integrated circuits not only on an individual die but also now on a stack of die.
7. New models must be developed to optimize optical interconnect systems that include emitter and detector latency.
8. All of the above technologies will increase the heat dissipation of the die as a whole and increase the number of occurrences of reliability critical "hot spots" within the die. Predictive thermal models, that can accommodate thermal impacts of low-κ dielectrics with reduced heat conductivity, RF standing waves, the multiple heat generating layers embedded in the 3D IC stack, and heat generated by, as well as thermal performance of optical devices and quantum well devices will be needed.

Modeling and simulation is a key tool to support all of the technology areas working with the interconnect problem. The required modeling and simulation capabilities range from high-level predictions of interconnect impact on IC layout and electrical behavior (such as signal delay, distortion, and interconnect reliability) to prediction of resistivity increase of further shrinking copper interconnects (due to grain structures, Cu/barrier interfaces, and impurities) and the physical structure and properties of new low−κ dielectrics and other more exotic interconnect materials.



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In all of these cases, modeling and simulation should provide predictions accurate enough to reduce as much as possible the need and costs of extensive experiments. These needs span from first simulations carried out to screen the field for well-directed experiments on new interconnect technologies and architectures to predictive capability within experimental error for relatively mature technologies.

As in many other fields of technology, the need in interconnects for modeling and simulation is increasing due to the larger number of parameters and effects to be included. For example, the introduction of low-κ dielectrics with low thermal conductivity is drastically increasing the need for combined thermal, mechanical, and electrical modeling (which in this issue of the roadmap has newly become one of the near-term challenges for modeling and simulation).

Specific interconnect needs for modeling and simulation include:

- Performance prediction (including high frequency effects and reliability) for complex (*e.g.,* 3D) structures fabricated with real non-idealized processes (etching, PVD, CMP), with hierarchical capability to choose the appropriate trade-off between speed and accuracy for the application in question;
- Tools and methodologies to connect product and process designs in an integrated flow to meet target specifications or identify deficiencies; and
- Materials modeling capabilities to predict structure as well as physical and electrical performance of materials used in interconnect structures (metal, barrier, and dielectric).

Especially important is the size-dependent resistivity of copper, its surface diffusion and electromigration, and copper thinning and dishing in CMP. See the *Modeling and Simulation* chapter.


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# 2007 ITRS INTERCONNECT APPENDIX

## *DIELECTRIC*

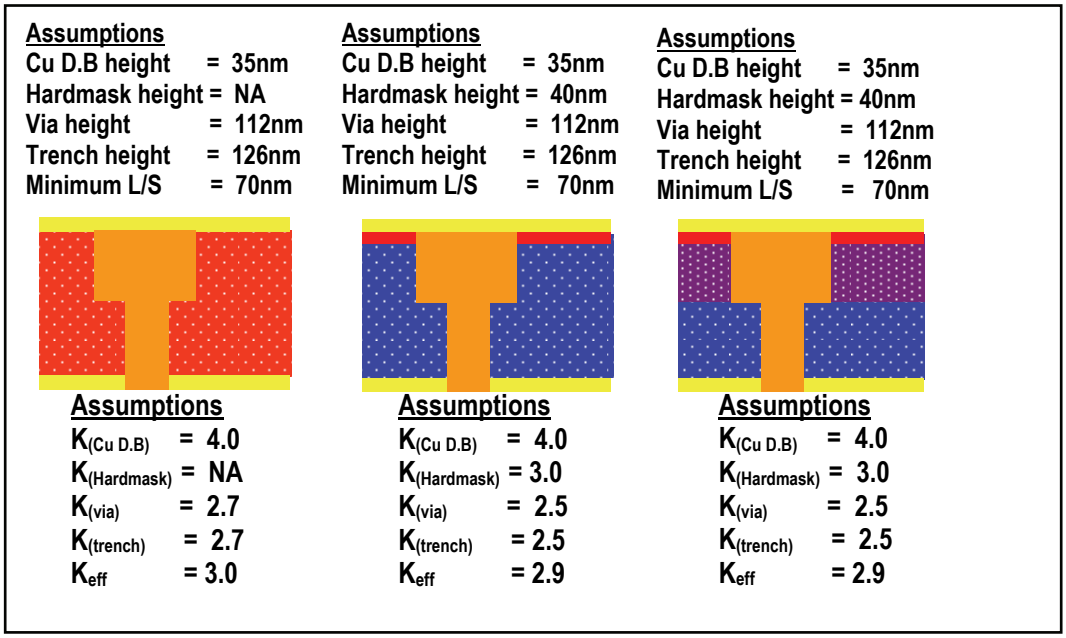


*Figure A1 65 nm Dielectric Potential Solutions (2007, 2008) Aggressive Case*

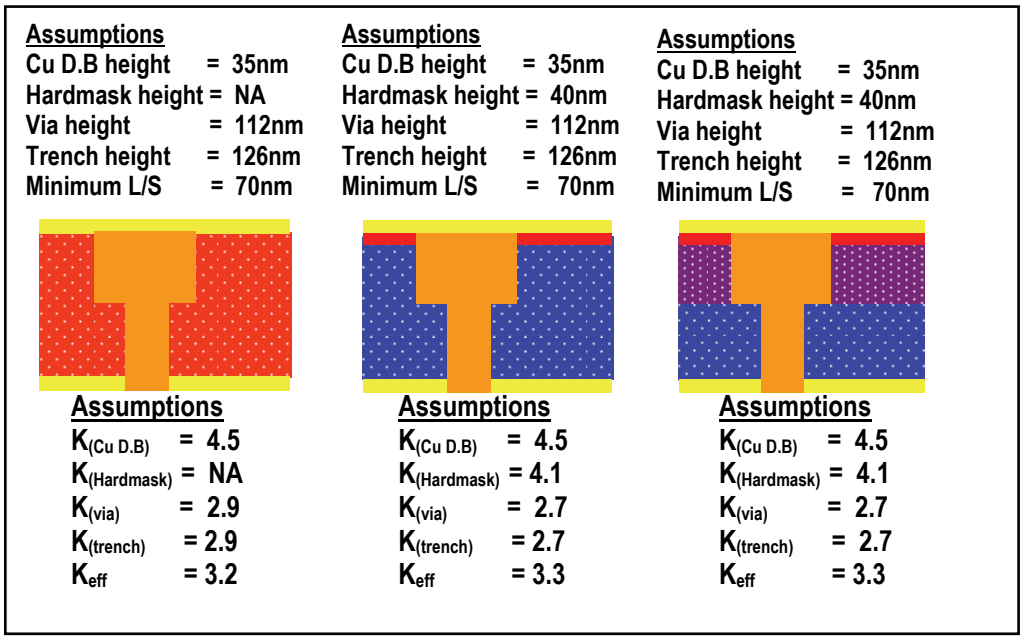


*Figure A2 65 nm Dielectric Potential Solutions (2007, 2008) Realistic Case*



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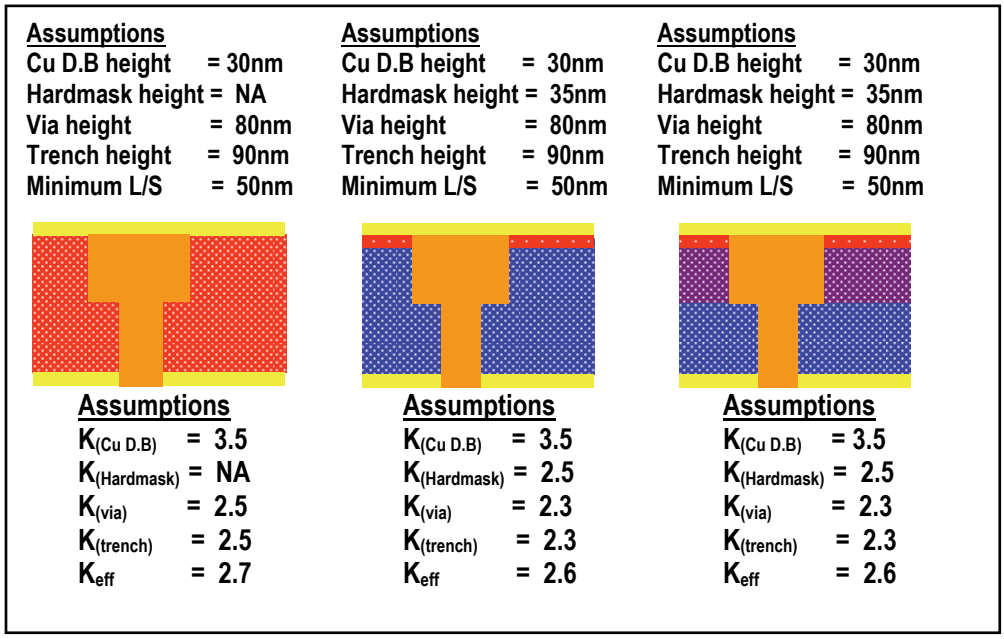


*Figure A3 45 nm Dielectric Potential Solutions (2009, 2010, 2011) Aggressive Case*

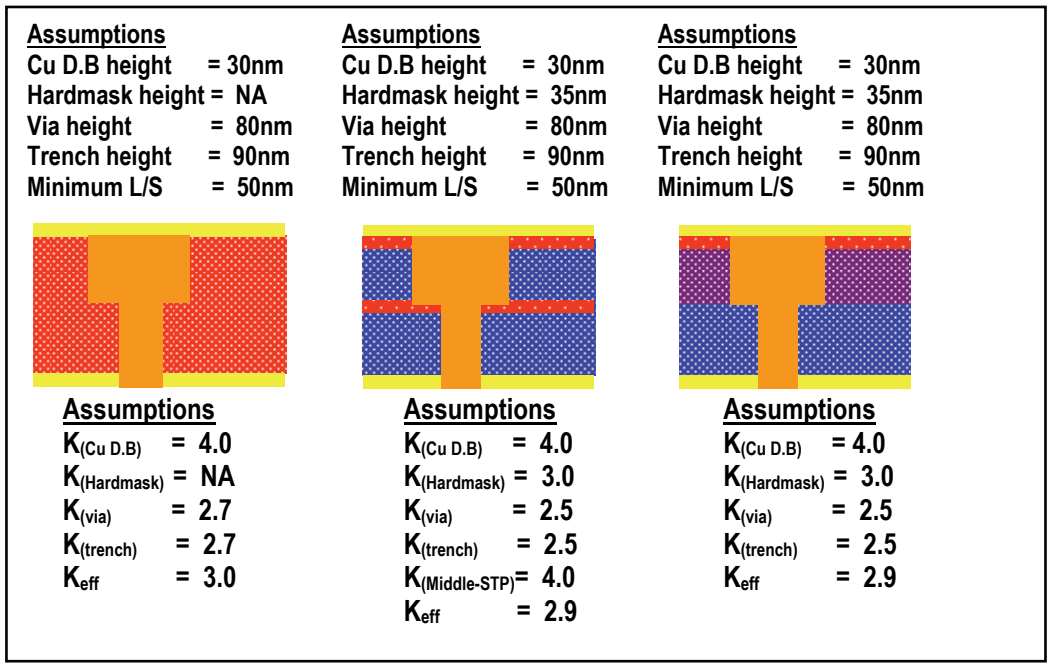


*Figure A4 45 nm Dielectric Potential Solutions (2009, 2010, 2011) Realistic Case*


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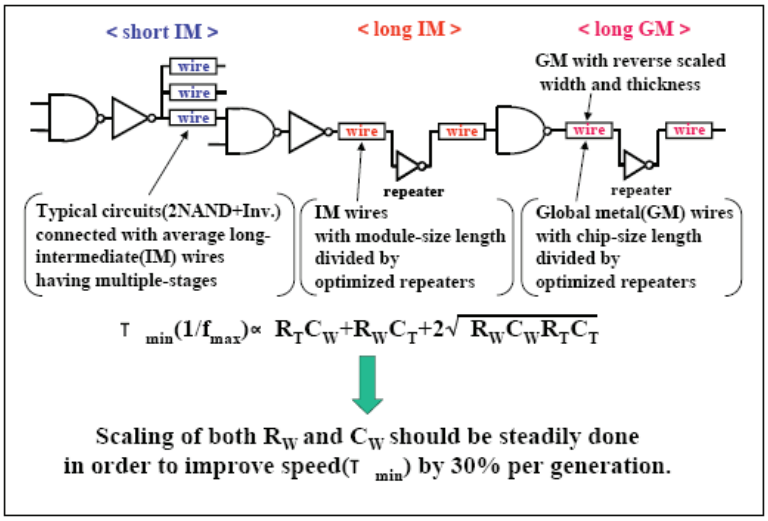


*Figure A5 Critical Path in High-End SOC and RC Scaling Scenario*

*Table A1 Assumption on Interconnect Parameter Estimation Model*

| | <Assumption on Interconnect parameter estimation> |
|---|---|
| Design rule | x0.70/node-scaling, Reverse-scaling for GM |
| Chip-size | Constant(=7mm sq) as 1-clock cycle limit |
| Module-size | Constant(=1mm sq) based on gate density increase |
| Repeater | Inserted for SGM and GM wires |
| Gate density | x2.0/node(based on ITRS2002 MPU-R.M) |
| Active power density | x0.6/node with average-long IM wire |
| Logic depth | x0.75/node-scaling |

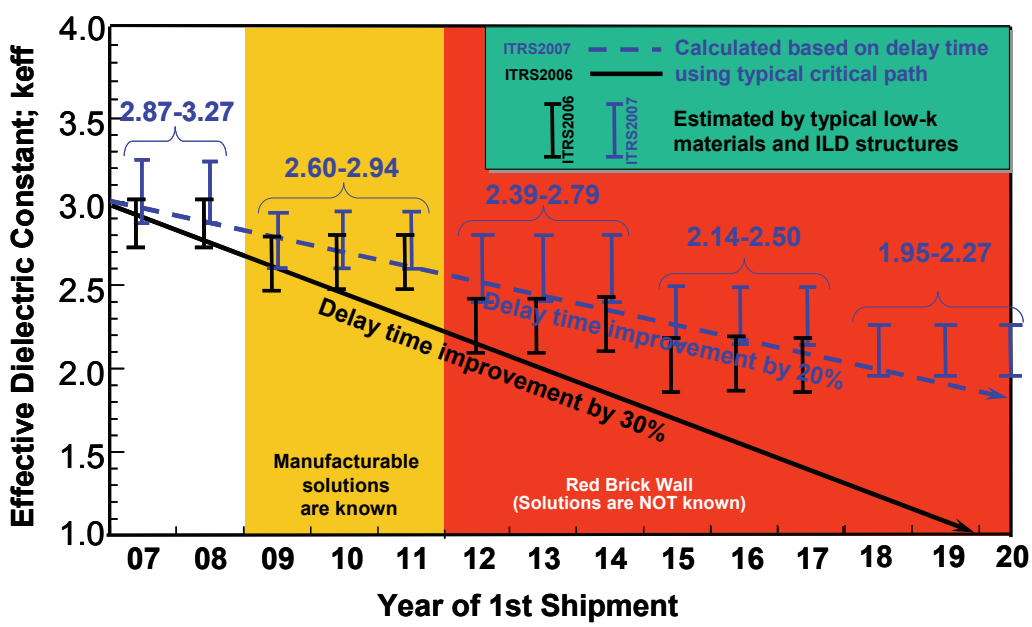


*Figure A6 ITRS 2007 $\kappa_{eff}$ Roadmap Revision*



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